BETA-GALLIUM OXIDE LATERAL FIELD-EFFECT TRANSISTORS: FABRICATION AND PERFORMANCE

A Thesis

Presented to the Faculty of the Graduate School

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In Partial Fulfillment of the Requirements for the Degree of

Master of Science

by

Yaoyao Long

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ABSTRACT

As a promising ultra-wide-bandgap semiconductor for high power devices, β-Ga_2O_3 is under broad research owning to its high breakdown field and melt-grown substrates availability. The lateral β-Ga_2O_3 power devices have received lots of attraction due to high-speed operation. In this work, the β-Ga_2O_3 lateral power devices have been researched from MOSFETs to FinFETs for superior performance. The threshold voltage modulation by fin width in β-Ga_2O_3 lateral fin transistors was demonstrated for the first time. Moreover, the advantage of fin geometry in mitigating the high interface trap density on the top surface of (0 1 0) β-Ga_2O_3 was also shown in this research. Besides, the β-Ga_2O_3 fin dry etching has been studied to optimize the FinFET performance. Factors impacting the fin waist narrowing, including the thermal paste, in fin waist narrowing of β-Ga_2O_3 dry etching were discussed for the first time.

BIOGRAPHICAL SKETCH

Yaoyao (Emma) Long was born in China as the only child of Yue Zhang, a talented and great virologist and hematologist, on May 14th, 1996. She believed she liked science and engineering and went to The Ohio State University, majoring in Materials Science and Engineering. Emma received her Cum Ladue Honor Bachelor of Science degree in Materials Science and Engineering from The Ohio State University in May 2019. Then, she was accepted to Cornell University and continued studying Materials Science and Engineering the following fall. In her journey at Cornell, she focused her research on wide bandgap semiconductors. Emma is expected to receive her Master of Science degree in Materials Science and Engineering from Cornell University in August 2021. Right after, she will join Georgia Institution of Technology and start her Doctor of Philosophy in Electronic and Computer Engineering, focusing on MEMS.

Publication

- Wenshen Li, Devansh Saraswat, Yaoyao (Emma) Long, Kazuki Nomoto, Debdeep Jena, and Huili Grace Xing, Near-ideal reverse leakage current and practical maximum electric field in β-Ga_2O_3 Schottky barrier diodes, Appl. Phys. Lett. 116, 192101 (2020); DOI: 10.1063/5.0007715

Patent

- Kathleen Smith, Yaoyao (Emma) Long, Kazuki Nomoto, Wenshen Li, Debdeep Jena, and Huili Grace Xing, Gallium Oxide (Ga_2O_3) Lateral MOSFET for High Power RF with a Tall Fin Geometry, in submission to US patent

Conference Presentations

- Wenshen Li, Devansh Saraswat, Yaoyao (Emma) Long, Kazuki Nomoto, Debdeep Jena, and Huili Grace Xing, Observation of Near-Ideal Reverse Leakage Current in β-Ga_2O_3 Schottky Barrier Diodes and Its Implications for High Electric-Field Operation, 62nd Electronic Materials Conference (EMC), June 2020
- Kathleen Smith, Yaoyao (Emma) Long, Wenshen Li, Kazuki Nomoto, Mingli Gong, Debdeep Jena, and Huili Grace Xing, Single and Multi-fin Normally-Off Lateral β-Ga_2O_3 Transistors on (010) Ga_2O_3 substrates with Threshold Voltage Modulation by Fin Width Design, 51st IEEE Semiconductor Interface Specialists Conference (SISC), December 2020
- Yaoyao (Emma) Long, Kathleen Smith, Wenshen Li, Kazuki Nomoto, Debdeep Jena, and Huili Grace Xing, β-Ga_2O_3 Lateral FinFETs Fabrication and Preliminary Devices Performance, Cornell Nanoscale Science and Technology Facility 2020 Annual Meeting, September 2020
- Yaoyao (Emma) Long, Wenshen Li, Mingli Gong, Kathleen Smith, Kazuki Nomoto, Xiang Li, David Lishan, Debdeep Jena, and Huili Grace Xing, Fin-Waist Formation in β-Ga_2O_3 Fin Arrays Defined by ICP-RIE, 63rd Electronic Materials Conference (EMC), June 2021

- Kathleen Smith, Yaoyao (Emma) Long, Kazuki Nomoto, Debdeep Jena, and Huili Grace Xing, Fundamental Limits of Lateral Ohmic Resistance, Lester Eastman Conference on High-Performance Devices (LEC) 2021, August 2021

To my family and friends

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My sincere thanks also go to Dr. David Lishan. As one of the top experts in etching, Dr. Lishan can provide me with the vale suggestions and insights during my etch study. Also, as a good friend of mine, Dr. Lishan always provides me his warmest and generous encouragement during a hard time, both research and lifetime.

I am also very grateful to my mentors, Dr. Wenshen Li, Dr. Austin Hickman, and Dr. Kazuki Nomoto. They not only have taught me lab and research skills but also mentally supported me along with my master's journal. Without their generous help, I cannot fit into this group and these new research areas quickly, let alone joining the conferences and presenting my achievements there.

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1 Introduction and Motivation

In more than 70-year history of semiconductors, silicon, with 1.1 eV bandgap energy (E_g), is in a dominant stage for a long time, and it still has a significant market share nowadays. However, with the higher and higher demand on the voltage-handling capability, scaling with the critical electrical field (E_c), the wide bandgap semiconductor (E_g>3 eV) and ultra-wide bandgap semiconductors are under the spotlight of research, such as silicon carbide (SiC), gallium nitride (GaN), Diamond, gallium oxides(Ga_2O_3), etc. [1-3]. This study will focus on the gallium oxides lateral structure devices and the fabrication process optimization.

1.1 Beta-Gallium Oxides (β-Ga_2O_3)

Gallium oxide is an optically transparent and electrically conducting material, which enable gallium oxide an excellent candidate both in optical and electrical applications [4]. Gallium oxides have five commonly identified polymorphs, including α (corundum), β (monoclinic), γ (defective spinel), δ (orthorhombic), ε (generally accepted as orthorhombic) phases [5-12]. Among these phases, monoclinic structured β-Ga_2O_3 is the most stable polymorph. Our group has been working on gallium oxide devices and made significant progress [13-22]. Therefore, this study will mainly focus on the topics mentioned before using β-Ga_2O_3.

As the most stable phase, the β-Ga_2O_3 has the monoclinic structure, with the lattice parameter, a=12.23 Å, b=3.04 Å, c=5.80 Å, α=γ=90°, β=103.8° [12]. The crystal structure of β-Ga_2O_3 is shown in figure 1.1-1, where there are two crystallographically

different Ga atoms, including tetrahedral and octahedral coordination geometries [23, 24]. This asymmetry leads to physical, optical, and electrical anisotropy [23, 24]. The thermal conductivity along the [010] direction (29W/mK at 25℃) is around 2.5 times higher than the one along the [100] direction (11W/mK at 25℃) [25-27]. Moreover, the β-Ga_2O_3 has an ultrawide bandgap at the range of 4.5-4.7 eV [28, 29] and a very high breakdown field (critical electric field) at 8 MV/cm [30].

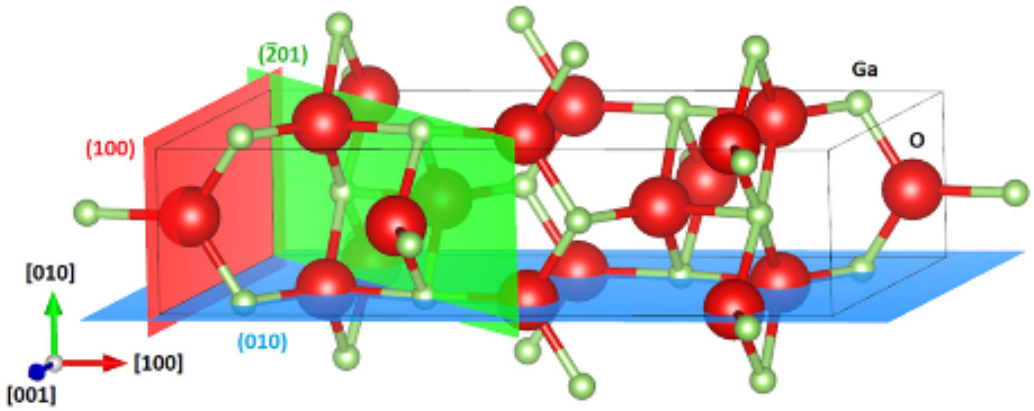


Figure 1.1-1 β-Ga_2O_3 crystal structure [31].

There are three commonly used planes, (1 0 0), (0 1 0), and ($\bar{2}$ 0 1). (1 0 0) plane contains only O atoms, which is a strong cleavage plane, shown in (figure 1.1-2a). (0 1 0) plane is a non-cleavage plane, where there are all types of Ga and O atoms, shown in (figure 1.1-2b). Meanwhile, ($\bar{2}$ 0 1) plane consists exclusively of octahedrally bonded Ga atoms [4, 31], shown in (figure 1.1-2c). In this study, the samples covered all three planes.

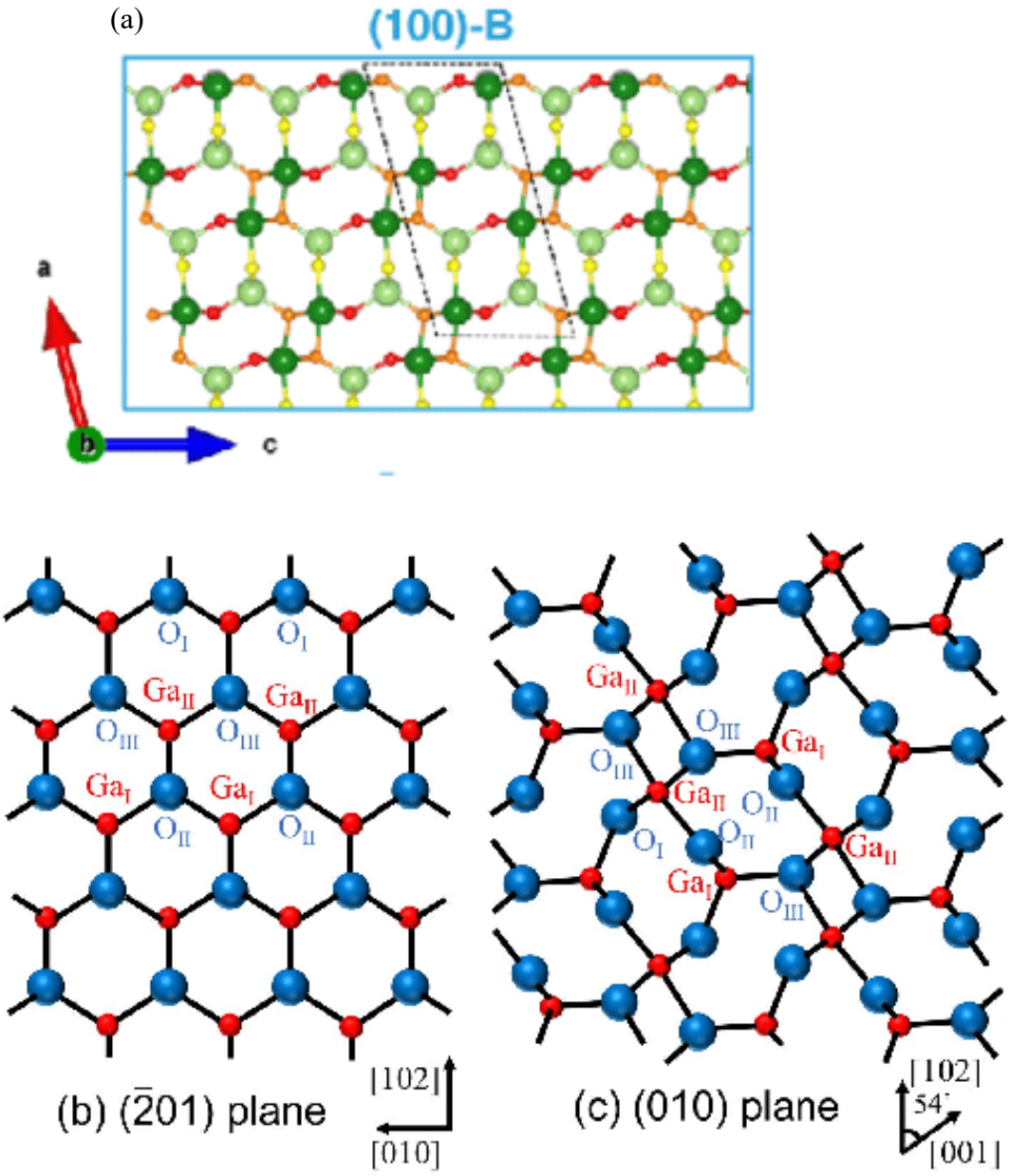


Figure 1.1-2 β-Ga_2O_3 (a) (1 0 0) [32], (b) ($\bar{2}$ 0 1) [31], and (c) (0 1 0) planes [31].

Besides these distinguished properties, the melt-growth techniques are available for β-Ga_2O_3, which enables up to 6-inch substrates production with well-controlled dislocation density less than 10^4 cm^{-2} [30]. In addition, the controllable n-type doing of β-Ga_2O_3 is also available by halide vapor phase epitaxy (HVPE), metalorganic chemical vapor deposition (MOCVD), mist chemical vapor deposition

(Mist-CVD), or molecular beam epitaxy (MBE) [4]. The n-type doping concentration is in the range of 10^{15}-10^{18} cm^{-3} [4]. With these advantages, the β-Ga_2O_3 substrate can be massively produced.

Moreover, with the ultrahigh bandgap, β-Ga_2O_3 is able to have the very high unipolar figure-of-merit (FOM), around four times larger than gallium nitride (GaN) (table 1.1-1). This high FOM enables β-Ga_2O_3 really low conduction loss [18], shown in (figure 1.1-3).

	Si	4H-SiC	GaN	β-Ga_2O_3
Band Gap (eV)	1.1	3.3	3.4	4.5-4.7
Breakdown Field, E_c (MV/cm)	0.3	2.5	2.8	6-8
Mobility, μ_e ($cm^2/V{\cdot}s$)	1400	1000	1500	200
Baliga's FOM	1	340	660	1000-2300

Table 1.1-1 The properties of β-Ga_2O_3 relative to other common semiconductors [18].

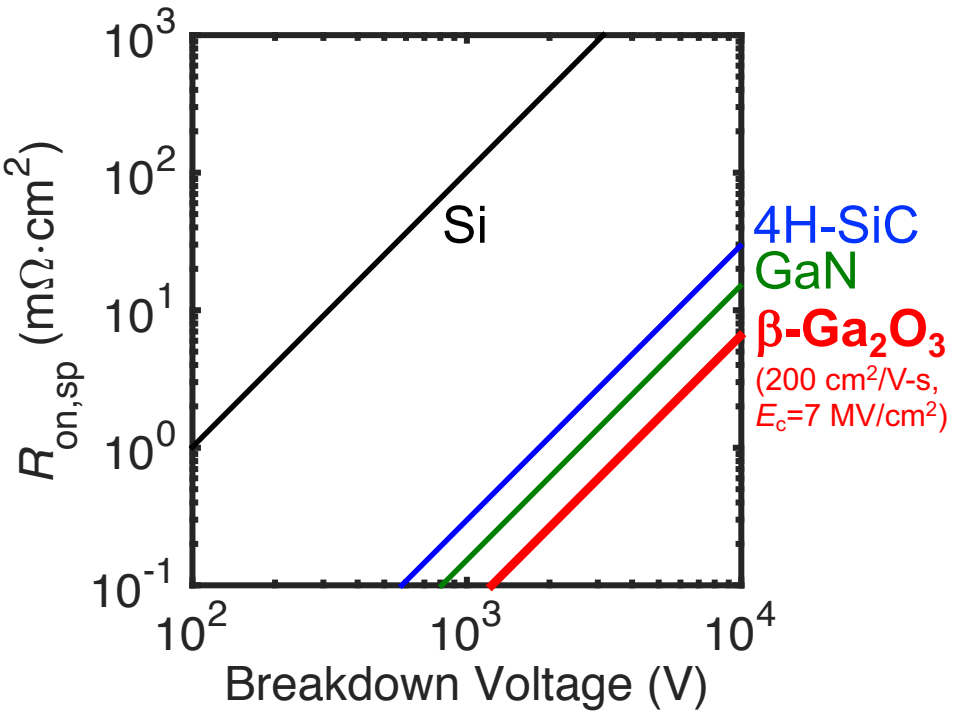


Figure 1.1-3 The unipolar material limit as calculated from Balliga's FOM, the left bottom corner is the desired corner. [18]

1.2 Lateral Structure Devices (Field-Effect Transistor)

Although, the vertical structure has the advantages in achieving higher current power devices. Lateral structure devices have better performance in high switch speed applications. Moreover, comparing to vertical structure devices, lateral structure devices are generally simple to be fabricated, considering the implemented field-shaping features on the wafer surface and the typical applications of buried layers and sinkers. As the common form in lateral structure devices, metal oxide semiconductor field-effect transistor (MOSFET) was first investigated. Then for better performance, fin field-effect transistor (FinFET) was researched in this study.

2 All-Cornell β-Ga_2O_3 MOSFETs

2.1 Motivation

With the advantages of β-Ga_2O_3 and lateral structure devices mentioned in the introduction, the basic structure of lateral structure devices, MOSFET, was considered the first attempt. Additionally, due to the advantage in growing high purity epitaxial thin film, the molecular beam epitaxy (MBE) was considered to provide a high-quality β-Ga_2O_3 sample to start with.

2.2 Sample Information

The MOSFETs were fabricated on the (0 1 0) β-Ga_2O_3 sample, which is grown by Nicholas Tanen using MBE at 500°C. The Ge doped layer is 104 nm thick with the n-type doping concentration at 1.7E18 cm^3. Right below the channel layer, there is an unintended doped (UID) layer with the thickness at 144 nm, shown in (figure 2.2-1). Overall, the fabricated sample is a small irregular shape (circled in figure 2.2-2) and sample ID at 180315Nta.

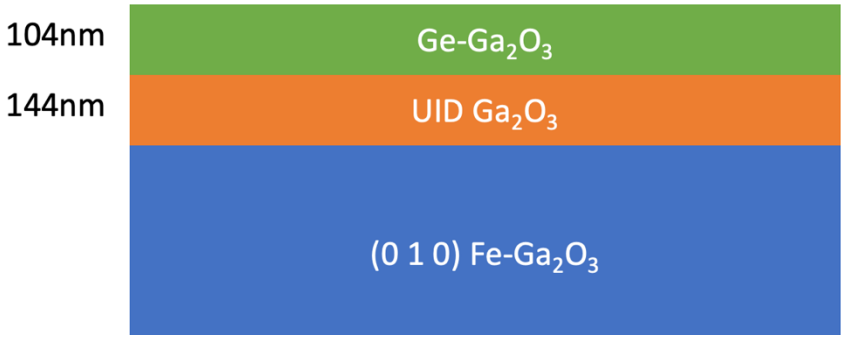


Figure 2.2-1 (0 1 0) β-Ga_2O_3 FET structure with a 104 nm thick Ge doped channel layer, with a doping concentration at 1.7E18 cm^{-3}, on top of a 144 nm thick UID layer grown on a semi-insulating bulk substrate.

Figure 2.2-2 β-Ga_2O_3 sample structure overall look, fabricated part circled in red.

This sample has Hall mobility at 55.5 cm^2/V-s and an estimated volume carrier concentration at 1.8E13 cm^{-3}, which shows the sample has decent electric properties. By atomic force microscopy (AFM), the sample has a smooth surface, shown in (figure 2.2-3), with the root mean square (RMS) of surface roughness at 0.52 nm at 2x2 μm area (figure 2.2-3a) and 0.62 nm at 10 X 10 μm area (figure 2.2-3b).

(a) (b)

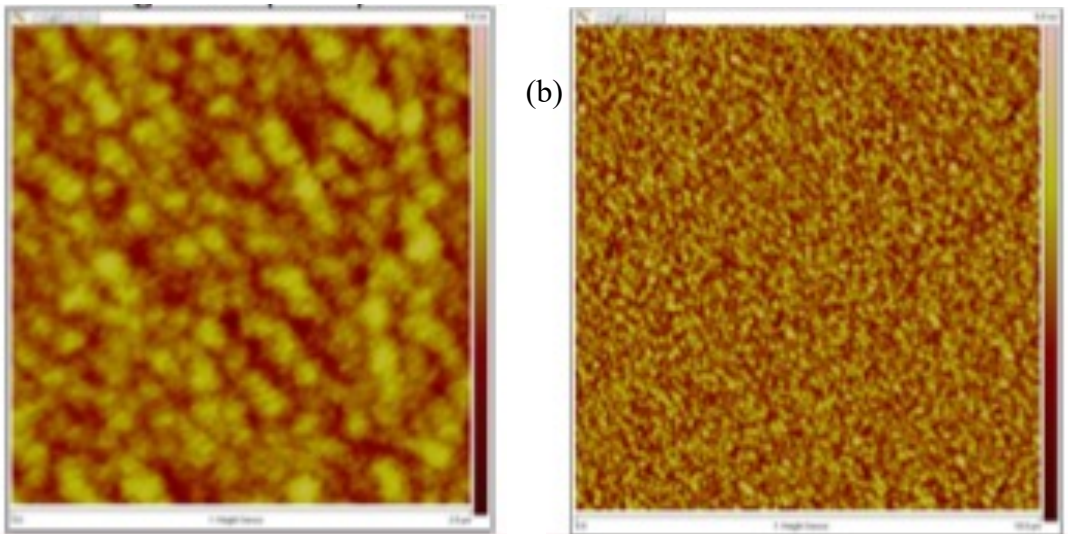


Figure 2.2-3 The AFM images of β-Ga_2O_3 sample surface. RMS of surface roughness (a) 0.52 nm at 2x2 μm area, (b) 0.62 nm at 10 X 10 μm area.

2.3 Device Fabrication Process

In this MOSFET structure, the source and drain contacts were made with Ti and Au, the thickness of which is 50/110 nm, and the gate was made with Ni/Au, the thickness of which is 50/100 nm. The dielectric layer was made with 19/1 nm thick Al_2O_3/SiO_2. The combination of these oxides can enable the MOSFET with low leakage. The drain to source distance is designed to be 13 μm, and the gate length is 10 μm with the FET8 mask series. The device structure is shown in figure 2.3-1b.

The MOSFET was fabricated following the process flow shown in figure 2.3-1a. The sample was first dry-etched for device isolation, then deposited source and drain metal by electron beam evaporation. The source and drain metal contacts were then annealed by rapid thermal anneal (RTA). The transmission line measurements (TLM) show the source and drain contacts are decently ohmic, with a contact resistance (R_c) at 18.68 Ωmm, shown in (figure 2.3-2). The dielectric layer was deposited by atomic layer deposition (ALD), and the thickness was confirmed by a spectroscopic ellipsometer. The gate metal was also deposited by electron beam evaporation. Finally, the drain and source contact holes were opened by the HF timed wet etching.

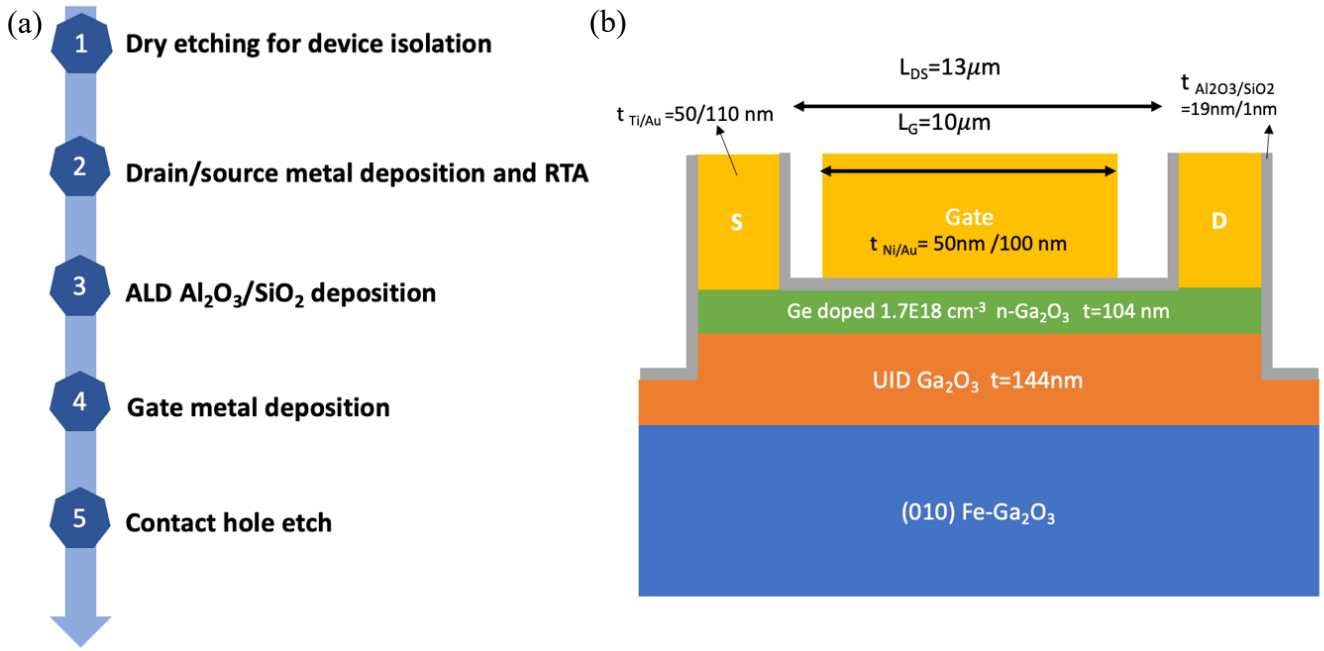


Figure 2.3-1 The device structure and fabrication process flow of all-Cornell β-Ga_2O_3 MOSFETs. (a) Fabrication process flow, (b) device structure.

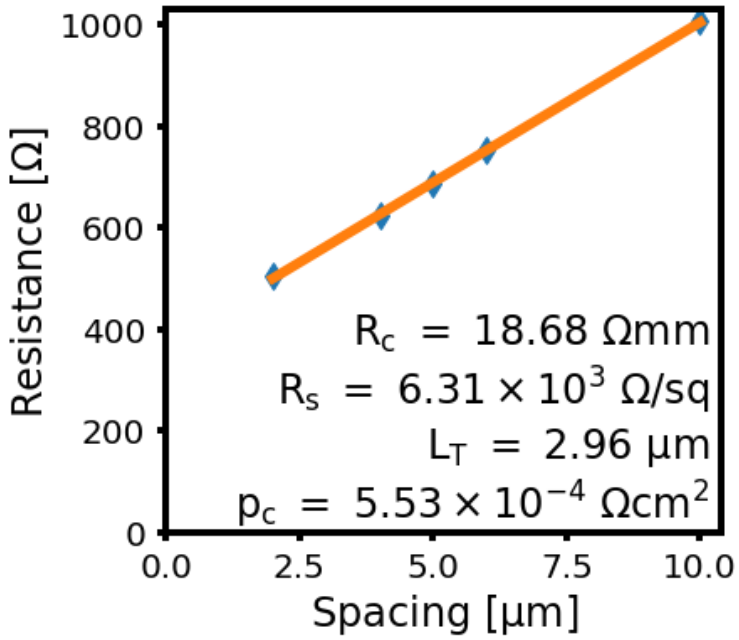


Figure 2.3-2 TLM result of the drain and source of all-Cornell β-Ga_2O_3 MOSFETs, which shows the drain and source contacts are ohmic.

2.4 Devices Performance

After measurement on Cascade probe station, from figure 2.4-1, the MOSFET operated in depletion mode with the threshold voltage at -10.9 V, which is close to the theoretical value at -9.4 V, obtained using the Equation 2.4-1,

Equation 2.4-1

$$V_T = V_{FB} - |2\phi_F| - \frac{\sqrt{2\varepsilon_s q N_d (|2\phi_F| - V_{SB})}}{C_{ox}}$$

where V_{FB} is flatband voltage given by Equation 2.4-2,

Equation 2.4-2

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{x_{ox}} \rho_{ox}(x) dx$$

with work function difference between metal and semiconductor, given by Equation 2.4-3,

Equation 2.4-3

$$\phi_{MS} = \phi_M - \phi_S = \phi_M - \left(\chi + \frac{E_g}{2q} - |\phi_F|\right)$$

And ϕ_F given by Equation 2.4-4, for p-type MOSFET, n-type substrate in this case.

Equation 2.4-4

$$|\phi_F| = V_t \ln \frac{N_d}{n_i}$$

In this threshold estimation, many parameters were neglected, including the fixed charge, interface charge, trap, etc. Additionally, the inaccurate value of electron affinity of Ga_2O_3 and work function of the metal gate could be the reason for the difference between the calculated value and measured value.

From figure 2.4-1b, the on and off current ratio is about 10^6, which shows the gate has outstanding control. The gate current is about 10^{-8} mA/mm, which shows excellent leakage control.

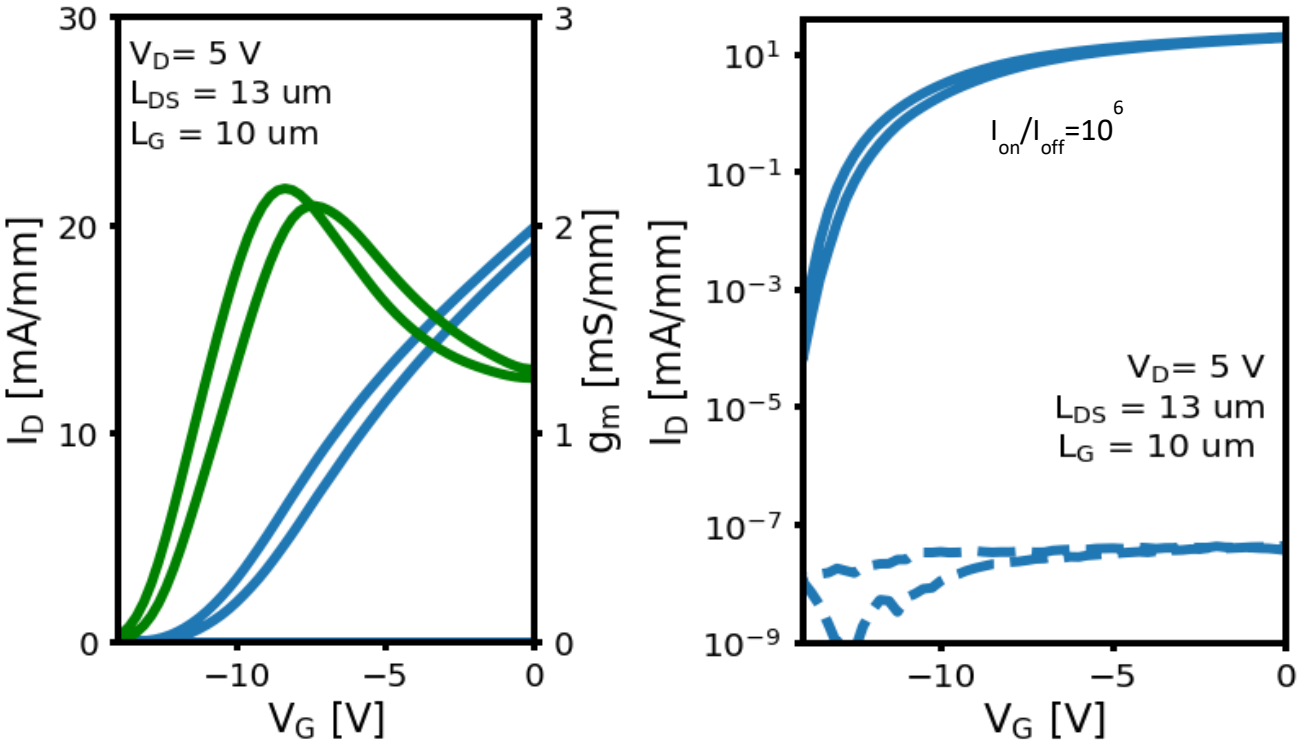


Figure 2.4-1 Transfer curve of the all-Cornell β-Ga_2O_3 MOSFET (a) at linear scale, (b) at log scale.

According to figure 2.4-1 and Equation 2.4-5, in the linear region, the field-effect mobility is around 11 cm^2/V-s, which shows the MOSFET has decent carrier mobility.

Equation 2.4-5

$$\mu_{FE} = \frac{L * g_m}{W * C_{ox} * V_{DS}};\ g_m = \frac{\partial I_D}{\partial V_G}$$

In figure 2.4-2, the family curve (output characterization) shows the MOSFET has a great on-resistance, as low as 278.2 Ω·mm (36.2 mΩ·cm^2).

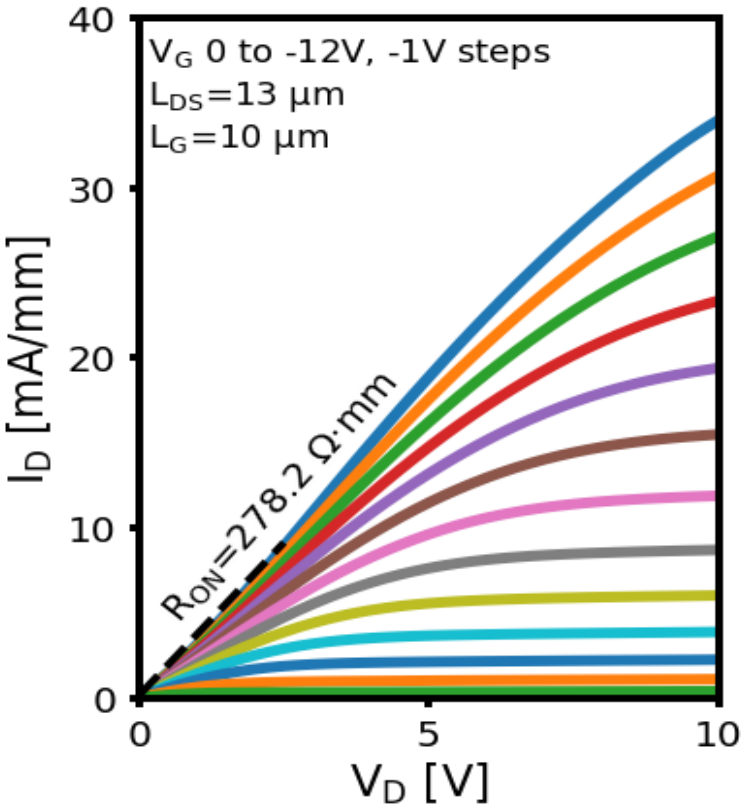


Figure 2.4-2 Family curve (output characterization) of the all-Cornell β-Ga_2O_3 MOSFET.

2.5 Conclusion

Overall speaking, the all-Cornell β-Ga_2O_3 MOSFETs have shown a remarkable performance, which means the success in both high-quality β-Ga_2O_3 sample MBE growing and the hereditable fabrication process flow designing. However, an enhancement-mode operation is still the goal for future lateral structure field-effect transistors. Therefore, with the experience of making MOSFETs, the FinFETs

structure will be discussed in the next chapter, which achieved an enhancement mode operation.

3 β-Ga_2O_3 FinFETs

3.1 Motivation

With the success of the all-Cornell β-Ga_2O_3 MOSFETs, a better performance β -Ga_2O_3 lateral device is demanded. Comparing to MOSFET in lateral structures, FinFET structure is more suitable for high-power, high-speed operation. For a given device footprint, the current increases with a taller fin and without sacrificing enhancement-mode operation. Furthermore, due to the larger interface between the active device region and substrate wafer surface, FinFET is favorable for thermal management.

3.2 Sample Information

The FinFETs were fabricated on the (0 1 0) β-Ga_2O_3 sample, grown by Thaddeus (Tadj) Asel from AFRL on MBE at 900°C. The channel layer is 200nm thick Si doped β-Ga_2O_3, with a doping concentration at 2E18 cm^3, shown in (figure 3.2-1). Overall, the sample is 10 mm long, 7.5 mm wide, and sample ID at EFEB30131, shown in (figure 3.2-2).

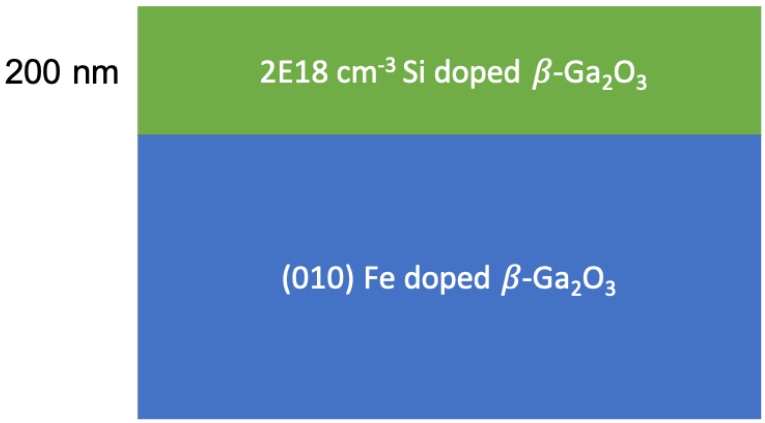


Figure 3.2-1 (0 1 0) β-Ga_2O_3 sample structure, a 200 nm thick Si doped channel layer, with a doping concentration at 2E18 cm^{-3}.

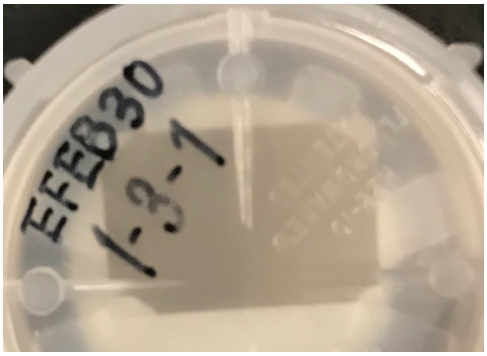


Figure 3.2-2 β-Ga_2O_3 sample overall look.

By the Hall measurement, this sample has Hall mobility at 81.8 cm^2/V-s, estimated volume carrier concentration at 3.0E18 cm^{-3}, which shows the sample has good electric properties. By atomic force microscopy (AFM), the sample has a smooth surface, shown in (figure 3.2-3), with the root mean square (RMS) of surface roughness at 0.44 nm at 2x2 μm area (figure 3.2-3a) and 2.1 nm at 10 X 10 μm area (figure 3.2-3b).

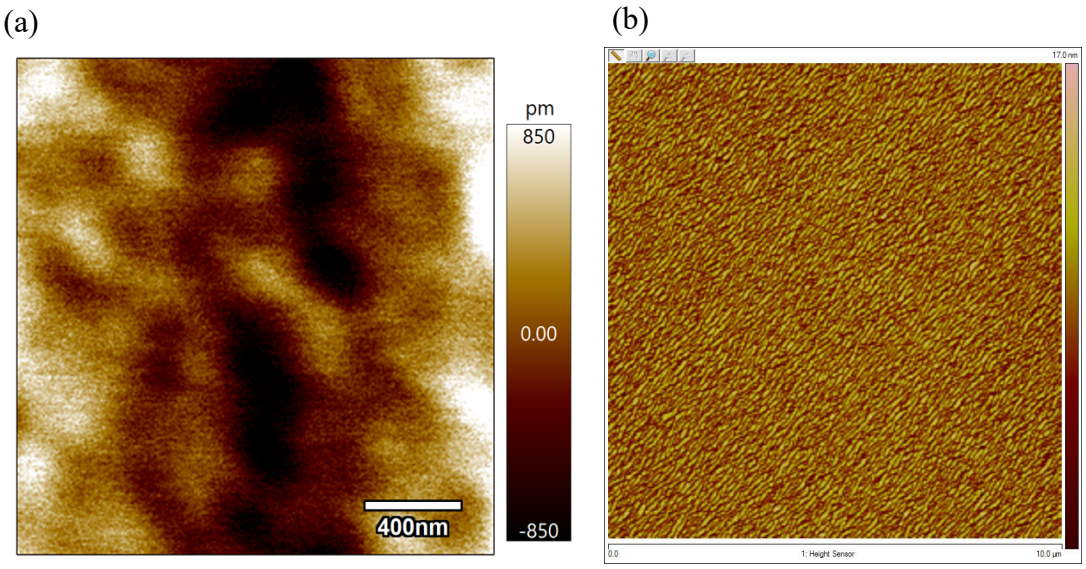


Figure 3.2-3 The AFM images of β-Ga_2O_3 sample surface. RMS of surface roughness (a) 0.44 nm at 2x2 μm area, (b) 2.1 nm at 10 X 10 μm area.

3.3 Determination of Fin Widths

One of the essential features of FinFET is that the gate is able to control the channel depletion by both top and side surfaces. Comparing to the planar MOSFET, where the top gate surface entirely controls the channel depletion, the FinFET structure has a better gate control. As the fin width decreasing, the channel depletion can be entirely controlled by the side gate surface, which has a lower interface charge density, shown in (figure 3.3-1). Meanwhile, the threshold voltage can generally move from the negative to the positive side, and the device can achieve the enhancement mode operation.

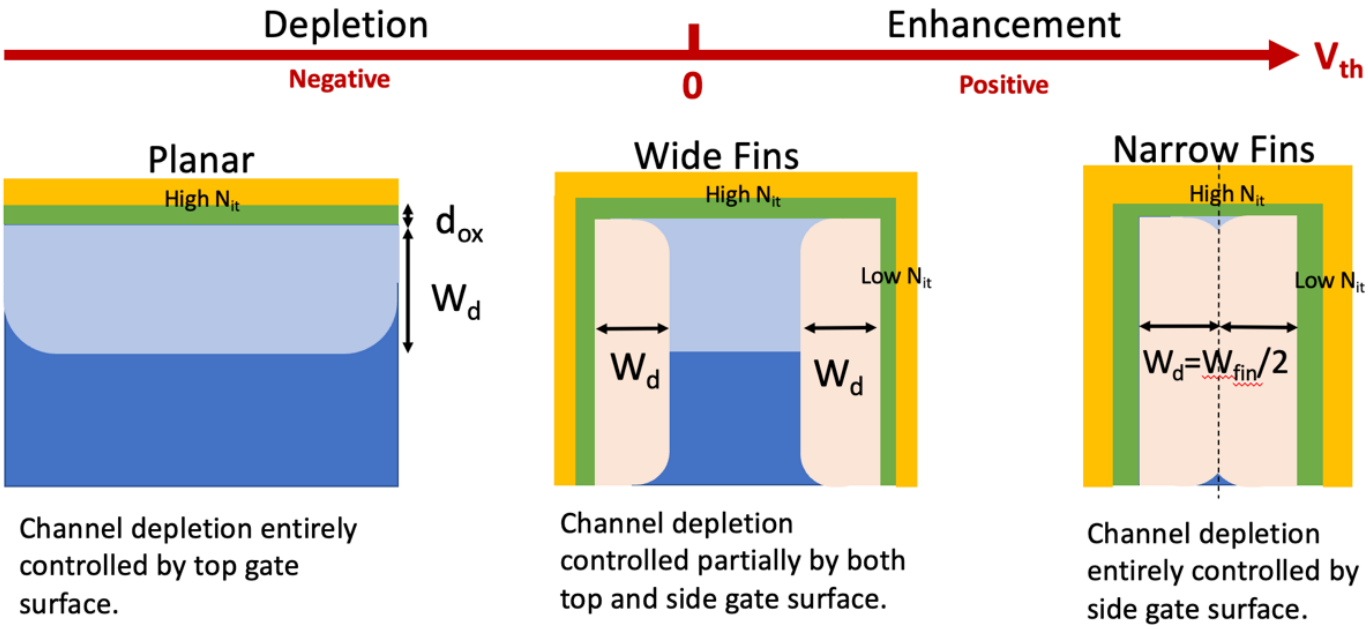


Figure 3.3-1 The reason of the FinFET operation moving from depletion mode to enhancement mode, made by Kathleen Smith.

Based on the threshold voltage equation of planar MOSFET (Equation 3.3-1), the threshold voltage equation of FinFET (channel depletion entirely controlled by side gate surface) can be generated, shown in (Equation 3.3-2). According to this equation, the estimated enhancement-mode transition will happen in the fin width at 50 nm. Thus, the fin width range is designed between 50 nm and 400 nm.

Equation 3.3-1

$$V_{th} = V_{FB} - \left(\frac{qW_d{}^2 N_d}{2\varepsilon_s} + \frac{qW_d N_d d_{ox}}{\varepsilon_{ox}}\right) - \frac{Q_{it}(\varphi_s) d_{ox}}{\varepsilon_{ox}}$$

Equation 3.3-2

$$V_{th} = V_{FB} - \left(\frac{qW_{fin}{}^2 N_d}{8\varepsilon_s} + \frac{qW_{fin} N_d d_{ox}}{2\varepsilon_{ox}}\right) - \frac{Q_{it}(\varphi_s) d_{ox}}{\varepsilon_{ox}}$$

3.4 Devices Structure and Fabrication Process Design

In this FinFET structure, the source and drain were made with Ti and Au, the thickness of which is 50/110 nm, and the gate was made with Ni/Au, the thickness of which is 50/100 nm. The dielectric layer was made with 20/2 nm thick Al_2O_3/SiO_2. Like the combination in MOSFET, these high K (dielectric constant) oxides can enable the FinFET with low leakage. The drain to source distance is designed at 7.5 μm, and the gate length is 1.5 μm. The fin width is at the range of 50nm to 400nm. The device structure is shown in (figure 3.4-1b).

To achieve this structure, the sample was fabricated in the process flow, based on the process flow of MOSFETs, shown in (figure 3.4-1a). First, the sample was dry-etched for device isolation, then deposited the Ni as fin recess etching hard mask by E-beam enhanced PVD. The fin dimensions were defined by electron beam lithography (EBL) and ion milling on Ni hard mask considering the fin size range at nm scale. Then the fin arrays were generated by dry etching at 350 W ICP power, 20 W RIE power, 5 mTorr, 20℃ with 35 sccm BCl_3 and 5 sccm Ar. Prior to SEM, the etched samples were soaked in HF for 10min to remove etch damage/residue. After removing the metal hard mask, the source and drain metals were deposited by E-beam enhanced PVD. The source and drain metal were then annealed by RTA, the same as MOSFET. After transmission line measuring (TLM), the drain and source have shown an ohmic contact performance, with the average contact resistance (R_c) at 14 Ωmm, shown in (figure 3.4-2). The dielectric layer was deposited by atomic layer deposition (ALD), and the thickness was confirmed by spectroscopic ellipsometer. The gate metal was also deposited by rotated E-beam enhanced PVD. Finally, the drain and source contact

holes were opened by the HF timed wet etching. Additionally, in order to decrease the contact resistance of source and drain, the post-deposition annealing (PDA) was applied with RTA, and the average contact resistance (R_c) decreased to 12 Ωmm, shown in (figure 3.4-3).

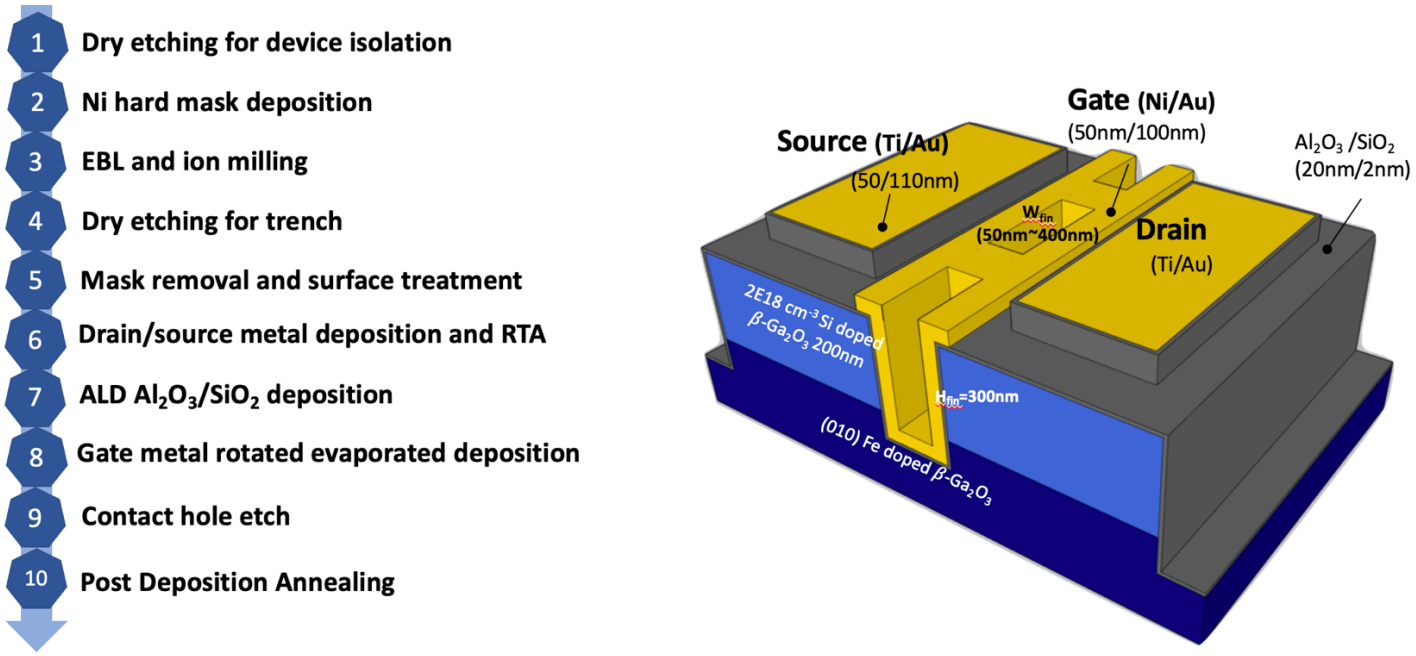


Figure 3.4-1 The device structure and fabrication process flow of β-Ga_2O_3 FinFETs. (a) Fabrication process flow, (b) device structure.

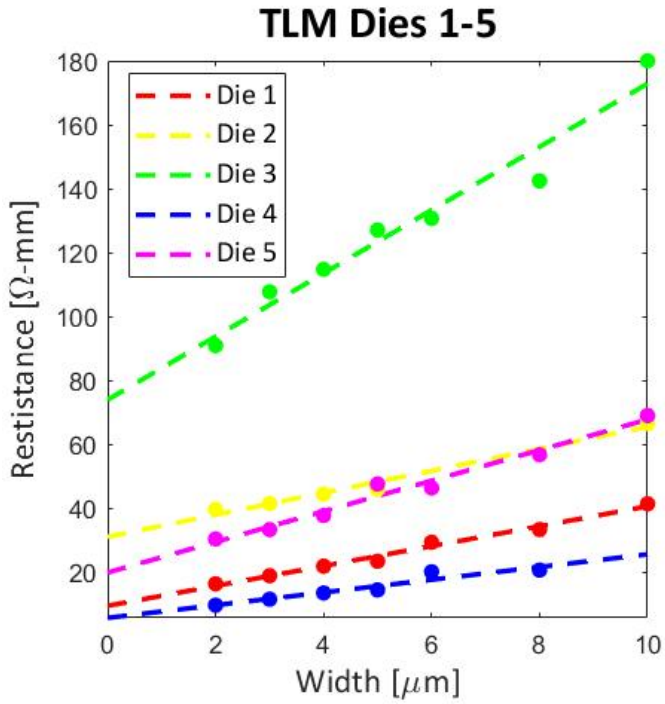


Figure 3.4-2 TLM result of the drain and source of β-Ga_2O_3 FinFETs before PDA, which shows the drain and source have an ohmic contact, with the average contact resistance (R_c) at 14 Ωmm, measured by Kathleen Smith.

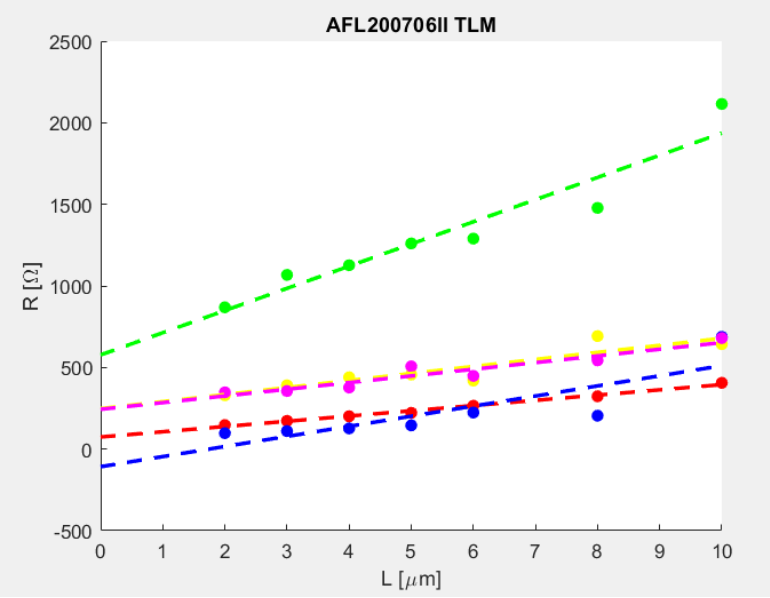


Figure 3.4-3 TLM result of the drain and source of β-Ga_2O_3 FinFETs post PDA, the average contact resistance (R_c) decreased to 12 Ωmm, measured by Kathleen Smith.

3.5 Devices Performance

This work first demonstrated the threshold voltage modulation by fin width in β-Ga_2O_3 lateral fin transistors. As shown in figure 3.5-1, with the fin width decreasing, the threshold voltage shifted from negative to positive, and the transition happened at around 100m wide fins. Also, in figure 3.5-1b, the on and off current ratio is about 10^7, which shows the gate has excellent control. In figure 3.5-2, the subthreshold slope is as high as 120 mV/dec. The leakage is low enough, as the gate current is around 10^{-14}.

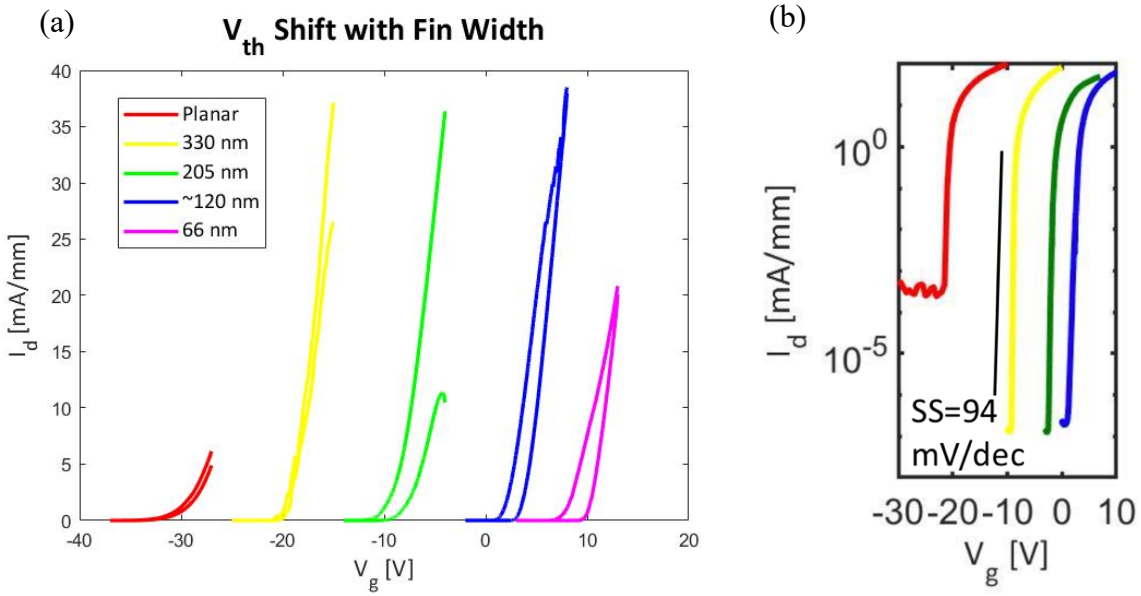


Figure 3.5-1 Transfer curve of the β-Ga_2O_3 FinFET (a) at linear scale, (b) at log scale. Both of figures show the threshold voltage modulation by fin width, measured by Kathleen Smith.

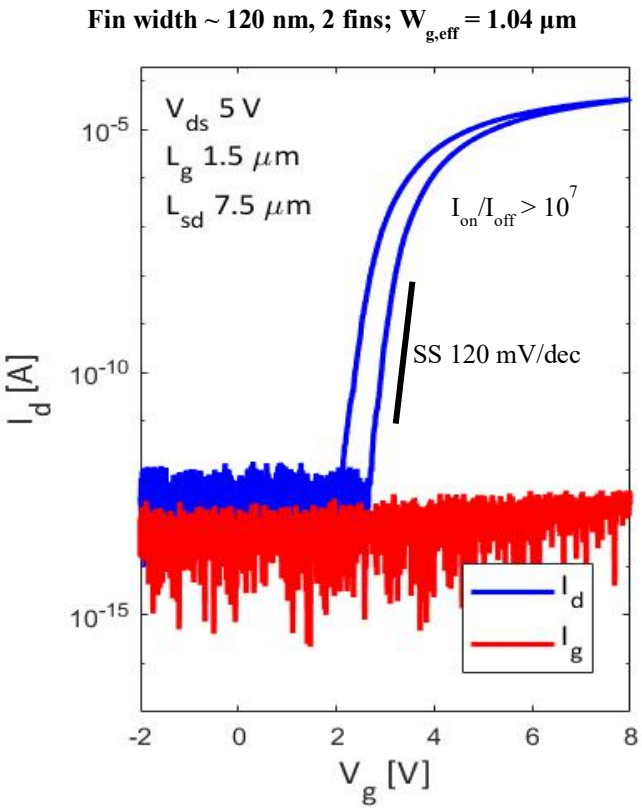


Figure 3.5-2 Log scale transfer curve of the β-Ga_2O_3 FinFET. There are two fins in the fin array, the fin width of each is 120 nm, measured by Kathleen Smith.

After post-deposition annealing (PDA), the on resistance of the FinFETs generally decreased, shown in the family curves in figure 3.5-3a, and the decremental rate is at most 90%, shown in figure 3.5-3b.

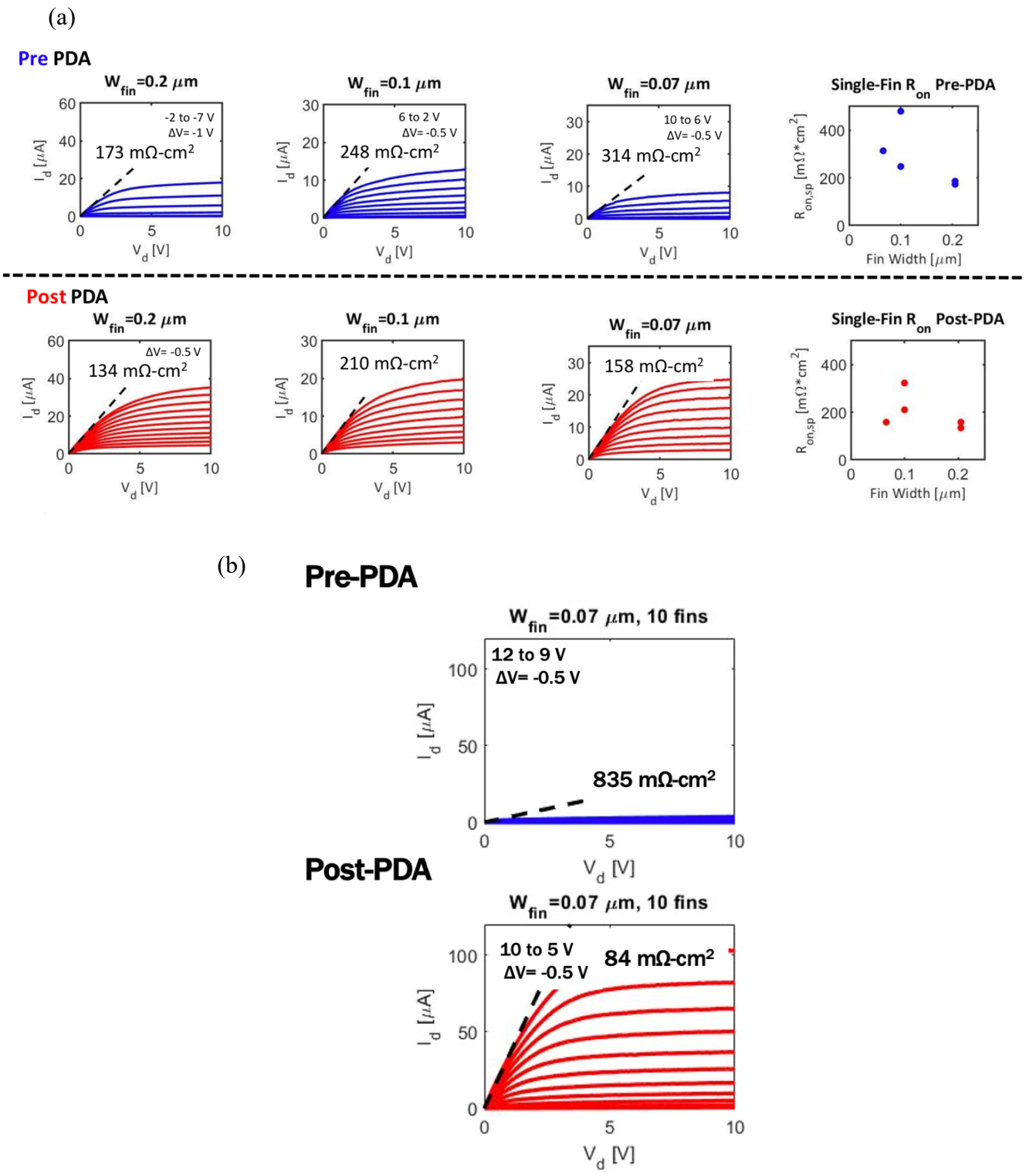


Figure 3.5-3 The on resistance decreasing after PDA, (a) the general decreasing in all fin dimensions. (b) the highest on resistance decreasing for 10-fin array with 70 nm wide fins, measured by Kathleen Smith.

Meanwhile, the β-Ga_2O_3 FinFETs have a moderate breakdown voltage. For the single fin FinFET with 100 nm wide fin and 1.5 μm gate to drain length, the breakdown voltage is around 650 V, shown in figure 3.5-4a. For the multi-fin one with 200 nm wide fin and 10 μm gate to drain length, the breakdown voltage is around 843 V, shown in figure 3.5-4b.

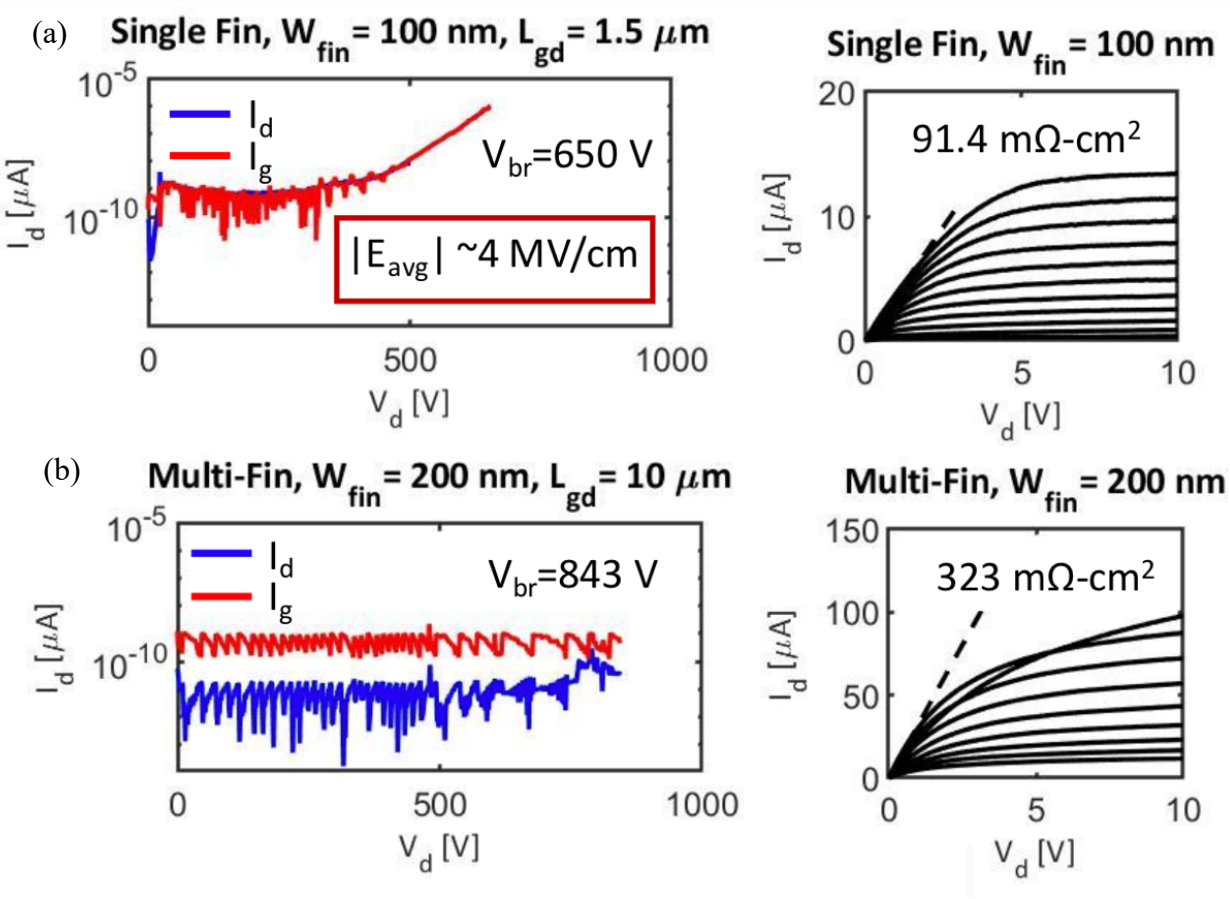


Figure 3.5-4 Breakdown performance of β-Ga_2O_3 FinFETs, (a) with 100nm wide single fin, (b) with 200 nm wide multi-fin, measured by Kathleen Smith.

3.6 Fin Conditions

In figure 3.6-1, it could be observed that the measured fin widths are generally smaller than the designed ones, which indicates that the overexposure happened during EBL. A more accurate does test is needed for future experiments. In this experiment, the smallest fin width survived is 35 nm. However, the 35 nm fin arrays did not have an electronic performance during the measurements, which indicates the less high-quality fins were generated during the etching comparing to wider fins. From the scanning electron microscopy (SEM) images in figure 3.6-1, it is also evident that the small size fins do not have a uniform shape as the large size ones. Therefore, it is eager to optimize the etchings creating fin arrays.

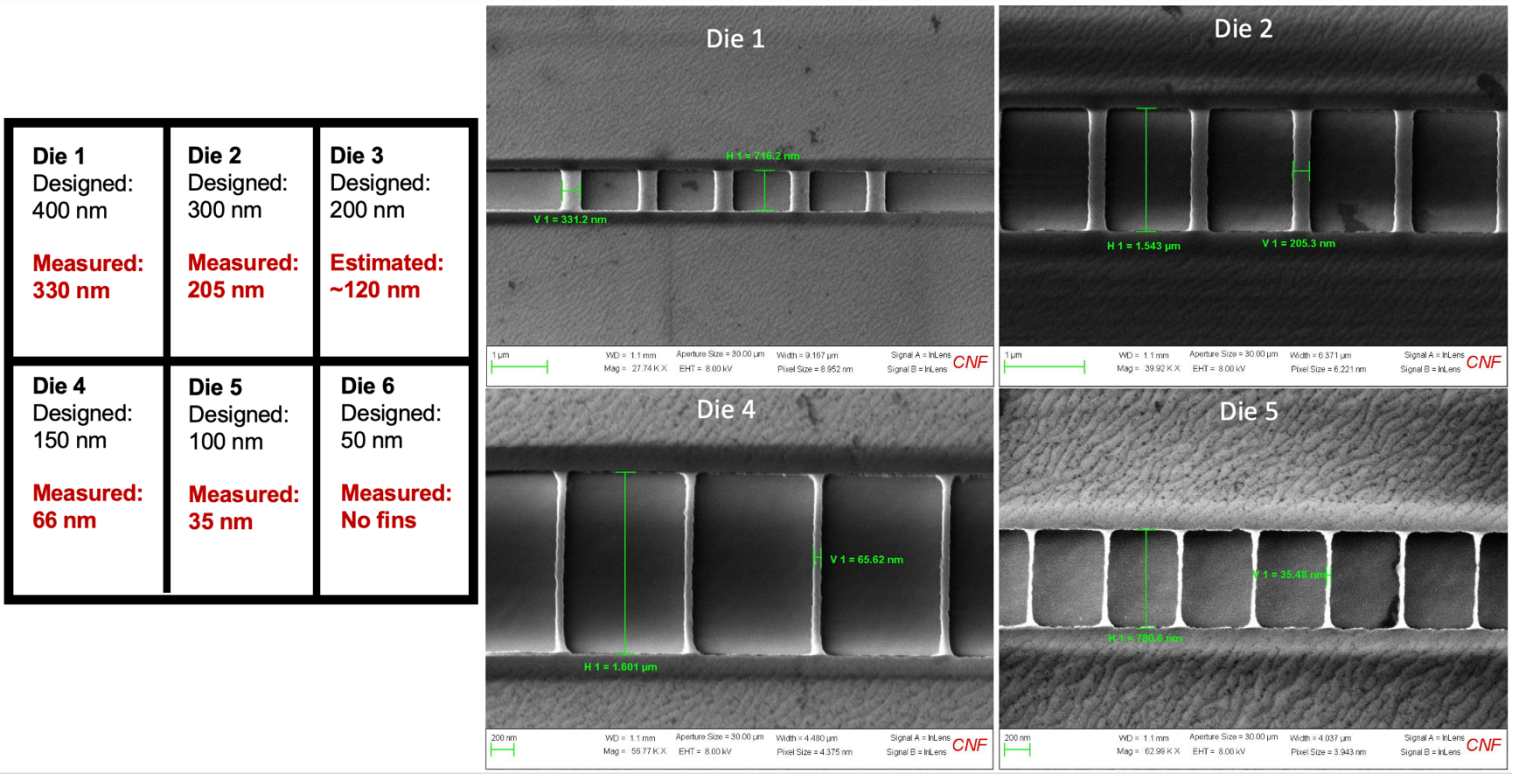


Figure 3.6-1 The SEM images of the β-Ga_2O_3 fin arrays.

3.7 Conclusion

In general, the β-Ga_2O_3 FinFETs achieved an outstanding performance, where the threshold voltage modulation by fin width in β-Ga_2O_3 lateral fin transistors was first demonstrated. Moreover, they also demonstrated the advantage of fin geometry in mitigating the high interface trap density on the top surface of (0 1 0) β-Ga_2O_3. For the future, the denser fin arrays with an increased number of fins are desired for better performance, which needs a better etching recipe to improve the fin quality and survival rate. Moreover, the ohmic contacts are desired to be improved for lower on-resistance.

4 β-Ga_2O_3 Fin Dry Etching Optimization

4.1 Motivation

As mentioned before, the fin-structures are particularly attractive since they enable the RESURF effect, offering the side-gates extended conducting channel with a high conductance, with which not only lateral but also vertical FinFET can enable an enhancement mode performance. However, there have been only a few reports on the single crystal β-Ga_2O_3 fin etching shape perfection with inductively coupled plasma (ICP) reactive ion etching (RIE). This subject is of high importance since the perfection of fin shape affects the survival of fins and the electric field distribution etc. Both in our previous β-Ga_2O_3 vertical fin-structure devices and our first-generation β-Ga_2O_3 FinFETs, we observed a "waist" developed in the middle of a fin as shown in (figure 4.1.1), this shape imperfection "narrowed waist" will severely pinch the current

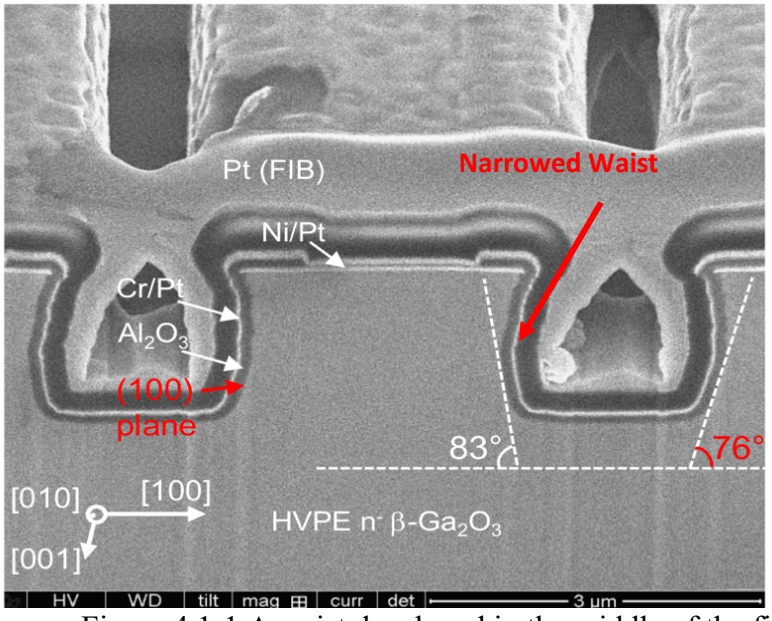


Figure 4.1-1 A waist developed in the middle of the fins, which can cause a severely current pinching, picture made by Wenshen Li.

flow. In this section, I will systematically investigate the effect factors of fin waist narrowing and etch rate during β-Ga_2O_3 fin ICP-RIE process in BCl_3 and Ar atmosphere and the possible etching mechanism in this process.

4.2 Possible β-Ga_2O_3 Dry Etching Mechanism in BCl_3/Ar

The β-Ga_2O_3 etching mechanism in BCl_3/Ar has not yet been confirmed in the community, but Shah et al. [33] introduced a hypothesis that could explain their observations and our fin behaviors. Their hypothesis extended the aluminum oxide dry etching mechanism in BCl_3/Ar [34, 35] to gallium oxide etching systems [33]. In this hypothesis, BCl_3 works as an effective scavenger of oxygen[34]. Below a critical oxygen pressure, BCl_3 will react with oxygen and generate chemically inner gas $B_3Cl_3O_3$ and boron trioxide (B_2O_3) solid. While the $B_3Cl_3O_3$ gas could be pumped out, the boron trioxide solid could deposit and accumulate on both bottom and sidewall surfaces. The B_2O_3 on the sidewall will work as a passivation film, but the bottom ones will prevent the etching unless the physical sputtering could remove them and reveal the gallium oxide surface to be both physically and chemically etched[33], shown in (figure 4.2-1).

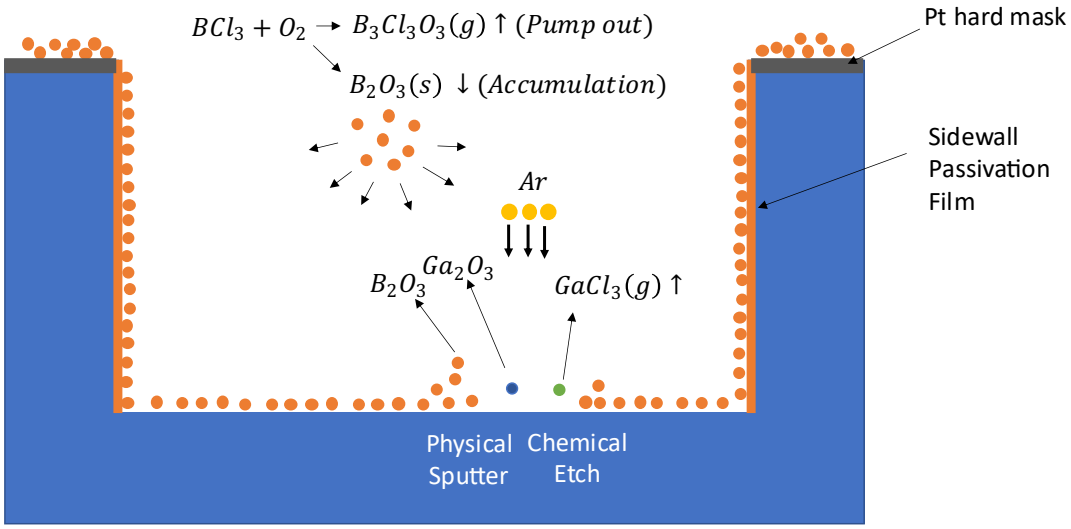


Figure 4.2-1 A cartoon illustrate the possible etching mechanism of beta-gallium oxide in BCl_3/Ar. The BCl_3 enter the chamber and react with oxygen in the atmosphere with the products of solid B_2O_3 and $B_3Cl_3O_3$ chemically inert gas which will be pumped out. The B_2O_3 will accumulate in the bottom and sidewall. The bottom ones will impede the chemical reaction, and sidewall ones will act as sidewall passivation layer.

4.2.1 Important Chemical and Physical Reactions Involved

As previously mentioned, there are several important chemical reactions and physical reactions in this mechanism, including the BCl_3 involved series chemical reactions and the Ar involved physical sputtering.

4.2.1.1 Chemical reactions

For the chemical reactions, the first one is the BCl_3 reacting with oxygen, as stated, shown in (Equation 4.2-1,2). For the reaction producing $B_3Cl_3O_3$, the effective reactive radicals of BCl_3 are BCl_2^+ ions, while the BCl_3 mainly produces B_2O_3. In

these two reactions, the oxygen could come from Ga_2O_3, and the O_2, H_2O leaked from plasma processing equipment.

Equation 4.2-1

$$BCl_2^+ + O_2 \rightarrow B_3Cl_3O_3$$

Equation 4.2-2

$$BCl_3 + O_2 \rightarrow B_2O_3$$

The second one is the BCl_3 chemical etching on revealed gallium oxide surface, producing $GaCl_3$ and B_2O_3 shown in (Equation 4.2-3). The melting point of by-product $GaCl_3$ is 77.9℃ at 1atm, while the boiling point is 201℃. In this experiment, the pressure is 5 mtorr, much lower than the atmosphere, where the melting and boiling point are much lower than the values at 1atm. Therefore, with over 200℃ substrate surface temperature, most of the $GaCl_3$ by-products are in the gas form and could be pumped out, which is mostly the case in this experiment.

Equation 4.2-3

$$Ga_2O_3 + 2BCl_3 = 2GaCl_3 + B_2O_3$$

$$\Delta G = -327.362\ kJ/mol$$

Moreover, the water leakage from the plasma processing equipment could also react with BCl_3 and produce B_2O_3 and HCl, and the HCl could trigger the by-reaction with Ga_2O_3 and produce $GaCl_3$ shown in (Equation 4.2-4,5). Simply combining the two equations, it could derive the Equation 4.2.1-3.

Equation 4.2-4

$$3H_2O + 2BCl_3 = 6HCl + B_2O_3$$

$$\Delta G = -262.384\ kJ/mol$$

Equation 4.2-5

$$Ga_2O_3 + 6HCl = 2GaCl_3 + 3H_2O$$

$$\Delta G = -64.978\ kJ/mol$$

In the chamber, the B_2O_3 is not able to be chemically removed by BCl_3 and produce the $B_3Cl_3O_3$ because the pressure of $B_3Cl_3O_3$ always remains at its saturation value. Therefore, the B_2O_3 accumulation on the bottom surface could only be removed by physical sputtering.

4.2.1.2 Physical sputtering

During etching, the Ar and BCl_2^+ are the two main sputter species to remove the accumulated B_2O_3 enabling the following chemical and physical etching. Meanwhile, the revealed Ga_2O_3 surface could also be sputtered off, as well as the residual solid chemical reaction by-product $GaCl_3$ as stated in (Equation 4.2-3,5).

4.2.2 Hypothesis of Waist Narrowing Formation

As mentioned at the beginning of this section, when B_2O_3 on the sidewall is in solid form, it could work as a sidewall passivation film. When above certain point, the B_2O_3 can form a metastable state, while the single bond length between O and B can be long enough and generate the polarized –B=O radical [36] (The Lewis structure of boron trioxides is shown in figure 4.2-2). Therefore, the B_2O_3 is not stable enough to form an efficient sidewall passivation film.

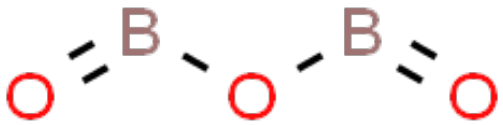


Figure 4.2-2 The Lewis structure of boron trioxides. Above certain temperature, the single bonds between boron and oxide can be long enough and generate the polarized –B=O radical.

At around 3.5 GPa, the transform point of B_2O_3 is around 525℃, as shown in the B_2O_3 phase diagram in (figure 4.2-3). In our experiment, the pressure is 5 mtorr, much lower than 3.5 GPa, the transform point could much lower than 525℃. In this case, with a higher local surface temperature, the B_2O_3 sidewall passivation film could disappear locally. Therefore, the isotropic chemical reaction between Ga_2O_3 and BCl_3 can happen in these areas and create a local basin on the sidewalls.

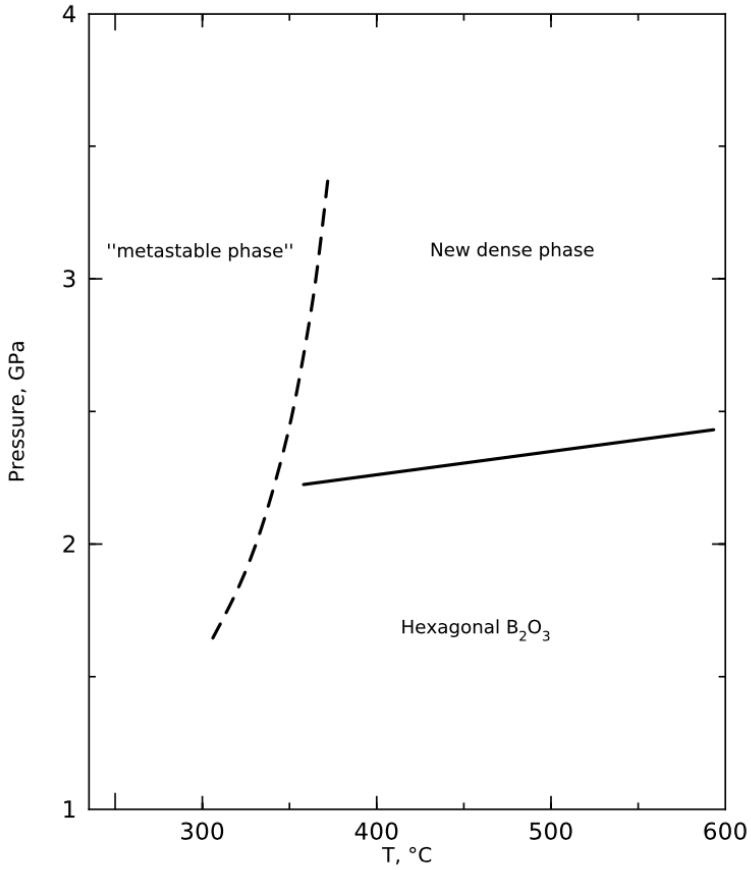


Figure 4.2-3 Phase diagram of born trioxides. At 3.5 GPa at 525℃, the metastable phase of B_2O_3 can be formed [36].

In figure 4.2-4, the heat distribution in the trench is mainly generated by ion bombardments. In this case, the bottom areas which receive the most bombardments have the highest surface temperature, least boron trioxides left, and fast etch rate, enabling the fin generations. At the bottom part of the sidewalls, due to the geometry of the corner, more B_2O_3 particles can deposit and pile up in the corners. Even though the corners have the highest local temperature because of the most frequent bombardments and bad heat dissipation, but with the thicker B_2O_3 layer, the local sidewall passivation film is still stable to protect the sidewall. At the upper part of the

sidewall, with the least bombardments and good heat dissipation, the local surface temperature is the lowest and much below the transformation temperature. Therefore, the upper part sidewall passivation layers are still functional. However, in the middle part, the surface temperature can be high enough due to the thin passivation film and bad heat dissipation, where the unstable film is easy to desorb from the sidewall and expose the sidewall surface to be etched and form the local basin. In this case, the sidewall waist narrowing can appear in the fins.

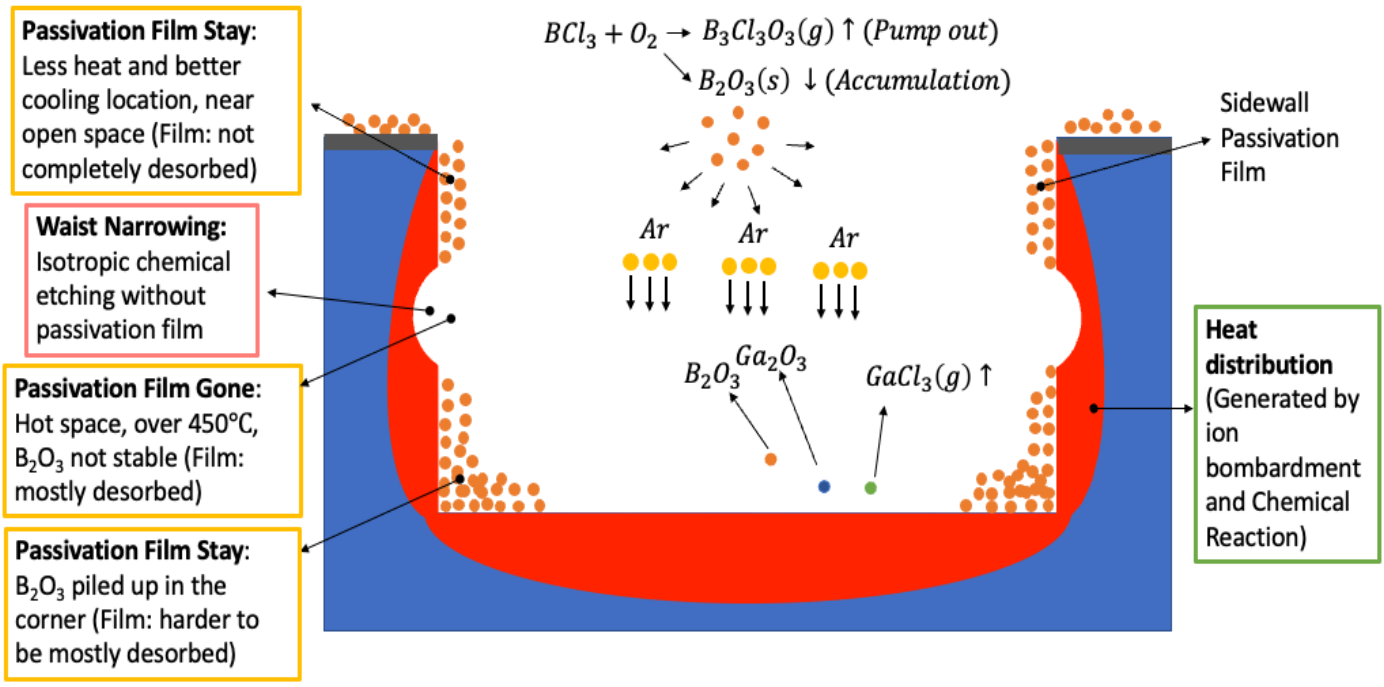


Figure 4.2-4 The hypothesis of waist formation in Ga_2O_3 fin ICP-RIE with BCl_3 and Ar. In this Ga_2O_3 trench, the red areas represent the heat distribution, which is generated by ion bombardment and chemical reaction. The orange particles are the B_2O_3 particles generated by the chemical reaction between BCl_3 and O_2, those particles form the sidewall passivation film. The grey areas on the top of the samples represent the metal hard mask during the etching, also work as top passivation layer.

4.3 Definition of Nomenclature Used in Fin Etching

In this experiment, the recessing parts to create fin arrays are in two ways. One is the fin etching, which stands for creating the fin arrays by etching the ground down, shown in (figure 4.3-1a). Instead, the trench etching is only etching down the trench's areas between fins in arrays, shown in (figure 4.3-1b).

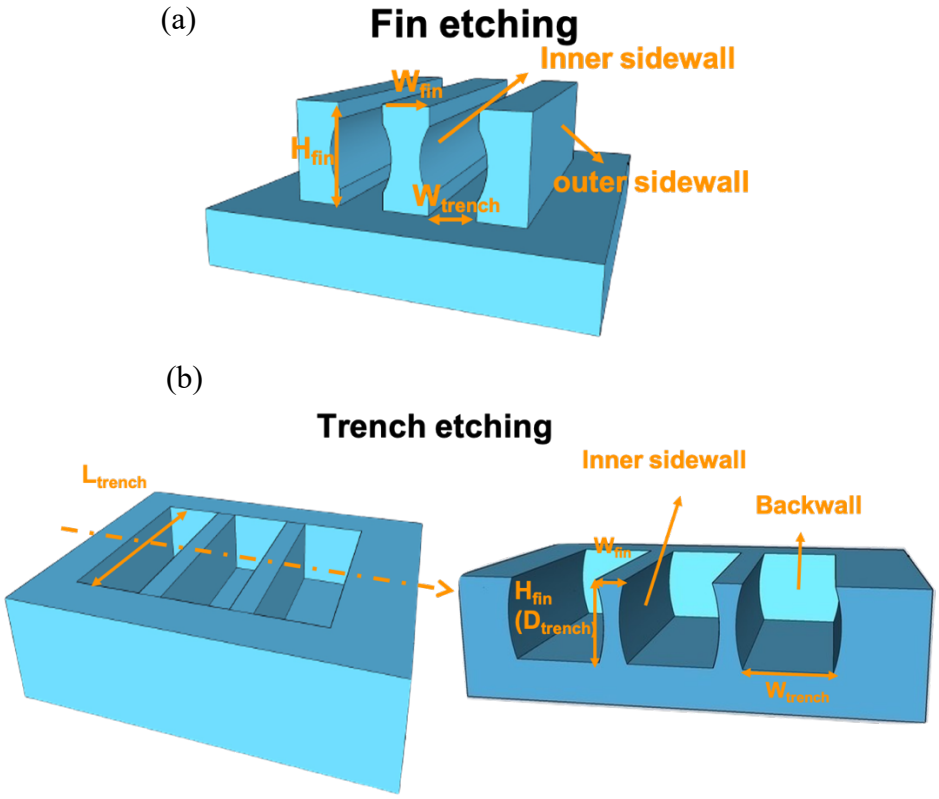


Figure 4.3-1 The illustration of dimensional parameters of fins, trenches, and fin waist. (a) Fin etching stands for creating the fins by etching the ground down. (b) Trench etching stands for creating the fins by only etching the trench areas down.

Definitions of dimensional parameters for fins, trenches, fin waist, and waist narrowing are illustrated in figure 4.3-1. With the defined dimensions, the fin aspect ratio is fin height (H_{fin}) over the fin width (W_{fin}), while the trench ratio is fin height (H_{fin}) over the trench width (W_{trench}). In figure 4.3-2, the fin waist narrowing is defined

by half of the difference between the fin width and waist width. For higher waist narrowing, the current pinch can be more severe. Therefore, a lower waist narrowing is desired.

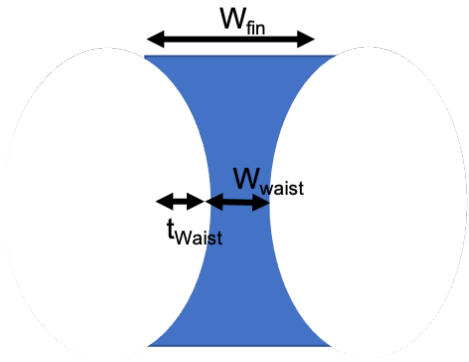


Figure 4.3-2 The definition of fin waist narrowing, which is half of the difference between the fin width and waist width.

4.4 Ga_2O_3 Fin Etch Condition

The fin and trench arrays were fabricated on single-crystal β-Ga_2O_3 substrates with 3 orientations: (010), (001), and (-201). Hard masks of Pt were patterned by EBL for fin/trench widths less than 1 μm and optical lithography for the wider ones.

The dry etch parameters were fixed at 350 W ICP power, 20 W RIE power, 5 mTorr, 20℃ with 35 sccm BCl_3 and 5 sccm Ar. Prior to SEM, the etched samples were soaked in HCl and/or HF for 10min to remove etch damage/residue.

4.5 Factors Impacting Ga_2O_3 Fin Waist Narrowing

In this Ga_2O_3 fin etching test, the fin and trench arrays geometries and etching conditions variables were differed under control to find the weak and strong factors influencing the waist narrowing.

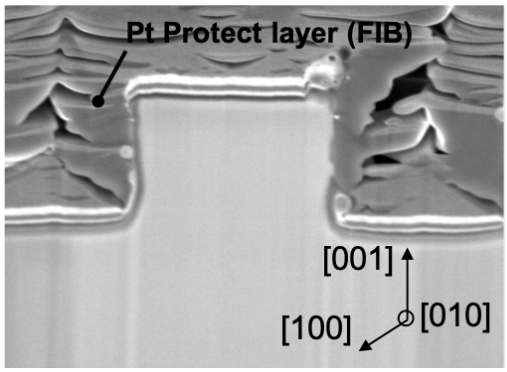
4.5.1 Strong Factors

By differing the strong factors, the waist narrowing has an obverse either incremental or diminishing trend.

4.5.1.1 Fin Height (Etch Depth)

In this experiment, the fin heights are varied from 1.3 to 1.8 μm for the same 2 μm wide fin arrays with 2 μm wide trenches in between on fin etching (0 0 1) substrate. As shown in figure 4.5-1, the 1.6 μm high fins have the waist narrowing of 101.5 ± 9 nm (figure 4.5-1a), but the 1.8 μm high fins have a much larger waist narrowing at around 169.1 ± 9 nm (figure 4.5-1b).

(a)



(b)

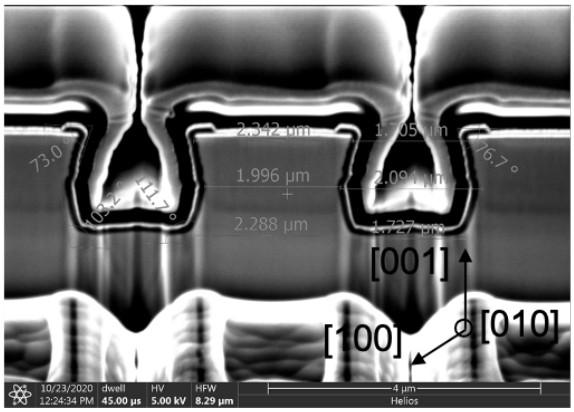


Figure 4.5-1 The SEM pictures of fin arrays created by fin etching with 2 μm fin width, 2 μm trenches width, (a) 1.6 μm fin height, (b) 1.8 μm fin height. SEM taken by Kazuki Nomoto.

In figure 4.5-2, there is a clear incremental trend between the fin height and waist narrowing. Therefore, the fin height is a strong factor affecting the waist narrowing.

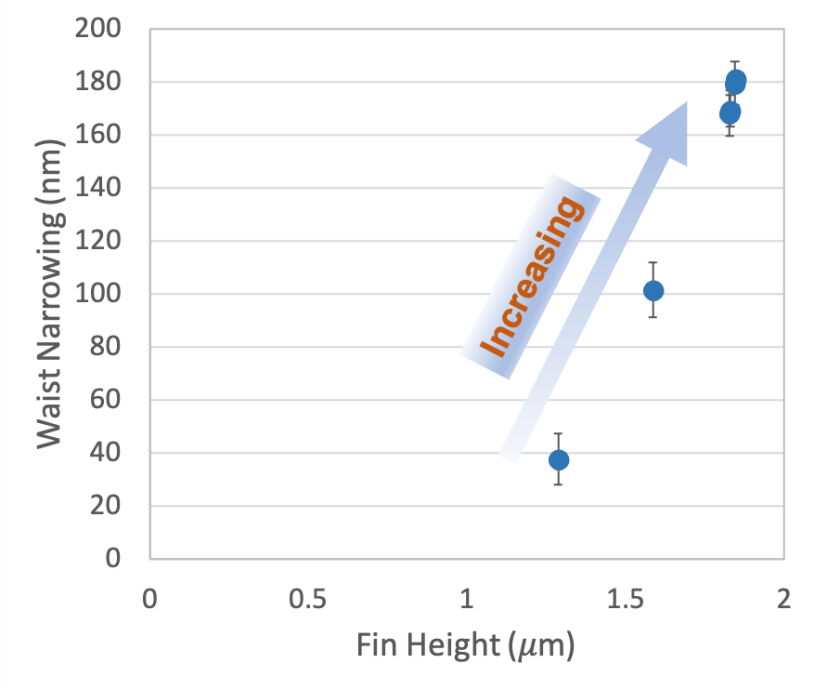


Figure 4.5-2 The relation between fin height and waist narrowing. With the increasing of fin height, the waist narrowing increased.

Based on the mechanism introduced before, in order to create taller fins (deeper trench), there should be more ion bombardments happened in the trench areas, which can lead to more heat in this area. Besides, the heat is trapped inside the trench with relatively worse heat dissipation due to the deeper trench. Therefore, in the trenches, there can be higher surface temperature and more chance for B_2O_3 desorption and more severe waist narrowing, illustrated in (figure 4.5-3).

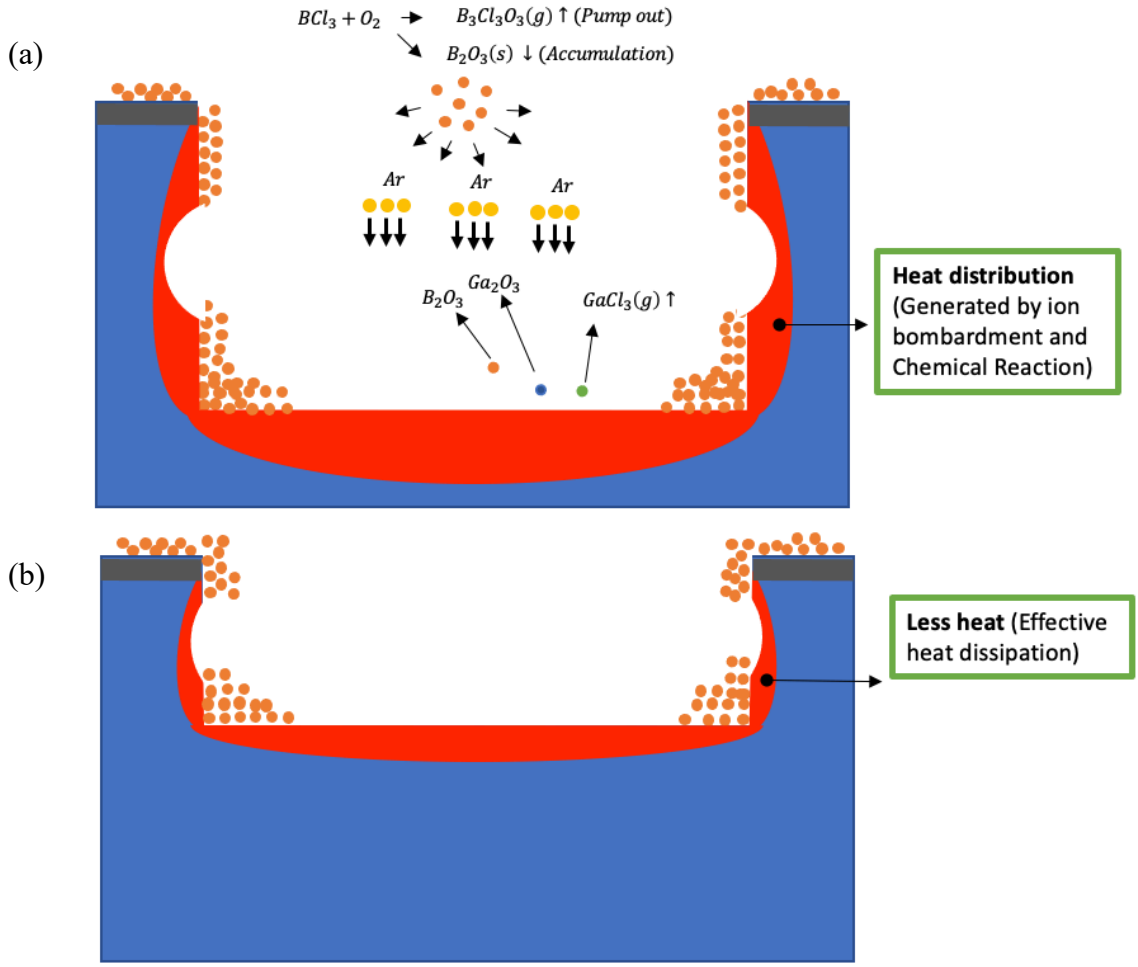


Figure 4.5-3 Illustration of taller fins have more severe fin waist narrowing. The red areas represent the heat distribution. (a) Fins with deeper trench; (b) fins with shallower trench.

4.5.1.2 Trench Width

The fin arrays with different trench width were created by both fin and trench etching, with and without thermal paste. In all conditions, the fin arrays with a wider trench have more waist narrowing.

In figure 4.5-4, the 2.4 μm wide fin arrays were created by fin etching at (0 0 1) substrate with the same 1.6 μm fin height. The fin array (in figure 4.5-4a,b) has a

trench width of 3.0 μm, where the waist narrowing is around 66.5 ± 10 nm. For the fin arrays with the same fin width but 0.9 μm less trench width (2.1 μm), shown in (figure 4.5-4c,d), the waist narrowing is around 201.5 ± 10 nm, which is about 3 times more than the one with 3.0 μm wide trench.

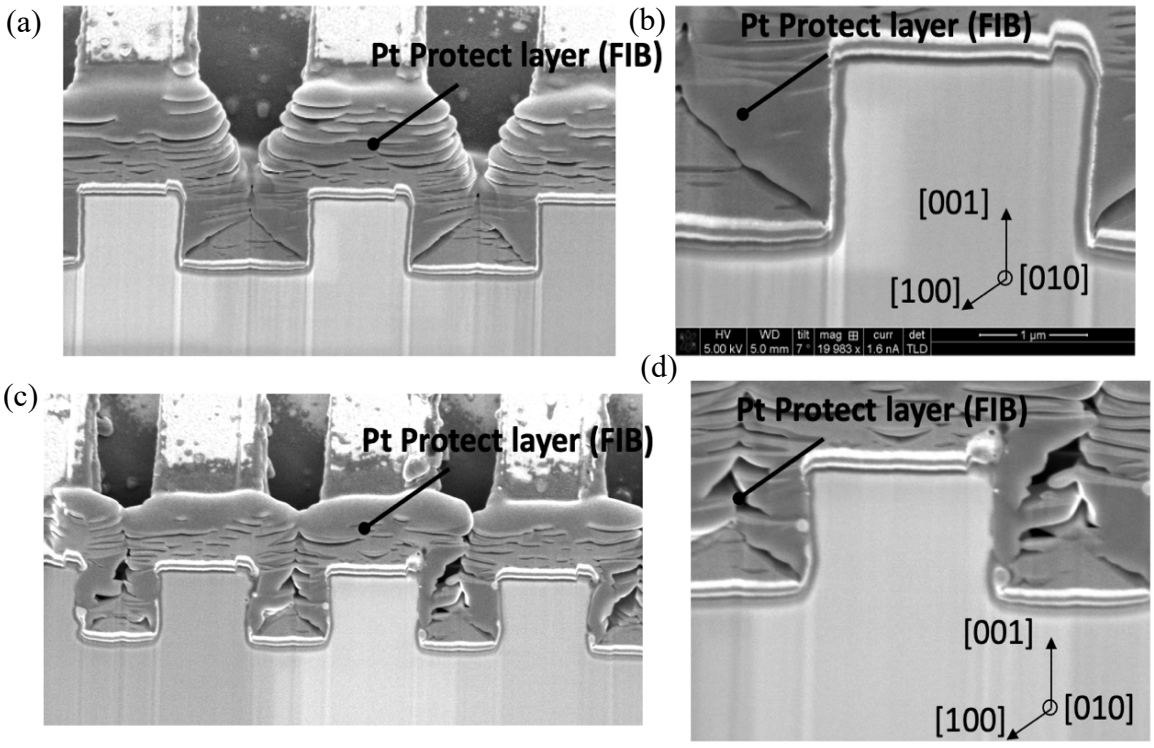
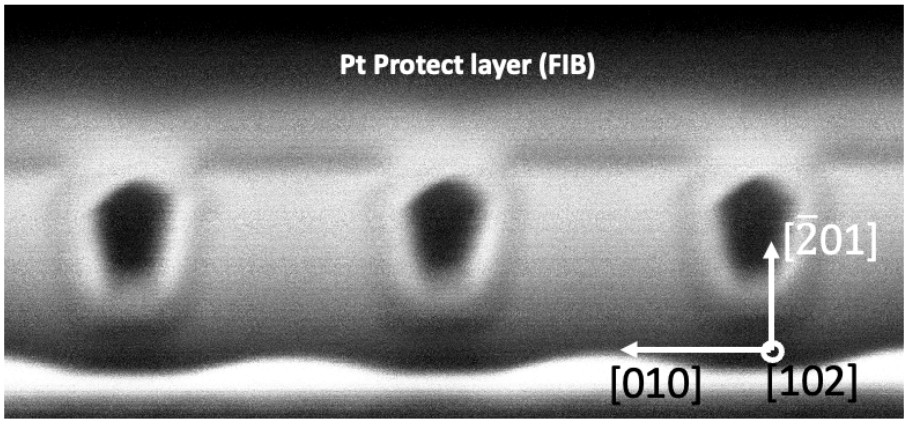


Figure 4.5-4 The SEM pictures of fin array with 2.4 μm fin width, 1.6 μm fin height created by fin etching on (0 0 1) substrates. (a) The fin arrays with 3.0 μm trench width; (b) single fin with 3.0 μm trench width. In the fin arrays with 3.0 μm trench width, the waist narrowing is around 66.5 ± 10 nm. (c) The fin arrays with 2.1 μm trench width. (d) single fin with 2.1 μm trench width. In the fin arrays with 2.1 μm trench width, the waist narrowing is around 201.5 ± 10 nm, an obvious waist is built up in the mid of the fin. SEM taken by Kazuki Nomoto.

The same results were observed in the fin arrays created by trench etching. For the 0.3 μm wide, 0.52 μm high fin arrays created by fin etching at ($\bar{2}$ 0 1) substrate, the trench width is varied from 200 to 800 nm, and the waist narrowing changes from 31.8

± 9 to 0.7 ± 9 nm. Figure 4.5-5a shows the fin arrays with 200 nm trench width, where the waist narrowing is 31.8 ± 9 nm. When the trench width increases to 800 nm, the waist narrowing of the fins decreases to 0.7 ± 9 nm, the sidewall of which is almost straight, shown in (figure 4.5-5b). In figure 4.5-6, the waist narrowing decreases linearly with the increase of the trench width in the 0.3 μm wide, 0.52 μm high fin arrays.

(a)



(b)

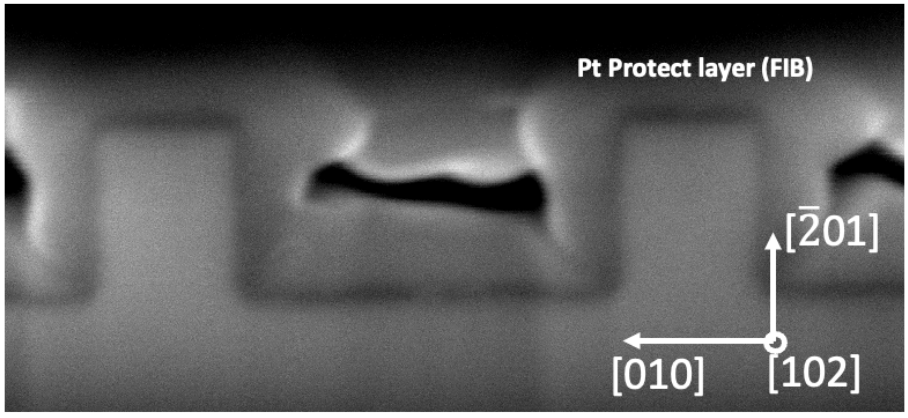


Figure 4.5-5 The SEM images of fin array with 0.3 μm fin width, 0.52 μm fin height created by trench etching on ($\bar{2}$ 0 1) substrates. (a) The fin arrays with 0.2 μm trench width, the waist narrowing is around 31.8 ± 9 nm, an obvious waist is built up in the mid of the fin. (b) The fin arrays with 0.8 μm trench width, the waist narrowing is around 0.7 ± 9 nm. SEM taken by Mingli Gong.

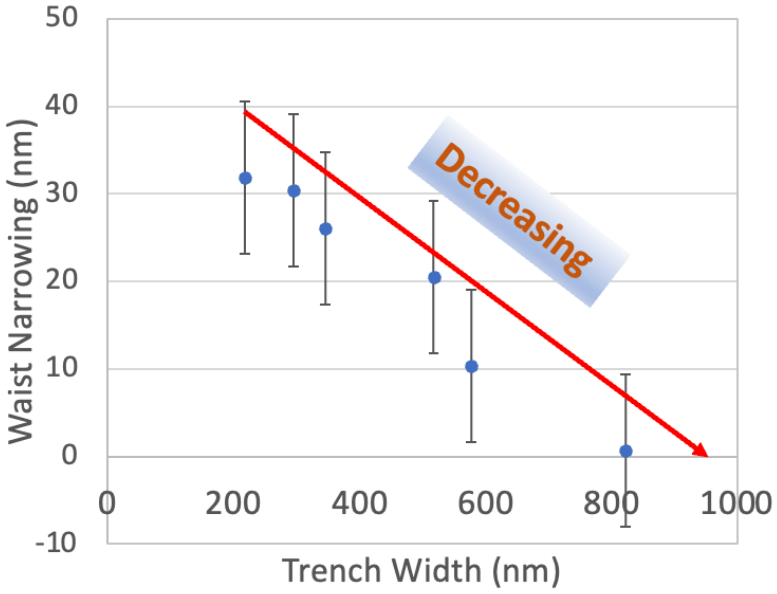
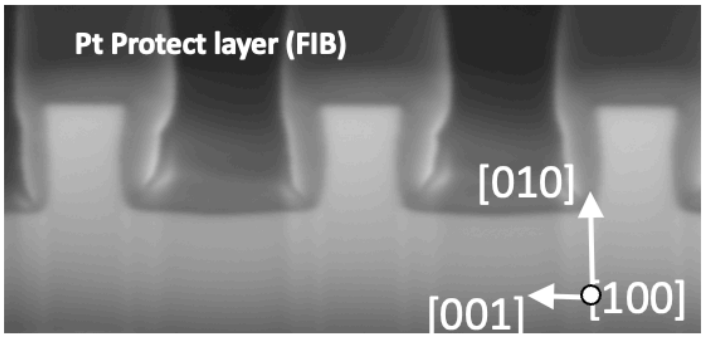


Figure 4.5-6 For 0.3 μm wide 0.52 μm high fin arrays created by trench etching on ($\bar{2}$ 0 1) substrates, the trench width varied from 200 nm to 800 nm, while the waist narrowing decreases around linearly.

Same observations were obtained in the trench etched fin array on (0 1 0) substrate with thermal paste. The fin arrays are 0.3 μm wide and 0.56 μm high, while the trench width varied from 300 nm to 900 nm, and the waist narrowing changes from 17.8 ± 2 nm (figure 4.5-7a) to 8.8 ± 2 nm (figure 4.5-7b) with it, the waist narrowing decreases about linearly with the incremental trench width, shown in (figure 4.5-8).

(a)



(b)

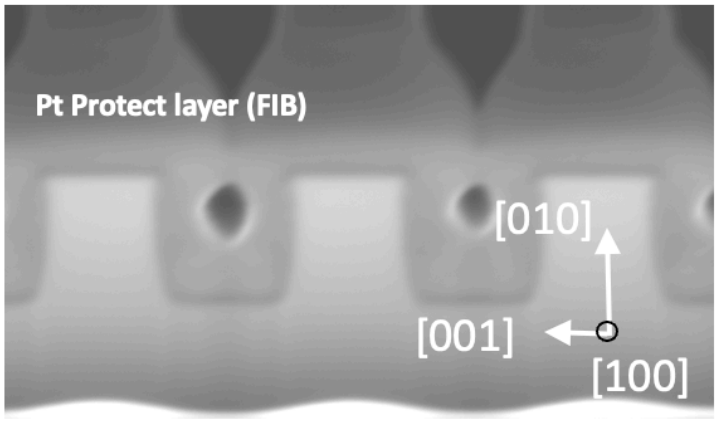


Figure 4.5-7 The SEM images of fin array with 0.3 μm fin width, 0.56 μm fin height created by trench etching on (0 1 0) substrates. (a) The fin arrays with 0.9 μm trench width, the waist narrowing is around 8.8 ± 2 nm. (b) The fin arrays with 0.3 μm trench width, the waist narrowing is around 17.8 ± 2 nm, a more severe waist is built up in the mid of the fin. SEM taken by Mingli Gong.

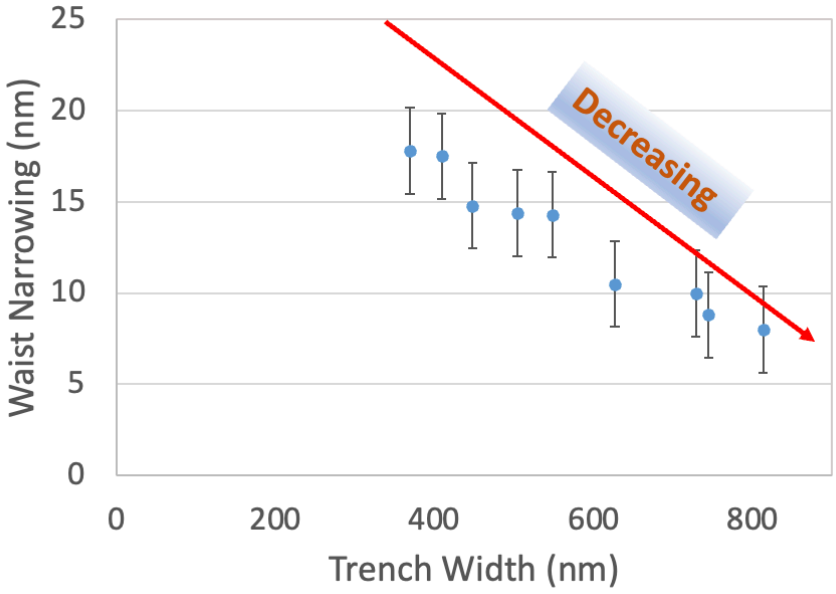


Figure 4.5-8 For 0.3 μm wide 0.52 μm high fin arrays created by trench etching on ($\bar{2}$ 0 1) substrates, the trench width varied from 200 nm to 800 nm, while the waist narrowing decreases around linearly.

Based on the mechanism stated before, the fin arrays with wider trench have opener trench space, which benefits the cooling in the trench areas, where the low-temperature chamber ambient gas can take off the heat from the sample surface. Therefore, the B_2O_3 passivation film is more stable to protect the sidewall from forming the waist on the fins, illustrated in (figure 4.5-9a). However, for the fin arrays with a narrow trench, more heat can be stuck inside the trench, and with the temperature built up beyond the transforming temperature, the more local passivation film desorption occurs and more severe waist narrowing forms, illustrated in (figure 4.5-9b).

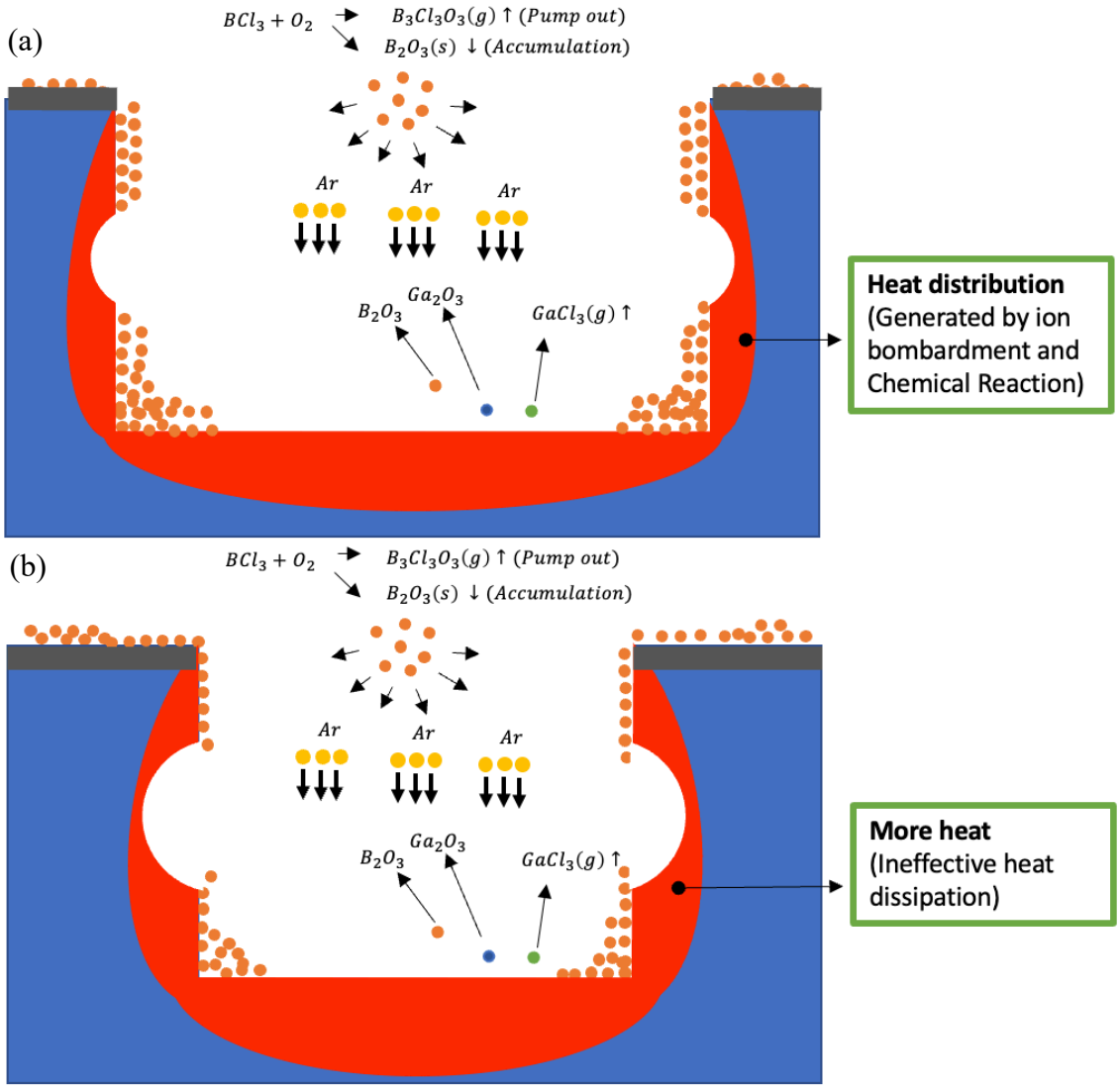


Figure 4.5-9 Illustration of narrower fins have more severe fin waist narrowing. The red areas represent the heat distribution. (a) Fins with wider trench; (b) fins with narrower trench.

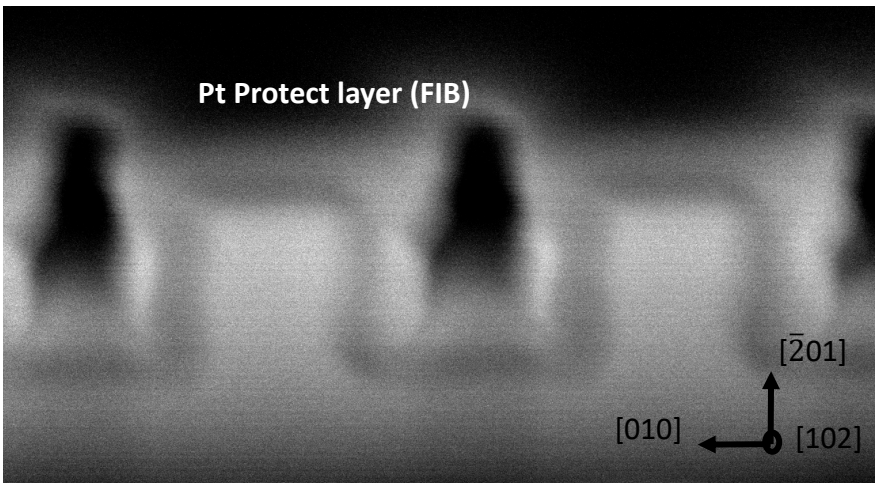
Same reason for the observation, where the outside walls of outmost fins are always straight, the outside of the outmost fin can be assumed as an extremely wide trench.

4.5.1.3 Thermal Paste

In this experiment, the AIT Mart – Cool GREASE® CGR7016 was used as thermal paste, applying in between Ga_2O_3 substrate and sapphire carrier wafer. This thermal paste is boron nitride filled, electrically insulating, and thermally conducting, with electrical resistivity larger than $1x10^{14}$ Ω/cm and thermal conductivity larger than 4.0 W/m℃. In addition to its thermal and electrical properties, its thixotropic and high-temperature resistive properties also make this thermal paste an ideal candidate for dry etching.

There are two sets of fin arrays trench etched in this experiment. The fins on one set have 0.45 μm fin height and 200 nm to 800 nm trench width without thermal paste. The other set has the 0.56 μm high fin and 300 nm to 900 nm wide trench, with thermal paste. In figure 4.5-10a, the fin arrays with 520 nm wide trench in the substrate etched without thermal paste have the waist narrowing at 20.5 ± 8 nm. However, in figure 4.5-10b, the taller fin arrays with a narrower trench (450 nm wide) in the substrate etched with thermal paste has minor waist narrowing at 14.4 ± 2 nm.

(a)



(b)

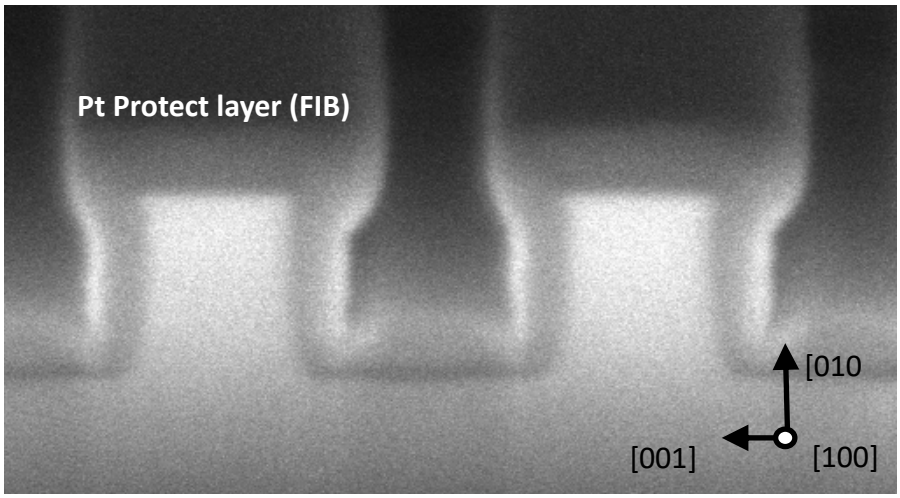


Figure 4.5-10 The SEM images of fin array created by trench etching. (a) The 0.45 μm high fin arrays with 0.52 μm trench width etched without thermal paste, the waist narrowing is around 20.5 ± 8 nm. (b) The 0.56 μm fin arrays with 0.45 μm trench width, the waist narrowing is around 14.4 ± 2 nm, a less waist narrowing is built up in the mid of the fin. SEM taken by Mingli Gong.

Moreover, in figure 4.5-11, in both conditions (with and without thermal paste), the waist narrowing decreases with the increasing trench width; more importantly, it is evident that the general trend line of the condition with thermal paste is much below

the one without thermal paste. Therefore, the thermal paste is able to decrease the waist narrowing and improve the sidewall waist.

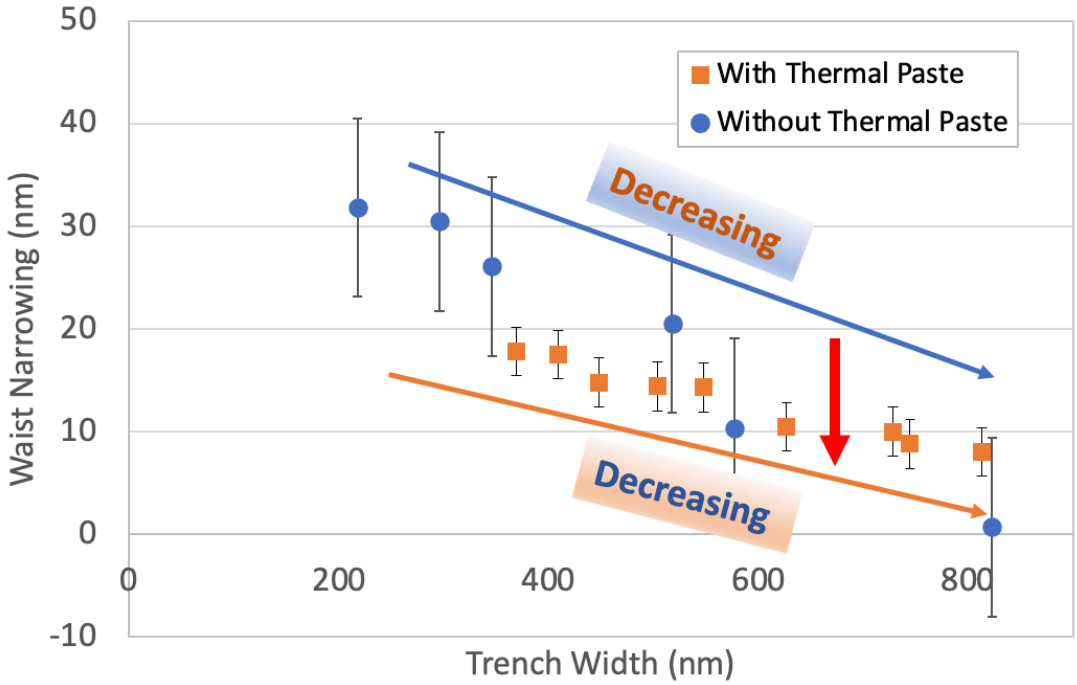


Figure 4.5-11 For the fin arrays created by trench etching, in both conditions 0.45 μm high fins without thermal paste and 0.56 μm high fins with thermal paste, the waist narrowing decreases around linearly with the increasing trench width. The fin arrays etched with thermal paste generally have lower waist narrowing than the one without thermal paste, which indicate the improvement brought by thermal paste.

Comparing to the air gap (thermal conductivity less than 0.03W/m°C) between substrate and carrier, the thermal conductivity increased more than 100 times with thermal paste. The thermal paste primarily improves the heat dissipation of substrate through the backside to the carrier wafer and decreases the surface temperature of not only the bottom but also the sidewall of the trench area in the fin arrays. Therefore, according to the mechanism introduced in 4.2, the sidewall passivation film is more stable locally with evener and lower local surface temperature (below or close to the

unstable metaphase transformation temperature) and better protect the local sidewall from generating the waist or lessen the waist narrowing, illustrate in figure 4.5-12.

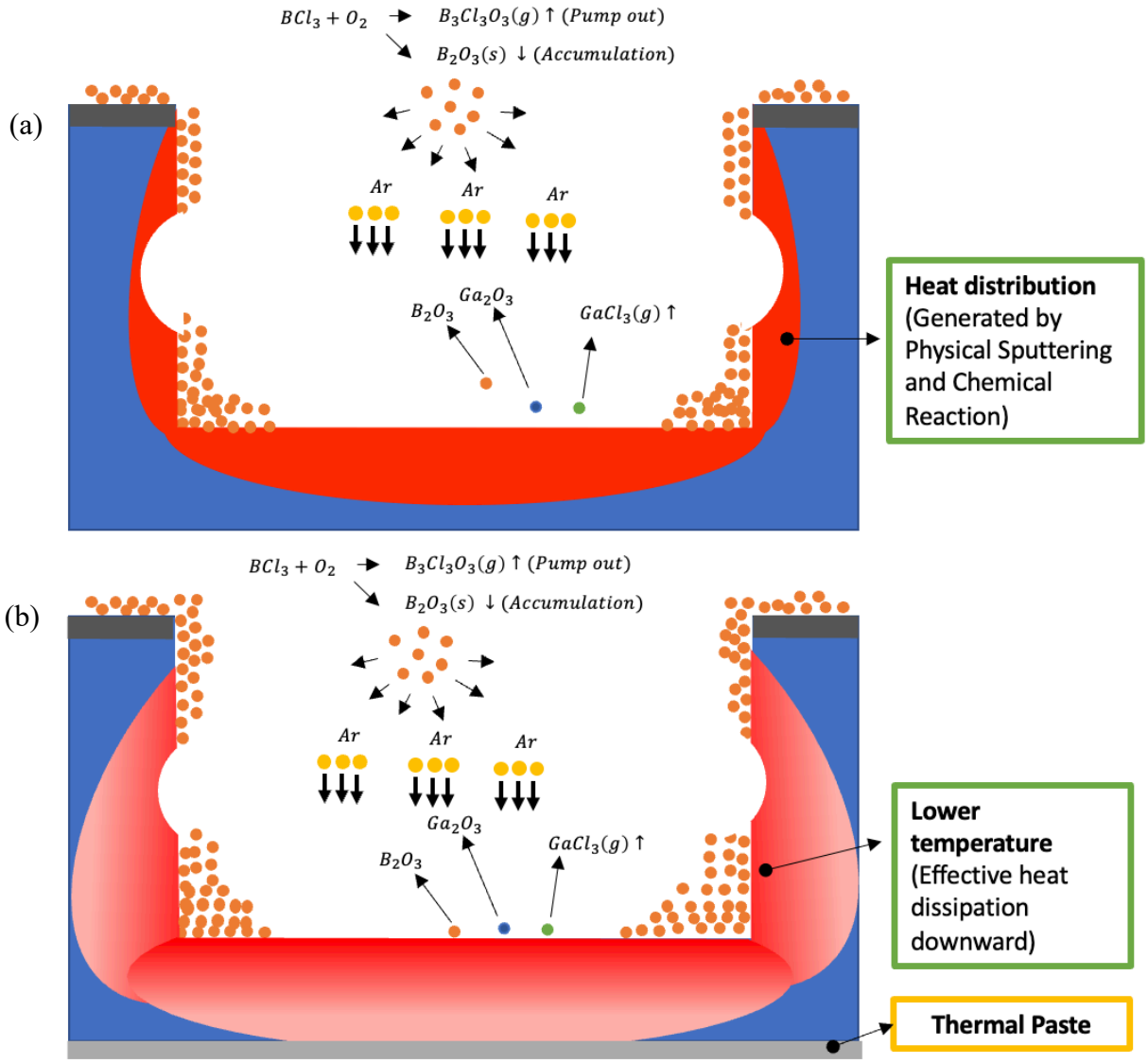


Figure 4.5-12 Illustration of thermal paste can reduce the fin waist narrowing. The red areas represent the heat distribution. (a) Etching without thermal paste; (b) etching with thermal paste, which improve the heat dissipation through the substrate back side.

Additionally, the lower surface temperature can also decrease the etch rate by decreasing the activation of both chemical and physical reactions involved in the etching process on the sample surface. In the experiment, by applying thermal paste,

the vertical etch rate of the substrate decreased from 50 nm/min to 39 nm/min, which is coherent to the theory. Besides, from the observation, applying thermal paste also increased metal hard mask selectivity from 1:36 to 1:48. The reason could be that the metal hard mask is etched only via single physical sputtering, while both chemical and physical reactions influence the substrate etching. Therefore, the hard mask selectivity will increase with thermal paste.

4.5.2 Weak Factors

Likewise, the weak factors have less impact on the waist narrowing. With different values of weak factors, the waist narrowing stays at the same level with a slight fluctuation.

4.5.2.1 Fin Width

The fin width effects on waist narrowing are investigated on both trench etched substrate and fin etched substrate. In figure 4.5-13, the fin arrays were created by fin etching with 1.5 μm fin height, and fin width varied from 1 μm to 8 μm. The same waist narrowing of fins was observed in each case, shown in (figure 4.5-13c), from 1 μm with 170 ± 8 nm shown in figure 4.5-13a, to 8 μm with 173 ± 8 nm shown in figure 4.5-13b.

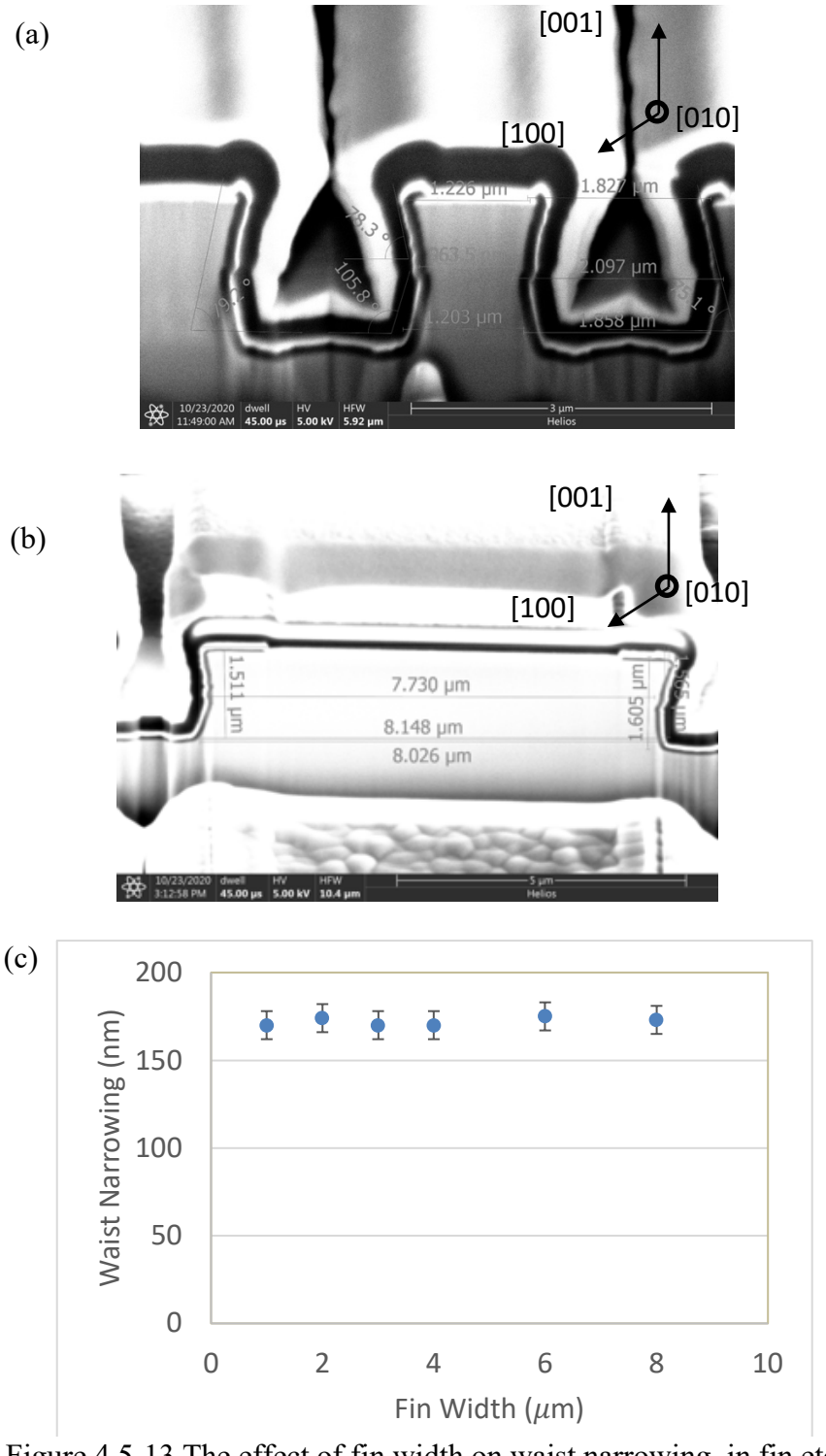


Figure 4.5-13 The effect of fin width on waist narrowing, in fin etched substrate. (a) The 1 μm wide fin with waist narrowing at 170 ± 8 nm, (b) 8 μm wide fin with waist narrowing at 173 ± 8 nm, (c) waist narrowing is around 170nm for all fins with different fin width, but same fin height and trench width. SEM taken by Kazuki Nomoto.

Same observations were obtained in trench etched substrate. In figure 4.5-14, the fin arrays all have fin height at 0.56 μm, trench width at 0.45 μm, but different fin width at 0.77 μm (figure 4.5-14a) and 0.37 μm (figure 4.5-14b). In both cases, the waist narrowing is around 3.9 ± 3nm.

Although the fin width can influence the survival rate of the fin arrays, the tolerance for the waist of narrow fins is not as high as the wider fins. However, based on the experiments stated above, the fin width is a weak factor of waist narrowing with the same survival condition. Based on the mechanism stated in 4.2, as long as the fins are survival, the waist narrowing generation mechanism is mainly related to trench areas. Therefore, the fin width is a weak factor generating waist narrowing.

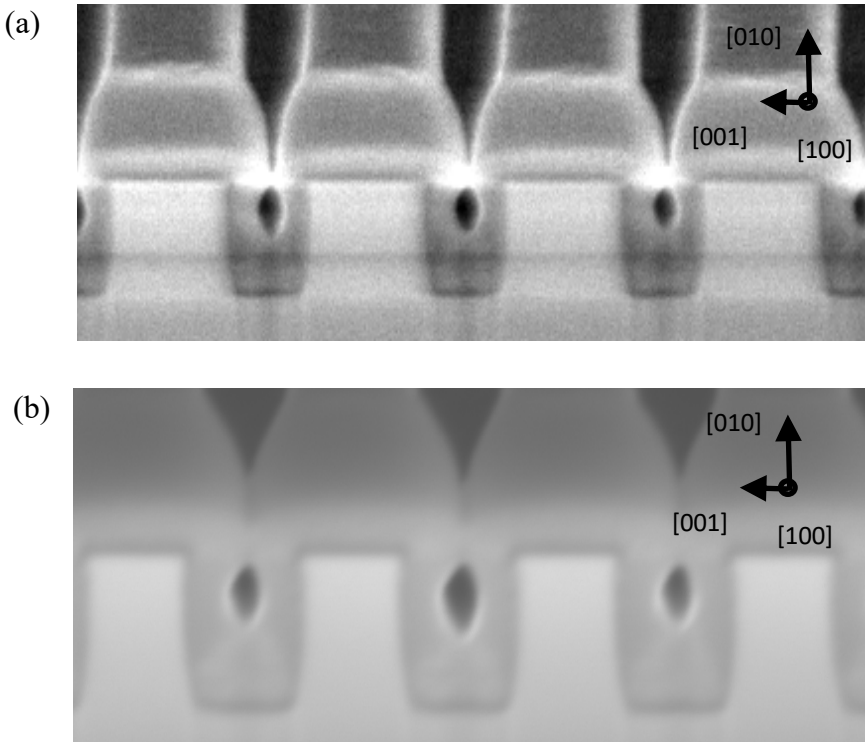


Figure 4.5-14 SEM pictures showing the effect of fin width on waist narrowing, in trench etched substrate. (a) The 0.77 μm wide fin with waist narrowing at 3.9 ± 3 nm, (b) 0.37 μm wide fin with waist narrowing at 3.9 ± 3 nm. Waist narrowing is around same for all fins with different fin width, but same fin height and trench width. SEM taken by Mingli Gong.

4.5.2.2 Fin Direction

The fin direction influence on the waist narrowing is investigated both in the fin arrays created by fin etching and trench etching. In figure 4.5-15, the fin arrays created by fin etching, orient from along [0 1 0] direction to perpendicular to [0 1 0] direction. In all four directions, the waist narrowing is around 100.5 ± 10 nm. Same observations are obtained in the fin arrays created by trench etching with thermal paste, where the fin directions orient from along [1 0 0] direction to perpendicular to [1 0 0] direction, shown in (figure 4.5-16). The waist narrowing of these fin arrays is around 1.8 ± 8 nm. Therefore, the fin direction is also a weak factor of waist narrowing. Based on the mechanism stated in 4.2, the etching is dominated by physical sputtering, where the chemical bond energy is not a strong factor. Thus, the fin direction is a week factor generating waist narrowing, and the sidewall surface temperature is around the same in the conditions with different fin directions.

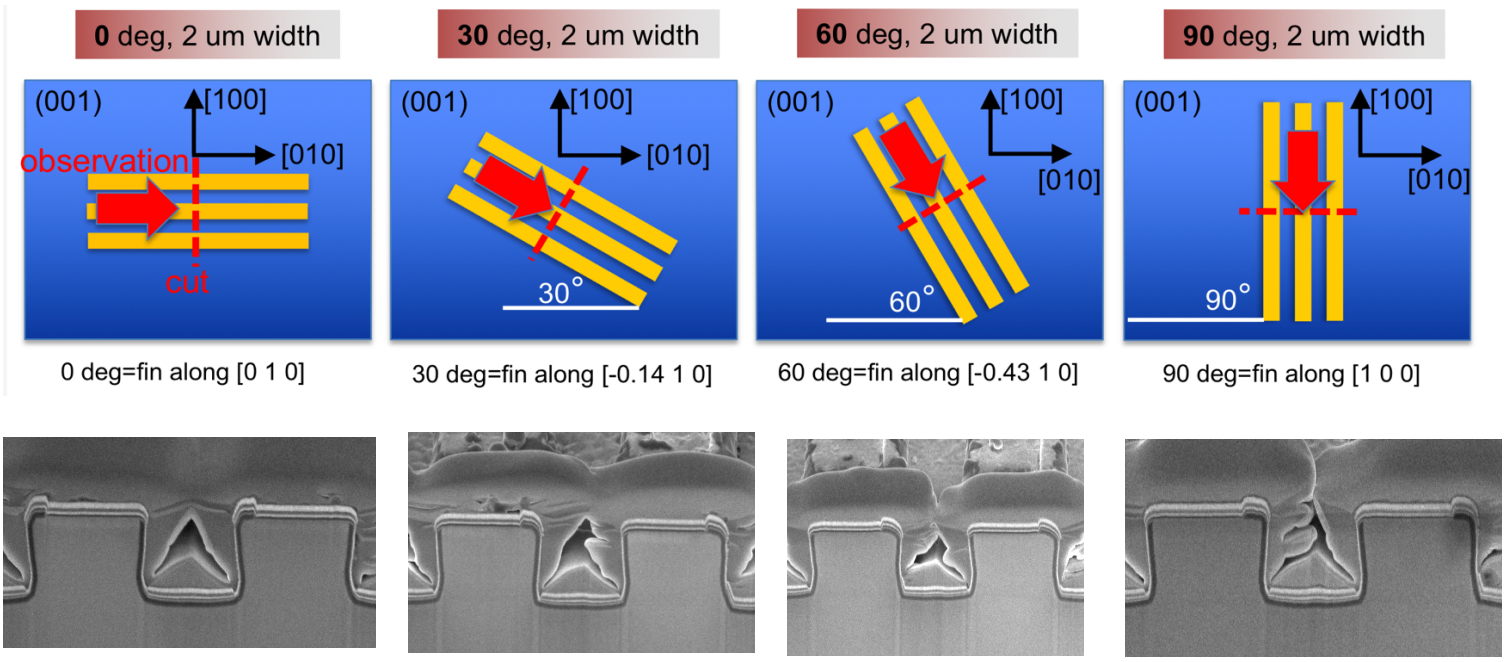


Figure 4.5-15 The fin arrays created by fin etching, where the fin height is 1.6 μm, trench width is 2.2 μm. The angle between fin direction and [1 0 0] are 0-degree, 30- degree, 60-degree, and 90-degree. In all four cases, the waist narrowing is around 100.5 ± 10 nm. SEM taken by Wenshen Li.

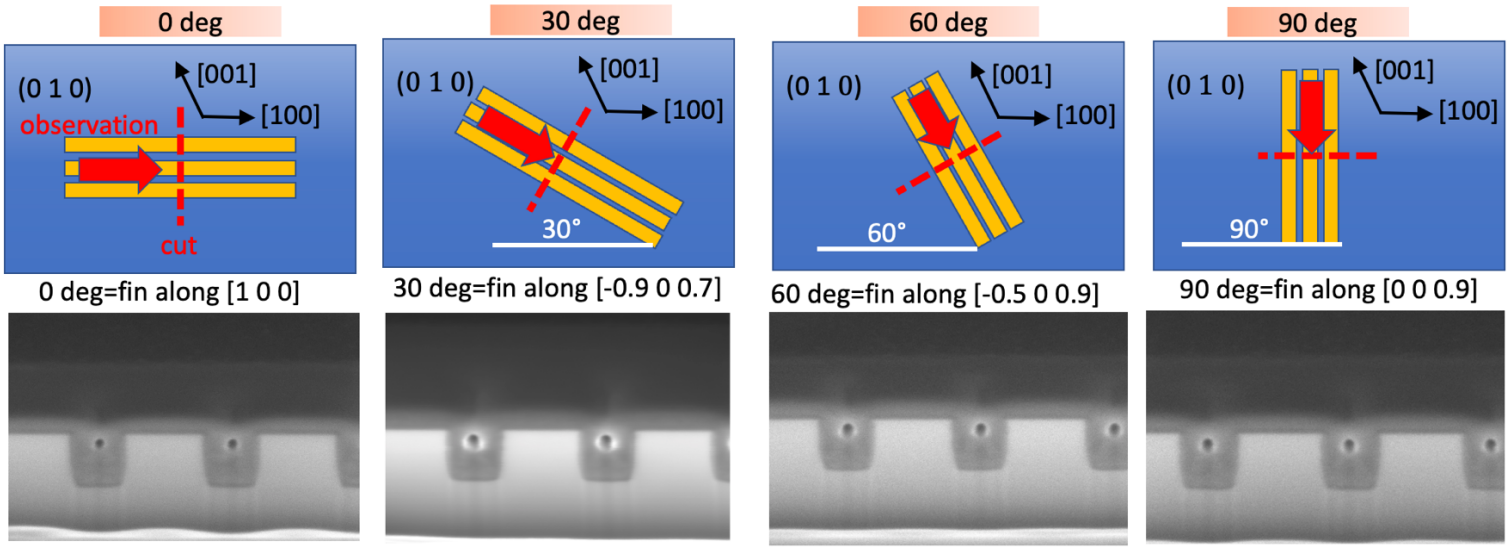
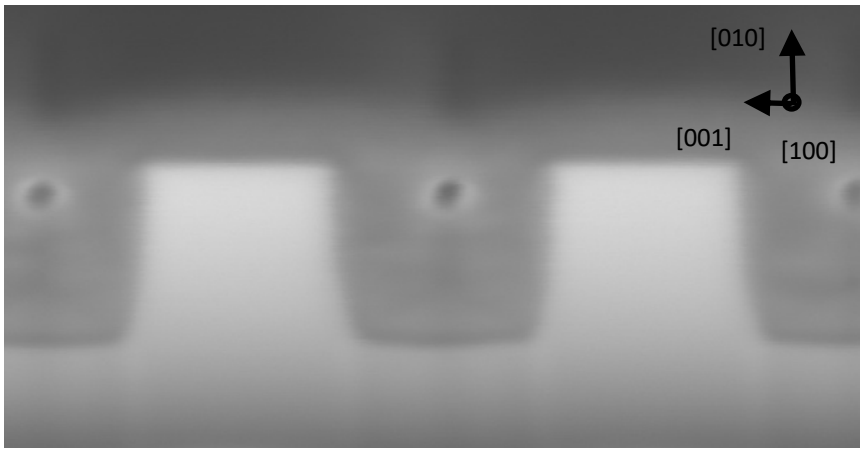


Figure 4.5-16 The fin arrays created by trench etching with thermal paste, where the fin height is 0.56 μm, trench width is 0.46 μm. The angle between fin direction and [0 1 0] are 0-degree, 30- degree, 60-degree, and 90-degree. The waist narrowing is around 1.7 ± 8 nm in all four cases, SEM taken by Mingli Gong.

4.5.2.3 Trench Length

In this experiment, the trench length is much larger than the trench width, which is mostly the case in the designing of FinFET. In order to investigate the influence of trench length on waist narrowing, the trench length of the fin arrays is varied from 0.78 μm to 19.80 μm. In these fin arrays, the trench width is 0.45 μm, the fin height is 0.56 μm. The fin arrays were created by trench etching with thermal paste. As shown in figure 4.5-17, the fin arrays with the trench length at 0.78 μm has the waist narrowing at 3.9 ± 3 nm (figure 4.5-17a), the fin arrays with the trench length at 19.8 μm has the waist narrowing at 3.9 ± 3 nm (figure 4.5-17b). Furthermore, the same waist narrowing is observed in the fin arrays with different trench lengths, shown in (figure 4.5-18).

(a)



(b)

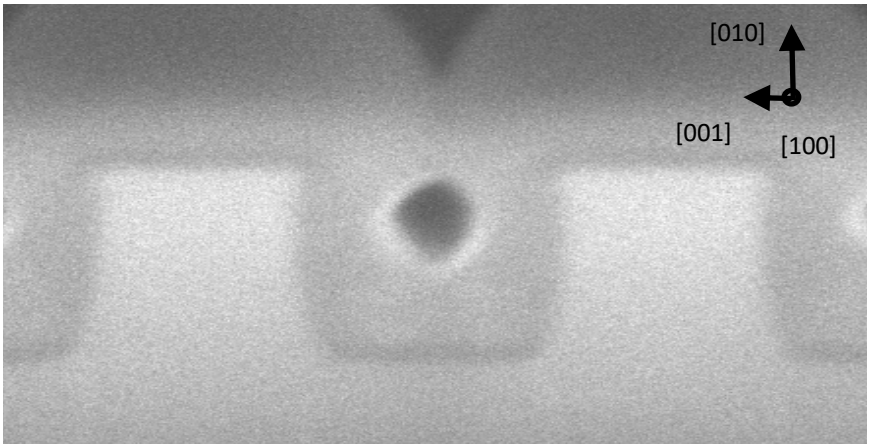


Figure 4.5-17 SEM pictures showing the effect of trench width on waist narrowing, in trench etched substrate with thermal paste. The fins all have 0.37 μm wide and 0.56 μm high fin, the trench width is all at 0.45 μm. (a) The trench length is 0.78 μm with waist narrowing at 3.9 ± 3 nm, (b) The trench length is 19.80 μm with waist narrowing at 3.7 ± 3 nm. Waist narrowing is around the same for both conditions, SEM taken by Mingli Gong.

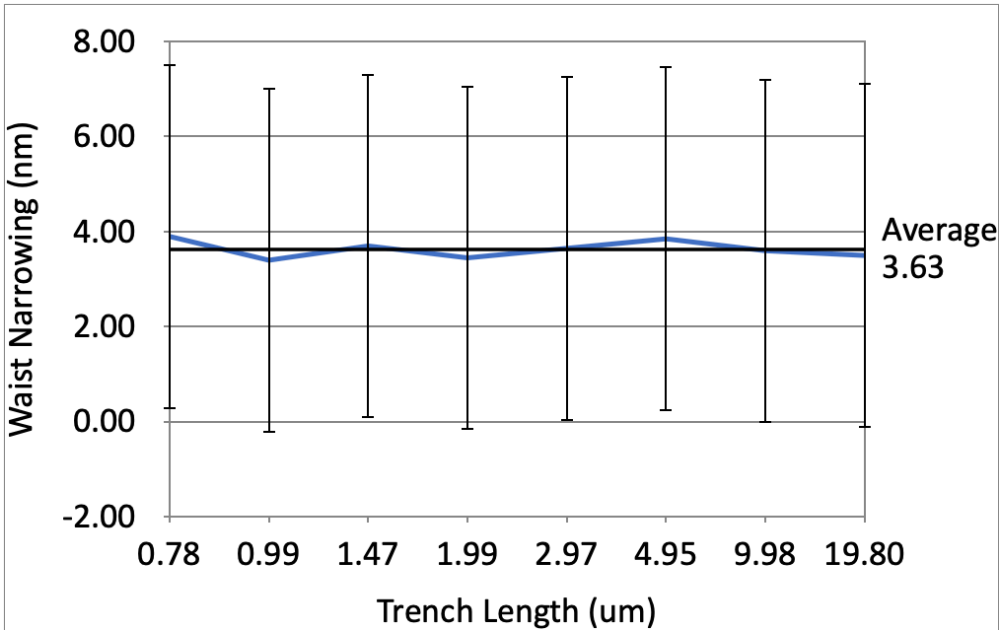


Figure 4.5-18 The effect of trench length on waist narrowing, in trench etched substrate with thermal paste. Waist narrowing is around 3.7 ± 3 nm for all fins with different trench length, but same fin height and trench width.

Based on the mechanism stated in 4.2, the trench along the trench length direction can be assumed to be extremely wide. According to 4.5.1.2, the extremely wide trench can have a sidewall close to straight due to the lower surface temperature (lower than B_2O_3 transformation temperature) brought by advanced heat dissipation. Therefore, the trench length can no longer influence the waist narrowing in the trench areas.

4.5.2.4 Number of Fins

The influence of the number of fins in fin arrays is also investigated. The number of fins varied from 2 to 40, while the fin width (0.37 μm) and height (0.56 μm), trench width (0.44 μm) are the same in the fin arrays. For the 5 fins arrays, the waist narrowing is around 3.9 ± 1 nm (figure 4.5-19a). For the 40 fins arrays, the waist narrowing is around 3.8 ± 1 nm (figure 4.5-19b). In figure 4.5-20, the waist narrowing

of all fin number conditions is around 4.0 nm. Therefore, the number of fins is not a strong factor in waist narrowing.

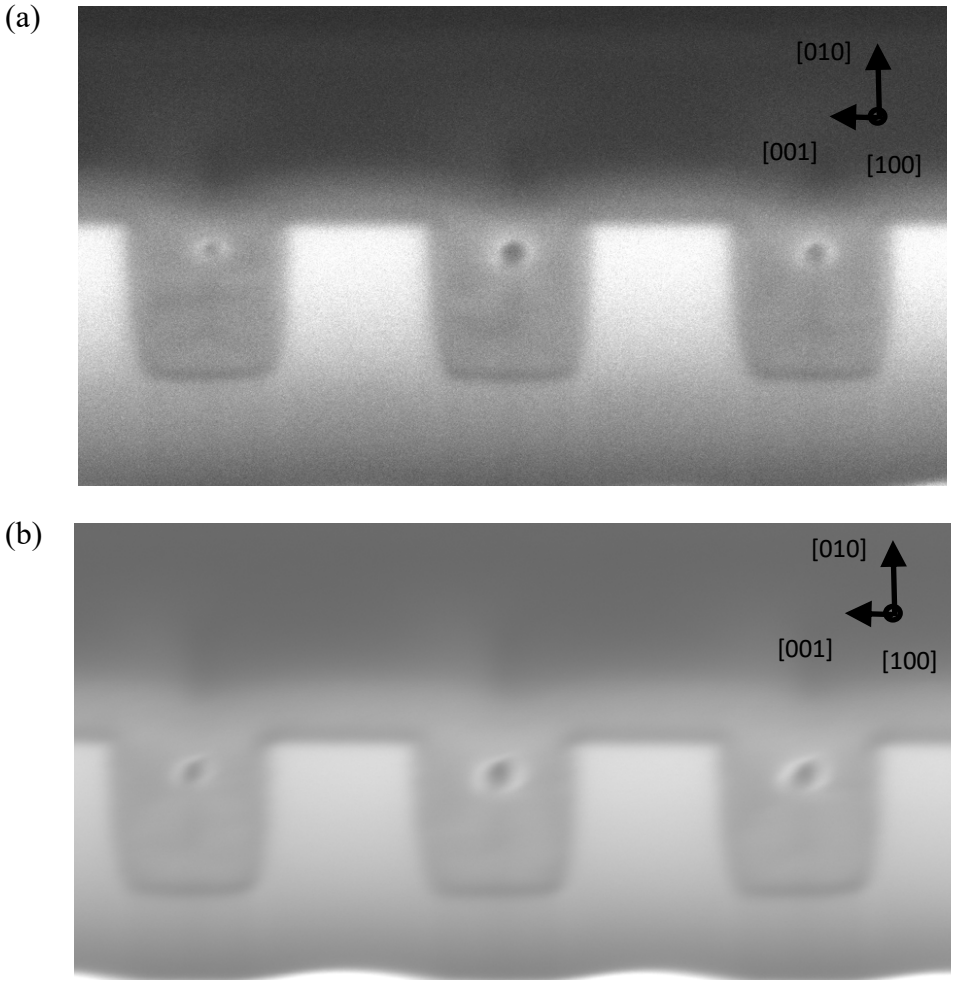


Figure 4.5-19 SEM pictures showing the effect of trench width on waist narrowing, in trench etched substrate with thermal paste. The fins all have 0.37 μm wide and 0.56 μm high fin, the trench width is all at 0.44 μm. (a) The number of fins is 5 with waist narrowing at 3.9 ± 1 nm, (b) The number of fins is 40 with waist narrowing at 3.8 ± 1 nm. Waist narrowing is around the same for both conditions, SEM taken by Mingli Gong.

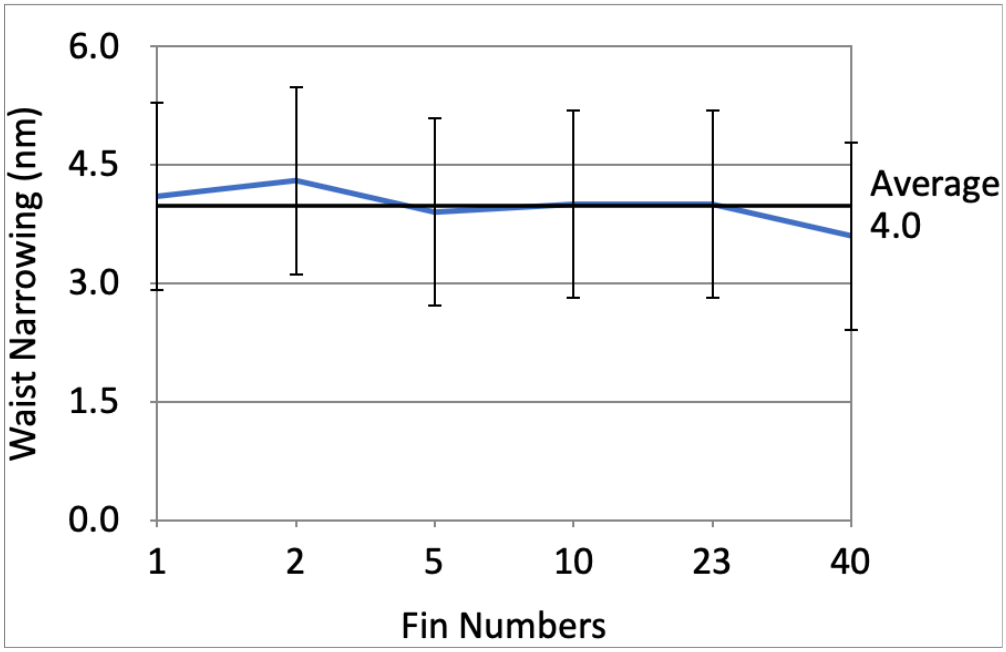


Figure 4.5-20 The effect of number of fins on waist narrowing, in trench etched substrate with thermal paste. Waist narrowing is around 4.0 ± 1 nm for all fins with different number of fins, but same fin height and trench width.

Based on the mechanism stated in 4.2, waist narrowing is mainly related to the trench area reaction. As long as the dimensions and temperature conditions of trenches remain the same, the number of fins is not a strong factor of waist narrowing.

4.6 Overall Fin Geometry

Besides the waist, the fins have common geometries, including the trapezoid fin shape neglecting the waist, boat-shaped trench, and height difference between the inside and outside of the outmost fin.

4.6.1 Trapezoid Fin Shape

Among all the etch conditions, whether the arrays are trench etched or fin etched, with thermal paste or without thermal paste, or in any substrate, the fins have an overall trapezoid shape, neglecting the waist, shown in figure 4.6-1.

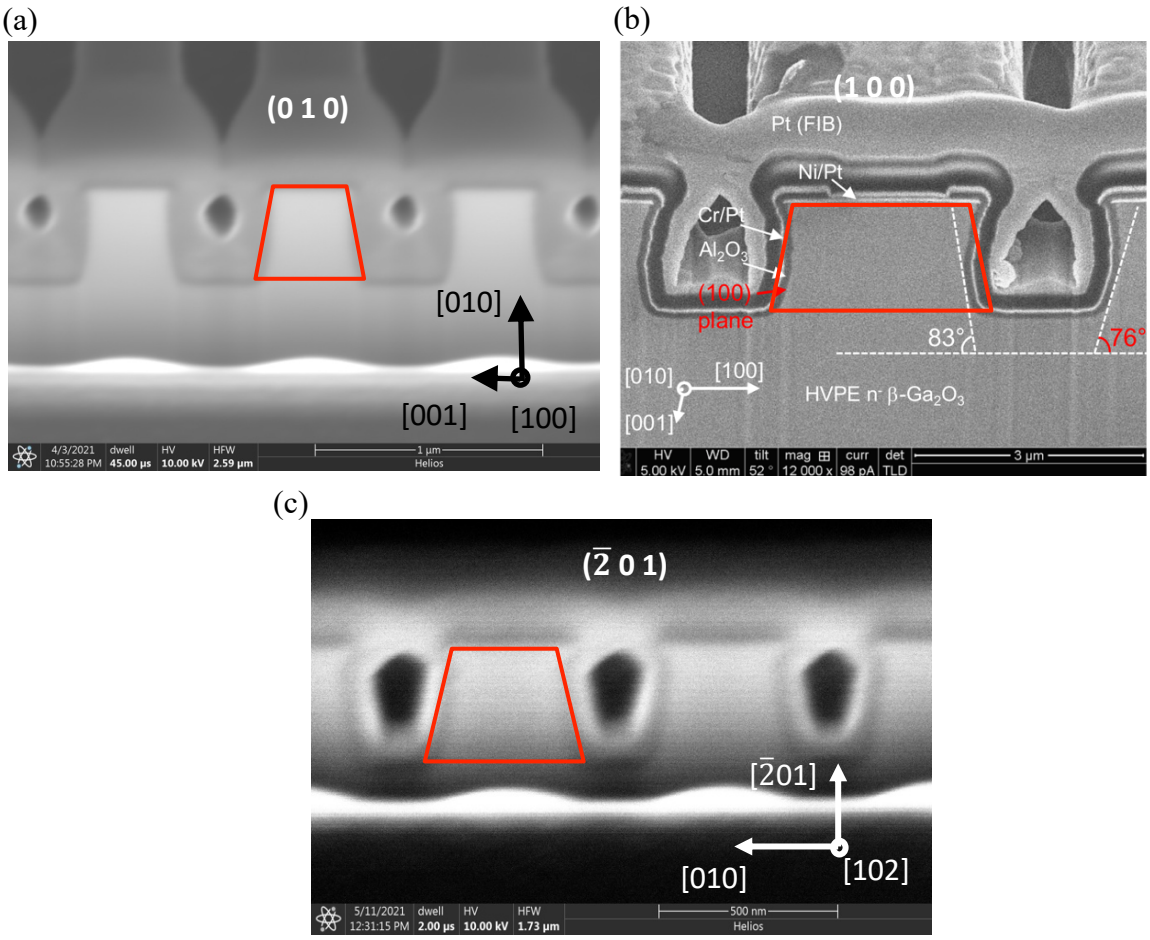


Figure 4.6-1 The trapezoid fin shape in fin arrays. (a) Trench etched fin arrays in (0 1 0) substrate with thermal paste. (b) Fin etched fin arrays in (1 0 0) substrate. (c) Trench etched fin arrays in ($\bar{2}$ 0 1) substrate, SEM taken by Mingli Gong.

Based on the mechanism introduced in 4.2, the trapezoid shape is formed due to the B_2O_3 accumulation in the corner. Because of the geometry of the corner, the B_2O_3 partials favor to pile up in the corner area. In this case, the bottom of the corner area is not able to be sufficiently etched. Therefore, the bottom of the trench will gradually shrink and form the vanishing stairs, which can be seen as a sloop, illustrated in (figure 4.6-2). From the fin aspect, the fins will have a trapezoid shape.

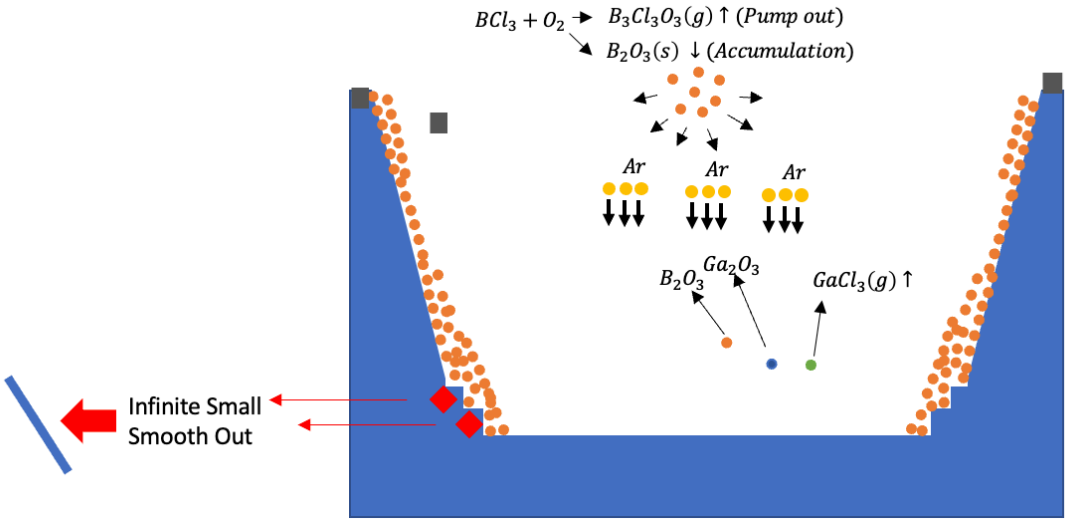


Figure 4.6-2 Illustration of trapezoid fin shape formation. The corner B_2O_3 particles imped bottom etching, and the trench bottom shrinks gradually. The infinite small stairs can be assumed as a smooth sloop and forming the trapezoid fin shape.

4.6.2 Boat-shape Trench Bottom and Trench Height Difference

In all conditions, the trenches in the fin arrays have a boat-shaped bottom, where the middle part of the trench is deeper than the corner part, shown in (figure 4.6-3). The wider trench is, the more obviously the boat-shaped trench has. The 0.8 μm long trench has 40 ± 2nm difference, while the 5 μm long trench has 92 ± 2nm difference.

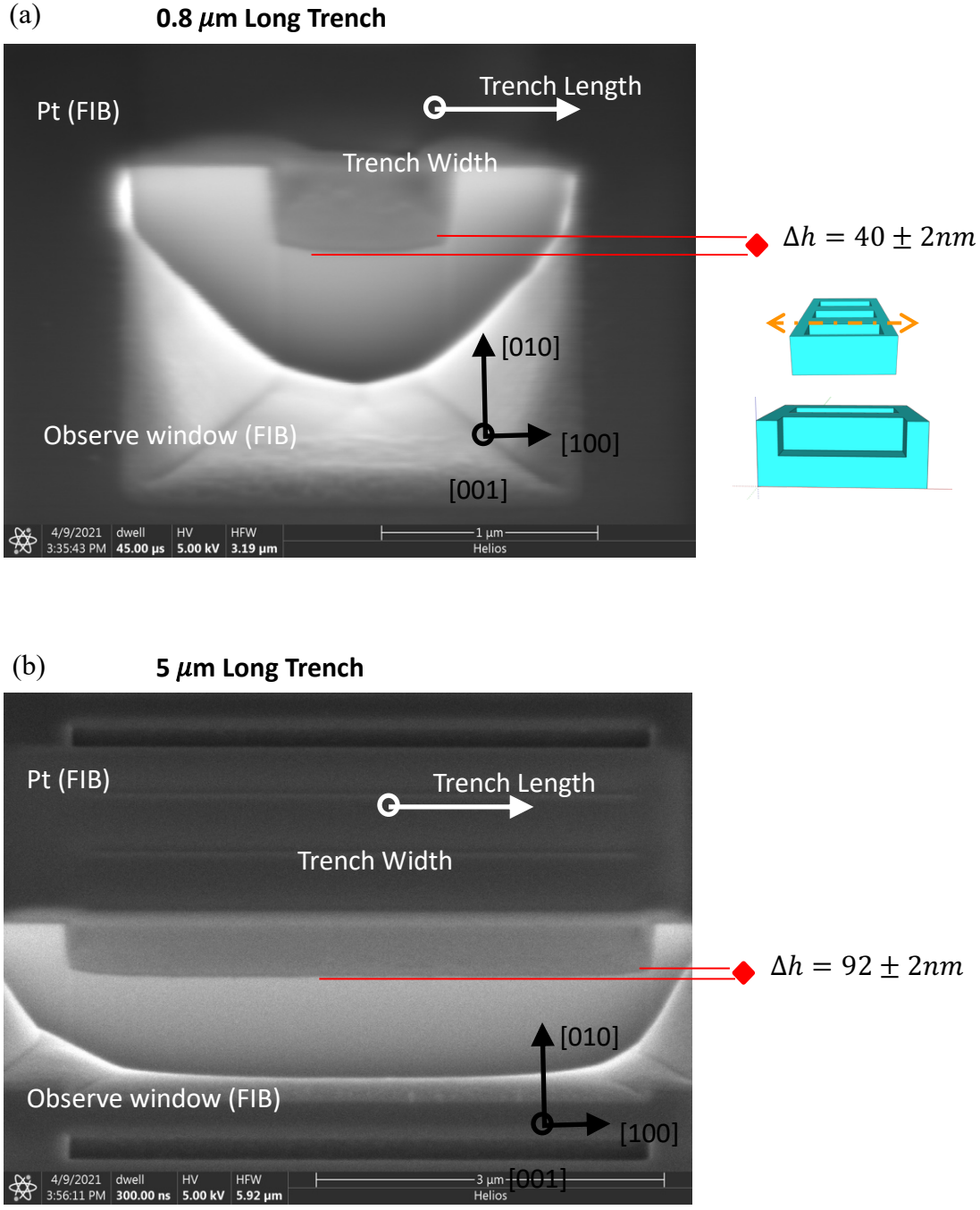


Figure 4.6-3 The boat-shape trench in trench etched fin arrays with thermal paste. (a) The 0.8 μm long trench has 40 ± 2nm depth difference; (b) the 5 μm long trench has 92 ± 2nm depth difference, SEM taken by Mingli Gong.

Based on the mechanism mentioned in 4.2, the center of the trench bottom has more chance to have chemical and physical etching, plus an opener geometry allows better by-product discharging. This geometry advantage can lead to a higher surface temperature and clearer sample surface to continue the etching, so a higher etch rate happens in the mid of the trench bottom and forming a boat-shaped trench bottom, with a deeper central part and shallower edge part, illustrated in (figure 4.6-4).

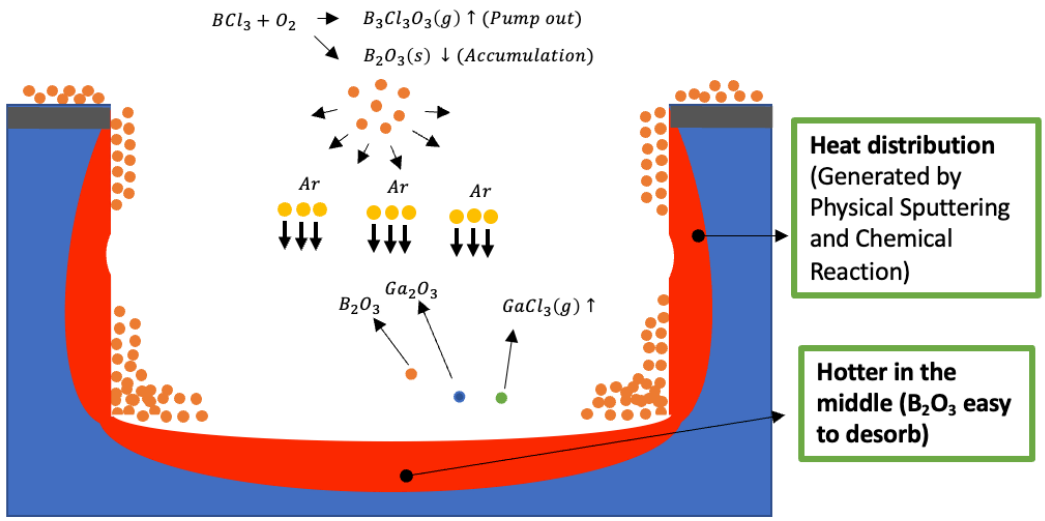


Figure 4.6-4 Illustration of boat-shape trench boat formation. The higher local surface temperature, which lead to the higher etch rate and higher depth in the center area of the trench.

It has also been observed that the outside of the outmost fin is deeper than the inside. In figure 4.6-5, the depth difference is around 64±2nm. For the same reason stated before, the outside can be regarded as an extremely wide trench, where the etch

rate is higher than the inner trenches, leading to a deeper etch depth on the outside than inside.

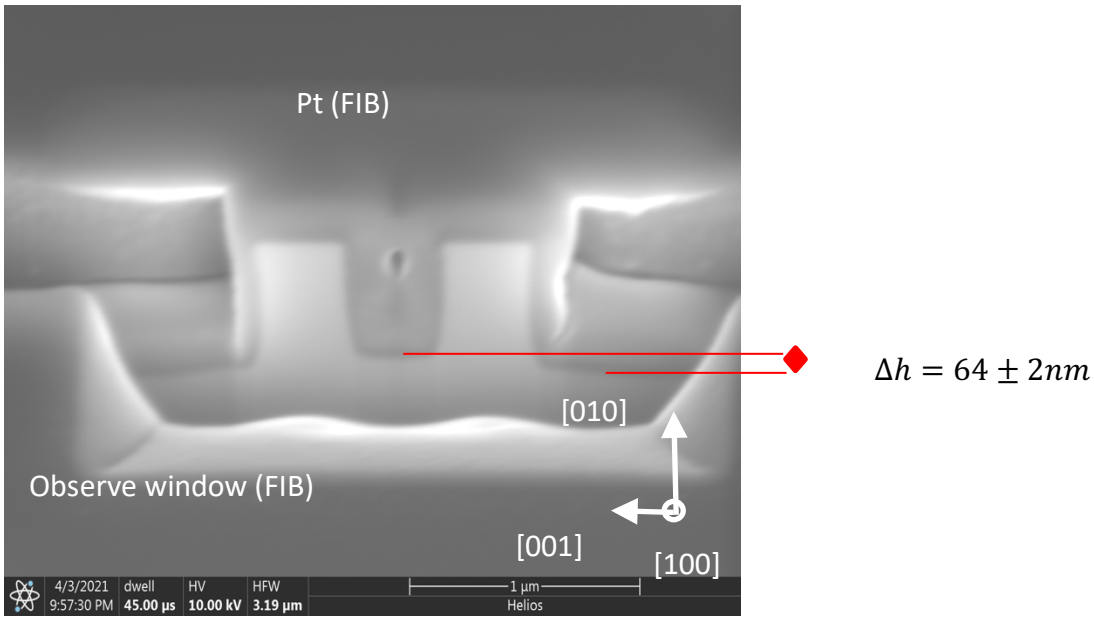


Figure 4.6-5 The depth difference of outmost fin inside and outside trenches. In this two-fin fin array, the outside trench is 64±2nm deeper than the inside one, SEM taken by Mingli Gong.

4.7 Other Factors Impacting Ga_2O_3 Fin Etching

In this section, the other effect factors during the etching will be covered to make this study more complete. These effect factors studies are all from the literature published before. They include crystallographic plane, chamber pressure, involved gas, and etch power. These factors can influence etch rate, surface roughness, surface feature homogeneity, even the waist narrowing based on the hypothesis state in 4.2. The following discussions are all under the conditions that neglect the surface reconstruction and other factors that can influence the involved chemicals' lattice, such as differing bond angles and energies.

4.7.1 Crystallographic Plane

As mentioned in the introduction part, gallium oxide has different structures in different crystallographic planes, therefore, different surface energy. From figure 4.7-1, the (1 0 0) has the lowest surface energy, while (1 0 1) has the highest one [32]. In the surface energy perspective, the lower surface energy means the chemical etching is harder to process, so the (1 0 0) plane will have the lowest etch rate. However, based on the experiment of J. Hogan, etc. (figure 4.7-2), the etch rate is about the same in all three planes, (1 0 0), (1 0 0), and ($\bar{2}$ 0 1) [31]. Based on the mechanism introduced in 4.2, this could come from the domination of physical reaction, where the rate of removing the B2O3 layer is the etch rate limit factor. Therefore, the etch rate of each plane is about the same as observed in the experiment of J. Hogan, etc.

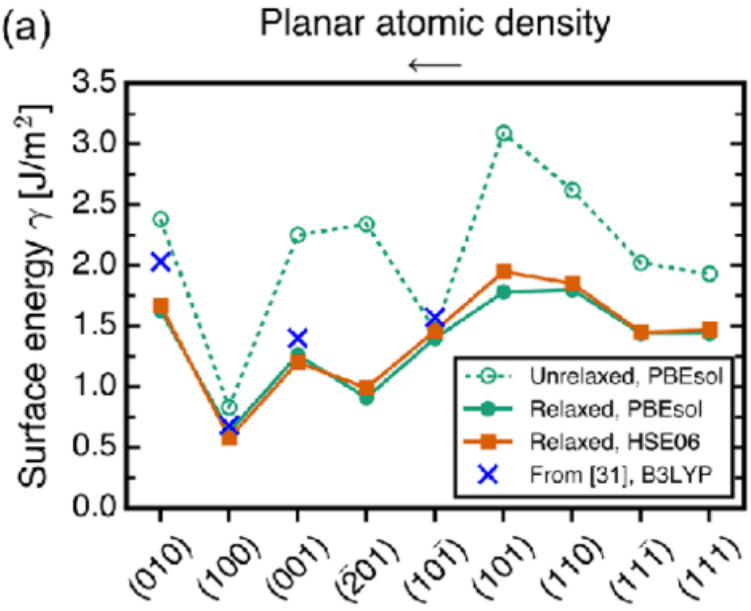


Figure 4.7-1 The surface energy of different plane of β-Ga_2O_3 [32].

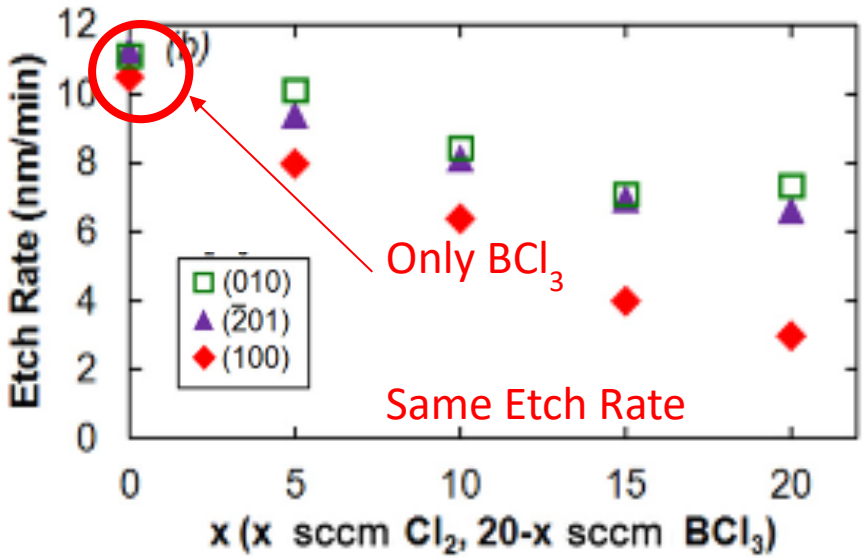


Figure 4.7-2 β-Ga_2O_3 etch rate of (0 1 0), (1 0 0) and ($\bar{2}$ 0 1) in different Cl_2, BCl_3 gas composition. For the pure BCl_3 case, all three directions have the same etch rate [31].

4.7.2 Pressure

With higher chamber pressure, there will be higher etchant ion density, which will lead to a greater frequency of collision between ion and substrate. The increasing amount of ion bombardments can generate a higher etch rate [31] and severe waist narrowing due to the increasing heat brought by ion bombardments, based on the hypothesis stated in 4.2.

4.7.3 Etchant Gas

The etchant gas has two parameters that can be changed, including flow rate and gas compositions. The flow rate is related to the chamber pressure. With a higher flow rate, the etch rate and waist narrowing could increase accordingly. Cl_2 is under much attention for the gas composition since the Cl_2 is widely used in GaN etching with good performance [31, 33]. However, with the increase of Cl_2 percentage in either

pure BCl_3 or BCl_3/Ar mixed atmosphere, the Ga_2O_3 etch rate dramatically decreased [31, 33], shown in figure 4.7-2 and figure 4.7-3.

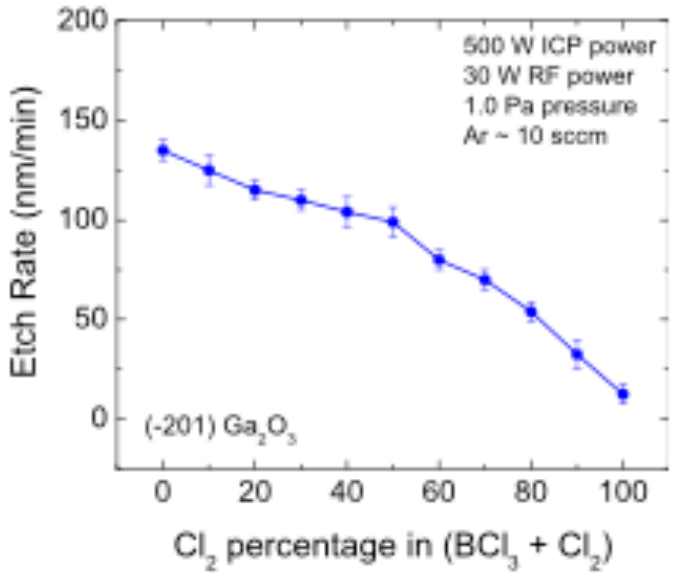


Figure 4.7-3 The etch rate decreases as the Cl_2 percentage increase, in Cl_2/BCl_3 Ar ICP plasma [33].

The rate decreasing when adding Cl_2 comes from the etching mechanism gradually switched from BCl_3 mechanism to Cl_2 mechanism, where the gallium oxide is etched not as sufficient as in BCl_3. In Cl_2/Ar atmosphere, the dominant reaction of etching is the chemical reaction between Cl_2 and Ga_2O_3 to remove Ga and O atoms from the substrates. The physical sputtering of Ar and Cl_2^+ is a minor part of etching [33]. However, the capability of Cl and Cl_2 to remove O is not as effective as BCl_3 on Ga_2O_3, as BCl_3 is a more effective scavenger of O. Therefore, with the increasing of Cl_2 percentage, the Ga_2O_3 etch rate will gradually decrease. This hypothesis can also be proved by the observation in figure 4.7-2, where the etchings on the (1 0 0) plane always have a lower etch rate with introducing Cl_2 and are more sensitive with Cl_2

percentage. Since the (1 0 0) plane has the lowest energy and consists of only O atoms, as mentioned in figure 4.7-1 and the introduction part, the chemical reaction will be more difficult to happen with lower surface energy and less effective scavenger of O, so the lowest etch rate on the (1 0 0) plane. Moreover, based on the theory in 4.2, the waist narrowing could be more severe without the protection of the B_2O_3 sidewall passivation layer.

Moreover, with the introducing of O_2, the etch rate can also decrease [31]. Based on the theory stated in 4.2, Since the O_2 can exacerbate the B_2O_3 formation, which can impede the etching and decrease the etch rate, but the waist narrowing can decrease due to the thicker sidewall passivation film.

4.7.4 Power

With the increasing of etching power, both inductively coupled plasma (ICP) and reactive ion etching (RIE), the Ga_2O_3 etch rate will increase accordingly [31], due to the higher energy of sputtering species and higher surface temperature, which could probably worsen the fin waist. Moreover, the surface roughness can also increase with increasing power [31] because the species with greater kinetic energy can cause more surface damage. Moreover, it has been observed by J. Hogan, etc., that the increasing of RIE power can lead to worse surface roughness than ICP's [31]. The reason is likely due to the different etchant gas ionization mechanisms between ICP and RIE. In the RIE system, a larger forward bias is needed for ionizing etchant gas and accelerating them towards the sample surface, which can create a rougher surface [31]. Besides, the inhomogeneous surface feature has been observed on the RIE etched sample surface with all RF powers [31]. These uneven etch profiles could result from incomplete

removal of etch products, which act as micro-masks locally since the RF power in RIE appears to be so low that the plasma cannot be homogenously ignited. However, this uneven etch profile is not detectable in the ICP system because the plasma generated by a magnetic field before applying forward plasma enables much higher plasma densities in ICP compared to RIE. This difference in the etching mechanism can also explain that a much lower forward bias is needed to reach a similar etch rate in ICP than RIE [31].

4.8 Conclusion

In order to decrease the waist narrowing during the Ga2O3 fin ICP-RIE etch in BCl3/Ar, the thermal paste is needed for each round of etching. Besides, during the fin geometry design, it is better to apply wider and shallower trench in the fin arrays as possible. Moreover, if a higher etch rate is required, it is recommended to increase ICP power rather than RIE power, increase pressure, or gas flow rate. However, the worsen waist narrowing and rougher sample surface need to be anticipated.

5 Conclusion and Future Work

In summary, this study completed the fabrication and analysis of the first All-Cornell β-Ga_2O_3 MOSFETs. The decent performance of this work provides good experience in designing and fabrication of β-Ga_2O_3 field-effect transistors, and it is also a solid base of the study in β-Ga_2O_3 FinFETs. The success of the work in β-Ga_2O_3 FinFETs contributes to the first demonstration of the threshold voltage modulation by fin width in β-Ga_2O_3 lateral fin transistors. Furthermore, the study in β-Ga_2O_3 fin ICP-RIE etching fin waist narrowing effect factors provides the community an essential peek in this area for the first time. For the future, with the detailed study in β-Ga_2O_3 fin etching with ICP-RIE, the denser fin arrays with an increased number of fins in Ga_2O_3 FinFETs can be implied, and a better performance can be anticipated with it. Also, better solutions to improve the ohmic contact for lower on-resistance are still eager to be found. For the etching study, more etch tests are needed to be confirmed the assumptions about the influence of sample plane, power, pressure, and etchant gas on waist narrowing.

APPENDIX A

1. Process flow of β-Ga_2O_3 MOSFETs

0	Hall Measurement	Nanomatrics Hall System	
1	cleaning	cleaning 1	acetone and IPA with sonication, DI rinse
2		cleaning 2	1:1 DHF (5 min) and rinse in DI+N2 blow
3	Lithography for mesa isolation (Stepper) FET8MESA (3X3)	pre treatment	180 oC, 5 min. Cool for 30 sec
4		spin PR (SPR700)	5000 rpm, 30 s
5		pre baking	95 oC, 60 sec
6		exposure(AS200)	exposure time: 0.2 sec. Align on R.
7		post exposure bake	115 oC, 60 sec
8		development	726 MIF, 60 sec
9		rinse	DI 30 sec+N2 blow
10		Check patterns	
11	Clean	descum(Glen1000)	recipe #3 (RIE = 100 W), 2 mins
12	Dry etching for mesa isolation	ICP etching (PT770)	with xing 4, for 3 min , aim for 150 nm etched hight
13	Remove PR	remove PR masks	Acetone and IPA with sonication (5 min each), DI rinse
14	Observation	P10	etched height: 166.4 nm
15	Lithography for ohmic contacts (Stepper) FET8OHM (3X3)	cleaning	acetone and IPA with sonication (3 min each), DI rinse
16		cleaning 2	1:1 DHF (5 min) and rinse in DI+N2 blow
17		pre treatment	180 oC, 5 min. Cool for 30 sec
18		spin PR (nLOF 2020)	7000 rpm, 30 s
19		pre baking	115 oC, 60 sec
20		exposure(AS200)	exposure time: 0.2 sec. Align on R.
21		post exposure bake	115 oC, 60 sec
22		development	726 MIF, 60 sec
23		rinse	DI 30 sec+N2 blow
24		check patterns	
25		post bake	115 oC, 5 mins
26		descum(Glen1000)	recipe #3 (RIE = 100 W), 2 mins
27		surface cleaning1	30:1 BOE (1 min), DI rinse, N2 blow
28		surface cleaning2	1:1 DI/HCl (1 min), DI rinse, N2 blow

29	Ti/Au deposition	deposition	Ti/Au =50/110 nm (< 1e-6 Torr)
30		lift-off	1165, acetone, IPA with sonication (5 min), DI rinse
31	Observation	OPTM	check patterns
32	Anealing	RTA	470 C in N2 for 1 min
33	Check Ohmic Contact	Cascade Probe station	check TLM & Hall pattern
34	cleaning	cleaning	acetone and IPA with sonication, DI rinse
35	Gate Dielectric	dielectric deposition (Oxford ALD)	Al2O3/SiO2=19nm/1nm, plasma300C
36		Check the thickness (Woollam Spectroscopic Ellipsometer)	Al2O3/SiO2=20.882nm/1.060nm
37	Lithography for gate (Stepper) F8GATE3X3	cleaning	acetone and IPA with sonication (3 min each), DI rinse
38		pre treatment	180 oC, 5 min. Cool for 30 sec
39		spin PR (nLOF 2020)	7000 rpm, 30 s
40		pre baking	115 oC, 60 sec
41		exposure(AS200)	exposure time: 0.2 sec. Align on O.
42		post exposure bake	115 oC, 60 sec
43		development	726 MIF, 60 sec
44		rinse	DI 30 sec+N2 blow
45		check patterns	
46		Descum (Glen 1000)	recipe #3 (RIE = 100 W), 2 mins

47	Gate metal deposition	deposition	Ni/Au=50/100 nm
48		lift-off	1165, acetone and IPA with sonication (5 min), DI rinse
49	Observation	OPTM	check patterns
50	Lithography forContact Hole (Stepper) FET8CHOLE	cleaning	acetone and IPA with sonication (3 min each), DI rinse
		pre treatment	180 oC, 5 min. Cool for 30 sec
		spin PR (SPR700)	5000 rpm, 30 s
		pre baking	95 oC, 60 sec
		exposure(AS200)	exposure time: 0.2 sec. Align on R.
		post exposure bake	115 oC, 60 sec
		development	726 MIF, 60 sec
		rinse	DI 30 sec+N2 blow
		Check patterns	
	Wet etch	Hard Baking	115 oC, 5 min
		Descum (Glen 1000)	recipe #3 (RIE = 100 W), 2 mins
		Timed wet etching	6:1 BOE 40 s
		lift-off	1165, acetone and IPA (5 min), DI rinse
51	Measurement	Cascade probe station	

2. Process flow of β-Ga_2O_3 FinFETs

#	Process	Process/Equipment	Conditions
0	Observation	AFM	2x2 surafce roughness
1		OPTM	Sample surface
2	Hall Measurement	Nanomatrics Hall System	
3	cleaning	cleaning 1	acetone and IPA with sonication, DI rinse
4		cleaning 2	1:1 DHF (5 min) and rinse in DI+N2 blow
5	Lithography for mesa isolation (Stepper) FET8MESA (3X3)	pre treatment	180 oC, 5 min. Cool for 30 sec
6		spin PR (nLOF2020)	7000 rpm, 30 s
7		pre baking	95 oC, 60 sec
8		exposure(AS200)	exposure time: 0.2 sec. Align on R.
9		post exposure bake	115 oC, 60 sec
10		development	726 MIF, 60 sec
11		rinse	DI 30 sec+N2 blow
12		Check patterns	
13	Clean	descum(Glen1000)	recipe #3 (RIE = 100 W), 2 mins
14	Cr/Ni Mask	deposition	Cr/Ni=20/30 nm (< 2e-6 Torr)
15		lift-off	1165, acetone, IPA with sonication (5 min), DI rinse
16	Clean	Descum (Glen 1000)	recipe #6 (RIE = 500 W), 3 mins
17	Dry etching for mesa isolation	ICP etching (PT770)	Xing 4, for 5 min; aim for 250 nm etched hight
18	Remove Cr/Ni Mask	Remove Cr/Ni Mask	Cr etchant 40C
19	Observation	P10	etched height: ___ nm
20	Recess Etching	deposition	Ni=20 nm
21		JEOL 9500	EBL
22		AJA Ion Mill	Ion milling
23		Zeiss Supra SEM	Etch width /surface
24		Dry etching (PT770)	Xing 4, for 5 min; aim for 240 nm etched hight
25	Remove Ni Mask	Remove Ni Mask	Ni Etchant
26	Observation	Zeiss Supra SEM	sidewall
27	Remove dry etching damage	HF Treatment	HF (10 min) and rinse in DI+N2 blow
28	Observation	Zeiss Supra SEM	sidewall
29		P10	biggest feature etched height: ___ nm
30		AFM	etched height: ___ nm

31	Lithography for ohmic contacts (Stepper) FET8OHM (3X3)	cleaning	acetone and IPA with sonication (3 min each), DI rinse
32		cleaning 2	1:1 DHF (5 min) and rinse in DI+N2 blow
33		pre treatment	180 oC, 5 min. Cool for 30 sec
34		spin PR (nLOF 2020)	7000 rpm, 30 s
35		pre baking	115 oC, 60 sec
36		exposure(AS200)	exposure time: 0.2 sec. Align on R.
37		post exposure bake	115 oC, 60 sec
38		development	726 MIF, 100 sec
39		rinse	DI 30 sec+N2 blow
40		check patterns	
41		post bake	115 oC, 5 mins
42		descum(Glen1000)	recipe #3 (RIE = 100 W), 2 mins
43		surface cleaning1	30:1 BOE (1 min), DI rinse, N2 blow
44		surface cleaning2	1:1 DI/HCl (1 min), DI rinse, N2 blow
45	S/D metal deposition	deposition	Ti/Au =50/110 nm (< 1e-6 Torr)
46		lift-off	1165, acetone, IPA with sonication (5 min), DI rinse
47	Observation	OPTM	check patterns
48	Anealing	RTA	470 C in N2 for 1 min
49	Check Ohmic Contact	Cascade Probe station	check TLM & Hall pattern
50	cleaning	cleaning	acetone and IPA with sonication, DI rinse
51	Gate Dielectric	dielectric deposition (Oxford ALD)	Al2O3/SiO2=19nm/1nm, plasma300C
52		Check the thickness (Woollam Spectroscopic Ellipsometer)	Al2O3/SiO2=___nm/___nm

53	Lithography for gate (Stepper) F8GATE3X3	cleaning	acetone and IPA with sonication (3 min each), DI rinse
54		pre treatment	180 oC, 5 min. Cool for 30 sec
55		spin PR (nLOF 2020)	7000 rpm, 30 s
56		pre baking	115 oC, 60 sec
57		exposure(AS200)	exposure time: 0.185 sec. Align on O.
58		post exposure bake	115 oC, 60 sec
59		development	726 MIF, 60 sec
60		rinse	DI 30 sec+N2 blow
61		check patterns	
62		Descum (Glen 1000)	recipe #3 (RIE = 100 W), 1 mins
63	Gate metal deposition	Odd hour evap	Ni/Au=50/100 nm
64		lift-off	1165, acetone and IPA with sonication (5 min), DI rinse
65	Observation	OPTM	check patterns
66		zeiss Supra SEM	
67	Lithography forContact Hole (Stepper) FET8CHOLE	cleaning	acetone and IPA with sonication (3 min each), DI rinse
68		pre treatment	180 oC, 5 min. Cool for 30 sec
69		spin PR (SPR700)	5000 rpm, 30 s
70		pre baking	95 oC, 60 sec
71		exposure(AS200)	exposure time: 0.2 sec. Align on R.
72		post exposure bake	115 oC, 60 sec
73		development	726 MIF, 60 sec
74		rinse	DI 30 sec+N2 blow
75		Check patterns	
76	Wet etch	Hard Baking	115 oC, 5 min
77		Descum (Glen 1000)	recipe #3 (RIE = 100 W), 2 mins
78		Timed wet etching	6:1 BOE 40 s
79		lift-off	1165, acetone and IPA (5 min), DI rinse
80	Measurement	Cascade probe station	
81	PDA	cleaning	acetone and IPA with sonication (3 min each), DI rinse
		RTA	350 C in N2 for 1 min

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