DEMONSTRATION OF FERROELECTRIC HZO UNDER THE GATE OF ALN/GAN HIGH-ELECTRON-MOBILITY TRANSISTORS

A Thesis

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by

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ABSTRACT

Gallium Nitride-based high electron mobility transistors (GaN HEMTs) represent the forefront of technological innovation. Renowned for their high speed and power capabilities, GaN HEMTs are utilized across a diverse array of sectors, including telecommunications, power electronics, aerospace, defense, industrial, medical, and consumer electronics. Integrating GaN with an aluminum nitride (AlN) barrier enhances speed, power output, and thermal management. Traditional HEMTs, however, are reaching their physical limits. This thesis investigates the addition of a ferroelectric hafnium zirconium oxide (HZO) layer beneath the gate of AlN/GaN HEMTs to overcome these limitations. This is achieved through the use of the remnant polarization of ferroelectrics to modulate the threshold voltage and demonstrate the ability for memory, giving GaN HEMTs improved device performance and more functionality. Through the development of multiple HEMT devices with varying HZO thicknesses, hysteresis in device output currents is verified and alterable, exhibiting a threshold voltage tuning range of 0.5-1.2 V. Also addressed in this thesis are the challenges and uncertainties associated with processing devices and working with ferroelectrics, emphasizing the necessity for meticulous care throughout the process. In summary, this work lays the foundation for the benefits of incorporating ferroelectric layers under the gate of AlN/GaN HEMTs, paving the way for better devices in the future.

BIOGRAPHICAL SKETCH

Akshey Dhar received a Bachelor of Arts in Physics from the University of California, Berkeley in 2021. Following graduation he spent one year as a research assistant at the Energy Technologies Area in the Lawrence Berkeley National Laboratory, working on multi-harmonic electro-thermal spectroscopy devices.

He then pursued a Masters of Science degree in Materials Science and Engineering at Cornell University under Professor Debdeep Jena and Professor Grace Xing. His work was on developing HEMTs with a ferroelectric HZO layer under the gate.

Akshey is expecting to receive his Masters of Science in July 2024 and will pursue a PhD at Cornell University in the Electrical and Computer Engineering department starting August 2024.

For my family.

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I wouldn't be anywhere without my mom and my dad. Through all my ups

and downs, they have been there for me, keeping me happy and loved. Their constant support is what got me to where I am today and I am so grateful to have them in my life.

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CHAPTER 1

INTRODUCTION

1.1 Gallium Nitride High Electron Mobility Transistors

Everywhere we look, we witness many devices that utilize the power of semiconductors. From computers to cars, and even ceiling lights, semiconductors have become indispensable as we push ourselves towards future advancements.

For more than half a century, silicon(Si) has been the essential building block for most devices.[7] Without Si, our current level of technological advancement would probably be significantly limited. The properties of Si make it suitable for a wide range of applications. With its band gap of 1.1 eV, it is used in diodes, transistors, integrated circuits, microprocessors, etc. Alongside its electrical properties, the material's abundance and cost-effectiveness help drive down production costs, while its established manufacturing infrastructure and scalability support the mass production of increasingly smaller and more powerful devices.

As the amount of computations run by different processors increases, the demand for faster speeds and higher power outputs increases. With the transition to using artificial intelligence everywhere, from coding to creating images to driving vehicles, there is a necessity for faster computing speeds. While Si is widely used across various applications, it is approaching its physical limits in terms of output and cannot satisfy increasing demands. Many other materials have been proposed and are currently being used to achieve these high

demands, but the go-to material is gallium nitride.

Gallium nitride(GaN) has emerged as the next generation candidate for high speed and high power applications due to its high mobility, higher electron saturation velocity and high breakdown field.[8] Table 1.1 shows different material properties relative to developing effective devices. From the table we can see that GaN possesses better parameters than the conventional Si in almost every category. With its wide bandgap, GaN is able to operate at even higher voltages, frequencies and temperatures than previous commonly used semiconductors. This has led to GaN becoming one of the most popular semiconductors in the past two decades.

Material	E_{gap} (eV)	E_C (MV/cm)	μ ($cm^2/V-s$)	v_{sat} (x$10^7 cm/s$)	σ_{therm} (W/cm-K)
Silicon	1.12	0.3	1440	1.0	0.3
InP	1.34	0.5	5400	3.9	0.68
GaAs	1.42	0.52	9400	0.9	0.55
GaN	3.4	3	1400	2.4	2.5
AlN	6.2	15	450	1.4	3.4
SiC	3.3	3	900	0.8	4.2

Table 1.1: Materials properties of relevant materials [1]

One of the most important properties of GaN is the intrinsic polarization of the material.[9] GaN can be found in three different crystal structures, α-phase (wurtzite), β-phase (zinc blende), and rock salt structure (Figure 1.1). While the rock salt phase is only stable at high pressures and the zinc blende phase is metastable, the wurtzite structure is thermodynamically stable at room temperature and pressure. As a result, the wurtzite phase has piqued the interest of many researchers. The wurtzite structure occupies a hexagonal crystal structure and has a six fold rotational symmetry. Notably, the structure does not have an inversion center along the c-axis of the crystal. This gives rise to the crystal

being piezoelectric, and thus makes GaN a polar material.

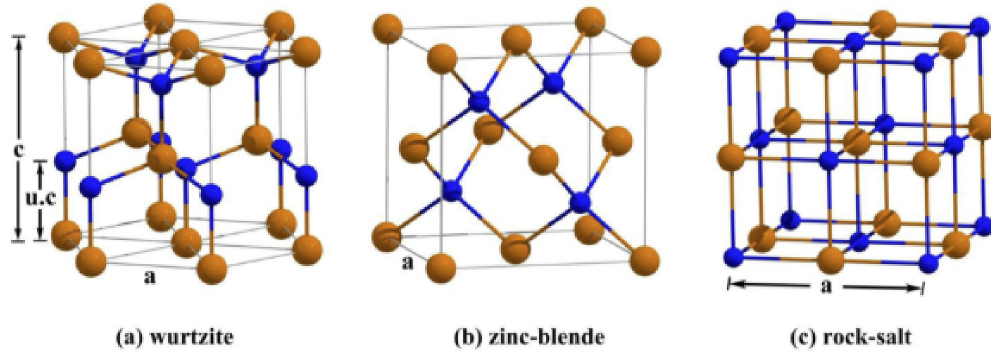
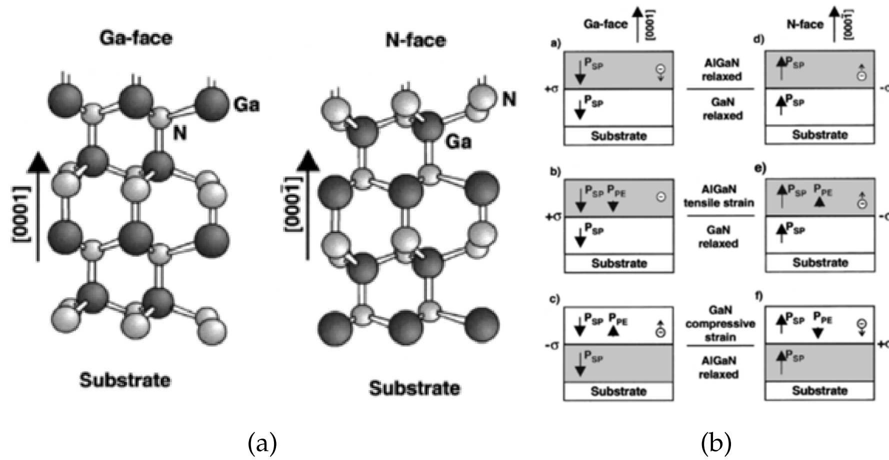


Figure 1.1: Different structures of GaN (a) α-phase (Wurtzite) (b) β-phase (Zinc-blende) (c) Rock salt phase. Ga and N atoms are shown in brown and blue color, respectively [3]

With the combination of GaN and another polar material, like AlGaN, in a heterostructure, a two dimensional electron/hole gas(2DEG/2DHG) can be formed.[10][11] Figure 1.2 illustrates the resulting charge profiles of developing a heterostructure with two different polar materials. The difference in the polarization between the GaN and AlGaN layers causes a significant electric field at the heterojunction interface. The polarization-induced electric field at the heterojunction interface causes electrons to accumulate at the interface between the GaN and AlGaN layers. The name two dimensional electron gas originates from electrons being confined in an essentially two dimensional layer. With the electrons confined to a thin region in the GaN layer and a high quality crystal structure, the resulting electron mobility becomes very high, giving devices the name high electron mobility transistors(HEMTs). The higher mobility in these devices allows for higher speed, frequency and power operations. These properties make GaN a strong choice for usage in applications such as RF amplifiers, microwave transmitters, and power electronics.



(a) (b)

Figure 1.2: Polarization of GaN and the resulting charges in an AlGaN/GaN heterostructure [4]

1.1.1 Aluminum Nitride

As device architecture progresses and transistors are scaled down, it is important to choose materials that provide the best results to maximize the properties and performance of the devices. While the conventional AlGaN/GaN HEMT device structure provides high speeds and high power outputs, aluminum nitride(AlN) as a barrier and buffer material offers more beneficial properties.

When calculating the limits of GaN for high power and high frequency applications, the values far eclipse the best data found for fabricated GaN HEMTs. While the limit of a device is usually determined by its material properties, in this case it is determined by the efficiency of the devices. Much of the power dissipation in GaN HEMTs is lost as heat. With heat being the performance limiting factor, it is essential to use a material that most effectively draws heat away from the active region. AlN boasts an exceptionally high thermal conductivity, around 3.4 W/cm-K, which is considerably higher than that of many other materials used in semiconductor devices.[12] By using AlN as a buffer material,

its superior thermal conductivity enables more efficient heat dissipation from the active regions of the device. Additionally, by incorporating AlN barriers, devices can operate at higher power densities and sustain longer operational lifetimes without overheating. This thermal advantage not only enhances the overall efficiency of the device, but also contributes to the development of more compact and powerful electronic systems.[13]

Like GaN, AlN possesses a hexagonal wurtzite crystal structure (Figure 1.3), making it a polar material. The polarization value of AlN is larger than that of GaN and AlGaN. This leads to a larger polarization induced electric field and consequently a higher 2DEG density. When compared with AlGaN and InAlN barriers, an AlN barrier is able to generate a higher 2DEG density at a fraction of the barrier thickness. This can be used very effectively in the scalability of devices when compared to other common top barrier semiconductors.[14]

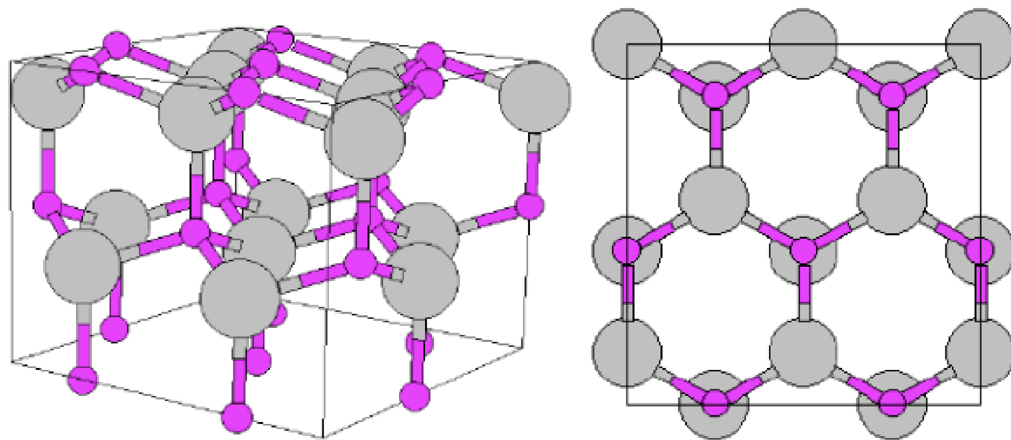


Figure 1.3: Wurtzite structure of AlN crystal. The gray sites represent Al atoms while the colored sites represent the N atoms.[5]

Another issue that arises during scaling is the increase in short channel effects. It has been shown that when using an AlN barrier, short channel effects can ideally be prevented to a gate length of 10 nm.[1] Devices with AlN barriers

can also benefit from the high breakdown voltage and large band gap for high voltage operation.[15]

1.2 Ferroelectricity and FeHEMTs

Despite the high speeds achievable with AIN/GaN HEMTs, there remains a desire for improved device performances. One of the motivations for improvements stems from the fact that there is a fundamental limit to how fast transistors can be switched on and off: the Boltzmann Limit. A solution to passing this limit is by adding a ferroelectric layer to the device structure of a transistor.

Another roadblock for improving devices arises from the physical limitations on electron mobility through materials. An example of this problem is the existing bottleneck between the memory and logic interconnects in computer hardware as processing amounts increase. Only so much information can travel through wires at once, leading to increased computation times. One way to get around this problem is by merging both logic and memory in the same device/transistor. This can also be achieved by integrating ferroelectric materials into devices, allowing transistors to effectively possess their own memory.[6][16]

1.2.1 What is Ferroelectricity

Ferroelectricity is a property of materials that allow them to exhibit a switchable spontaneous electric polarization.[17] Similar to that of ferromagnetism in magnetic materials, by applying an external electric field to a ferroelectric material,

the spontaneous electric polarization is able to be switched.

The origin of ferroelectricity is related to the crystal structure of materials. The switching of polarizations is often caused by the displacement of ions in the crystal structure. Consequently, ferroelectrics must have a noncentrosymmetric crystal structure to exhibit this behavior. Ferroelectricity is also considered a subclass of pyroelectricity(ability to generate a temporary voltage or current when put under a temperature gradient and vice versa) and thus also a subclass of piezoelectricity(electric charge build up due to mechanical stress on the material).

The ability, not only to switch polarization states, but also to remember the state it was in, allows the material to develop a hysteresis loop. Figure 1.4 illustrates an example of a hysteresis loop for ferroelectric materials. When an electric field is applied, the polarization reaches a saturation point and then relaxes to a remnant polarization when the field is reduced to zero. The key property of ferroelectrics is their ability to have two distinct remnant polarization states depending on the electric field applied to the device. The two different states contribute towards a memory window for the devices.

One of the most common uses of ferroelectric materials today is in Ferroelectric Random Access Memory(FRAM) as a non-volatile way of storing information.[18][19] FRAM is able to use the two different remnant polarization states to represent binary information for a computer. FRAM boasts faster write speeds, lower power consumption and higher read/write endurance when compared to flash memory. Other uses of ferroelectric materials include ferroelectric capacitors for use in medical ultrasound machines and infrared cameras as well as sensors for detecting things like fires and vibration levels.

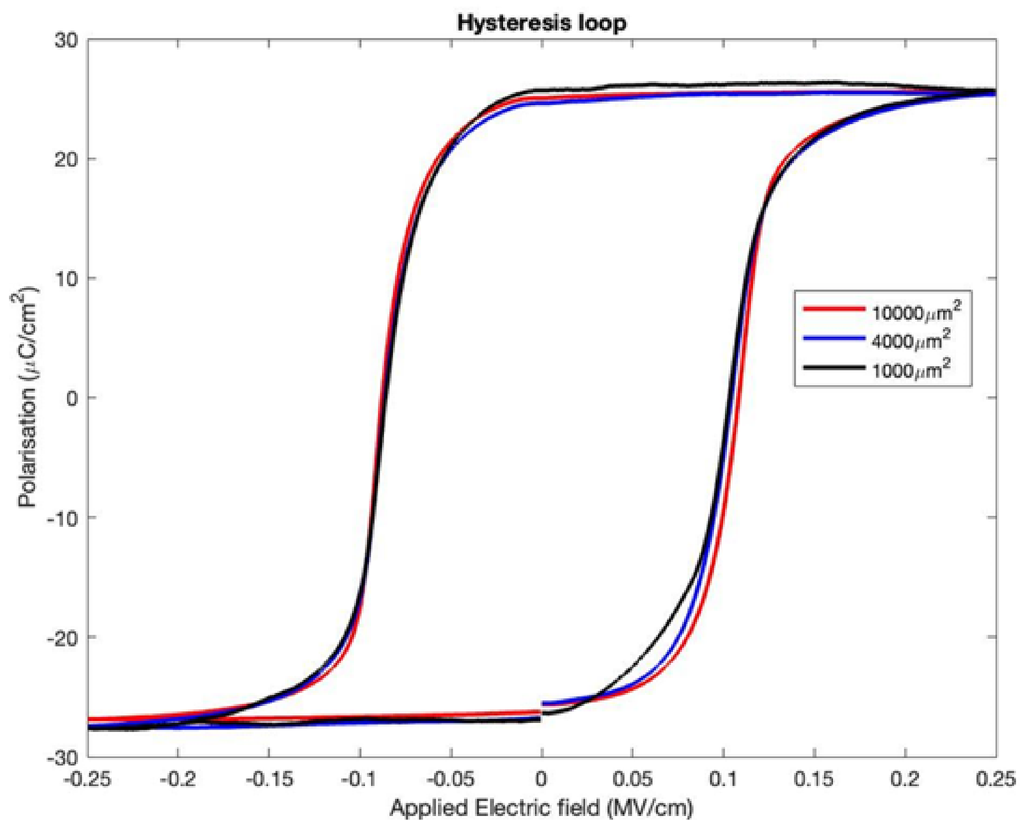


Figure 1.4: P-E loop of PZT measured at different pad areas

1.2.2 FerroHEMT/FeHEMTs

By adding a ferroelectric layer to a transistor it becomes a FeHEMT. There are multiple different configurations of where the ferroelectric layer is located. The different configurations would lead to the device acting as a FeHEMT or as FRAM. These different device architectures can be illustrated in Figure 1.5.

As ferroelectrics are already commonly known for their memory window, and thus their use as memory storage devices in FRAM, by adding a ferroelectric layer to a FET device, the memory window from the ferroelectric is integrated into the threshold voltage of the transistor.

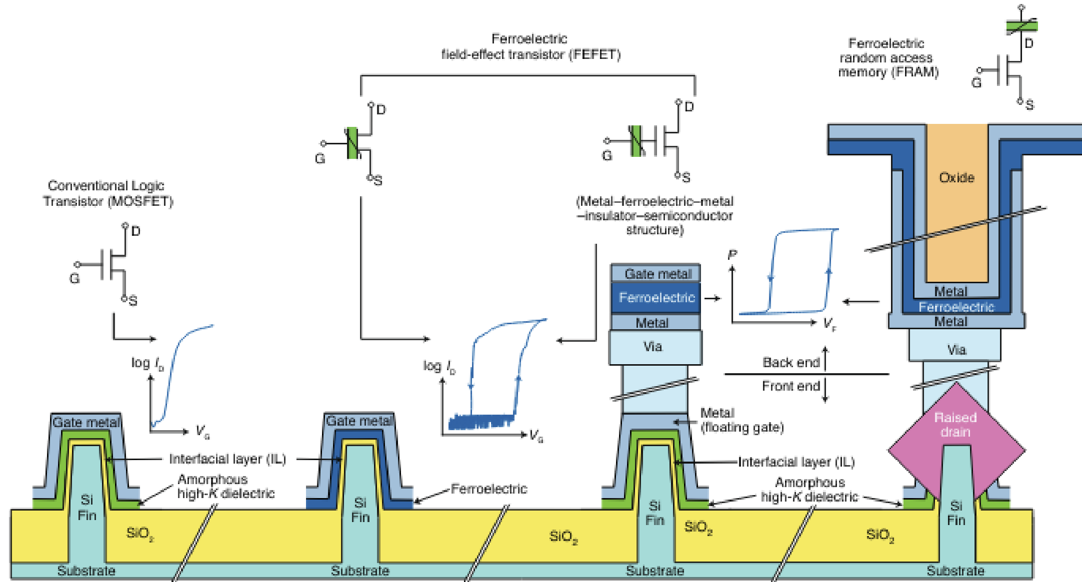


Figure 1.5: Schematic of different applications of ferroelectric materials used in transistor devices [6]

With HEMTs relying on the materials' polarizations to create a sheet charge, the integration of a ferroelectric, with its own high polarization effect, creates a unique effect of being able to modulate the 2DEG density.[20][21] By being able to modulate the 2DEG density, the threshold voltage of the device not only has a memory window, but also effectively becomes able to be tuned depending on the gate voltage applied to the device.

Another feature created by adding a ferroelectric under the gate is the reduction in the subthreshold slope of a transistor.[20] [22] Defined as the gate voltage needed to increase the drain current by an order of magnitude, the subthreshold slope is a good indicator to measure the switching rate of the transistor. The lower the value, the faster the device is able to switch between on and off states. At room temperature, transistors cannot have a lower subthreshold slope than 60 mV/dec. This is known as the Boltzmann Limit. However, due to the negative differential capacitance of ferroelectric materials, adding a ferroelectric to a

transistor allows it to break the Boltzmann Limit.[23][24][25]

Because ferroelectrics have a high dielectric constant, FerroHEMTs also exhibit additional distinctive features. Most processed devices generally have a gate dielectric layer. The primary function of this layer is to electrically insulate the gate electrode from the underlying semiconductor channel. This prevents current flow between the gate and the channel, allowing the gate to control the channel conductivity via an electric field rather than through direct contact and reducing the gate leakage.[26]

Historically, SiO_2 is the most common gate dielectric due to its excellent insulating properties and compatibility with silicon semiconductor processes. As devices are scaled smaller, the gate dielectric thicknesses are reduced as well. To achieve higher capacitance and better performance at smaller scales, high-k dielectrics are being used more frequently. Some popular high-k dielectrics used in Si processes are hafnium oxide and zirconium oxide.[27]

One other way having a gate dielectric alters the device properties is by influencing the threshold voltage of the transistor.[28] Both the thickness and the dielectric constant have an effect on the threshold voltage. Due to this, we should see a threshold voltage shift to more negative values when adding a ferroelectric layer under the gate.

1.3 Hafnium Zirconium Oxide

When choosing a ferroelectric material to place under the gate, the selection is very limited. One of the ferroelectric materials that is of special interest in the

realm of semiconductors is hafnium zirconium oxide(HZO). About a decade ago, it was found in previous studies that if you dope hafnium oxide(HfO_2) with zirconium(Zr), the material becomes ferroelectric. This is because the non-centrosymmetric orthorhombic phase is not observed in the HfO_2 phase diagram and only appears with the addition of dopant materials.[2]

Doping HfO_2 with various materials like Si, Y, Al, La, etc., induces the formation of the ferroelectric orthorhombic phase.[29][30] Among these dopants, Zr stands out as particularly promising. Specifically, the ferroelectric polarization reaches its maximum stability when the composition is balanced at $H_{0.5}Z_{0.5}O_2$.[31][32] The stability of maximum ferroelectric polarization at a 50-50 composition of $H_{0.5}Z_{0.5}O_2$ arises from the similar physical and chemical properties of Hf and Zr. This is beneficial from a processing point of view because it is able to be deposited through a simple ALD process of alternating between precursors HfO_2 and ZrO_2. Since the ratio is equal, it is much easier to realize a homogeneous material. Also due to the lower crystallization temperature of ZrO_2, the processing temperature can be much lower than that of other dopant materials.[33]

One of the main benefits of using HZO is that it can exhibit ferroelectricity at small thicknesses. Another main ferroelectric used in semiconductor processing is lead zirconium titanate (PZT). PZT is commonly used as a material for memory in FRAMs. While it has a large dielectric constant, its downsides are that it is not scalable. With a minimum thickness of 50 nm to achieve ferroelectricity, it will not be able to keep up with the demand of the shrinking of devices. However, HZO has reported to exhibit ferroelectricity at as thin as 5 nm.[19] Unlike PZT, HZO is also CMOS compatible.[34] Table 1.2 shows the compar-

isons between PZT and HZO. HZO shows the same polarization as PZT while also having a higher breakdown field.

	Units	PZT	HZO
Film Thickness	nm	≥ 50	5-40
Annealing Temperature	C	≥ 600	400-600
Remnant Polarization	$\mu C/cm^2$	20-40	1-40
Coercive Field	MV/cm	~0.05	1-2
Breakdown Field	MV/cm	0.5-2	1-2
Dielectric Constant	–	~1300	~30
ALD capability	–	Limited	Simple
CMOS compatibility	–	Has Pb and O_2 diffusion	Stable

Table 1.2: Comparison of different values between PZT and HZO [2]

1.4 Outline of This Work

This work focuses on the results of fabricating an AlN/GaN/AlN HEMT with the addition of a layer of ferroelectric HZO underneath the gate. The goal of the study aims to show the dependence of threshold voltage on the polarization of the HZO layer as well as the reduction of the gate leakage due to the high k properties of HZO. Additionally, this work aims to show the resulting memory window and the potential applications FeHEMTs have in memory/logic integration. This work will also address the possibilities of having subthreshold slopes less than 60mV/dec.

Chapter 2 explains the fabrication process of the FeHEMTs. It discusses the different masks used as well as a step by step procedure for developing the devices.

Chapter 3 verifies the ferroelectric properties of the HZO films using PUND/polarization measurements and EDX analysis.

Chapter 4 discusses the results measured from the FeHEMT devices with alloyed contacts. It will go over PUND, CV, transfer and output measurements.

Chapter 5 also discusses the results from FeHEMT devices, but with lower contact resistance regrown contacts instead of alloyed contacts.

Chapter 6 provides a comprehensive summary of the study's findings and conclusions. It discusses the potential applications of integrating HZO into HEMTs and offers insights into future directions for further research.

CHAPTER 2

DESIGN AND FABRICATION

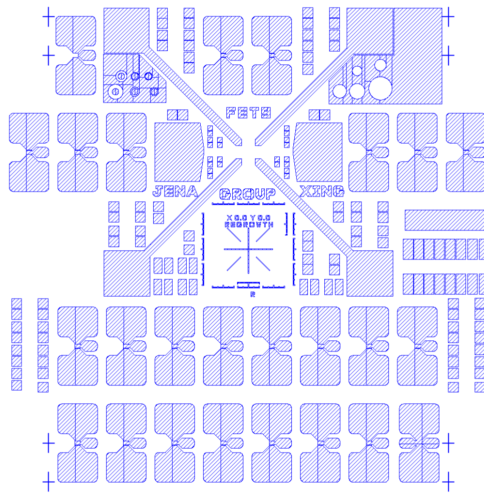
2.1 HEMT Design

The pattern of the masks, and subsequently the HEMTs, is designed by Dr. Kazuki Nomoto and is a common pattern used in the Jena-Xing group. There are a total of five masks used in all the processes needed. The different masks used are the regrown mask, the alignment mask, the device isolation mask, the ohmic contact mask and the gate contact mask and can be seen in Figure 2.1. I will now briefly go into the purpose and function of each mask, where a more in depth look at the fabrication process will be in the next section below.

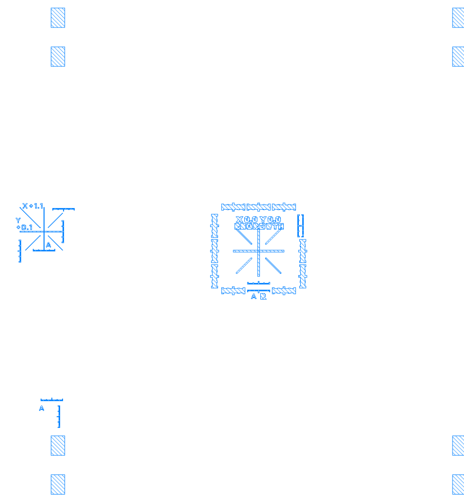
The regrown mask is one of two masks only used in the fabrication if regrown contacts are being used. If processing with alloyed contacts, this mask/step can be skipped. The mask details the regions desired for ohmic contacts. When using a positive resist, the areas for ohmic contacts are able to be etched and ultimately placed in an MBE for regrowth of n+ GaN.

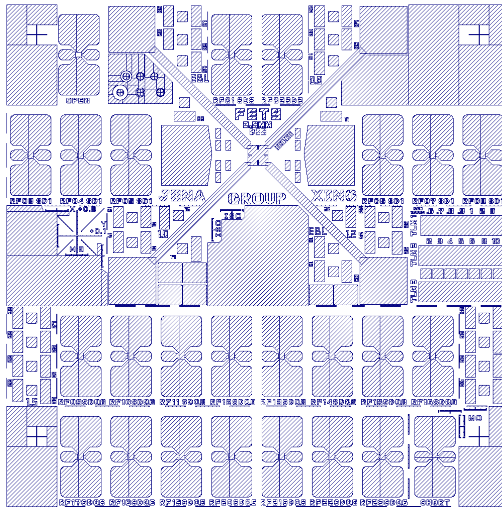
The alignment mask is the second mask that is only used in a regrown contact procedure. Its purpose is to provide an alignment mark to be etched which is still visible after the SiO_2 and poly-GaN are removed after coming out of the MBE. The following steps for a regrowth process use this alignment mark.

The device isolation mask is the first mask used for alloyed contacts and the third mask used for regrown contacts. It provides coverage around the source, drain, and gate contacts, as well as all other device features, to facilitate etching. This etch, as the name suggests, allows the devices to be isolated from each

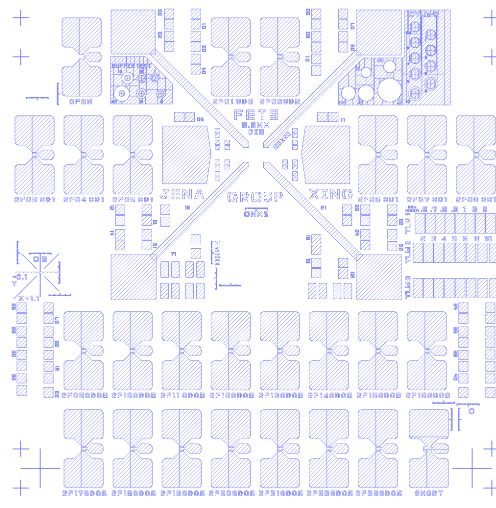


(a) Regrown Mask


(b) Alignment Mask for Regrowth Process



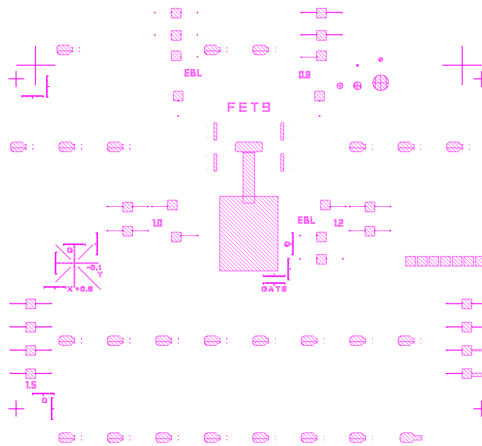
(c) Isolation Mask



(d) Ohmic Contact Mask

other preventing unwanted leakage pathways.

There are two different types of device isolation masks used, one for the regrown process and one for the alloyed contact process. The one for the alloyed contacts has an extra feature. It utilizes what's called "ohmic claw" etching. In the middle of the source and drain pads there are holes that are etched during the device isolation etching process. This lets metal, during the ohmic metal deposition step, flow into the holes and make direct contact with the 2DEG



(e) Gate Contact Mask

Figure 2.1: Different masks used for optical lithography for processing HEMTs

decreasing the contact resistance. Figure 2.2 demonstrates an example of the ”ohmic claw” holes etched into the device.

The fourth mask is the ohmic contact mask and is used in the previously mentioned ohmic metal deposition step. With a negative resist, the mask defines the area needed for the pads of the source and drain locations.

The gate contact mask is the last mask used in these fabrication processes. Similarly to the function of the ohmic contact mask, the gate contact mask details the area for the gate contact pads when used with a negative resist.

Two different device processes were used in the fabrication of the FeHEMTs, which will be explained in the next section.

Figure 2.2: Example of the ”Ohmic Claw” holes etched into ohmic layer after the device isolation etch step. The holes are 1 μm in diameter.

2.2 HEMT Fabrication

In the first part of this section, I will discuss the use of alloyed contacts in processing HEMTs. The second part will cover the process of adding electron beam lithography gates to one of the devices. Lastly, I will explore the use of regrown contacts instead of alloyed contacts to achieve lower contact resistance.

2.2.1 Alloyed Contacts

The devices processed were grown with Molecular Beam Epitaxy. Starting with SiC substrates the grown stack is as follows: AlN buffer, bulk GaN, AlN, GaN

cap, with the 2DEG forming between the bulk GaN and the AlN layers. Figure 2.3 illustrates a schematic for the as grown structures. As we can see from the band diagram simulation in Figure 2.3, there is a two dimensional electron gas between the AlN barrier and GaN channel regions due to the polarization difference between the two materials.[35] The samples were then diced into 7mm x 7mm pieces and processed in the cleanroom to create HEMTs.

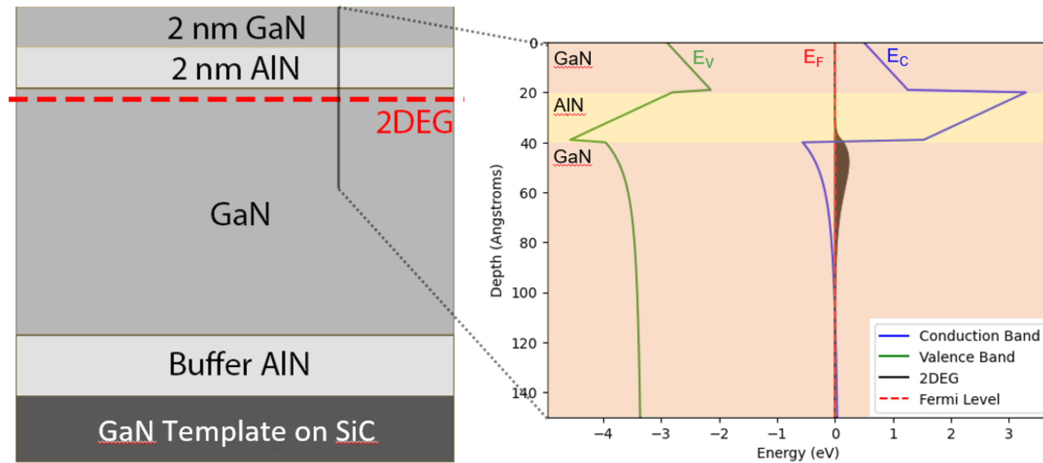


Figure 2.3: Structure of device grown in an MBE along with a band diagram illustrating the location of the 2DEG

A schematic of the processed devices are shown in Figure 2.4. Before processing, the samples were tested for charge density, mobility and sheet resistance through hall measurements. To conduct this measurement, Indium dots were applied to the corners of the pieces through a soldering iron.

The alloyed contacts device fabrication consists of three main steps: device isolation, ohmic contacts, and gate contacts. Before the device isolation step, the process starts with sample cleaning with HCl, Acetone and IPA. The HCl is necessary to remove any indium dots left on the sample during the hall measurements. The acetone and IPA are sonicated and clean the rest of the sample

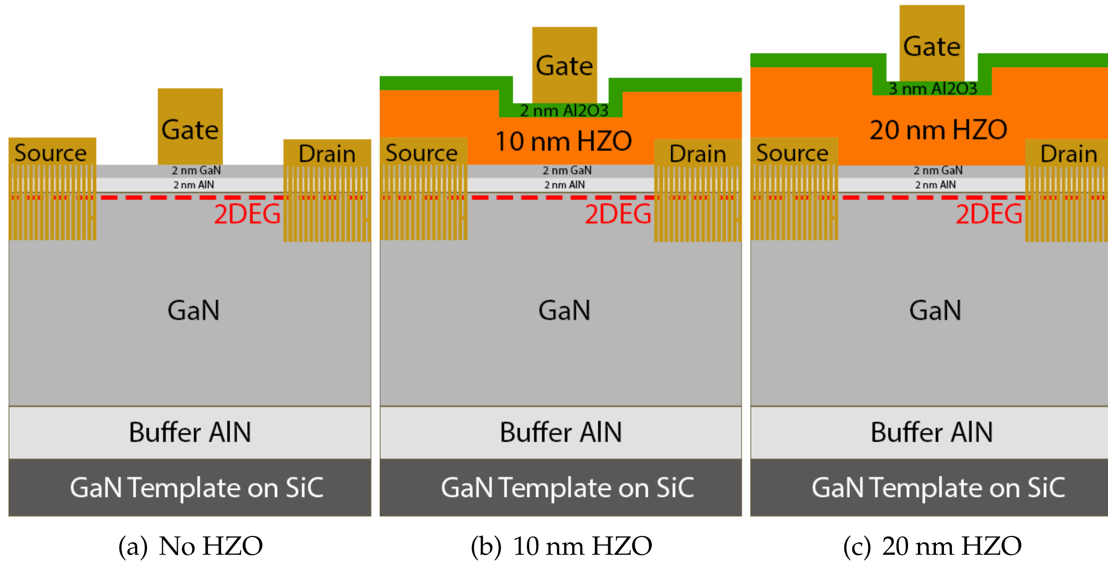


Figure 2.4: Processed device structures for alloyed contact devices. Both devices with Ta/Al/Ni/Au and Ti/Al/Ni/Au alloyed contacts have the same device structures

by removing any unwanted debris. Followed up with N_2 to dry the sample, the next step is the Isolation Etch. SPR 700, a positive photoresist, is spun onto the samples with a ramping speed of 5000 rpm, a max speed of 5000 rpm and for 30 seconds. The samples were then baked at 95C for 60 seconds. A pattern was then applied to the sample using the isolation mask described above. The exposure was carried out in the GCA AS200 i-line Stepper. The general process used in the Stepper involved an exposure time of 0.2 seconds, followed by a post-bake of 60 seconds at 115C. To develop the photoresist, the samples were added to 726 MIF for 60 seconds and then rinsed with DI water.

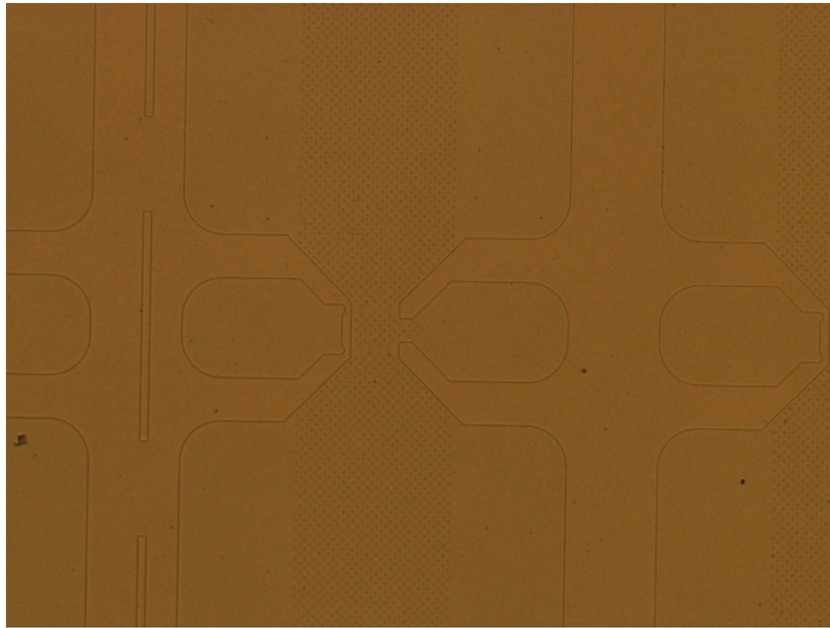
After verifying the patterns with an optical microscope, the samples were placed in the Glen 1000 for an O_2 descum for 120 seconds. The samples are then transferred to the PT770 ICP etcher for the device isolation. The chamber is seasoned before each etch. The etching recipe uses BCl_3 and yields an etch rate of around 7 nm/min.[36] The samples are etched for 10 minutes. The etch

is then verified with the P7 Profilometer and then placed in 1165, followed by Acetone and IPA, to remove the photoresist. The resulting device isolation along with the ”ohmic claw” etched holes can be seen in Figure 2.5.

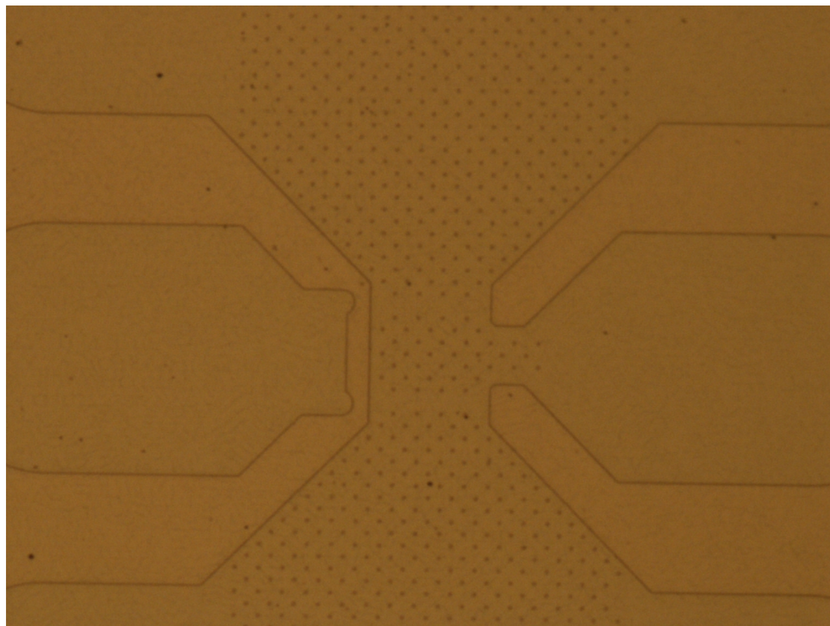
For the ohmic contacts step, a negative photoresist, nLOF 2020, is spun onto the samples with a ramping speed of 7000 rpm, a max speed of 7000 rpm and for 30 seconds. The spinning is followed by a bake at 115C for 60 seconds. The process in the Stepper is repeated but instead using the ohmic contact mask. The sample is again post baked at 115C for 60 seconds and developed in 726 MIF for 1 minute, followed by a verification of the patterns optically. The samples go through an O_2 descum in the Glen 1000 etcher and then placed in an electron beam evaporation chamber. The chamber is pumped down to 2e-6 torr, where titanium/tantalum, aluminum, nickel and gold are evaporated onto the samples. (Titanium and tantalum were both used to try to achieve better ohmic contacts and thus lower contact resistances. This will be discussed more in later sections.) The thickness of each layer is 20 nm, 100 nm, 50 nm and 40 nm respectively. Following removing the samples from the evaporator, they are thus added to 1165 for metal and photoresist liftoff. The liftoff process includes sonicated acetone and IPA after 1165.

The goal of this stack of metals for the source and drain contacts is for the connection to be ohmic, as suggested by the name of the step. If TLM were to be measured on the samples after the evaporation, the contacts would be schottky in nature. To convert these contacts to be ohmic, we can anneal them at a high temperature. These samples were annealed in a rapid thermal annealer at 830C for 60 seconds. Post annealed images of the contacts can be seen in Figure 2.6

Following the ohmic contacts, a blanket deposition of HZO and Al_2O_3 is

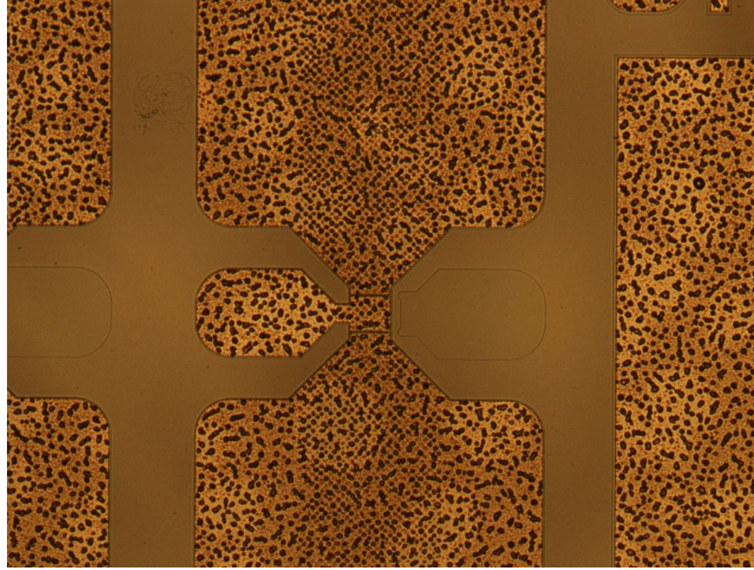


(a)

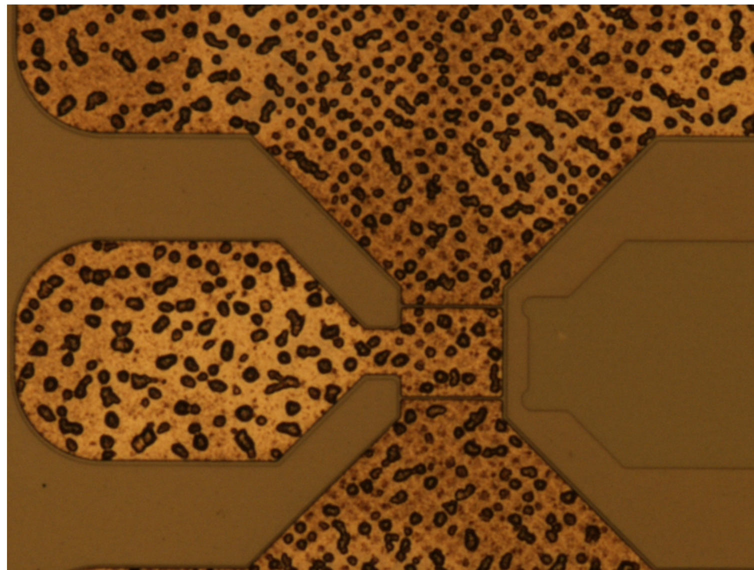


(b)

Figure 2.5: Optical images of a tranistor on the device post device isolation etch. The ″ohmic claw″ etched holes can be seen on the regions of the source and drain pads. (a) Transistor image with 0.6 μm gate length, (b) zoomed in image of transistor



(a)



(b)

Figure 2.6: Optical images of the source and drain pads after annealing at 830C for 60 seconds. The metal stack used is Ti/Al/Ni/Au with thicknesses of 20 nm, 100 nm, 50 nm and 40 nm respectively. (a) Transistor image with 0.6 μm gate length, (b) zoomed in image of transistor

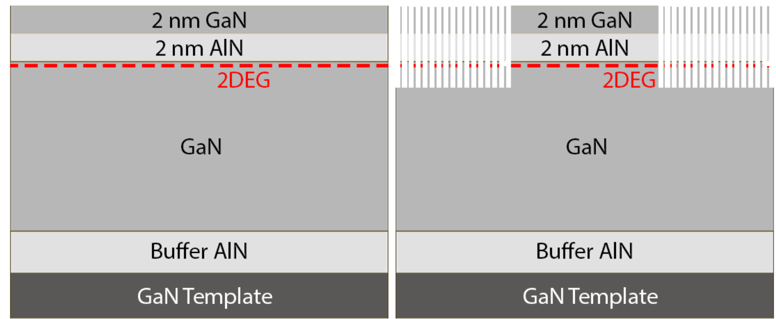
deposited on the sample through Atomic Layer Deposition(ALD). Due to this being the layer of interest, two different values were chosen for the thickness of the HZO and Al_2O_3 to analyze the effects on the devices. The combinations

of 10nm HZO - 2nm Al_2O_3 and 20nm HZO - 3nm Al_2O_3 were chosen. Since the optimal concentration of Hf to Zr for ferroelectricity is 50-50, there are even cycles of HfO_2 and ZrO_2 in the ALD.

Al_2O_3 was chosen to be deposited on top of the HZO layer due to the electrostatic coupling between the two materials. This coupling leads to a strong interface polarization which contributes to the improved ferroelectricity of the HZO layer. This additional layer should be able to increase the remnant polarization as well as decrease the leakage current.[37] [38]

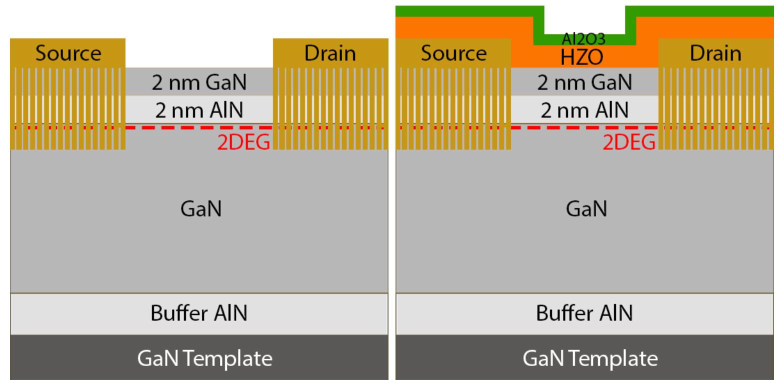
The last step is to add the metals for the gate contacts. This process is very similar to the previous step for depositing ohmic contacts on the source and drain. It starts with spinning the negative photoresist nLOF 2020 with a ramping speed of 7000 rpm, a max speed of 7000 rpm and for 30 seconds and baking it for 60 seconds at 115C. The stepper is used again with the gate contact mask. After a post bake at 115C for 60 seconds, the samples are developed in 726 MIF for 1 minute. After an O_2 descum in the Glen 1000, the samples are loaded into the evaporator for deposition of nickel and gold with thicknesses of 50 nm and 100 nm respectively. The metal and photoresist are then lifted off with the series of 1165, acetone and IPA.

Throughout the process, one of the critical factors was the alignment of the photolithography masks using the stepper. This alignment hinges on the accuracy of the alignment marks detailed in the previous section. Even a slight misalignment can potentially short some or all of the devices, rendering them inoperative. Paying crucial attention to these steps helps increase the number of devices produced per fabrication session.



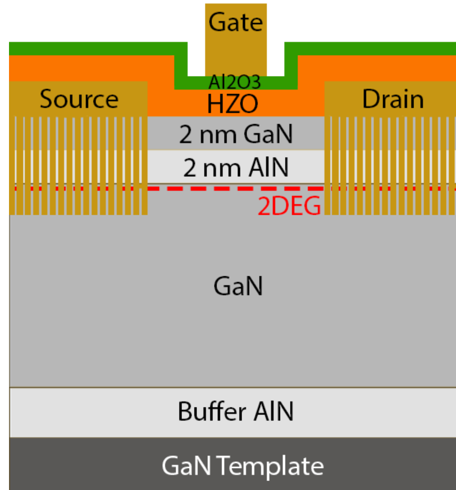
(a) Clean sample and remove indium dots

(b) Device isolation etch with ”ohmic claw” holes



(c) Ohmic metalization

(d) ALD deposition



(e) Gate metalization

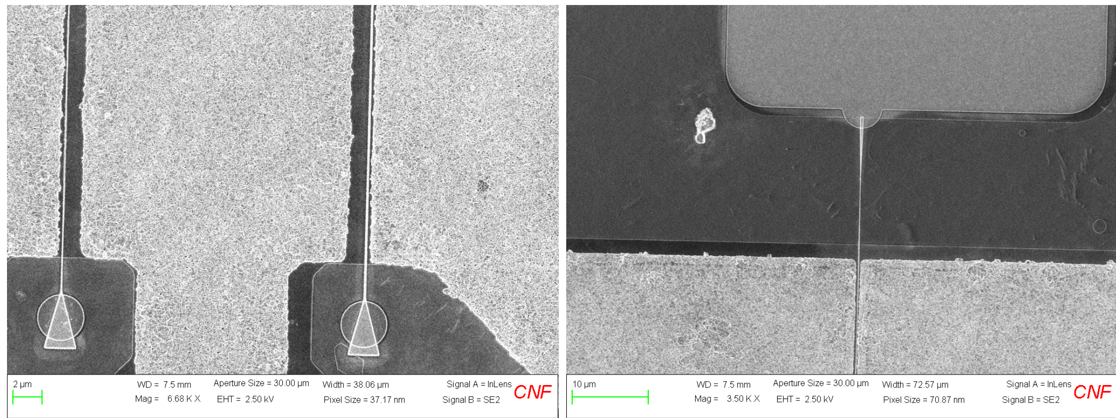
Figure 2.7: Schematic of the process flow for developing alloyed contacts

2.2.2 Electron Beam Lithography Gates

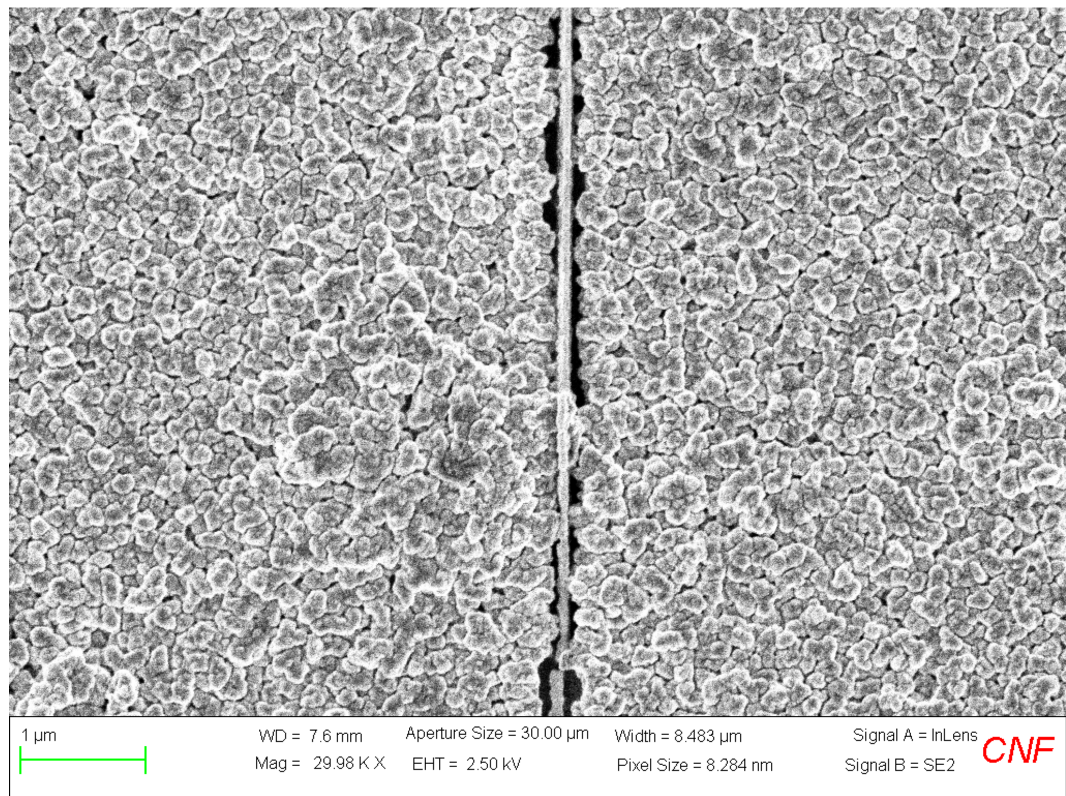
Electron beam lithography (EBL) gates were deposited on the sample with a 10 nm layer of HZO. This specific device was selected because it exhibited the fewest instances of shorted transistors among all devices tested. The original device featured numerous open spots designed for EBL gates to be added. By employing EBL gates with smaller dimensions compared to optical gates, the source-to-drain distance was effectively reduced. However, issues arose with alloyed contacts requiring annealing. The alloyed metal diffused laterally, resulting in shorts in some devices. The design choice for the location of the EBL gates was also to be closer to the source than the drain, to maximize the gate-to-drain distance. Figure 2.8 shows images of the examples of the gates being shorted to the source.

The process for developing the EBL was only two steps as the main device was already processed. The resist used was a bottom layer of PMGI SF9, which was spun on with a ramping speed of 5000 rpm, a max speed of 5000 rpm and for 30 seconds and was baked at 185C for 5 minutes. On top, a layer of UV 210GS-0.6 was spun on with a ramping speed of 2000 rpm, a max speed of 5000 rpm and for 60 seconds and was baked at 135C for 90 seconds. A cross section image of the resist stack used can be seen in Figure 2.9.

The exposure was done in a JEOL JBX-6300FS system. The beam current used was 1nA and the dose was 170 $\mu C/cm^2$. After exposure, the sample was baked at 115C for 105 seconds and then developed in MIF 726 for 65 seconds. Just like for the optical gates, the samples were taken for an O_2 descum in the Glen 1000 and then loaded into the evaporator for deposition of nickel and gold with thicknesses of 50 nm and 100 nm respectively. To lift off the metal, the



(a) (b)



(c)

Figure 2.8: SEM images of gate located too close to the source contacts, resulting in being shorted

samples were submerged in 1165 at 80C for 10 minutes and followed by IPA.

Two different gate lengths were chosen for the process, 100 nm and 200 nm. Due to the resist used, the resulting gate lengths were around 110 nm and 180

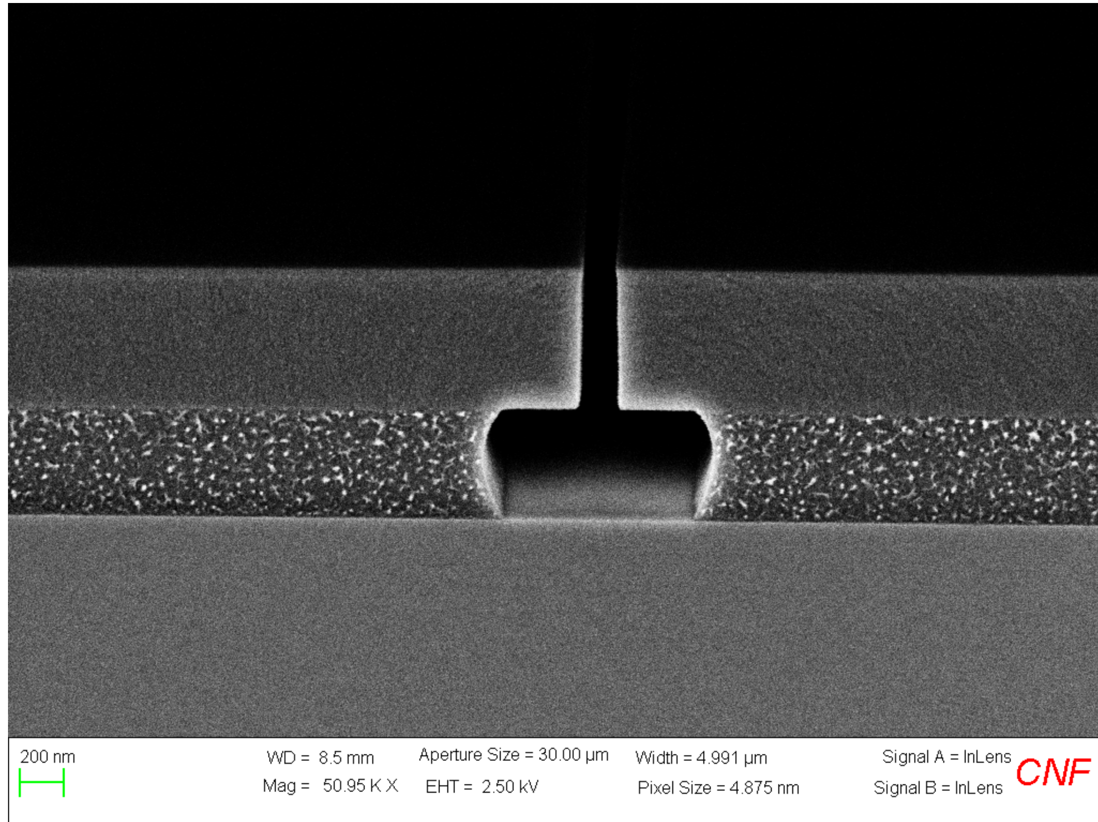


Figure 2.9: SEM cross section image of the resist used in the EBL exposure. The different layers, from the bottom, are: (1) Si substrate, (2) PGMI SF9, (3) UV 210GS-0.6

nm respectively. Figures 2.10 and 2.11 shows SEM images of the gates after Ni/Au deposition.

2.2.3 Regrown Contacts

The second type of device processed used regrown contacts. The design is essentially the same as for alloyed contacts with the difference that the ohmic contacts are n+ GaN, grown in the MBE, rather than an alloyed metal stack of Ti or Ta/Al/Ni/Au. Regrown contacts are useful as their contact resistance is much lower than those with alloyed contacts. The use of regrown contacts has

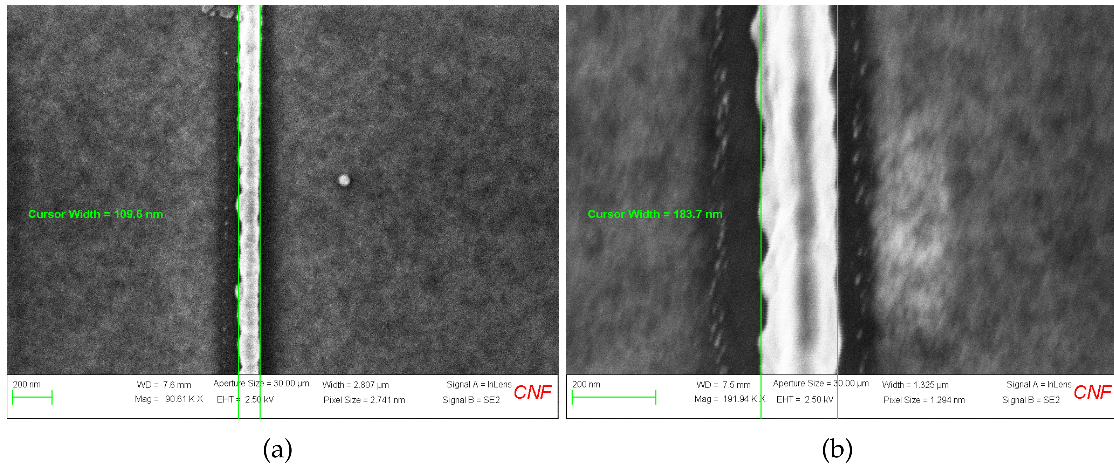


Figure 2.10: SEM images of resulting gate widths after Ni/Au deposition in an electron beam evaporator: (a) Expected length = 100 nm, actual length ~110 nm; (b) Expected length = 200 nm, actual length ~180 nm

been heavily investigated over the last few decades. With the improved interface quality devices with regrown contacts are able to achieve higher on currents and lower on resistances.

The process for developing regrown contacts is very similar to making annealed contacts, with the only difference being the development of the ohmic contacts. A schematic of the process flow for the devices are shown in Figure 2.12.

First, after cleaning the sample with HCl, Acetone and IPA, a layer of SiO_2 is blanket deposited across the whole sample through plasma enchanced chemical vapor deposition (PECVD). The thickness of the SiO_2 layer is about 250 nm. About 40 nm of chromium is then deposited over the SiO_2 through e-beam evaporation. After spinning nLOF 2020, with a ramping speed of 7000 rpm, a max speed of 7000 rpm and for 30 seconds and baking at 115C for 60 seconds, the stepper is used to pattern the regrown mask onto the sample.

Post developing of the resist, the Cr layer is etched away with a recipe using

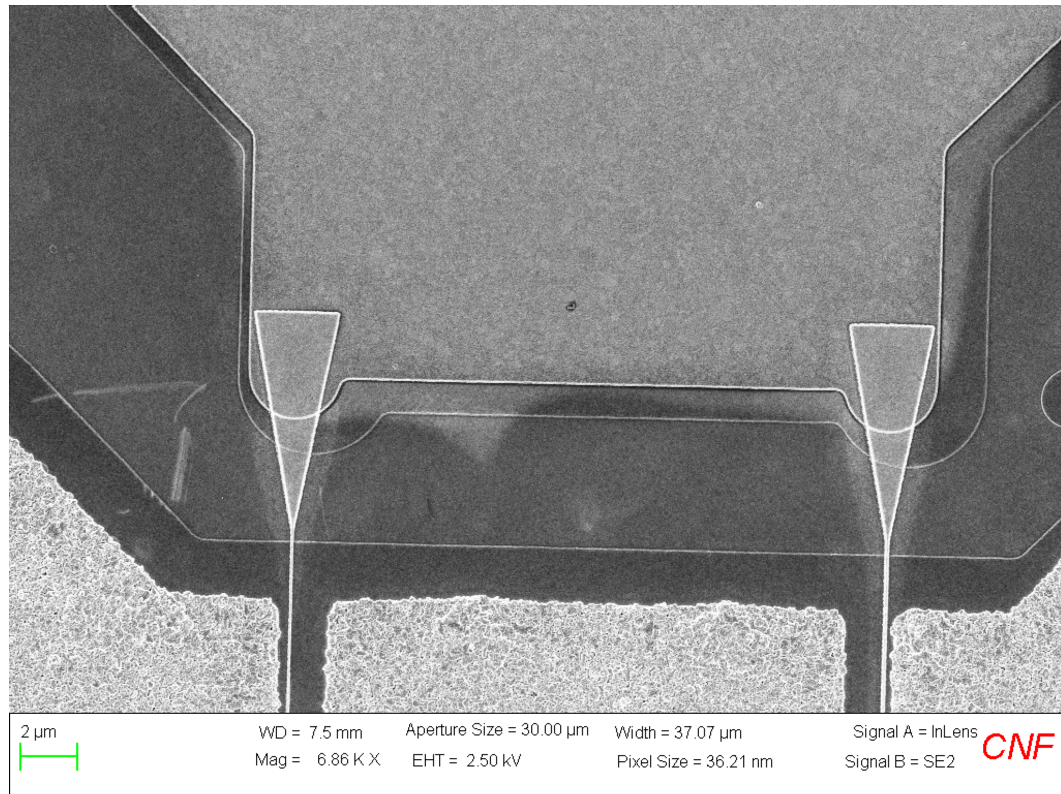


Figure 2.11: SEM image of deposited gates on transistor devices. These gates have enough room between the source and are not shorted. The gate lengths from left to right are ~110 nm and ~180 nm

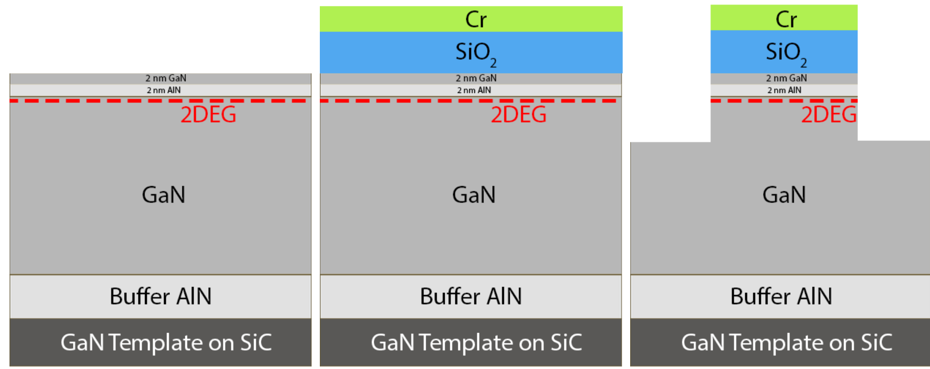
Cl_2 and O_2. The device is then placed in 1165, Acetone, and IPA to liftoff the resist. Using the Cr as a mask, the SiO_2 is etched away down to the GaN layer. The etch recipe uses CF_4 and CHF_3. Confirming that the GaN layer is exposed, the device is placed back into the etcher to etch around 20 nm into the device structure with BCl_3. The sample now has a SiO_2 hard mask for depositing the regrown GaN.

The sample is then taken to the MBE lab to prepare for the regrowth process. HCl is used to remove the rest of the Cr and clean the sample for the MBE. The sample is then mounted in the MBE with indium where around 60 nm of n+ GaN is regrown onto the device.

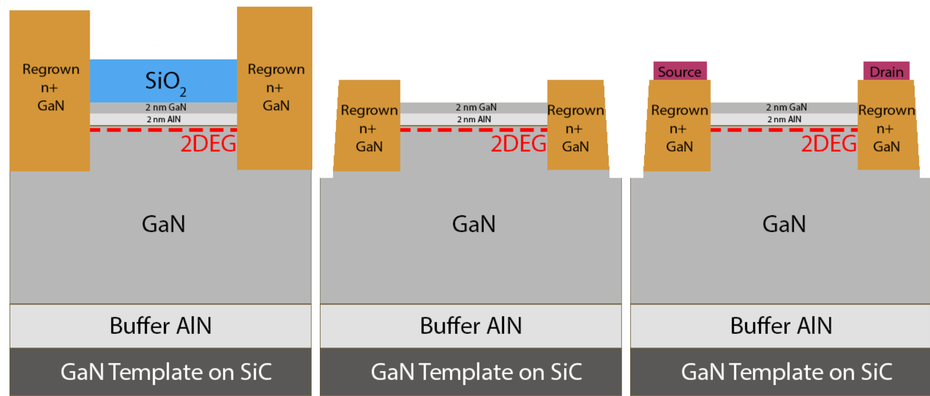
Following the deposition in the MBE, the sample is placed in HCl to remove the leftover indium. The next step is to create an alignment mark to use for the rest of the processes. SPR 700, is spun onto the samples with a ramping speed of 5000 rpm, a max speed of 5000 rpm and for 30 seconds, followed by a bake at 95C for 60 seconds. The alignment mask was used in the stepper to apply the wanted pattern. The samples are then placed into the etcher after developing the resist. With BCl_3, Cl_2 and Ar, around 700 nm are etched into the sample.

The photoresist is lifted off with 1165 and then the sample is placed in 6:1 buffered oxide etch(BOE) for 30 minuted to remove the SiO_2 hard mask. Once removed, the sample is sonicated in IPA.

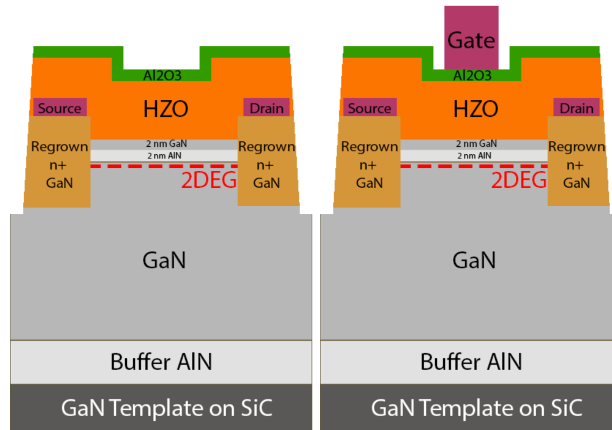
After the hard mask is removed, the rest of the process flow follows the same steps as the alloyed contact process flow: (1) device isolation, (2) Ti/Au ohmic metalization[39], (3) the deposition of HZO and Al_2O_3 through ALD, (4) annealing of the HZO layer, (5) Ni/Au gate metallization.



(a) Clean sample and remove indium dots (b) Deposit SiO_2 and Cr (c) Etch SiO_2 and Cr to create hard mask



(d) Regrow n+ GaN in MBE (e) Device isolation etch (f) Ohmic metallization



(g) ALD deposition (h) Gate metalization

Figure 2.12: Schematic of the process flow for developing regrown contacts

CHAPTER 3

VERIFYING FERROELECTRICITY IN HZO FILMS

An important step before testing the fabricated devices is to verify the ferroelectricity in the HZO films. Not only is this essential because it is the focus of this study, but also because ferroelectricity can be confused for many different factors and vice versa. An example of this is the hysteresis in the transfer curves of the transistors. While ferroelectricity causes hysteresis loops, another contributing factor to the loops is energy traps in the material.[40][41] It is important to keep that in mind when analyzing the data.

To verify the ferroelectricity, two different methods are used. The first method is to use energy dispersive X-ray spectroscopy(EDX). The HZO film was deposited with a composition of $H_{0.5}Z_{0.5}O_2$, chosen for its robust orthorhombic phase and strong ferroelectric properties. Using EDX, we can look at the composition of HZO that was deposited.

Figure 3.1 shows an SEM image with a box outlining the location of where the EDX was performed. The values obtained are in Table 3.1. The resulting composition of the HZO was not 50-50 and was closer to 65-35. From the $H_{0.5}Z_{0.5}O_2$, as more Zr is added, the material goes from being a ferroelectric to becoming an antiferroelectric.[31] This is problematic because antiferroelectrics lack any remnant polarization. Therefore, we can anticipate that the remnant polarization will be lower than the desired level.

The second method is to use a positive up negative down(PUND) measurement to calculate the polarization of the material.[42] One of the main ways to gauge the capabilities of a ferroelectric material is to look at its polarization ver-

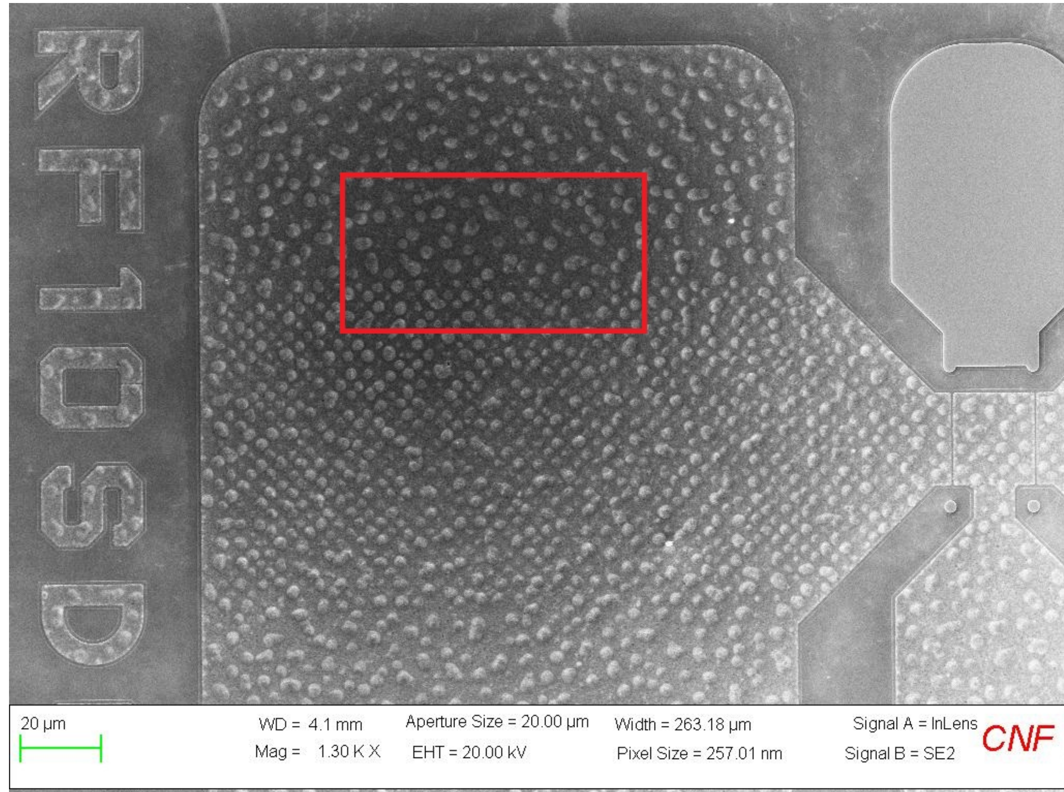


Figure 3.1: SEM image of a processed device source pad with a 20 nm HZO layer on top. The red box signifies where the EDX measurement was taken.

Element	Atomic Number	Normalized Mass Percent	Atomic Percent
Zirconium	40	49.53	65.76
Hafnium	72	50.47	34.24

Table 3.1: Energy dispersive x-ray spectroscopy measured values of mass percentage and atomic percentage of zirconium and hafnium deposited on the device.

sus electric field plot. The curve in this plot is known as a P-E loop. The P-E loop of a material can tell us everything we need to know about the strength of the ferroelectricity of the material. The values in the loop enable us to extract the saturation and remnant polarizations as well as the coercive field of the ferroelectric. The shape of the curve also gives information about whether the material is a dielectric, ferroelectric or even antiferroelectric.

A way to measure the P-E loop of a material is by using the PUND method. PUND measurements consist of applying two positive voltage pulses followed by two negative voltage pulses, where the voltage of the pulse determines the V_{Max} of the measurement. These four pulses are why the measurement is called positive up negative down. The need for two pulses of each is to be able to isolate the polarization coming from the switching and the intrinsic polarization. The first pulse switches the polarization and the second pulse is utilized to subtract out the base polarization. The measurement is typically done on a capacitor-like structure. Figure 3.2 illustrates a diagram for the probing method. Once the voltage pulses are applied, the current is measured after each pulse. The current is then integrated to get the charge. By subtracting the U and D pulses from the respective P and N pulses, we are able to generate the two halves of the P-E loop.

The measured P-E loop from the Metal-Ferroelectric-Metal structure can be seen in Figure 3.3. At first it is obvious that the loop does not look as perfectly shaped as the PZT P-E loop in Figure 1.4. Extracting the values from the graph we get a remnant polarization of 14.15 $\mu C/Cm^2$, a saturation polarization of 23.595 $\mu C/Cm^2$ and a coercive field of 1.7 MV/cm. When compared to the values in literature (Table 1.2), the measured values are lower than desired. The primary contributing factor is likely what was observed during the EDX measurement: the material exhibits slight antiferroelectric behavior. As a result, the remnant polarization decreases towards zero. Even though the films are not perfectly ferroelectric, they still possess a remnant polarization, still letting the devices work as expected.

On top of verifying the deposited HZO films, we can also look at the di-

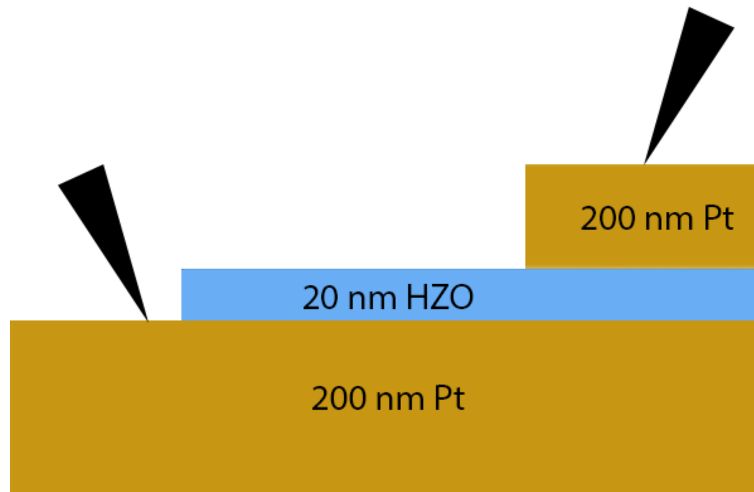


Figure 3.2: Schematic of the metal-ferroelectric-metal(MFM) structure used to measure the P-E loops of the HZO layer

rectionality of the hysteresis loops in the transfer curves and capacitance voltage measurements. It is said that if the loops are counter-clockwise, then the hysteresis is due to ferroelectricity.[20] The loops will be looked at more in the following sections.

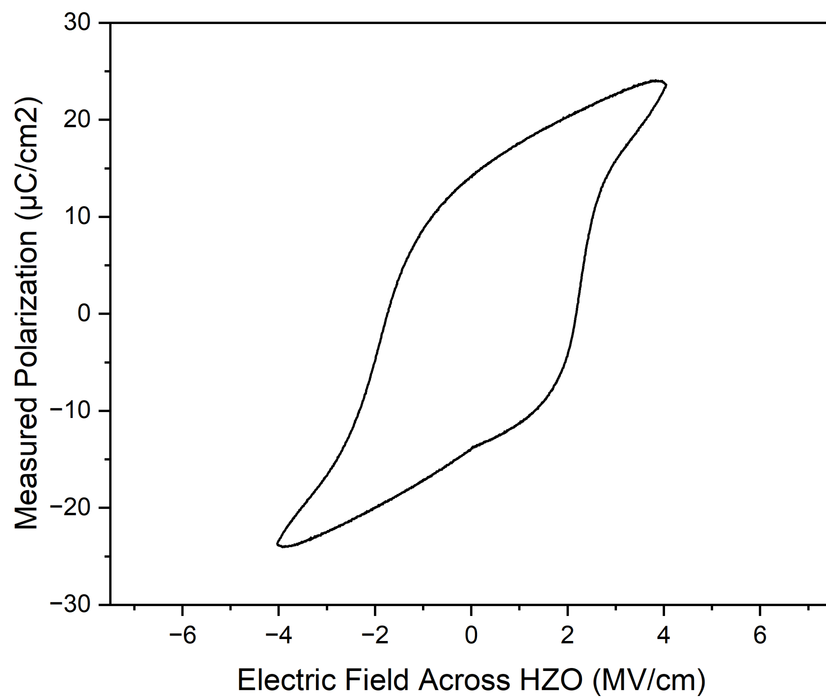


Figure 3.3: Measured P-E loop from the MFM structure for 20 nm of HZO

CHAPTER 4

ALLOYED CONTACTS DEVICE CHARACTERIZATION AND PERFORMANCE

There were five devices processed with alloyed contacts. The values obtained from hall measurements before processing can be seen in Table 4.1. We can see that there is a high 2DEG density as well as high mobility as expected.

Device	Sheet Charge	Mobility	Sheet Resistance
Units	$/cm^2$	$cm^2/V\text{-}s$	Ω/sq
1	-1.825 x 10^{-13}	1260	271.4
2	-1.895 x 10^{-13}	1400	234.5
3	-1.879 x 10^{-13}	936	354.8
4	-2.447 x 10^{-13}	1170	218.3
5	-2.414 x 10^{-13}	1210	214.4

Table 4.1: Measured data through Hall Measurements of the device structures before processing

Since achieving low contact resistance is crucial for optimizing device properties, two different metals were employed in the metal stack for the ohmic contacts. The first three were processed using tantalum and the last two were processed with titanium instead. After processing the first three samples, the contact resistance was not as low as desired so a second attempt was made. With the new devices, the contact resistance still did not reach the desired low level. The contact resistance for the five devices vary between 1 and 9 ohm-mm. Table 4.2 shows all the calculated contact resistances and sheet resistances for the five devices. While a lower contact resistance is useful, it doesn't affect the data collected relating to the ferroelectricity.

Out of the devices processed with tantalum, one was kept as a control without any HZO deposited on it. Between the other two, one had 10nm of HZO

Device	Alloyed Material	Contact Resistance	Sheet Resistance
Units	–	Ω-mm	Ω/sq
1	Ta/Al/Ni/Au	7.42	1122.7
2	Ta/Al/Ni/Au	5.98	587
3	Ta/Al/Ni/Au	1.08	715.6
4	Ti/Al/Ni/Au	8.44	1037.6
5	Ti/Al/Ni/Au	2.06	1011.16

Table 4.2: Measured contact resistance and sheet resistance post device processing. Devices 1-3 were calculated through CTLM measurements and devices 4-5 were calculated through TLM measurements

and 2nm of Al_2O_3 and the other had 20nm of HZO and 3nm of Al_2O_3. For the devices with titanium, there was one device processed as a control without HZO and one processed with 20nm of HZO and 3nm of Al_2O_3. Diagrams of the devices can again be seen in Figure 2.4. The default devices analyzed throughout the rest of this paper will be the devices with titanium unless otherwise specified.

4.1 PUND Loops

Figure 4.1 shows the polarization loop from a device with 20nm of HZO. The PUND measurements were performed on capacitance pads patterned on the devices during processing. A diagram of how the devices are probed can be seen in Figure 4.2. It is good to note that due to the measurement being performed on the devices, the pathway of current goes through the 2DEG as well as the HZO layer.

In the P-E loop we can observe the expected hysteresis. From the loop, we can extract the remnant polarization to be 11.485 $\mu C/cm^2$, a saturation polarization of 21.31 $\mu C/cm^2$, and a coercive field of 1.3 MV/cm. Contrasting the

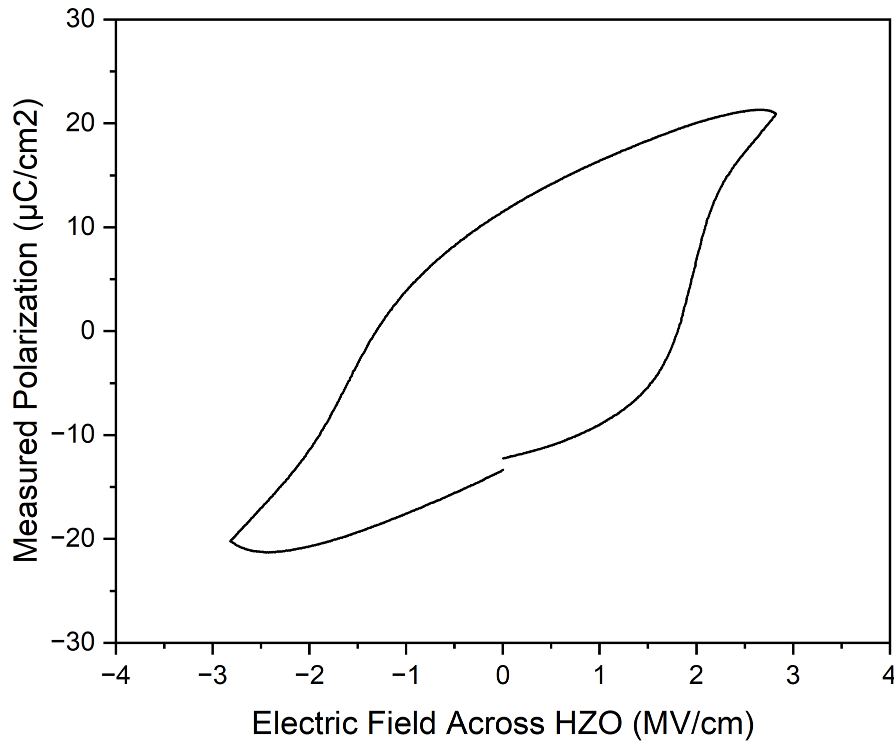


Figure 4.1: P-E loop measured on processed device with 20 nm of HZO as well as a 2DEG layer

values from the device to the measured values from the MFM structure (Figure 3.3), the remnant polarization is slightly lower. Due to both this sample and the MFM structure being co-loaded into the ALD, there should be no additional effect from the material being slightly antiferroelectric when comparing the two values. There are a couple more contributing factors that we can consider.

It has been shown that different top and bottom electrodes contribute to different values of remnant polarization.[43] This is attributed to the different work functions of the electrodes as well as their coefficients of thermal expansion (CTE). It was reported that the larger the difference of coefficients of thermal expansion, the larger the remnant polarization. The CTE for HZO is around

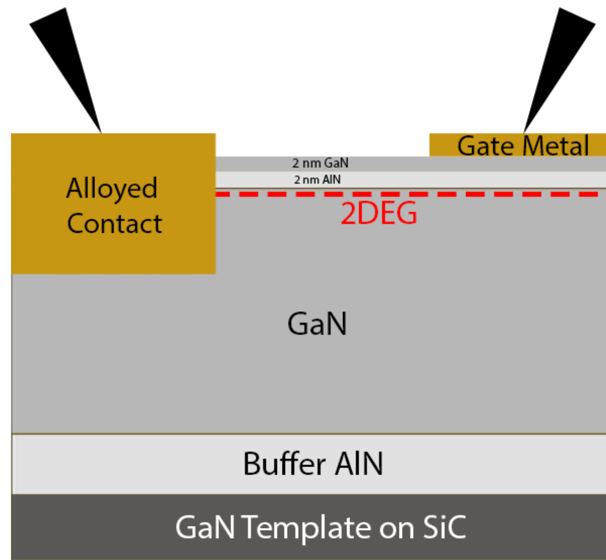


Figure 4.2: Schematic of the probing structure for measuring capacitance and performing PUND measurements

$9x10^{-6}$/K. With a CTE of around $4.5x10^{-6}$/K, a large mismatch with HZO, tungsten was found to be one of the best electrodes for high remnant polarization. On the device, the bottom electrode is GaN and the top electrode is Ni/Au. The CTE of GaN and Ni is $5.59x10^{-6}$/K and ~$8.5x10^{-6}$/K respectively.[44][45] With in-plane tensile strain the most favorable for the formation of the ferroelectric orthorhombic phase, it is possible that after the anneal, there wasn't enough strain to fully develop the HZO.

Another potential factor contributing to the decrease in remnant polarization is the interaction with the 2DEG. With the PUND measurement calculations being based on the current measured through the detector, if there is a possible leakage path through the 2DEG, the remnant polarization may not be able to maintain its maximum value.

4.2 Capacitance-Voltage Measurments

Capacitance-Voltage measurements were performed on the devices to analyze more about the interaction between ferroelectric HZO and the 2DEG as well as to demonstrate any memory window appearing in the data. The measurements were performed at different frequencies(20kHz, 40kHz, 60kHz, 80kHz, 100kHz, 200kHz, 400kHz, 600kHz, 750kHz, 1MHz, 2MHz, 3MHz, 4MHz, 4.5MHz and 5MHz) and temperatures(25C, 50C, 100C, 150C and 200C). The devices were probed on the capacitance pads(same as for the PUND measurements) and between the source and gate on the transistor structures.

4.2.1 No HZO

The room temperature capacitance measured from the sample with no HZO, overlaid with a 1DPoisson simulation of the capacitance, can be seen in Figure 4.3.[35] From the data we can see that the measured data matches well with the simulation. As expected, the capacitance does not vary with frequency.

Figure 4.4, illustrates the capacitance measured at multiple increasing temperatures. There is very little change between the different temperatures(with the messiness due to the data measured at lower frequencies having higher loss tangents at higher temperatures). From this data we can confirm that the AlN and GaN layers are not temperature dependent.

Analyzing the temperature and frequency dependence of the capacitance in the device without HZO, we observe a negligible presence of trapped charges, as evidenced by the absence of hysteresis across all temperatures and frequen-

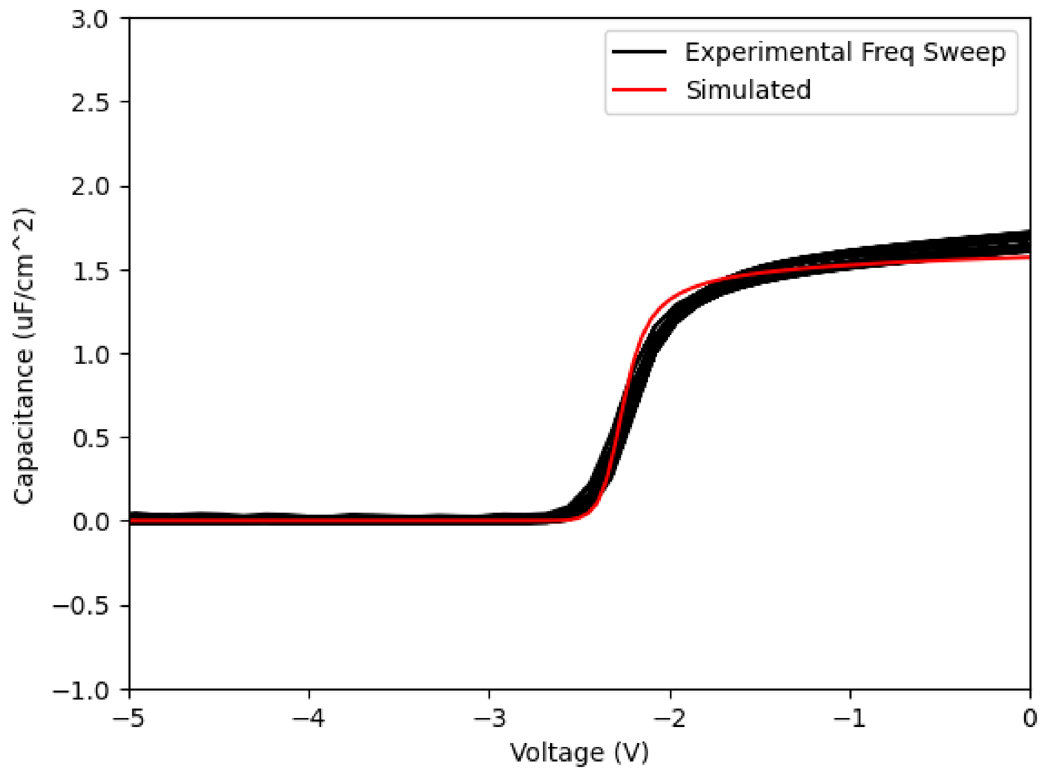


Figure 4.3: Capacitance-voltage measurement of AlN/GaN HEMT with no HZO layer at multiple frequencies compared to simulated capacitance. The simulation was performed with 1DPoisson software.

cies.

4.2.2 20nm HZO

Based on the absence of hysteresis loops in the device without HZO, we can confidently attribute the hysteresis loops observed in the capacitance measurements of the samples with HZO to ferroelectricity. The measurement in Figure 4.5 is for the sample with 20nm of HZO and was performed at 20 kHz.

The first thing of notice is the characteristic butterfly loops that ferroelectrics are known to have. The loops are centered around 0 volts and have a loop width

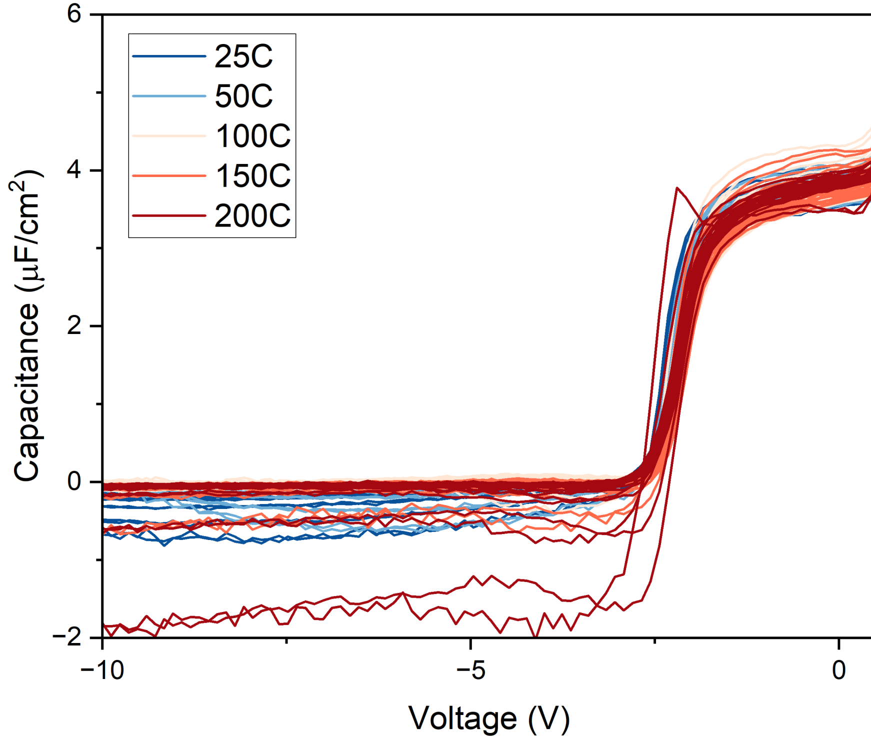


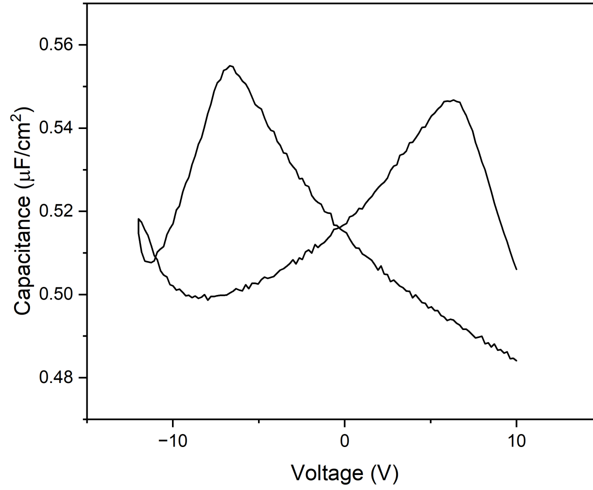
Figure 4.4: Capacitance-voltage measurement of AlN/GaN HEMT with no HZO layer at multiple frequencies and temperatures. The device is measured at 25C, 50C, 100C, 150C and 200C

of about 2.3 MV/cm.

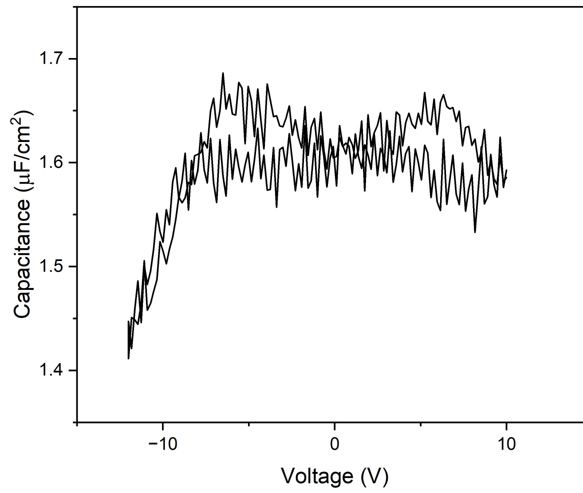
With the capacitance measurement, we can extract the dielectric constant of HZO in the devices. We can compare our calculated value to that in literature to analyze the quality of the HZO film. In literature the dielectric constant is about 30. To calculate the dielectric constant, we can use the equation below:

$$\frac{1}{C_{Total}} = \frac{t_{HZO}}{k_{HZO}\varepsilon_0 A} + \frac{t_{Al_2O_3}}{k_{Al_2O_3}\varepsilon_0 A} + \frac{t_{AlN}}{k_{AlN}\varepsilon_0 A} + \frac{t_{GaN}}{k_{GaN}\varepsilon_0 A} \tag{4.1}$$

Solving for the dielectric constant gets us the equation:



(a) 40 μm diameter capacitance pad



(b) 1.5 μm gate length, between gate and source

Figure 4.5: Capacitance-voltage measurement of AlN/GaN HEMT with a 20 nm HZO layer at 20 kHz. The measurement was performed on (a) a 40 μm diameter capacitance pad and (b) a 1.5 μm gate length probed between the gate and the source

$$k_{HZO} = \left[\frac{\varepsilon_0 A}{t_{HZO}} \left(\frac{1}{C_{Total}} - \frac{t_{Al_2O_3}}{k_{Al_2O_3}\varepsilon_0 A} - \frac{t_{AlN}}{k_{AlN}\varepsilon_0 A} - \frac{t_{GaN}}{k_{GaN}\varepsilon_0 A} \right) \right]^{-1} \tag{4.2}$$

Below is a table with all the values used in the equation:

Variable	Value Used
C_{Total} at 0V	6.469 x 10^{-12} F
$k_{Al_2O_3}$	9.34
k_{AlN}	9
k_{GaN}	9.7
$t_{Al_2O_3}$	3 nm
t_{AlN}	2 nm
t_{GaN}	4 nm
A	~5026.55 μm^2
ε_0	8.854 pF/m

Table 4.3: Values used in calculating the dielectric constant of HZO from capacitance voltage measurements

At 0V, after plugging all the values into the equation, the calculated dielectric constant is 26.17. The value is close to what was expected for the composition measured during EDX, around 30. We can assume that there is a near 35-65 ratio between Hf and Zr and that the anneal process was effective.

On account of the capacitance pads being on a device with a 2DEG, it is expected for the capacitance to drop to zero as the channel is depleted. In Figure 4.5(b), we can see the depletion starting whereas we cannot in Figure 4.5(a). This is due to the device breaking down before the depletion occurs.

The breakdown can be attributed to the lateral breakdown of HZO. At higher electric fields (around 3.5 MV/cm in these measurements), the formation of oxygen defects is increased and can destructively breakdown the layer. Although the breakdown field of HZO is slightly higher than what we are applying, as a result of the HZO being blanket deposited over the device, where there is break-

down, the source, drain and gate become shorted. A way around this would be to perform an isolation etch of the HZO to prevent any shorting.

4.2.3 10nm HZO

The devices with 10nm of HZO (and tantalum contacts) were able to deplete more constantly without breakdown. In Figure 4.6, we can see a temperature dependent series of capacitance measurements. Although there isn't a pronounced butterfly loop, there is still a notable hysteresis in the depletion regime. The hysteresis loop is also counterclockwise, which, as previously mentioned, is a strong indicator of ferroelectricity.

When the temperature of a ferroelectric increases toward its curie temperature, the hysteresis window decreases; however, in Figure 4.6 we can see the loop widening as the temperature increases. At room temperature, the width of the loop is about 0.5 volts. As the temperature rises to 200C, the width of the loop becomes around 1.25 volts. This can once more be attributed to lateral breakdown, which induces the formation of oxygen defects. The defects create cites for charges to get trapped inside, thus causing the loops to widen. The counterclockwise directionality of the loops indicates that ferroelectricity remains the dominant force contributing to the hysteresis. Possibly at higher temperatures, the direction might switch to clockwise.

Another possible interpretation of the loops widening at higher temperatures is that there is an electric field assisted annealing of the HZO layer. It is possible that the HZO layer was not fully crystallized. The higher temperature and electric field might crystallize the HZO more, thus improving the remnant

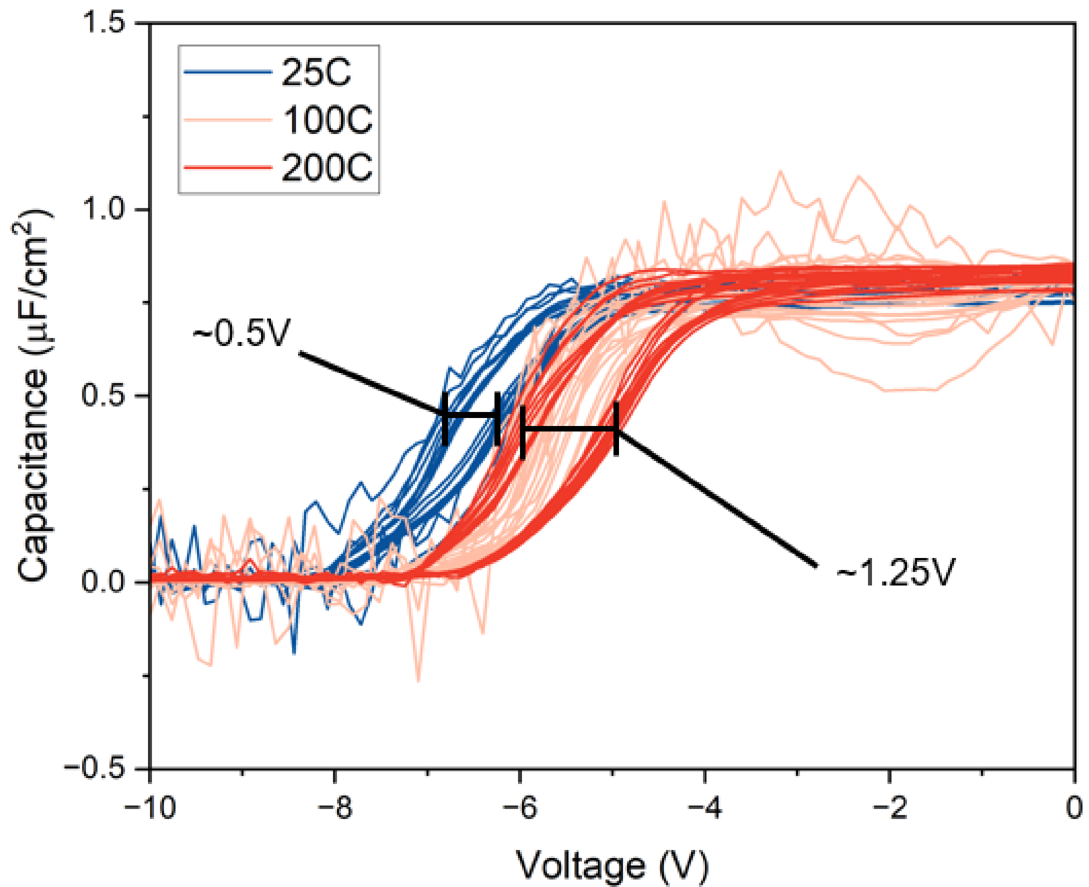


Figure 4.6: Capacitance-voltage measurement of AlN/GaN HEMT with a 10 nm HZO layer at multiple temperatures. The device is measured at 25C, 100C and 200C

polarization and widening the loop.

4.3 Current-Voltage Measurements

Each device exhibits various configurations, including different gate lengths, source-to-drain distances, and source-to-gate distances. All the devices shown in this paper have a gate width of 50 um, a source to drain distance of 5 um and a source to gate distance of 2.5 um. The gate lengths vary between 0.8 um, 1.0

um, 1.2 um and 1.5 um.

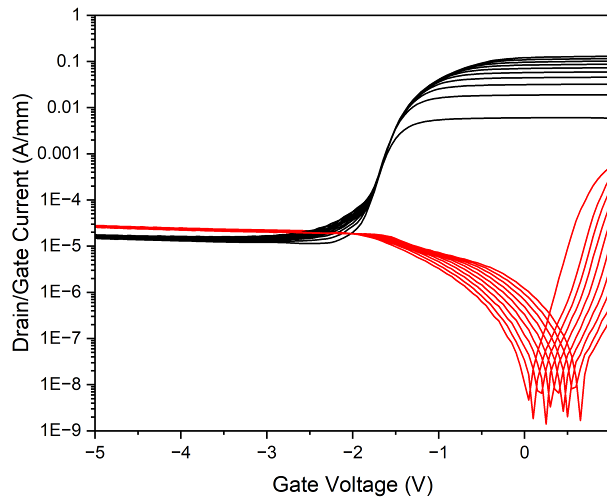
Although some of the devices, like the ones with tantalum contacts, have higher contact resistances, it is still worthwhile to look at all the different IV measurements.

4.3.1 Transfer Curves

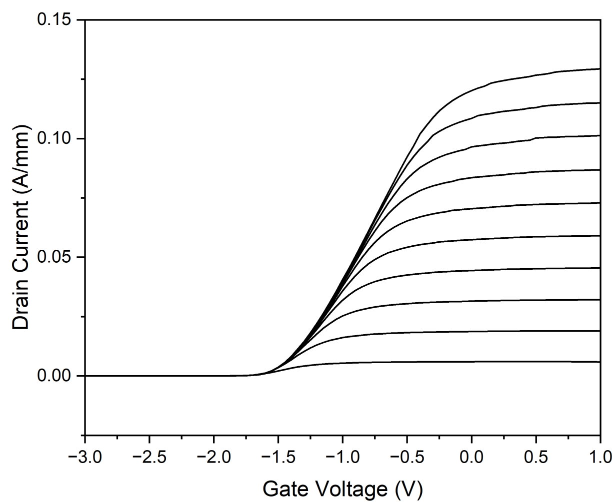
First we can look at the gate voltage versus drain and gate current of the devices with no HZO. As we can see in Figure 4.7, the device acts as a normal transistor and is able to be switched off. The device has an on/off ratio of around 4-5 orders of magnitude and has a threshold voltage of about -1.5 V.

After verifying the functionality of the device, a dual sweep is run by sweeping the gate voltage from 2 V to -10 V and back to 2V. The results of the dual sweep for both samples with no HZO are shown in Figure 4.8. For both devices, we can see that the forward and backward sweeps trace over each other perfectly, making it hard to even see both lines. This aligns with our expectations and is consistent with the capacitance-voltage measurements. The direction of sweeping the gate voltage does not matter and the threshold voltage will always be around -1.5 V for this device structure. This also helps to set an important baseline that further emphasizes that the hysteresis loops are most likely attributable to ferroelectricity rather than any other factors such as charge traps.[46]

Moving on to the samples with HZO, we can start with the device with 10 nm of HZO. From the transfer curve in Figure 4.9, we can see that the device is



(a) Log Scale



(b) Linear Scale

Figure 4.7: Transfer curves in log scale and linear scale of the device with no HZO layer. The drain voltage waS stepped from 0.1 V to 2 V by 0.2111 V steps

able to pinch off and act as a functioning transistor with an on/off ratio of about 4 orders of magnitude. The addition of the HZO does not negatively impact the device performance.

Looking at a dual sweep of the device (Figure 4.10), we can see counter-

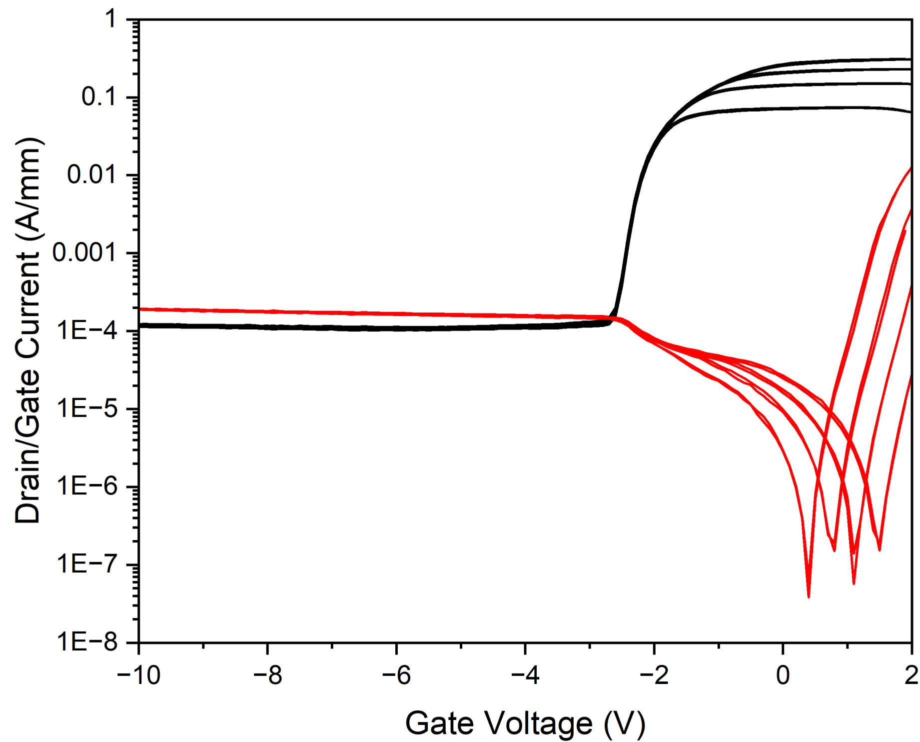
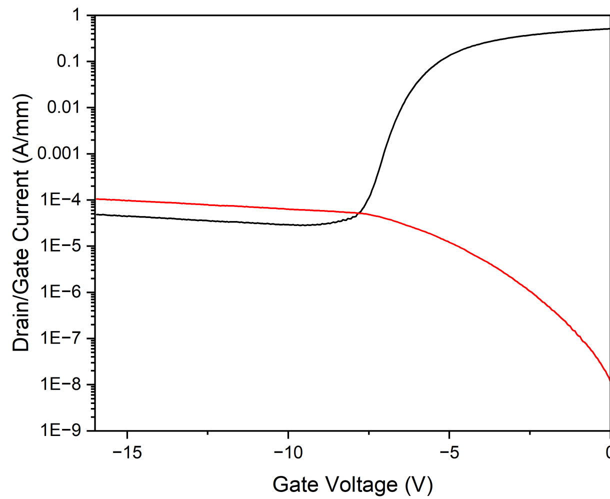


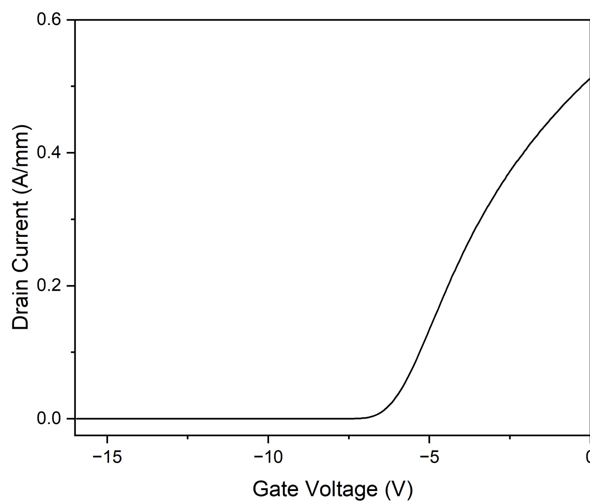
Figure 4.8: Dual transfer sweep of device with no HZO layer. The gate voltage was swept from 2 V to -10 V and back to 2V. The drain voltage was stepped from 0.5 V to 2 V by 0.5 V steps

clockwise hysteresis. The current when sweeping the gate voltage from positive to negative is always higher than the current when sweeping the gate voltage from negative to positive. The memory window of the hysteresis is about 0.5V, matching with the value obtained during the capacitance measurements at room temperature. Due to the added barrier under the gate, the threshold voltage has shifted to around -7 V for the down sweep and -4 V for the up sweep.

Notably in this device, there were visually much steeper drain current lines during the turn on region. This leads us to extract the subthreshold slope of the device. Figure 4.11 illustrates the subthreshold slope of the transfer measure-



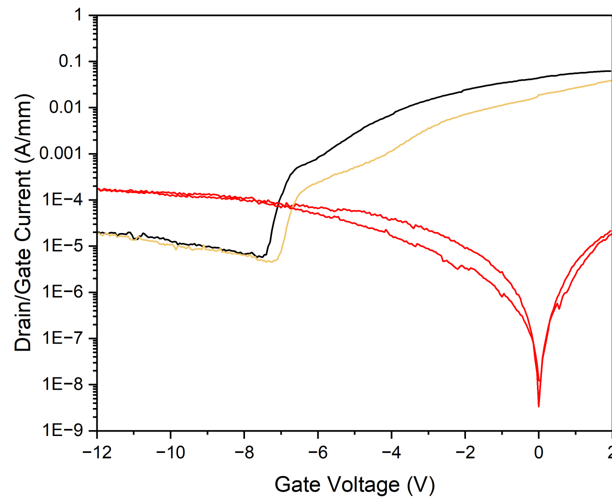
(a) Log Scale



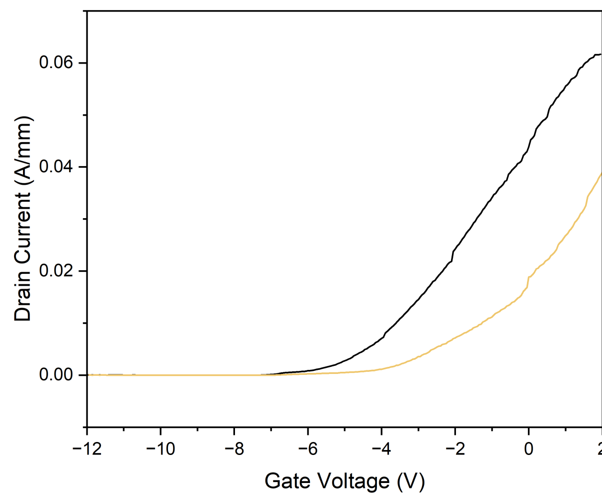
(b) Linear Scale

Figure 4.9: Transfer curves in log scale and linear scale of the device with a 10 nm HZO layer. The drain voltage is at 2 V

ments vs the current. Unfortunately, even with this device having the steepest slope of all measurements, there are no points that exhibit a subthreshold slope below the Boltzmann Limit. It is possible that this is owing to poor contact resistance. Another possibility is that there was not enough strain during the



(a) Log Scale



(b) Linear Scale

Figure 4.10: Dual transfer curves in log scale and linear scale of the device with a 10 nm HZO layer. The drain voltage is at 1 V. The black and beige lines represent the down sweep and up sweep of the gate voltage respectively

annealing process to produce a ferroelectric with a high enough negative differential capacitance effect to further reduce the subthreshold slope.

Figure 4.12 shows the dual transfer sweep of the device with 20 nm of HZO.

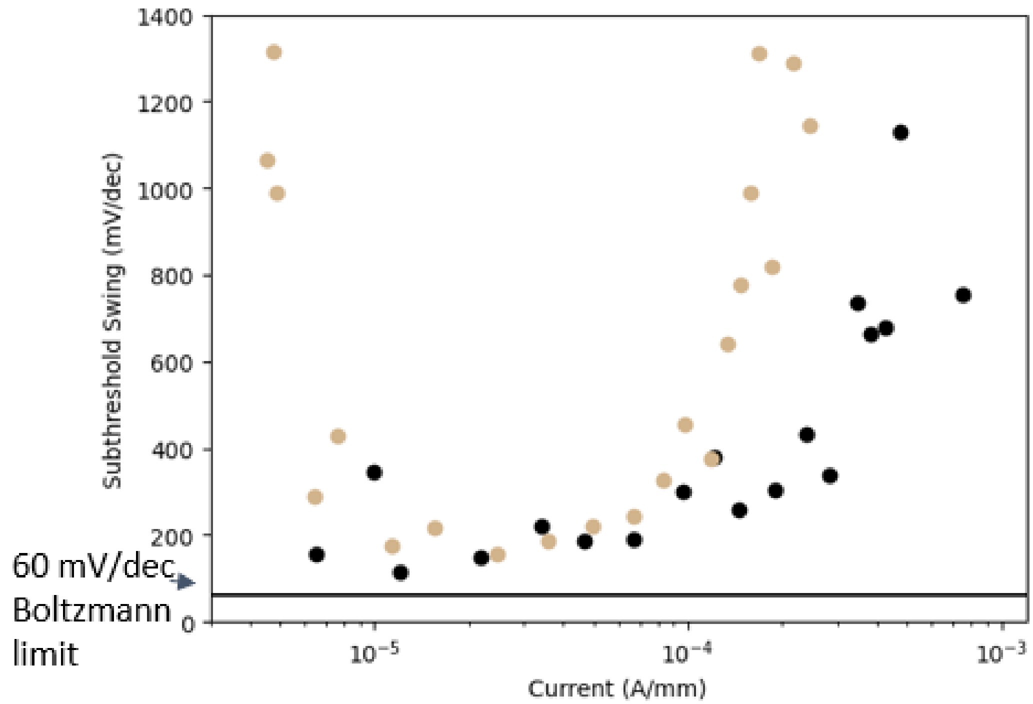
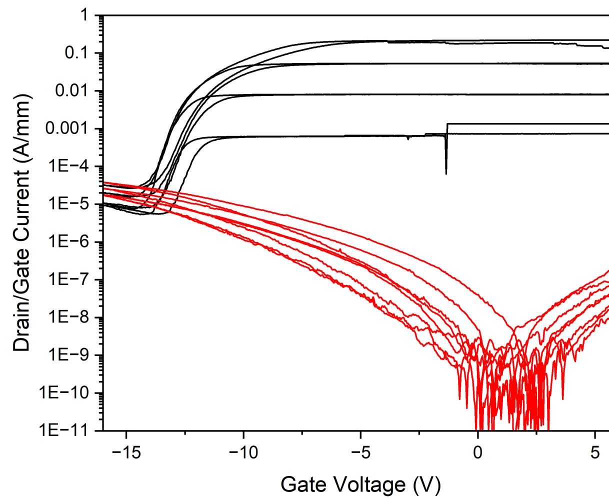


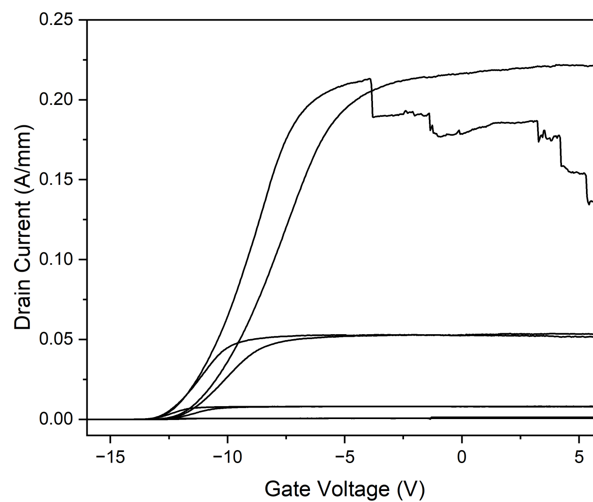
Figure 4.11: Subthreshold slope plot of the measured data from Figure 4.10(a)

Similarly to the sample with 10 nm of HZO, there is an observed counterclockwise hysteresis. The memory window is also about 0.5V. From this, we can say that the thickness of HZO, between 10 nm and 20 nm, has no effect on the width of the memory window in these devices. The only effect the thickness of HZO has is the shifting of threshold voltages. With 20 nm of HZO, the threshold voltage has shifted to around -13.4 V for the down sweep and -12 V for the up sweep.

When comparing the transfer curves between the samples with HZO and the ones without, there are a couple differences. Other than the previously mentioned shifting the threshold voltage and the added hysteresis, the gate current is largely reduced. Figure 4.13 shows a comparison between the gate currents from the samples with and without HZO. At large positive gate biases, we can see that the gate current is drastically reduced. It is about 6 orders of magnitude



(a) Log Scale



(b) Linear Scale

Figure 4.12: Dual transfer sweep of device with a 20 nm HZO layer. The gate voltage was swept from 6 V to -16 V and back to 6V. The drain voltage was measured at 0.1 V, 1 V, 3 V, and 5 V

at positive voltages and 1 order of magnitude at negative voltages less than the sample without HZO. While this is expected with any gate dielectric, it is an added benefit that HZO is a high-k dielectric when compared to conventional

dielectrics like SiO_2. This helps to allow device scaling as HZO is able to maintain a high capacitance without being thin enough for quantum tunneling.

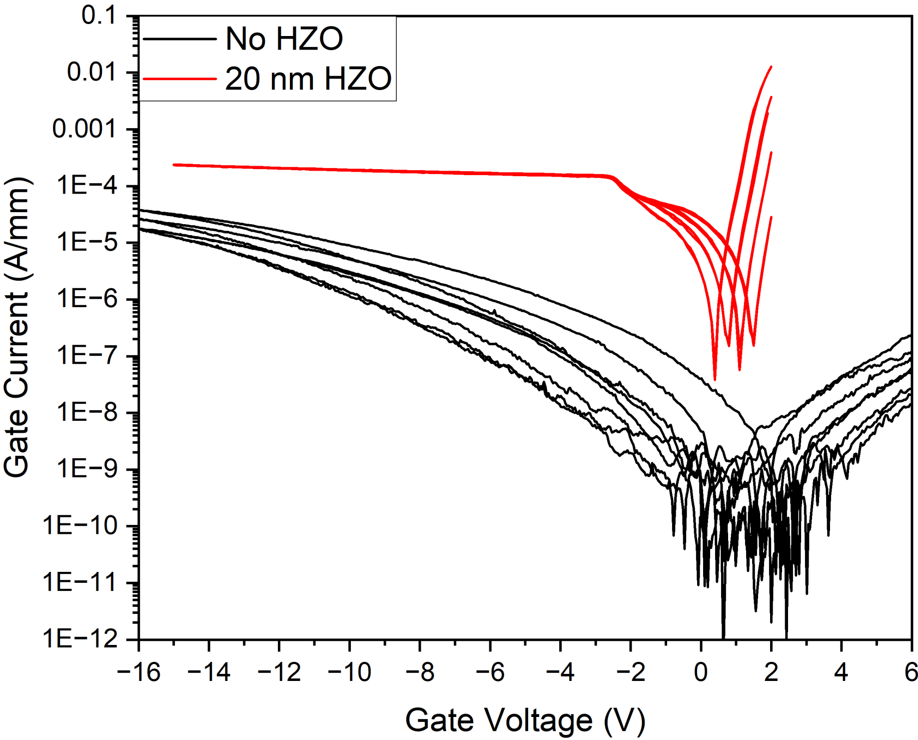


Figure 4.13: Plot of the gate current vs the gate voltage comparing the between the sample with 20 nm of HZO and the sample without any HZO

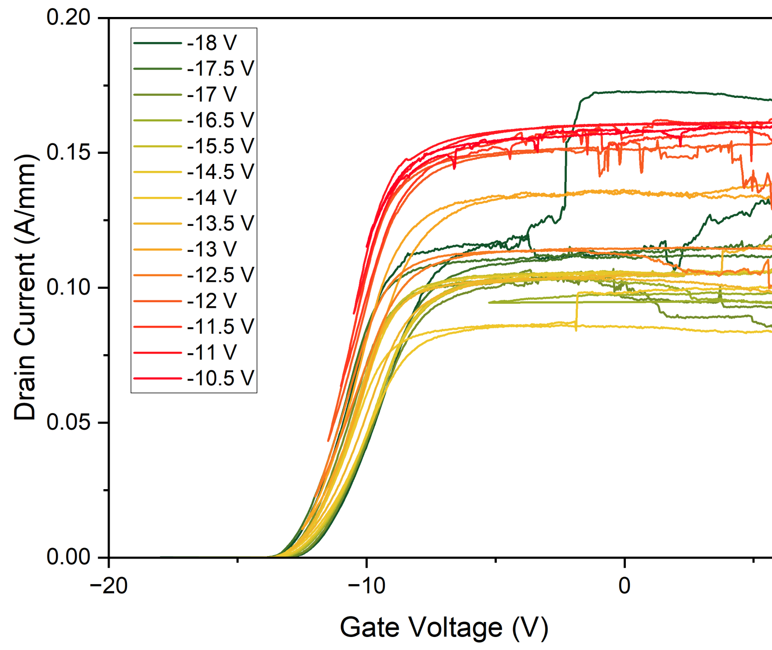
On the opposite side at a high negative bias, we see a high gate current, comparable to the devices without HZO. Although this may appear counterintuitive based on the preceding explanation, the gate current leakage originates from the device's processing architecture rather than the materials themselves. After the HZO is annealed it crystallizes. Since the HZO layer was blanket deposited over the whole device after depositing the ohmic contacts, there is a potential direct connection between the source/drain and the gate. The layer is still insulating so there isn't any shorting of the devices, but there is a slight pathway for cur-

rent to leak through the gate. This is different from the previously mentioned lateral breakdown, but suffers from the same issue of the HZO being a blanket deposition and would require an isolation etch of the HZO to fix.

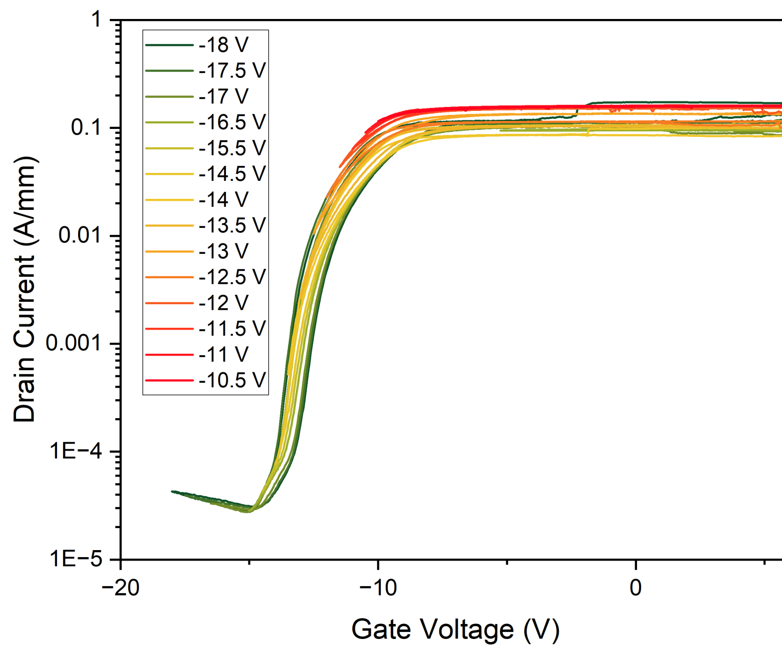
One of the main features we expect to see in devices with a ferroelectric layer is the ability to modulate the threshold voltage of the device. To observe this effect, we can conduct multiple dual sweeps of the gate voltage, keeping the maximum voltage constant while varying the minimum voltages. Figure 4.13 shows the compilation of all the dual transfer sweeps overlaid on each other. In the data taken, the gate voltage was swept from 6V to V_{min} and back to 6V. V_{min} was changed from -18 V to -10.5 volts.

As usual, the transfer curves all exhibit counterclockwise hysteresis. By increasing the value of V_{min}, the threshold voltage on the sweep from negative to positive starts the shift more negative. Throughout the different V_{min} sweeps, the threshold voltage from positive to negative gate voltages stays mostly constant. At a V_{min} of -18 V there is about a 1 V memory window. By a V_{min} of -13.5 V, the memory window is mostly gone and the device acts as a conventional HEMT. This gives rise to about a 1 V threshold voltage tuning range. By biasing V_{min} to different values, we are able to control what the threshold voltage of the device is.

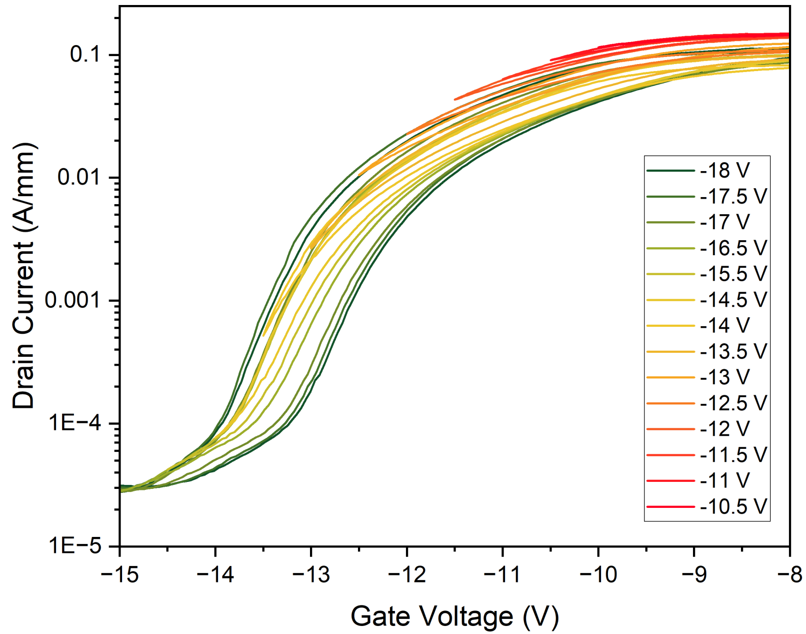
The mechanism for this is due to the ferroelectric not fully switching at higher V_{min} values. If the ferroelectric layer is not fully able to switch, the P-E loop of the material becomes smaller and gives rise to a lower remnant polarization. With small polarization values, there is less impact on the polarization difference occurring at the location of the 2DEG. At around -13.5 V, the HZO's polarization is not able to affect the polarization of the GaN and AlN junction



(a) Linear Plot



(b) Log Plot



(c) Zoomed In Log Plot

Figure 4.13: Transfer hysteresis plot of device with a 20 nm HZO layer. The gate voltage was swept from 6 V to V_{min} and back to 2V. V_{min} was changed between -18 V and -10.5 V. The drain voltage was at 4 V.

at all.

With this data, we can clearly see that the ferroelectric layer is able to modulate the 2DEG channel density and thus the threshold voltage. This can potentially be used in being able to switch a device between D-mode and E-mode as well in other applications like dynamic threshold voltage control in RF devices.

4.3.2 Output Curves

Looking at the output curves of the devices, we can again start with the devices with no HZO layer. Figure 4.14 illustrates the output for the device. The

data shows a drain voltage sweep from 0 V to 10 V with the gate voltage being stepped from -5 V to 4V by steps of 1V. The output plot exhibits the same properties you would expect from a typical FET device. Due to the higher contact resistance, the on current (about 0.8 A/mm) is not as high as other recorded values in literature. The measured on resistance is 8.42 ohm-mm. Additionally, there is some noticeable gate leakage at higher gate biases. This confirms our previous statements about the higher gate leakage in devices without a layer of HZO.

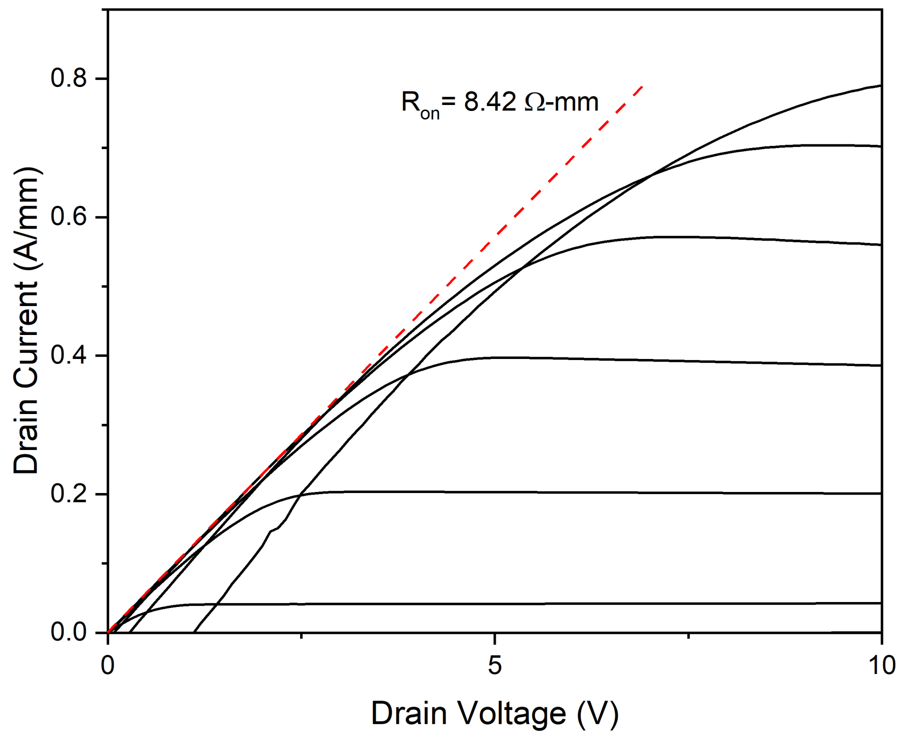


Figure 4.14: Output plot of device with no HZO layer. The gate voltage was stepped from -5 V to 4 V by 1 V steps

Moving on to the output of the device with 20 nm of HZO, we can see in Figure 4.15 that this device also displays typical output behavior. Again the

drain voltage was swept from 0 V to 10 V and the gate voltage was stepped from -10 V to 2 V with steps of 1 V. With around similar contact resistance to the sample with no HZO, we are able to get a similar on current of close to 0.8 A/mm and an on resistance of 3.74 ohm-mm. There is also no noticeable gate leakage. Again, the high-k dielectric layer is working as intended to suppress the leakage.

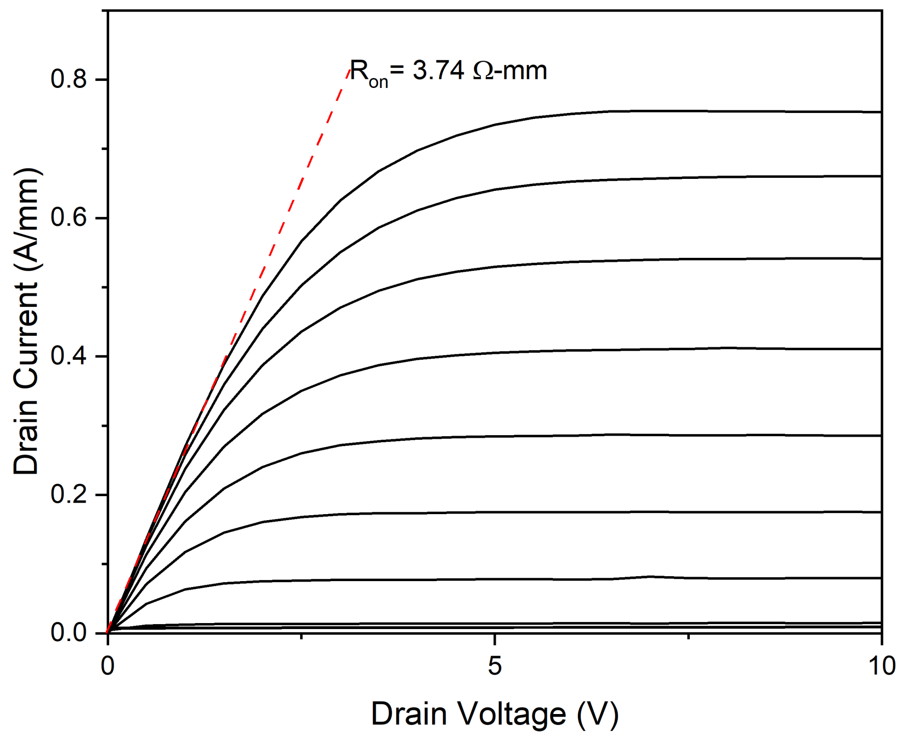


Figure 4.15: Output plot of device with a 20 nm HZO layer. The gate voltage was stepped from -10 V to 2 V by 1 V steps

On top of being able to perform dual transfer sweeps, we can also look at what the result is with a dual output sweep. This dual output sweep is illustrated in Figure 4.16. The drain voltage is still swept from 0 V to 10 V but the direction of the stepping of the gate voltage changes directions. What we ob-

serve is that the output curves consistently show higher output current when the gate voltage is swept from positive to negative voltages. The measurement is repeatable and always fulfills this condition. This matches the same results we found from the dual transfer hysteresis measurements. The device is effectively able to remember the state it was at and allows us to choose the output current we desire, outputting two different drain current values for the same gate current bias.

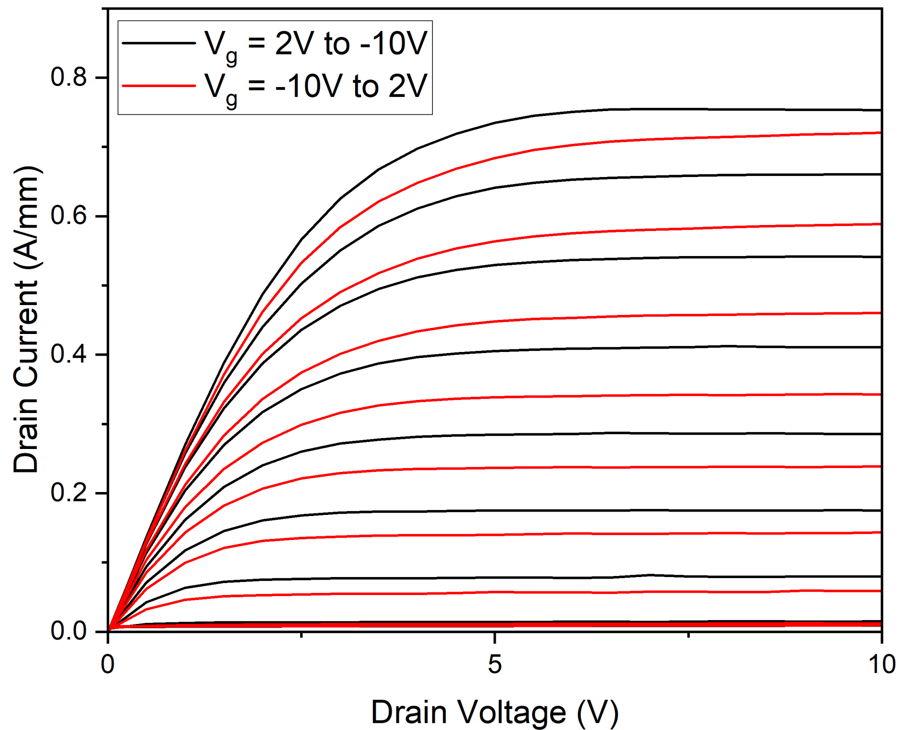


Figure 4.16: Dual output plot of device with a 20 nm HZO layer. The gate voltage was stepped from -10 V to 2 V for the red line and from 2 V to -10 V for the black lines

4.3.3 Electron Beam Lithography Transfer/Output Data

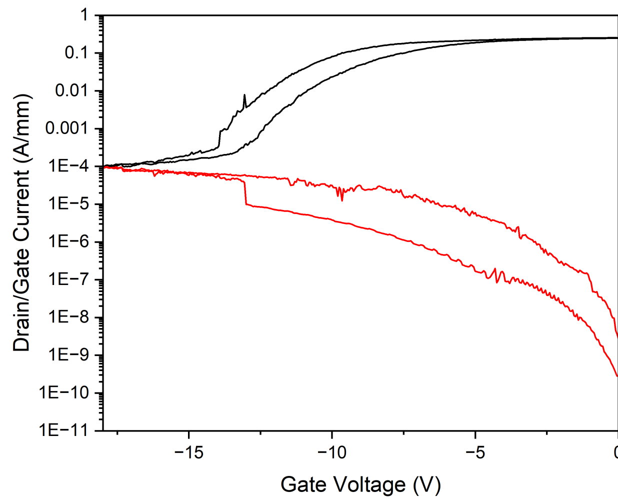
Transfer Characteristics

The last set of data to look at is the measured transfer and output characteristics from electron beam lithography gates. It is of note to remember that the EBL were placed on the sample with 10 nm of HZO. Figure 4.17 shows the transfer data collected from a gate length of about 100 nm and a source to drain distance of 1 um. The on/off ratio is lower than for the optical gates on the same device. This can be attributed to the short channel effects. Because of drain-induced barrier lowering, the transistor permits increased leakage current when the gate voltage falls below the nominal threshold voltage.

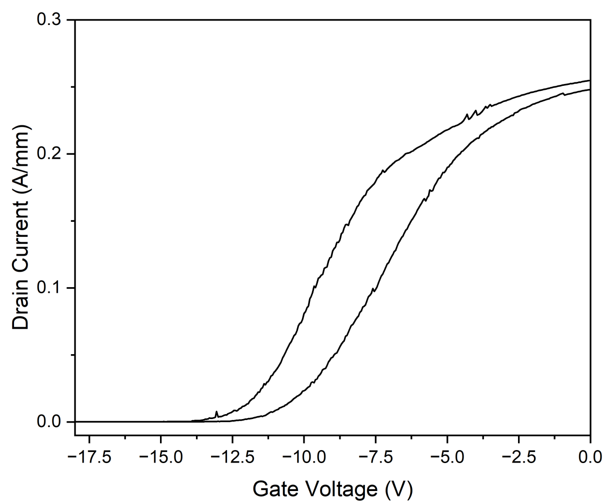
The short channel effects also cause a decrease in the threshold voltage. With the optical gates, the threshold voltage of the down sweep was -6 V. But with the EBL gates, the threshold voltage has shifted to be -13 V for the down sweep and -12 V for the up sweep. There are ways of mitigating this, but those will not be addressed in the scope of this thesis.

Output Characteristics

Figure 4.18 gives us a look at the output of the EBL gate device. The gate voltage was stepped from -10 V to 2 V with steps of 1 V. With the smaller gate length, we can see that the output current is higher than the optical gate counterpart. The on current is about 0.9 A/mm and the calculated on resistance is 3.99 ohm-mm. Even with the short channel effects, there is no noticeable gate leakage at higher voltages. From the transfer curve we can see that the current saturates at a gate



(a) Log Scale



(b) Linear Scale

Figure 4.17: Dual transfer sweep of device with a 10 nm HZO layer using EBL defined gates. The gate voltage was swept from 0 V to -16 V and back to 0V. The drain voltage was measured at 1 V

voltage around -5 V. In the output, even at a gate voltage of 2 V, there isn't any effect from the gate leakage. This further confirms that HZO acts effectively as a gate dielectric, reducing gate leakage.

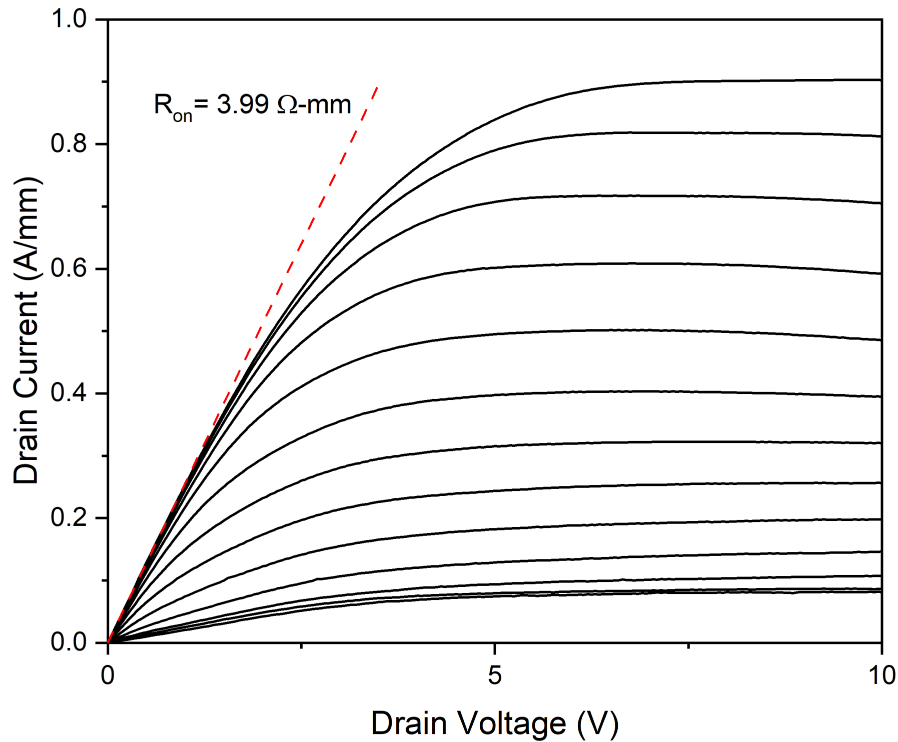


Figure 4.18: Output plot of device with a 10 nm HZO layer using EBL defined gates. The gate voltage was stepped from -10 V to 2 V by 1 V steps

Hysteresis

Notably, the hysteresis is still prominent in the EBL transfer curve. The memory window is about 1.2 V. This is a bit larger than the values obtained for the optical gates. It is possible that due to the increased current output, the HZO layer has an easier time switching and thus is able to provide a larger memory window. Knowing this, we can say that the gate length has a positive effect on the ferroelectric properties of the device and that they are easily able to be scaled down without worry about the ferroelectric properties.

CHAPTER 5

REGROWN CONTACTS DEVICE CHARACTERIZATION AND PERFORMANCE

Two devices were processed with regrown contacts. Table 5.1 shows the values from hall measurements of the devices before processing. Since the structure of the devices for the regrown process, grown in the MBE, are the same for the alloyed contact devices, they have similar sheet charge, mobility and sheet resistances.

Device	Sheet Charge	Mobility	Sheet Resistance
Units	$/cm^2$	$cm^2/V\text{-}s$	Ω/sq
1	-1.635 x 10^{-13}	1380	277.4
2	-1.513 x 10^{-13}	1420	290.2

Table 5.1: Measured data through Hall Measurements of the device structures for regrown contacts before processing

After processing the ohmic contacts on the devices, TLM measurements were carried out to calculate the contact and sheet resistances. Table 5.2 shows all the calculated contact resistances and sheet resistances for the regrown contact devices. As expected, both contact and sheet resistances are much lower than for the alloyed contacts. The values are at an optimal range for examining the full capabilities of the devices.

Device	Contact Resistance	Sheet Resistance
Units	Ω-mm	Ω/sq
1	0.358	270.98
2	0.312	111.74

Table 5.2: Measured contact resistance and sheet resistance post device processing of regrown contacts. Values were calculated through TLM measurements

The devices are currently still being processed and thus there is no measured data obtained from them yet. In the future, the devices are planned on

being finished and measured, with the expectation of achieving improved on currents, higher on/off ratios, and maintaining or enhancing interactions with the ferroelectric HZO layer.

CHAPTER 6
CONCLUSION AND FUTURE WORKS

Devices are nearing the limits of their current capabilities, prompting the need for significant innovations to achieve further improvements. One promising innovation involves integrating ferroelectric materials. This thesis explores the enhancements achieved by integrating a ferroelectric layer beneath the gate of an AlN/GaN high electron mobility transistor. By doing so, it aims to highlight the potential advancements available in emerging device architectures.

The material selected for the ferroelectric layer is hafnium zirconium oxide (HZO) thanks to its strong ferroelectric properties in the orthorhombic phase. HZO is particularly advantageous because it maintains ferroelectricity even at very thin layers (as thin as 5 nm) and is fully compatible with CMOS fabrication processes.

Five different devices were fabricated, each with varying thicknesses of HZO. The devices were processed with alloyed contacts and although the contact resistance was not ideal, the devices performed as anticipated. Through these devices, the study aimed to demonstrate the ability to modulate the threshold voltage, reduce gate leakage, achieve a decreased subthreshold slope, and exhibit memory storage capabilities.

PUND measurements confirmed the remnant polarization of the HZO films to be 14.155 $\mu C/cm^2$ in the MFM structure and 11.485 $\mu C/cm^2$ in the device structure. The observed decrease in remnant polarization compared to values reported in the literature is likely attributed to the emergence of antiferroelectric behavior, stemming from a higher concentration of Zr relative to Hf in the ma-

terial.

The transfer curves of the devices displayed clear counterclockwise hysteresis. This hysteresis, combined with the modulation of the gate voltage, showcased a tuning range of 1 V for the threshold voltage. Although the subthreshold slope did not surpass the Boltzmann Limit, the gate leakage current in samples with HZO was reduced by approximately six orders of magnitude compared to those without HZO. Additionally, the output current analysis revealed two different current levels for the same gate voltage bias, indicating the memory capabilities of the device.

Given that the slight antiferroelectric properties led to a decrease in the remnant polarization of the HZO layer, future work should focus on analyzing devices with a more robust HZO layer. By achieving a composition closer to 50 percent Hf and 50 percent Zr, the remnant polarization is expected to align more closely with values reported in the literature. This adjustment could result in a larger memory window in the transfer curves and a greater threshold voltage tuning range.

In addition to perfecting the deposition of the HZO layer, exploring other ferroelectric materials could yield better interaction with the AlN/GaN heterostructure. Currently, significant research is focused on ferroelectric aluminum scandium nitride (AlScN).[11] Since AlScN is a nitride that can be deposited using Molecular Beam Epitaxy, it is feasible to create an all-nitride ferroelectric HEMT heterostructure in-situ. This approach could result in cleaner interfaces, larger hysteresis curves, and improved device performance.

APPENDIX A

CALCULATION ON VOLTAGE DROP IN HZO LAYER

During the PUND measurements, it is important to calculate the electric field through only the HZO layer since there are so many other layers that voltage drops across. Below shows the equations used to calculate the voltage drop across the HZO in the devices.

$$\frac{1}{C_{Total}} = \frac{1}{C_{HZO}} + \frac{1}{C_{Al_2O_3}} + \frac{1}{C_{AlN}} + \frac{1}{C_{GaN}} \quad (A.1)$$

$$\frac{1}{C_{Total}} = \frac{t_{HZO}}{k_{HZO}\varepsilon_0 A} + \frac{t_{Al_2O_3}}{k_{Al_2O_3}\varepsilon_0 A} + \frac{t_{AlN}}{k_{AlN}\varepsilon_0 A} + \frac{t_{GaN}}{k_{GaN}\varepsilon_0 A} \quad (A.2)$$

$$Q = CV = \left[\frac{t_{HZO}}{k_{HZO}\varepsilon_0 A} + \frac{t_{Al_2O_3}}{k_{Al_2O_3}\varepsilon_0 A} + \frac{t_{AlN}}{k_{AlN}\varepsilon_0 A} + \frac{t_{GaN}}{k_{GaN}\varepsilon_0 A}\right]^{-1} \times 1V \quad (A.3)$$

$$V = \left[\frac{t_{HZO}}{k_{HZO}\varepsilon_0 A} + \frac{t_{Al_2O_3}}{k_{Al_2O_3}\varepsilon_0 A} + \frac{t_{AlN}}{k_{AlN}\varepsilon_0 A} + \frac{t_{GaN}}{k_{GaN}\varepsilon_0 A}\right]^{-1} \times 1V \times \frac{t_{HZO}}{k_{HZO}\varepsilon_0 A} \quad (A.4)$$

Using the same values as in Table 4.3:

$$V = \left[\frac{20nm}{30\varepsilon_0 A} + \frac{3nm}{9.34\varepsilon_0 A} + \frac{2nm}{9\varepsilon_0 A} + \frac{2nm}{9.7\varepsilon_0 A}\right]^{-1} \times 1V \times \frac{20nm}{30\varepsilon_0 A} \quad (A.5)$$

$$V = 0.470719V \quad (A.6)$$

This means that for ever 1V applied to the device, around 0.47V drop across the HZO layer.

APPENDIX B

ALLOYED CONTACTS PROCESS FLOW

B.1 Device Isolation

Step	Device Isolation Etch
1	sonicated Acetone and IPA, 3 minuted each
2	Spin SPR700, 5000 5000 30sec
3	Bake 95C, 60sec
4	Autostepper, 0.2sec exposure, mask = FET9ISO2
5	Post-bake 115C, 60sec
6	Develop in 726 MIF, 60sec
7	Verify patterns optically
8	Glen 1000 O2 descum, recipe 3 - active mode, 100W, 120sec
9	Etch GaN/AlN/GaN layers with PT770, recipe Xing 2 - etch rate ~ 7.5 nm/min
10	Remove photoresist - sonicated 1165, Acetone and IPA, 3 minuted each

B.2 Ohmic Contacts

Step	Ohmic Metallization
1	sonicated Acetone and IPA, 3 minuted each
2	Spin nLOF2020, 7000 7000 30sec
3	Bake 115C, 60sec
4	Autostepper, 0.2sec exposure, mask = FET9OHM
5	Post-bake 115C, 60sec
6	Develop in 726 MIF, 60sec
7	Verify patterns optically
8	Glen 1000 O2 descum, recipe 3 - active mode, 100W, 120sec
9	30:1 BOE dip, 1 min
10	Deposit Ti/Al/Ni/Au (20/150/50/50 nm) via odd-hour evaporator
11	Remove photoresist - sonicated 1165, Acetone and IPA, 3 minuted each
12	Measure TLM pre-anneal
13	Anneal contacts via RTA - 830C, 60sec, N2 ambiant

B.3 HZO Deposition

Step	HZO Deposition
1	Via Arradiance ALD deposit HZO/Al2O3, 50-50 cycles of Hf and Zr
2	Verify thicknesses in Woollam RC2 Spectroscopic Ellipsometer
3	Anneal HZO via RTA - 400C, 60sec, N2 ambiant

B.4 Optical Gate Contacts

Step	Gate Metallization
1	sonicated Acetone and IPA, 3 minuted each
2	Spin nLOF2020, 7000 7000 30sec
3	Bake 115C, 60sec
4	Autostepper, 0.2sec exposure, mask = FET9GT
5	Post-bake 115C, 60sec
6	Develop in 726 MIF, 60sec
7	Verify patterns optically
8	Glen 1000 O2 descum, recipe 3 - active mode, 100W, 120sec
9	30:1 BOE dip, 1 min
10	Deposit Ni/Au (50/100 nm) via odd-hour evaporator
11	Remove photoresist - sonicated 1165, Acetone and IPA, 3 minuted each

B.5 EBL Gate Contacts

Step	EBL Gate Metallization
1	sonicated Acetone and IPA, 3 minuted each
2	Pre-bake 200C, 300sec
3	Spin PMGI SF9, 5000 5000 30sec
4	Bake 185C, 300sec
5	Spin UV210GS-0.6, 2000 5000 60sec
6	Bake 135C, 90sec
7	Expose via JEOL 6300 - Dose = 170 um/cm2
8	Post-bake 115C, 105sec
9	Develop in 321 MIF, 65sec
10	Verify patterns optically
11	Glen 1000 O2 descum, recipe 3 - active mode, 100W, 120sec
12	30:1 BOE dip, 1 min
13	Deposit Ni/Au (50/100 nm) via odd-hour evaporator
14	Remove photoresist - 1165 at 80C for 10min, IPA

APPENDIX C

REGROWN CONTACTS PROCESS FLOW

C.1 n+ GaN Regrowth

Step	Regrown n+ GaN Contact
1	sonicated Acetone and IPA, 3 minuted each
2	Soak in 6:1 BOE, 30sec
3	Deposit SiO2 (~250 nm) via Oxford PECVD - recipe: low rate SiO2
4	Deposit Cr (40-50 nm) via odd-hour evaporator
5	Spin SPR700, 5000 5000 30sec
6	Bake 95C, 60sec
7	Autostepper, 0.2sec exposure, mask = FET 9 Regrowth Mask
8	Post-bake 115C, 60sec
9	Develop in 726 MIF, 60sec
10	Verify patterns optically
11	Glen 1000 O2 descum, recipe 3 - active mode, 100W, 120sec
12	30:1 BOE dip, 1 min
13	Etch Cr layer with PT770, recipe Xing 6 - etch rate ~ 33 nm/min
14	Remove photoresist - sonicated 1165, Acetone and IPA, 3 minuted each
15	Etch SiO2 via Oxford 81, recipe CHF3/O2 oxide etch
16	Check height of SiO2/Cr layer with P7 Profilometer
17	Etch ~20 nm in GaN/AlN layer with PT770, recipe Xing 2
18	Soak in HCl, 60sec,
19	Load into MBE chamber for n+ GaN deposition

C.2 Alignment Etch

Step	Alignment Etch
1	Soak in HCl till backside Indium is fully removed
2	sonicated Acetone and IPA, 3 minuted each
3	Spin SPR700, 5000 5000 30sec
4	Bake 95C, 60sec
5	Autostepper, 0.2sec exposure, mask = FET 9 Alignment Mask
6	Post-bake 115C, 60sec
7	Develop in 726 MIF, 60sec
8	Verify patterns optically
9	Glen 1000 O2 descum, recipe 3 - active mode, 100W, 120sec
10	Etch layers with PT770 (~5 min), recipe Xing 1
11	Remove photoresist - sonicated 1165, Acetone and IPA, 3 minuted each
12	Soak in 6:1 BOE - 15min, followed by HF - 5 min for SiO2/n+ GaN liftoff

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