CGMD for Full Screen Semiconductor Process Simulation

A Dissertation

Presented to the Faculty of the Graduate School

of Cornell University

In Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

June-Yo Chen

August 2025

CGMD for Full Screen Semiconductor Process Simulation

June-Yo Chen, Ph.D.
Cornell University 2025

Semiconductor scaling now demands sub-10 nm patterning and sub-nanometer dopant control—requirements that strain the cost and accuracy limits of extreme-ultraviolet (EUV) lithography and conventional TCAD process simulators. This dissertation develops two complementary, simulation-driven pathways to overcome those barriers. First, a coarse-grained molecular-dynamics (MD) framework is used to map the process window for PS-b-PMMA directed self-assembly (DSA) on chemo-epitaxial, brush-coated substrates. Systematic sweeps of pinning-site radius, brush height, and graft density reveal a cooperative confinement regime: brush heights of 2–4 σ combined with pinning radii of 6–8 σ maximize six-fold bond-orientational order (ψ_6 > 92 %), suppress line-edge roughness to < 1 σ (three-sigma envelope), and eliminate pillar tapering. Relative to an unpatterned substrate, optimal flat-pin templates raise ψ_6 from 88.7 % to > 91 %, underscoring the cost-saving potential of DSA as a partial substitute for EUV multiple patterning.

Second, a quantum-informed, multi-process MD workflow couples density-functional-theory-derived Si–B Lennard-Jones parameters with a Tersoff Si potential to track boron implantation, pre-deposition, and rapid-thermal annealing in a single LAMMPS environment. The model reproduces 3 keV SIMS profiles for 1×10^{16} cm^{-2} and 5×10^{15} cm^{-2} implants to within ± 5 % over 0–15 nm—more than twice the accuracy of SRIM-based predictions. A 1 nm amorphous B capping layer boosts near-surface concentration by ≈ 35 % without widening the 10–90 % junction depth, while a 950 °C, 8 M-step spike anneal removes ≈ 46 % of vacancies and ≈ 42 % of interstitials, balancing activation against defect regeneration. Collectively, the framework delivers sub-nanometer junction accuracy, explicit defect chemistry, and seamless process

integration, opening a predictive route for co-optimizing implant dose, energy, surface treatments, and millisecond anneals.

Together, these two simulation platforms provide actionable design rules and quantitative benchmarks that enable cost-effective nanolithography and high-precision dopant engineering, thereby advancing the manufacturability of next-generation CMOS technology.

BIOGRAPHICAL SKETCH

June-Yo Chen was born in 1994 in Taichung, Taiwan. He graduated from Taichung First Senior High School in 2012 and went on to earn his Bachelor of Science degree in Chemical Engineering from National Tsing Hua University (NTHU) in 2016. During his undergraduate studies, he developed a strong interest in nanomaterials and computational modeling, which led him to pursue further academic research.

After graduation, he moved to the United States to pursue his doctoral studies at Cornell University in the Robert Frederick Smith School of Chemical and Biomolecular Engineering. At Cornell, he joined the research group of Prof. Yong Lak Joo, where his Ph.D. work focused on advanced simulation methods for semiconductor manufacturing processes. His research included ion implantation modeling, directed self-assembly of block copolymers, and process optimization using machine learning. He also completed an internship at Applied Materials, gaining hands-on experience in cleanroom fabrication and semiconductor process integration.

In 2025, June-Yo successfully defended his dissertation and received his Ph.D. in Chemical Engineering. Upon graduation, he is expected to join United Integrated Services (UIS) in Phoenix, Arizona, as an Instrumentation and Control Engineer, where he will contribute to the design and optimization of semiconductor fab systems.

ACKNOWLEDGEMENTS

Pursuing and completing this dissertation has been an extraordinary journey—one made possible only through the guidance, collaboration, and unwavering support of many people. I would like to express my deepest gratitude to all who have walked this path with me.

First and foremost, I thank Prof. Joo, my advisor, for your sharp scientific insight, rigorous standards, and constant encouragement. Your thoughtful questions and calm confidence pushed me to examine every assumption and to keep moving forward whenever I encountered obstacles. This work simply would not exist without your mentorship.

I am also profoundly grateful to Prof. Shuwen Yue and Prof. Julia Dshemuchadse. Your constructive feedback during committee meetings and manuscript reviews sharpened my thinking and broadened the scope of my research. The perspectives you shared—spanning theory, experiment, and materials analysis—helped me refine the dissertation into its present form.

My sincere thanks go to the members of our research group. Late-night simulation runs, whiteboard debates, frantic conference deadlines, and the daily exchange of ideas created an environment that was both intellectually stimulating and supportive. Your willingness to lend a hand, share data, or simply listen made even the toughest stretches of research feel achievable. I could not have asked for a better team of colleagues and friends.

Last, but never least, I am indebted to my family. Your unconditional love, patience, and encouragement gave me the strength to persevere far from home and to stay focused on my goals. Knowing that you believed in me—even when I doubted myself—has been my greatest source of motivation.

I would also like to extend heartfelt thanks to the music of Aespa and LE SSERAFIM. During the most difficult periods of writing and experimentation—when motivation waned and self-doubt crept in—their songs offered me unexpected strength and comfort. In particular, Aespa's *Supernova* and LE SSERAFIM's *EASY* became my companions through moments of discouragement and emotional lows. Their lyrics and energy reminded me to keep going, to embrace uncertainty, and to believe in my worth even when things felt overwhelming. In times when I felt alone, their music reminded me that I wasn't—and for that, I am deeply grateful.

To everyone who has guided, challenged, and supported me along the way: thank you. This dissertation is as much a product of your generosity and belief as it is of my own efforts.

TABLES OF CONTENTS

LIST OF TABLES

LISTS OF FIGURES

CHAPTER 1

Introduction to Semiconductor Fabrication Processes

1.1 Overview of Semiconductor Fabrication Processes

Modern semiconductor manufacturing is a highly complex, multi-step endeavor, requiring hundreds of sequential process stages to transform raw silicon wafers into functional integrated circuits. A single wafer typically undergoes on the order of 300–500 individual processing steps (lithography, etching, doping, deposition, etc.), and the entire fabrication cycle can span several weeks.[1] In fact, advanced chip fabrication flows regularly exceed 500 process steps in total.[2] These steps must be carefully coordinated to build up the intricate transistor structures and interconnects with nanometer precision, while minimizing defects and variations.

Each “unit process” contributes a layer or feature to the device. For example, photolithography defines circuit patterns, ion implantation introduces dopants, and thin-film deposition lays down conductive or insulating layers. The combination and repetition of these unit processes gradually construct the integrated circuit in a layer-by-layer fashion.[3] The complexity and length of modern process flows reflect the drive toward ever smaller feature sizes (per Moore’s Law) and the integration of new materials. As devices shrink and new structures like 3D transistors emerge, fabrication processes have had to evolve in sophistication. Today’s state-of-the-art chips pack billions of nanoscopic transistors, which can only be realized through extremely precise and controlled processing steps executed in ultraclean facilities.

The sheer number of steps and the tight specifications in semiconductor fabrication make it both technically demanding and capital intensive. Leading-edge wafer fabs employ specialized equipment for each major process (lithography scanners, implant machines, furnaces, deposition reactors, etc.), and even a minor error in one step can compromise the entire device yield. An overview of several key fabrication processes is provided below, followed by a discussion of simulation techniques used to model these processes. Emphasis is given to the challenges in modeling such complex processes and the motivations for employing advanced simulation methods – including molecular dynamics (MD), coarse-grained MD (CGMD), and density functional theory (DFT) – to gain deeper insight and predictive capability in semiconductor process engineering.

1.2 Photolithography

Photolithography is the patterning process at the heart of semiconductor manufacturing – it is the method by which circuit designs are transferred onto the silicon wafer. Without lithography, mass-production of microchips would not be possible; indeed, "there would be no semiconductor industry without lithography".[4] In a typical photolithographic step, a light-sensitive polymer (photoresist) is coated on the wafer, then exposed to intense light through a photomask that contains the desired circuit pattern. The exposed regions of resist undergo chemical changes, allowing them to be selectively removed in a development process. Subsequent etching steps transfer the revealed pattern into the underlying material. This sequence – coat, expose, develop, etch – is repeated many times with different masks to define all the fine features of the integrated circuit.[5]

For Advances in Lithography, the minimum feature size printable by photolithography is fundamentally limited by the wavelength of light used. To continue shrinking

transistor dimensions, the industry has continually moved to shorter exposure wavelengths and novel techniques. Deep ultraviolet (DUV) lithography at 248 nm and 193 nm (using excimer lasers) enabled patterning down to the 90 nm and 45 nm technology nodes through various resolution enhancement tricks.[6, 7] The current workhorse is 193 nm immersion lithography, often with multiple patterning steps to achieve features far smaller than 193 nm. More recently, extreme ultraviolet (EUV) lithography at a 13.5 nm wavelength has been introduced for leading-edge nodes (~7 nm, 5 nm, and beyond).[8, 9] EUV's much shorter wavelength allows it to print extremely fine patterns (on the order of 20 Å resolution) with a single exposure, largely eliminating the need for multiple-patterning techniques.[10] This has resulted in immediate benefits: smaller feature sizes and higher transistor densities per chip. In summary, continuous innovation in optical lithography – from DUV to EUV – has been pivotal for sustaining Moore's Law of scaling.

As for the Cost and Complexity, the leap to EUV, however, has come with tremendous engineering challenges and costs. EUV scanners are among the most complex machines ever built. Each is roughly the size of a bus, containing over 100,000 precision parts, and costs on the order of $150 million.[11] These systems require ultrapure vacuum environments, defect-free reflective optics, and high-energy plasma light sources, making them extraordinarily expensive to manufacture and operate. The total investment to implement EUV lithography in a fab (including supporting infrastructure and maintenance) easily runs into billions of dollars.[12] Because only a few companies can afford such tools, EUV has heightened the economic barriers of cutting-edge chip production. The complexity is also extreme – for instance, EUV masks have multilayer mirrors and even a single particle can ruin a mask due to the short wavelengths involved. All these factors make EUV lithography as much a triumph of engineering as of science.

On the other hand, Directed Self-Assembly (DSA) is an alternative. The escalating cost and physical limits of optical lithography have motivated exploration of

alternative nanopatterning methods. One promising approach is directed self-assembly (DSA) using block copolymers, which can form periodic nanostructures through molecular self-organization.[13-15] In DSA, a thin film of block copolymer can self-assemble into regular patterns (lines, holes, etc.) with feature sizes below what optical tools can resolve. Importantly, DSA can work in conjunction with conventional lithography – for example, a larger guide pattern defined by photolithography can direct the self-assembly of polymers to refine features at a much finer scale. This can effectively multiply the resolution of a given lithographic exposure. The key advantage of DSA is cost-effectiveness: it leverages relatively inexpensive materials and chemical processes rather than requiring new optical equipment.[16] Studies have shown that DSA could allow the continued use of existing 193 nm lithography tools and delay the need for EUV in certain layers, yielding significant cost savings.[17] However, challenges remain in achieving defect-free self-assembly and integrating DSA into high-volume manufacturing. Nonetheless, DSA BCP stands out as an attractive complementary technique to push patterning to the sub-10 nm scale without the astronomical expense of next-generation steppers.

In summary, photolithography is an essential enabling process that dictates how small and dense features on a chip can be. Advances like EUV have extended optical lithography to the atomic scale, albeit at high cost, while novel techniques like DSA offer potential low-cost routes to further extend patterning capabilities. The relentless demand for higher transistor density will continue to drive innovation in lithography and patterning, be it through new optics, new materials, or new self-assembling processes.

1.3 Ion Implantation

Ion implantation is the principal technique for introducing dopant impurities into semiconductor wafers in a highly controlled manner. Since the 1970s, it has become by far the most widely used method for doping silicon, effectively replacing earlier

thermal diffusion methods for most applications.[18, 19] In an ion implantation process, ions of the desired dopant element (such as B, P, or As for silicon) are generated in an ion source, accelerated to high kinetic energies (ranging from a few keV to several MeV), and directed at the target silicon wafer. The energetic ions penetrate the surface and come to rest below the surface after a series of collisions.[20, 21] By adjusting the ion energy, dose, and incident angle, manufacturers can precisely control the depth and concentration profile of the implanted dopants.

A major advantage of ion implantation is its excellent dose and depth controllability compared to thermal diffusion doping.[18] Implantation is typically a room-temperature or low-temperature process, so it does not cause the substantial lateral spreading of dopants that occurs in high-temperature diffusion. Each ion's path is stochastic, but on average the dopant distribution follows a known profile (often approximately Gaussian about a projected range) that can be predicted for given implant conditions. This allows engineers to implant dopants in very localized regions (e.g. source/drain of a transistor) with minimal impact on surrounding areas. By contrast, old diffusion methods introduced dopants across the wafer more uniformly and required physical masking to control where doping occurred. Ion implantation also enables shallow junctions for modern transistors by using low ion energies (even just a few hundred eV for ultra-shallow junctions).[22, 23] As device features have scaled down, implants with energies in the sub-keV range are used to confine dopants within around 10–20 nm of the surface.

However, the violent collision process inherent to implantation leaves damage in the silicon lattice that must be repaired. As each ion plows through the crystal, it creates a cascade of atomic displacements – knocking silicon atoms out of their lattice sites and generating point defects (vacancies and interstitials) and sometimes even an amorphous layer if the dose is high.[24, 25] After a heavy implant, the silicon may be "amorphized" in the near-surface region – essentially a glassy layer of Si – and even a lighter implant produces numerous crystalline defects. Immediately after implantation,

the wafer's electrical properties are degraded because many dopant atoms are not on proper lattice sites (hence electrically inactive) and the crystal damage introduces deep-level traps that immobilize charge carriers.[26] For this reason, ion implantation is always followed by an annealing step to heal the damage and activate the dopants. During annealing, the silicon lattice is healed as displaced atoms return to lattice sites and defects recombine, and dopant atoms incorporate substitutionally into the lattice, becoming electrically active.[27] The annealing process must be carefully tuned: it should be hot and long enough to repair damage and achieve high activation, but not so excessive that the dopants diffuse beyond the intended junction depth. The next section discusses the annealing techniques used to achieve this balance.

1.4 Annealing

Thermal annealing is a critical step after ion implantation (and after other processes that induce defects) to restore the crystalline order and electrically activate dopants. In essence, annealing involves heating the wafer to an elevated temperature for a controlled duration, allowing the silicon atoms to regain their proper lattice positions and enabling dopant atoms to occupy substitutional sites. The primary goal of post-implant annealing is to repair implantation-induced lattice damage (which has a high activation energy, on the order of ~5 eV) while simultaneously minimizing undesirable dopant diffusion (activation energies ~3–4 eV for dopant diffusion).[28, 29] Because defect repair typically has a higher activation energy than dopant diffusion, using a very high temperature for a very short time can preferentially heal damage before dopants have time to diffuse significantly.[30, 31]

In the early days of semiconductor processing, annealing was performed in furnaces at temperatures around 800–1000 °C for extended times (tens of minutes to hours). The furnace anneals successfully repaired damage and activated dopants, but the long durations led to substantial dopant diffusion (smearing out junction profiles) and were incompatible with the ultra-shallow junctions needed for modern devices. The industry

therefore shifted to rapid thermal annealing (RTA) in the 1980s and 1990s.[32] RTA uses high-intensity lamps or lasers to heat the wafer to peak temperatures ~1000–1100 °C for only a few seconds or less, then quickly cool it down. By shortening the anneal time dramatically (to seconds or milliseconds), RTA achieves the necessary lattice repair and dopant activation while limiting the time available for dopants to diffuse.[33] RTA is typically done one wafer at a time for uniformity, in contrast to batch furnaces.

As device dimensions pushed into the deep nanometer regime, even RTA was not sufficient to prevent diffusion in some cases. This led to millisecond annealing techniques such as flash lamp annealing and laser spike annealing. In these approaches, the wafer is heated to extremely high temperatures (1200–1300 °C or more) but only for a few milliseconds or even microseconds. The temperature ramp rates are on the order of 10^5–10^6 °C/s. Millisecond anneals provide an almost instantaneous thermal pulse: the wafer surface can reach >1200 °C to anneal out damage and activate almost 100% of dopants, but it cools before significant diffusion can occur.[34] Empirical data and simulations show that such ultrafast anneals yield very abrupt, shallow junctions with excellent electrical activation.[35, 36] For example, in boron-implanted silicon, millisecond laser annealing can activate dopants to near full solid solubility while keeping junction depths on the order of 10 nm. The trade-off is that millisecond processes require specialized tools (for uniform laser or lamp illumination) and precise control to avoid thermomechanical stress or wafer damage from the rapid heating.

Today, an annealing step (or a series of anneals) is carefully integrated into the fabrication flow after implants and some deposition steps. Typical modern processes might use a combination of anneals: a quick sub-millisecond flash anneal for ultra-shallow junction activation, followed by a slightly longer “medium” anneal (on the order of seconds) to remove any residual defects, and possibly a low-temperature furnace anneal for strain relaxation or other purposes. Such multistage annealing

balances the need for maximal activation with minimal diffusion. Overall, advanced annealing techniques are indispensable for fabricating the shallow, abrupt doping profiles in today's CMOS devices. Continued innovations in annealing (e.g. microwave annealing, pulsed laser anneals) are being explored to further improve dopant activation and reduce thermal budgets.[37, 38]

From a modeling perspective, annealing is challenging to simulate because it involves multiple kinetic processes: defect recombination, dopant diffusion, clustering, and interactions of defects with dopants (e.g. transient enhanced diffusion due to implant damage). Traditional continuum process simulators use fitted diffusion equations with parameters that attempt to capture these phenomena. However, as discussed later, atomistic simulation methods (MD and DFT) are increasingly employed to provide more fundamental insight into defect and diffusion behavior during annealing, helping to improve and calibrate continuum models. In summary, annealing is the thermal "repair and activate" step that ties together the implantation and diffusion engineering in semiconductor fabrication.

1.5 Deposition Techniques

In addition to patterning and doping, chip fabrication requires numerous deposition steps to add new material layers (conductors, semiconductors, or insulators) onto the wafer. Thin-film deposition processes create the various layers that make up transistors (gate oxide, gate electrode, etc.), interconnect wiring (metal layers and vias), and passivation or protective coatings. Deposited films must meet stringent requirements for thickness uniformity, step coverage over topography, composition, purity, and electrical properties. Several deposition techniques are commonly used in semiconductor manufacturing, each with its own advantages.

First is the Chemical Vapor Deposition (CVD). CVD uses reactive gases introduced into a reactor chamber that, when energized (by heat, plasma, or other means),

undergo chemical reactions at the wafer surface to form a solid film.[39] For example, to deposit silicon dioxide (SiO_2), a typical CVD process might flow silane (SiH_4) and oxygen at high temperature, which react to form SiO_2 on the wafer and gaseous byproducts. CVD is essentially a chemical growth process – materials "grow" on surfaces via surface reactions of precursor gases. This method excels at conformality (covering complex 3D structures evenly) and can achieve high deposition rates.[40] Variants of CVD include low-pressure CVD (LPCVD), plasma-enhanced CVD (PECVD), and others, tuned for different film types and temperatures. A downside of CVD is that it can incorporate impurities or produce byproducts that are hard to fully remove.[41] Nonetheless, CVD is widely used for depositing dielectrics (SiO_2, Si_3N_4), polysilicon, and even metals like tungsten in contact holes.

Another deposition method is Physical Vapor Deposition (PVD). PVD, in contrast, is a physical process that does not rely on chemical reactions to form the film. The most common form of PVD in chip-making is sputtering.[42] In a sputter deposition system, a target of the desired film material (e.g. aluminum or copper) is bombarded by energetic ions (usually argon plasma). Atoms ejected ("sputtered") from the target travel through a vacuum and deposit on the wafer, coating it with a thin film.[43] PVD is essentially line-of-sight deposition: material is vaporized and then condenses on the substrate. It generally yields high-purity films (since no chemical byproducts are involved) and is good for depositing metals and some dielectrics.[44] However, PVD films may have poor step coverage in high-aspect-ratio features (because vaporized atoms travel in straight lines). Still, PVD is heavily used for metal interconnect layers (aluminum, copper barrier/seed layers, etc.) and for some insulators. Evaporation is another PVD method (thermally evaporating material), though less common in modern fabs compared to sputtering.

The last one is Atomic Layer Deposition (ALD). ALD is a special variant of CVD that deposits films one molecular layer at a time by self-limiting surface reactions.[45] In ALD, precursor gases are introduced sequentially in pulses. For instance, to grow

HfO_2, a metal precursor (hafnium chloride, $HfCl_4$) is pulsed into the chamber and reacts with the wafer surface, forming at most one monolayer of hafnium atoms attached (and leaving some surface Cl).[46] Excess precursor is purged, then a second reactant (e.g. H_2O) is pulsed in, which reacts with the adsorbed layer to form HfO_2 and release HCl byproduct. This completes one ALD cycle, depositing ~1 atomic layer. By repeating the cycles, a film of precise thickness can be built up layer-by-layer.[47] ALD's strengths are unparalleled thickness control (Angstrom-level) and excellent conformity even in deep, narrow features – each cycle deposits a uniform layer no matter the topology.[48] It is ideal for high-κ gate dielectrics, spacer layers, or any application requiring ultra-thin, pinhole-free films over complex structures. The trade-off is that ALD is relatively slow due to its sequential nature.[49] Thus, ALD is used selectively for critical thin films where its precision is needed, while faster methods like CVD handle bulk film deposition.

Overall, deposition processes provide the material building blocks (silicon, oxides, nitrides, metals) for device structures. A modern integrated circuit may have dozens of deposited films, from angstrom-thin atomic layers to micrometer-thick dielectric stacks. The choice of deposition technique depends on the material and requirements: for example, a thick intermetal dielectric might use high-density plasma CVD for speed, whereas a nanometer-thin high-κ gate oxide would use ALD for accuracy.

On the other hand, deposition steps are interwoven with lithography and etch steps. Often, a film is deposited over the entire wafer and then patterned (using lithography and etching) to remain only in desired areas. For instance, a blanket metal film might be deposited by PVD and then etched away except where interconnected wires are needed. In other cases, deposition fills an etched trench or via (e.g. CVD of dielectric into an isolation trench). The ability to precisely simulate deposition processes – predicting film conformality, thickness uniformity, stress, etc. – is valuable for process development. While continuum models (like fluid dynamics and surface reaction kinetics) are used for CVD reactor design, atomistic modeling can help understand

film microstructure or interface formation. However, deposition modeling often involves length scales (feature-scale to reactor-scale) that are beyond straightforward molecular simulation, so multi-scale approaches or empirical models are common.

As features continue to shrink and aspect ratios increase (e.g. contacts in 3D NAND or through-silicon vias), deposition techniques like ALD have grown in importance.[50] New materials such as metal gate electrodes and phase-change memory compounds have also expanded the use of various deposition methods. From a simulation standpoint, predicting how a new material will deposit and integrate is a significant challenge, often requiring a combination of first-principles calculations (to understand surface reactions), molecular modeling (for film growth mechanisms), and experimental calibration.

1.6 Molecular Dynamics Simulations and LAMMPS

Given the complexity of semiconductor fabrication, simulation and modeling have become indispensable tools to understand processes at a fundamental level and to optimize them without excessive trial-and-error experimentation. One important class of simulation techniques is molecular dynamics (MD), which models the physical movements of atoms and molecules over time. In an MD simulation, a system of atoms is advanced step-by-step by numerically solving Newton's equations of motion, with interatomic forces computed from a chosen potential (force field). By tracking all atomic trajectories, MD can provide a detailed, atomistic view of phenomena such as collision cascades, chemical reactions, or diffusion events in materials.

In the context of semiconductor processing, MD is particularly valuable for studying processes that involve atomic-scale interactions and damage creation – for example, ion implantation damage, defect formation during annealing, or thin-film growth at the atomic level.[51] Unlike continuum process simulators, MD makes no continuum assumption: it treats matter as discrete atoms, which is essential for capturing

phenomena like channeling of implanted ions along crystal axes or the formation of defect clusters.[52] Classical MD (using empirical interatomic potentials) can simulate systems of millions of atoms, reaching spatial scales of tens of nanometers and timescales up to nanoseconds or microseconds, depending on the available computing power. While this is still far smaller and faster than a full device or process scale, MD can zoom into the critical early moments of a process (like the first picoseconds of an ion implantation event) with high fidelity.

A widely used MD engine in materials simulation is LAMMPS (Large-scale Atomic/Molecular Massively Parallel Simulator).[53] LAMMPS, developed at Sandia National Laboratories, is an open-source, high-performance MD code designed to run efficiently on parallel supercomputers.[54] It supports a broad range of interatomic potentials for different materials – metals, semiconductors, polymers – and even coarse-grained or mesoscale potentials.[54] Because of its parallel spatial-decomposition algorithms and MPI (Message Passing Interface) implementation, LAMMPS can handle simulations partitioned across many processors, enabling simulation of large atomistic systems (millions of atoms) or long simulation times, as far as is feasible. LAMMPS has been widely adopted in the semiconductor research community for tasks such as modeling silicon lattice dynamics, simulating ion bombardment effects, and exploring thin-film deposition physics. Its flexibility allows users to implement custom potential or integrate with other methods (for example, coupling MD with a continuum finite element solver for multi-scale modeling).

Despite its power, classical MD does face limitations that motivate the use of complementary methods. One key limitation is the timescale: simulating beyond a few nanoseconds of physical time is often impractical because each femtosecond-scale time step requires force calculations for every atom.[55] Many semiconductor processes (like dopant diffusion during annealing) occur over milliseconds or seconds – far out of reach for brute-force MD. Another limitation is size: even a million-atom simulation corresponds to a cube of material only in the order of tens of

nanometers across, whereas device features and pattern dimensions are in the micrometer range or larger. As a result, MD alone cannot directly simulate an entire semiconductor process or device; it can only simulate a tiny representative volume for a brief moment. Moreover, the accuracy of MD hinges on the quality of the interatomic potential used. Empirical potentials (e.g. Tersoff or Stillinger–Weber for Si) are fitted to limited data and may not capture every aspect of defect energetics or chemical reactions, especially when new elements or complex bonding states (as in doping or interfaces) are involved.[56, 57]

In practice, MD is often used in tandem with higher-level models. For example, MD simulations of energetic ion impacts can predict the immediate damage structure (vacancies, interstitials, displacements).[58] These atomistic configurations can then be handed off to kinetic Monte Carlo (KMC) or cluster dynamics simulations that evolve the defects over longer times to emulate annealing. This multi-scale modeling leverages MD for what it does best (capturing fast atomic collision dynamics and defect formation) and then uses more coarse-grained stochastic methods to simulate the slower diffusion and defect interactions that occur over milliseconds or seconds. An example of this is the simulation of ultra-shallow junction formation: MD might simulate a hundred boron ions striking a silicon substrate (each over a few picoseconds), generating an initial damage and dopant distribution;[59] then a KMC simulation takes over to model defect recombination and dopant diffusion during the subsequent anneal, over microseconds to milliseconds.

It is also common to integrate MD with first-principles calculations to improve the realism of the simulations.[60, 61] For instance, density functional theory can be used to calculate the formation energies or migration barriers of specific defects, which can then calibrate the parameters in an MD force field or in a continuum diffusion model. In fact, DFT-informed MD is a powerful approach: one can derive or refine interatomic potentials based on DFT data for the interactions of interest (such as a dopant atom with a silicon lattice). In the present context of semiconductor process

modeling, such an approach was taken to develop a more accurate B–Si interaction potential for MD simulations of boron implantation and annealing. By fitting a classical potential to match DFT energies of various B–Si configurations, the MD simulations can more faithfully reproduce defect formation and dopant clustering behavior observed in experiments.

Finally, MD outputs can feed directly into continuum Technology CAD (TCAD) tools. For example, MD might reveal that a certain fraction of implanted dopant atoms forms immobile clusters, or that a certain defect anneals out with a particular activation energy. These insights can be translated into improved continuum models – e.g. a defect cluster "container" model or an adjusted diffusion coefficient in TCAD – thereby enhancing the predictive accuracy of process simulators. The bottom line is that molecular dynamics provides the microscopic, physics-based view of semiconductor processes, which is essential for understanding fundamental limits and mechanisms, and it works best when linked with coarse-grained models to cover the full span of length and time scales. LAMMPS, with its performance and versatility, has been a crucial tool in carrying out such large-scale atomistic simulations in semiconductor process research.

1.7 Coarse-Grained Molecular Dynamics (CGMD)

While atomic-scale MD is a powerful technique, its computational expense motivates strategies to extend simulations to larger scales. Coarse-grained molecular dynamics (CGMD) is one such strategy, in which groups of atoms are treated as a single pseudo-particle (bead), and effective interaction potentials are used between these coarse-grained beads.[62, 63] By reducing the total number of particles and smoothing out high-frequency degrees of freedom, CGMD can simulate systems that are larger in size or longer in time than all-atom MD can handle, albeit at the cost of losing atomic detail.[64] Coarse-graining is especially useful for materials like polymers and

biological macromolecules, where one can often represent a cluster of atoms (e.g. a monomer unit) as a single bead without losing the essence of the large-scale behavior.

In semiconductor manufacturing, an important application of CGMD is in modeling self-assembling materials and other mesoscale phenomena. A prime example is the directed self-assembly of block copolymers (as mentioned in the lithography section). All-atom MD of long polymer chains forming domains would be prohibitively slow and unnecessary – the interesting behavior is the phase separation and morphology on the tens-of-nanometers scale, not the vibration of every bond. With CGMD, each polymer block might be represented by a handful of beads interacting via a tunable potential that captures the thermodynamic incompatibility between different blocks. Researchers have developed coarse-grained models for di-block copolymers that reproduce their ability to form lamellae or cylinder patterns of around 10–20 nm half-pitch.[65] Using CGMD, they can simulate microphase separation and defect dynamics in block copolymer films under various conditions, which provides insight into how to guide the self-assembly to desired patterns for lithography.

More broadly, CGMD serves as a bridge between atomistic simulations and continuum models. It allows one to incorporate some chemical specificity and molecular structure (unlike a purely continuum or phase-field model) while greatly expanding the accessible length scale. For instance, CGMD can model ~100 nm scale chunks of material or simulate microseconds of dynamics, which might encompass, say, the aggregation of point defects into a dislocation loop during annealing, which is difficult for all-atom MD. In CGMD, the form of the coarse interactions can be derived from finer-level simulations or experiments (a process known as force-field coarse-graining or mapping). There are even hierarchical approaches where one first uses MD or DFT to parametrize a coarse-grained model, and then uses that model to explore larger system behavior.

One important consideration is that coarse-graining often averages out fast processes, so it may miss some atomistic mechanisms.[66] For example, a coarse model of silicon might not capture a rare diffusion pathway that an atomistic model would. Therefore, CGMD is usually used for phenomena where the fine details are less critical than the collective behavior (like the morphology of a polymer blend or the elastic response of a material). In semiconductor process modeling, areas where CGMD can be particularly useful, including modeling stress evolution in thin films (treating regions of crystal as mesoscale elements), simulating large-scale defect clustering, or exploring the flow of resist polymers in nanoimprint lithography, to name a few.[67, 68]

Several specialized coarse-grained methods exist as well – e.g. dissipative particle dynamics (DPD), which adds stochastic and dissipative forces to mimic solvent interactions, or Monte Carlo lattice models for phase separation. These can be seen as cousins of CGMD, targeting specific types of problems.[69, 70]

It's worth noting that LAMMPS and similar MD packages are capable of running coarse-grained models just as well as all-atom models. LAMMPS, for instance, provides potentials for bead-spring polymer models, DPD, and other coarse-grained techniques. This flexibility enables researchers to stay within one simulation framework while moving up and down the scale as needed. For example, one might simulate a small region of a silicon crystal with full atomistic MD to parameterize defect energetics, then embed that knowledge into a coarse-grained model that treats groups of atoms as single units to simulate defect dynamics in a larger region over longer times.

In summary, coarse-grained MD extends the reach of molecular simulation into regimes that are closer to device-scale. By sacrificing atomic-resolution detail, one gains the ability to model mesoscale structure formation and long-time kinetics that are otherwise intractable. In the multi-scale toolkit for semiconductor process

modeling, CGMD fills the important middle ground between atomistic MD (nanometers, nanoseconds) and continuum TCAD (millimeters, seconds), often providing the link that connects fundamental materials behavior to practical device-level outcomes.

1.8 Density Functional Theory (DFT)

While classical MD and CGMD rely on empirical or effective potentials, density functional theory (DFT) is a first-principles quantum mechanical method that offers a more fundamental – albeit computationally intensive – view of materials.[71] DFT calculates the electronic structure of a system by solving quantum-mechanical equations for electrons under the approximation that properties of the many-electron system can be determined from an electron density functional.[71] In simpler terms, DFT allows one to compute the total energy, charge density distribution, and related properties of a collection of atoms from the basic principles of quantum physics, without requiring fitted interatomic potentials. It is one of the most popular and versatile methods in computational physics and chemistry for studying molecules and solids.

In semiconductor manufacturing research, DFT plays a crucial role in elucidating material properties and reaction mechanisms at the atomic scale. For instance, DFT can be used in four different topics.

First is “Calculate Defect and Dopant Energetics”. DFT can determine the formation energy of point defects (vacancies, interstitials) or defect complexes in semiconductors, as well as the binding energies of dopant-defect clusters. These quantities are essential for understanding phenomena like transient enhanced diffusion (TED) and dopant activation.[72] For example, DFT calculations can reveal how a boron atom pairing with a silicon interstitial (forming a B–I cluster) becomes energetically favorable, which in turn helps explain the TED of boron in silicon.[73] Similarly, DFT can

predict which lattice sites are energetically preferred by a dopant (substitutional vs interstitial) and how that changes with Fermi level or charge state.

Second is “Compute Diffusion Barriers”. The migration of dopants or defects is governed by activation barriers – the energy required for an atom or defect to move from one site to another. DFT, often combined with techniques like the nudged elastic band (NEB) method, can calculate these migration energy barriers.[74] For instance, for a given dopant in silicon, DFT might show that the interstitial diffusion pathway has a lower barrier than the vacancy mechanism, quantifying values that can be plugged into diffusion models.[75, 76] Knowing accurate diffusion barriers is key to predicting how dopants will redistribute during anneals.

Third is “Investigate Surface Reactions and Materials for Deposition”. Many depositions and etch processes hinge on surface chemical reactions. DFT allows modeling of reaction pathways on semiconductor surfaces.[77] For example, the adsorption and dissociation of a CVD precursor on a silicon surface, or the reaction of etchant radicals with a silicon or oxide surface. These studies can identify rate-limiting steps or explain the selectivity of processes. In atomic layer deposition, DFT might be used to design precursor molecules by computing how completely a precursor can react in one cycle and how much activation energy is needed for removal of ligands.[78]

The last is “Explore New Materials and Phases”. The introduction of new materials (high-κ dielectrics, metal gates, ferroelectrics, 2D materials, etc.) in semiconductor devices often requires knowledge of their structural and electronic properties.[79] DFT can predict lattice constants, band structures, band gaps (with some limitations), dielectric constants, and interface properties of novel materials before they are even synthesized.[80, 81] This guides experimental efforts by narrowing down candidates. For example, for a new high-κ gate dielectric, DFT might evaluate a variety of oxides

or multilayer structures and identify which have desirable high permittivity and band alignment with silicon.

One of DFT's biggest strengths is accuracy at the atomic scale. DFT simulations typically involve systems of up to a few hundred atoms (due to steep computational cost scaling with system size), which is sufficient to model local structures like a defect in a crystal or a surface patch.[82] The results, including formation energies, barrier heights, charge distributions, feed directly into higher-level models. For instance, DFT-informed process simulation is now a common paradigm: a DFT study might compute the activation energy for a dopant diffusing via a vacancy mechanism, and that value is then used in continuum diffusion simulations to replace a previously fitted parameter. This improves the physical soundness of device simulations, especially as devices shrink and old empirical models become less reliable.

Moreover, DFT often acts as the foundation for developing better interatomic potentials for MD.[83, 84] Classical potentials have parameters that can be tuned to reproduce DFT energy surfaces. For example, if one is simulating SiC and needs a new potential that handles implanted aluminum defects, one can perform a series of DFT calculations on small SiC supercells with Al in various configurations (substitutional, interstitial, etc.). Those data points can then be used to fit or validate a modified potential for Al–Si–C interactions in an MD simulation.

Despite being powerful, DFT has its own limitations. Standard DFT (using common exchange-correlation functionals) sometimes underestimates semiconductor band gaps and can struggle with strongly correlated electrons or rare events (like exact defect levels in band gaps).[85] It also cannot directly simulate large systems or long times – it's essentially a zero-Kelvin, ground-state calculation for a snapshot.[86] However, there are extensions like *ab initio* molecular dynamics (where DFT computes forces on the fly for a small system over a short time) and time-dependent DFT (for excited states), which extend its reach modestly. Generally, though, DFT in process modeling

is used to get static properties and activation energies that inform bigger-picture models.

As for the multiscale integration part, the ultimate power of DFT, MD, and CGMD (or continuum) is realized when they are used together in a multiscale workflow. A noteworthy recent example involved the simulation of Al implant damage in 4H-SiC power devices: researchers combined MD to model the ion impacts, DFT to calculate the electronic trap states of the resulting defects, and a tight-binding transport simulation to assess how those defects degrade MOSFET performance.[87] This kind of end-to-end simulation – from atomistics to electrical characteristics – underscores the motivation for using all these techniques in concert. DFT supplies the "first principles" data, MD captures the real-time atomistic evolution, and coarse-grained or device-level models project the implications to device behavior.

In summary, DFT is the fundamental tool that anchors the simulation hierarchy by providing quantitative insights into atomic-level processes in semiconductors. It complements MD and CGMD by addressing what they cannot: electronic structure, accurate energetics, and quantum effects. Together, these methods help researchers tackle the grand challenge of predictive process simulation – the ability to virtually experiment with new process recipes or materials and foresee their impact on the final device. The continued advancement of simulation algorithms and computational power is steadily bringing this vision closer to reality, enabling more efficient and cost-effective development in semiconductor manufacturing.

1.9 Conclusion

The above sections have outlined the key processes in semiconductor fabrication and the simulation techniques employed to model them. Semiconductor manufacturing involves a complex interplay of physical and chemical steps – from lithography and doping to annealing and deposition – all of which must be optimized to create

nanostructures with atomic precision. Capturing this complexity in models requires a multiscale approach. Atomistic simulations (MD and DFT) provide deep insight into phenomena like ion-induced damage, defect dynamics, and surface reactions, uncovering physics on the scale of angstroms and femtoseconds. Coarse-grained modeling extends the simulation reach to mesoscopic scales, allowing one to study polymer self-assembly or microstructure evolution over larger domains and longer times. These detailed simulations can then inform or be integrated with continuum process and device simulations, which operate at the scale of the whole chip.

The motivation for using advanced modeling in semiconductor processing is clear – it offers a window into the sub-microscopic world where intuition and experimental characterization alone struggle. For example, understanding why a certain annealing schedule yields better activation, or how a new dopant interacts with point defects, or whether a novel patterning technique will reliably produce uniform features, are questions that simulations can help answer without costly wafer runs. Each method (MD, CGMD, DFT) comes with challenges: whether it be the trade-off between accuracy and scale, the need for reliable potentials, or the heavy computational demands. Yet, each contributes essential capabilities to the overall modeling toolkit.

In an era where further improvements in semiconductor technology are increasingly difficult and expensive, predictive simulation has become indispensable. By employing MD, CGMD, and DFT in complementary roles, researchers and engineers can explore the process parameter space more efficiently, troubleshoot problems at the atomic level, and even discover new process strategies (like new materials or annealing methods) before implementing them in the fab. The following chapters of this dissertation will leverage this simulation-driven approach. Building on the background provided here, we will delve into specific case studies of semiconductor process modeling – illustrating how the combination of molecular dynamics, coarse-grained modeling, and first-principles calculations can be applied to contemporary

challenges in semiconductor manufacturing, and how these methods together advance our ability to design processes for the next generation of nanoelectronics.

CHAPTER 2

Simulation of Directed Self-Assembly in Block Copolymers using LAMMPS: A Study on PS-co-PMMA and Pinned Coated Brush Polymers

2.1 Introduction

2.1.1 Photolithography process for the semiconductor field

Photolithography is a fundamental process in the semiconductor industry, serving as a key technology for defining the intricate patterns that form the transistors, interconnects, and other critical structures on silicon wafers.[88, 89] The process involves the use of light to transfer a circuit pattern from a photomask onto a light-sensitive material known as photoresist, which has been applied to the surface of the wafer. After exposure to light, the exposed or unexposed areas of the photoresist are developed, depending on whether a positive or negative photoresist is used, creating a precise pattern that will guide subsequent etching or deposition steps.

As semiconductor technology has advanced, the demand for smaller and more complex devices has pushed the limits of traditional photolithography. Feature sizes have continued to shrink, following Moore's Law, leading to an increased need for high-resolution patterning techniques. To address this, photolithography equipment has evolved to incorporate advanced technologies such as Deep Ultraviolet (DUV) and, more recently, Extreme Ultraviolet (EUV) lithography, which uses shorter wavelengths of light to achieve finer resolution. [90, 91]

EUV lithography, in particular, represents a significant leap in photolithography capabilities, allowing the industry to create features as small as 7 nm and beyond.[92] However, this leap comes with a substantial increase in cost. EUV systems are

incredibly complex, requiring highly specialized components like ultra-clean environments, advanced optics, and precision-controlled light sources. The cost of a single EUV lithography machine can exceed $150 million, with additional expenses for maintenance, operation, and necessary infrastructure upgrades. The total investment required for EUV integration into a manufacturing facility can easily reach billions of dollars, which poses a significant challenge even for the largest semiconductor companies.

Given these financial barriers, the semiconductor industry is actively exploring alternative and complementary patterning techniques that can reduce reliance on such costly photolithography equipment. One promising solution is Directed Self-Assembly (DSA) using Block Copolymers (BCPs). The key advantage of DSA BCP is its cost-effectiveness compared to traditional photolithography. While photolithography requires expensive equipment to achieve the necessary resolution, DSA allows for pattern refinement at the molecular level without relying on advanced optical systems. Instead, it uses relatively low-cost materials and simpler processing steps to achieve high-resolution patterns. DSA BCP can either be used in conjunction with photolithography, as a way to "fine-tune" patterns created through conventional means, or as a replacement for certain steps, significantly reducing the overall cost of the patterning process.

In summary, while photolithography remains an essential technology for semiconductor manufacturing, the increasing costs of cutting-edge photolithography equipment—particularly for EUV—have prompted the industry to seek alternatives like DSA BCP. This approach not only offers a more cost-effective solution but also opens up new possibilities for advanced patterning, helping the industry to continue advancing while managing the high financial barriers posed by state-of-the-art lithography systems.

2.1.2 Self-assembly block copolymers

As devices shrink, traditional photolithography approaches its physical and economic limits, prompting the exploration of alternative techniques. DSA BCPs offers a promising solution, potentially surpassing the resolution limits of traditional methods while significantly reducing cost and complexity.[93]

Block copolymers, such as PS-co-PMMA (Polystyrene-b-Polymethylmethacrylate), capitalize on their ability to self-organize into ordered nanostructures, enabling the fabrication of patterns at resolutions difficult to achieve through other means. These copolymers inherently phase separate due to the chemical dissimilarity of their blocks, a process driven by thermodynamics. This self-organization is influenced by the molecular weight, volume fraction of each block, and the Flory-Huggins parameters.[94]

When external fields or patterned substrates are introduced, BCPs can be steered to assemble into complex, ordered structures. The surface energy of the substrate can selectively attract different blocks, influencing the copolymers to form diverse structures like hexagonally packed cylinders (contact hole structures), gyroids, and lamellae.[95]

Advancements in substrate design have further refined DSA capabilities. One of the promising methods is chemo-epitaxy, which creates chemically distinct regions on the substrate to direct the copolymer assembly into desired configurations, crucial for controlling the orientation and periodicity of the domains.[96, 97] Conversely, graphoepitaxy uses substrate features such as grooves or posts to guide the copolymer assembly, enhancing the alignment and order of the nanostructures and facilitating their integration into traditional lithographic workflows.[98, 99]

Thus, DSA of block copolymers emerges as a highly efficient nanolithography strategy, combining bottom-up assembly with top-down patterning techniques. By designing

substrate templates and controlling processing conditions, such as solvent annealing or thermal treatments, researchers can harness the inherent properties of BCPs to fabricate nanoscale features with precise shapes and orientations, essential for the next generation of electronic devices.

2.1.3 Brush polymer guided substrate for chemo-epitaxy

This work investigates the use of brush polymers coated on a substrate as a method for chemo-epitaxy. Three key factors—brush polymer length, brush domain dimensions, and polymer density—are examined to optimize the morphology of Directed Self-Assembly (DSA) block copolymer (BCP) patterns. The focus of this study is on contact hole structures, specifically hexagonal cylinders, aiming to enhance pattern resolution and complexity through chemical patterning and polymer design.

To explore the formation of various nanostructures, the composition of BCPs and polymer chain modifications were systematically simulated. The study then assessed the impact of tuning brush polymer parameters on the resulting patterns. While the effects of brush polymers have been widely studied, these simulations seek to refine our understanding of how subtle variations in brush composition and dimensions influence microdomain morphology in DSA applications. The resulting patterns act as templates that guide the self-assembly of BCPs into desired structures, such as contact holes. The introduction of brush copolymers offers potential improvements in controlling the assembly process, potentially overcoming limitations of traditional chemical patterning techniques.

This research also examines how the density and molecular length of brush copolymers affect their ability to guide BCP assembly. Simulations of variations in brush density and length aim to identify optimal conditions for achieving precise and reproducible patterns. These findings are critical for designing substrates that both

effectively guide BCP assembly and remain compatible with existing manufacturing processes.

A preliminary literature review suggests that the application of brush copolymers for chemical patterning in DSA has not been extensively explored, presenting an opportunity for significant contributions to the field. This research could provide valuable insights into the scalable use of brush copolymers in nanolithography, particularly in enhancing the manufacturability and resolution of DSA patterns.

2.1.4 Simulation methods

In this study, we utilize the Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS) in conjunction with Coarse-Grained Molecular Dynamics (CGMD) and Dissipative Particle Dynamics (DPD) to simulate the self-assembly of block copolymers (BCP) for Directed Self-Assembly (DSA) applications. While LAMMPS is a powerful and versatile tool for large-scale molecular dynamics simulations[53, 100], CGMD and DPD are key methodologies that enable us to effectively model the mesoscale behavior of polymer systems.

Coarse-Grained Molecular Dynamics (CGMD) is employed to simplify the system by reducing the degrees of freedom, enabling the simulation of large systems while maintaining essential structural characteristics.[101-103] By grouping several atoms into larger coarse-grained beads, CGMD allows for the study of long-range interactions and large-scale molecular movements, which are critical in understanding the phase separation and self-assembly processes of BCPs. This method is especially useful in DSA studies, where the balance between computational efficiency and accurate representation of molecular interactions is crucial.

Dissipative Particle Dynamics (DPD) is another technique that we incorporate to capture the hydrodynamic behavior of the system. DPD is particularly well-suited for

simulating soft matter systems, such as polymers, as it introduces a dissipative force that mimics the effects of thermal fluctuations and fluid dynamics at the mesoscale.[104-106] This allows for a more realistic representation of the molecular self-assembly process in BCPs, where solvent effects and dissipative interactions play a significant role. By using DPD, we can model the dynamic evolution of BCP morphologies under various conditions, such as different brush polymer densities and substrate patterns.

In the context of DSA, these simulation methods are used to model the formation of ordered nanostructures on chemically or topographically patterned substrates. By carefully defining the interaction parameters between polymer blocks and the substrate, we simulate the phase separation that leads to well-ordered patterns such as cylinders, lamellae, or spheres. Specifically, the study focuses on optimizing the contact hole pattern formation by investigating the impact of brush polymer characteristics, including pinned domain dimensions, brush density, and brush length.

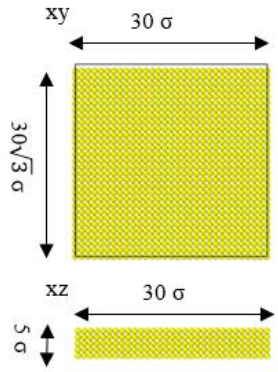
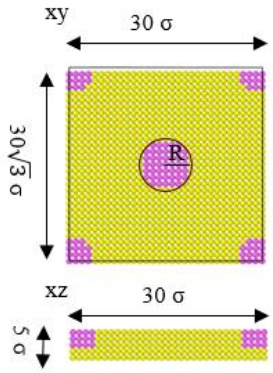
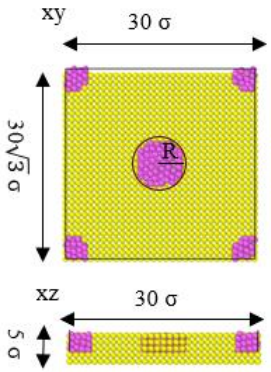
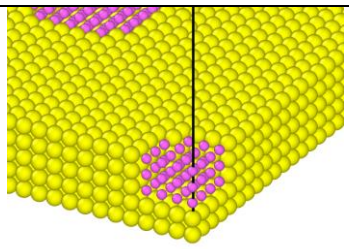
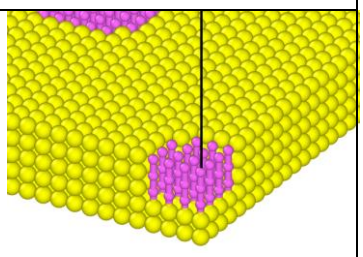
By combining LAMMPS with CGMD and DPD, we aim to gain deeper insights into the molecular mechanisms driving DSA in BCP systems. This approach provides a more comprehensive understanding of how different variables influence the final pattern fidelity and feature size, ultimately contributing to the optimization of DSA processes for next-generation semiconductor manufacturing.

2.2 Methodology

2.2.1 Model overview

In this study, the model is developed according to previous work.[107-109] Three types of substrates are constructed: pure substrate, flat pinned substrate, and brush pinned substrate, to investigate the effects of chemo-epitaxy. The dimensions of each model are outlined in Table 1. The non-pinned region (represented by yellow beads) acts as a neutral substrate, showing no selectivity toward either PS or PMMA. Meanwhile, the pinned domain (shown as pink beads) exhibits PS-affinity interactions, functioning as the chemo-epitaxy mechanism.

Table 1. CGMD simulation model design of non-pinned substrate, flat pinned and brush pinned.

	Non-pinned substrate	Flat pinned	Brush pinned
Model structure			
Pinned pattern	N/A		

2.2.2 Simulation system parameters

The block copolymer under investigation is an A-B type di-block copolymer, specifically polystyrene-block-polymethylmethacrylate (PS-b-PMMA). A coarse-grained modeling approach is employed to reduce the degrees of freedom in the system, which simplifies the simulation while maintaining a reasonable representation of the macroscopic properties. This method allows us to explore larger length scales without fully capturing all the microscopic structural details.

The bead-spring model is used in conjunction with Kuhn segments to represent the polymer chains, approximating them as generalized Lennard-Jones particles. In this model, one monomer unit (σ) corresponds to a size of 1 nm, which is approximately the Kuhn length of styrene. This coarse-grained bead represents around 4 styrene molecules. Similarly, one coarse-grained bead of polymethyl methacrylate (PMMA) is equivalent to approximately 4.5 molecules of methyl methacrylate. This approach helps strike a balance between computational efficiency and structural accuracy in simulating the self-assembly behavior of block copolymers.

In a polymer chain, the length varies from 10 beads to 160 beads with a specific composition. For instance, when L=100 σ and PS: PMMA = 70 : 30, the polymer chain consists of 100 beads, with 70 PS beads and 30 PMMA beads. The interaction between bonded BCP (block copolymer) beads is modeled using the FENE (Finite Extensible Nonlinear Elastic) bond potential, as shown in Table 2. The spring constant K for the FENE bond is $30\varepsilon\sigma^{-2}$, where ε is the energy parameter and σ represents the bead diameter. The maximum bond extensibility is set to 1.5σ. For long-range interactions, the Lennard-Jones (LJ) potential with a tail correction is applied, while the Weeks-Chandler-Andersen (WCA) potential is used to control repulsive interactions between non-bonded beads.

Table 2. Fene bond and Lennard Jones potential used in the simulation system.

Name	Equation
Fene bond	$U_{fene}(r) = -0.5KR_{max}{}^2 \ln\left[1 - (\frac{r}{R_{max}})^2\right]$

Lennard Jones interaction-1: attractive force	$U_{attractive}(r) = 4\varepsilon[(\sigma/r)^{12} - (\sigma/r)^{6}] + S_{LJ}$ for r < 2.5 σ
Lennard Jones interaction-2: repulsive force	$U_{repulsive}(r) = 4\varepsilon[(\sigma/r)^{12} - (\sigma/r)^{6}] + \varepsilon$ for r < 2.5 σ

The density of the BCP site is 0.85 beads per nm^3 is maintained and the Nosé–Hoover is for thermostat. The interaction of Lennard Jones parameters is selected according to previous works.[107-109] The optimized parameters ($\epsilon_{PS-PS,attractive} = 0.15$, $\epsilon_{PMMA-PMMA,attractive} = 0.15$ and $\epsilon_{PS-PMMA,replusive} = 0.15$) are used in the main simulations.

On the other hand, Dissipative Particle Dynamics (DPD) has proven to be a powerful method for simulating soft matter systems due to its ability to bridge multiple scales, offering an efficient mesoscopic approach that captures both the microscopic details of molecular dynamics (MD) and the macroscopic behaviors of complex fluids, which is introduced by Hoogerbrugge and Koelman.[110, 111] The inherent structure of DPD, which employs coarse-grained particles representing clusters of atoms or molecules, makes it particularly suitable for handling large-scale simulations that are computationally prohibitive for classical MD.

One key advantage of DPD is its capability to model hydrodynamic interactions effectively while maintaining computational efficiency. As demonstrated in studies such as those by Ma et al., DPD was used to investigate the mesoscale structures and proton conduction properties in polymer membranes, showing how the method can model both the molecular structure and transport properties in soft materials.[112] Additionally, Flekkøy and colleagues emphasize the versatility of DPD, particularly in cases where multiple length scales coexist, such as in the simulation of complex fluids and soft matter. [113] This versatility is crucial for accurately simulating the dynamic behavior of soft matter systems, where interactions and structural evolution occur over a wide range of spatial and temporal scales.

When applying a DPD thermostat, the interaction between two beads is defined by the non-conservative component of the DPD force field. The total force exerted on bead *i* by bead *j* is the sum of the following individual force terms.

Table 3. Dissipative particle dynamics function used as the thermostat

Name	Equation
Dissipative particle dynamics	$\vec{f} = (F^D + F^R)\vec{r}_{ij} \quad r < r_c$
Dissipative force	$F^D = -\gamma\omega^2(r)(\vec{r}_{ij} \cdot \vec{v}_{ij})$
Random force	$F^R = s\omega(r)\alpha(\Delta t)^{-\frac{1}{2}}$
Weighing function	$w(r) = 1 - \frac{r}{r_c}$
Scale factor	$s = \sqrt{2k_B T\gamma}$

In table 3, F_D represents the dissipative force, functioning as a heat source, while F_R is the random force, acting as a heat sink. The vector r_{ij} denotes the unit vector between beads *i* and *j*, and v_{ij} is the relative velocity between them. The temperature parameter is T, and k_B is the Boltzmann constant. The random number α, drawn from a Gaussian distribution with a mean of zero and variance $\sigma^2=1$, introduces stochastic behavior. The time step for each iteration is Δt, and $\omega(r)$ is a weighting function, equal to 1 when $r \leq r_c$ (cutoff radius) and 0 otherwise.

2.2.3 Chemo-epitaxy with brush-coated substrates

Two distinct chemo-epitaxial templates were explored. In the first, an idealized "flat-pinned" substrate was constructed by embedding immobile, PS-affine beads at predefined circular sites; radius of $3, 4, 5, 6$, and $8\,\sigma$ were positioned either at the center or at the four corners of the simulation cell to impose a static chemical field that favors hexagonal cylinder packing. The second, more experimentally realistic template replaced these static pinned domains with polymer brushes. Each brush chain was

grafted to the otherwise neutral substrate at one end, leaving the free end mobile so that the layer could respond elastically to the surrounding melt. To emulate the imperfect coverage found in spin-coated mats, the graft density was varied from 25 % to 100 %, while the contour length of the brushes was tuned independently between 2 σ and 8 σ. Systematic sweeps of pinning-site radius, graft density, and brush length allowed us to map the parameter space and identify the combinations that most effectively promote the formation of highly ordered, hexagonally packed PS-*b*-PMMA cylinders.

2.2.4 Simulation details

The initial coarse-grained configuration was generated with an in-house Python script that places all beads—block-copolymer (BCP) chains and substrate layers—on a predefined lattice. After construction, the system was first equilibrated for at least 1×10^6 integration steps under a uniform, non-selective Lennard-Jones (LJ) potential applied to every bead pair.

To accelerate the calculation, interactions between the pillar beads and the underlying substrate beads were set to zero and the substrate beads were fixed in space, thereby eliminating unnecessary force evaluations while keeping a rigid template. Equilibration and production runs were carried out in the NVT ensemble (constant number of beads, fixed simulation box, and constant temperature) using a dissipative-particle-dynamics (DPD) thermostat to maintain the target temperature.

After the initial equilibration, chemically selective LJ parameters were activated to capture the thermodynamic driving force for microphase separation. Production trajectories were then propagated for a sufficiently long duration to ensure that the targeted morphology emerged and reached a steady state. All simulations employed a reduced time step of $\Delta t=0.005$. Molecular dynamics were performed with LAMMPS, and trajectory snapshots were analyzed and rendered with OVITO.

2.2.5 Analysis method

To obtain a quantitative, orientation-invariant measure of how closely the simulated block-copolymer (BCP) pillars approach an ideal hexagonal array, we evaluate the bond-orientational order parameters originally proposed by Steinhardt, Nelson and Ronchetti.[114] Because these parameters are derived from local spherical-harmonic projections, they have proven highly effective in distinguishing crystalline symmetries from amorphous backgrounds across a wide spectrum of soft-matter and polymeric systems.[115, 116]

The positions of the PMMA beads are analyzed with the expressions listed in Table 4. Perfect hexagonal packing in two dimensions exhibits six-fold rotational symmetry, so the harmonic index is fixed at $\ell = 6$ throughout, where $\ell = 6$ equals to $\psi 6$. Only PMMA beads (atom type 2)–which define the cylindrical domains of interest–are included; substrate-brush and PS beads (types 1 and 3–5) are excluded. The neighbor shell is delineated by the first minimum of the partial radial-distribution function, giving a cut-off radius $r_{cut} \approx 1.30\ \sigma$ and an average coordination number $N_{nn} \approx 6$, as expected for an ideal hexagonal lattice. This definition maximizes sensitivity to six-fold order while suppressing spurious long-range correlations. For ease of comparison, the resulting $\psi 6$ values are normalized to that obtained for a simulated ideal contact-hole lattice.

Table 4. the Steinhardt bond-orientational order parameters

Formula	Explanation
$\varphi_l(i) = \sqrt{\frac{4\pi}{2l+1}\sum_{m=-l}^{l} \lvert q_{lm}(i)\rvert^2}$	Scalar magnitude of the local ℓ-fold orientational order around bead i

$q_{lm}(i) = \frac{1}{N_b(i)} \sum_{j=1}^{N_b(i)} Y_{lm}(r_{ij})$	Complex spherical-harmonic projection of the bond vectors connecting bead *i* to its N_b (*i*) neighbors

Cylinder morphology was quantified by analyzing the cross-sectional geometry slice-by-slice along the pillar axis. Each cylinder was partitioned into horizontal slabs of thickness $\Delta z \approx 1\ \sigma$, and within every slab the in-plane bead coordinate (x_i, y_i) were referenced to the slice center of mass $(\bar{x}, \bar{y})$.Two complementary descriptors were then computed. First, the side-wall roughness was defined as the root-mean-square (RMS) lateral fluctuation, $R_{cylinder} = \sqrt{{\sigma_x}^2 + {\sigma_y}^2}$, where $\sigma_x = std(x_i)\ and\ \sigma_y = std(y_i)$; this metric is the three-dimensional analogue of the line-width and line-edge roughness figures widely used in semiconductor metrology. A three-sigma criterion applied to the distribution of $R_{cylinder}$ values identified cylinders whose roughness lay within the 99.7 % confidence envelope required for process qualification. Second, the mean cylinder size was captured by the RMS radius, $R_{RMS} = \sqrt{\langle r^2 \rangle}$, where the instantaneous radial distance of each bead from the slice center is $r_i = \sqrt{(x_i - \bar{x})^2 + (y_i - \bar{y})^2}$; this orientation-invariant quantity characterizes the average pillar diameter independently of local roughness. Together, these two metrics provide a quantitative picture of the in-plane roughness and the axial tapering behavior of the cylinders, allowing direct comparison across different simulation conditions.

Table 5. Formulas used to characterize cylinder roughness and radius

Metric	Expression
Cylinder roughness	$R_{cylinder} = \sqrt{{\sigma_x}^2 + {\sigma_y}^2}$
Cylinder RMS radius	$R_{RMS} = \sqrt{\langle r^2 \rangle}$, $r_i = \sqrt{(x_i - \bar{x})^2 + (y_i - \bar{y})^2}$

2.3 Results and Discussion

2.3.1 Self-assembly behavior of PS-b-PMMA

Figure 1 juxtaposes the simulation snapshots with the mean-field phase diagram of diblock copolymers. [95] When the minority-block volume fraction (f_{PMMA}) is 0.50, the polymer adopts the expected lamellar (L) morphology. Reducing f_{PMMA} to 0.40 first produces perforated lamellae and then, at 0.30, a well-defined hexagonal array of PMMA cylinders (C). A further decrease to 0.20 eliminates long-range order and yields a disordered (D) melt, reproducing the canonical sequence L → C → D predicted by theory and experiment.[117]

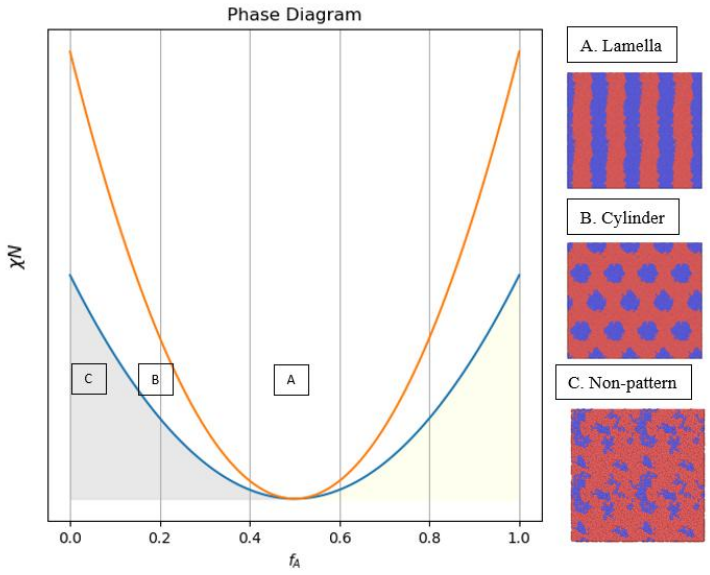
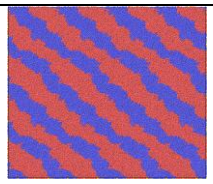
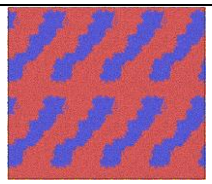
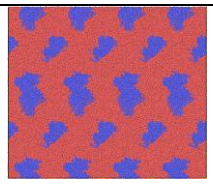
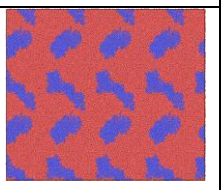
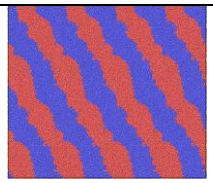
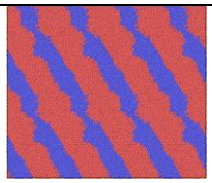
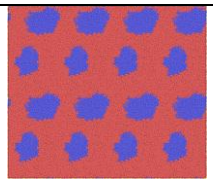
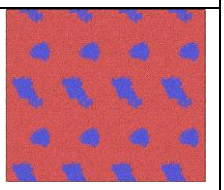
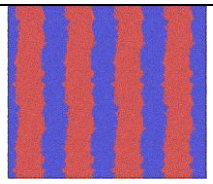
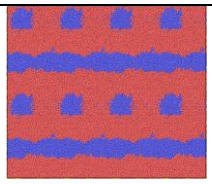
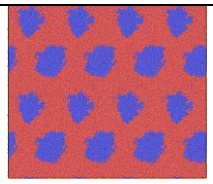
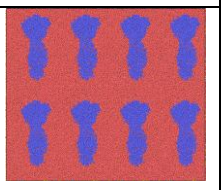


Figure 1. The theoretical block copolymer phase diagram. The blue color is the PMMA bead, while the red color is the PS beads

Because microphase separation is governed by the product χN, we first surveyed the effect of chain length N (expressed as the reduced contour length L in units of σ). Table 6 summarizes the morphologies obtained for L = 80, 100, and 120 σ at four PS : PMMA compositions. Cylindrical ordering is absent for L < 80 σ, but emerges sharply once χN exceeds ≈ 140 (≈ L = 80 σ in this model). Increasing L beyond that threshold primarily sharpens the domain interfaces without shifting the phase boundaries. Among the conditions tested, the combination L = 100 σ and f_{PMMA}=0.30 produces the most regular, defect-free hexagonal array and therefore offers the greatest potential for

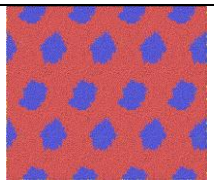
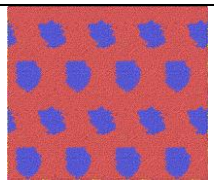
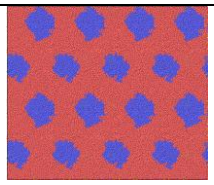
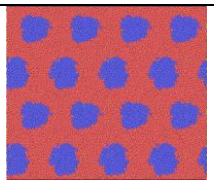
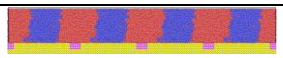
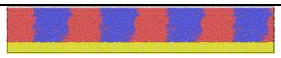
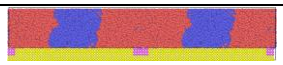
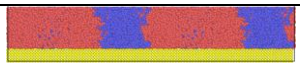
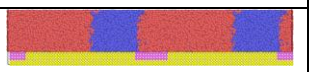
contact-hole patterning. This parameter was selected as the baseline for all subsequent chemo-epitaxy simulations.

Table 6. The comparison between mole ratio and the length of BCP on neutral substrate.

	PS : PMMA ratio			
BCP length (σ)	50:50	60:40	70:30	80:20
L = 80 σ				
L = 100 σ				
L = 120 σ				

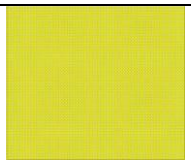
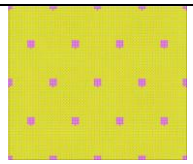
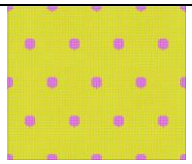
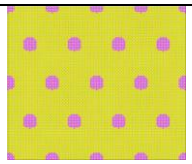
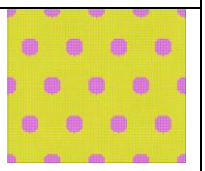
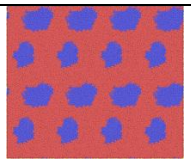
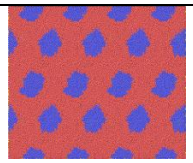
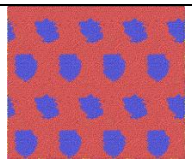
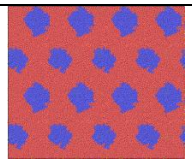
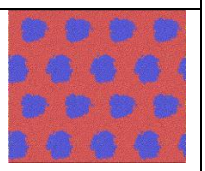
With these baseline parameters established, we introduced immobile PS-affine discs ("flat-pinned domains") to guide cylinder placement. Table 7 summarize the outcome for pinning-site radius R=3–6 σ. Each disc nucleates a single PMMA cylinder, and the global hexagonal order—quantified by the averaged bond-orientational parameter ⟨ψ6⟩—improves markedly relative to the unpatented case.

Table 7. The relationship between the radius of pinned domain and the structure of the DSA BCP on flat pinned substrate. The composition of the BCP is PS : PMMA = 70 : 30 with co-polymer length equal to 100 σ. Ψ6 is normalized by the ideal contact hole structure.

	Pinned domain radius (σ)			
	R = 3 σ	R = 4 σ	R = 5 σ	R = 6 σ
xy				
xz				
yz				
Ψ6(%)	90.7659	91.0266	91.1832	90.6224

The optimum range R = 4 ~ 5σ coincides with one half of the natural cylinder-to-cylinder spacing, indicating that commensurability between the pinning site and the intrinsic lattice constant minimizes defects. A control simulation with no pinning (Table 8) attains only ⟨ψ6⟩=88.65 %, underscoring the templating effect of chemo-epitaxy.

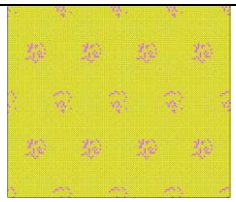
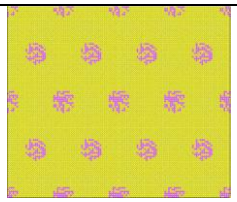
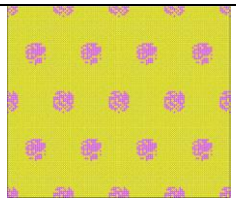
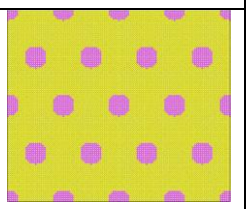
Table 8. comparison between flat pinned domain and non-pinned domain

	Pinned domain radius (σ)				
	R = 0 σ	R = 3 σ	R = 4 σ	R = 5 σ	R = 6 σ
Substrate					
DSA BCP					
Ψ6(%)	88.6538	90.7659	91.0266	91.1832	90.6224

2.3.2 Brush-pinned template: effect of graft density and pinned area

Table 9 and figure 2 show that the two shortest brush layers—2 σ and 4 σ—deliver the highest normalized bond-orientational order, $\psi_6 \approx 91.8$–92.5 %, over the entire graft-density range of 25–100 %. By contrast, extending the brushes to 6 σ or 8 σ lowers ψ_6 by roughly 1–3 %. The trend is readily explained by the relative balance of chemical versus topographic guidance. When the grafted chains are shorter than about 5 σ, they remain close to the substrate and act chiefly as a chemical affinity patch that anchors the PS block without intruding into the volume occupied by the PMMA cylinders; the cylinders therefore retain a high degree of six-fold orientational order that is largely insensitive to surface coverage. Once the brushes grow to 6 σ or 8 σ, their swollen coronas protrude well into the self-assembling film, crowding the space needed for regular packing and introducing an unintended grapho-epitaxial constraint; the resulting steric interference distorts the local lattice, depressing ψ_6 to the 89–91 % range. Graft density modulates this behavior only secondarily: short brushes tolerate a wide span of coverages, but a moderate window (25–75 %) still yields the very highest ψ_6, whereas complete coverage (100 %) slightly blurs the chemical contrast through lateral crowding of free ends. Overall, maintaining a brush height no greater than ~4 σ—comparable to, or smaller than, half the natural cylinder pitch—preserves high six-fold symmetry across a broad range of graft densities, while longer brushes invariably introduce grapho-epitaxial perturbations that erode the orientational order of the resulting cylinder array.

Table 9. The relationship between different brush polymer density and the DSA BCP pattern on the brush coated substrate.

Normalized Ψ6 (%)	Brush density (%)			
	25%	50%	75%	100%
Substrate				
Brush Length = 2 σ	92.449	91.872	92.104	91.831

Brush Length = 4 σ	92.124	91.444	91.333	91.200
Brush Length = 6 σ	91.726	91.141	90.842	90.687
Brush Length = 8 σ	91.482	90.695	90.100	89.458

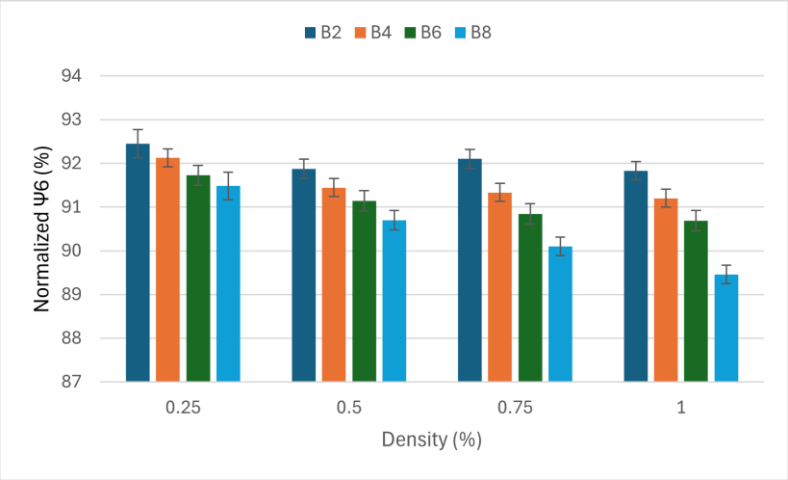


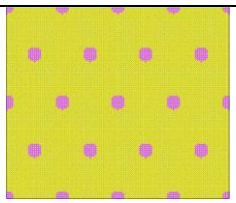
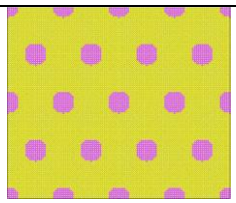
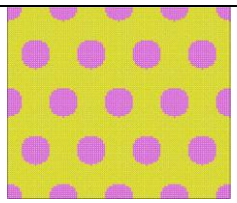
Figure 2. The relationship between different brush polymer densities and Normalized Ψ6. (B2 means brush length equals to 2 beads, B4 means brush length equals to 4 beads, B6 means brush length equals to 6 beads, and B8 means brush length equals to 8 beads)

2.3.3 Brush-pinned template: effect of pinning-site radius on brush-pinned chemo-epitaxy

Table 10 and figure 3 reveal that the influence of pinning-domain radius (R = 4, 6, 8 σ) on six-fold orientational order depends sensitively on brush height. When the grafted chains are short (≤ 4 σ) they lie close to the substrate, act almost exclusively as chemical affinity patches, and therefore benefit from a broader target: ψ_6 rises steadily with R and reaches a maximum of ≈ 92 % at R = 8 σ. Once the brushes extend to intermediate lengths (~4 σ), their coronas begin to protrude into the film; under these conditions ψ_6 levels off near 91.6 % and shows only a shallow optimum at R ≈ 6 σ, indicating that moderate domains still guide the cylinders effectively but additional area beyond one lattice spacing confers little extra advantage. For the longest brushes (≥ 6 σ) the trend reverses: the swollen chains crowd the volume that the PMMA

cylinders must occupy, so enlarging the pinning site simply introduces more steric interference and ψ_6 decreases monotonically, the value at $R = 8\ \sigma$ being ~1.4 % lower than at 4 σ for an 8 σ brush. Taken together, these observations establish a coupled design rule: widening the pinning domain improves hexagonal order only when the brush layer remains short and closely bound to the surface, whereas templates with brushes protruding appreciably above the substrate should restrict the domain radius to roughly one natural cylinder spacing to preserve maximal symmetry.

Table 10. The relationship between different pinned domains and the DSA BCP pattern on the brush coated substrate.

Normalized Ψ6 (%)	Pinned Domain Radius (σ)		
	4 σ	6 σ	8 σ
Substrate			
Brush Length = 2 σ	91.833	92.109	92.250
Brush Length = 4 σ	91.507	91.596	91.474
Brush Length = 6 σ	91.441	91.110	90.746
Brush Length = 8 σ	91.038	89.866	89.719

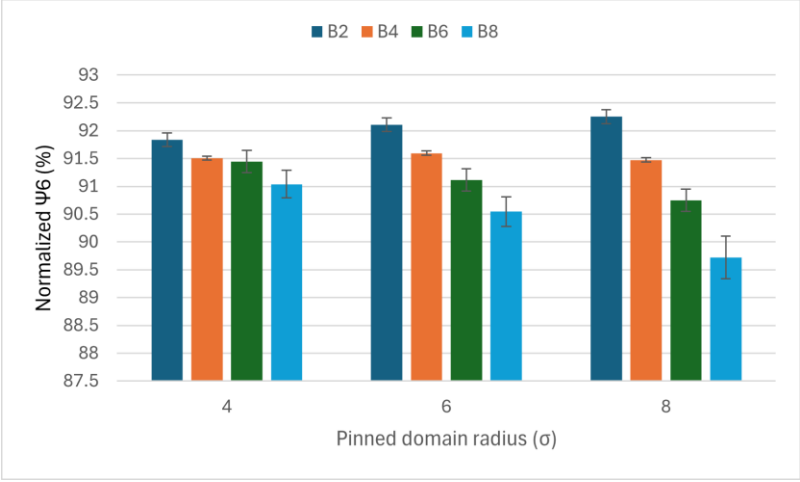


Figure 3. The relationship between different pinned domains and Normalized Ψ6.

2.3.4 Cylinder Roughness and Tapering Effect

Table 11 and table 12 quantify how surface roughness evolves with height for cylinders templated by brush-pinned domains of increasing radius ($R = 4, 6, 8\ \sigma$) and brush length (brush length = 2–8 σ). Two features stand out. First, although the mean roughness averaged over the central core of the pillars ($5\ \sigma \le z \le 19\ \sigma$) is essentially invariant at $\approx 6.0\ \sigma$ for all three radius, the width of the roughness distribution—measured by its three-sigma envelope—contracts steadily as the pinning site or the brush layer is enlarged. For a fixed radius the envelope narrows by 15–20 % when brush length is extended from 2 σ to 8 σ, consistent with the notion that a thicker, more compliant brush mantle damps interfacial undulations. Second, at every brush length the largest pinned domain ($R = 8\ \sigma$) delivers the smoothest cylinders: the three-sigma spread falls to $0.97 \pm 0.35\ \sigma$, compared with $1.18 \pm 0.43\ \sigma$ for $R = 4\ \sigma$, shown as table 10. This additional gain can be traced to the broader chemical footprint provided by the 8 σ pinned domain, which packs the cylinder base more tightly and suppresses low-*z* roughening. The data therefore suggest that roughness stability is governed by a cooperative confinement mechanism: longer brushes furnish radial support along the entire pillar while a sufficiently wide pinning domain locks the cylinder at its foot, together yielding the lowest fluctuations observed. At the opposite extreme—short brushes combined with large pinned domain—lack of top-end guidance can still trigger local roughening spikes near the free surface, underscoring the need to balance brush height and domain radius when both surface smoothness and global six-fold order are required.

Table 11. The relationship between roughness and pinned domains.

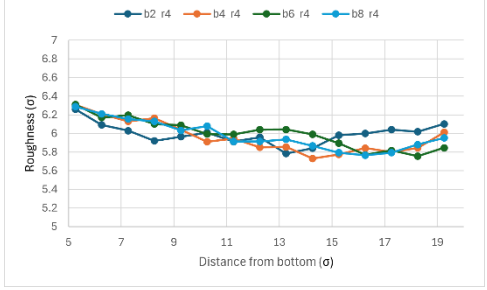
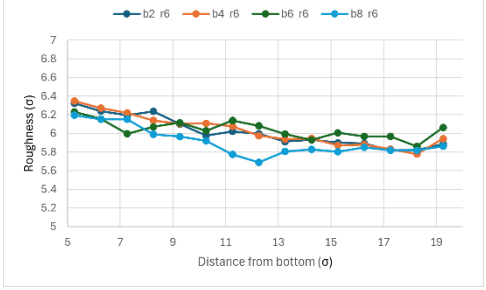
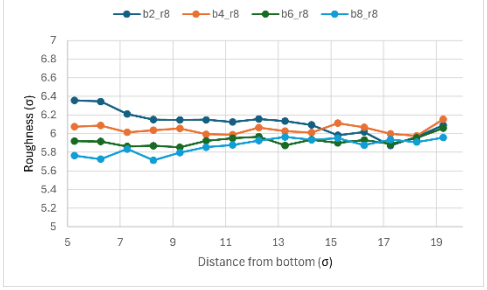
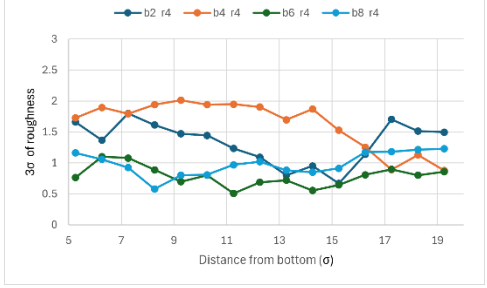
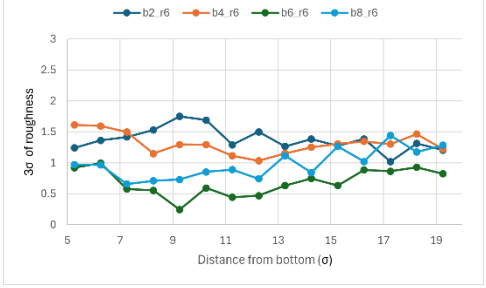
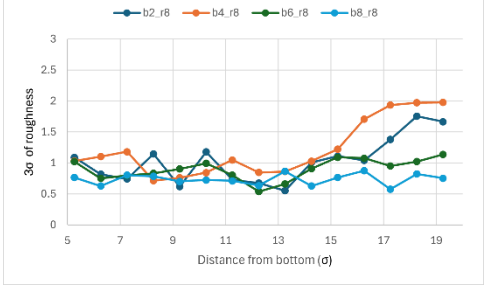
Pinned domain radius = 4 σ	Pinned domain radius = 6 σ	Pinned domain radius = 8 σ
		
		

Table 12. The roughness along the z direction over 5 σ ≤ z ≤ 19 σ (n = 4)

	Pinned domain radius = 4 σ	Pinned domain radius = 6 σ	Pinned domain radius = 8 σ
Avg. Roughness	5.984 ± 0.151	5.998 ± 0.153	5.987 ± 0.130
Avg. 3 σ	1.182 ± 0.430	1.087 ± 0.341	0.971 ± 0.346

On the other hand, slope analysis of the cylinder-radius profiles (table 13 and table 14) offers quantitative insight into pillar tapering across the brush-pinned parameter space. For each sample the radius $R(z)$ was fitted to a linear function over the interval $5\,\sigma \le z \le 19\,\sigma$, and the resulting slope, $\Delta R/\Delta z$, serves as a single-number descriptor of shape: negative values correspond to conventional tapering (bottom-wide, top-narrow), positive values to inverse tapering, and slopes statistically indistinguishable from zero indicate straight pillars, shown as Figure 4. The data reveals two cooperative effects. First, increasing brush length systematically flattens the radius profile. At a fixed pinning radius of 6 σ, the slope rises from -3.6×10^{-2} for the 2 σ brush to -8.1×10^{-3}

for the 6 σ brush, a four-fold reduction in tapering. Second, enlarging the pinning domain further mitigates shape anisotropy: with an 8 σ pinned domain the longest brush (8 σ) yields a small positive slope ($+6 \times 10^{-3}$), while the shortest brush still exhibits only modest conventional tapering (-2.4×10^{-2}). These trends support a simple physical picture. Long grafted chains provide a compliant, radially confining sheath that suppresses differential shrinkage along the pillar axis, whereas a broader chemical footprint at the base distributes the pinning force over a larger area and minimizes corner effects, thereby promoting uniform growth in the upper section. Consequently, the combination of large pinning domains and long brushes produces the straightest pillars ($|\Delta R/\Delta z| \approx 0$), whereas short brushes tethered to small domains generate the most pronounced tapering.

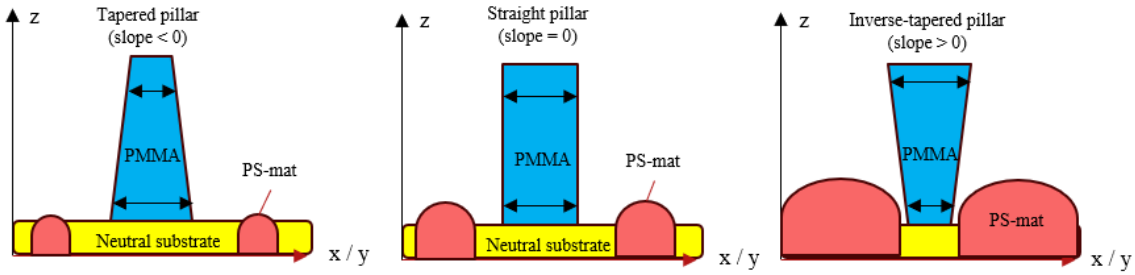


Figure 4. The schematic diagram of tapering effect for cylinders

Table 13. The relationship between pinned domain and the linear slopes

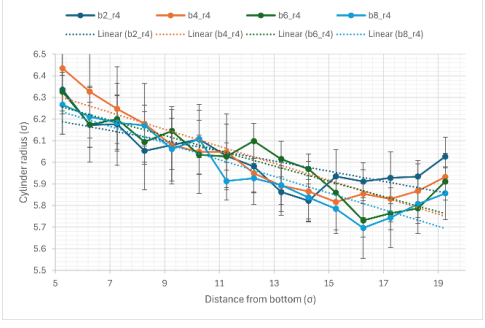
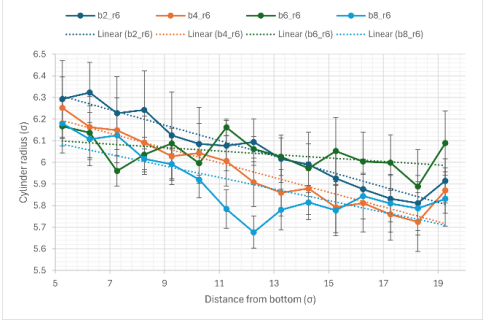
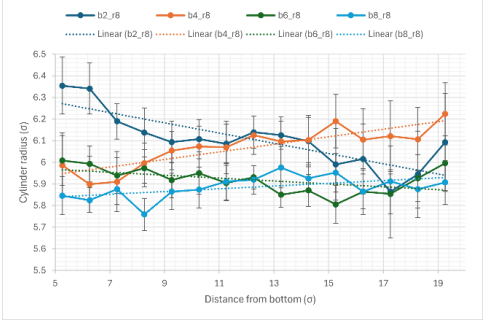
Pinned domain radius = 4 σ	Pinned domain radius = 6 σ	Pinned domain radius = 8 σ
		

Table 14. The relationship between linear slop and tapering effects

Slope (Δradius/Δz)	Pinned Domain Radius (σ)			
Pinned domain	Brush length = 2 σ	Brush length = 4 σ	Brush length = 6 σ	Brush length = 8 σ
R = 4 σ	-0.0235	-0.0391	-0.0352	-0.0385
R = 6 σ	-0.0358	-0.0341	-0.0081	-0.0267
R = 8 σ	-0.0237	0.0175	-0.0068	0.0063

2.4 Conclusions

This study employed coarse-grained molecular-dynamics simulations to clarify how chemo-epitaxial templates fashioned from brush-coated pinning domains guide PS-*b*-PMMA into the hexagonally packed contact-hole morphology required for advanced lithography. Beginning with a neutral substrate, we established a baseline copolymer composition ($L = 100\,\sigma$, $f_{PMMA} = 0.30$, $\chi N \approx 140$) that exhibits the highest intrinsic degree of order and then quantified the coupled influences of pinning-site radius, brush-chain length, and graft density on three performance metrics: six-fold bond-orientational order (ψ6), side-wall roughness, and pillar tapering. Flat, immobile pinning domain enhanced ψ6 from 88.7 % in the unpatterned film to values exceeding 91 % when their pinned domain matched one-half of the natural cylinder pitch (4 σ). Replacing these pinned domains with mobile brush layers preserved—and in favorable cases slightly surpassed—this level of ordering provided the brush height remained at or below one half-period of the lattice; longer brushes introduced steric crowding that degraded ψ6 by as much as three percentage points.

The simulations further reveal a cooperative confinement mechanism governing surface quality. As brush height increases from 2 σ to 8 σ, the three-sigma envelope of side-wall roughness contracts by roughly twenty percent, an effect that is amplified by an additional ten percent when the pinning-site radius is expanded to 8 σ. This smoothing arises because a compliant brush mantle damps interfacial fluctuations while a broad chemical footprint anchors the cylinder base. Linear-slope analysis

shows that such cooperative confinement also controls pillar shape: tapering is essentially eliminated only when long brushes ($\geq 6\,\sigma$) are paired with the largest pinning domains, whereas short brushes tethered to narrow domains produce the most pronounced bottom-wide pillars. Synthesizing these trends yields a practical design window for sub-10 nm contact-hole printing: graft densities of 25–75 %, brush heights of 2–4 σ, and pinning radii of 6–8 σ simultaneously maximize $\psi 6$ (> 92 %), minimize roughness (< 1.0 σ on a three-sigma basis), and suppress taper.

By combining quantitative order metrics with geometric analyses of roughness and tapering, the present work provides a materials-selection map that can guide the integration of brush-assisted chemo-epitaxy with optical lithography, thereby offering a route to pattern fidelity without exclusive reliance on costly EUV exposure. Future extensions will incorporate multi-layer stacks and experimentally calibrated interaction parameters, enabling wafer-scale validation and direct assessment of defectivity across realistic process windows.

CHAPTER 3
A Multi-Process Molecular Dynamics Framework for High-Precision Boron Ion Implantation in Silicon LDD Devices

3.1 Introduction

This section focuses on a Lightly Doped Drain (LDD) process modeling framework that integrates multiple semiconductor fabrication steps. In contrast to the broad overview provided in Chapter 1, this chapter zeroes in on specific concepts and techniques critically for accurately simulating LDD formation. The following subsections introduce the key background topics – from basic semiconductor doping and LDD device structures to advanced processing techniques and atomistic simulation methods – that set the stage for the detailed modeling work presented. By covering these targeted areas, the introduction clarifies how the chapter's approach combines various processes (implantation, annealing, deposition) within a single model tailored to LDD engineering.

3.1.1 P-Type and N-Type Semiconductor

Modern semiconductor devices rely on controlled doping to tailor electrical properties. Doping is the intentional introduction of impurity atoms into a pure (intrinsic) semiconductor crystal in order to modify its conductivity.[118] Adding trivalent impurities (from group III of the periodic table, like boron or indium) creates a p-type semiconductor, whereas adding pentavalent impurities (group V elements such as phosphorus, arsenic, or antimony) produces an n-type semiconductor.[118] In p-type silicon, dopant atoms like boron substitute for silicon and have one fewer valence electron, which results in mobile "holes" (positive charge carriers) in the lattice. Conversely, n-type dopants like phosphorus have one extra valence electron, contributing additional free electrons (negative carriers) to the material. The concentration and type of dopant introduced can change the semiconductor's carrier

density by many orders of magnitude, effectively turning a near-insulator into a conductive material.[119] Careful spatial control of p-type and n-type regions is what allows formation of p–n junctions and transistor structures. For example, in CMOS transistor fabrication, the source and drain regions are heavily doped (n+ or p+) while the channel region under the gate is lightly doped or has the opposite type of doping to set the desired threshold voltage.[120] These well-defined doping profiles are essential for device functionality and are achieved through highly controlled processing techniques, as discussed below.

3.1.2 Lightly Doped Drain (LDD) Structure

As transistors scaled into the sub-micron regime, engineers introduced the Lightly Doped Drain (LDD) structure to improve device reliability and mitigate short-channel effects. In a conventional MOSFET, the abrupt junction between the highly doped source/drain and the channel can create a very strong electric field at the drain end when the device is biased, accelerating carriers to high energies (hot carriers) that damage the gate oxide and shift device characteristics. The LDD structure addresses this by inserting a narrow lightly doped n^- region between the channel and the n^+ source/drain regions (for an n-channel transistor).[121] This graded junction spreads out and lowers the peak electric field at the drain, thereby reducing hot-carrier injection and improving the transistor's breakdown voltage. Ogura et al. (1980) first demonstrated that LDD transistors achieved significantly less hot-electron degradation and higher breakdown compared to conventional devices, at the cost of a slight increase in series resistance due to the lightly doped extensions.[121] Subsequent analyses confirmed that while the LDD implant regions inevitably introduce extra source/drain resistance (diminishing drive current modestly), they dramatically cut down the maximum field and prolong device lifetime under high voltages.[122]

The typical fabrication sequence for an LDD MOSFET involves two implant steps: a low-dose, low-energy implant to form the shallow n^- extension regions self-aligned to

the gate edges, followed by the deposition of a sidewall spacer and then a second, higher-dose implant to form the deep n^+ source/drain regions.[122] The sidewall spacer (often made of a CVD-deposited dielectric) offsets the second implant from the gate, so that the heavily doped n^+ area begins where the lightly doped extension ends. After subsequent annealing, this process yields a graded junction profile: very shallow doping near the channel and heavier doping farther out. The LDD structure thus balances competing needs – it preserves performance as much as possible while protecting the device against the worst of hot-carrier and short-channel effects. LDD implants became a standard feature of sub-micron MOSFET technologies and are central to the process modeled in this chapter.

3.1.3 Types of Ion Implantation

Ion implantation is the primary method for introducing dopant atoms into precise locations in silicon for modern processes, offering fine control over dose and depth. In a conventional beam-line ion implanter, dopant ions (such as B^+, P^+, or As^+) are accelerated to a specified energy and directed at the wafer, where they collide with the lattice and come to rest at some average penetration depth governed by the ion energy.[123] By adjusting the implant energy, species, and dose, manufacturers can tune junction depths and sheet resistances with great accuracy. For instance, achieving the ultra-shallow junctions needed for LDD source/drain extensions requires extremely low implant energies (on the order of a few keV or below for boron), since higher-energy implants would place dopants too deep into the substrate.[124] One practical challenge of these ultra-low-energy implants is low beam current – the ion beam inherently carries fewer ions at low acceleration voltages, reducing throughput.[124] Additionally, light dopants like boron tend to channel along crystal directions during implantation, leading to deeper tails than intended.[125]

To push junction depths even shallower without sacrificing throughput or precision, researchers developed specialized implantation techniques. One approach is the cluster

ion implantation, wherein a molecule containing the dopant (e.g. decaborane, $B_{10}H_{14}$) is ionized and accelerated as a single heavy particle.[126] Upon impact, the molecule breaks apart, effectively implanting a cluster of boron atoms in nearly the same location. Decaborane implantation at a given total energy per molecule deposits boron atoms with much lower per-atom energy, thus inherently producing shallower profiles than an equivalent monomer implant.[127] Studies have shown that a 3 keV decaborane implant, after rapid annealing, can achieve junction depths of ~20 nm – extremely shallow by conventional standards.[127] Moreover, because each decaborane ion carries ten boron atoms, space-charge effects are reduced and higher beam currents can be used, improving dose rate capacity. Molecular dynamics simulations indicate that while B cluster implants and B^+ implants yield similar dopant distributions, a single decaborane impact displaces roughly four times more Si atoms than a single B ion, creating a more locally amorphized region that must be annealed to recrystallize.[128] Despite the extra damage, cluster implantation proved effective for forming ultra-shallow junctions in research prototypes, and it addresses the beam current limitation of ultra-low-energy single-ion beams.

Another variant is plasma immersion ion implantation, often simply called plasma doping (PLAD).[129] In plasma doping, the wafer is placed directly in a plasma containing the dopant species (e.g. BF_3 or AsH_3 gases are dissociated to provide dopant ions). A pulsed bias on the wafer accelerates ions from the plasma sheath into the substrate. This technique enables doping of non-planar structures and large areas uniformly without the beam steering of a traditional implanter. PLAD is especially useful for doping complex 3D device architectures (like FinFET sidewalls or memory device trenches) where line-of-sight beam implantation would be non-uniform.[130] It generally operates at lower ion energies (plasma potentials of a few 100 V to 1–2 kV) and higher pressures, leading to very shallow, conformal doping profiles. The trade-off is that dose control and repeatability can be more challenging than in beam-line tools. In summary, whether via conventional beam-line implants, cluster ions, or plasma-

based methods, ion implantation offers a versatile toolbox for achieving the tailored dopant profiles required by advanced LDD processes.

3.1.4 Ultra-Shallow Junctions

Ultra-shallow junctions refer to source/drain junction depths on the order of tens of nanometers or less – a regime essential for sub-100 nm gate length transistors to suppress short-channel effects.[131, 132] As device dimensions shrink, the depth of the junctions must scale down accordingly; for example, in sub-0.1 μm (100 nm) MOSFET technologies, extension junctions often need to be well below 50 nm deep.[133] If the junctions are too deep relative to the channel length, undesirable phenomena like punch-through leakage and threshold voltage roll-off occur. Achieving such shallow junctions is non-trivial because it demands extremely low implant energy (less than 5 keV for boron, as noted) and minimal high-temperature exposure thereafter. Boron, the typical p-type dopant for PMOS source/drains, presents a particular challenge: it has a fast diffusion rate in silicon, so even brief thermal treatments can cause significant smearing of a shallow profile.[134] For instance, to reach junction depths under 50 nm, boron implants must be done at energies of ~0.5–1 keV or lower. At these energies, ion beam currents are very low, and implanted atoms tend to remain in an amorphized surface layer.

Several process innovations have been developed to realize ultra-shallow junctions while maintaining electrical activation of dopants. Pre-amorphization of the silicon surface with a non-dopant implant (such as Si or Ge ions) is one common technique: by amorphizing the lattice to a certain depth before dopant implantation, channeling of dopants is eliminated and the as-implanted profile is very abrupt.[135, 136] After dopant implantation into the amorphous layer, a careful anneal can regrow the crystal and electrically activate the dopants with minimal diffusion beyond the original amorphous/crystalline interface. Another strategy, mentioned above, is the use of cluster implants like $B_{10}H_{14}$, which effectively allow higher doses at ultra-low

equivalent implant energies.[124] With decaborane, for example, a 5 kV acceleration yields boron atoms implanted only ~1–5 nm from the surface (in an amorphous layer ~4 nm thick), which after a rapid anneal still form an extremely shallow junction (tens of nm) with acceptable sheet resistance. Yet another approach is in-situ doped epitaxial deposition – for instance, depositing a very shallow silicon or SiGe layer doped with the desired impurities, which then out-diffuse a short distance into the substrate upon annealing.[137] Researchers have shown that a selectively grown ~100 nm P-doped SiGe layer can diffuse phosphorus to form ~25 nm deep extensions after a 900 °C rapid thermal anneal.[137] This "diffusion from a doped layer" technique yields a steep concentration gradient at the diffusion front and can be preferable for certain applications. Regardless of method, tight thermal budget control is essential: ultra-shallow junction formation must be paired with brief, carefully optimized anneals to activate dopants without letting them diffuse much. The next subsection discusses the annealing solutions developed for this purpose.

3.1.5 Rapid Thermal Annealing (RTA)

Once dopants are implanted into silicon (particularly with the very shallow profiles and lattice damage described above), a thermal annealing step is required to repair implantation damage and activate the dopants electrically (i.e. incorporate them substitutionally into the lattice).[32] Rapid Thermal Annealing (RTA) has become the standard technique for this, especially for ultra-shallow junction fabrication.[138] In an RTA process, wafers are heated to a high peak temperature (often 950–1050 °C or even higher) for only a very short duration (a few seconds or less), then cooled rapidly. This is often implemented as a spike anneal, where the wafer is ramped up to the peak temperature and immediately ramped down, with no sustained soak time. The virtue of RTA lies in its low thermal budget: by drastically limiting the time at high temperature, RTA provides the needed dopant activation and damage anneal without giving dopants enough time to diffuse far from their as-implanted positions.[139] In effect, RTA

enables near “freeze-in” of the doping profile after activation, preserving the steep dopant gradients required for ultra-shallow junctions.[140]

For example, boron-implanted extensions (prone to rapid diffusion) can be activated by a spike RTA at ~1050 °C for just a couple of seconds, achieving high electrical activation while only slightly broadening the junction profile.[141] The peak temperature can be higher than in a furnace anneal because the duration is so brief – higher temperature helps maximize dopant activation (and recrystallize the amorphous layers) in the limited time available. Modern RTA tools use lamp-based or laser-based heating to attain extremely fast ramp rates (several hundred °C per second or more). This is crucial for shallow junctions: a slow ramp would add to the effective anneal time and permit unwanted diffusion.[140, 142] By contrast, older furnace annealing methods required minutes of bake time at temperature, which is far too long for <50 nm junctions (the dopants would diffuse out significantly, and concentration profiles would “smear” out).

RTA not only activates dopants but also helps restore the silicon crystal quality after ion implantation. End-of-range damage, interstitial clusters, and other implant-induced defects are partially annealed out during the thermal spike. However, because the time is limited, some residual defects can remain – these may require additional processing or careful optimization to minimize.[143] In advanced processes, millisecond-scale annealing techniques (like flash lamps or laser anneals) have been introduced to push thermal budgets even lower than conventional RTA. These methods heat the wafer to peak temperatures in the millisecond or microsecond regime. Millisecond anneals can achieve dopant activation with essentially no diffusion; for instance, a microsecond laser anneal can melt a very shallow silicon layer and regrow it, activating dopants, all in an extremely short timeframe. Such techniques are beyond the scope of a typical LDD process flow, and RTA (on the order of seconds) remains the workhorse for LDD junction formation. In summary, RTA provides the critical ability to anneal implant damage and electrically activate ultra-shallow junctions while freezing in the abrupt

dopant profiles designed by the implantation step. Without RTA or an equivalent low-duration anneal, the benefits of careful low-energy implants would be lost to diffusion.

3.1.6 Plasma Deposition Techniques

In addition to implantation and annealing, semiconductor process flows rely on deposition steps to add thin films needed for device structures. Plasma-enhanced deposition techniques are widely used in modern fabrication to create these films at lower temperatures and with good control over film properties.[144] In the context of an LDD process, one important deposition is the formation of the sidewall spacer after the extension implant. This spacer – often a thin layer of silicon dioxide or silicon nitride – is typically deposited conformally over the wafer and then anisotropically etched back to leave a spacer on the gate sidewall. The spacer deposition is commonly done by Plasma-Enhanced Chemical Vapor Deposition (PECVD), which allows deposition of dielectrics at relatively low substrate temperatures (300–400 °C) using plasma to enhance chemical reactions.[145] For example, a silicon nitride spacer can be deposited by PECVD at ~400 °C, whereas a traditional Low-Pressure CVD (LPCVD) process for nitride might require ~700 °C or higher. The ability to deposit at lower temperatures is crucial once transistor structures like shallow junctions or delicate gate stacks are in place, as high-temperature processing could cause dopant diffusion or other unwanted changes.[146]

Plasma deposition methods encompass not only PECVD for insulators but also sputtering and other PVD (physical vapor deposition) techniques for metals, all utilizing plasma to either decompose precursors or eject material for film formation. Plasma processes offer advantages such as improved film conformality and tunable film stress/density by adjusting plasma power and chemistry. In the spacer example, both LPCVD and PECVD can be used for silicon nitride spacers, but PECVD provides more flexibility for low-temperature processing and can yield slightly different film stress which impacts device performance.[147] Plasma-deposited silicon

nitride or oxide films are also used as screen oxides or capping layers during implants – for instance, a thin oxide deposited before implant can act as a screen to reduce channeling and to trap impurities. After implantation, that layer might be removed. Another key application is the deposition of dopant-containing films. In certain process flows (though less common in advanced CMOS), a doped oxide like borosilicate glass may be deposited on the surface and later driven in as a dopant source.[148] Plasma deposition can facilitate such a step by creating a uniform dopant-rich layer. More broadly, plasma-enhanced deposition is ubiquitous in device fabrication: from interlayer dielectric deposition to passivation layers, plasma processes enable high-quality films at throughputs and temperatures compatible with complex device integration.[147] In the integrated LDD process modeling context, understanding plasma deposition is important because it interfaces with other steps (e.g. the spacer deposition affects where the second implant goes, and any film deposition can modify the surface conditions for subsequent implants or anneals). While the modeling framework in this chapter is primarily atomistic for implantation and annealing, it is designed to be compatible with additional process modules – in principle, one could incorporate atomic-scale simulations of deposition or surface modification as well. For now, we note that plasma-assisted deposition techniques are an integral part of the LDD flow and overall CMOS process, ensuring that needed thin films (like spacers) are in place with minimal thermal budget and excellent uniformity.

3.1.7 DFT-Calibrated Interatomic Potentials for MD Simulation

The later sections of this chapter delve into a molecular dynamics (MD) simulation framework for LDD process steps. A crucial foundation for any MD simulation is the interatomic potential – a mathematical description of the forces between atoms. Traditional MD simulations use empirical or semi-empirical potentials (for example, the Tersoff or Stillinger–Weber potentials for silicon) that are fitted to reproduce certain properties from experiments or quantum calculations.[57, 149] However, classical potentials may not be accurate for all conditions, especially when new

elements or uncommon interactions are involved (such as a dopant atom recoiling through a lattice and interacting with defects). In this work, we improve the fidelity of the MD model by deriving custom interatomic potentials for the Si–B system using Density Functional Theory (DFT) calculations. This approach is often termed DFT-informed or quantum-informed MD.[150, 151] By calculating the energy of various atomic configurations with DFT – a first-principles quantum mechanics method – one can calibrate a more accurate potential that reproduces those DFT results in MD simulations. In essence, DFT provides a higher-accuracy benchmark for atomic interactions, which is then fit with an analytic potential functional form usable in large-scale MD.

In our case, a Lennard-Jones (LJ) type pair potential for B–Si and B–B interactions were derived from DFT computations, and then combined with a many-body Si–Si potential (the Tersoff potential) to create a hybrid potential suited for silicon with implanted boron. The rationale is that silicon's behavior is well captured by an existing many-body potential, but the interactions involving boron (an impurity in silicon) required new parameters reflecting quantum mechanical calculations. This DFT-calibrated potential aims to bridge the accuracy gap between classical MD and ab initio methods. Generally, incorporating DFT data can vastly improve predictive accuracy: recent studies show that machine-learning or DFT-fitted potentials can approach quantum-level precision while maintaining MD-level efficiency.[152] Wang et al. (2024) note that "Machine learning interatomic potentials overcome the challenges of high computational costs in DFT and the low accuracy of classical MD, enabling more efficient and precise simulations".[152] In the same spirit, our quantum-informed potential retains the computational speed needed to simulate millions of atoms, but with far better realism for B–Si collisions, defect formation energies, and diffusion behaviors than a generic force field. The development of these interatomic potentials is a foundational step that allows the subsequent MD simulations to faithfully capture processes like low-energy boron implantation and rapid annealing within a single integrated model.

3.1.8 Applications of MD in Semiconductor Fabrication Modeling

Molecular dynamics has emerged as a powerful tool for modeling physical processes in semiconductor fabrication at the atomic scale, complementing continuum process simulators (TCAD) which operate at the diffusion or device level.[153] MD is uniquely suited to simulate the early, ballistic phase of ion implantation – essentially the collision cascade events as an ion penetrates the substrate. Researchers have long used MD to study displacement cascades and predict damage generation and amorphization in silicon from implanted ions.[154] For example, by using MD to track individual silicon and dopant atoms during a low-energy implant, one can directly observe channeling vs. scattering, estimate the amorphous layer thickness, and identify defect structures formed by the implant. Such atomistic insights feed into better calibration of Monte Carlo implant models and damage anneal models in TCAD. In this chapter, we apply MD to model not just the implant itself but also the subsequent annealing, thereby covering the full sequence of LDD extension formation. This kind of multi-step MD simulation has become feasible thanks to improved potentials (as discussed above) and more powerful computing. Our approach builds on prior studies that combine MD with annealing simulations. We validate our simulated boron profiles against Secondary Ion Mass Spectrometry (SIMS) measurements and find good agreement when using the DFT-informed potential, whereas classical potentials would not capture certain clustering and channeling effects.

Beyond ion implantation, MD has been applied to other fabrication steps in research contexts. Thin-film deposition is one area: MD simulations have been used to study the microstructure of films grown by sputtering or evaporation, by simulating the arrival of deposition species on a substrate and their subsequent aggregation. This helps in understanding phenomena like film amorphization, interface mixing, or roughness development on the nanoscale (important, for example, in understanding how a plasma-deposited spacer might have a certain density or stress).[155-157]

Similarly, MD has been used to investigate laser annealing and melting/recrystallization dynamics in silicon – providing insight into how dopants redistribute during very rapid melt fronts. However, a limitation of MD is the timescale: processes like thermal diffusion over milliseconds are far beyond direct MD (which typically covers nanoseconds). To tackle this, one strategy is to integrate MD with higher-level models. For instance, one can use MD to simulate a sub-nanosecond laser spike anneal (where a thin surface layer melts and refreezes), then hand off the resulting structure to a kinetic Monte Carlo or continuum model for longer-term diffusion. This kind of multiscale simulation is a growing area of interest. In our LDD framework, we demonstrate that MD can handle the implant and the immediate annealing spike entirely within one atomistic simulation, which is a significant step toward multiscale process modeling. By capturing dopant implantation, transient diffusion, and defect evolution in one unified atomistic environment, we address some gaps left by traditional process simulators (which usually treat these steps separately and with continuum approximations). The applications of MD in process modeling thus span from fundamental studies of damage and diffusion to practical calibration of process parameters. The insights gained, such as how a 1 nm surface boron layer influences junction abruptness, or how varying implant tilt angles affects channeling, can directly inform process engineers in optimizing implant and anneal conditions for next-generation devices.

In summary, this chapter's introduction has outlined the essential background: the nature of p/n doping and LDD structures, the specialized implantation and annealing techniques for ultra-shallow junctions, the role of plasma deposition in device processing, and the novel use of DFT-calibrated MD simulations to integrate these steps. Equipped with this context, the subsequent sections will present the development and validation of our quantum-informed MD framework for LDD process simulation. This framework is tailored to capture the implant damage, dopant activation, and diffusion phenomena at atomic resolution, thereby providing a more detailed and predictive modeling tool for advanced semiconductor process engineering.

3.2 Methodology

This section details the multi-scale workflow used to generate quantum-informed interatomic potentials, carry out large-scale molecular-dynamics (MD) simulations of boron implantation, and model the subsequent rapid-thermal annealing (RTA). Figure 5 sketches the data flow from density-functional theory (DFT) to atomistic analysis.

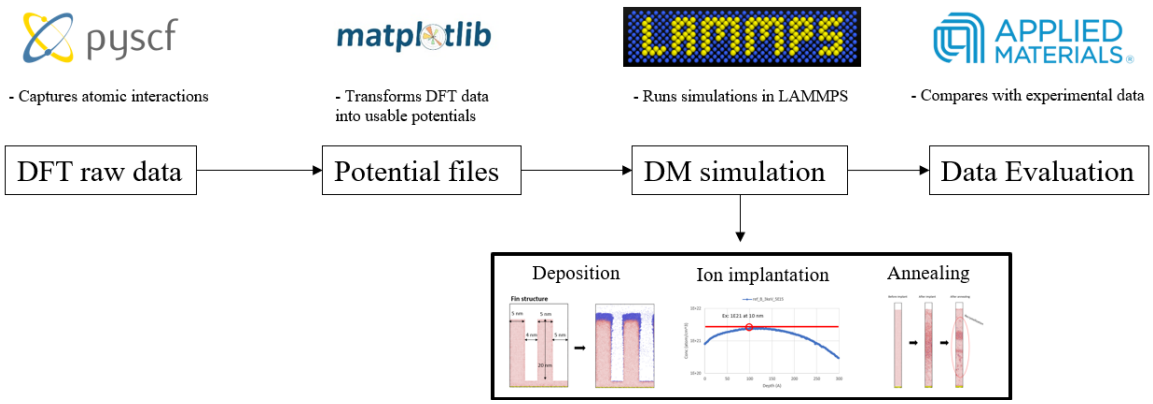


Figure 5. The flow chart of the simulation for multi-process model development

3.2.1 Density function theory for Si-B interaction

A GGA-PBE functional with a TZVP basis set was used in PySCF v2.5 to calculate the potential energy surface (PES) of isolated *Si–B* and *B–B* pairs. Crystallized Si atoms plus one B atom were strained along the pair axis from 1.8 Å to 5.0 Å in 0.1 Å increments. All structures were spin-polarized and converged to 10^{-8} Ha.

The DFT energies were fitted to a 12-6 Lennard-Jones (LJ) form, $U_{ij}(r) = 4\varepsilon_{ij}\left[\left(\frac{\sigma_{ij}}{r}\right)^{12} - \left(\frac{\sigma_{ij}}{r}\right)^{6}\right]$, using nonlinear least squares ($R^2 > 0.995$). The resulting

parameters (Table 1) are used unchanged in the MD simulations. Convergence tests (basis-set size, k-point mesh) changed by < 2 %.

Table 15. The LJ parameters of Si-B and B-B interactions

Pair	E (eV)	σ (Å)
Si-B	3.5	1.44
B-B	2.98	1.26

3.2.2 MD model construction

Simulations were performed with LAMMPS compiled in double precision. The substrate is a $10 \times 10 \times 30$ nm³ diamond structure Si cell (~300 000 atoms) with periodic x and y boundaries; the bottom 0.5 nm is fixed to mimic semi-infinite bulk. The hybrid potential comprises the Tersoff Si–Si parameters and the DFT-derived LJ terms for B-containing pairs via pair_style hybrid/overlay. Long-range Coulomb forces are not required at the low implantation energies considered. After energy minimization, the lattice is equilibrated at 300 K under an NVT Nose–Hoover thermostat (damping 100 fs) with a 0.05 fs time-step.

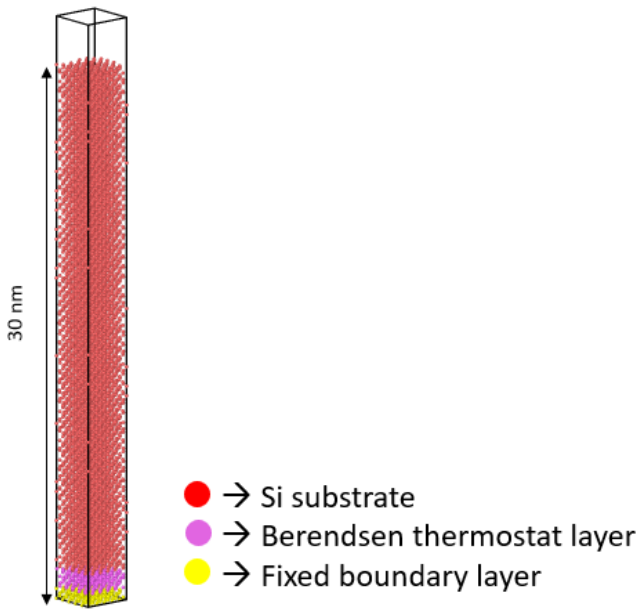


Figure 6. The ion implantation model

3.2.3 Ion implantation protocol

Boron ion was implanted at a nominal energy of 3 keV. To minimize crystallographic channeling, the beam was directed 7° off the normal surface. Implantation simulations were performed for two different doses: 1×10^{16} cm^{-2} and 5×10^{15} cm^{-2}. In both cases, boron ions were introduced individually, with the system equilibrated to thermal stability following each implantation step before proceeding to the next ion. This pacing prevents artificial cell heating and allows local dynamic annealing to proceed between impacts. Ions were introduced 3 nm above the surface with velocities drawn from a Maxwellian distribution consistent with the beam energy, using LAMMPS fix deposit. Throughout implantation, the bottom 2 nm of the substrate was coupled to a 300 K Nose–Hoover thermostat to act as a heat sink, whereas the remainder of the cell evolved micro-canonically so that thermal collision cascades were captured without thermostat interference. An adaptive time-step control (fix dt/reset) limited the per-atom kinetic energy increment to 0.1 eV per step, ensuring numerical stability during high-energy recoils. On the other hand, to increase the concentration of near surface area. A 0.5–1.5 nm amorphous B enriched film, was first deposited under 300 K followed by the Boron ion implantation.

3.2.4 Rapid thermal annealing

Postimplant configurations were heated from 300 K to 1223 K (950 °C) over 50 ps, held for 250 ps, and quenched to 300 K in 200 ps under an NVT ensemble with 100 fs damping. The timestep was reduced to 0.25 fs during ramp phases to maintain energy conservation. Defect evolution was probed *in situ* by performing a Wigner–Seitz cell occupation analysis, allowing real-time quantification of both vacancy and self-interstitial populations as the lattice recrystallized.

3.3 Results and discussion

3.3.1 Validation of the DFT-derived Si-B Lennard-Jones potential

Figure 7 presents the Density Functional Theory (DFT)-calculated reference energies for Si–B and B–B dimers, alongside the corresponding fitted 12-6 Lennard-Jones (LJ) potential curves. The LJ form accurately reproduces the short-range repulsive wall below 1.3 Å within 0.03 eV and locates the potential minimum within 0.02 Å of the DFT result, demonstrating a high level of agreement.

The derived Lennard-Jones parameters for the Si–B interaction are a well depth (ε) of 3.5 eV and a zero-crossing distance (σ) of 1.44 Å. For B–B interactions, ε and σ are determined to be 2.98 eV and 1.26 Å, respectively. These parameters are essential for accurately describing interatomic forces in molecular dynamics simulations, especially under non-equilibrium conditions such as ion implantation.

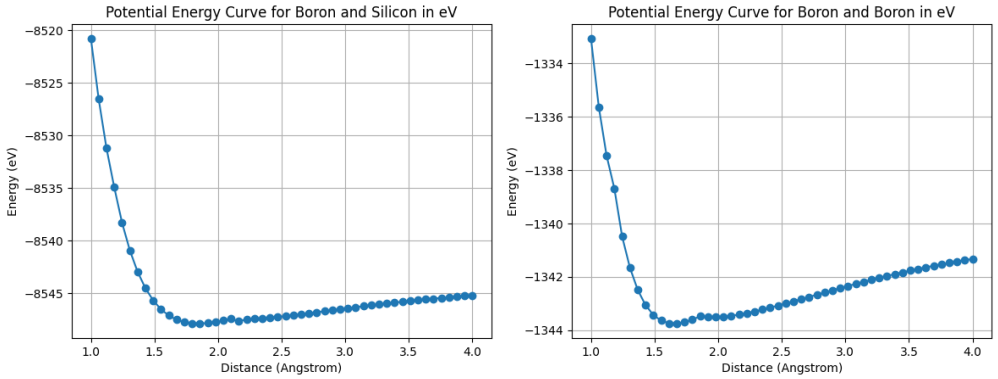


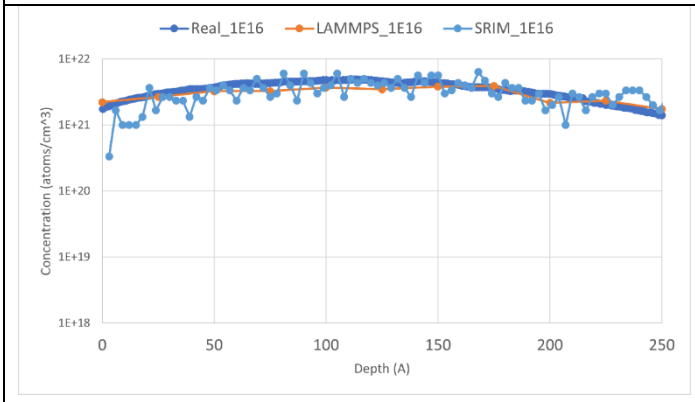
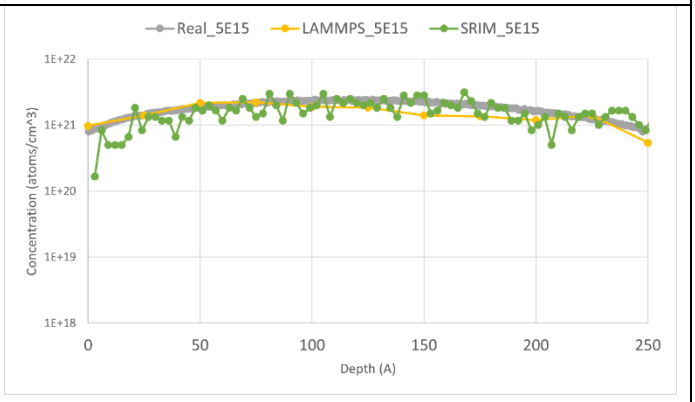
Figure 7. the DFT calculated LJ potential for (a) Si and B (b) B and B

3.3.2 Boron implantation depth profile versus SIMS and SRIM

The as-implanted boron concentration profiles obtained from LAMMPS, SRIM2013, and experimental secondary-ion mass spectrometry (SIMS) are compared in Table 16 for two doses: 5×10^{15} cm^{-2} and 1×10^{16} cm^{-2} at 3 keV. In the near-surface window (0–15 nm) the LAMMPS curve tracks SIMS to within ±5 %, whereas SRIM overshoots the peak by ≈12 % and underestimates the low-energy tail. Quantitatively, the

root-mean-square deviation (RMSD) between LAMMPS and SIMS in the 0–150 Å range is 3.1×10^{19} cm^{-3}, more than a factor of two lower than the SRIM–SIMS RMSD (6.9×10^{19} cm^{-3}). This improvement stems from the explicit treatment of dynamic annealing and defect recombination during the MD trajectory, effects that are absent from the binary-collision approximation used in SRIM.

Table 16. The concentration profile of Boron implanted Si substrates in different doses.

Implanted dose equal to 1E16	Implanted dose equal to 5E15
	

3.3.3 Impact of an amorphous-boron cap on implant profile

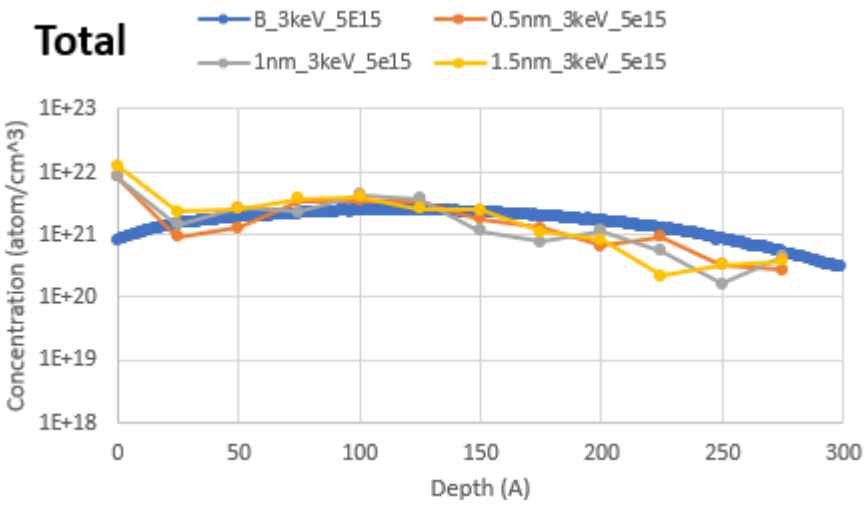
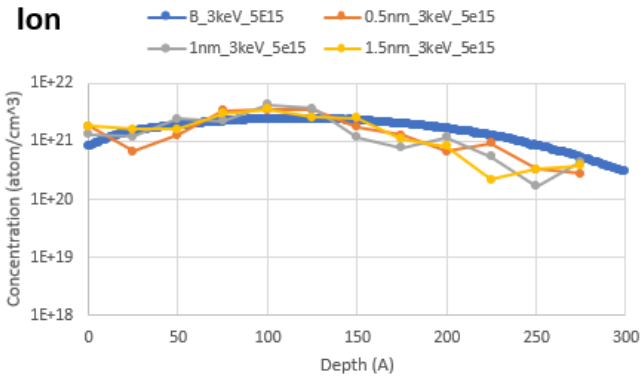
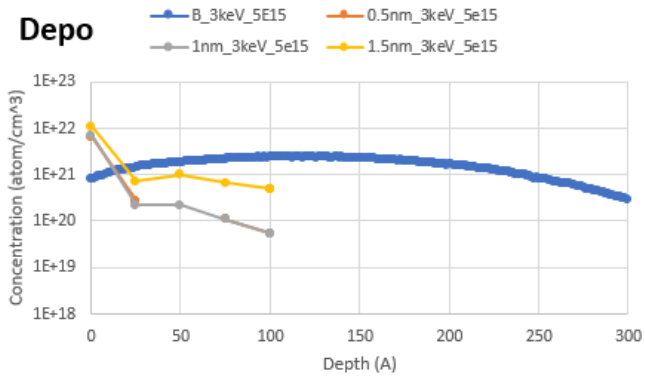
For lightly-doped-drain (LDD) transistors, the ideal junction features a very high dopant concentration in the first few nanometers—to minimize contact resistance—followed by a rapid roll-off to a low background level that suppresses short-channel leakage. To meet this requirement, we deposited a conformal amorphous-boron (a-B) overlayer at 300 K before ion implantation, creating a sacrificial dopant reservoir that is consumed by the ensuing implant and anneal sequence.

Table 17 compares three cap thicknesses (0.5, 1.0, and 1.5 nm). A 1.0 nm a-B layer increases the near-surface plateau by ≈ 35 % without extending the 10 % tail depth, whereas a 1.5 nm cap widens the junction by ≈ 1.2 nm, eroding lateral abruptness. Table 3 summarizes the trade-off: a cap of 1.0 ± 0.2 nm delivers the steepest 10–90 %

junction together with the lowest calculated sheet resistance, making it the optimal compromise for p-type LDD targets.

These results demonstrate that pre-implant boron deposition is an effective knob for independently boosting surface dose while protecting junction abruptness, enabling tighter control of LDD profiles than can be achieved with implantation parameters alone.

Table 17. the effect on concentration profile with various deposited boron layers

<table>
<tr><td colspan="2">Total boron concentration profile</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Ion implanted boron concentration profile</td><td>Deposited boron concentration profile</td></tr>
<tr><td> 
</td><td> 
</td></tr>
</table>

3.3.4 Defect evolution during rapid-thermal annealing

Wigner–Seitz analysis was used to track the populations of vacancies and self-interstitials as a function of anneal duration, where the thermal profile (300 K → 950 °C → 300 K) was identically ramped, but the isothermal hold was varied from 4 M to 16 M molecular-dynamics steps. The initial, as-implanted lattice contained 2589 vacancies and 2861 interstitials shown as Table 18. Extending the hold to 6 M steps reduced these defects by 23 % and 21 %, respectively, while an 8 M-step treatment achieved the deepest anneal, lowering the vacancy count to 1395 and the interstitial count to 1667. Beyond this optimum, defects began to re-emerge: at 10 M steps the vacancy and interstitial populations rebounded by ~26 %, and by 16 M steps they exceeded the 4 M-step baseline by ≈10 %, indicating that over-annealing can generate defects due to higher kinetic energy for the dopants. These results underscore that a narrowly tuned spike—equivalent to 8 ± 2 M MD steps under the present thermal budget—maximizes recrystallisation while avoiding the defect re-generation that accompanies prolonged high-temperature exposure.

Table 18. The defect analysis of different RTA methods

Anneal Conditions	**Vacancy**	**Interstitial**	**Reduced Vacancy (%)**	**Reduced Interstitial (%)**
4 M steps	2589	2861	Reference	Reference
6 M steps	1992	2264	-23.06%	-20.87%
8 M steps	1395	1667	-46.12%	-41.73%
10 M steps	1756	2028	-32.16%	-29.11%
16 M steps	2840	3112	+9.69%	+8.77%

3.4 Conclusion

This work establishes a quantum-informed, multi-process molecular-dynamics framework that extends the fidelity of dopant-process simulation well beyond the reach of traditional continuum TCAD. By parameterizing B–Si and B–B interactions with DFT-derived 12-6 Lennard-Jones terms and combining them with a many-body Tersoff description of the Si lattice, we obtain a transferable hybrid potential that faithfully captures both collision cascades and post-impact lattice chemistry. Large-scale LAMMPS simulations reproduce 3 keV boron SIMS profiles for 1×10^{16} cm^{-2} and 5×10^{15} cm^{-2} implants to within ± 5 % over the 0–15 nm window, outperforming SRIM by more than a factor of two in RMS error. Introducing a 1 nm amorphous B-rich pre-deposition layer boosts the surface plateau by ≈ 35 % without widening the 10–90 % junction—demonstrating how the platform can evaluate coupled deposition + implant recipes that are impractical to explore experimentally or with BCA models.

Rapid-thermal annealing simulations further show that a narrowly tuned spike (≈ 8 M MD steps at 950 °C) removes ~46 % of vacancies and ~42 % of interstitials while deeper holds induce defect regeneration; the model therefore captures the competing kinetics of recrystallisation and defect re-nucleation that govern ultra-shallow junction integrity. Because implantation, pre-deposition and annealing are executed in a single atomistic workflow driven by first-principles energetics, process engineers can vary dose, energy, capping thickness and thermal budget within one predictive environmental level of integration unavailable in commercial tools.

In short, the present framework delivers (i) sub-nanometer accuracy in junction profiling, (ii) explicit tracking of implantation-induced defect chemistry, and (iii) seamless coupling of sequential fabrication steps inside a unified simulation engine. These capabilities open a path to co-optimize LDD formation across multiple knobs—implant parameters, surface treatments, and millisecond anneals—before silicon is

ever processed. Future extensions will integrate accelerated MD and kinetic-Monte-Carlo staging to reach millisecond-to-second time scales and expand the chemistry set to heavier p- and n-type dopants, paving the way for predictive, automictically informed design of next-generation CMOS junctions.

REFERENCES

1. Rajasekhar, A., B. Gimi, and W. Hu, *Applications of semiconductor fabrication methods to nanomedicine: a review of recent inventions and techniques.* Recent patents on nanomedicine, 2013. **3**(1): p. 9-20.

2. Pabst, D., et al. *Deterministic scheduling of wafer fab operations*. in *Proceedings of the Brooks Worldwide Automation Symposium*. 2003.

3. Jain, M. and N. Jain, *Recent Developments in Semiconductor Wafer Fabrication: Materials, Processes, and Innovations.* 2025.

4. Bratton, D., et al., *Recent progress in high resolution lithography.* Polymers for advanced technologies, 2006. **17**(2): p. 94-103.

5. Pimpin, A. and W. Srituravanich, *Review on micro-and nanolithography techniques and their applications.* Engineering journal, 2012. **16**(1): p. 37-56.

6. Rothschild, M. *Photolithography at wavelengths below 200 nm*. in *Technical Digest. Summaries of Papers Presented at the Conference on Lasers and Electro-Optics. Conference Edition. 1998 Technical Digest Series, Vol. 6 (IEEE Cat. No. 98CH36178)*. 1998. IEEE.

7. Liberman, V., et al., *Prospects for photolithography at 121 nm.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2002. **20**(6): p. 2567-2573.

8. Tallents, G., E. Wagenaars, and G. Pert, *Lithography at EUV wavelengths.* Nature photonics, 2010. **4**(12): p. 809-811.

9. Mojarad, N., J. Gobrecht, and Y. Ekinci, *Interference lithography at EUV and soft X-ray wavelengths: Principles, methods, and applications.* Microelectronic Engineering, 2015. **143**: p. 55-63.

10. Fu, N., et al., *EUV lithography: State-of-the-art review.* J. Microelectron. Manuf, 2019. **2**(2): p. 1-6.

11. Wu, B. and A. Kumar, *Extreme ultraviolet lithography: A review.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2007. **25**(6): p. 1743-1761.

12. Lio, A., *EUV photoresists: A progress report and future prospects.* Synchrotron Radiation News, 2019. **32**(4): p. 9-14.

13. Jeong, S.-J., et al., *Directed self-assembly of block copolymers for next generation nanolithography.* Materials today, 2013. **16**(12): p. 468-476.

14. Hu, H., M. Gopinadhan, and C.O. Osuji, *Directed self-assembly of block copolymers: a tutorial review of strategies for enabling nanotechnology with soft matter.* Soft matter, 2014. **10**(22): p. 3867-3889.

15. Morris, M., *Directed self-assembly of block copolymers for nanocircuitry fabrication.* Microelectronic Engineering, 2015. **132**: p. 207-217.

16. Pinto-Gómez, C., et al., *Directed self-assembly of block copolymers for the fabrication of functional devices.* Polymers, 2020. **12**(10): p. 2432.

17. Van Bel, J., et al., *Rectification of extreme ultraviolet lithography patterns by directed self-assembly: a roughness and defectivity study.* Journal of Micro/Nanopatterning, Materials, and Metrology, 2024. **23**(4): p. 043001-043001.

18. Stolk, P.A., et al., *Physical mechanisms of transient enhanced dopant diffusion in ion-implanted silicon.* Journal of Applied Physics, 1997. **81**(9): p. 6031-6050.

19. Rudan, M. and M. Rudan, *Thermal diffusion—Ion implantation.* Physics of Semiconductor Devices, 2018: p. 673-701.

20. Nastasi, M.A. and J.W. Mayer, *Ion implantation and synthesis of materials*. Vol. 5. 2006: Springer.

21. Hernández-Mangas, J., et al., *Improved binary collision approximation ion implant simulators.* Journal of applied physics, 2002. **91**(2): p. 658-667.

22. Simoen, E., et al., *Ion-implantation issues in the formation of shallow junctions in germanium.* Materials science in semiconductor processing, 2006. **9**(4-5): p. 634-639.

23. Satta, A., et al., *Shallow junction ion implantation in Ge and associated defect control.* Journal of The Electrochemical Society, 2006. **153**(3): p. G229.

24. Prussin, S., D.I. Margolese, and R.N. Tauber, *Formation of amorphous layers by ion implantation.* Journal of applied physics, 1985. **57**(2): p. 180-185.

25. Williams, J., *Ion implantation of semiconductors.* Materials Science and Engineering: A, 1998. **253**(1-2): p. 8-15.

26. Kalbitzer, S., et al., *The effects of ion implantation on the electrical properties of amorphous silicon.* Philosophical Magazine B, 1980. **41**(4): p. 439-456.

27. Adekoya, W., J. Muller, and P. Siffert, *Rapid thermal annealing of electrically-active defects in virgin and implanted silicon.* Applied Physics A, 1987. **42**(3): p. 227-232.

28. Fair, R.B., *Modeling of dopant diffusion during rapid thermal annealing.* Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 1986. **4**(3): p. 926-932.

29. Kim, Y., H.Z. Massoud, and R.B. Fair, *The Effect of Annealing Ambient on Dopant Diffusion in Silicon during Low-Temperature Processing.* Journal of The Electrochemical Society, 1990. **137**(8): p. 2599.

30. Brown, W., W. Augustyniak, and T. Waite, *Annealing of radiation defects in semiconductors.* Journal of Applied Physics, 1959. **30**(8): p. 1258-1268.

31. Gunawan, R., et al., *Optimal control of rapid thermal annealing in a semiconductor process.* Journal of Process Control, 2004. **14**(4): p. 423-430.

32. Hill, C., S. Jones, and D. Boys, *Rapid thermal annealing-theory and practice*, in *Reduced thermal processing for ULSI*. 1989, Springer. p. 143-180.

33. Seidel, T., et al., *A review of rapid thermal annealing (RTA) of B, BF 2 and As ions implanted into silicon.* Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 1985. **7**: p. 251-260.

34. Kwok, C.T.M., et al., *Mechanistic benefits of millisecond annealing for diffusion and activation of boron in silicon.* Journal of Applied Physics, 2009. **105**(6).

35. Timans, P., et al., *Millisecond annealing: Past, present and future.* MRS Online Proceedings Library (OPL), 2006. **912**: p. 0912-C01-01.

36. Feng, L.M., Y. Wang, and D.A. Markle. *Minimizing pattern dependency in millisecond annealing*. in *2006 International Workshop on Junction Technology*. 2006. IEEE.

37. Michalak, T.J., et al., *Study of millisecond laser annealing on recrystallization, activation, and mobility of laser annealed SOI doped via arsenic ion implantation.* Journal of Vacuum Science & Technology B, 2014. **33**(1).

38. Timans, P., et al., *Optimization of diffusion, activation and damage annealing in millisecond annealing*. 2008. 65-87.

39. Carlsson, J.-O. and P.M. Martin, *Chemical vapor deposition*, in *Handbook of Deposition Technologies for films and coatings*. 2010, Elsevier. p. 314-363.

40. Sreenivasan, R., R.A. Adomaitis, and G.W. Rubloff, *Demonstration of spatially programmable chemical vapor deposition: Model-based uniformity/ nonuniformity control.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2006. **24**(6): p. 2706-2715.

41. Choy, K.L., *Chemical vapour deposition of coatings.* Progress in Materials Science, 2003. **48**(2): p. 57-170.

42. Helmersson, U., et al., *Ionized physical vapor deposition (IPVD): A review of technology and applications.* Thin Solid Films, 2006. **513**(1): p. 1-24.

43. Rossnagel, S.M., *Thin film deposition with physical vapor deposition and related technologies.* Journal of Vacuum Science & Technology A, 2003. **21**(5): p. S74-S87.

44. Lin, M., et al., *Sandwich-structured polymer dielectrics exhibiting significantly improved capacitive performance at high temperatures by roll-to-roll physical vapor deposition.* Chemical Engineering Journal, 2024. **498**: p. 155586.

45. Johnson, R.W., A. Hultqvist, and S.F. Bent, *A brief review of atomic layer deposition: from fundamentals to applications.* Materials Today, 2014. **17**(5): p. 236-246.

46. Hackley, J.C. and T. Gougousi, *Properties of atomic layer deposited HfO2 thin films.* Thin Solid Films, 2009. **517**(24): p. 6576-6583.

47. Xie, S., et al., *Atomic Layer-by-Layer Deposition of Pt on Pd Nanocubes for Catalysts with Enhanced Activity and Durability toward Oxygen Reduction.* Nano Letters, 2014. **14**(6): p. 3570-3576.

48. Elers, K.-E., et al., *Film Uniformity in Atomic Layer Deposition.* Chemical Vapor Deposition, 2006. **12**(1): p. 13-24.

49. Dalapati, G.K., et al., *Electrical and Interfacial Characterization of Atomic Layer Deposited High- κ Gate Dielectrics on GaAs for Advanced CMOS Devices.* IEEE Transactions on Electron Devices, 2007. **54**(8): p. 1831-1837.

50. Li, Y., et al., *FEOL CMP modeling challenges and solution in 3D NAND*. SPIE Advanced Lithography. Vol. 10962. 2019: SPIE.

51. Singh, G., A.M. Waas, and V. Sundararaghavan, *Understanding defect structures in nanoscale metal additive manufacturing via molecular dynamics.* Computational Materials Science, 2021. **200**: p. 110807.

52. Nordlund, K., F. Djurabekova, and G. Hobler, *Large fraction of crystal directions leads to ion channeling.* Physical Review B, 2016. **94**(21): p. 214109.

53. Thompson, A.P., et al., *LAMMPS - a flexible simulation tool for particle-based materials modeling at the atomic, meso, and continuum scales.* Computer Physics Communications, 2022. **271**: p. 108171.

54. Gowthaman, S., *A review on mechanical and material characterisation through molecular dynamics using large-scale atomic/molecular massively parallel simulator (LAMMPS).* Functional Composites and Structures, 2023. **5**(1): p. 012005.

55. Nikolskiy, V., D. Pavlov, and V. Stegailov. *State-of-the-Art Molecular Dynamics Packages for GPU Computations: Performance, Scalability and Limitations*. in *Supercomputing*. 2022. Cham: Springer International Publishing.

56. Matsunaga, K., C. Fisher, and H. Matsubara, *Tersoff Potential Parameters for Simulating Cubic Boron Carbonitrides.* Japanese Journal of Applied Physics, 2000. **39**(1A): p. L48.

57. Vink, R.L.C., et al., *Fitting the Stillinger–Weber potential to amorphous silicon.* Journal of Non-Crystalline Solids, 2001. **282**(2): p. 248-255.

58. Tang, M., et al., *Intrinsic point defects in crystalline silicon: Tight-binding molecular dynamics studiesof self-diffusion, interstitial-vacancy recombination, and formation volumes.* Physical Review B, 1997. **55**(21): p. 14279-14289.

59. Matsuo, J., et al., *Ultra Shallow Junction Formation by Cluster Ion Implantation.* MRS Online Proceedings Library, 1998. **532**(1): p. 17-22.

60. Kyrychenko, A., Y. Stepanenko, and J. Waluk, *Molecular Dynamics and DFT Studies of Intermolecular Hydrogen Bonds between Bifunctional Heteroazaaromatic Molecules and Hydroxylic Solvents.* The Journal of Physical Chemistry A, 2000. **104**(42): p. 9542-9555.

61. Tran, B., S.T. Milner, and M.J. Janik, *Kinetics of Acid-Catalyzed Dehydration of Alcohols in Mixed Solvent Modeled by Multiscale DFT/MD.* ACS Catalysis, 2022. **12**(21): p. 13193-13206.

62. Joshi, S.Y. and S.A. and Deshmukh, *A review of advancements in coarse-grained molecular dynamics simulations.* Molecular Simulation, 2021. **47**(10-11): p. 786-803.

63. Liwo, A., et al., *Theory and Practice of Coarse-Grained Molecular Dynamics of Biologically Important Systems.* Biomolecules, 2021. **11**(9): p. 1347.

64. Rudd, R.E. and J.Q. Broughton, *Coarse-grained molecular dynamics and the atomic limit of finite elements.* Physical Review B, 1998. **58**(10): p. R5893-R5896.

65. Park, S.J., et al., *Self-consistent field theory and coarse-grained molecular dynamics simulations of pentablock copolymer melt phase behavior.* Molecular Systems Design & Engineering, 2024. **9**(12): p. 1235-1253.

66. Shkurti, A., et al., *Acceleration of coarse grain molecular dynamics on GPU architectures.* Journal of Computational Chemistry, 2013. **34**(10): p. 803-818.

67. Root, S.E., et al., *Predicting the Mechanical Properties of Organic Semiconductors Using Coarse-Grained Molecular Dynamics Simulations.* Macromolecules, 2016. **49**(7): p. 2886-2894.

68. Jackson, N.E., *Coarse-Graining Organic Semiconductors: The Path to Multiscale Design.* The Journal of Physical Chemistry B, 2021. **125**(2): p. 485-496.

69. Zhang, P., et al., *Multiscale Particle-Based Modeling of Flowing Platelets in Blood Plasma Using Dissipative Particle Dynamics and Coarse Grained Molecular Dynamics.* Cellular and Molecular Bioengineering, 2014. **7**(4): p. 552-574.

70. Curk, T., *Dissipative particle dynamics for coarse-grained models.* The Journal of Chemical Physics, 2024. **160**(17).

71. Orio, M., D.A. Pantazis, and F. Neese, *Density functional theory.* Photosynthesis Research, 2009. **102**(2): p. 443-453.

72. Jiang, J., et al., *Time-dependent density functional theory for ion diffusion in electrochemical systems.* Journal of Physics: Condensed Matter, 2014. **26**(28): p. 284102.

73. Jones, R., et al., *Self-interstitial clusters in silicon.* Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 2002. **186**(1): p. 10-18.

74. JÓNSSON, H., G. MILLS, and K.W. JACOBSEN, *Nudged elastic band method for finding minimum energy paths of transitions*, in *Classical and Quantum Dynamics in Condensed Phase Simulations*. p. 385-404.

75. Rahman, M.H., M. Biswas, and A. Mannodi-Kanakkithodi, *Understanding Defect-Mediated Ion Migration in Semiconductors using Atomistic Simulations and Machine Learning.* ACS Mater Au, 2024. **4**(6): p. 557-573.

76. Ahmad, A., et al., *A DFT-based kinetic Monte Carlo simulation of multiphase oxide-metal thin film growth.* Journal of Applied Physics, 2024. **135**.

77. Sibanda, D., S.T. Oyinbo, and T.-C. Jen, *A review of atomic layer deposition modelling and simulation methodologies: Density functional theory and molecular dynamics.* Nanotechnology Reviews, 2022. **11**(1): p. 1332-1363.

78. Fang, G., et al., *Theoretical design and computational screening of precursors for atomic layer deposition.* Coordination Chemistry Reviews, 2016. **322**: p. 94-103.

79. Rignanese, G.M., *Dielectric properties of crystalline and amorphous transition metal oxides and silicates as potential high-κ candidates: the contribution of density-functional theory.* Journal of Physics: Condensed Matter, 2005. **17**(7): p. R357.

80. Tunega, D., T. Bučko, and A. Zaoui, *Assessment of ten DFT methods in predicting structures of sheet silicates: Importance of dispersion corrections.* The Journal of Chemical Physics, 2012. **137**(11).

81. Jain, A., Y. Shin, and K.A. Persson, *Computational predictions of energy materials using density functional theory.* Nature Reviews Materials, 2016. **1**(1): p. 15004.

82. Cohen, A.J., P. Mori-Sánchez, and W. Yang, *Insights into Current Limitations of Density Functional Theory.* Science, 2008. **321**(5890): p. 792-794.

83. Boisse, J., C. Domain, and C.S. Becquart, *Modelling self trapping and trap mutation in tungsten using DFT and Molecular Dynamics with an empirical potential based on DFT.* Journal of Nuclear Materials, 2014. **455**(1): p. 10-15.

84. Hernández, N.C. and J.F. Sanz, *From periodic DFT calculations to classical molecular dynamics simulations.* Computational Materials Science, 2006. **35**(3): p. 183-186.

85. Doumont, J., F. Tran, and P. Blaha, *Limitations of the DFT--1/2 method for covalent semiconductors and transition-metal oxides.* Physical Review B, 2019. **99**(11): p. 115101.

86. Schuch, N. and F. Verstraete, *Computational complexity of interacting electrons and fundamental limitations of density functional theory.* Nature Physics, 2009. **5**(10): p. 732-735.

87. Wang, Y., et al., *A Multiscale Simulation on Aluminum Ion Implantation-Induced Defects in 4H-SiC MOSFETs.* Electronics, 2024. **13**(14): p. 2758.

88. Sebastian, E.M., et al., *Nanolithography and its current advancements.* Materials Today: Proceedings, 2020. **26**: p. 2351-2356.

89. Nishimura, Y., et al., *Photolithography*, in *Flat Panel Display Manufacturing*. 2018. p. 287-310.

90. Ober, C., et al., *EUV photolithography: resist progress and challenges*. SPIE Advanced Lithography. Vol. 10583. 2018: SPIE.

91. Smith, M., et al., *Comprehensive EUV lithography model*. SPIE Advanced Lithography. Vol. 7969. 2011: SPIE.

92. Ha, D., et al. *Highly manufacturable 7nm FinFET technology featuring EUV lithography for low power and high performance applications*. in *2017 Symposium on VLSI Technology*. 2017.

93. Ji, S., et al., *Directed self-assembly of block copolymers on chemical patterns: A platform for nanofabrication.* Progress in Polymer Science, 2016. **54-55**: p. 76-127.

94. Mai, Y. and A. Eisenberg, *Self-assembly of block copolymers.* Chem Soc Rev, 2012. **41**(18): p. 5969-85.

95. Wang, X., et al., *Morphologies of block copolymers composed of charged and neutral blocks.* Soft Matter, 2012. **8**(11): p. 3036-3052.

96. Rincon Delgadillo, P., et al., *Process sensitivities in exemplary chemo-epitaxy directed self-assembly integration*. SPIE Advanced Lithography. Vol. 8680. 2013: SPIE.

97. Rincon Delgadillo, P., et al., *Implementation of a chemo-epitaxy flow for directed self-assembly on 300-mm wafer processing equipment.* Journal of Micro/Nanolithography, MEMS, and MOEMS, 2012. **11**(3): p. 031302.

98. Segalman, R.A., H. Yokoyama, and E.J. Kramer, *Graphoepitaxy of Spherical Domain Block Copolymer Films.* Advanced Materials, 2001. **13**(15): p. 1152-1155.

99. Bita, I., et al., *Graphoepitaxy of Self-Assembled Block Copolymers on Two-Dimensional Periodic Patterned Templates.* Science, 2008. **321**(5891): p. 939-943.

100. FrantzDale, B., S.J. Plimpton, and M.S. Shephard, *Software components for parallel multiscale simulation: an example with LAMMPS.* Engineering with Computers, 2010. **26**(2): p. 205-211.

101. Takada, S., *Coarse-grained molecular simulations of large biomolecules.* Curr Opin Struct Biol, 2012. **22**(2): p. 130-7.

102. Marchetto, A., et al., *CGMD Platform: Integrated Web Servers for the Preparation, Running, and Analysis of Coarse-Grained Molecular Dynamics Simulations.* Molecules, 2020. **25**(24).

103. Ries, M., et al., *Extensive CGMD Simulations of Atactic PS Providing Pseudo Experimental Data to Calibrate Nonlinear Inelastic Continuum Mechanical Constitutive Laws.* Polymers, 2019. **11**(11): p. 1824.

104. Groot, R.D. and P.B. Warren, *Dissipative particle dynamics: Bridging the gap between atomistic and mesoscopic simulation.* The Journal of Chemical Physics, 1997. **107**(11): p. 4423-4435.

105. Moeendarbary, E., T.Y. Ng, and M. Zangeneh, *Dissipative particle dynamics: introduction, methodology and complex fluid applications—a review.* International Journal of Applied Mechanics, 2009. **1**(04): p. 737-763.

106. Liu, M., et al., *Dissipative particle dynamics (DPD): an overview and recent developments.* Archives of Computational Methods in Engineering, 2015. **22**: p. 529-556.

107. Pinge, S., et al., *Three-dimensional line edge roughness in pre-and post-dry etch line and space patterns of block copolymer lithography.* Physical Chemistry Chemical Physics, 2020. **22**(2): p. 478-488.

108. Shebert, G.L. and Y.L. Joo, *Simultaneous uniaxial extensional deformation and cylindrical confinement of block copolymers using non-equilibrium molecular dynamics.* Soft Matter, 2018. **14**(8): p. 1389-1396.

109. Pinge, S., et al., *Designing an ordered template of cylindrical arrays based on a simple flat plate confinement of block copolymers: a coarse-grained molecular dynamics study.* Soft Matter, 2018. **14**(4): p. 597-613.

110. Hoogerbrugge, P. and J. Koelman, *Simulating microscopic hydrodynamic phenomena with dissipative particle dynamics.* Europhysics letters, 1992. **19**(3): p. 155.

111. Koelman, J. and P. Hoogerbrugge, *Dynamic simulations of hard-sphere suspensions under steady shear.* Europhysics letters, 1993. **21**(3): p. 363.

112. Ma, Y., et al., *Dissipative particle dynamics and molecular dynamics simulations on mesoscale structure and proton conduction in a SPEEK/PVDF-g-PSSA membrane.* RSC Advances, 2017. **7**(63): p. 39676-39684.

113. Flekkøy, E.G., P.V. Coveney, and G. De Fabritiis, *Foundations of dissipative particle dynamics.* Physical Review E, 2000. **62**(2): p. 2140-2157.

114. Steinhardt, P.J., D.R. Nelson, and M. Ronchetti, *Bond-orientational order in liquids and glasses.* Physical Review B, 1983. **28**(2): p. 784-805.

115. Mickel, W., et al., *Shortcomings of the bond orientational order parameters for the analysis of disordered particulate matter.* The Journal of Chemical Physics, 2013. **138**(4).

116. Haeberle, J., M. Sperl, and P. Born, *Distinguishing noisy crystalline structures using bond orientational order parameters.* The European Physical Journal E, 2019. **42**(11): p. 149.

117. Muramatsu, M., et al. *Defect and roughness reduction of chemo-epitaxy DSA pattern*. in *Novel Patterning Technologies 2018*. 2018. SPIE.

118. Madkhali, O., *A review of novel methods to improve the optical and electrical properties of n-type and p-type sulphides and oxides: leading the frontiers of semiconductor technology.* Physica Scripta, 2024. **99**(2): p. 022004.

119. Scaccabarozzi, A.D., et al., *Doping Approaches for Organic Semiconductors.* Chemical Reviews, 2022. **122**(4): p. 4420-4492.

120. Jain, A., J.J. Chambers, and J.B. Shaw, *Advancement of CMOS Doping Technology in an External Development Framework.* AIP Conference Proceedings, 2011. **1321**(1): p. 31-36.

121. Ogura, S., et al., *Design and characteristics of the lightly doped drain-source (LDD) insulated gate field-effect transistor.* IEEE Transactions on Electron Devices, 1980. **27**(8): p. 1359-1367.

122. Liou, J.J., A. Ortiz-Conde, and F. Garcia-Sanchez, *Parameter extraction of lightly-doped drain (LDD) MOSFETs*, in *Analysis and Design of Mosfets: Modeling, Simulation and Parameter Extraction*, J.J. Liou, A. Ortiz-Conde, and F. Garcia-Sanchez, Editors. 1998, Springer US: Boston, MA. p. 291-326.

123. PEARTON, S.J., *ION IMPLANTATION IN III–V SEMICONDUCTOR TECHNOLOGY.* International Journal of Modern Physics B, 1993. **07**(28): p. 4687-4761.

124. Song, J.-H., et al., *Electrical Properties of Ultra Shallow p Junction on n type Si Wafer Using Decaborane Ion Implantation.* MRS Online Proceedings Library, 2011. **686**(1): p. 35.

125. Kaga, T. and Y. Sakai, *Effects of lightly doped drain structure with optimum ion dose on p-channel MOSFETs.* IEEE Transactions on Electron Devices, 1988. **35**(12): p. 2384-2390.

126. Ihara, S., S. Itoh, and J.i. Kitakami, *Mechanisms of cluster implantation in silicon: A molecular-dynamics study.* Physical Review B, 1998. **58**(16): p. 10736-10744.

127. Matsuo, J., et al., *Ultra Shallow Junction Formation by Cluster Ion Implantation.* MRS Proceedings, 1998. **532**: p. 17.

128. Collart, E.J.H., et al., *Cluster formation during annealing of ultra-low-energy boron-implanted silicon.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2000. **18**(1): p. 435-439.

129. Felch, S.B., et al., *Plasma doping for the fabrication of ultra-shallow junctions.* Surface and Coatings Technology, 2002. **156**(1): p. 229-236.

130. Cuiyang, W., et al. *A plasma doping process for 3D finFET source/drain extensions*. in *2014 20th International Conference on Ion Implantation Technology (IIT)*. 2014.

131. Barnett, J., et al. *Advanced techniques for achieving ultra-shallow junctions in future CMOS devices*. in *2010 International Workshop on Junction Technology Extended Abstracts*. 2010.

132. Colombeau, B., et al., *Ultra-Shallow Junction Formation—Physics and Advanced Technology.* AIP Conference Proceedings, 2008. **1066**(1): p. 11-18.

133. Parihar, M.S., D. Ghosh, and A. Kranti, *Ultra Low Power Junctionless MOSFETs for Subthreshold Logic Applications.* IEEE Transactions on Electron Devices, 2013. **60**(5): p. 1540-1546.

134. Liu, R., et al., *The effects of rapid thermal processing on ultra-shallow junctions for deep sub-micron MOSFETs.* Solid-State Electronics, 1995. **38**(8): p. 1473-1477.

135. Simoen, E., et al., *Ion-implantation issues in the formation of shallow junctions in germanium.* Materials Science in Semiconductor Processing, 2006. **9**(4): p. 634-639.

136. Napolitani, E. and G. Impellizzeri, *Chapter Three - Ion Implantation Defects and Shallow Junctions in Si and Ge*, in *Semiconductors and Semimetals*, L. Romano, V. Privitera, and C. Jagadish, Editors. 2015, Elsevier. p. 93-122.

137. Uchino, T., A. Miyauchi, and T. Shiba, *MOSFETs with ultrashallow junction and minimum drain area formed by using solid-phase diffusion from SiGe.* Electron Devices, IEEE Transactions on, 2001. **48**: p. 1406-1411.

138. Joshi, V., et al. *Analyzing electrical effects of RTA-driven local anneal temperature variation*. in *2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*. 2010.

139. Prekodravac, J., et al., *The effect of annealing temperature and time on synthesis of graphene thin films by rapid thermal annealing.* Synthetic Metals, 2015. **209**: p. 461-467.

140. Agarwal, A., et al., *Ultra-shallow junction formation by spike annealing in a lamp-based or hot-walled rapid thermal annealing system: effect of ramp-up rate.* Materials Science in Semiconductor Processing, 1998. **1**(3): p. 237-241.

141. Cho, K., et al., *Transient enhanced diffusion during rapid thermal annealing of boron implanted silicon.* Applied Physics Letters, 1985. **47**(12): p. 1321-1323.

142. Agarwal, A., H.-J. Gossmann, and A.T. Fiory, *Effect of ramp rates during rapid thermal annealing of ion implanted boron for formation of ultra-shallow junctions.* Journal of Electronic Materials, 1999. **28**(12): p. 1333-1339.

143. Zagozdzon-Wosik, W., *Defect Generation and Gettering during Rapid Thermal Annealing.* Journal of The Electrochemical Society, 1988. **135**(8): p. 2065.

144. Yi, K., et al., *Plasma-Enhanced Chemical Vapor Deposition of Two-Dimensional Materials for Applications.* Accounts of Chemical Research, 2021. **54**(4): p. 1011-1022.

145. Beliaev, L.Y., et al., *Optical, structural and composition properties of silicon nitride films deposited by reactive radio-frequency sputtering, low pressure and plasma-enhanced chemical vapor deposition.* Thin Solid Films, 2022. **763**: p. 139568.

146. Batey, J. and E. Tierney, *Low-temperature deposition of high-quality silicon dioxide by plasma-enhanced chemical vapor deposition.* Journal of Applied Physics, 1986. **60**(9): p. 3136-3145.

147. Park, C.-Y., et al., *Investigation of silicon nitride for spacer via plasma-enhanced atomic layer deposition using a (tert-butylamino)dimethylsilane precursor.* Applied Surface Science, 2024. **670**: p. 160715.

148. Cote, D.R., et al., *Plasma-assisted chemical vapor deposition of dielectric thin films for ULSI semiconductor circuits.* IBM Journal of Research and Development, 1999. **43**(1.2): p. 5-38.

149. Dodson, B.W., *Development of a many-body Tersoff-type potential for silicon.* Physical Review B, 1987. **35**(6): p. 2795-2798.

150. Tse, J.S., *AB INITIO MOLECULAR DYNAMICS WITH DENSITY FUNCTIONAL THEORY.* Annual Review of Physical Chemistry, 2002. **53**(Volume 53, 2002): p. 249-290.

151. Sulpizi, M. and M. Sprik, *Acidity constants from DFT-based molecular dynamics simulations.* Journal of Physics: Condensed Matter, 2010. **22**(28): p. 284116.

152. Wang, G., et al., *Machine learning interatomic potential: Bridge the gap between small-scale models and realistic device-scale simulations.* iScience, 2024. **27**(5): p. 109673.

153. Minixhofer, R. *TCAD as an integral part of the semiconductor manufacturing environment*. in *2006 International Conference on Simulation of Semiconductor Processes and Devices*. 2006.

154. Roy, A., et al., *A review of displacement cascade simulations using molecular dynamics emphasizing interatomic potentials for TPBAR components.* npj Materials Degradation, 2025. **9**(1): p. 1.

155. Weber, B., K. Gärtner, and D.M. Stock, *MD-simulation of ion induced crystallization and amorphization processes in silicon.* Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 1997. **127-128**: p. 239-243.

156. Stevens, R.J., L.V. Zhigilei, and P.M. Norris, *Effects of temperature and disorder on thermal boundary conductance at solid–solid interfaces: Nonequilibrium molecular dynamics simulations.* International Journal of Heat and Mass Transfer, 2007. **50**(19): p. 3977-3989.

157. Kamali, R. and A. Kharazmi, *Molecular dynamics simulation of surface roughness effects on nanoscale flows.* International Journal of Thermal Sciences, 2011. **50**(3): p. 226-232.