SILICON CARBIDE HETEROSTRUCTURE HIGH ELECTRON MOBILITY TRANSISTORS: MODELING, MATERIAL GROWTH, PROCESSING AND CHARACTERIZATIONS

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SILICON CARBIDE HETEROSTRUCTURE HIGH ELECTRON MOBILITY TRANSISTORS: MODELING, MATERIAL GROWTH, PROCESSING AND CHARACTERIZATION

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Silicon carbide (SiC) based semiconductor electronic devices and circuits are presently being developed for advantageous use in high-temperature, high-power, and high-radiation conditions under which conventional semiconductors cannot adequately perform. However, there has been little work on the heterostructure field effect transistor, which can be developed to be high electron mobility transistor (HEMT).

This dissertation presents the whole process for the SiC heterostructure field effect transistor: Modeling, material growth, fabrication and characterizations. First, the modeling and simulation of the two dimensional electron gas in SiC heterostructure are presented. Next, we will discuss the epitaxy growth for the SiC heterostructure. And then, we show the device processing of the heterostructure field effect transistor and high electron mobility transistor (HEMT). Finally, both materials and devices are characterized by various optical and electrical methods.

BIOGRAPHICAL SKETCH

Jie Lu was born in Hebei Province, P. R. China, on Nov.6 1982. He graduated from Nanjing University in 2004 and earned Bachelor of Science in Physics. In the last two years in Nanjing University, he completed a project on “transport properties of AlGaN/GaN heterostructure” in Prof. Bo Shen’s group. In August 2004, he joined Cornell University as a Ph.D. student in Department of Electrical and Computer Engineering. During the next five years (2004-2009), under the guidance and instruction by Prof. Michael Spencer, he worked on the wide bandgap semiconductor: material growth of SiC by CVD, structure modeling, device processing and characterization.

To 我的父母-吕士勇，卢善文

我的姥姥-王琦

我的未婚妻-张华君

洪永妙老师，师母-王昕

Prof. Spencer and Prof. Eastman

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I can’t imagine how would I finish my work without the help from people around me, my professors, my group-mates, my friends, my parents and my wife.

First, I would like to express my deep thanks for my advisor, Prof. Michael Spencer. It was him who gave me the chance to come to this beautiful place and great university. During the past five years, he always encouraged and supported me on the area I was interested in. He is a so smart, so nice, so great professor and sometime I felt he was like my father.

In our group, we have many talented students. Chris Thomas, our “big brother”, an amazing guy who was a national soccer player in Jamaica and a great father of three children, gave me countless help on both my research and my life (if not him, I could not pass through the “car incident”, which almost made me crashed). For an international student like me, it was so tough in the first 1-2 years. However, life became much easier when I met with Chris. Another friend in my group, MVS Chandra, is also a very nice and amazing person. He has very broad knowledge across different field, physics, material, circuit and device. Also he does never mind to offer his help to anyone around him, giving me the training in CNF and helping me to revise the paper. Also there are many other people at Cornell who I really enjoyed working with, Prof. Eastman, Prof. Hong, Prof. Dan, Schaff, Choi, Xingqun Jiang, Shiram, Lori, Tiju, Tad, Xiaodong Chen, Junxia Shi, Josh, Jonshu. Finally I want to express my appreciations to my parents and my wife. They are the solid supports behind me forever.

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Introduction

1. What is Silicon Carbide? Fundamentals of the physical and chemical properties of SiC.
2. Why is Silicon Carbide? The applications of SiC in various areas.

SiC is a wide band-gap indirect semiconductor with high breakdown voltage, high saturation electron drift velocity and high thermal conductivity [1-5]. It is a compound of silicon and carbon bonded together and possesses a one-dimensional polymorphism called polytypism. The basic structural unit of SiC consists of a primarily covalently bonded tetrahedron of four carbon atoms with a silicon atom positioned at the center of mass of the tetragonal structure (or vice versa), as shown in Figure. The approximate bond length between the Si-Si or C-C atoms is 3.08 Å, whereas the distance between Si and C is approximately 1.89 Å, shown in Figure 1.1. The SiC crystals are constructed with these tetrahedra joined to each other at the corners.

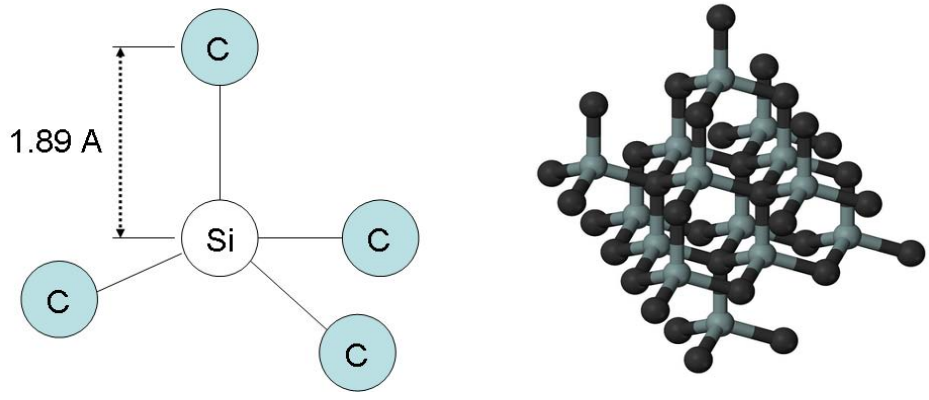

Figure 1.1 Molecule structure of Silicon Carbide

In a polytypic compound, similar sheets of atoms or symmetrical variants are

stacked atop each other and related according to a symmetry operator. The differences among the polytypes arise only in the direction perpendicular to the sheets (along the c-axis) [6]. In SiC, the sheets can be represented as a close-packed array of spheres forming a two-dimensional pattern with six-fold symmetry. Each sheet represents a bilayer compound of one layer of Si atoms and one layer of C atoms. Using the notations from hexagonal crystal structures, the first sheet can be defined as the basal or c-plane with Miller-indexed directions [7]. The most stable way to stack an identical second sheet of close-packed spheres is to place the spheres atop the "valleys" in the first sheet. There are two possibilities for arranging the second sheet relative to the first sheet in this way. The second sheet may be displaced along, for example, [1001] until the spheres lie in the valleys denoted "B" in Figure 1.2, or the sheet may be displaced along [5, 8], for example, [0011] until the spheres lie in the valleys denoted "C" in Figure 1.2.

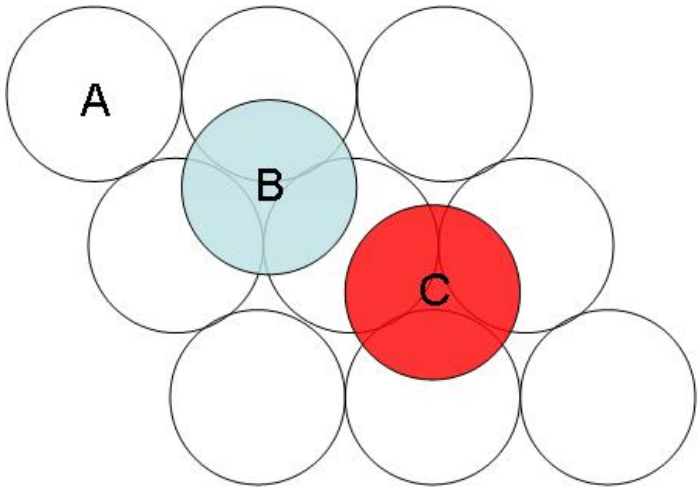

Figure 1.2 Illustration of hexagonal plane

Thus, a sheet can be denoted A, B, or C, depending on the positions of its spheres. All polytypes can be described as different stackings of A, B, and C sheets, with the restriction that sheets with the same notation cannot be stacked upon each other. A

large number (over 250) of SiC polytypes exist [4], with some having stacking sequences of several hundreds of bilayers. The crystal structures of the SiC polytypes are cubic, hexagonal, or rhombohedral. The only cubic polytype is referred to as β-SiC, whereas the hexagonal and rhombohedral polytypes are referred to collectively as α-SiC. Due to the increasing number of discovered polytypes of α-SiC, it was suggested that each polytype could be named with a number according to the periodicity in the stacking direction and the letter H, for hexagonal, or R, for rhombohedral. Subsequently, it became common to refer to β-SiC as 3C-SiC [4].

The simple stacking sequence of ABCABC… produces the zincblende 3C structure (with the stacking along the [111] direction), which is the only possible cubic polytype, shown in Figure 1.3. All of the other polytypes are mixtures of the fundamental zincblende and wurtzite structures. Some common hexagonal polytypes with more complex stacking sequences are 4H- and 6H-SiC. 4H-SiC is composed equally of cubic and hexagonal structures, while 6H-SiC is two thirds cubic. Despite the cubic elements, each has overall hexagonal crystal symmetry. The stacking sequences for 4H and 6H are ABACABAC… and ABCACBABCACB…, espectively. Figure 1.3 illustrates most common polytypes of SiC: 3C, 4H, and 6H.

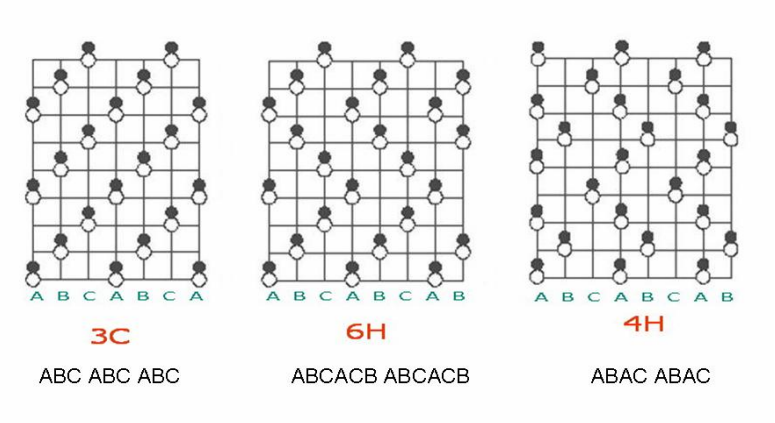

Figure 1.3 Illustration of different polytypes of SiC

Physical Properties

Next to diamond, SiC is the hardest substance known to man. In fact, the first use of SiC was as an abrasive for sandpaper and it is still being used for that today. It is also used tools such as sharpening wheels for knifes and other sharp edged tools. SiC does not occur naturally on earth, but has been found to be one of the constituent materials in some meteorites. Its color can be black, green, yellow, yellow-green, blue, or transparent, depending on the type and amount of impurities that are in the material.

Chemical Properties

SiC does not melt, but sublimes at a temperature of 2200° C (atmospheric pressure) [9]. It is also very radiation hard and is nonreactive at room temperature. At high temperatures, however, SiC can be etched by salts such as potassium hydroxide (KOH), select halogen gas plasmas, hydrogen, and HCl. Electrochemical means of etching SiC have also been reported.

Electrical Properties

Owing to the different arrangements of Si and C atoms within the SiC crystal lattice, each SiC polytype exhibits unique electrical and optical properties. Some important semiconductor material properties of the 3C-, 4H-, and 6H-SiC polytypes at room temperature are given in Table 1.1, allowing a comparison with the properties of Si, GaAs, and GaN [1, 9, 10].

Table 1.1 Comparison of SiC polytypes with other semiconductors

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, Eg (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant, ε_r[1]	11.9	13.1	9.66	10.1	9	5.5
Electric Breakdown Field, E_c (kV/cm)	300	400	2500	2200	3000	10000
Electron Mobility, μ_n ($cm^2/V{\cdot}s$)	1500	8500	500 80	1000	1250	2200
Hole Mobility, μ_p ($cm^2/V{\cdot}s$)	600	400	101	115	850	850
Thermal Conductivity, λ (W/cm·K)	1.5	0.46	4.9	4.9	1.3	22
Saturated Electron Drift Velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2	2	2.2	2.7

[1] $\varepsilon = \varepsilon_r \cdot \varepsilon_o$ where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m

Semiconductor electronic devices function in the temperature range [9, 11] where intrinsic carrier concentrations are negligible so that conductivity is controlled by intentionally introduced dopant impurities [12, 13]. Furthermore, the intrinsic carrier concentration is a fundamental prefactor governing undesired junction reverse-bias leakage current. As temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow unacceptably large. Eventually, at such higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device dopants.

The wide bandgap energy and low intrinsic carrier concentration of SiC allow it to maintain semiconductor behavior at much higher temperatures than Si or GaAs, which in turn permits SiC semiconductor device functionality at these much higher temperatures [14].

The high breakdown field [15] and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized [11]. The high breakdown field of SiC relative to Si or GaAs enables the blocking voltage region of a power device to be roughly 10

times thinner and 10 times more heavily doped, permitting roughly a 100-fold decrease in the blocking region resistance. In addition, the high breakdown field and wide energy bandgap of SiC also enable much faster power switching than is possible in comparably volt-amp rated Si power-switching devices, resulting in SiC based power converters which can operate at higher switching frequencies with much greater efficiency (i.e., less switching energy loss) [7]. Higher switching frequency in power converters is highly desirable because it permits use of smaller capacitors, inductors, and transformers, which in turn can reduce overall system size and weight. While the smaller on-resistance and faster switching of SiC help minimize energy loss and heat generation, the higher thermal conductivity enables more efficient removal of waste heat from the active device. Waste heat radiation efficiency increases greatly with 12 increasing temperature difference between the device and the cooling ambient. Thus, the ability of SiC to operate at high junction temperatures permits much more efficient cooling to take place, so that heat-sinks and other device-cooling hardware (i.e., fan cooling, liquid cooling, air conditioning, etc.) typically needed to keep high-power devices from overheating can be made much smaller or even eliminated. Uncooled operation of high-temperature and/or high-power SiC electronics would enable revolutionary improvements in aerospace systems. Replacement of hydraulic controls and auxiliary power units with distributed “smart” electromechanical controls and sensors capable of harsh-ambient operation will lead to substantial jet-aircraft weight savings, reduced maintenance, reduced pollution, higher fuel efficiency, and increased operational reliability. SiC high-power solid-state switches will also afford large efficiency gains in electric power management and control. Performance gains from SiC electronics could enable the public power grid to meet the increased consumer electricity demand without building additional generation plants, and improve power quality and operational reliability through ``smart'' power management [7, 16]. More

efficient electric motor drives, enabled by improved SiC power devices, will benefit industrial production systems as well as transportation systems such as diesel-electric railroad locomotives, electric masstransit systems, nuclear-powered ships, and electric automobiles and buses.

Finally, the saturated electron velocity [10], which is a measure of the maximum velocity that an electron in a semiconductor can attain at high electric fields, is twice as much for SiC as it is for Si. This an important parameter for submicron field effect transistors (FET's), as, regardless of the semiconductor material used, the electrons in these devices will see saturation conditions due to the inherently high fields [17]. This means that, although the electron mobility of SiC is smaller than that of Si, for comparable devices with submicron channel lengths, the SiC device will be faster than its Si counterpart. The speed advantage of SiC submicron field effect transistors means that these devices can operate at higher frequencies than Si based ones.

All these properties when taken together give SiC devices a distinct advantage in the area of high power, high temperature, and high frequency applications [18].

In this thesis, we will show the whole process for the SiC heterostructure field effect transistor: Modeling, material growth, fabrication and characterizations.

In chapter II, the epitaxial growth of SiC heterostructure will be investigated. Different factors which influence the growth process are discussed.

In chapter III, based on the good growth condition, we achieved some heterostructure samples in good quality, from which we observed two dimensional electron gas (2DEG) by using optical and electrical measurements.

In chapter IV, the fabrication technology of SiC devices is introduced.

In chapter V, finally, a quantum characterization of 2DEG is presented, which shows the quantum plateau in SiC materials for the first time in the world and gives the strongest supports on the existence of the 2DEG in SiC heterostructure.

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Chapter II Material Growth

This chapter shows the growth and characterization of 3C-SiC layer grown on both C-face and Si-face 6H on-axis SiC substrate. By changing different growth conditions, surface morphology of the epi-layers shows a strong dependence on growth pressure, C/Si ratio, HCl flow and growth temperature. Lightly doping and high quality 3C-layer has been achieved at optimized condition, high pressure, high C-Si ratio and low HCl flow. To reduce the Nitrogen doping at the interface, which is the main source of the low mobility, both HCl etching and Hydrogen etching at different temperature process were investigated and pursued.

2.1 Growth Methods

As we showed in the previous chapter, Silicon carbide (SiC) is a potentially useful material for high-power, high-frequency and high temperature electronic devices, due to its wider band gap and higher electrical breakdown field than seen in Si and GaAs. So to get a high quality epitaxial layer of SiC is the very important for device [1, 2].

Epitaxial deposition is a process that produces single-crystal films with the same crystallographic orientation as the underlying substrate, like CVD and MBE. Epitaxial growth from a CVD process is sometimes referred to as vapor-phase epitaxy (VPE). Other epitaxial processes that have been developed since 1960 include molecular-beam epitaxy (MBE) and liquid-phase epitaxy.

Table 2.1 Comparison of MEB and MOCVD

Growth method	features	limit
MBE (Molecular Beam Epitaxy)	Deposit epilayer at ultrahigh vacuum	Hard to grow materials with high vapor pressure
MOCVD (Metal-Organic Chemical Vapor Deposition)	Use metalorganic compounds as the sources	Some of the sources like AsH3 are very toxic.

CVD is widely accepted as offering the most promise for the well-controlled homoepilayer growth and heteroepilayer growth required for most SiC electronic devices [1, 3]. The CVD process uses different chemical as a deposition precursor. The growth of Group III-V compounds from metal-organic and hydride sources were first reported in 1960. Later, it was established that many common compound semiconductors could be deposited from metal-organic materials. When applied to the growth of epitaxial films, this technique is sometimes called metalorganic vapor-phase epitaxy or organometallic VPE. As used for the epitaxial growth of compound semiconductors, MOCVD has advanced rapidly since the mid-1980s. It has become established as a unique and important epitaxial crystal growth technique, yielding high-quality, low-dimension structures for fundamental semiconductor physics research and production of useful semiconductor devices [4, 5]. The CVD technique is attractive because of its relative simplicity, when compared with other growth methods. Excellent control over film composition can be achieved by precisely metering the amounts of gaseous species introduced to the chamber [6]. Thus, MOCVD can be used to produce heterostructures, multiquantum wells, and superlattices with very abrupt transitions in composition, as well as alloys with tailored doping profiles [5, 7, 8].

CVD technologies are often sorted by reactor type and pressure, including low pressure CVD (LPCVD), atmospheric pressure CVD (APCVD), ultrahigh vacuum

CVD (UHVCVD), hot-wall CVD [9-13] or cold-wall CVD [14], shown as Figure 2.1.

Our CVD reactor is shown in Figure 2.2, which is vertical cold wall CVD. Gaseous precursors, propane, silane, HCl are introduced to the reaction chamber from the gas manifold [3, 15]. Hydrogen is used to be the carrier gas. The substrate, located on a graphite carrier coated with SiC, is heated by graphite filament. Growth occurs primarily on this hot surface.

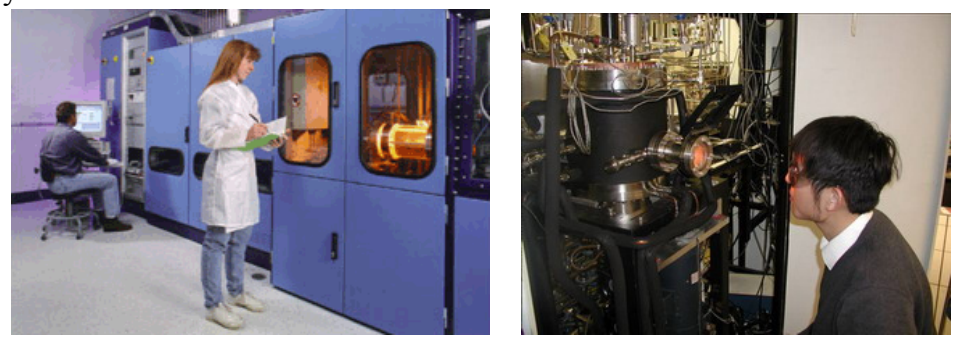


Figure 2.1 Hot-wall (NASA) and Cold wall CVD

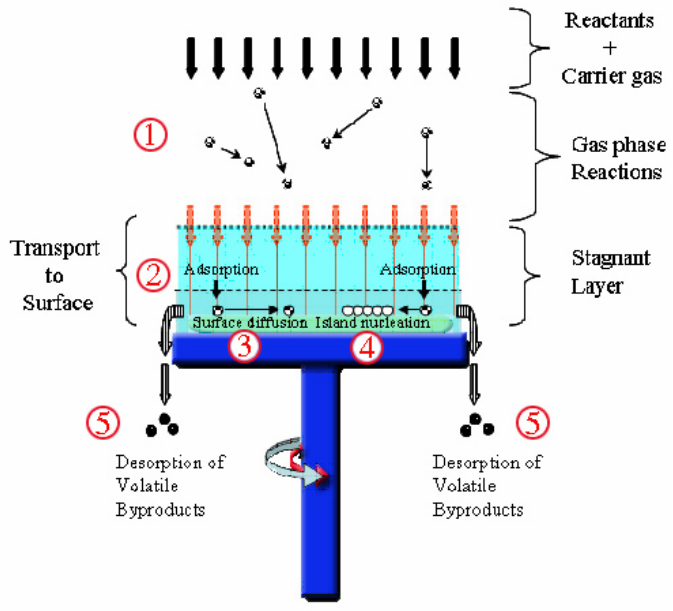


Figure 2.2 Gas transport in vertical rotating disc reactor

Commercially available 6H-SiC C-face and Si-face on-axis substrates were used. The gases of SiH_4 and C_3H_8 were used as source gases, and H_2 purified by a Pd

purifier was used as the carrier gas. Typical gas flow rates of H_2 and SiH_4 were 20 slm and 2 sccm, respectively. The C/Si ratio was varied from 0.6 to 1.5 by controlling the C_3H_8 flow rate [16, 17]. The substrate temperature was 1350C for growth and 1500-1600C for etching. The reactor pressure was varied from 200torr to 600torr. The growth rate was about 80-800um/h at different pressure.

2.2 Etching process before the growth

Epitaxial growth on a substrate is highly dependent on the surface quality of the substrate, since even minor defects may propagate into the film being grown and degrade its quality. In our experiments, we have tried etching under both pure hydrogen and mixture of HCl and hydrogen environment. Surface morphology shows strong dependence with the pressure, temperature, time and flowing gas [10, 13, 18, 19].

2.2.a HCL etching

At first, we used HCl and H_2 mixture to be the etching environment and heated the wafer up to 1500C. The chamber pressure is 60torr. After 10mins etching, we could see some steps and terraces by AFM (Atomic force microscope). The step height is about 1-2 nm, which is the lattice constant of SiC. However, the round shape of the step in the AFM pictures showed that the etching under HCl flowing is not effective.

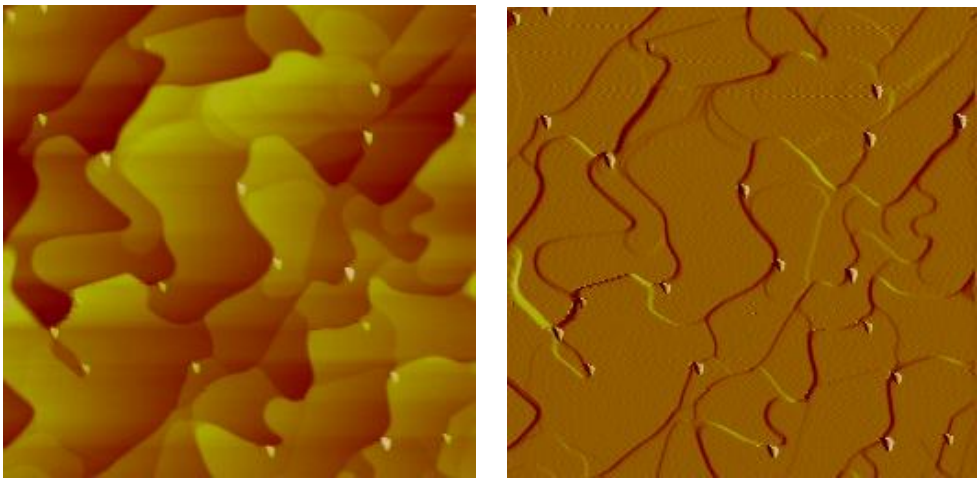


Figure 2.3 AFM pictures for HCl etching at 1500C and 60torr for 10mins. Range scale is 5um and color scale is 15nm.

2.2.b Hydrogen etching under 200torr pressure

Then we did etching by pure hydrogen, without HCl, at 1600C, under 200torr pressure and for 10mins. The conditions are chosen based on our previous work. At high temperature, the various reactions which would be capable of occurring in the coexistence of hydrogen and silicon carbide are classified into three types: dissociation of SiC crystals, vaporization of Silicon, and formation of hydro-carbon by the reaction between C and hydrogen [1, 15, 20-22]. Table1 shows the reaction processes.

Table 2.2 Reaction processes in MOCVD

$$SiC(s) = Si(s) + C(s)$$
$$SiC(s) = Si(l) + C(s)$$
$$SiC(s) = Si(g) + C(s)$$
$$SiC(s) = Si(g) + C(g)$$
$$SiC(s) = \tfrac{1}{2}Si_2(g) + C(s)$$
$$SiC(s) = \tfrac{1}{2}Si_2C(g) + \tfrac{1}{2}C(s)$$

Table 2.2 (Continued)

$SiC(s)+\frac{3}{2}H_2(g)=Si(g)+CH_3(g)$

$SiC(s)+2H_2(g)=Si(g)+CH_4(g)$

$SiC(s)+\frac{1}{2}H_2(g)=Si(g)+\frac{1}{2}C_2H_2(g)$

$Si(l)+\frac{1}{2}H_2(g)=SiH(g)$

$Si(l)+2H_2(g)=SiH_4(g)$

$C(s)+\frac{1}{2}H_2(g)=CH(g)$

$C(s)+H_2(g)=CH_2(g)$

$C(s)+\frac{3}{2}H_2(g)=CH_3(g)$

$C(s)+2H_2(g)=CH_4(g)$

$2C(s)+H_2(g)=C_2H_2(g)$

$2C(s)+2H_2(g)=C_2H_4(g)$

The results are shown as Figure 2.4, better steps and parallel edges were achieved. But there were lots of particles spread on the surface, which could be Silicon droplets during the etching. The etching process follows the formation of hydrocarbons through the reaction between hydrogen carrier gas and the surface carbon. The remaining silicon on the surface can evaporate, or form silicon droplets depending on the pressure.

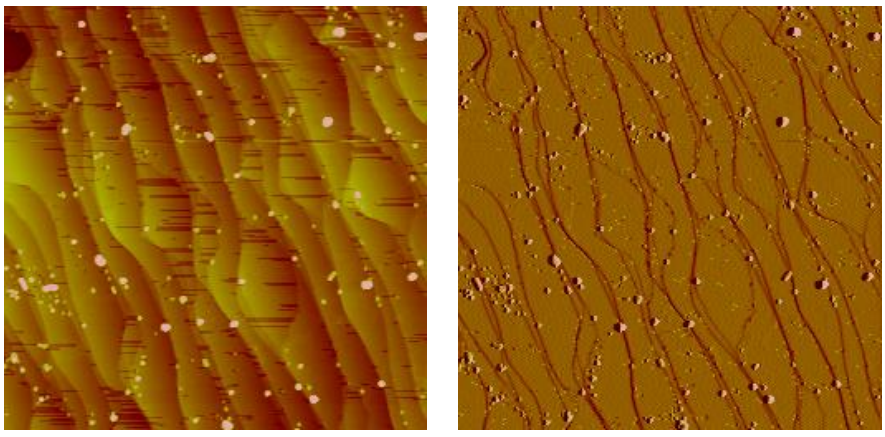


Figure 2.4 AFM pictures for pure H_2 etching at 1600C and 200torr for 12mins. Range scale is 5um and color scale is 10nm.

To reduce the hydrocarbon formation and the Si droplets, we flow some propane

during the etching process cut down the etching time. The silicon droplets will react with the propane to re-form SiC layer, shown in Figure 2.5. Clear steps and terraces can be observed and the surface is much cleaner than the one without propane flowing.

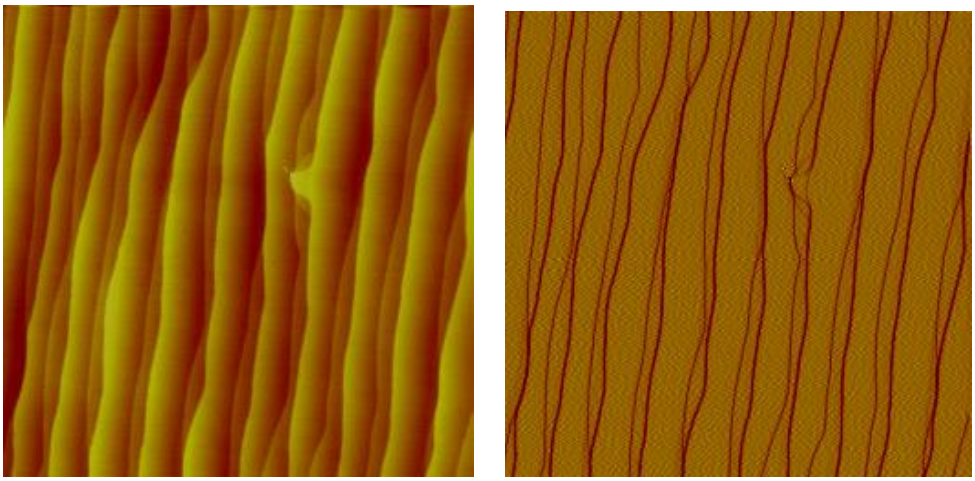


Figure 2.5 AFM pictures for pure H_2 etching at 1600C and 200torr for 3mins with flowing little propane. Range scale is 5um and color scale is 4nm.

Then we tried higher temperature points, 1650C to see if the surface morphology could be improved. From Fig.6, we can see the round edge shape, which shows the over-etching.

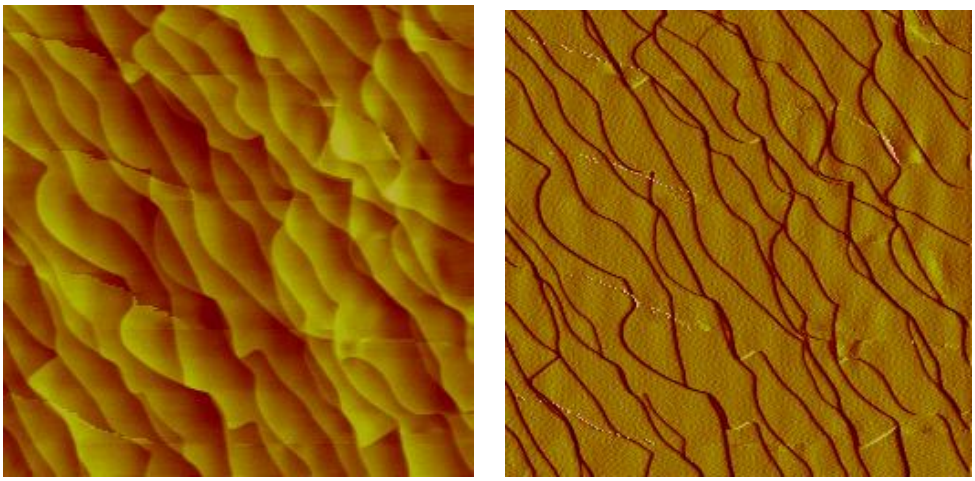


Figure 2.6 AFM pictures for pure H_2 etching at 1650C and 200torr for 3mins with flowing little propane. Range scale is 10um and color scale is 5nm.

2.2.c Hydrogen etching at 1600C under different pressure

We changed the pressure to be 65 torr, the lowest pressure we could reach under 2slm hydrogen flowing. After 3mins etching, some screw defects showed up. After all, the best condition we got for the Hydrogen etching is 1600C, 200torr, 2slm flow of Hydrogen, 3-5mins.

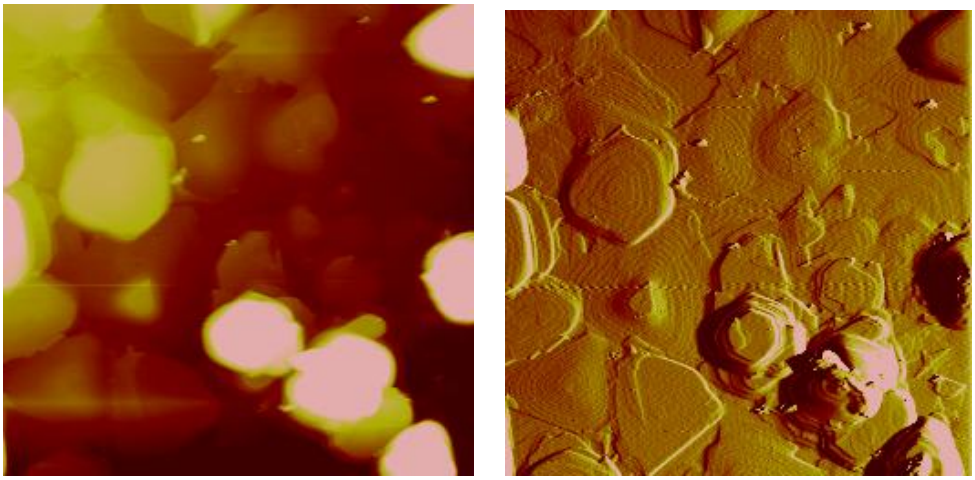


Figure 2.7 AFM pictures for pure H_2 etching at 1600C and 65torr for 3mins with flowing little propane. Range scale is 10um and color scale is 20nm.

2.2.d. Other conditions for long etching—15 mins

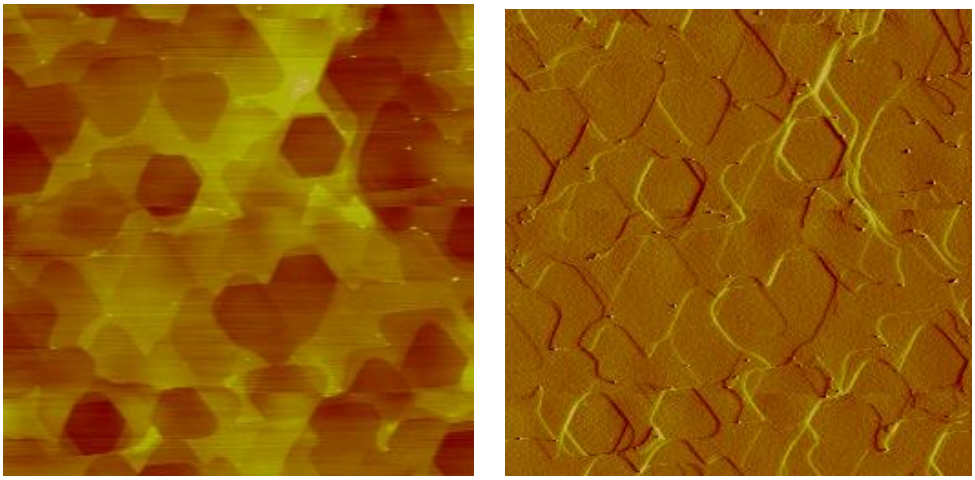


Figure 2.8 AFM pictures for pure H_2 etching at 1450C and 600torr for 15mins with flowing little propane.Range scale is 5um and color scale is 10nm.

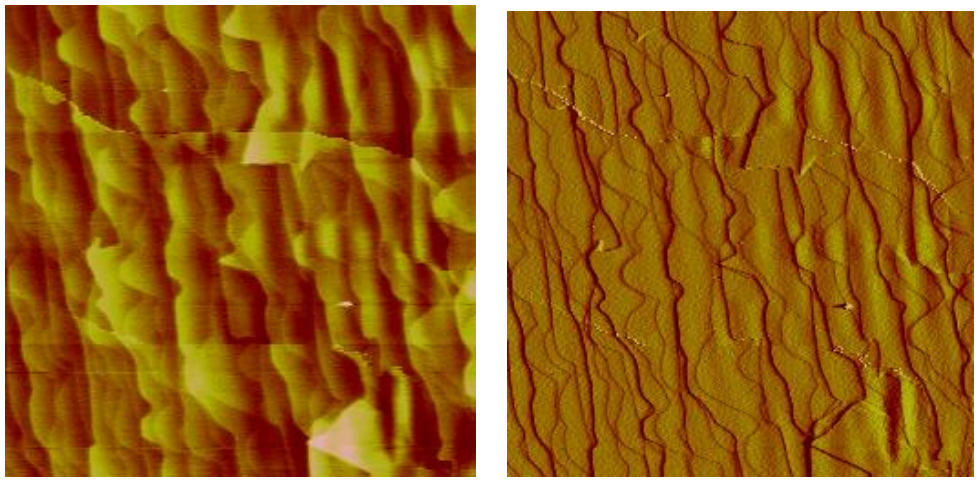


Figure 2.9 AFM pictures for pure H_2 etching at 1550C and 200torr for 15mins with flowing little propane. Range scale is 10um and color scale is 3nm.

2.3 Epi-growth of SiC by CVD

One of the most interesting properties of SiC is the occurrence of different polytypes in this material with different physical properties, like bandgap, polarization charge. Therefore, it may be possible to build devices from heterostructures consisting two different polytypes with confined electrons in a two dimensional interface, which is called two dimensional electron gas (2DEG). However, the growth of heteropolytypic structures is not easy to control. Here we will present a simple introduction for the growth mechanism of homo-epitaxy and hetero-epitaxy for SiC growth.

Before explaining the growth mode in detail, we will look at the cold wall vertical CVD growth system in our lab. In Figure 2.10, we can see that the reactance (in our case were H_2, Propane, Silane and HCl) flowed from the top injector to the rotated susceptor (carrier). A substrate was sitting on the carrier at a controlled temperature.

The carrier is made of graphite coated with SiC. The reactance, Silane, Propane and HCl [23], were carried by hydrogen. The exhausted gases were pumped out through the outlet in the bottom. The susceptor with carrier was rotating at 1000rpm.

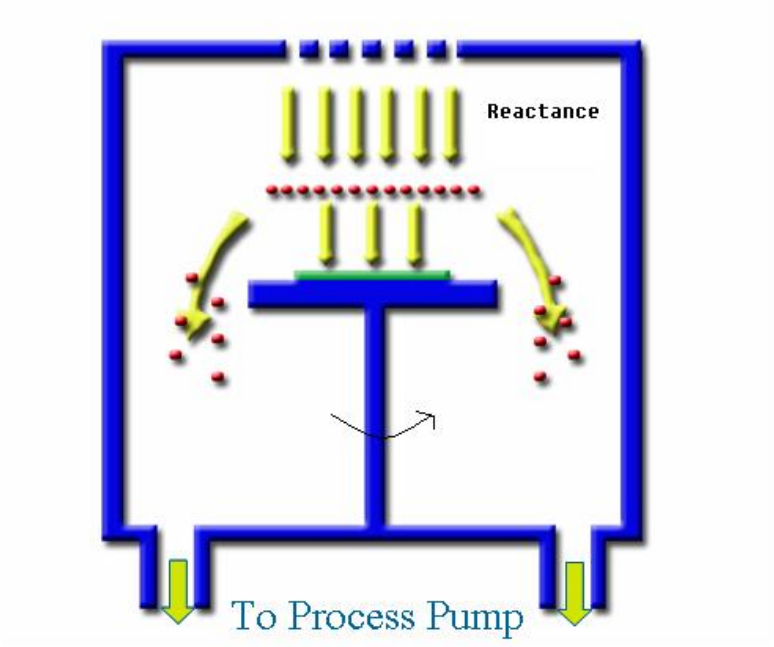


Figure 2.10 Structure diagram of cold wall CVD in out lab

2.4 Homo-epitaxy growth

Homoepitaxial growth is the growth that the polytype of the epilayer matches the polytype of the SiC substrate. Homoepitaxial growth could be attributed to lateral growth from atomic steps (step-flow growth), by which grown layers inherit the stacking order of substrates, and named this method “step control” epitaxy [24-26], shown in Figure 2.11.

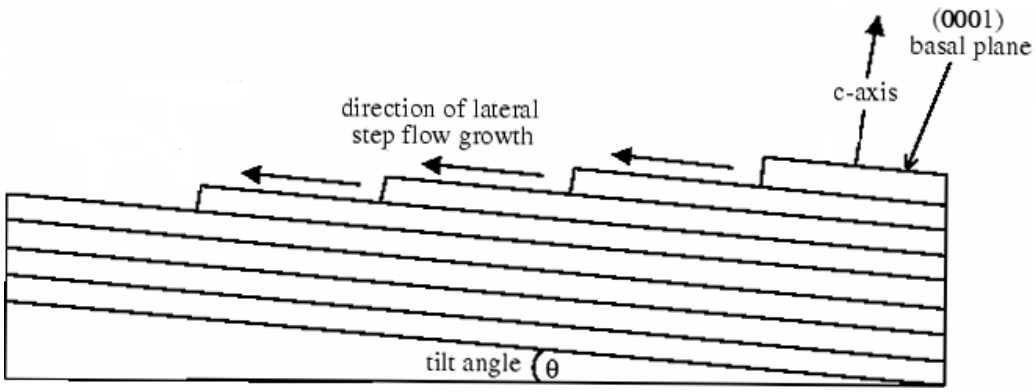


Figure 2.11 Cross section view of step-flow growth

The reactant atoms impinge on the surface and attempt to connect to the atoms that are already bonded there. When the surface is flat, these reactant atoms, upon arriving, have only the option of attaching to the atoms below them [27]. This bond is not a strong one, and, as a consequence, the atoms can move about on the surface. These loosely bonded atoms are said to have been adsorbed onto the surface and are called adatoms [25, 28].

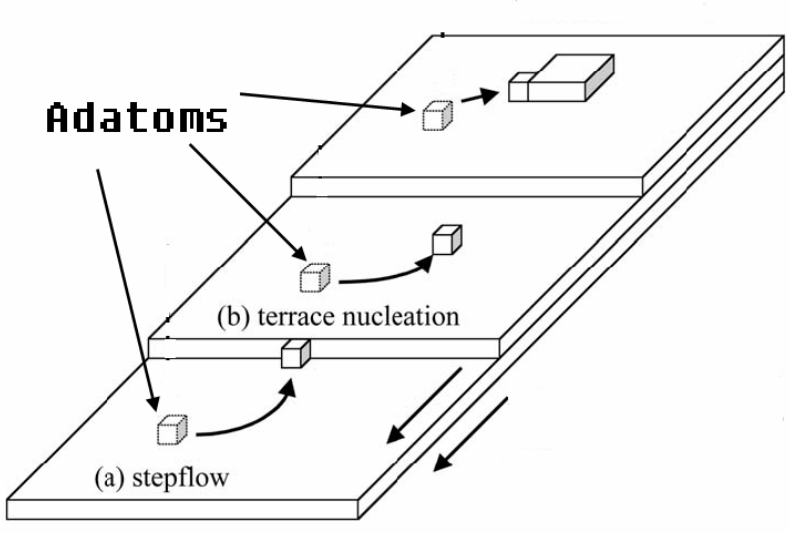


Figure 2.12 Movement of adatoms on the surface of wafer

Adatoms move about the surface by diffusion, searching for favorable sites to

create additional bonds that will help to incorporate them into the crystal. The sites that offer the highest number of bonds are the vacancy and kink sites. Once the adatoms bond to these sites, they become a part of the crystal and are said to be crystallized [29].

If the adatoms diffuse about the surface and bond to a step edge, they are still not crystallized because the bonding here is not strong enough to stabilize an adatom, and therefore, they will continue to move along the step edge until a bond site that is strong enough to hold them in place, such as a kink site, is found. Once the adatoms find a kink site, they can finally be incorporated into the crystal [25, 30]. The net effect of the adatoms arriving and diffusing along the crystal surface and along the step edges to find site where they can be incorporated into the steps results in growth by advancement of the step edges. This method of growth where the steps are continually advanced from the edges is called step flow growth [31, 32].

Step-flow growth has been one of the most attractive subjects from a viewpoint of crystal growth. The main factors that dominate the process are surface off-angle, diffusion length, and nucleation rates.

When steps are too far apart (on-axis), adatoms can nucleate and bond in the middle of the terraces instead of at the steps, leading to heteroepitaxial growth of 3C-SiC. In the other hand, for step flow process, there is a sufficiently short distance between the steps (off-axis), so Si and C atoms impinging onto the growth surface can find their way to steps where they bond and incorporate into the crystal [28, 33].

Matsunami has given out the calculations of the surface reaction based on a diffusion model [31, 33]. In their simulation, they defined a parameter “a” to represent the super-saturation level. The value of “a” depends on experimental conditions such as growth rate, growth temperature, and terrace width. So when the value of “a” is higher than a critical point, two-dimensional nucleation growth happens. If it’s smaller

than the critical point, the step-flow growth will take place. In general, longer diffusion length(higher temperature) and shorter terrace width (larger off angle) can lead to the step control flow growth, which is homo-epitaxial growth.

Figure 2.13 is the AFM pictures of the surface after homo-epitaxy, from which we can see the steps and two growth directions clearly. The bi-directional growth is due to the off-cut angle on the surface.

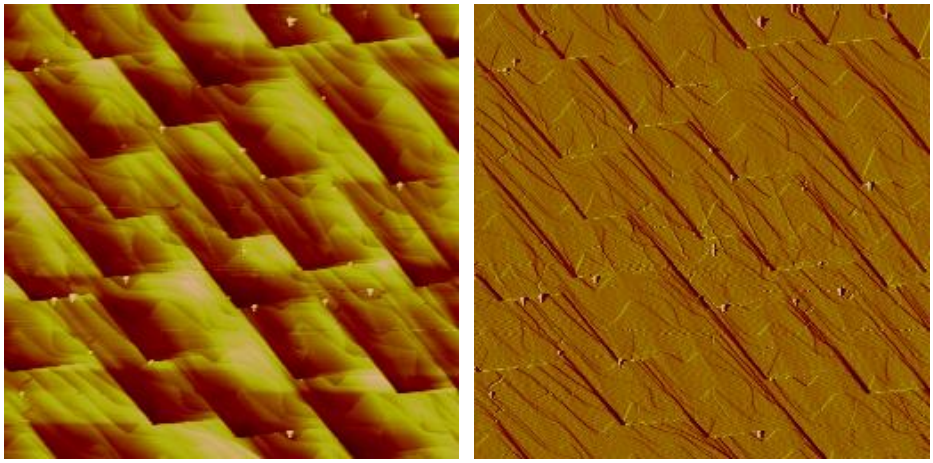


Figure 2.13 AFM pictures for Homo-epitaxy.

Range scale is 10um and color scale is 10nm.

2.5 Nucleation in hetero-epitaxy growth

To get two dimensional electron gas, we need to grow hetero-eptaxial layer, 3C-SiC on 6H-SiC or 4H-SiC.

As we showed above, hetero-epitaxy, which is 2D nucleation growth, needs lower temperature and short diffusion length, in relative terms, the longer terrace width, which could be achieved by using very on-axis wafer [34]. So we chose on-axis semi-insulating 6H-SiC substrate and set the growth temperature to be 1350C [12, 35].

To see the temperature dependence on the nucleation density, we compared the surface after growth at different temperature, 1350C, 1450C, 1550C and 1650C.

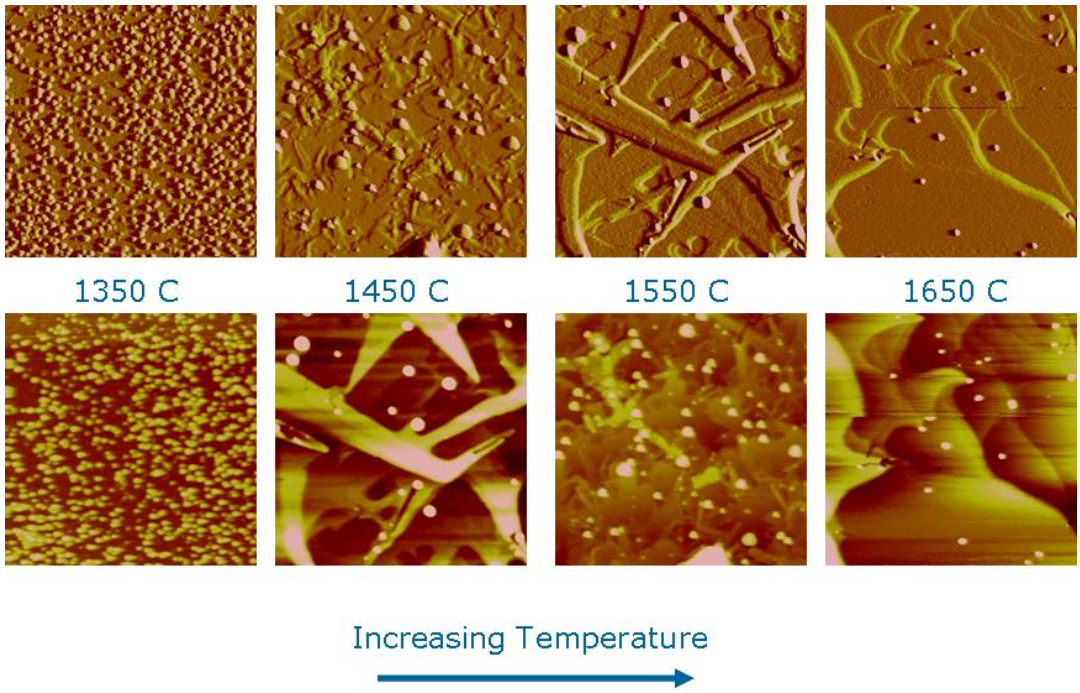


Figure 2.14 surface morphology after growth at different temperature

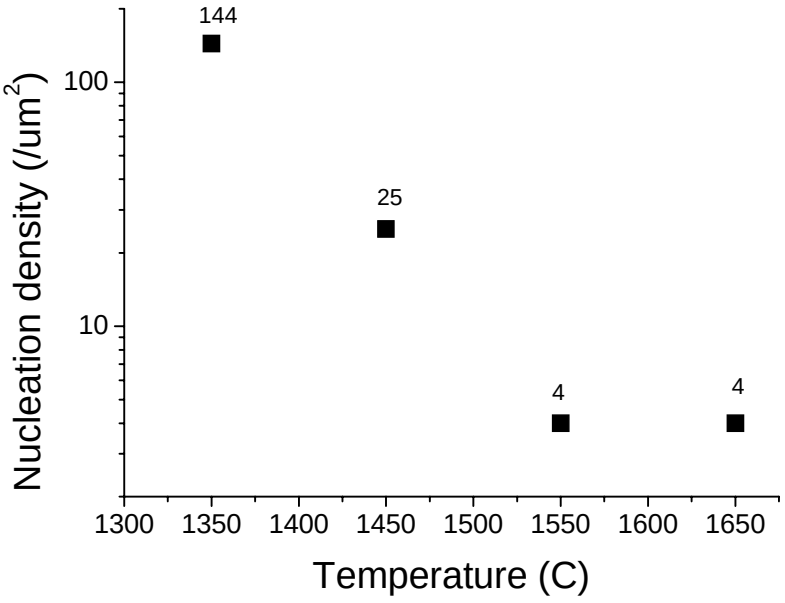


Figure 2.15 Nucleation density with respect of growth temperature

From Figure 2.14-15, we found that the nucleation density decreased by ramp up the temperature. For the surface grown at 1650C, we can see clear steps, which is the

step flow feature.

2.6 Hetero-epitaxy at different pressure

2.6.a Hetero-epitaxy at low pressure

The chamber pressure during the growth is very critical, because it can change the C/Si window and nucleation rate.

First, we set the growth pressure to be 200torr and Silane flow to be 2scc. After several runs, we got the good growth condition under this pressure to be C/Si ratio 0.3 and HCl/Si 90. The AFM and SEM pictures of the surface are shown in below. From these pictures, we can see the islands feature clearly. Those islands are formed due to the two different phases of 3C-SiC, as we showed in the first chapter. So different Si-C pairs started to nucleate all over the surface in the beginning, then expanded and met with each other. The edges we see between those islands are the boundaries.

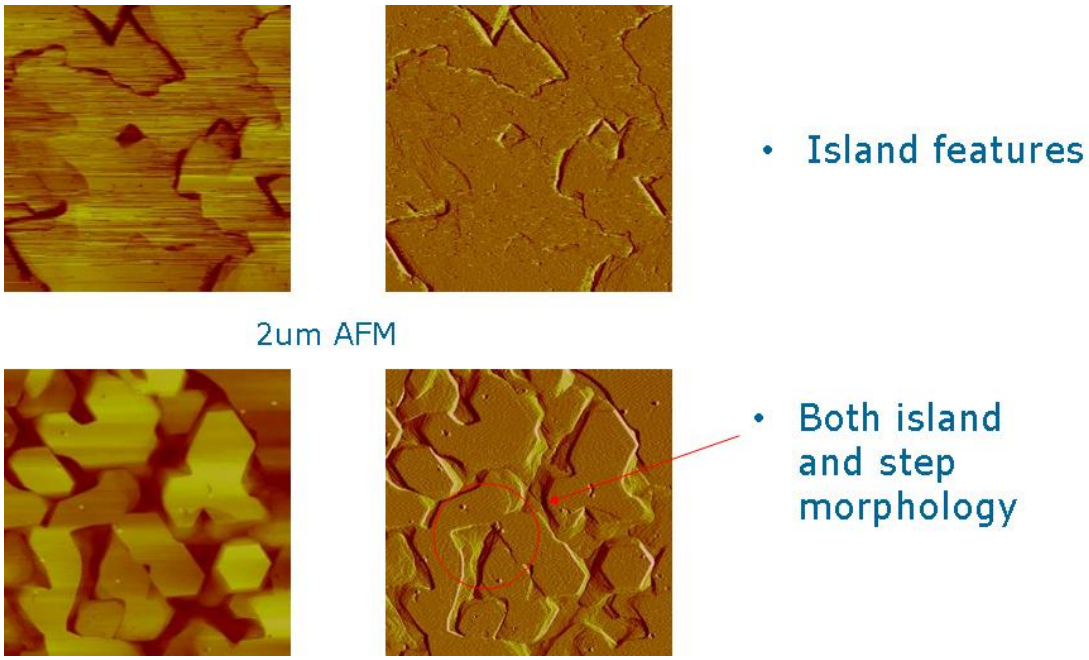


Figure 2.16 Surface morphology after growth under low pressure, low C/Si ratio and high HCl

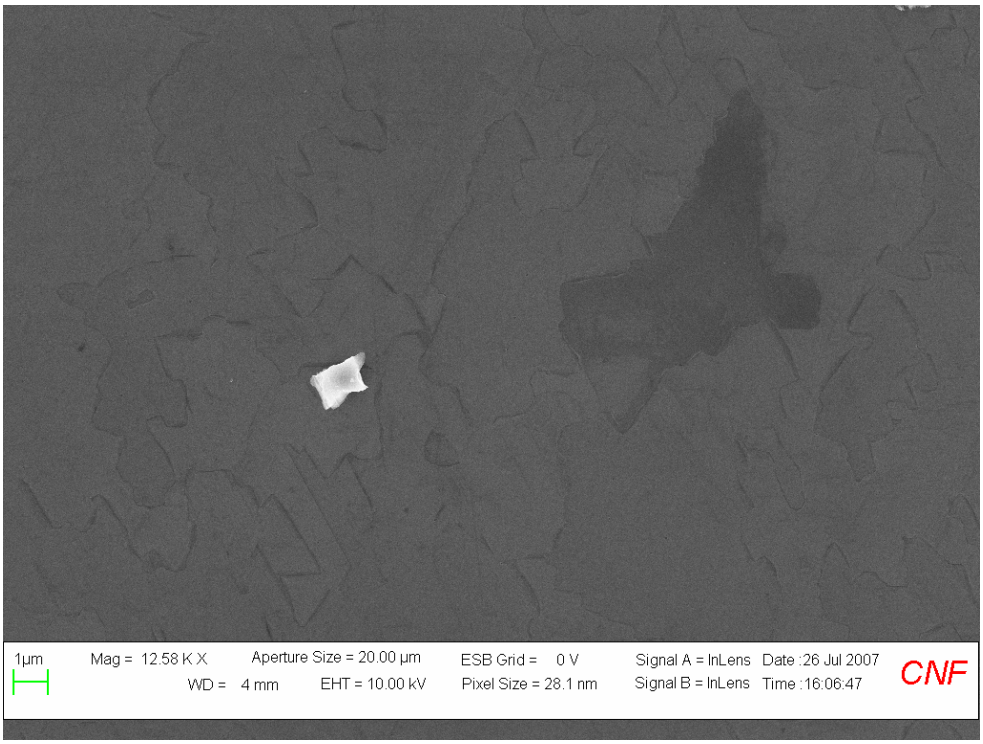


Figure 2.17 SEM pictures for the surface morphology after growth under low pressure, low C/Si ratio and high HCl

By using Hall measurement, we got carrier density and mobility of the samples. In the hetero-epi sample, the carrier density is as high as 3.7e13/cm^2 at 77K, however, for the homo-epi one, the carrier was froze out at 77K, shown as Fig.16 and 17. This fact proved the existence of the 2DEG.

Table 2.3 Comparison between the hetero-epi sample and homo-epi sample

	Hetero-epi	Homo-epi
Carrier density (300K)	4.55e13 /cm^2	1.38e13/cm^2
Mobility (300K)	137 cm^2/V.s	88 cm^2/V.s
Carrier density (77K)	3.7e13/cm^2	Freezing out
Mobility (77K)	181 cm^2/V.s	No data

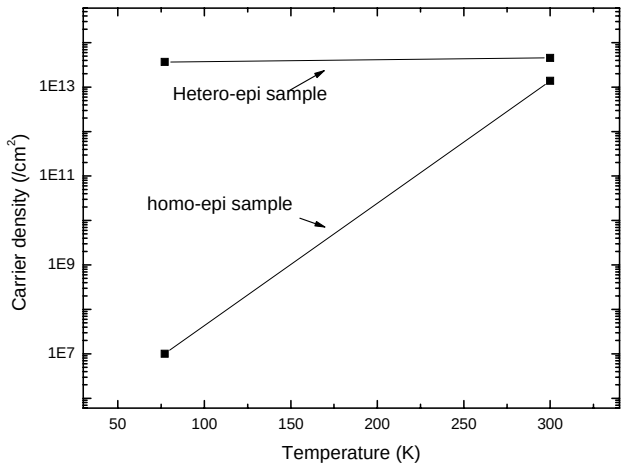


Figure 2.18 Carrier was froze out at 77K in homo-epi layer but not in hetero-epi one

From the Hall measurement and simulation, we believed the existence of 2DEG, but the doping seems too high, so we could not get any C-V data for those samples and the mobility is too low [36].

In our case, the high doping is from the Nitrogen molecules [37], which were stuck on the surface before the growth. Also Nitrogen prefers to stick on C-face SiC substrate than the Si face. These nitrogen atoms gave the strong N-type doping, which is the source of the low mobility and leakage current.

Many references have claimed that doping can be changed by varying C/Si ratio. And the pressure, HCl flow can also influence the doping.

2.6.b Hetero-epitaxy at High pressure

After some testing and improvement for our system, we found that the system was very stable under 600torr. Then we ramped down the flow of the HCl and the C/Si increased to be 1.5.

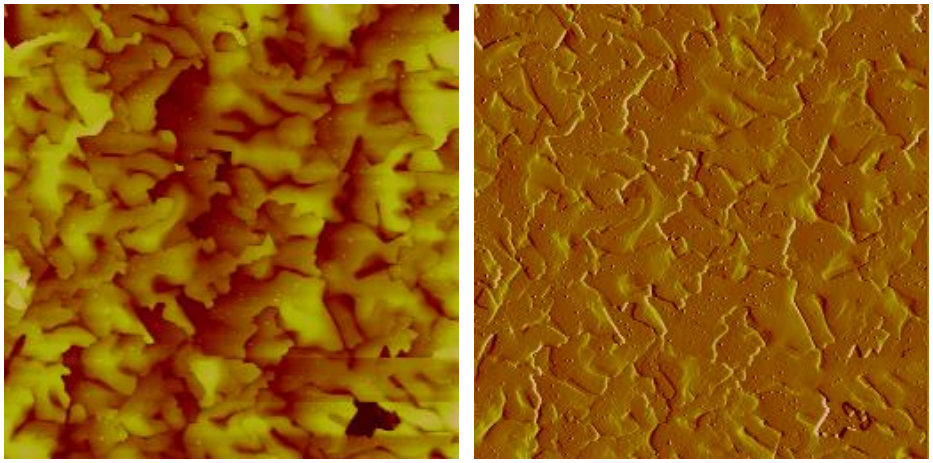
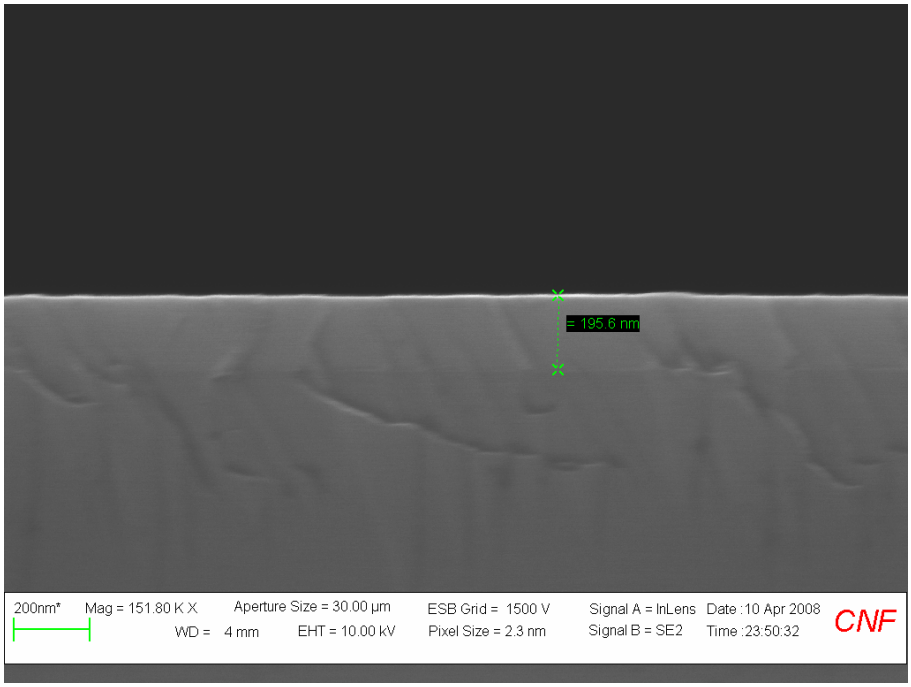
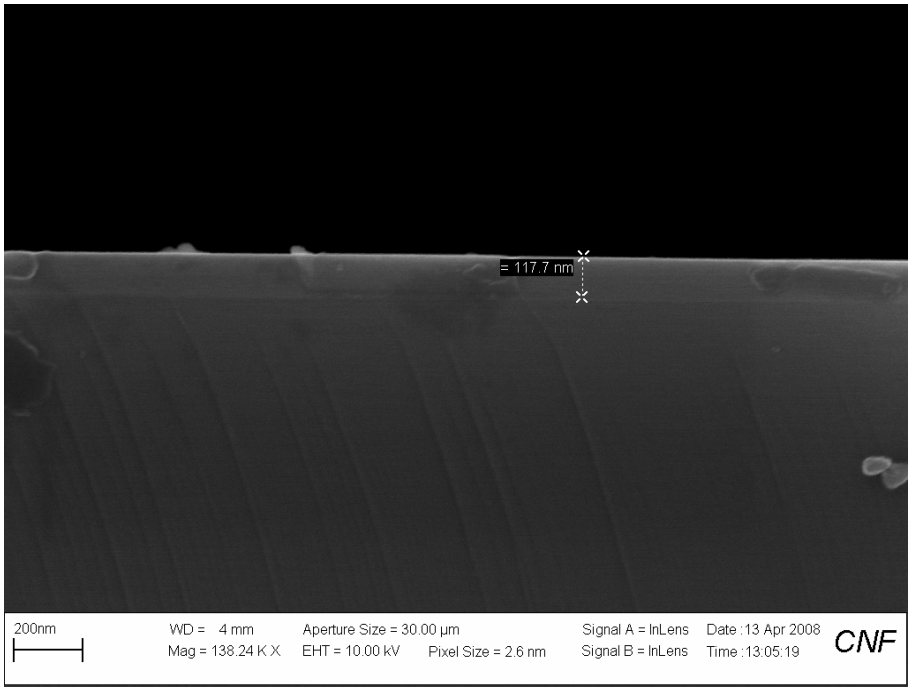


Figure 2.19 AFM pictures for hetero-epi layer under high pressure, high C-Si ratio condtions. Range scale is 25um and color scale is 20nm.

The growth rate is about 800nm/min. Figure 2.20 is the SEM pictures for the cross section of three samples for different growth time, 15mins, 7.5mins, and 3.5mins. The color of epi-layer is lighter than the substrate, because it's conductive and the substrate is semi-insulating.



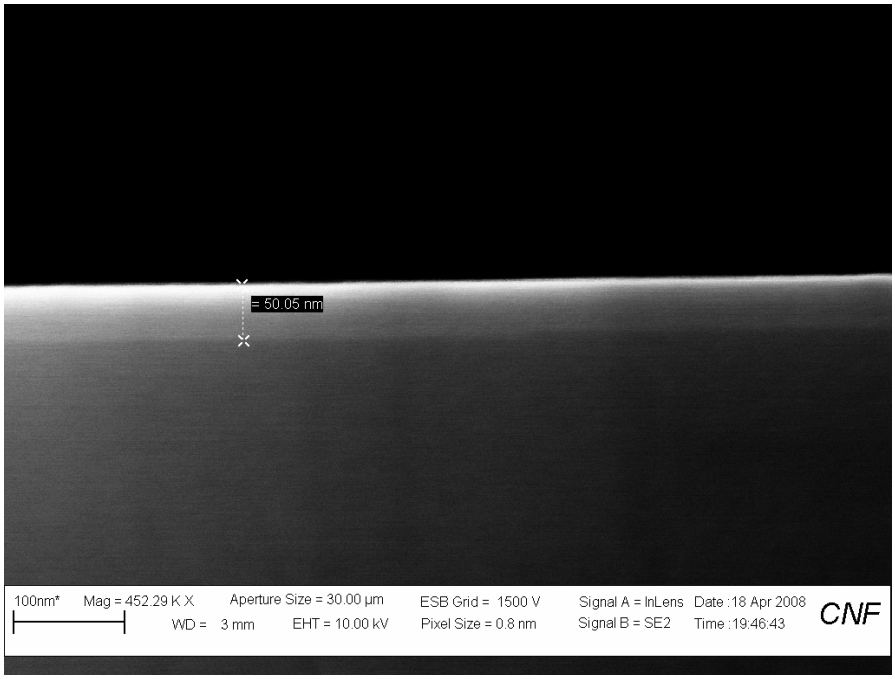
SEM picture for the cross section of sample for 15mins growth



SEM picture for the cross section of sample for 7.5mins growth

Figure 2.20 SEM picture for the cross section of sample for 3.5mins growth

Figure 2.20 (Continued)



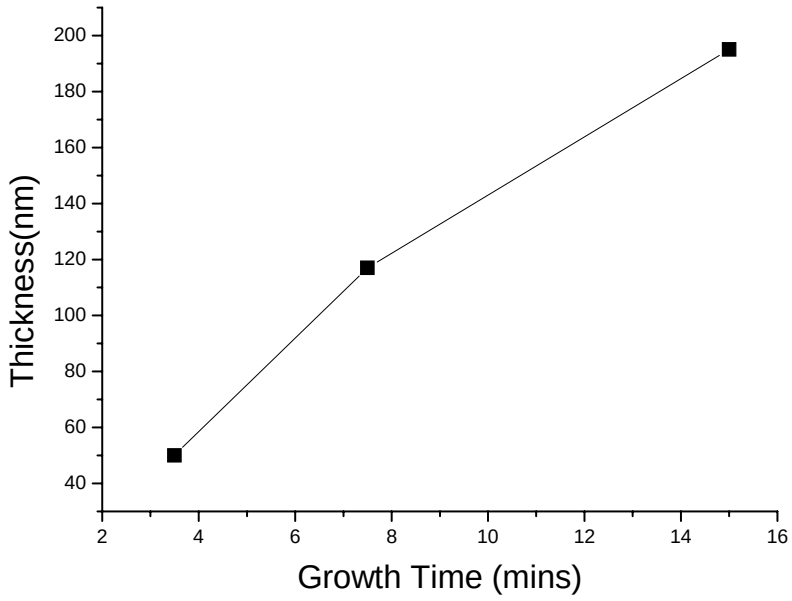


Figure 2.21 Thickness of epi-layer vs. Growth time

2.7 Discussion of the composition of the epi-layer

From the study in previous section, we could see the epi-layer clearly by SEM, however, we are not sure what the composition of the whole layer is. Pure 3C-SiC, or mixture of 6H-SiC?

To understand the point, we applied C-V measurements on the heterostructure samples. In Figure 2.22-2.23, we show the C-V results of samples grown with different thickness of epi-layer, 200nm thick and 50nm thick respectively. (the details of the C-V measurements will be studied in chapter IV "Characterizations").

The interesting phenomenon is in both figures, we found that the peak of 2DEG stayed at 30nm deep position from the surface. That means the 3C-SiC is always about 30nm thick, no matter how long the growth time is.

The only explanation for this is the growth temperature-1350C is too high for the C-face SiC on-axis wafer, so the main growth during the whole epi-process is homo-epitaxy. And the hetero-epitaxy only happened at the "temperature ramping-down" layer, in which the temperature is around 1300C and just the ideal environment for the 3C-SiC nucleation. That is why the 3C-SiC is always same thickness, because the "temperature ramping-down" layers are all same.

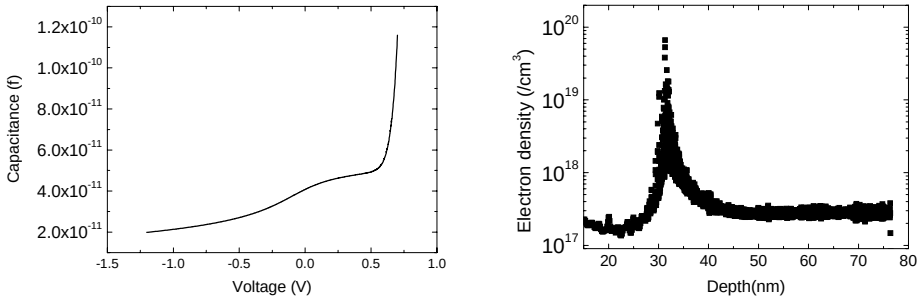
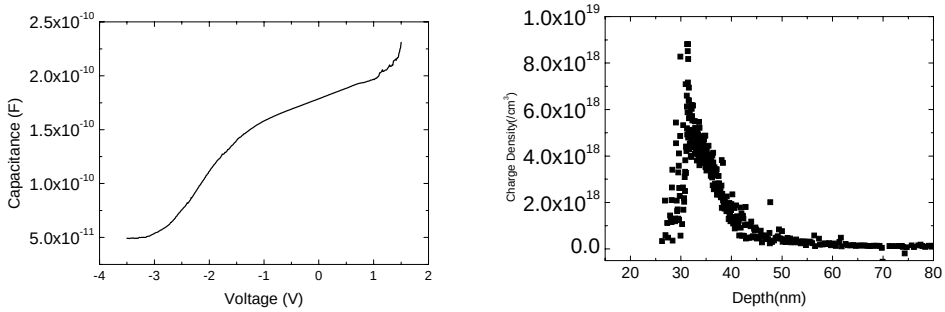


Figure 2.22 Capacitance-Voltage results for the heterostructure samples

Figure 2.22 (Continued)



2.8 Conditions of the islands size dependence

In most heterostructure samples, the dimensions of the islands in 3C-SiC, which are formed due to the two different phases of 3C-SiC, vary from 2-3 um. The boundaries among those islands are critical for limiting the mobility of the heterostructure.

To enlarge those islands, we change the process of temperauture ramping down, shown in Figure 2.24

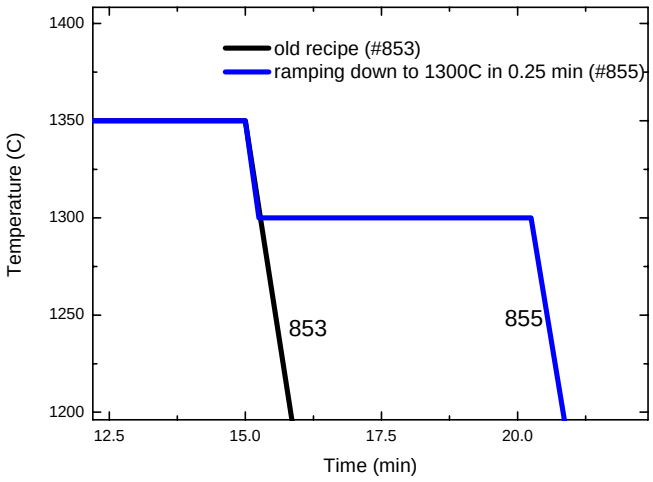


Figure 2.23 Schematic illustrations of the ramping down process in the end of the epi-growth

The black curve is the normal method to ramp down the tempurature, in which we just cut off the flow of reactance (but kept HCl flowing) and let the chamber to cool down to 450C directly.

Base on our previous analysis, we believe that the 3C-SiC growth happened at about 1300C. As indicated by some references, the nucleation density of the 3C-SiC on the top of the terrace of the 6H-SiC substrate is determined by the flow of reactance, the pressure and the temperature. Keeping other factors same, when the temperature increases, the SiC molecule will move faster and the nucleation density will decrease. As a result, the islands will be larger than before. So we changed the ramping down recipe, in which we dropped the temperature to 1300C and keep that for 5 minutes, shown in blue curve in Figure 2.24. The new recipe gave us much larger islands, which is over 10time s bigger than before, shown in Figure 2.25.

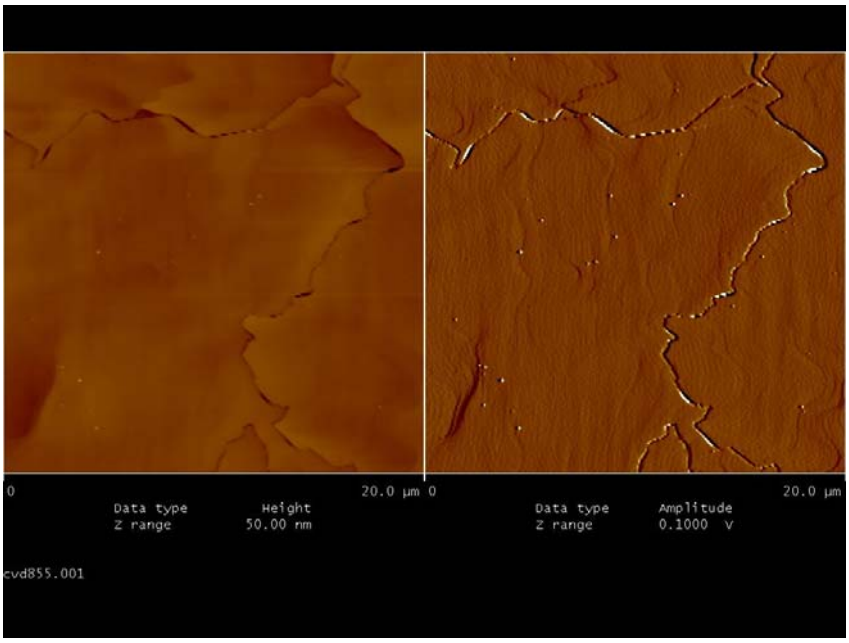


Figure 2.25 Smooth and large island features (size of islands is ~30um)

In summary, growth and characterization of 3C-SiC layer grown on both C-face and Si-face 6H on-axis SiC substrate are shown. By changing different growth conditions,

surface morphology of the epi-layers shows a strong dependence on growth pressure, C/Si ratio, HCl flow and growth temperature. Lightly doping and high quality 3C-layer has been achieved at optimized condition, high pressure, high C-Si ratio and low HCl flow. To reduce the Nitrogen doping at the interface, which is the main source of the low mobility, both HCl etching and Hydrogen etching at different temperature process were investigated and pursued.

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Chapter III Simulations: Self-consistent calculations of 2DEG in the 3C/4H heterostructure

In previous chapter, we learned how to grow SiC heterostructure by CVD system. In this chapter, the new device model of two dimensional electron gas (2DEG) FET based on polytypic SiC has been demonstrated by using self-consistent solutions of the Schrodinger and Poisson equations. Low doped cubic SiC epi-layer is grown on hexagonal SiC semi-insulating substrate. Electrons are accumulated to form two dimensional electron gas at the interface due to the strong polarization charge from the C-face substrate [1]. The variations of carrier density were calculated by change of the Schottky barrier, thickness of 3C layer. The carrier density of 2DEG is found to be as high as 0.9e19/cm^3. The thickness of 3C layer has less effect on the carrier density, but we found the pinch-off voltage strongly depends on the thickness of the 3C layer. Furthermore, we also investigate the structure with different polarization face of substrate, in which two dimensional hole gas are formed at the interface.

3.1 Physics basis of two-dimensional electron gas

The underlying idea of heterostructures is that, at equilibrium, charge transfer occurs across a heterojunction to equalize the Fermi level on both sides. The charge transfer effect makes possible an old dream of semiconductor technologists, i.e., getting conduction electrons in a high purity semiconductor without having to introduce mobility-limiting donor impurities. Undoubtedly, studies on the conduction electrons at the heterointerface are of the most importance. Considering the heterostructures quantum mechanically, the energy, momentum, and wave function of the conduction electrons are quantized in the z direction perpendicular to the

heterointerface, and the conduction electrons become the co-called two-dimensional electron gas (2DEG) [2-4].

In effective mass approximation, the one-electron Hamiltonian is given by

$$H = p^2 / 2m + V(z)$$

Where $p = -i\hbar\nabla$ and a constant isotropic effective mass m has been assumed for simplicity. To determine the eigenfunctions of H, we consider a macroscopic square of side in the L in *xy*-plane and apply periodic boundary conditions in the *x*- and y-directions. Since H is independent of x and y, the eigenfunctions take the form

$$\Psi_{\alpha k}(r,z) = L^{-1}\exp(ikr)\phi_\alpha(z)$$

Where r=(x,y) and k=(k_x,k_y) with both k_x and k_y equal to interger multiples of $2\pi/L$. By substituting equation in the eigenvalue equation for H we find that the eigenvalue associated with $\psi_{\alpha k}$ is

$$\varepsilon_{\alpha k} = \varepsilon_\alpha + \hbar^2 k^2 / 2m$$

$\phi_\alpha(z)$ and ε_α are determined by the 1D Schrodinger equation

$$-\frac{\hbar^2}{2m}\frac{d^2\phi_\alpha(z)}{dz^2} + V(z)\phi_\alpha(z) = \varepsilon_\alpha\phi_\alpha(z)$$

Where $k^2 = k_x^2 + k_y^2$. [5]

3.2 Self-consistent calculation of Schrodinger and Poisson equations

In this section, we consider charge control of the SiC based heterostructure with a Schottky contact on the surface (3C-SiC). The current flow through the reverse-biased Schottky diode is low enough so that the bending of quasi Fermi level can be neglected. Simulation requires that the following parameters be specified: temperature, Schottky barrier height at the sample surface, and doping level and donor ionization

energy for each layer. The layer furthest from the Schottky contact was assumed to be semi-infinite in order that equilibrium conditions can be reached. The model was based on a one-dimensional solution of Schrodinger and Poisson equations in the z direction perpendicular to the heterointerface [5].

The electrostatic potential is related to charge distribution by the Poisson's equation

$$\frac{d}{dz}\left(\varepsilon\frac{d}{dz}\right)V(z) = -q\left[N_d^+ - N_{el}\right]$$

where N_d^+ is the ionized donor density, and N_{el} is the density of conduction electrons.

The ionized donor density N_d^+ is expressed as

$$N_d^+ = \frac{N_d}{1 + 2\exp(-\frac{E_d - E_f}{k_0 T})}$$

where N_d is the donor concentration. The donor binding energy E_d in 3C-SiC is 0.06ev beneath the conduction band edge.

For free electrons, the wave function of the ith subband is determined by the Schrodinger's equation,

$$\left(-\frac{\hbar^2}{2m^*}\frac{d^2}{dz^2} + V(z)\right)\psi_i(z) = E_i\psi_i(z)$$

Under equilibrium conditions, the distribution of two dimensional electrons in each subband obeys Fermi statistics, and the electron density is given by

$$n_{2D}(z) = \sum_i \frac{mKT}{\pi h^2}\left|\psi_i(z)\right|^2 \ln[1 + \exp(\frac{E_f - E_i}{KT})]$$

We also consider the polarization effect in the herterosturctures. In general, in several semiconductor heterostrutures, there exist both the spontaneous polarization and strain-induced or piezoelectric polarization resulted from the lattice mismatch at the interface between two materials [6]. However, in SiC 3C/4H heterostuctures, both of the two polytypes match perfectly. As a result, the piezoelectric polarization vanishes. Further more, the spontaneous polarization of the 3C-type polytype is also zero due to symmetry arguments [7, 8]. So we only need to consider the spontaneous polarization in 4H-type. Some groups have calculated the polarization in 4H, which can cause an electric field $E=3*10^{6}$V/cm in 3C.

Figure 3.1 is the schematic illustrating the electrostatics of the 3C/4H SiC heterojunction. The source and drain in the HEMT structure on the left are assumed to be far enough away from the gate region so that their influence on the heterostructure electrostatics is negligible. Charge neutrality is satisfied in the entire structure [8].

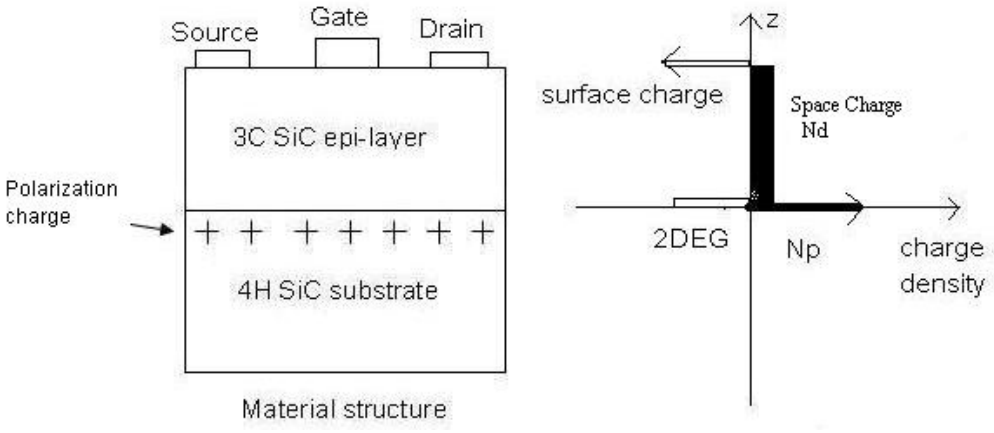

Figure 3.1 the schematic illustrating the electrostatics of the 3C/4H SiC heterojunction

3.3 Results and Discussions

After solving the equations of (1)-(4) by self-consistent method, we got the electron distribution at the interface of 3C/4H heterostructure with C-face semi-insulating substrate, shown in Figure 3.2.

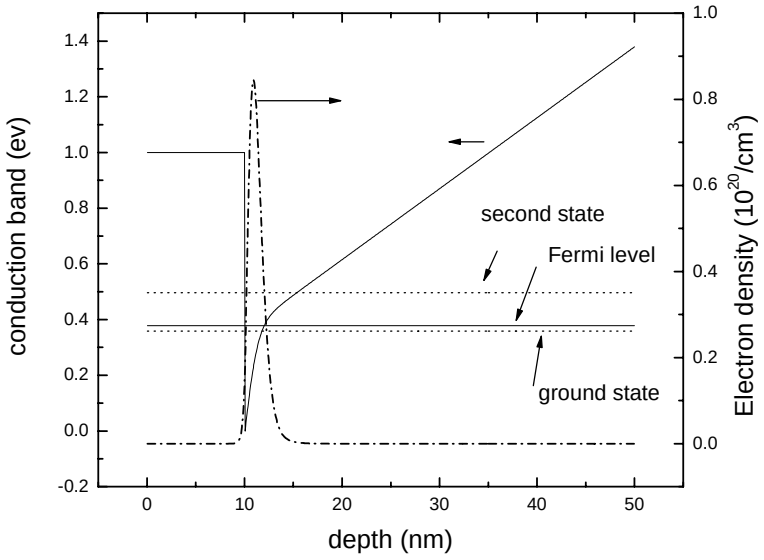

Figure 3.2 Schematic illustrating the distribution of 2DEG at the 3C/4H interface(Dash curve pointing to right), potential profile (triangular solid curve), and positions of energy states and Fermi level (pointing to left).

From the simulation, we can see that the electron concentration is as high as 0.9e20/cm^3 at the interface and two dimensional electron gas density is 1.3e13/cm^2. This high density electron gas comes from the 3C layer and surface state and are trapped by strong spontaneous polarization charge of 4H substrate at the interface. The Fermi level stays between the first two energy states and 3C-layer is fully depleted beyond the interface.

To demonstrate a real device, we need to get pinch-off condition. By varying the surface schocttky bias, the carrier density was changed at the interface. Figure 3.3 shows the variation of 2DEG density with respect of Shocttky barrier for the structure with 40nm thickness of 3C layer. The 2DEG density decreased to 1e7/cm^2 at the bias of 10.7V, which means the 2DEG is fully depleted.

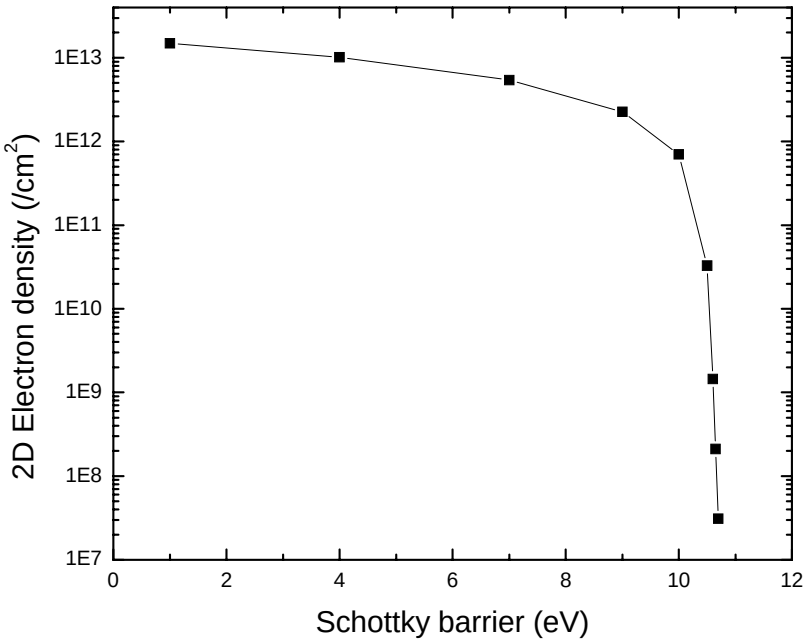

Figure 3.3 The 2DEG density with varying surface barrier illustrating the depletion of the electron gas for the structure with 36nm thick 3C layer. The pinch off-voltage is 10.7 V

We also investigated the effects of the thickness of 3C layer on the variations of the pinch-off condition. By increasing the thickness, we get higher pinch-off bias, shown in Figure 3.4 It demonstrates the 3C layer is fully depleted and electron gas mainly come from the surface and contact. When we fixed the bias, the 2DEG density is not sensitive to variations of the barrier layer thickness.

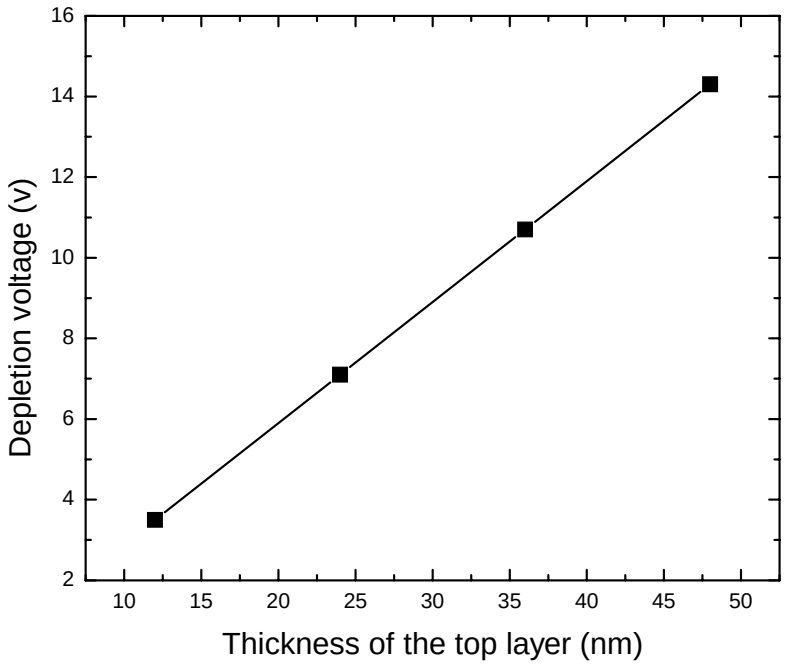

Figure 3.4 Pinch-off voltage with respect to thickness of 3C-layer

Next we make some assumptions for real device modeling. We use saturation velocity in 3C-SiC to be 1e7cm/s [9]. The dependences of saturation current and transconductance with gate voltage for different 3C thickness are obtained, shown in Figure 3.5 and 3.6. From the results we get, it's easy to see that the pinch-off voltage decreases (the absolute value increases) and the transconductance, shown in Figure 3.5, decreases by increasing the thickness of 3C SiC, which means thinner 3C-SiC layer can give us better control of the channel carriers.

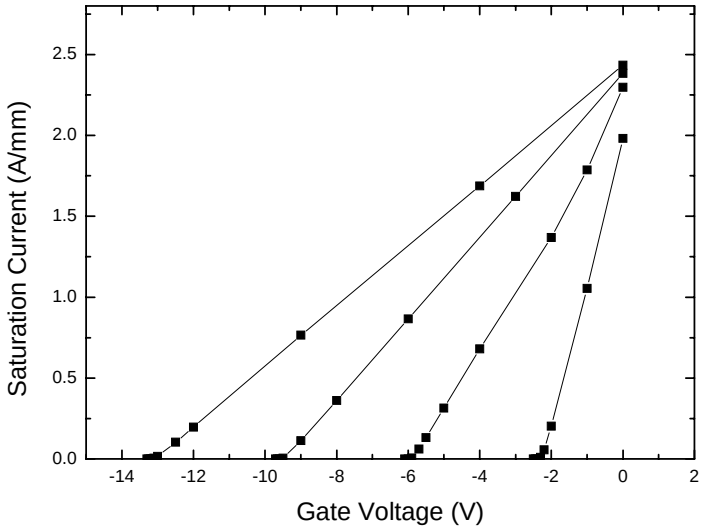

Figure 3.5 Saturation current with respect to different gate voltage for different thicknesses of 3C-layer (12nm-48nm)

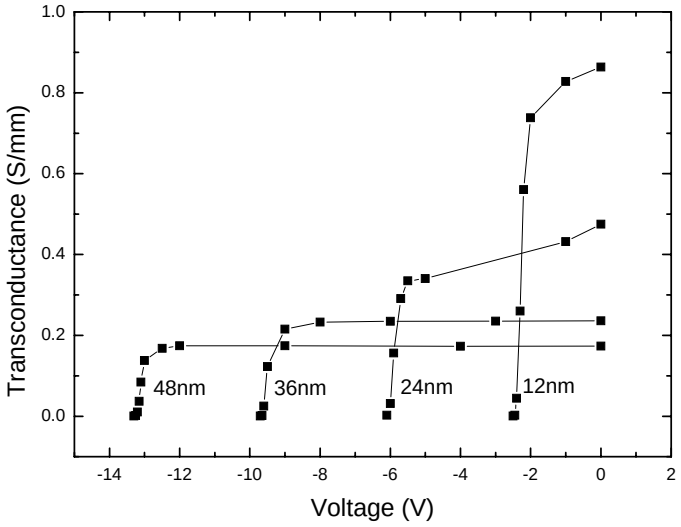

Figure 3.6 Transconductance with respect to gate voltage for different thickness of 3C-layer

3.4 Conclusion

A new device model of a HEMT based on polytypic SiC has been demonstrated by using self-consistent solutions of the Schrodinger and Poisson equations. A low doped 3C SiC epi-layer is considered on 4H SiC semi-insulating substrate. Electrons are accumulated to form a two dimensional electron gas at the interface due to the strong polarization charge from the C-face substrate. The variations of carrier density were calculated by change of the Schottky barrier, thickness of 3C layer. The carrier density of the 2DEG is found to be as high as $1.3\times10^{13}/cm^2$. By proposing real device parameters, we get the dependence of saturation current and transconductance with gate voltage.

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Chapter IV Fabrication of SiC devices

The utilization of wide bandgap semiconductors such as SiC for the fabrication of high-frequency and microwave electronic devices has been of interest to device physicists and researchers for many years [1]. Based on the electronic and thermal properties of the semiconductor material, it has been predicted that devices fabricated from selected SiC polytypes will have a performance superior to that of present devices, and this has motivated a significant development effort. One major focus of this research was the development of process technology.

4.1 Process Integration

a. Photolithography mask

Photolithography technique is employed to produce n+ contact layers in order to obtain good ohmic characteristics. This ion implantation requires the whole process to be adjusted for the implantation step. Additionally, the high activation annealing temperature needed for implantation prevents the conventional alignment mark process using gold (Au) or platinum (Pt) being performed prior to the implantation step.

b. n+ Implantation

In order to obtain good ohmic characteristics, both the source and drain regions were implanted using phosphorus to produce n+ contact layers [1]. The regions were formed by three separate doses (1.3e15 /cm2, 1.1e15 /cm2, and 8.0e14 /cm2) in box profiles to a depth of 0.2 mm with a projected volumetric concentration of 2e19/cm3. A thin sacrificial oxide was deposited on the surface and a patterned Au layer was used as the implantation mask. After implantation, the oxide and Au were removed using HF. The activation annealing was performed at 1300C for 2 hours [2].

c. Mesa Isolation

Active regions were defined by mesa etching. The mesas electrically isolated the active transistors from one another. The Plasma drying etching technique was employed with a photo-resist mask.

d. Ohmic Contact

55nm Ni was deposited and annealed at 980C for 4min 20sec under helium (He) ambient.

4.2 Plasma dry etching

Realization of advanced device structures fabricated from SiC requires the ability to etch this material smoothly, controllably, and with a minimal amount of damage to the underlying material. Methods for dry etching SiC are necessitated by the lack of wet etching techniques which are compatible with SiC device fabrication schemes [3].

The term “plasma etching” most often refers to plasma-assisted etching which occurs at relatively high pressures (e.g., > 10-1 torr) with the sample sitting on the grounded electrode of a parallel plate reactor. This type of reactor is most common among commercially available systems owing to its success in silicon device processing. Alternatively, plasma etching may also be performed in a barrel reactor or downstream from a plasma source where the plasma is generated inductively using rf power or in a microwave cavity. Typically, in the case of plasma etching, only a small sheath potential (10–20 eV) develops on the sample and thus the energy of bombarding ions is relatively low. Therefore, plasma etching processes of this type can be relatively gentle to the underlying semiconductor and tend to be largely isotropic in nature [3, 4].

The strong non-polar bonding of SiC makes it a rather difficult material to wet-etch [4]. Therefore, all of the pattern steps during device processing are carried out with dry etching due to the chemical stability and inertness of SiC in conventional acid or base solutions at normal temperatures. Most of the dry etching processes reported to date have employed reactive ion etching (RIE). The key problems associated with the dry etching process are the control of etch-induced surface damage and contamination. It is well known from Si and GaAs studies that these issues can adversely affect material properties, subsequent processing, and device performance. The process conditions for RIE are characterized by relatively high ion energies, which can create damage to the semiconductor, severe mask erosion, and poor surface morphology through micro-masking effects from backsputtering of the electrode material. High substrate biases commonly associated with RIE processes can also cause significant surface damage. In addition, rough or textured surface morphologies typically result from conventional RIE of SiC due to the clustering of residues which leads to a serious micro-masking problem. To avoid rough surfaces, hydrogen is generally added to the plasma chemistry. Inductively coupled plasma (ICP) and electron cyclotron resonance (ECR) have significant advantages over RIE. ICP processes are generally used for anisotropic deep etching due to the high ion density plasma sources and low process pressure. Operation at low pressure aids directionality of the ion flux. While ICP processes are suitable for deep etching of SiC, ECR plasmas have received attention for electronic materials processing applications. It was reported that high ion density ECR discharges produced much higher etch rates than RIE, and it was not necessary to add hydrogen to the plasma chemistry to obtain smooth surface morphologies. Advantages of ECR plasma etching over conventional RIE include high reactive ion density, low ion energy, and low working pressure. It is expected that low ion energy

in the ECR plasma would provide advantages in surface damage control.

This time we use Oxford PlasmaLab 100 RIE. The Oxford Plasmalab100 is an inductively coupled plasma based system that is configured for deep SiO2 etching. The system consists of one ICP process module connected to a single automated wafer transfer load lock. It is equipped with He backside cooling and has a temperature controlled electrode.

Generally people use metal mask during SiC etching. Using metal masks can get higher etching rate and good selectivity. However, it also could contaminate the surface and introduce more processes during fabrication, like evaporation, lift-off and etching the metal. For device fabrication, we want clean surfaces after etching and simple procedures. In our study, we tried to use photoresist mask, which is simple to make pattern and easily removed.

Photo Resist (PR) SPR220 is spun on the sample by 3000rpm for 30 second with baking at 115^{o}C for 90 second afterwards. The selectivity of 3:1 was achieved between PR and SiC. The stage temperature is 8^{o}C. And we vary the flow of CF_4, flow of Ar, chamber pressure and ICP power to see the change of etching rate and surface morphology. After etching, the photoresist is removed by 1165 and Acetone.

The etching rate was influenced by the flow of the reactants. In this case, we didn't use O_2, which could increase the etching rat but also damage the surface. The fixed condition in etching is shown in Table 5.1. After etching, we see that the etching rate increases via more CF_4 flow, which is shown in Figure 4.1. The selectivity is around 3, which means we could get as high as 900nm etching thickness.

Table 4.1 Fixed condition when CF_4 flow varied

Pressure	5m Torr
Stage temperature	8 C
ICP power	1500W
RIE power	30W
Ar flow	5sccm
Etching time	5min

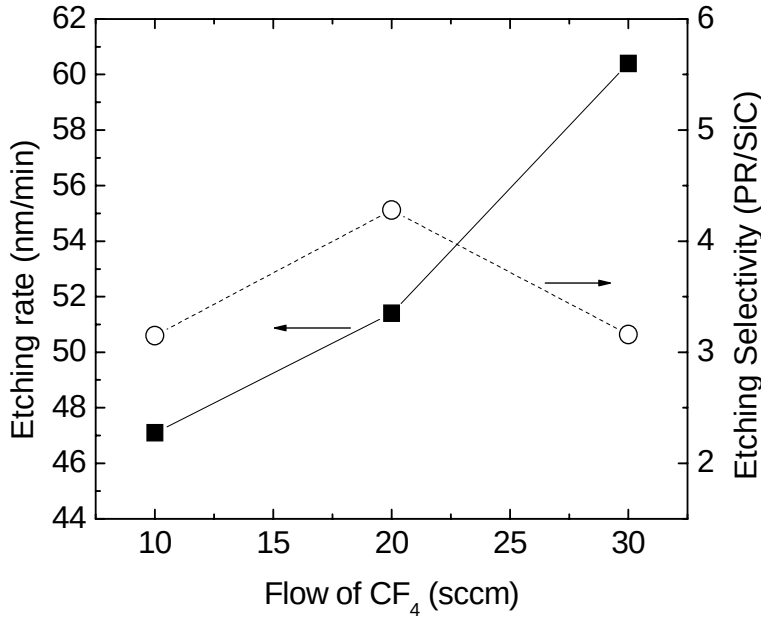

Figure 4.1 Etching rate with respect of flow of CF_4

Figure 4.2 shows the etching rate as a function of Ar flow. Here, we found that the etching rate doesn't change too much by varying the flow of Ar. Also, we increased the pressure from 5m Torr to 10m Torr and get lower etching rate, shown in Figure 4.3.

That could be explained by this: the higher pressure causes shorter free path, and decreases kinetic energy of ions.

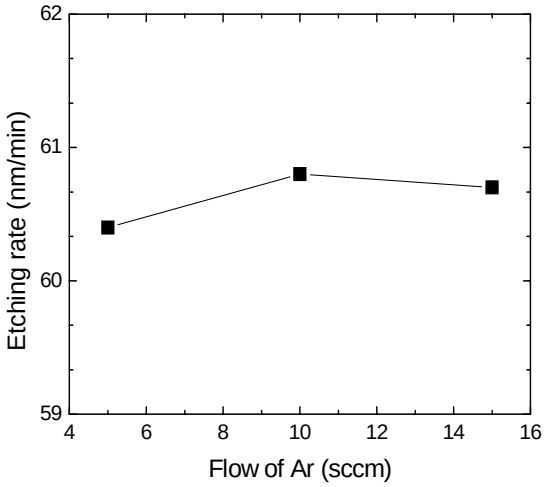

Figure 4.2 Etching rate vs. Ar flow

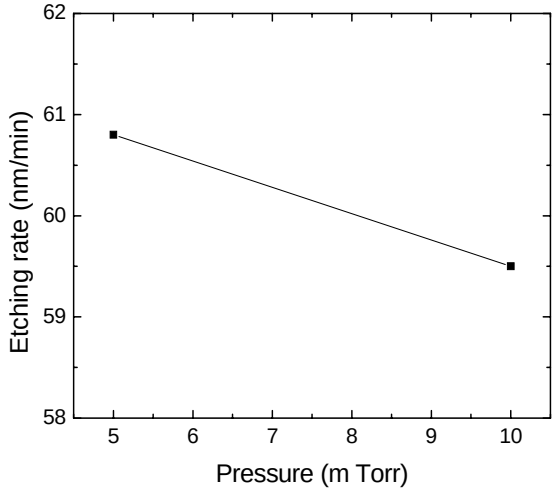

Figure 4.3 Etching rate vs. Pressure

After etching we use Acetone and IPA to remove the PR. The SEM image is shown in Fig.4.4. From that we can see after etching the surface of sample is still very clean.

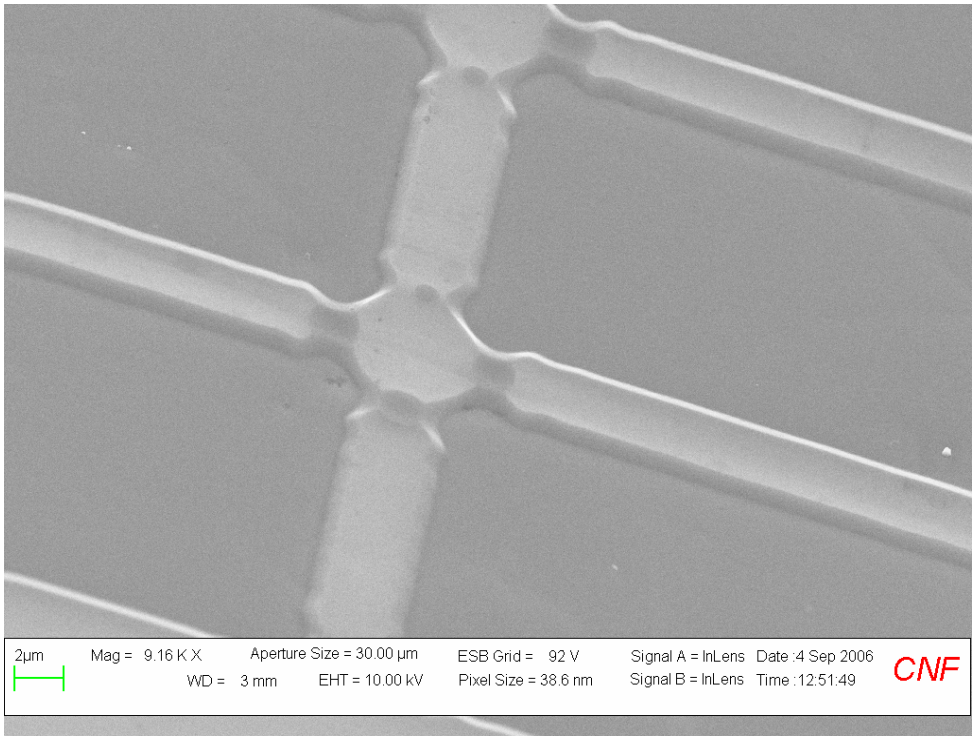

Figure 4.4 SEM image after etching

4.3 Ohmic Contact

TLM patterns had been put on the samples. The spaces among different contacts are 5um, 10u, 15um, 20um, 25um, 30um, 35um. And the contact scale is 50um width and 100um length. Figure 4.5 shows the linearity of the ohmic contacts at room temperature. And figure 4.6 gives the fitting results of the sheet resistance, which is 1600 ohm. The total resistance of the two contacts is 118 ohm, so for each is around 60ohm.

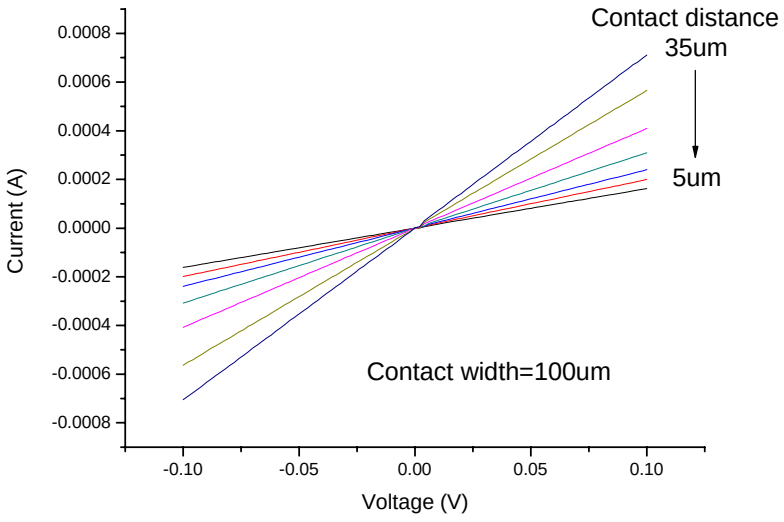

Figure 4.5 Results of TLM measurement

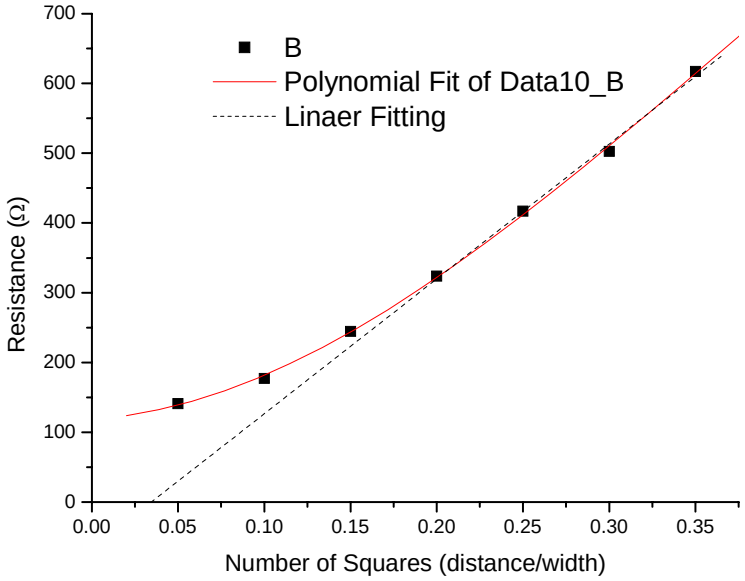

Figure 4.6 Polynomial Fitting of the resistance of the TLM patterns

4. Conclusion

We introduced the process technology of SiC materials and devices. And a new etching recipe for SiC was developed. We use photoresist to be mask and get very good etching selectivity. The etching rate is high and the surface quality is good for device fabrication. The conditions which could affect the etching rate have been studied, like reactance flow and pressure.

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Chapter V Characterization

In this chapter, we are going show some different characterization ways for 3C-SiC/6H-SiC heterostructure samples. The two main approaches are capacitance-voltage and Hall measurements. Those results give strong supports for the existence of two dimensional electron gas in SiC heterostructure. And it is the first time in the world to observe the Quantum Hall effect in SiC system.

SiC wafers are very expensive. As a consequence, for the development of the growth process, regular n+ 4H-SiC wafers, the lowest cost wafers, were used. Electrical measurements for identification of a 2DEG, however, are very tricky to do on these wafers, as the doping is on the order of the expected electron charge. Therefore, as soon as we determined that the process was reproducible, we started growing on semi-insulating substrates. The results presented here are on these semi-insulating substrates.

5.1 Capacitance-Voltage measurements

3C-SiC and 6H-SiC have large conduction band offset (0.7V) and hexagonal SiC exhibit strong spontaneous polarization as GaN, which gave the possibility to form a quantum well at the hetero-junction between these two polytypes [1]. The direction of polarization field is determined by the face type of the 6H-SiC [2]. Two dimensional hole gas (2DHG) in 3C/4H heterostructure which has 3C-SiC layer on Si-face 4H-SiC layer were studied before. To get 2DEG, we need to grow 3C-SiC on C-face hexagonal SiC.

The SiC epi-layers were grown on the C-face semi-insulating 6H-SiC substrate by vertical cold-wall chemical deposition (CVD). The Silane, Propane and HCl were used

to be the reactance and Hydrogen is the carrier gas. Unintentionally doped 6H-SiC buffer layer and 3C-SiC hetero-layer were grown at 1350C. The details for growth will be published in another paper soon. Two samples were prepared, which had 200nm and 50nm epi-layers respectively, shown in Figure 5.1. In SEM picture, we can distinguish the semi-insulating substrate and epi-layer clearly and measure the thickness of the epi-layer. From the structure graph, we could see that the polarization charge (N_p) at the hetero-interface attract the electron from both 3C and 6H SiC, and form 2DEG and depletion region (N_d) in epi-layers [3].

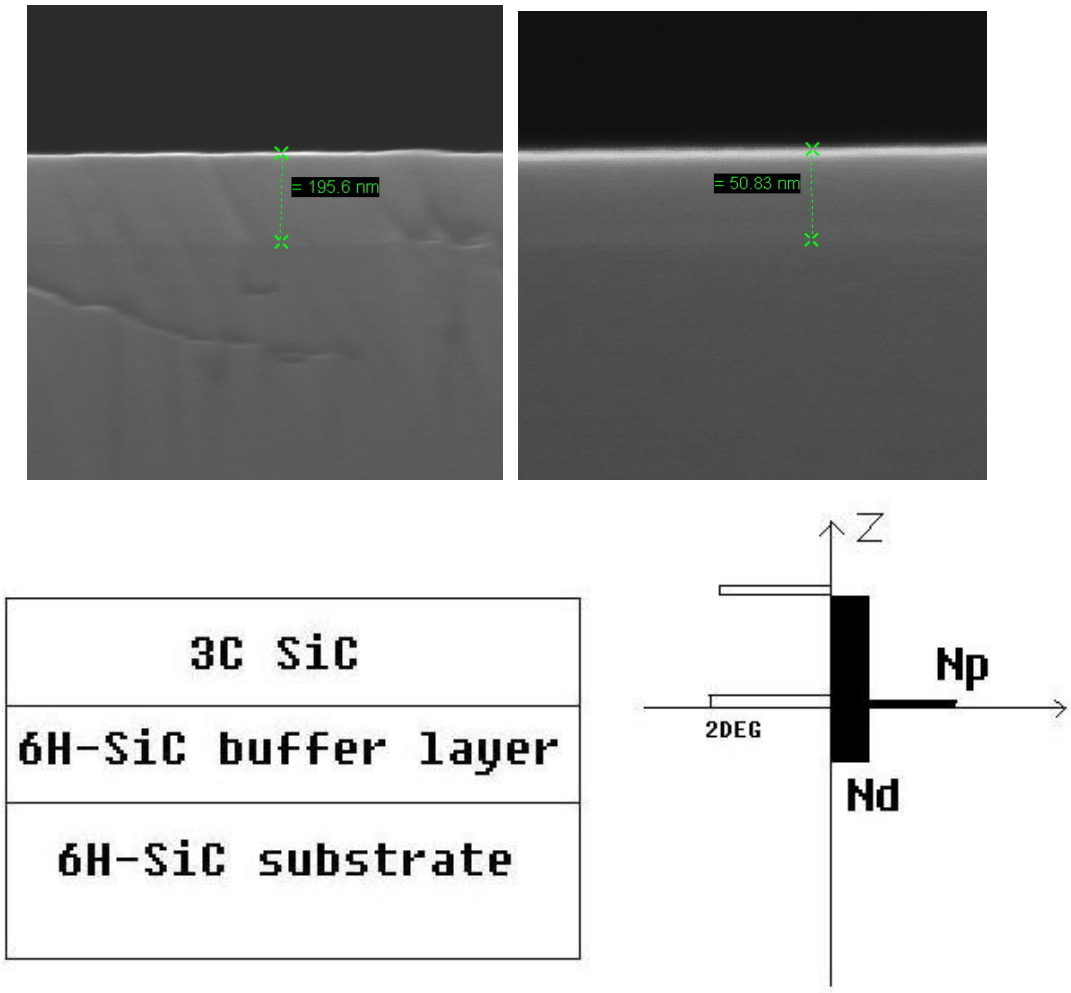


Figure 5.1 SEM pictures for the cross section and schematic illustrating the electrostatics of the 3C/6H SiC heterostructure

The capacitance-voltage (C-V) technique is a powerful method to study the fixed charges in metal-insulator-semiconductor structures and to extract the parameters in semiconductor heterostructures [4-6]. It has been used to investigate the 2DEG density and distribution in AlGaN/GaN heterostructures. The Ti/Au (20A/1500A) dots for the Schottky contact were evaporated on the top of 3C-SiC by using E-beam evaporation. The diameters of the Schottky contacts are 300um and 150um for the two samples respectively. To decrease the leakage current and get accurate results, the C-V measurements were done at low temperature 4K-100K and frequency 500K. The C-V results are shown in Figure 5.2.

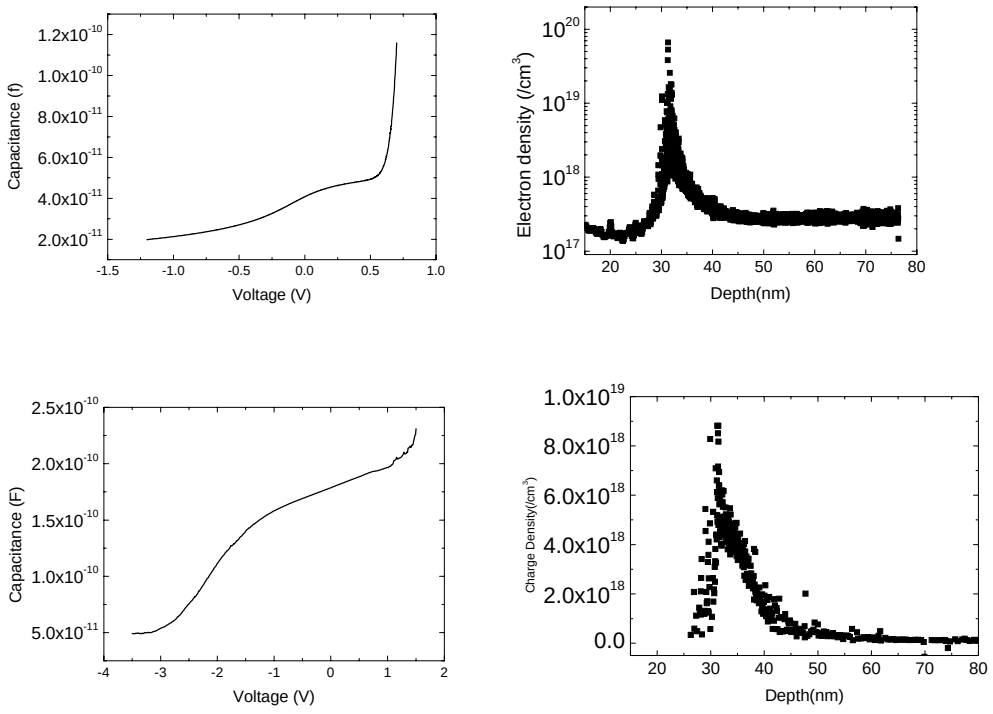


Figure 5.2 The capacitance-voltage results and charge distribution for two 3C/6H SiC heterostructures, “200nm thick epi” and “50nm thick epi”

Figure 5.2 shows the capacitance-voltage results of the “200nm epi” and “50nm epi” samples at 4K. The carrier density could be extracted by using the following

formulas:

$$d = \frac{\varepsilon_r \varepsilon_0 S}{C}$$

$$N = \frac{2\dfrac{dV}{d(1/C^2)}}{\varepsilon_r \varepsilon_0 S^2 q}$$

The electron distribution at the hetero-interface is illustrated on right in Figure 5.2. The peak of the 2DEG is about 33nm depth and the electron density is as high as $4x10^{19}/cm^3$. After integration over the interface, we got the 2D charge density to be $2.5x10^{12}/cm^2$. And we can see that the peak in "200nm epi-layer" sample is sharper than "50nm epi-layer" sample, which shows that the thicker buffer layer gives better quality of the interface. At 4K, the 2DEG in both samples were shown to be at 30nm depth in the epi-layer. When we increased the temperature, the peak of 2DEG shifted to deeper region, shown in Figure 5.3. To see the position of 2DEG clearly, we did 10-periods FFT smoothing on original data, so the peak of 2DEG were lower than Figure 5.2. This was also observed by other people and is believed to be due to the increase of parallel resistance.

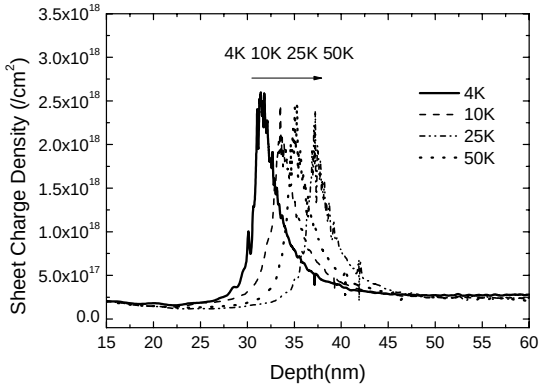


Figure 5.3 The distribution of 2DEG at different temperature. The results were extracted from the C-V data which were smoothed by 10-periods FFT method.

At forward bias, before we started to deplete the 2DEG, we were depleting the 3C-SiC layer at first. We could get the barrier height at different bias and extracted the built-in potential at zero bias.

$$V + V_{bi} = \frac{1}{2} N \varepsilon S^2 q(\frac{1}{C^2})$$

By using formula above, we fitted the curve V with respect to ($1/C^2$) linearly and the intercept is the built-in potential V_{bi}, shown in Fig. 4. We extracted the built-in potential V_{bi}. At 4K, the built-in potential is 0.72V, which is the difference of work function between Au and 3C-SiC.

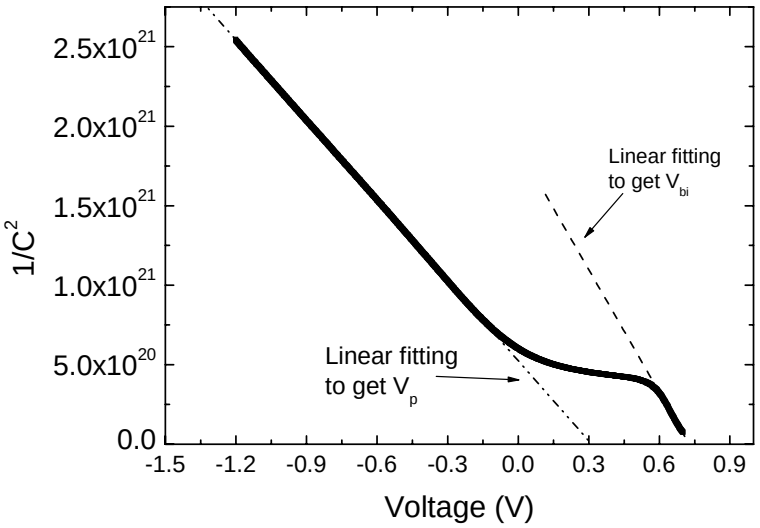


Figure 5.4 The value of $1/C^2$ with respect to voltage at 4K for the "200nm thick epi" sample and the Schottky barrier height extracted at different temperature

As we applied higher negative bias, the 2DEG at the interface will be depleted totally and we started to deplete the buffer layer directly. The potential equilibrium across the heterostructure is illustrated by formula:

$$\int \frac{N_{6H} q x}{\varepsilon} dx + \int \frac{N_{3C} q x}{\varepsilon} dx + \frac{N_P q}{\varepsilon} d_{3C} - V_{offset} - V_{bi} = V$$

The first two terms on left are the potential drop of the depletion region in both 6H-SiC and 3C-SiC. The third term is the potential induced by polarization charge N_p at the interface of the heterojunction and integrated through the whole 3C-SiC layer. The V_{offset} and V_{bi} are the conduction offset between 6H-SiC and 3C-SiC and Schottky barrier height (built-in potential) on 3C-SiC. The V on the right is the voltage we applied across the heterostructure. From the C-V results above, we found the doping level in 3C and 6H SiC.layers are about same, which is $2*10^{17}/cm^3$. So the formula could be simplified as

$V = V_p - V_{offset} - V_{bi} + \frac{1}{2} N q \varepsilon S^2 (\frac{1}{C^2})$, where $V_p = \frac{P_s q d_{3C}}{\varepsilon}$, which is the potential induced by polarization charge.

In Figure 5.4, by fitting the negative voltage part, we extracted the value of V_P to be 0.3+0.7+0.7=1.7V. The thicknes was estimated to be 30nm from the pinch-off condition voltage and the C-V results, and the polarization charge was extracted to be $3x10^{12}/cm^2$. This value agree well with previous measurements of the polarization charge in SiC, and are found to be lower than the theoretically predicted values [7, 8], shown in Figure 5.5 .

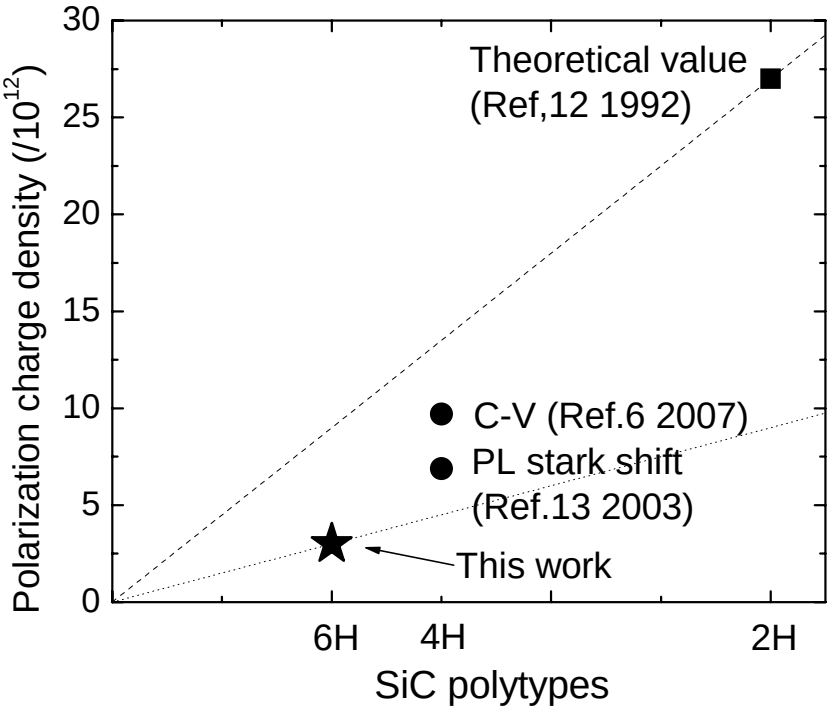


Figure 5.5 Spontaneous polarization field in 6H-SiC obtained different groups

Inclusion, two dimensional electron gas (2DEG) are observed in C-face 3C/6H SiC heterostructure by capacitance-voltage method for the first time. High quality 3C-SiC hetero-layer and 6H-SiC buffer layer was grown on 6H-SiC semi-insulating substrate by chemical vapor deposition (CVD). The carrier density of the 2DEG is found to be $2.5 \times 10^{12}/cm^2$. By semi-classical analysis of the electrostatics, we extracted the spontaneous polarization charge in 6H-SiC to be $3 \times 10^{12}/cm^2$.

5.2 Quantum Hall Measurements

We report the observation of the quantum Hall effect in a two dimensional electron gas (2DEG) at a C-face 3C/6H SiC polytype heterostructure. Quantum hall plateaus and

Shubnikov-de Haas oscillations were observed at 1.5 K and high magnetic fields, indicating the presence and confinement of a 2DEG. The measured mobility of the 2DEG is 2000cm^2/Vs and the electron sheet density is $2.7\times10^{12}/cm^2$.

Two dimensional electron gas (2DEG) exhibits the quantum Hall effect (QHE) when it is placed under a strong perpendicular magnetic field. In this chapter, we reviewed the theoretical quantum Hall transport measurement and extracted the physical parameters of 2DEG in SiC heterostructure through it [9].

If an electric current flows through a conductor in a magnetic field, the magnetic field exerts a transverse force on the moving charge carriers which tends to push them to one side of the conductor. A buildup of charge at the sides of the conductors will balance this magnetic influence, producing a measurable voltage between the two sides of the conductor. The presence of this measurable transverse voltage is called the Hall effect [10].

In 1985 Klaus von Klitzing won the Nobel Prize for discovery of the quantised Hall effect. For a two-dimensional metal or semiconductor, when the Hall effect measurement is operated at low temperatures, a series of steps appear in the Hall resistance as a function of magnetic field instead of the monotonic increase. If a magnetic field is applied perpendicular to the plane of the 2DEG, the electron trajectories will be a set of circles around the lines of field. It can easily be shown that electrons perform these orbits at the cyclotron frequency $\omega c=eB/m$. The contribution from in-plane motion to the energy then becomes quantised in units of the cyclotron energy $E=E_i+(n+1/2)\hbar\omega$ and Landau levels (LL) are formed. The energy is thus completely defined by the subband index i and the Landau level index n. As the magnetic field is increased the LL separation increases. (http://www.warwick.ac.uk/~phsbm/qhe.htm)

In the absence of magnetic field the density of states in 2D is constant as a function of energy, but in field the available states clump into Landau levels separated by the cyclotron energy, with regions of energy between the LLs where there are no allowed states. As the magnetic field is swept the LLs move relative to the Fermi energy. When the Fermi energy lies in a gap between LLs electrons can not move to new states and so there is no scattering. Thus the transport is dissipationless and the resistance falls to zero.

High Magnetic Field Instrument

In this work, we used Oxford Variable temperature inserts with temperature range 1.5 to 300K (VTI). VTI use an external pump to pull liquid helium from the cryostat reservoir through a heat exchanger fitted with a calibrated thermometer and heater. The flow rate is adjusted by a room temperature valve and the cooling power balanced with the heater. Both the heater and flow valve can be controlled electronically to give helium gas at the correct temperature.

The operation procedure to cool down the VTI is as follows:

1. Pump out the IVC (inner vacuum chamber) and OVC (outer vacuum chamber) to at least 5e-6Torr.
2. Flow the He gas into the sample space with the needle valve open and wait until the pressure reaches around 3psi and then stop flowing gas and monitor the sample space pressure. If it doesn't fall, then the needle valve tube is clogged (and need to be fixed before cooling down). If the pressure falls at a reasonable rate, then start flow He again and, while the gas is still flowing, close the needle valve and over pressure the sample space to 2-3 psi. If this pressure doesn't hold, there is something wrong with the needle valve and you should address this before cooling down.

3. Next, precool the He jacket by filling it with liquid N2 (use the leftmost of the two ports because that's the one which fits into a cup in the fridge which accesses the bottom of the dewar) until the magnet is submerged. A typical cool down was recorded below.

   10:45pm 182.9Ω

   10:50pm 184.3Ω

   10:55pm 189.3Ω

   11:00pm 204.6Ω

   11:05pm 206.4Ω

   11:25pm 206.4Ω (LN2 temp)

4. Then wait for 12 hours to let things to equilibrate. Now it's ready to transfer the LN2 out of the He jacket port into the LN2 jacket. Do this by putting a transfer tube in the leftmost He jacket port and connecting it to the LN2 jacket via a latex tube. Then put a tube down the rightmost port and blow N2 gas down to force the LN2 into the LN2 jacket. While you are doing this, you should be monitoring the magnet resistance. Once it starts to drop, stop the gas flow and fill up the rest of the LN2 jacket directly from an LN2 dewar. Then flow some more N2 gas into the H2 jacket ot make sure all the LN2 in the H2 jacket has boiled off.

5. Now we are ready to transfer liquid He into the He jacket. It should take around one 60L dewar to fill the fridge up to around 80%., because it will take a while before the H2 meter sartes to read anything. While you are transferring, you should work the needle valve by taking off the blue casing and turning the middle of the valve by hand (Note: the blue casing must be attached in order to turn the valve remotely using the temperature controller outside the shielded room). Once the needle valve seems to work,

you can put the casing back on. A typical transfer goes as follows:

10:25pm 218.7Ω

10:30pm 278.9Ω

10:35pm 380Ω

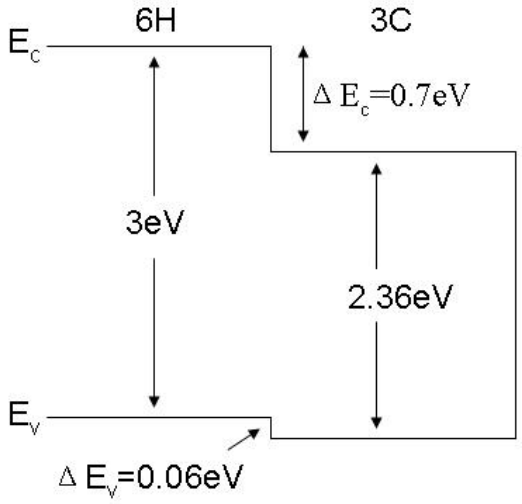
10:40pm 1028Ω

After another 5-10 minutes, the He meter should start to read something. Once the He meter stops increasing (around 80%) stop the transfer (the dewar is now empty), and you are done and can run the VTI in normally.

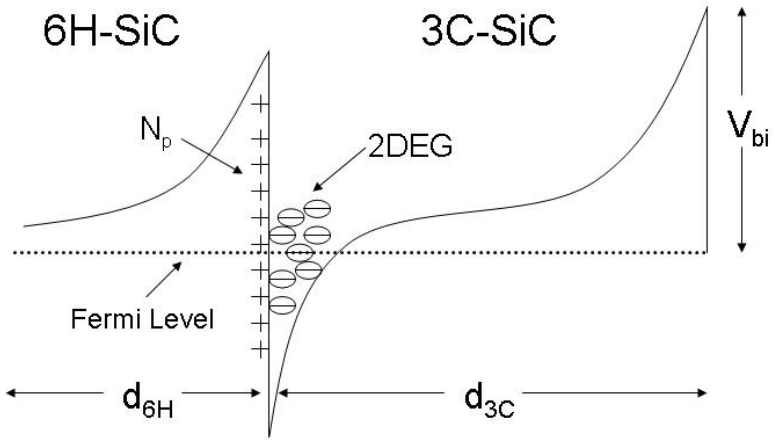
Such a SiC polytype heterojunction has been both theoretically proposed and experimental observed. Previous measurements have established the persistent conductivity of this structure at low temperatures, although the confinement within a 2DEG was less clear. In this section, we provide direct evidence for the confinement of the 2DEG in the form of quantum Hall and Shubnikov-de Haas measurements in a C-face 3C/6H SiC heterostructure at low temperature and in magnetic fields up to 10 T.

Our SiC epi-layers were grown on the C-face semi-insulating 6H-SiC substrates by vertical cold-wall chemical vapor deposition (CVD). Silane, propane and HCl were used as reactants in a hydrogen carrier gas. An unintentionally doped ($\sim 2\times 10^{17}/cm^3$ n-type as determined by capacitance-voltage measurements) 200nm thick 6H-SiC buffer layer and a 3C-SiC hetero-layer were grown at 1350°C and 200Torr at a growth rate ~0.8μm/hr. Figure 5.6 shows of diagram of the band offsets for this heterostructure. Phosphorus-implanted contact well regions were activated at 1350°C. The wafers were then fabricated in Hall bar geometry with high-purity Ni Ohmic

contacts alloyed at 1000°C. Typical Hall bar geometries with lengths of 100um and widths of ~5um were used.



(a)



(b)

Figure 5.6 (a) Band diagram for 6H-SiC and 3C-SiC, and (b) schematic illustrating the electrostatics of the 3C/6H SiC heterostructure at equilibrium, where N_p is the positive polarization charge at the C-face of SiC

Magnetotransport measurements were performed over the magnetic-field range 0–10 T and temperatures 1.5 K to 100 K, as shown in Figure 5.7 and Figure 5.8. In Figure 5.7 we plot the variation of the longitudinal resistance R_{xx} from 1.5 K to 100 K. At low temperatures, when the magnetic field is below 1 T, we observe negative magnetoresistance, which can be identified with weak localization in the disordered semiconductor system. At higher temperatures, electron scattering increases, and reduces the extent to which this localization phenomenon is observed.

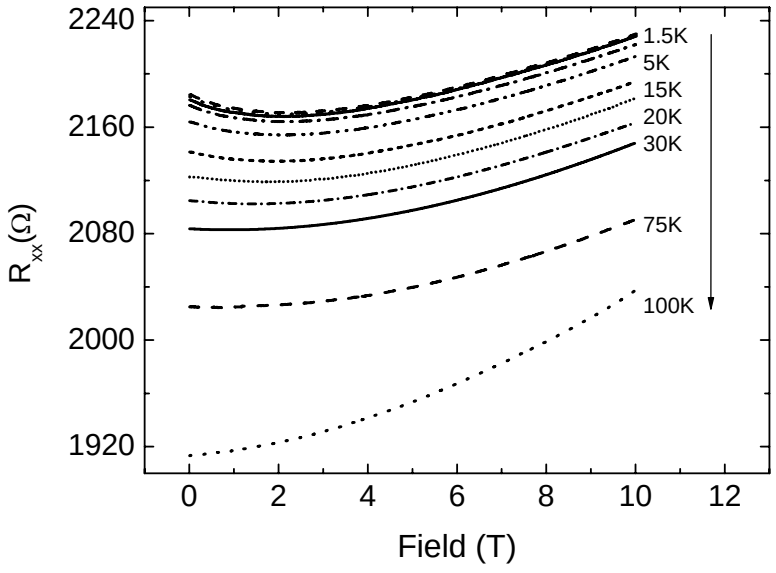
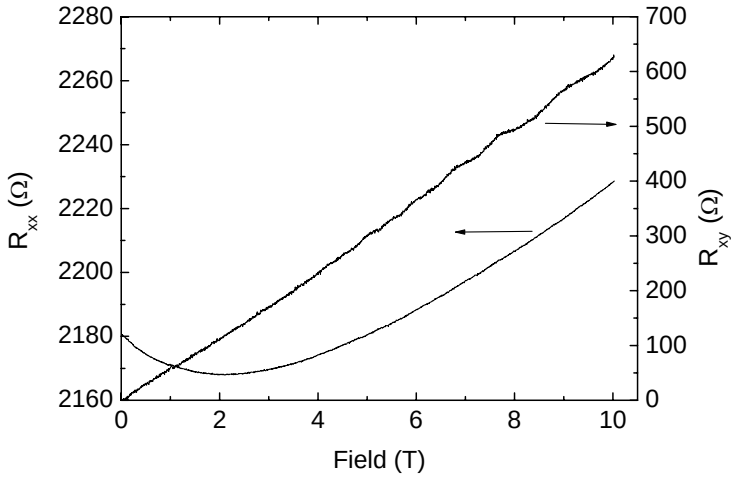


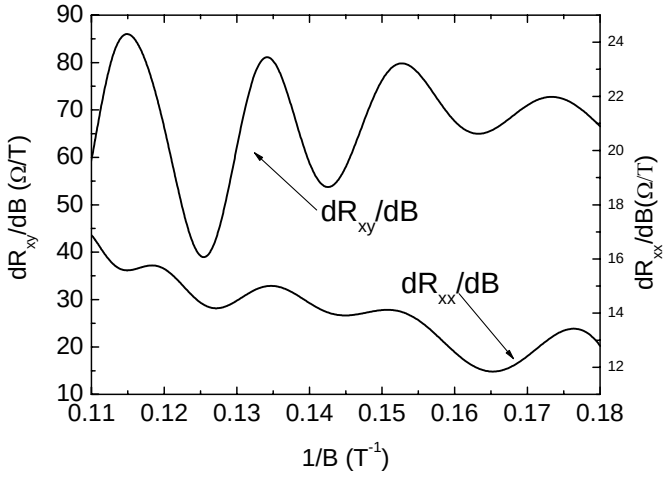
Figure 5.7 R_{xx} as a function of the magnetic field
up to 10 T at different temperatures

Figure 5.8a shows the measured R_{xx} and transverse resistance R_{xy} as a function of magnetic field at 1.5 K. Quantum Hall plateaus (QHP) in R_{xy} can be observed. However, in R_{xx}, the amplitude of the oscillations is weak. By taking derivative of R_{xy} and R_{xx} with respect to magnetic field, we can clearly identify the periods the quantum Hall plateaus in R_{xy} and Shubnikov-de Haas (SdH) oscillations in R_{xx} as a function of

1/*B* (Figure 5.8b). The QHP and SdH oscillations indicate the presence of a well-confined 2DEG.



(a)



(b)

Figure 5.8 (a): Longitudinal magnetoresistance R_{xx} and transverse magnetoresistance R_{xy} in 3C/6H SiC heterostructures as a function of magnetic fields oriented normal to the heterointerface at 1.5 K. (b): $d(R_{xy})/dB$ and $d(R_{xx})/dB$ as a function of 1/*B*, after FFT smoothing

Observation of the QHPs requires that the thermal energy broadening kT and the scattering-induced energy broadening $\hbar/\tau$ be smaller than the Landau level spacing $\hbar\omega=\hbar eB/m^*$, where k is Boltzmann's constant, T is the temperature, τ is the momentum relaxation time, B is the magnetic field, and m^* is the effective mass. The condition $\hbar\omega > \hbar/\tau$ is equivalent to $\mu B>10^4 \mathrm{cm}^2\mathrm{T/Vs}$, where μ is the carrier mobility $\mu=e\tau/m^*$. Figure 5.8 shows that the threshold magnetic field to observe the QHPs is ~5T. Based on the condition for the mobility, this provides an estimate μ~2000 cm^2/Vs.

Similarly, the 2DEG sheet density can be obtained from the periodicity of the QHPs [11], which is periodic in $1/B$:

$$N_{2DEG} = \frac{2e}{hP(1/B)}$$

where $P(1/B)$ is the period of the oscillation with respect to $1/B$ and h is Planck's constant. From equation (1) and Figure 5.8, we calculate the sheet density of the 2DEG to be $(2.7\pm0.2) \times 10^{12}/\mathrm{cm}^2$. This agrees well with capacitance-voltage measurements of the carrier density in these heterostructures.

In summary, we report the observation of the quantum Hall effect of a 2DEG in a SiC heterostructure. Clear quantum Hall plateaus and Shubnikov-de Haas oscillations were observed at 1.5 K and high magnetic field in a C-face 3C/6H SiC heterostructure, which indicates the presence and confinement of a 2DEG. The mobility of the 2DEG is ~2000 cm^2/V.s and the electron sheet density is $2.7\times10^{12}/\mathrm{cm}^2$. These results show that the 2DEG formed in 3C-SiC/6H-SiC heterostructures is comparable to the 2DEG in AlGaN/GaN structures in both sheet density and mobility, with the added benefits of lattice/thermal matching, making the SiC polytype heterostructure a promising candidate for HEMTs.

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