

HIGH MOBILITY OF SPUTTERED $\text{In}_2\text{Ga}_2\text{ZnO}_7$ (IGZO) THIN FILM
TRANSISTORS (TFTs)

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HIGH MOBILITY OF SPUTTERED InGaZnO₄ (IGZO) THIN FILM TRANSISTORS (TFTs)

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Amorphous In-Ga-Zn-O (a-IGZO) thin film transistors (TFTs) hold great potential for large area and flexible electronics. In addition to amorphous IGZO, a partially crystallized form of IGZO, referred to as c-axis aligned crystalline (CAAC) IGZO has been demonstrated, retaining the excellent uniformity of the amorphous phase while improving stability and exhibiting extremely low leakage current. Current research is focused on improving both the mobility and stability of IGZO TFTs. In this work, we seek to improve the electrical performance using controlled deposition and annealing techniques, and to understand the mechanisms for observed mobility improvements.

We demonstrate a dual layer IGZO TFTs that addresses both stability and performance issues when compared to single layer structures. Devices consisted of a 310°C deposited CAAC 20 nm thick channel layer capped by a second, 30 nm thick, 260°C deposited amorphous IGZO layer. The TFT exhibits a saturation field-effect mobility of $\sim 20 \text{ cm}^2/\text{Vs}$; exceeding by $>30\%$ the mobility of 50 nm thick single layer reference TFTs fabricated with either a-IGZO or CAAC IGZO. The deposition temperature of the amorphous layer influences the mobility of the underlying CAAC transport layer. Deposited at room temperature (RT), the mobility in the 310°C deposited CAAC layer is initially low ($6.7 \text{ cm}^2/\text{Vs}$), but rises continuously with time over 58 days to $20.5 \text{ cm}^2/\text{Vs}$, comparable to the value observed when the amorphous layer was deposited at 260°C. The findings are consistent with a hypothesis that the top amorphous layer has a higher solubility for impurities and/or structural defects than the underlying nanocrystalline

transport layer and that these defects can equilibrate even at room temperature. The rate of equilibration is consistent with the known diffusivity of hydrogen.

We demonstrate properties of IGZO TFTs fabricated using laser spike annealing (LSA) with a scanned continuous wave CO₂ laser. For peak annealing temperatures near 430°C and a 1ms dwell, TFTs exhibit saturation field-effect mobilities above 70 cm²/Vs with V_{on} near -3V. This value is over 4 times higher than furnace-annealed control samples (~16 cm²/Vs). This behavior is not due to large-scale structural change of the IGZO, as X-ray data shows no change for LSA anneals up to 800°C for 1-2 ms. However, the mobility of those devices decay from ~50 to ~10 cm²/Vs in 10 and 3 days when storing at room temperature and 50°C, respectively. The activation energy of mobility decay constant is estimated to be ~0.6 eV, which is consistent with the activation energy of hydrogen diffusion in a-IGZO. A model linking hydrogen donors which migrate to passivate and deactivate trap states associated with oxygen vacancies after the optimized LSA anneal is proposed to explain the high mobility. This mobility is also shown to be comparable to the estimated trap-free mobility in oxide semiconductors and suggests that shallow traps can be deactivated by transient thermal annealing under optimized conditions. The observed 75 cm²/Vs is also now a new lower limit to the trap-free mobility of IGZO. The processing enhancement may provide a path to achieve even higher performance in this promising thin-film low temperature semiconductor.

BIOGRAPHICAL SKETCH

Chen-Yang Chung graduated from Chemical Engineering with a minor in Economic from National Taiwan University in 2010. At the National Taiwan University, he completed two projects in Prof. Chung-Hsin Lu's group. The first project involved the mechanism of nest-like photoluminescence in $\text{YBO}_3 : \text{Tb}^{3+}$ nanoparticles formed by the microemulsion-mediated hydrothermal method, and the second focused on the synthesis of photocatalyst BiVO_4 via a reverse-microemulsion technique. After serving as a lieutenant in Taiwan Air Force for one year, he came to Cornell University to join Prof. Michael Thompson's group in 2011. At Cornell, his work has focused on IGZO TFT including both device fabrication and materials characterization. He successfully made ultra-high mobility IGZO TFTs with CO_2 Laser Spike annealing. He interned with TSMC in Hsinchu, Taiwan and Applied Materials in Gloucester, MA, where he gained industrial perspective and research applications. He will start working in Intel Corporation in Portland, OR after he graduates from Cornell.

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TABLE OF ACRYNUMS

CB.....	Conduction band
VB.....	Valence band
VBM.....	Valence band maximum
CBM.....	Conduction band minimum
TFT.....	Thin-film transistors
XPS.....	X-ray photoelectron spectroscopy
CAAC.....	c-axis aligned crystalline
C-V.....	Capacitance-voltage
I-V.....	Current-voltage
IGZO.....	In-Ga-Zn-O
a-IGZO.....	Amorphous In-Ga-Zn-O
a-Si:H.....	Hydrogenated amorphous silicon
LSA.....	Laser spike annealing
XRD.....	X-ray diffraction
CHESS.....	Cornell High Energy Synchrotron Source
CCD.....	Charge-coupled device
AOS.....	Amorphous oxide semiconductor
DOS.....	Density of states
DFT.....	Density function theory
V_{on}	Turn on voltage
μ_{sat}	Saturation field-effect mobility
S.S.....	Subthreshold slope

S/D.....Source and drain
P_{H2O}.....Partial pressure of water vapor
RT.....Room temperature
UV.....Ultra-violet
V_{DS}.....Drain to source voltage
V_{GS}.....Gate to source voltage
I_{DS}.....Drain to source current
DLTS.....Deep level transient spectroscopy

CHAPTER I

I. BACKGROUND AND INTRODUCTION

1.1 Introduction

Amorphous semiconductors, primarily a-Si, have dominated the solar cells and active-matrix (AM) flat-panel display markets. Single-crystalline semiconductors, typified by c-Si, are generally unsuitable for such applications because they cannot be uniformly formed over large areas ($>1 \text{ m}^2$) at low temperature (e.g. $< 400^\circ\text{C}$) on glass or plastic substrates. Due to defect trapping and carrier scattering on grain boundaries in polycrystalline materials, amorphous materials such as hydrogenated amorphous silicon (a-Si:H) have been used more widely for large-size applications. However, the drawbacks of low mobility ($< 1 \text{ cm}^2/\text{V s}$) and the instability under electric stress and photo-illumination still limit a-Si:H based devices in more advanced circuit applications. [1]

In 2004, Hosono reported that an amorphous oxide semiconductor (AOS) with the composition a-InGaZnO_4 (a-IGZO) could be used in the fabrication of transparent and flexible thin film transistors (TFTs) with significantly improved performance compared to conventional a-Si:H based TFTs [2]. Research on IGZO has improved the performance of IGZO TFTs by optimizing channel layer deposition parameters [3], source/drain contact resistance [4], post-deposition annealing [5][6], and dielectric materials [7][8].

In this thesis, I discuss two new techniques to fabricate high mobility IGZO TFTs. The first one is based on a dual layer CAAC (c-axis aligned crystalline)/amorphous IGZO, the other one on post-deposition annealing by LSA. The observed mobility of $>70 \text{ cm}^2/\text{Vs}$ in the LSA annealed TFTs is now a new lower bound on the trap-free IGZO mobility. The mechanisms

controlling the mobility of IGZO TFTs structures are discussed.

1.2 Advantage of Amorphous Oxide Semiconductor (AOS)

Amorphous semiconductors are widely used in the fabrication of active matrix displays. For the past 30 years, hydrogenated amorphous silicon (a-Si:H) based TFTs have been used extensively. However, the relatively low mobility ($\sim 1 \text{ cm}^2/\text{Vs}$) and the instability under electric field bias stress and illumination increasingly limits a-Si:H devices use in advanced applications. Compared to conventional a-Si:H, amorphous InGaZnO_4 (a-IGZO) devices exhibit significant improvements in electrical performance and hence are considered to be a promising candidate for future active-matrix flat-panel displays (AM-FPD). The low mobility of a-Si:H is attributed to the directional nature of the tetrahedral Si sp^3 orbitals shown in Fig. 1-1 (a), which restricts the transport of the electrons in the matrix. In contrast, the dominant spherical orbitals of amorphous oxide semiconductor (AOS) are shown in Fig. 1-1 (b). In AOS, the conduction bands is primarily spherical s-type in nature and hence the transport of electrons through the matrix is not as restricted as that of directional orbitals. Moreover, AOS are insensitive to bond angle variance of metal-oxide-metal chemical bonds due to structural randomness inherent in amorphous materials [9].

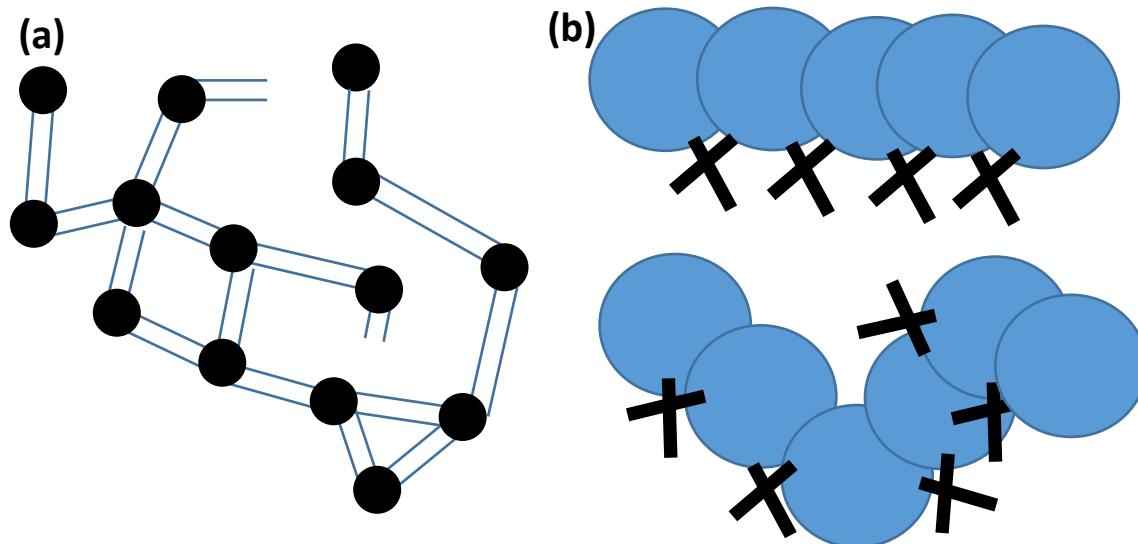


Figure 1-1. (a) sp^3 hybridized orbitals of $a\text{-Si:H}$ and (b) spherical orbitals of AOS.

Because of the amorphous characteristic, AOS also possess the advantage of low processing temperature and no grain boundaries. The absence of grain boundaries eliminates trapping of electrons at specific defect structures and generates a more uniform set of properties for large area flat panel displays.

1.3 The feasibility of AOS device fabrication in industry

Hosono proposed several candidates elements for AOS materials, including Zn, Cd, Hg, Ga, In, Ti, Ge, Sn and Pb. After excluding the toxic and rare elements among the candidate elements, Zn, In, Ga and Sn remained with potential to be used in industry. Table 1 shows several viable compounds based on these four cations. Most of these were eliminated as candidates because of disadvantages in properties or costs. Tin-containing compounds, Zinc-Tin-Oxide (ZTO) and Tin-Gallium-Zinc-Oxide (TGZO) are difficult to etch during fabrication. Although the mobility of Indium-Gallium-Oxide (IGO) and (Indium-Gallium-Zinc-Oxide) IGZO are similar, IGO is much

more expensive than IGZO because of the higher fraction of expensive In. In Indium-Zinc-Oxide (IZO) and Zinc Oxide (ZnO), the In-O and Zn-O bonds are too weak to prevent oxygen from escaping from the matrix, resulting in the generation of excess oxygen vacancies. This makes it difficult to turn the TFTs off because of electron doping arising from the excess oxygen vacancies [10].

Table 1 Comparison of practice AOS compounds based on Zn, Ga, In and Sn

Compound	Etch	Mobility	Transistor turn-off	Price
ZTO	Difficult	-	-	Low
TGZO	Difficult	-	-	Low
IGO	Easy	Good	Easy	High
IZO	Easy	Very good	Difficult	Moderate
ZnO	Easy	Good	Difficult	Low
IGZO	Easy	Good	Easy	Moderate

1.4 Advantage of IGZO as a candidate AOS materials

The incorporation of Ga in IZO actually helps to suppress oxygen vacancies since the Ga-O bond is stronger than Zn-O and In-O bonds. By bonding more strongly with oxygen, the undesired electron doping is avoided. A comparative study between a-IZO and a-IGZO has shown that IGZO can have two orders of magnitude lower carrier concentrations than a-IZO in the off state [11]. Moreover, the crystallization temperature of the multi-component IGZO is higher than the binary ZnO because of the more complex structure [12]. This allows higher processing temperature while retaining the amorphous structure. Theoretically, the mobility should be in the range of 10~50 cm²/Vs, dominated by indium in the amorphous ZnO matrix. In IGZO, the valence band is formed primarily by O 2p and Zn 3d-orbitals, while the conduction

band is formed by the s and p orbitals of the three metals with some influence by the O 2p-orbitals. The mobility of IGZO increases with the fraction of In_2O_3 , in agreement with Hosono's model since In^{3+} has the largest ionic radius among the metal cations. Finally, IGZO has a wide bandgap ($\sim 3\text{eV}$) and is highly transparent to visible light (with transmittance over 90%). This property opens up to new application including transparent electronics and "see-through" displays. Currently, IGZO is the only material which has been demonstrated to satisfy a balance between high mobility and large area uniformity [10].

1.5 Percolation conduction model and energy band diagram

Nomura et al. proposed a percolation conduction model for electron transport in IGZO [13]. The bumpy landscape shown in Figure 2-2 [14] is the potential energy barriers at the IGZO conduction band minimum (CBM) associated with the traps states and random Ga^+ and Zn^+ ions distribution near the CBM.

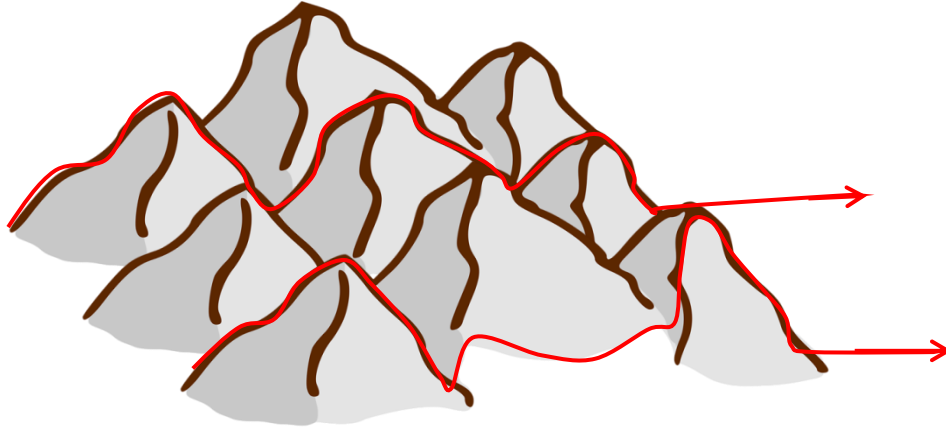


Figure 1-2. The percolation conduction model for electron transportation in IGZO. The bumpy surface represents potential energy barriers at the conduction band minimum and the flat layer represents the Fermi level. The arrows show how the electrons drift through these potential energy barriers.

In this model, quantum mechanical hopping is excluded as a conduction model because of the relatively long average distances between these potential energy barriers. The electron transport in IGZO is dominated by percolation, with electrons drifting between potential energy barriers (the arrows in Fig. 1-2). The bumpy surface represents the potential energy barriers at conduction band minimum and the flat layer represents the Fermi level. The arrows show how the electrons drift through these potential energy barriers. Kamiya et al. [15] showed the temperature dependence of electrical conductivity in a-IGZO films with different carrier densities. With low carrier densities, the electrical conductivity increased with increasing temperature because the Fermi level does not completely fill the valley of potential energy barriers. However, once the Fermi level is elevated above the maximum of these bumpy energy barriers (high carrier density), the valleys are filled and electron transport is temperature independent, behaving as a degenerate

semiconductor. The analysis also provides the activation energy of donor levels, which are estimated to be 0.11 eV below the CBM for a-IGZO.

Kamiya et al. [9] measured hard X-ray photoemission spectroscopy (HX-PES) spectra of a-IGZO film to quantify trap states. It exhibited additional, non-negligible signals in the deep subgap region above the valence band maximum (VBM) with a bandwidth of 1.5 eV, indicating high-density electron traps just above VBM. As-deposited a-IGZO film deposited at room temperature also exhibit extra gap states 0.2 eV below CBM, which is related to hysteresis in capacitance –voltage characteristics and TFT characteristics (further discuss in the next section) [16]. Based on these characteristics, a proposed energy band diagram of a-IGZO is shown in Fig. 1-3. Generally, there are donor levels and a localized state (as-deposited) 0.1 eV and 0.2 eV below CBM, respectively. A 1.5 eV wide high density deep state exists right above the VBM. Although these deep states do not significantly impact n-type TFTs carrier transportation, they are important for achieving p-type AOS TFTs. There have no demonstration of oxide TFTs operating in an inversion p-channel mode including ZnO and a-IGZO TFTs. A possible explanation is that the subgap states pin the Fermi level 1.5 eV above VBM under a reverse gate bias, especially as the density of these subgap states is more than two orders of magnitude larger than the hole carrier density.

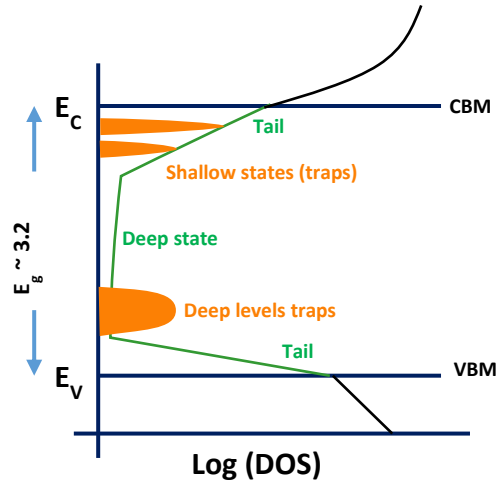


Figure 1-3. Energy band diagram of a-IGZO.

1.6 Defects and doping in IGZO

Conventional semiconductors such as Si or Ge are normally doped by impurities such as B, P or As. In IGZO, doping is thought to occur by defect structures, primarily oxygen vacancies and potentially hydrogen. Kamiya et al. [17] showed the DFT derived electronic structure of stoichiometric a-IGZO without oxygen deficiencies. They used pseudo-band structures although band theory is not strictly applicable to disordered systems without structural periodicity. For stoichiometric a-IGZO, the dispersion of the CB is reasonably large indicating band-like behavior (in contrast to localized states) No subgap states were found in the pseudo-band structure irrespective of the amorphous structure.

On the other hand, Kamiya et al. [17] also showed the electronic structure of non-stoichiometric a-IGZO with oxygen deficiencies. A localized band forms at the VBM, and other

deeper VB bands also have very small dispersions. This indicates that the VB states are mostly localized in a-IGZO. They also speculated that the strongly-localized states are formed because the disordered atomic configuration in a-IGZO breaks the coherent hybridization of O 2p orbitals that mainly form the VB in oxides. Another important feature found in the pseudo-band structure of stoichiometric a-IGZO with oxygen deficiencies is that the dispersion of the conduction band is decreased significantly from that of the stoichiometric a-IGZO, suggesting that the formation of an oxygen deficient state also breaks the coherency of the conduction band and forms a localized state near the CBM. Kamiya et al. speculated that this would be a candidate for electron traps near CBM observed by C-V measurements [16].

The electronic states of the oxygen deficient (or oxygen vacancy) a-IGZO are classified into two groups. The first group forms deep fully occupied oxygen vacancy (V_o) states at 0.4–1 eV above the VBM. In this case, electrons near the valence band are concentrated at the V_o sites. These defects are characterized by a large free volume. On the other hand, the second oxygen deficiency group forms a shallow donor state. In this case, the oxygen deficiency relaxes to smaller free volume, and therefore electrons cannot be trapped at a V_o site, which results in the doping of free electrons to the CB. This difference implies that large free volume corresponds to deep trap states and small free volume corresponds to shallow trap states.

Hydrogen is also thought to be an effective dopant for IGZO. Kamiya et al. [17] calculated more than ten H-doped a-IGZO models from different coordination of the H atoms, and found that the H atoms always form O-H bonds in the relaxed structure (by DFT structure relaxation calculations). For H-doped a-IGZO, the Fermi level is located ~1 eV above the CBM in the pseudo-band structure and the CBM wave function is delocalized over the material. These

indicate that the H doping results in electron doping through the reaction $\frac{1}{2}H_2(g) + O^{2-}$ (in a-IGZO) $\rightarrow -OH^-$ (in a-IGZO) $+ e^-$. A similar effect is reported also for ZnO [18]. Because the doped H atoms form strong O-H bonds, H doping should be strong and stable. It is consistent with the thermal desorption spectra (TDS) results, showing that the chemical bonds in wet O annealed a-IGZO is more stable than as-deposited or dry O annealed a-IGZO [19].

Omura et al. [20] used a similar DFT method to calculate electronic structures of c-IGZO containing oxygen vacancies (V_o), interstitial hydrogen (H_i), and interstitial oxygen (O_i). The calculations for the atomic structure relaxation suggest that H_i bonds to a lattice oxygen (O_o) to form $-OH$ bonds, and O_i occupies a split interstitial site [O_i (split)] forming a chemical bond with O_o which is similar to an O_2 molecule, or O_i occupies an octahedral interstitial site [O_i (oct)]. The electronic structure calculations reveal that V_o forms fully occupied states around the middle of the DFT band gap, while H_i does not form a defect level in the band gap but raises the Fermi level above the CBM. [O_i (split)] forms fully occupied states above the VBM of the defect-free model, while [O_i (oct)] forms both occupied and unoccupied states above the VBM. It is thus suggested that V_o and [O_i (split)] are electrically inactive for electrons but work as hole traps. In contrast, H_i acts as a donor and [O_i (oct)] is electrically active, trapping both electrons and holes.

A modified DFT calculation (SIC-LDA) by Körner et al. [21] showed different results compared to Kamiya et al. (standard LDA) [17] for the IGZO electronic structure. Körner et al. believe SIC-LDA can obtain a more reliable result than standard LDA for oxide systems. According to the SIC-LDA calculation, subgap states can be divided into two main groups. In the lower half of the band gap, the deep localized defect levels are related to undercoordinated O

atoms. The subgap states in the upper part of the band gap (shallow states) are caused by defects related to oxygen vacancies. The latter defect levels originate mostly from pairs of metal atoms which come close without a bridging oxygen. On the other hand, Kamiya's standard LDA calculation shows that the deep localized defect levels are related to oxygen vacancies with larger free volume and shallow states are related to oxygen vacancies with smaller free volume. However, both of these methods (SIC-LDA and standard LDA) agree that H interstitials form OH bonds and act as electron donors.

1.7 Deposition of IGZO

Researchers have been used different techniques to deposit IGZO for TFTs including PLD (pulse laser deposition)[2], RF magnetron sputtering [22][23][24] and solution processing [25][26]. RF magnetron sputtering deposition has been widely used in IGZO deposition due to the quality and efficiency [22]. Most work has focused on optimizing IGZO TFTs by stoichiometry and oxygen partial pressure during deposition [27]. Yabuta et al. [27] fabricated IGZO TFTs with various O_2/Ar partial pressures during IGZO deposition. The O_2 partial pressure was varied from 3.1 to 3.7 % of $O_2/(O_2+Ar)$ volume ratio. They showed that the electrical conductivity increased when the O_2 partial pressure decreased. Similarly, Chiang et al. [22] fabricated IGZO TFTs with various O_2 partial pressures at 0, 0.25 and 0.5 mTorr in a constant 5mTorr O_2/Ar processing pressure during IGZO deposition. The turn-on voltages of the IGZO TFT decreased when the O_2 partial pressure decreased. This is consistent with more oxygen vacancies formed at low oxygen partial pressures and that these oxygen vacancies induced more electron carriers. The oxygen vacancy formation in these oxides is governed by



where O_o^x indicates an oxygen atom occupying an oxygen lattice site; $V_o^{\cdot\cdot}$ is oxygen vacancy and e^- is a free mobile electron. The density of electrons increases as oxygen escapes from the matrix leaving oxygen vacancies.

These oxygen rich and poor conditions during IGZO deposition can be classified into two kinds of sputtering. Reactive and non-reactive sputtering refer to characteristics of the gas ratio in the sputter chamber. In reactive sputtering, IGZO is deposited with an Ar and O_2 plasma which leads generally to stoichiometric films with low oxygen vacancy concentrations and insulator characteristics. On the other hand, IGZO film deposited by pure Ar plasma (non-reactive sputter) are initially conductive because of a high concentration of oxygen vacancies that act as donors. As Ar is significantly heavier than oxygen, non-reactive sputtering has a higher deposition rate.

Nomura et al. [9] summarized Hall mobility and carrier concentration (N_e) for the films in the In_2O_3 - Ga_2O_3 - ZnO system. All the films were deposited on a SiO_2 glass substrate at room temperature and with an oxygen partial pressure of 1.0 Pa. Although pure In_2O_3 and ZnO films exhibited high Hall mobilities of ~ 34 and $\sim 19 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, respectively, they were crystalline even for films deposited at room temperature. Moreover, the carrier concentration of In_2O_3 and ZnO films are relatively high. Both Hall mobility and carrier concentration rapidly decreased with increasing Ga^{3+} ion content. Hall mobilities in the a-IGO films decreased from $\sim 25 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at $N_e \sim 10^{20} \text{ cm}^{-3}$ to $\sim 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at $N_e \sim 10^{18} \text{ cm}^{-3}$ as Ga^{3+} ion content increased from 30 to 50%.

1.8 TFT in IGZO

Two different configurations exist for TFTs as depicted in Fig. 1-4; (a) top gate and (b) bottom gate. This classification is defined by the gate electrode location and the relative position of the source/drain and gate terminals [28]. If the gate is above the channel layer, the device is in a top-gate configuration. In contrast, if the gate is below the channel layer, the device is in a bottom-gate configuration.

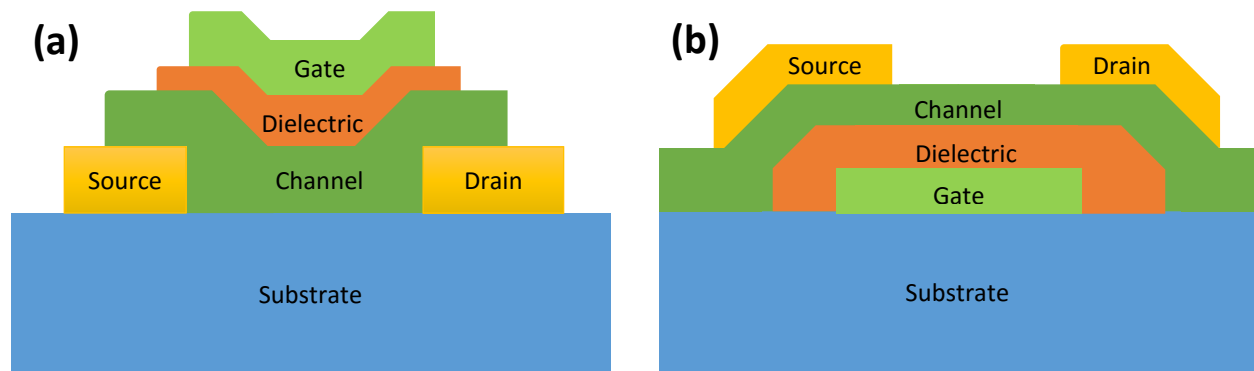


Figure 1-4. TFT configurations: (a) top-gate and (b) bottom-gate.

To obtain a high performance IGZO TFT, choosing suitable materials for gate dielectric materials and contact electrodes is important. Researchers have already tried various gate dielectrics including ZrO_2 [29], Y_2O_3 [30], SiO_2/HfO_2 [31], SiO_2+CeO_2 /polymer[7], organic polymers [32], SiN_x [33], SiO_2 [22], and SiN_x/SiO_2 [34]. Generally, SiN_x/SiO_2 dual gate dielectrics have been widely used in industry because SiO_2 adheres well to the IGZO layer and SiN_x blocks impurities from diffusing into the IGZO film from the glass substrate.

1.9 Annealing behavior

To reduce the density of trap states near the CBM (that affect electron transport and TFT operation), post-deposition annealing is a critical process to improve the TFTs performance and stability [15]. For example, Kimura et al. [16] compared annealed (300°C for 1h in air) and unannealed IGZO TFTs and showed the measured results of the I-V and C-V characteristics. For unannealed samples, the subthreshold slope (S) was 0.26 Vdecade⁻¹ with a field effect mobility (μ_{FE}) of 9.0 cm²V⁻¹s⁻¹. The hysteresis was large for this unannealed TFT. On the other hand, for devices annealed at 300°C, the subthreshold slope dropped to 0.15 V decade⁻¹ and the mobility increased to 12.3 cm²V⁻¹s⁻¹. In addition, the hysteresis disappears for the annealed TFT, indicating that post-deposition annealing dramatically improved transistor performances.

The extracted trap densities of unannealed and annealed TFTs can be extracted from C-V characteristics [16]. The trap densities of the unannealed a-IGZO TFTs are flat in the energy gap, $\sim 2.0 \times 10^{16}$ cm⁻³ eV⁻¹ in the deep energy far from CBM, but become larger near CBM. Moreover, post-deposition annealing reduces the trap density near CBM. The reduction of hysteresis of the annealed TFTs in I-V curves can be explained using the reduction in the trap densities.

The annealing environment is also critical. Nomura et al. [19] studied the influence of water vapor on IGZO TFTs performance. They showed the electrical performances of unannealed and annealed a-IGZO TFTs at 400°C for 1 h in various partial pressures of water vapor (P_{H_2O}). Thermal annealing not only improved the TFT characteristics but also reduced the distributions of the TFT parameters. Wet annealing between 7.3 and 19.7% relative humidity (relative to room temperature) was shown to result in the best TFT characteristics including the smallest sub-

threshold slopes, the largest mobilities, and the narrowest devices distributions. To understand the effect of different annealing ambients, Nomura et al. [19] also showed in-situ measurements of DC conductivity (σ_{DC}) as a function of temperature (T) for a-IGZO devices during thermal annealing in dry O₂, wet O₂, and dry N₂ ambients. Samples were heated from 300 to 700K at a heating rate of 20 K min⁻¹ followed by cooling down to 300K. Initially, the increase in σ_{DC} with increasing T from room temperature is associated with thermal excitation of electrons from donor levels. At higher annealing temperature, σ_{DC} continues increase as oxygen vacancies are formed generating free electrons ($M-OH + M-OH \leftrightarrow V_o^{\cdot\cdot} + M-O-M + H_2O\uparrow + 2e^-$, where M is metal cation and $V_o^{\cdot\cdot}$ is oxygen vacancy). When cooling down from 700 K to room temperature, the oxygen vacancies are destroyed in dry and wet O₂ ambients. However, in N₂ cooling ambient, σ_{DC} did not decrease since the thermal induced oxygen vacancies could be compensated by nitrogen atoms.

1.10 Contact metallurgy

Proper selection of source and drain (S/D) contact materials is also very important for high performance a-IGZO TFTs because ON currents, field effect mobilities, and subthreshold slopes are critically affected by the contact properties of S/D electrodes [35][36]. Ohmic contacts generally require optimizing both the carrier densities in the oxide and the position of the metal Fermi level relative to the semiconductor. Considering the work function of a-IGZO (~4.5eV), Ti (4.3eV) and Mo (4.7eV) metals are reasonable as S/D electrodes because of negligible Schottky barrier heights between S/D electrodes and the a-IGZO layer. For this reason, Ti and Mo have been widely employed in academic and industry research groups as S/D electrodes for a-IGZO TFTs [37][38].

To address the carrier density at the interface, Ahn et al. [35] compared the performances of a-IGZO TFTs with Ar and H₂ plasma treatment on IGZO S/D regions just prior to IZO metallization. Hydrogen acts as an electron donor and decreased the contact resistance improving the electrical performances in terms of mobility and subthreshold slope compared to TFTs treated with Ar plasma.

Titanium is also generally one of the preferred contact metallurgies. To understand the reaction between Ti and a-IGZO, Choi et al [39] compared the contact resistances of IGZO TFTs with Ti and Ag (reference) contacts. The TFTs with Ti contacts had lower contact resistance and higher field effect mobility compared to that of Ag. Cross sectional HRTEM image of a-IGZO TFT with Ti S/D electrode annealed at 300°C for 1 h in air was shown [39]. A thin interfacial TiO_x layer between Ti and a-IGZO was observed. The reduced contact resistance was attributed to the formation of this TiO_x interfacial layer. Ti attracts O atoms from a-IGZO to form TiO_x, leaving oxygen vacancies in the a-IGZO. These oxygen vacancies provide free electrons and increase carrier density, which is consistent with the lower turn-on voltage for Ti contacts.

Kiani et al. [40] used Pilling-Bedworth theory for metal oxide to explain the interaction between contact metals and a-IGZO, and especially to model trap formation at the interface of metal/a-IGZO. The Pilling-Bedworth ratio (R_{P-B}) is the molar volume of the oxide to that of the metal. For metals having a R_{P-B} less than one, the metal-oxide tends to be porous and unprotective because the metal oxide volume is not enough to cover the underlying metal surface. For R_{P-B} larger than one, compressive stresses build up in the oxide and, if the mismatch is too large ($R_{P-B} > 2$), the oxide coating tends to buckle and flake off continually exposing fresh metal, and is thus non-protective. The ideal R_{P-B} is 1, but protective coatings normally form for metals having R_{P-B} between 1 and 2. The charge build-up due to the metal oxidation (depend on R_{P-B})

leads to a complex capacitance diode at the interface of the metal contact/a-IGZO. Metal contact diffusion within the a-IGZO channel layer results in defects which alter the band-gap of the channel material. Therefore, the contact metal/a-IGZO interface has important significance in controlling the behavior of the overall TFT device.

1.11 CAAC (C-axis Aligned Crystalline) IGZO

To date, amorphous IGZO has been the primary focus of investigation into TFT channel materials. However, reliability issues such as degradation under bias temperature stress remain unresolved. And from an industrial point of view, device reliability is one of the most important factors. Yamazaki demonstrated a nanocrystallized IGZO film showing strong crystallographic texture, referred to as c-axis aligned crystal (CAAC) IGZO. This material retains the excellent uniformity of the amorphous phase while improving stability and exhibiting extremely low leakage currents (10^{-24} A/ μm). These characteristics make CAAC IGZO an ideal candidate for applications beyond traditional displays, including low-power displays, non-volatile RAM, and sensors [41]. Figure 1-5 shows the unit cell of single-crystal IGZO. IGZO consists of alternative hexagonal a-b planes of In_2O_3 and (Ga,Zn)O planes. The relative fraction and the composition of the (Ga, Zn)O planes are determined by the overall composition.

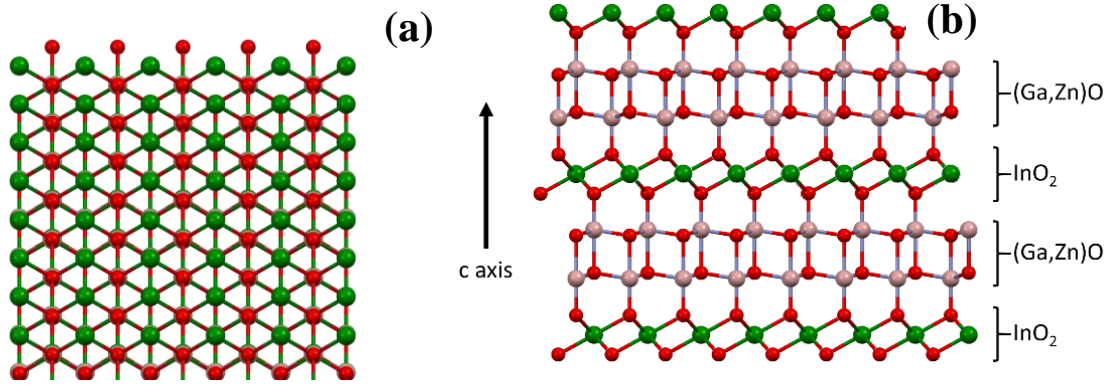


Figure 1-5. (a) Hexagonal a-b plane (green is indium and red is oxygen) and (b) alternating layers of indium oxide and gallium/zinc oxide in the single-crystal IGZO unit cell

Zhu et al. characterized CAAC IGZO based on crystallinity, texture and etch rate [42]. Both X-ray diffraction and general area detector diffraction (GADDS) showed that crystallinity increased rapidly above a deposition substrate temperature of 200°C with simultaneous formation of highly aligned CAAC. Optimal texture with strong c-axis alignment and a minimum GADDS full-width-at-half-maximum of 18° occurred at 250°C.

Figure 1-6 shows the XRD and GADDS spectra of amorphous and CAAC IGZO film deposited at room temperature and 310°C, respectively. XRD of a-IGZO exhibits only weak scattering at 32° while CAAC films show strong diffraction from (009) planes at $30.0 \pm 0.1^\circ$. In GADDS, a-IGZO exhibits only a weak amorphous ring at 32° while the CAAC film exhibits strong diffraction at $2\theta \approx 30^\circ$ over a narrow χ range. That is, the CAAC film shows strong c-axis texturing with a χ scan FWHM of $\approx 20^\circ$.

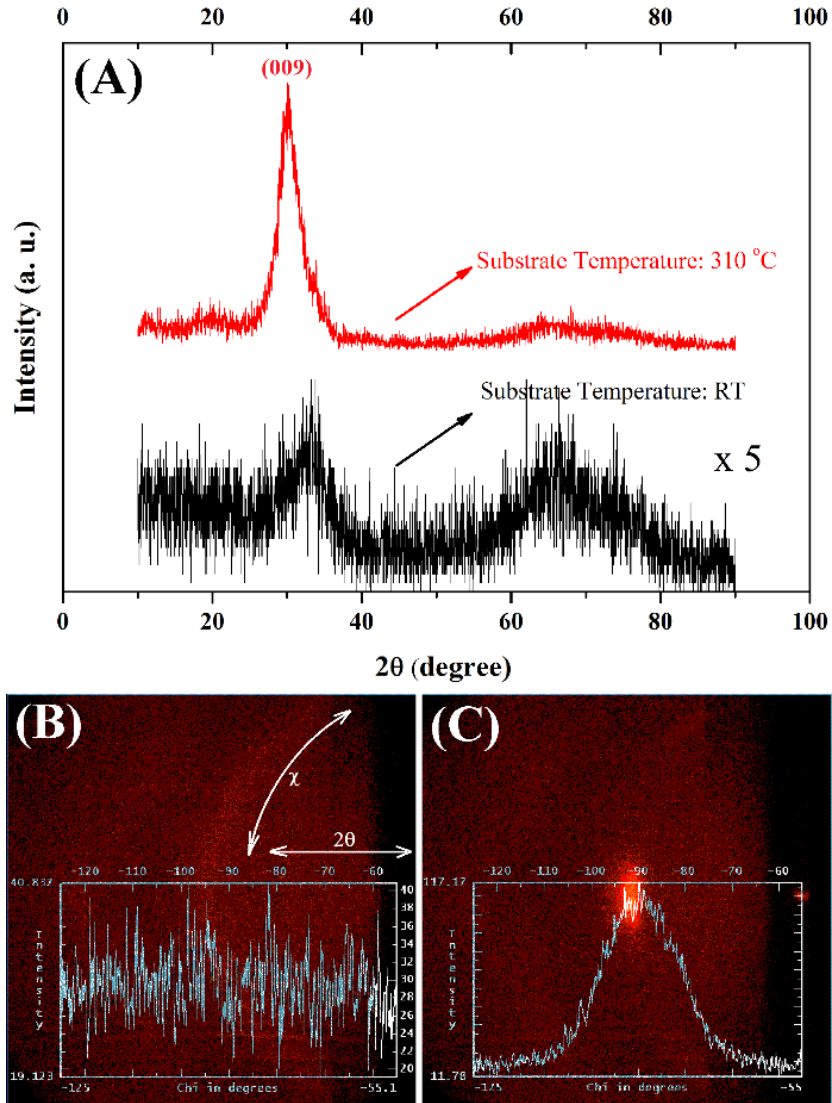


Figure 1-6. XRD of RT and 310 °C deposited IGZO (A), GADDS frames of samples deposited at RT (B) and 310 °C (C). Inset graphs show integrated GADDS intensity as a function of χ . [42]

Figure 1-7 shows the correlation of etch rate and XRD intensity. Chemical etch rate in 5 vol% HCl was highly correlated to crystallinity, dropping by a factor of ten in CAAC compared to amorphous IGZO; etch rate hence provides a highly sensitive measure of crystallinity.

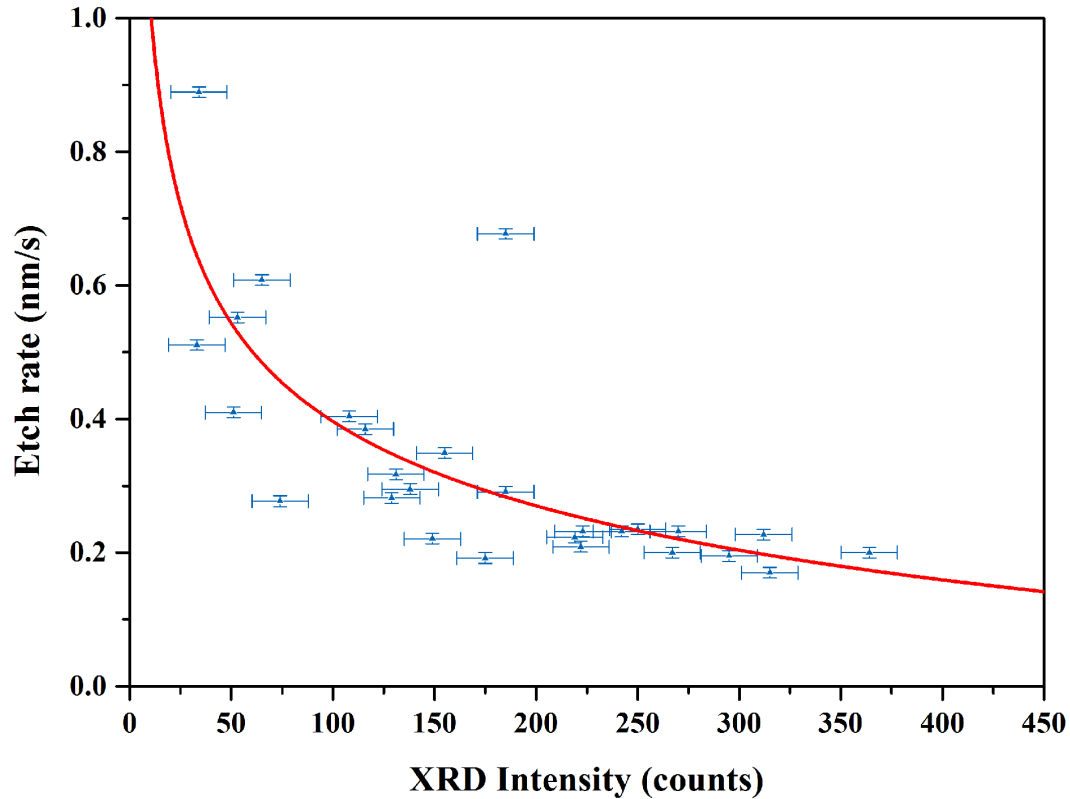


Figure 1-7. Correlation of etch rate with XRD intensity [42]

The formation of CAAC can be quantified in a diagram using the X-ray crystallinity and the GADDS texture measurements as shown in Figure 1-8. In this diagram for IGZO, crystallinity increases from left to right based on the XRD peak intensity, while the GADDS FWHM shows texture alignment improving from the top (amorphous) to the bottom (single crystal). a-IGZO, CAAC and polycrystalline are not thermodynamically well defined structures and hence are represented as areas. The impact of temperature can be readily seen as the curves move from a-IGZO to a maximum CAAC structure and ultimately toward the polycrystalline limit.

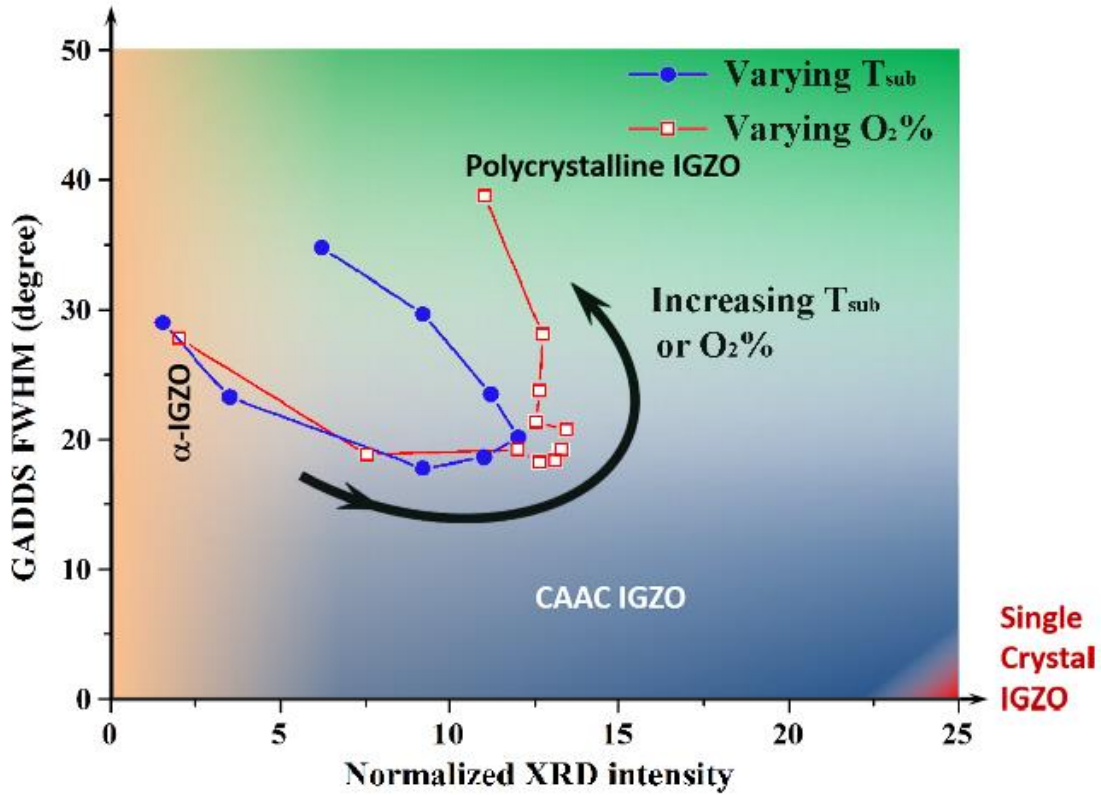


Figure 1-8. Diagram of CAAC IGZO formation using the X-ray crystallinity and the GADDS texture measurements. The two curves represent properties obtained from reference deposition conditions with either temperature or gas composition systematically varied about optimized conditions

Lynch et al. showed HRTEM images of cross-section and plain-view of the highly aligned CAAC IGZO in Figure 1-9[43]. Highly aligned film exhibited a high degree of crystallinity over the entire cross-section (Fig. 1-9(a)) image field of view with $\pm 9^\circ$ variation in lattice plane alignment (0.3nm spacing). The film is characterized in plan-view (Fig. 1-9 (b)) by islands of hexagonal symmetry that are well-aligned over the entire field of view with an average interplanar spacing of 0.3nm. The image FFT suggests a highly crystalline film with hexagonal

symmetry aligned to within $\pm 15^\circ$ over this field of view. The cross-section (c) and plan-view (d) images of the weakly-aligned film highlight the increasingly random orientation of the grains. The possible mechanism for growth of textured IGZO (similar to ZnO) by sputtering involves the nucleation of crystallites on an initially disordered (~ 5 nm) layer; subsequent ordered growth occurs if the substrate temperature is high enough to induce coalescence [42].

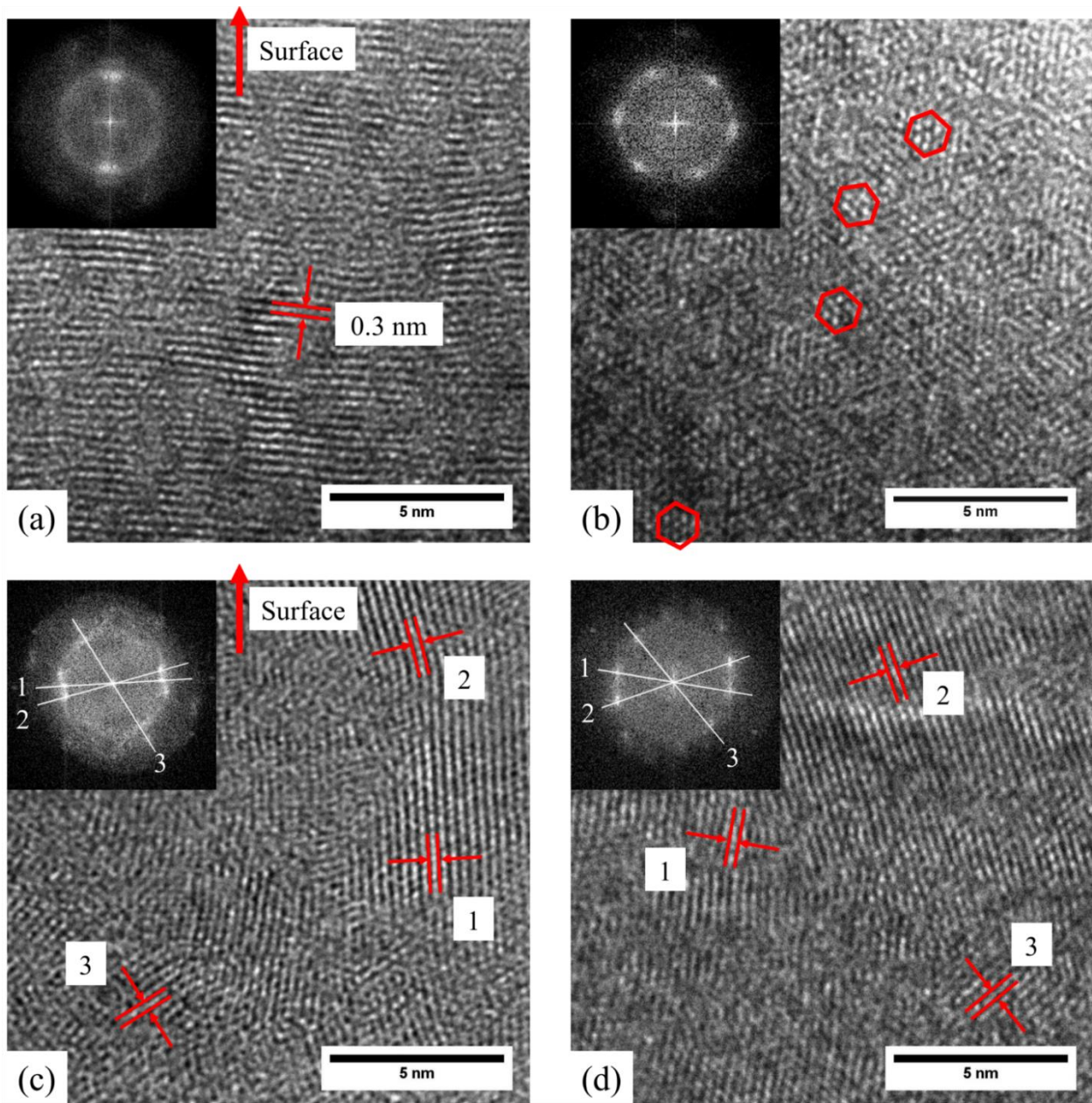


Figure 1-9. (a) Cross-section and (b) plan-view HRTEM images of a highly aligned CAAC IGZO. The cross-section (c) and plan-view (d) images of a weakly-aligned film highlight the increasingly random orientation of the grains. The numbered FFT diffractogram spots correspond to planes labeled within the images. Reproduced with permission from [42]. Copyright 2015, AIP Publishing LLC.

CHAPTER II

II. EXPERIMENTAL METHODS

2-1 Thin Film Deposition Techniques- PVD and CVD

There are two main methods to deposit thin films on substrates, Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD). In PVD, the target material is excited by a high energy source such as laser beam or electron beam, vaporizing the material and transporting it to the substrate where it condenses. CVD, on the other hand, uses sources supplied in the forms of gases or liquid precursors and deposition occurs following a chemical reaction near or at the substrate. The thin film properties in both cases are highly dependent on uniformity and deposition rate. In many PVD processes, atoms travel in a straight path in high vacuum with few collisions. In contrast, CVD processes are normally carried out at moderate pressure with many collisions of reactive species in the gas phase. Thus, in PVD the thin film uniformity is dependent on the supply rate and the geometry of the substrate surface, whereas in a CVD process the thin film uniformity is dependent on the gas or liquid flow patterns and on the source molecule diffusion through the surrounding gases. For PVD process carried out in ultra-high vacuum, there is an additional advantage that access to the deposition surface allows use of analytical techniques involving electron beams [44]. Many PVD processes can be used to deposit both elemental and alloys films, as well as many compounds via reactive deposition processes. In these reactive deposition processes, an ambient gas environment such as oxygen or nitrogen is employed to form oxides and nitrides [45]. PVD processes are generally divided into three major categories, sputtering, evaporation and ablation. We discuss primarily sputtering as

this was used to deposit IGZO. Low Pressure CVD (LPCVD), which is also used in this research, is also introduced.

2-2 Sputter Deposition

IGZO is most commonly deposited by sputtering from either ceramic targets or by reactive sputtering from multiple metal targets. Film deposition during sputtering can be described in terms of several sub-steps as shown in Figure 2-1.

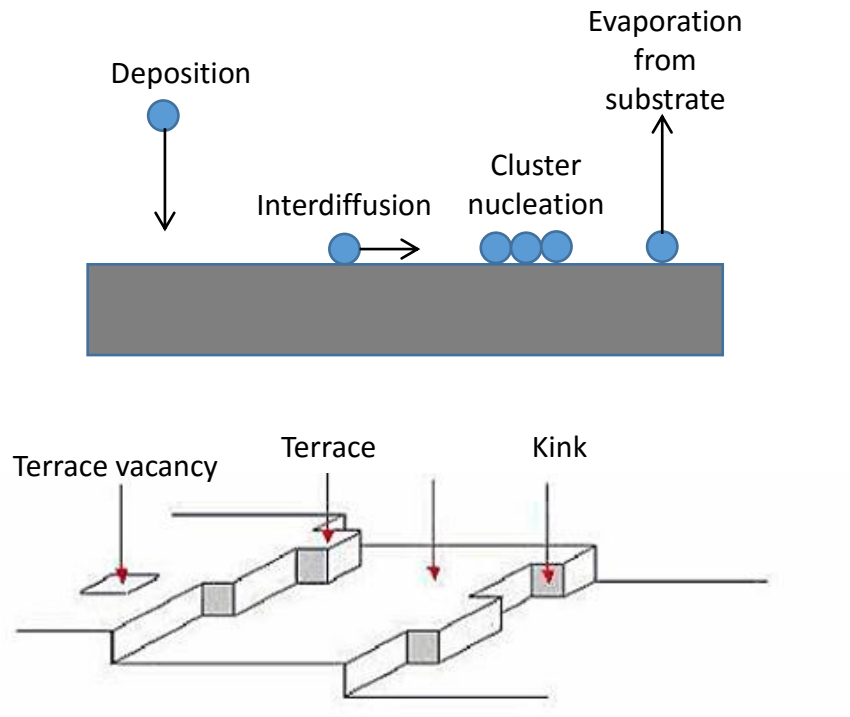


Figure 2-1. Atom/Molecule interaction with substrate during thin film deposition

During sputtering, atoms and molecules arrive at the surface with moderate energy and are absorbed onto the substrate. To reach lower energy states, bonds must be broken between the absorbed molecules and the surface so that the molecules can move to new locations and form

new bonds. In this surface diffusion step, the atoms or molecules interact with each other to form larger clusters. Below a critical cluster size (nucleation), these clusters are thermodynamically unstable and may desorb depending on the deposition parameters. After reaching a certain size, the clusters become thermodynamically stable and an equilibrium density of clusters exist on the substrate. The critical nuclei grow in number and in size until the saturation nucleation density is reached. The nucleation density and the size depends on parameters including the rate of impingement, the activation energy for adsorption, desorption, energy of the impingement, thermal diffusion, temperature, topography, and chemical properties of the substrate. A nucleus can grow both parallel to the substrate by surface diffusion of the adsorbed species, and perpendicular to substrate surface by direct impingement of the incident species. Generally, the rate of parallel growth on the substrate is much higher than that of perpendicular growth. In the coalescence step, small island nuclei coalesce with each other to reduce the islands' surface energy. This tendency to form larger islands, agglomeration, can be enhanced by increasing the surface mobility of the adsorbed species, such as by increasing the substrate temperature. Larger islands grow together, leaving holes and channels of uncovered substrate. These holes and channels are filled until a completely continuous film forms.

In the growing film, there are kink and terrace sites shown in Figure 2-1. Adsorbed species tend to be more stable on kink sites compare to terrace or other island sites because of the additional bonding. Under these conditions, the growth is termed step growth [46].

When a solid surface is bombarded with energetic particles such as accelerated ions, surface atoms of the solid are scattered backward due to collisions between the surface atoms and the energetic particles. This phenomenon is termed sputtering. Several sputtering systems can be employed for thin film deposition including DC diode, RF diode, magnetron, and ion beam

sputtering. A DC sputtering system is composed of a pair of planar electrodes, (cathode and anode) as shown in Figure 2-2.

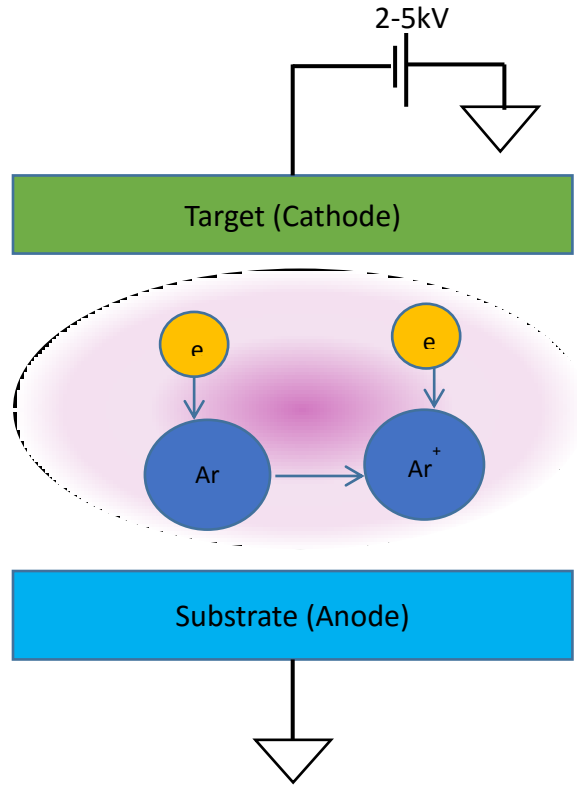


Figure 2-2. DC Diode Sputtering Deposition

The surface of the cathode is covered with the desired deposition material, while the substrates are placed on the anode. The sputtering chamber is filled with sputtering gas, usually Ar since it is relatively heavy and unreactive. An applied electric field accelerates the initially small number of free electrons in the chamber, which then inelastically collide with neutral Ar atoms. The inelastic collision excites the Ar atom to a positive ion. These Ar ions are then accelerated by the electric field and bombard the cathode target surface with momentum transfer, contributing to backward dislodgement of target material molecules and electrons. The sputtered electrons, called secondary electrons, strike other neutral Ar atoms in chamber to form additional

positive Ar ions to sustain the process. The sputtered target atoms both drift and are accelerated to the anode where they result in the deposition of a thin film on the substrate and chamber wall. The common pink glow discharge of the plasma results from the excitation of Ar. Near the cathode, electrons move faster than Ar ions due to their smaller mass. Thus positive charges build up near cathode, raising the potential of the plasma and fewer electrons collide with neutral Ar. Thus, as shown in Figure 2-3, there are fewer excited Ar ions near the cathode leading to dark space sheath, called Crookes dark space.

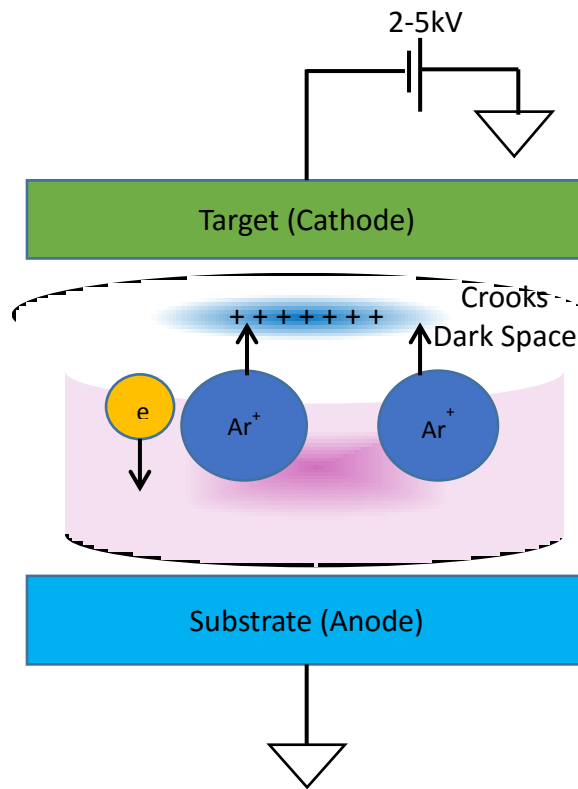


Figure 2-3. Crookes Dark Space in Sputter Deposition

If the target is not conductive (i.e. an insulator or semiconductor), positive charge would also accumulate on cathode target surface during Ar ion bombardment. This would reduce the potential difference between the plasma and the cathode. In order to sustain the glow discharge with insulator targets, high frequency (RF) voltage is applied to the target instead of DC. The insulator target is thus alternately ion and electron bombarded. Positive charges which accumulate on target surface during the negative cycle are neutralized by electrons during the positive cycle. Thus in RF plasma, there are two dark space sheath, which are ion accelerating zones, one near the target and the other one near the substrate as shown in Figure 2-4.

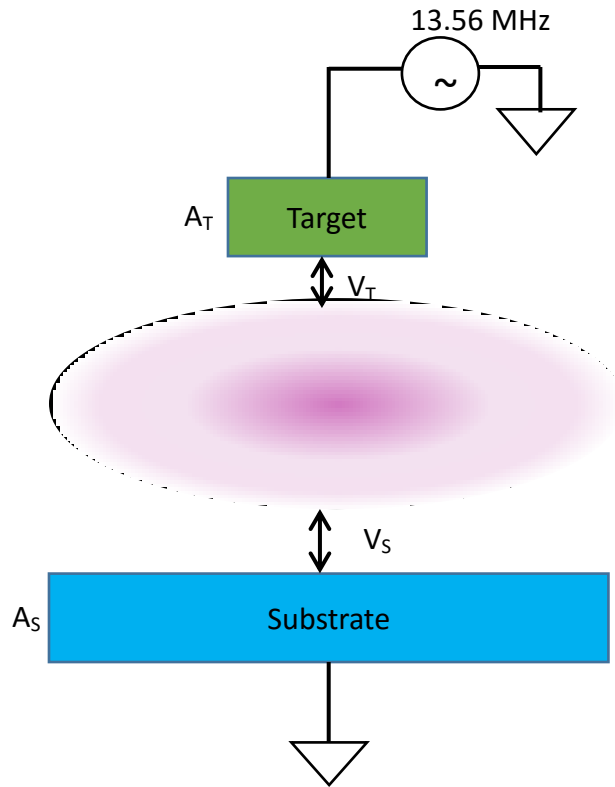


Figure 2-4. RF sputter system

During an RF discharge, Ar ions not only bombard the target but also the substrate. The relationship between the substrate, the target potential, and area in an RF sputter system is given by,

$$V_T/V_S = (A_S/A_T)^n \quad (1)$$

where V_T is the voltage across the target sheath, V_S is the voltage across the substrate sheath, n usually is 4, A_S is the area of the substrate electrode and A_T is the area of the target electrode. Thus, in order to reduce bombardment of the substrate film, the target area is normally reduced in an RF sputter system. Moreover, the RF frequency has to be high enough that the polarity can alternate before Ar ions pass through the dark space sheath to bombard the anode substrate. The typical frequency of 13.56 MHz is sufficient for electrons to strike neutral Ar to induce the plasma without requiring secondary electrons in the beginning [47].

To increase the sputter deposition rate, magnetron sputtering can be used. In magnetron sputter, a parallel magnetic field is applied to the glow discharge as shown in Fig. 2-5.

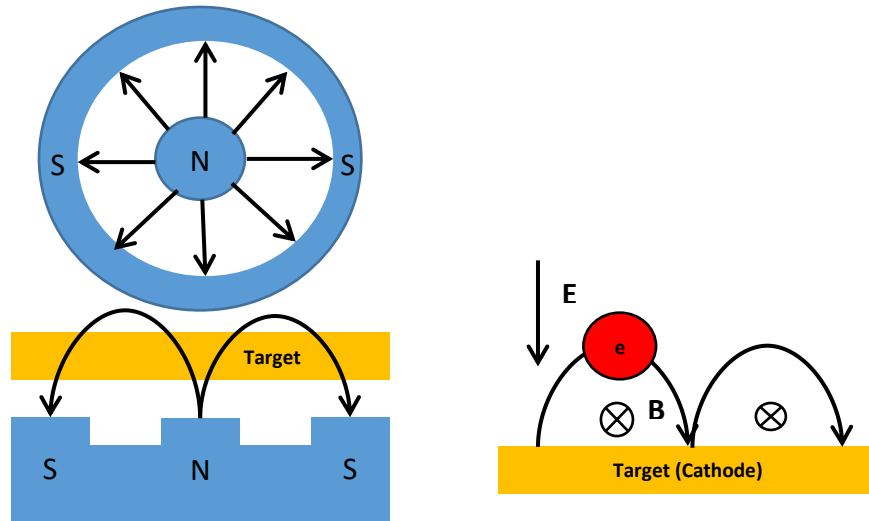


Figure 2-5. Magnetron sputter

Electrons in the glow discharge undergo cycloid motion, and the drifting orbit is in the direction of the $E \times M$, where E and M denote the electric field in the discharge and the magnetic field. The magnetic field is oriented such that these drift paths for electrons form a closed loop and confine electrons to remain near the target to sustain the plasma. This causes an increased opportunity of collision between the electrons and the sputtering gas molecules. The magnetic field causes the plasma density to increase, leading to increased current density at the cathode and contributes to an increased sputtering rate [48].

2-3 Annealing Furnace

After IGZO deposition and patterning, samples were annealed in a UHV compatible furnace with a dedicated gas delivery system, as shown schematically in Fig. 2-6. Samples were annealed after patterning to avoid any potential degradation during lithography or etch processes.

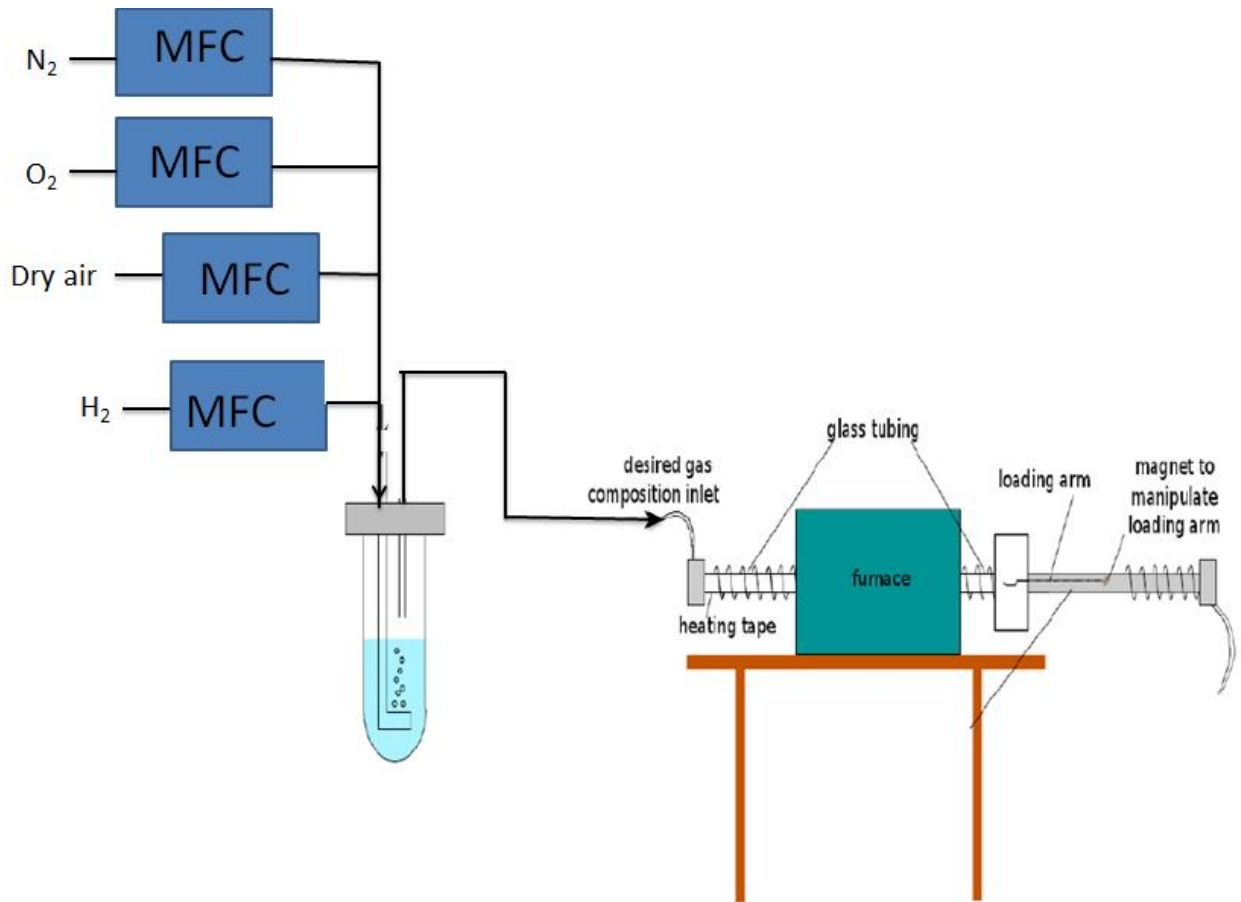


Figure 2-6. UHV compatible annealing furnace with gas ambient control. The hot zone is quartz to prevent sample contamination. Annealing ambient is controlled by varying the relative flow rate.

In contrast to most other studies that use just uncontrolled air for post-sputter annealing, the atmosphere was carefully controlled during these anneals. Although the furnace is UHV compatible, all anneals were carried out at atmospheric pressure. Flow meters controlled independent lines of nitrogen, oxygen, dry air (-62°C dew point), and water vapor saturated gas allowing arbitrary mixing ratios. Saturated water vapor gases were produced by bubbling nitrogen, oxygen or dry air through a frit immersed in de-ionized (DI) water held at a controlled temperature. A thermal bath for the DI water permitted the dew point of the saturated gas to be varies between 0°C to 30°C . The relation of $P_{\text{H}_2\text{O}}$ in the furnace system with the water bath temperature is shown in Figure 2-7. The amount of water vapor in furnace system was controlled by varying the temperature setting of the thermal bath.

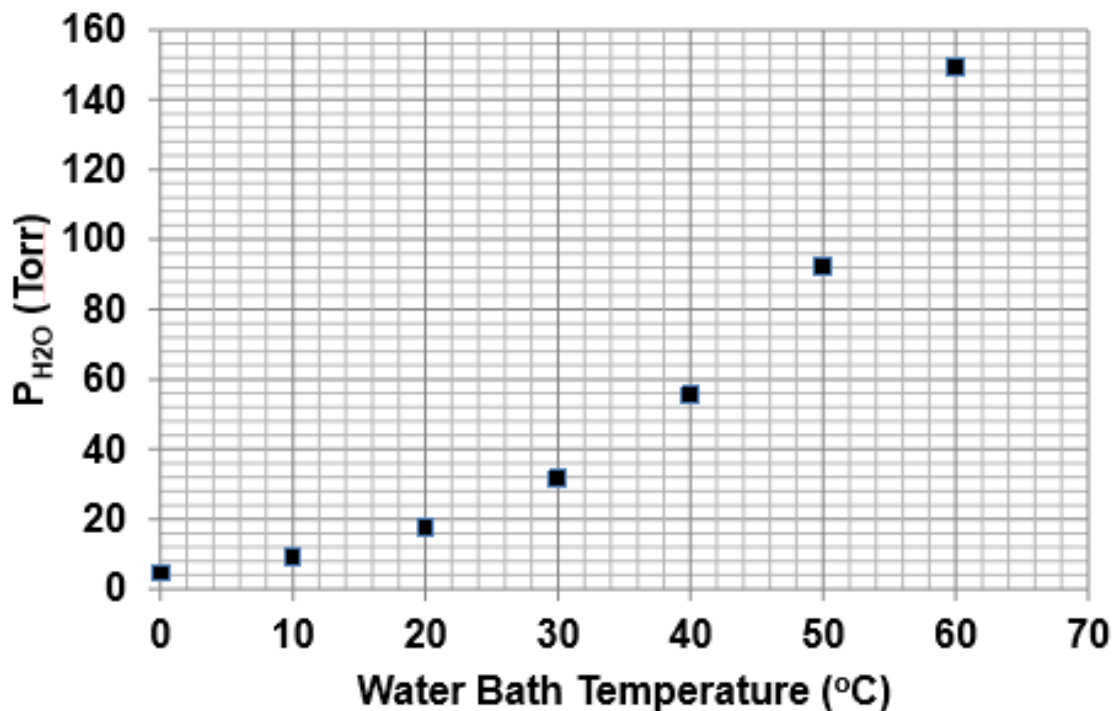


Figure 2-7. The relation of saturated water vapor pressure and water bath temperatures.

For anneals, samples were loaded into a load-lock at room temperature and the furnace was sealed. Gases flowed for a minimum of 10 min before the sample was moved into the furnace zone with a flow rate of typically 1100 sccm into a furnace volume of 2550 cm³. The gas exchange time is thus < 2.5 min. Prior to transferring samples to the hot zone of the furnace, the furnace was flushed with the process gas for 10 minutes. During anneals, the ambient gas was normally maintained as the sample cooled.

2-4 TFT device fabrication

The primary method for evaluation of IGZO films was the thin film TFT device. IGZO-based thin film transistors (TFTs) were fabricated using a staggered bottom-gate test structure as shown in Fig. 2-8 (a). p-doped 4-inch Si substrates (0.01-0.02 Ω-cm) were thermally dry oxidized (1100°C for 30 min with 3% HCl) to grow a 100 nm SiO₂ gate dielectric. The gate via was patterned using 6:1 BOE as shown in Fig. 2-8 (b). IGZO channel layers (Fig. 2-8 (c)) were deposited (generally with the substrate at 260°C) via RF magnetron sputtering in a load locked dedicated sputter chamber with a base pressure of 10⁻⁷ Torr under varying conditions. IGZO was deposited from a 2-inch target sintered InGaZnO_x (In₂O₃:Ga₂O₃:ZnO = 1:1:1) target sputtered at a typical pressure of 5 mTorr Ar and at a typical power of 120 W. Following deposition, devices were patterned lithographically and etched in 2 wt.% HCl. The source and drain electrodes were thermally evaporated and patterned using lift-off photolithography (Fig. 2-8 (d)). These contacts were a stack of Ti (10 nm adhesion) and Au (100 nm to reduce contact resistance to probe tips).

The channel width (W) and length (L) were generally 200 and 50 μm , respectively. No passivation was added to the structure.

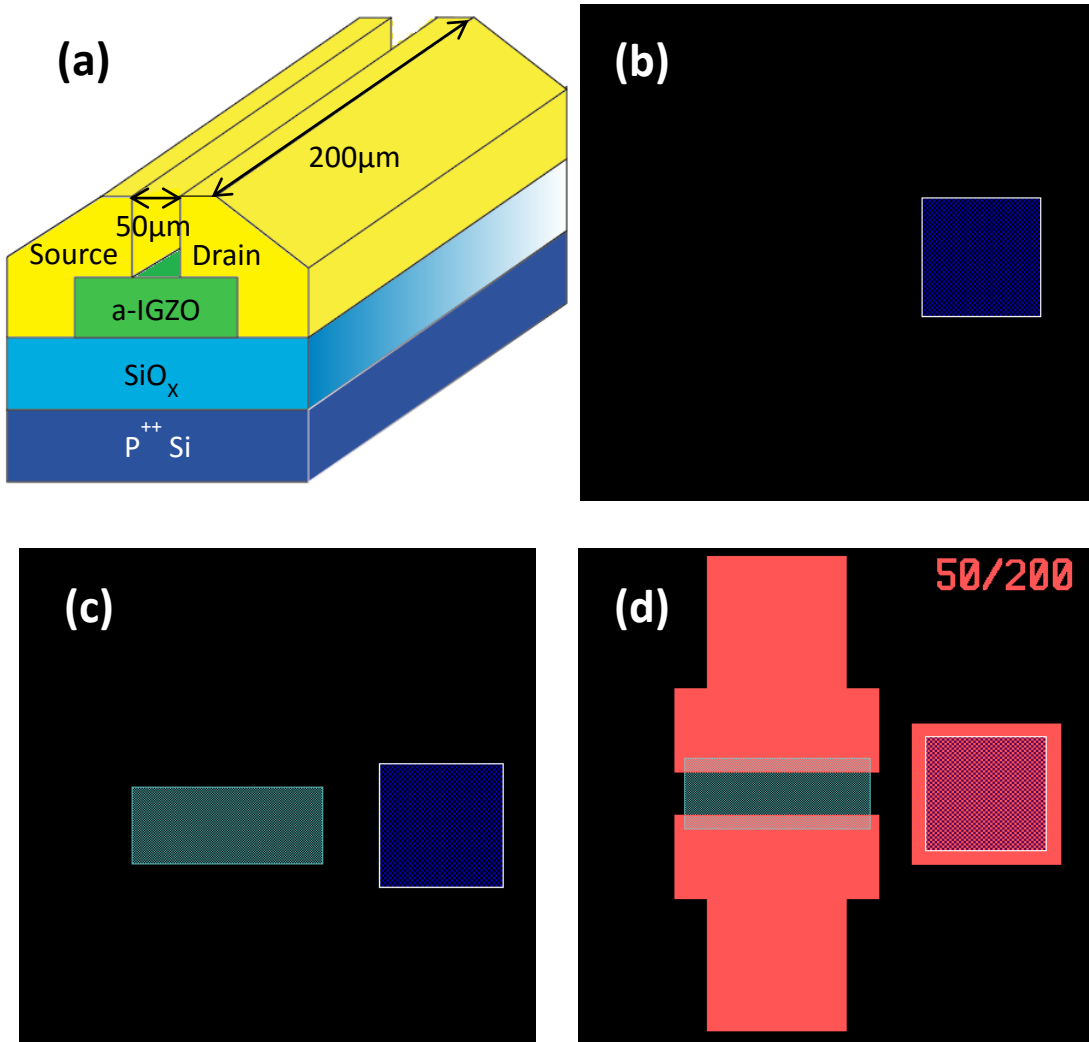


Figure 2-8. IGZO bottom gate TFT test structure and masks pattern.

2-5 Laser spike annealing (LSA)

Laser spike annealing systems, donated to Cornell by Intel, were equipped with a 120 W far-infrared CO₂ laser ($\lambda = 10.6 \mu\text{m}$), necessary optics for millisecond anneals, and a linear motion

stage (Aerotech ES14663-1) capable of traveling up to 400 mm/s. In addition, a 250 W fiber-coupled near-infrared diode laser ($\lambda = 980 \text{ nm}$) was incorporated to the CO₂ laser. The complement laser setup is shown in Fig. 2-9, where the red line represents the beam path for the CO₂ laser while the green line represents the optical fiber coupling the 980 nm beam. For all of the following experiments, laser scans were performed in and out of the page plane.

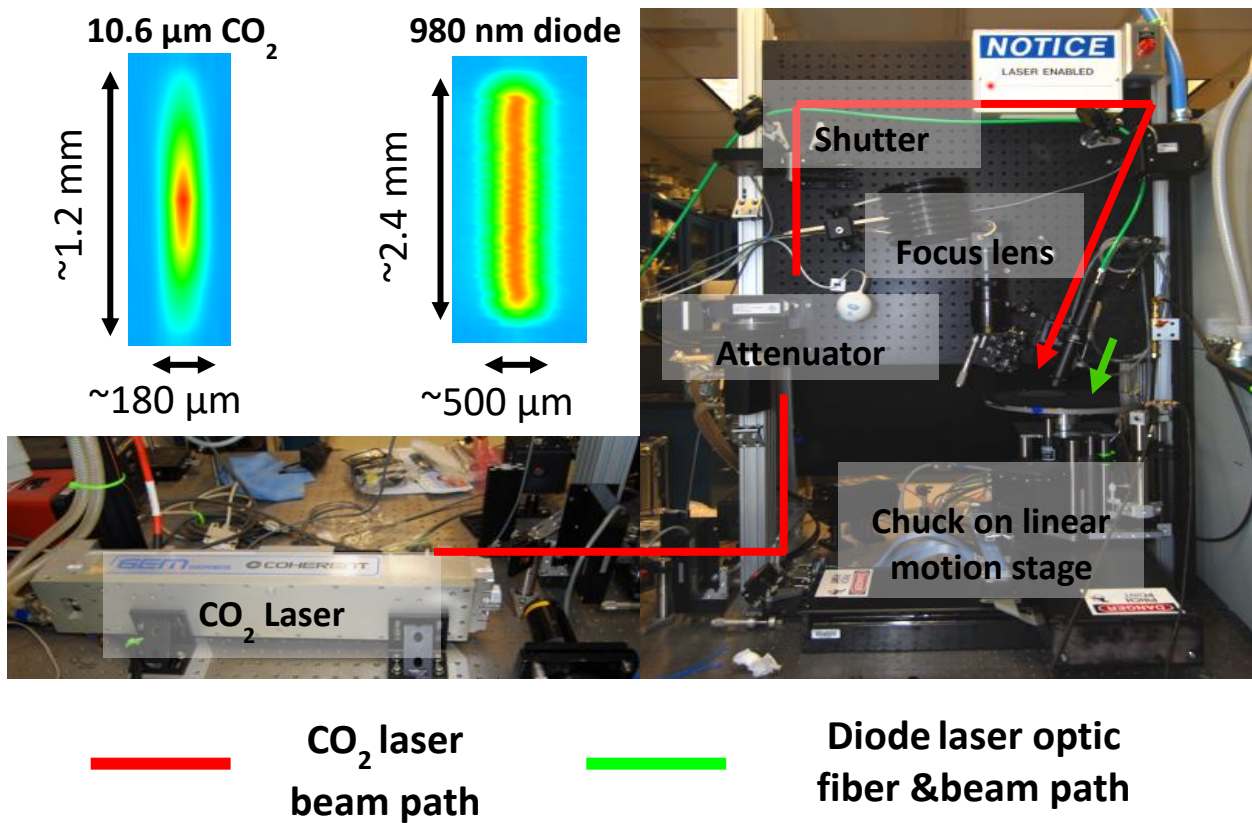


Figure 2-9. Laser spike annealing system. Inset: Beam intensity profile of CO₂ and diode laser.

Laser spike annealing (LSA) provides an opportunity to anneal films on sub-millisecond to millisecond time frames using a scanned continuous wavelength (CW) laser source [49]. In this work, we explored the use of a CO₂ ($\lambda = 10.6 \mu\text{m}$) based LSA with millisecond dwell times to anneal a-IGZO TFTs deposited by radio frequency (RF) sputtering. In LSA (Fig. 2-10), a line-

focused continuous wave CO₂ laser beam ($\lambda=10.6 \mu\text{m}$) is scanned over the substrate, rapidly heating the surface to a peak temperature which subsequently cools by thermal conduction into the substrate as the beam passes. A peak temperature in the range of 300 to 500°C was achieved by scanning a $\sim 90 \mu\text{m}$ by $700 \mu\text{m}$ beam at 100 mm/s resulting in a dwell time of 1ms. The dwell is defined as the FWHM of the laser in the scanning direction divided by the scan velocity. Peak temperatures reported are based on the measured temperature of blank Si wafers [49]. As the IGZO film were only 50 nm thick, the temperature of the films is expected to be very nearly equal to that of the substrate surface. In addition to rapid heating, LSA samples also cool rapidly at $\sim 350,000 \text{ K/s}$, in contrast to furnace samples that cool at $<2 \text{ K/s}$. These high quench rates enable the retention of metastable structures.

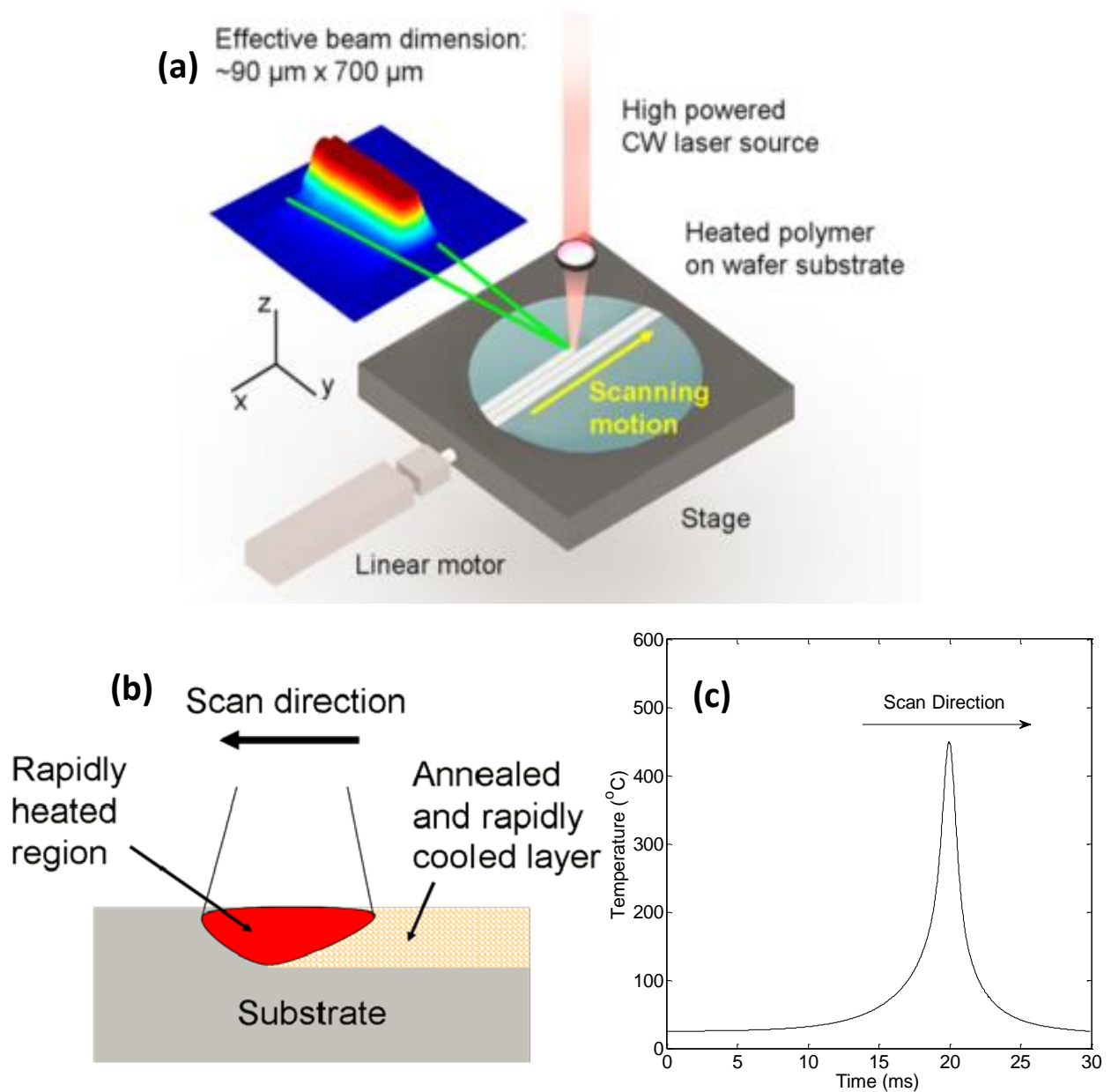


Figure 2-10. (a) Line-focused continuous wave CO_2 laser beam scanning over the substrate surface, rapidly heating the surface to a peak temperature which subsequently cools by thermal conduction into the substrate as the beam passes. (b) The top $\sim 100 \mu\text{m}$ of the substrate surface is rapidly heated and cooled. (c) Simulation of the film surface temperature as a function of time for a 1 ms dwell scan of a CO_2 ($\lambda=10.6 \mu\text{m}$) laser at a peak power of 400 W/cm.

2-6 Single Scan Laser spike annealing (LSA)

R. Bell et. al. developed a fast and accurate technique to characterize thermal annealing on millisecond timeframes using a laser-induced gradient profile as shown in Fig. 2-11. The single scan laser spike anneal (ss-LSA) technique, based on LSA as originally developed to activate dopants in silicon [50][51], has been used recently to study photolithography [52] and directed self-assembly [53]. A line-focused laser (typical aspect ratio 10:1 to 100:1) is scanned to locally heat a sample (Fig. 2-11(a)), with temperature profiles determined by the laser intensity profile (Fig. 2-11(b)), sample absorption, thermal conductivity, and scan velocity. The temporal temperature evolution at the surface for a 150 μs dwell ss-LSA scan with a peak temperature of 900°C is shown in Fig. 2-11(c). The peak temperature is governed both by laser power and dwell time. Temperature profiles across the width of a laser scan generate temperature gradients on the order of 1°C/ μm which are invariant along the scan length.

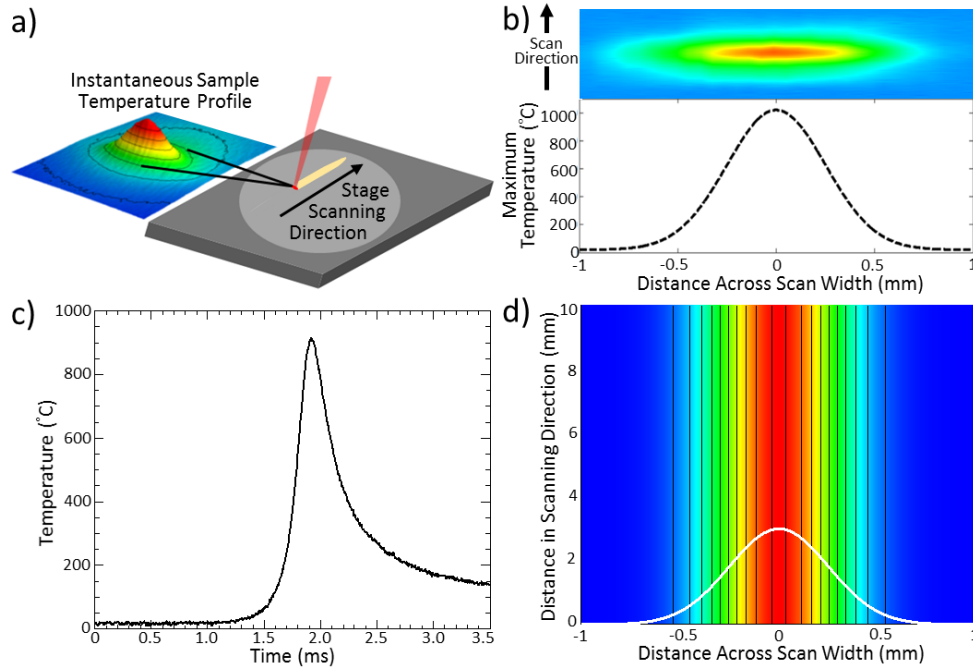


Figure 2-11. (a) *ss-LSA* schematic of a sample scanning through a line focused beam with a depiction of instantaneous temperature profile. (b) Intensity profile of a bi-Gaussian focused beam (top), and idealized *ss-LSA* lateral temperature profile with 1000°C peak temperature (bottom). (c) Temporal temperature profile for a 150 μs anneal with a peak temperature of 900°C. (d) Contour map of peak annealing temperatures across and along a *ss-LSA* scan. The lateral temperature profile is overlaid in white.

Area based LSA (area-LSA) and *ss-LSA* differ primarily in the intended temperature profile across the width of each individual scan. To achieve nearly uniform annealing conditions, area-LSA uses a flat-top intensity profile with scans overlapped to minimize temperature variations normal to the scanning direction. In contrast, for *ss-LSA*, scans are not overlapped and a well-defined annealing temperature gradient is created. This lateral temperature profile is almost

invariant along the length of the scan generating isoanneals in the scanning direction (Fig. 4-1(d)).

The temperature dependence of measured properties is determined by transforming from the position of spatially localized measurements to the corresponding annealing temperature. Accurate characterization of the lateral temperature profile, localization of spatial measurements, and absolute spatial referencing are keys to this transformation.

2-7 TFT Electrical Evaluation

Mobility determines the speed of electrons in the channel and V_{on} indicates the power required for operation. On/off ratio (I_{on}/I_{off}) indicates signal contrast against noise from current leakage and is the ratio of the saturation current to the noise floor. These mobility and V_{on} were extracted from the saturation current regime of the devices using the Equation 2:

$$I_{DS}^{1/2} = \sqrt{\frac{\mu WC}{2L}} (V_{GS} - V_{on}) \quad (2)$$

where μ is the electron mobility; I_{DS} is the drain-source output saturation current; V_{GS} is the applied gate voltage; W is the channel width length; L is channel length; and C is the gate dielectric capacitance per unit area [54]. Sub-threshold slope (S) also provides information of TFT device quality, related to the trap density in the interface of semiconductor and insulator.

TFT devices were tested using a Probe Station (Agilent B1500). Both output curves and transfer curves were normally collected.

Figure 2-12 (a) is an example of a typical output result. The source/drain voltage was swept from 0 to 20 V with gate/drain voltages of 0, 4, 8, 12, 16 and 20 V. Saturation currents were taken at V_{DS} at 30V. Figure 2-12 (b) shows a plot of $(I_{DS})^{0.5}$ versus V_{GS} . The mobility is extracted from the slope ($(\mu WC/2L)^{0.5}$) with the on voltage (V_{on}) given by the intercept.

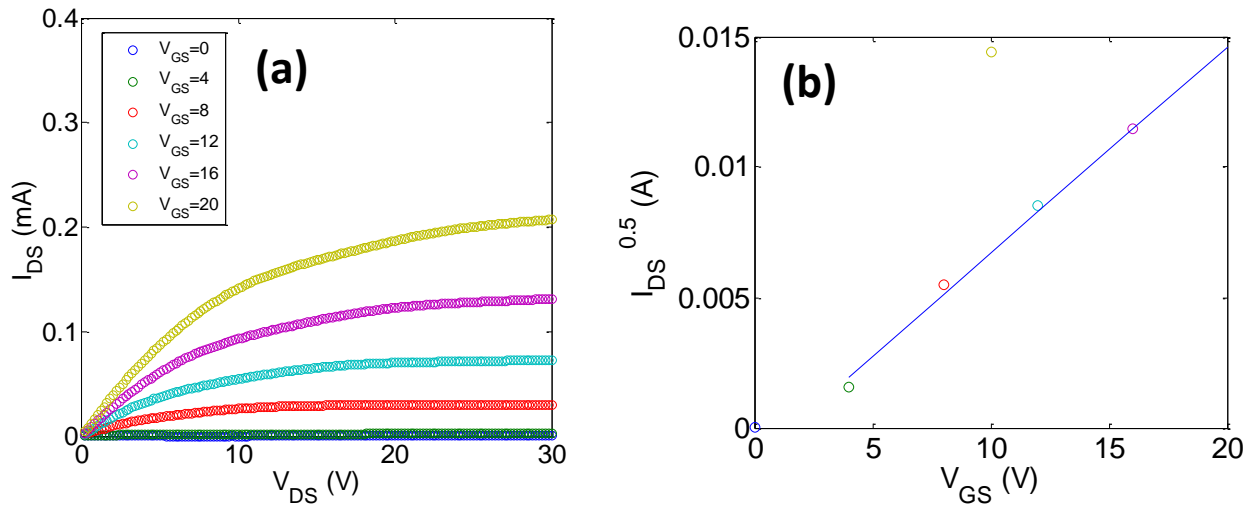


Figure 2-12. (a) I_{DS} - V_{DS} curve and (b) fitting line of saturation current versus V_{GS} .

In addition to output curves, the transfer curve characteristics were measured as shown in Figure 2-13. The On/off ratio (I_{on}/I_{off}) is defined as the ratio of current at $V_{GS} = 20V$ to the minimum current observed. This value is typically reported on a log10 scale, 10^7 for figure 2-13. The sub-threshold slope is defined as $S.S. = dV_{GS}/d(\log_{10} I_{DS})$. As S.S. is dependent on V_{GS} ,

usually the smallest value of S.S. is reported. Typically three devices fabricated under the same conditions were measured to obtain statistically significant results.

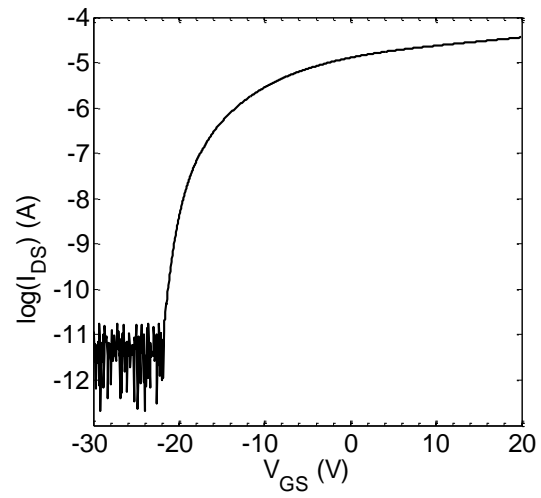


Figure 2-13. I_{DS} - V_{GS} curve at $V_{DS} = 10V$.

CHAPTER III

III. HIGH MOBILITY, DUAL LAYER, CAAC/AMORPHOUS IGZO TFTs

3-1 Introduction and summary:

Today's active matrix displays are based primarily on amorphous hydrogenated silicon (a-Si:H) TFTs, but their relative low mobility ($\sim 1 \text{ cm}^2/\text{Vs}$) and stability under electric stress and/or illumination increasingly limits their application in advanced displays. TFTs implemented using amorphous InGaZnO_4 (a-IGZO), a material with one order of magnitude higher mobility, are therefore beginning to replace a-Si:H in high resolution displays. [1, 2]

Research on IGZO, discovered as a TFT material in 2004 by Hosono[2], has improved the performance of TFTs by optimizing channel length and thickness[57], coping with edge effects[58], selecting optimal source/drain (S/D) ohmic[59] or Schottky contacts[60], using high-k dielectric oxide materials such as ZrO_2 [29], HfO_2 [31] and Al_2O_3 [61], dual-gate structure[62], [63], dual gate dielectrics [64], dual-active layer of ZIO/IGZO[65] and dual active layer of IGZO_x with high/low processing oxygen ratios[66].

Recently, Yamazaki et al. reported improvement in the reliability and stability of IGZO TFTs by fabricating TFTs using IGZO deposited as a nanocrystalline, c-axis aligned crystalline (CAAC) thin film[16,17]. Compared to a-IGZO TFTs, CAAC TFTs were found to have an extraordinary low off-state leakage current, approaching $\text{yA}/\mu\text{m}$ ($10^{-24} \text{ A}/\mu\text{m}$), with potential applications in solid state memories.

In this chapter, we extend the single CAAC based TFT by developing a dual layer IGZO TFT. The TFT channel is implemented in a 20 nm CAAC layer with a 30 nm deposited a-IGZO on top. We demonstrate a dual layer IGZO TFT consisting of a 310°C deposited CAAC (c-axis aligned crystal) 20 nm thick channel layer capped by a second, 30 nm thick, 260°C deposited amorphous IGZO layer. The TFT exhibits a saturation field-effect mobility of $\sim 20 \text{ cm}^2/\text{Vs}$; exceeding the mobility of 50 nm thick single layer reference TFTs fabricated with either material.

The deposition temperature of the second layer influences the mobility of the underlying transport layer. When the cap layer is deposited at room temperature (RT), the mobility in the 310°C deposited CAAC layer is initially low ($6.7 \text{ cm}^2/\text{Vs}$), but rises continuously with time over 58 days to $20.5 \text{ cm}^2/\text{Vs}$, i.e. to the same value as when the second layer is deposited at 260°C. This observation indicates that the two layers equilibrate at RT with a time constant on the order of $5 \times 10^6 \text{ s}$. An analysis based on diffusive transport indicates that the room temperature diffusivity must be of order of $1 \times 10^{-18} \text{ cm}^2/\text{s}$ with an activation enthalpy $E_A < 0.2 \text{ eV}$ for the mobility limiting species.

The findings are consistent with a hypothesis that the amorphous layer deposited on top of the CAAC has a higher solubility for impurities and/or structural defects than the underlying nanocrystalline transport layer, and that equilibration of the mobility limiting species is rate limited by hydrogen diffusion, whose known diffusivity fits these estimates.

3-2 Experimental methods:

Substrates for these studies were p⁺-type Si wafers with a 100 nm thermal oxide as the gate dielectric. A 50 nm thick dual IGZO layer was then deposited by RF sputtering (In₂O₃:Ga₂O₃:ZnO = 1:1:1), at 120 W of RF power and in an Ar: O₂ ratio of 9:1 and a pressure of 5 mTorr. The deposition temperature of the first 20 nm thick layer was varied between 300°C and 350°C, the range in which previous work showed optimal CAAC formation [18,19]. After deposition of the CAAC layer, the substrate temperature was lowered, in situ, to 260°C to deposit the second, 30 nm thick, a-IGZO capping layer; varying temperatures were explored for this capping layer from 260°C to room temperature. After fabrication, TFTs were furnace annealed for 30 minutes at 350°C in dry air. The completed TFT structure is shown schematically in Fig. 3-1.

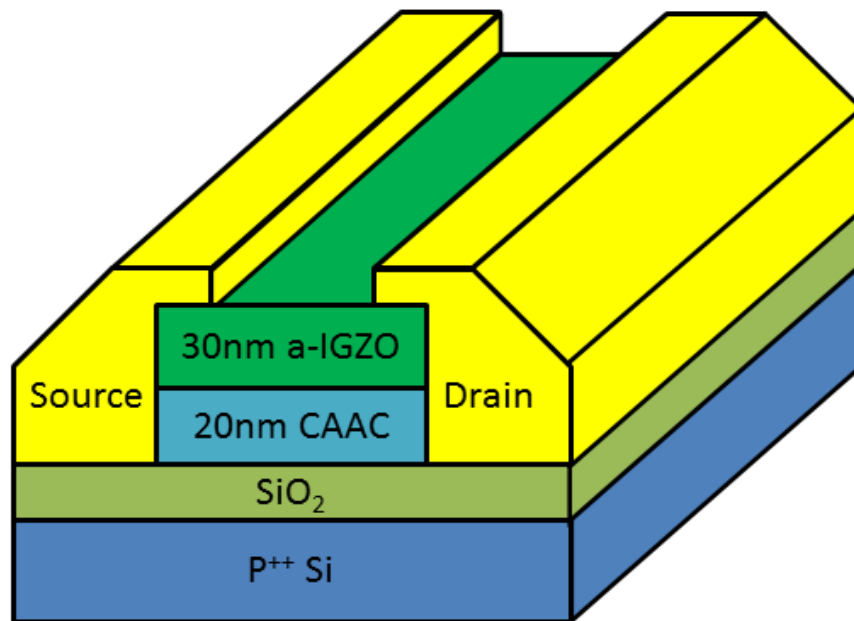


Figure 3-1. Cross section of the CAAC/amorphous IGZO TFT

3-3 XRD analysis of dual layer films:

Figure 3-2 show X-ray diffraction (XRD) from these layers as measured with a Rigaku Smartlab X-Ray diffractometer with a Cu K_{α} source.

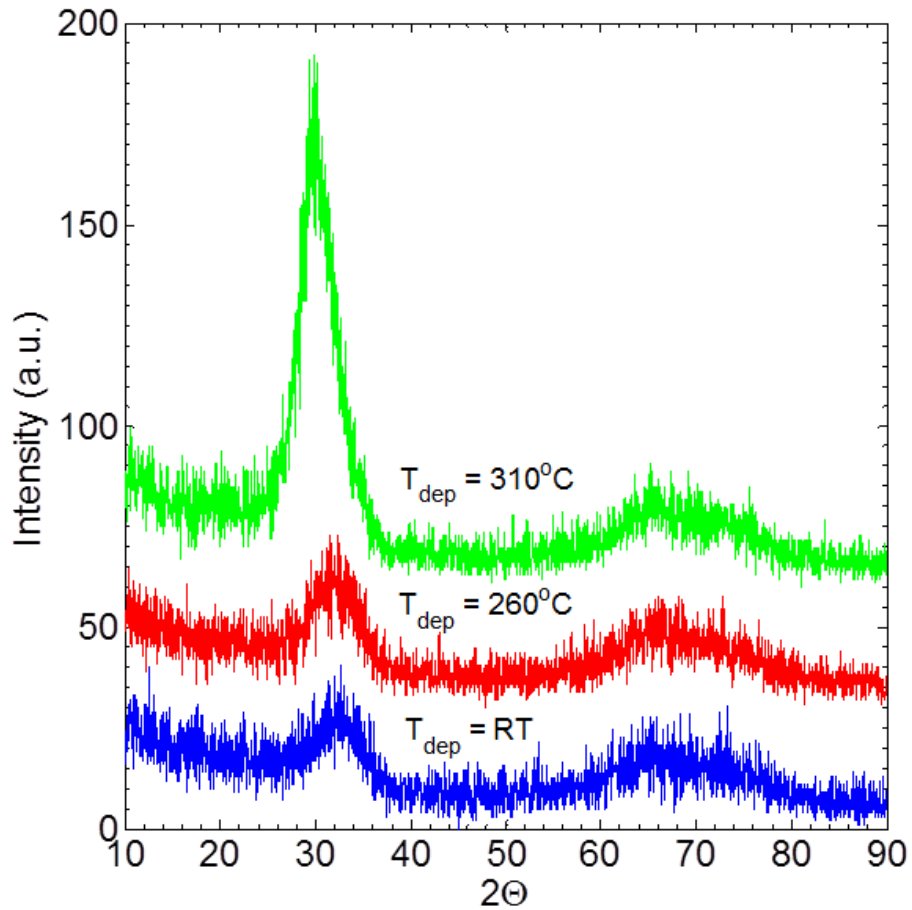


Figure 3-2. XRD of IGZO deposited at room temperature, 260°C and 310°C.

Samples deposited at room temperature and 260°C exhibit weak scattering at 31°, characteristic of amorphous IGZO, while the 310°C films show strong diffraction from (009) planes at

30.0±0.1° [67] indicating a c-axis oriented crystalline structure. These X-ray profiles remained stable during subsequent processing.

3-4 Electrical performance of IGZO TFTs deposited at substrate temperature at 310°C (CAAC), 310°C (CAAC), 260°C (amorphous), and 260°C (amorphous):

To distinguish processing conditions, we use double subscripts ($T_{310/260}$) to indicate dual layer films and to specify the deposition temperatures of the first and second layer. Single layer reference TFTs were also deposited, which we designate using a single subscript (T_{260}).

Electrical measurements were made at room temperature in the dark, using a Karl Süss PSM6 probe station. Transfer characteristics were measured at $V_{DS} = 10$ V. Saturation field-effect mobility and turn-on voltage were determined by fitting the square root of the saturation current ($I_{DS,sat}$), as a function of the gate voltage (V_{GS}) using:

$$I_{DS,sat} = \mu \times C_{ox} \times \frac{W}{L} \times \frac{(V_{GS} - V_{on})^2}{2}, [69]$$

where μ is the saturation field-effect mobility, $W/L = 200/50$ (L was set at 50 μm to minimize the contact effect [70]), and $C_{ox} = 32.3$ nF/cm² is the gate capacitance.

Figure 3-3 shows representative output curves of devices fabricated with 50nm IGZO deposited at (a) T_{310} , (b) $T_{310/260}$ (dual layer), and (c) T_{260} °C. The saturation current of devices constructed in single layer devices with either amorphous (T_{260}) or CAAC (T_{310}) are similar This agrees with

our[68] and literature findings[70] that the mobility of a-IGZO and CAAC is similar, consistent with conduction dominated by the spherical s states of In. However, the saturation current approximately doubles when a-IGZO is stacked on top of the CAAC ($T_{310/260}$). We deposited 20 nm and 50 nm pure CAAC films and fabricated TFTs using the standard process for comparison as shown in Fig. 3-4. As expected, the thin CAAC device shows degraded performance relative to the 50 nm device. The V_{on} shifted positively by 10 V and the mobility is approximately half (11.4 to 6.1 cm^2/Vs). With the thin CAAC, environmental contamination at the back channel interface has a much stronger effect on device performance. The total thickness of all the other devices measured in this work was kept at 50 nm to minimize this potential error.

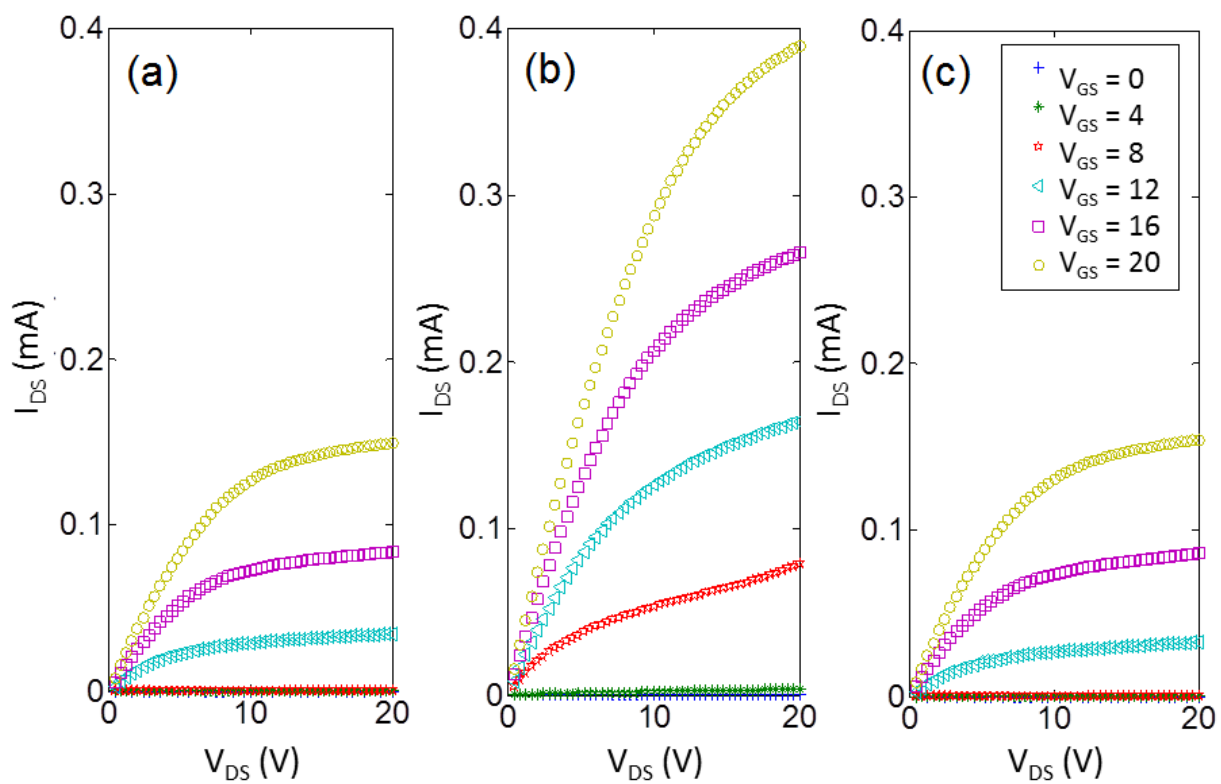


Figure 3-3. Output curves of IGZO TFTs deposited at substrate temperature at (a) 310°C (CAAC), (b) 310°C (CAAC) / 260°C (amorphous), and (c) 260°C (amorphous).

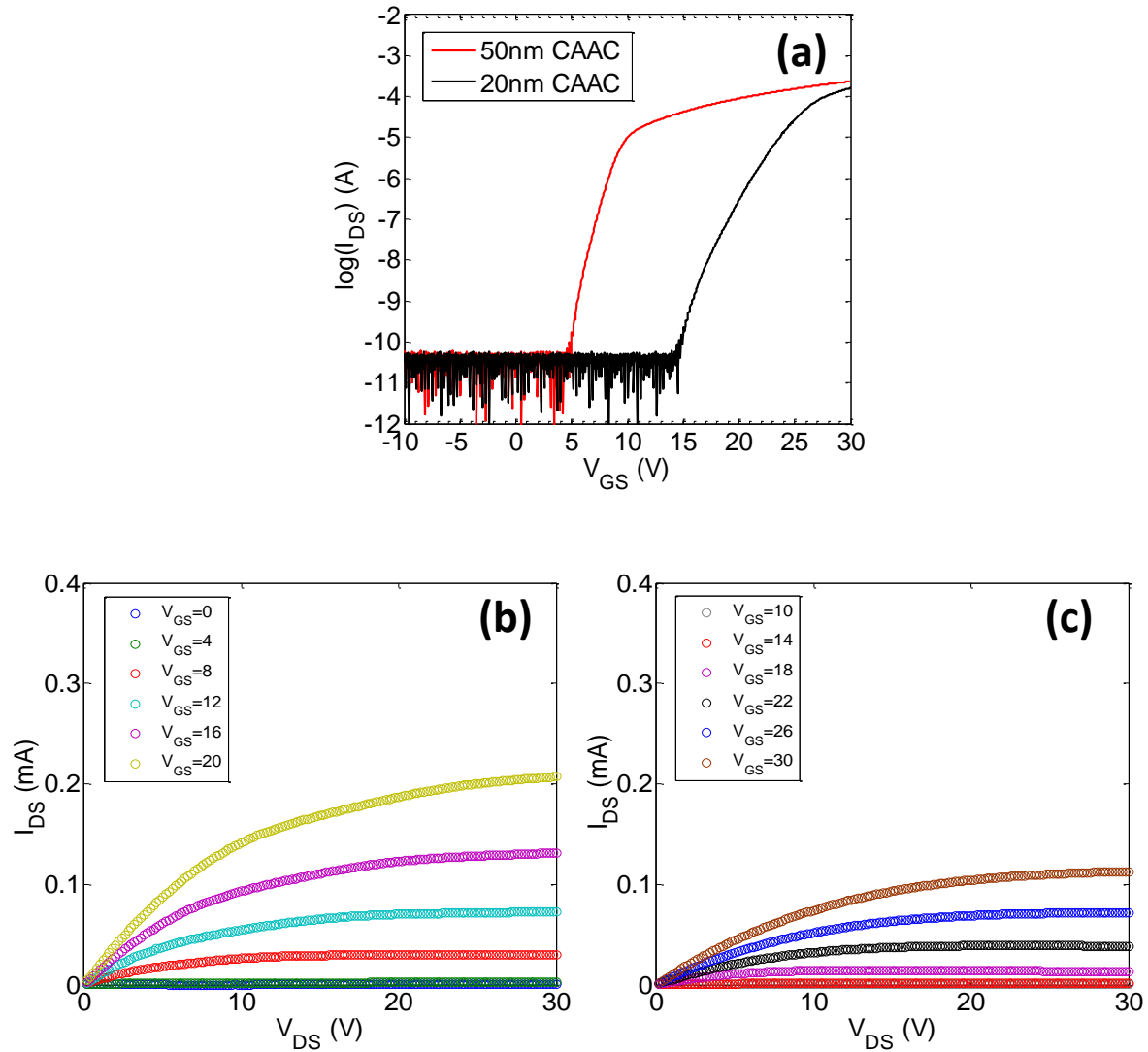


Figure 3-4. (a) Transfer curves of CAAC IGZO TFTs with 20 and 50nm thick channel layers and Output curve of CAAC IGZO TFTs of (b) 50nm and (c) 20nm thick channel layers deposited at substrate temperature of 310°C.

Figure 3-5 shows the electrical characteristics of these devices. Transfer characteristics are shown in Fig. 3-5(a) with summaries of the saturation mobility and turn-on voltage for the three conditions shown in Fig. 3-5(b) and (c) respectively. The measured saturation mobilities of the

single layer T_{310} (CAAC) and T_{260} (a-IGZO) TFT were 12.8 and 15.3 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively, whereas the mobility in the dual layer $T_{310/260}$ device was 20.6 $\text{cm}^2/\text{V}\cdot\text{s}$. The turn-on voltages of single-layer T_{310} and T_{260} are 7.5 and 7.6 V, respectively but lower, at 3.2 V, in the dual layer device. The mobility of pure CAAC IGZO TFT we obtained is slightly higher than others [71][72][70].

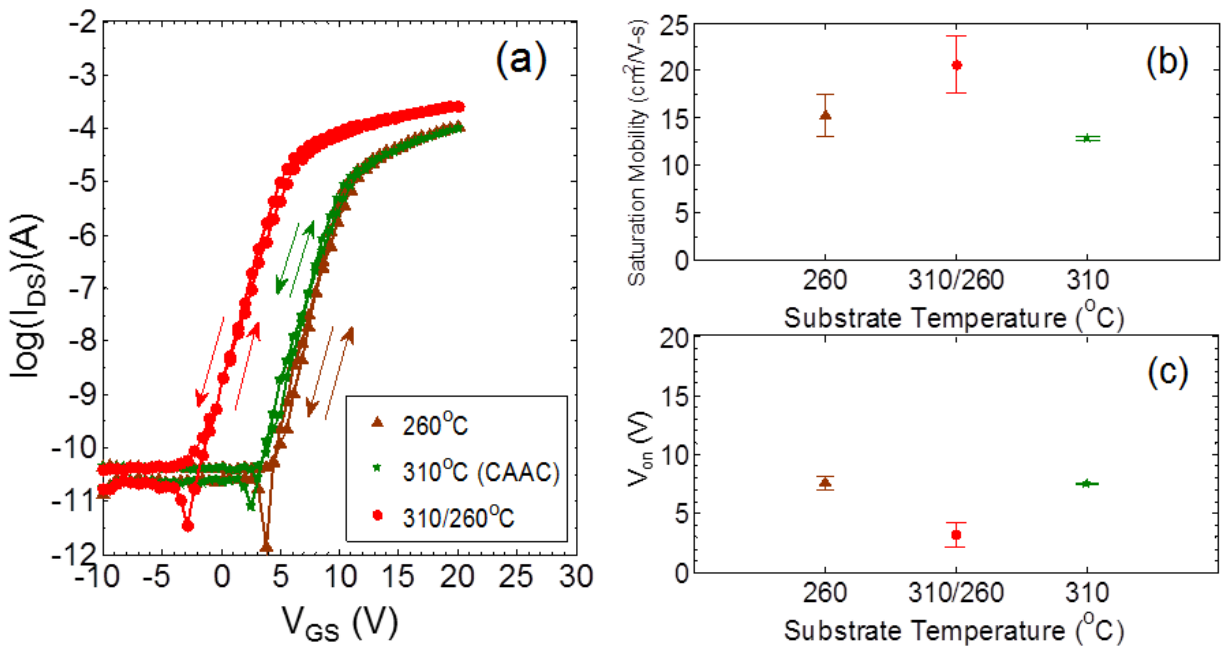


Figure 3-5. (a) Transfer curves, ($V_{DS} = 10\text{V}$), (b) saturation mobility, and (c) turn-on voltage of IGZO TFTs deposited at substrate temperatures of 310°C (CAAC), 310°C (CAAC)/ 260°C (amorphous) dial, and 260°C (amorphous).

3-5 Electrical performance of IGZO TFTs deposited at substrate temperature at 310°C (CAAC), 310°C (CAAC), 310°C (CAAC) | room temperature (amorphous), and room temperature (amorphous):

To study the influence of the deposition temperature of the amorphous layer, we fabricated devices in which the first layer was, as before, deposited at 310°C, but with the second layer deposited at room temperature. Figure 3-6 shows output curves corresponding to (a) TFT made in a single layer deposited at T_{310} , (b) in the dual layer $T_{310/RT}$, and (c) in a single layer T_{RT} . The output current is highest in the single layer CAAC device, but lower in RT and dual layer device, which now behave very similarly.

Figure 3-7 shows the corresponding transfer curves (a), saturation mobility (b) and turn-on voltage (c). The extracted saturation mobility of TFTs fabricated using single-layer (T_{310} and T_{RT}) IGZO was 12.8 and 6.4 $\text{cm}^2/\text{V}\cdot\text{s}$ respectively, but the mobility of the dual layer was 6.7 cm^2/Vs . Deposition of the second layer at room temperature reduced the mobility in the channel layer below that measured in a single layer deposited at the same temperature. Turn-on voltages for T_{310} and T_{RT} films were 7.5 and 13.5 V, respectively. As in the case of $T_{310/260}$ devices, the turn-on voltage of the dual layer TFT remained lower than either single layer device at 3.5 V.

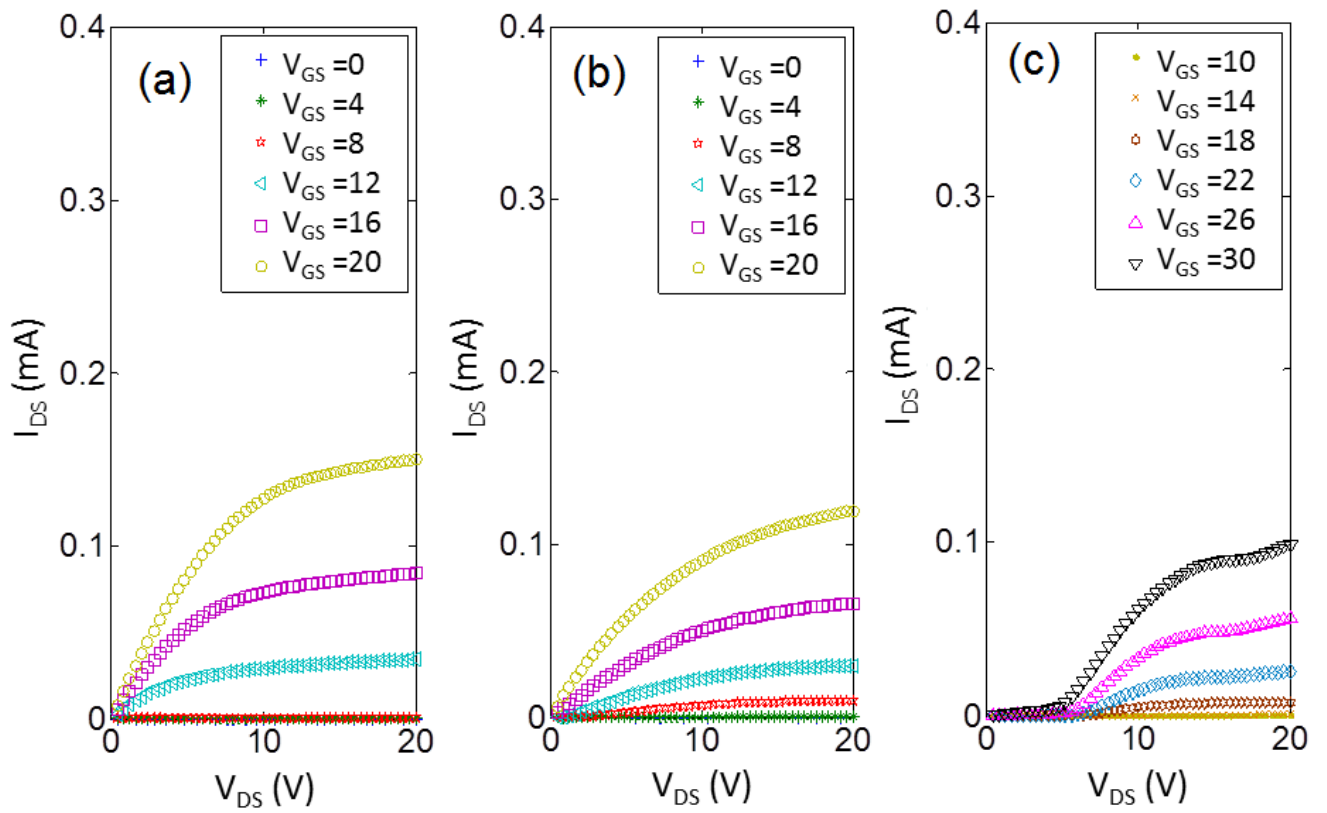


Figure 3-6. Output curves of IGZO TFTs deposited at substrate temperatures of (a) 310°C (CAAC), (b) 310°C (CAAC)/RT (amorphous) and (c) RT (amorphous).

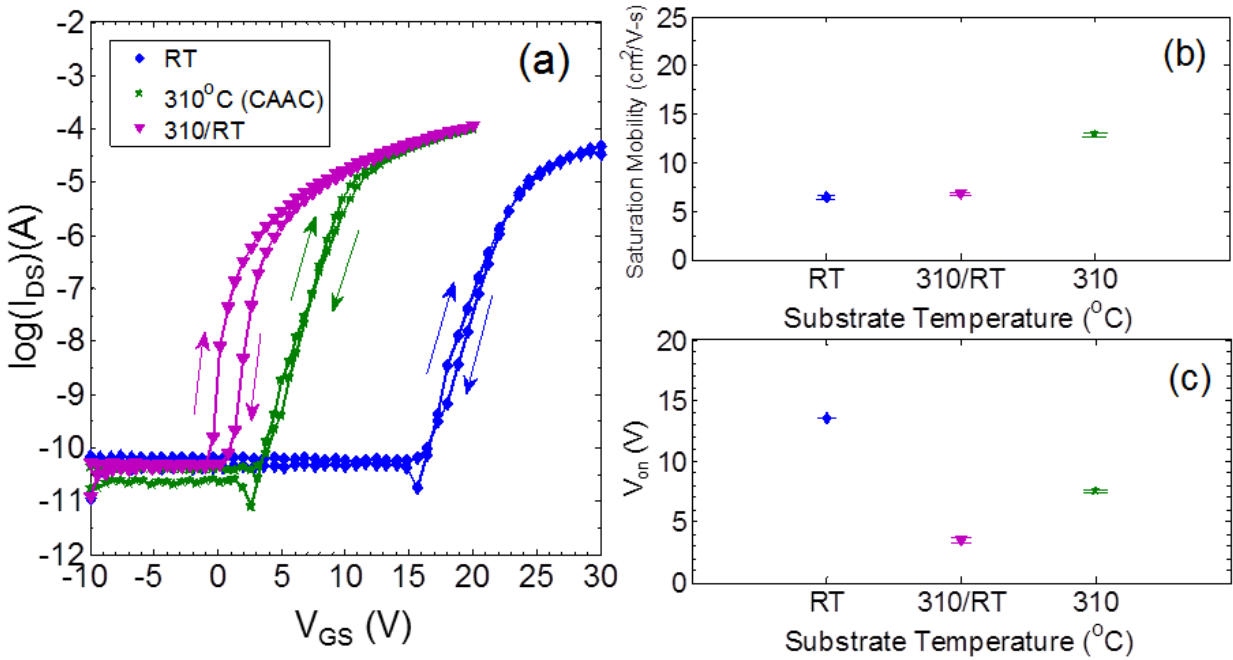


Figure 3-7. Electrical behavior of films with α -IGZO deposited at room temperature. (a) Transfer curves ($V_{DS} = 10\text{V}$), (b) saturation mobility and (c) turn-on voltage of IGZO TFTs deposited at substrate temperatures of 310°C (CAAC), 310°C (CAAC)/RT (amorphous), and RT (amorphous).

Figure 3-7 shows that the sweep hysteresis width of the $T_{310/RT}$ devices (a) was much larger than that exhibited by devices deposited at T_{310} and T_{RT} (b and c), indicating that this dual layer device is in an unstable state, electrically and structurally. In Fig. 3-5, there is no significant difference of off-state current between pure CAAC, pure amorphous (260°C), and dual layer (CAAC+ 260°C) TFT. However Fig. 3-7 indicates that films deposited at room temperature exhibit higher off-state currents compared to elevated temperature devices. It should be noted that the measured currents are an upper limit only, and the true off-state currents are expected to

much lower than observed in these measurements. (Our device measurements focused on the on-state and mobility parameters and we did not establish a noise sensitivity to accurately determine the true off-state current of these devices.)

3-6 Stability of dual-layer and single-layer IGZO TFTs:

Figure 3-8 shows the time dependence of the (a) saturation mobility and (b) turn-on voltage of T_{RT} , T_{260} , T_{310} , $T_{310/RT}$, and $T_{310/260}$ devices stored in the dark in a clean room air after 0, 37, 44 and 58 days. The saturation mobility in dual and single-layer TFTs remained essentially constant, but device to device variations narrowed with time. A notable exception was the $T_{310/RT}$ device in which the mobility rose from 6.7 to 20.5 $\text{cm}^2/\text{V}\cdot\text{s}$ after 38 days! Films deposited at elevated temperatures show relatively stable V_{on} decreasing slightly with time (total shift <2 V). In contrast, devices with films deposited at room temperature are unstable (both μ and V_{on}) with large positive shifts in V_{on} over the two month period. Table 2 summarizes the shifts in mobility and threshold voltage with time. Park [73] also observed V_{on} shifts which they attributed to water desorption from the back surface of a-IGZO, with the sign of the V_{on} shift depending on the film thickness. We believe this instability of room temperature single layer deposited films is related to water or OH adsorption with time. In the dual layer $T_{310/RT}$ device, the temporal changes in threshold and mobility are consistent with ionized hydrogen donors being lost.

Table 2. Electrical performance of single and dual layer deposited TFTs stored after 58 days.

Deposition Temp. (°C)	Mobility shift after 58 days (cm ² /V-s)	Turn-on Voltage shift after 58 days (V)	V _{on} Stable/Unstable
Single Layer Devices			
RT	6.4 → 0	3.5 → 8.9	Unstable drifting positive
260	15.3 → 15.7	7.6 → 6.2	Stable drifting negative
310	12.8 → 14.2	7.5 → 6.1	Stable drifting negative
Dual Layer Devices			
310/260	20.6 → 17.5	3.2 → 1.2	Stable drifting negative
310/RT	6.7 → 18.1	13.5 → 24.5	Unstable drifting positive

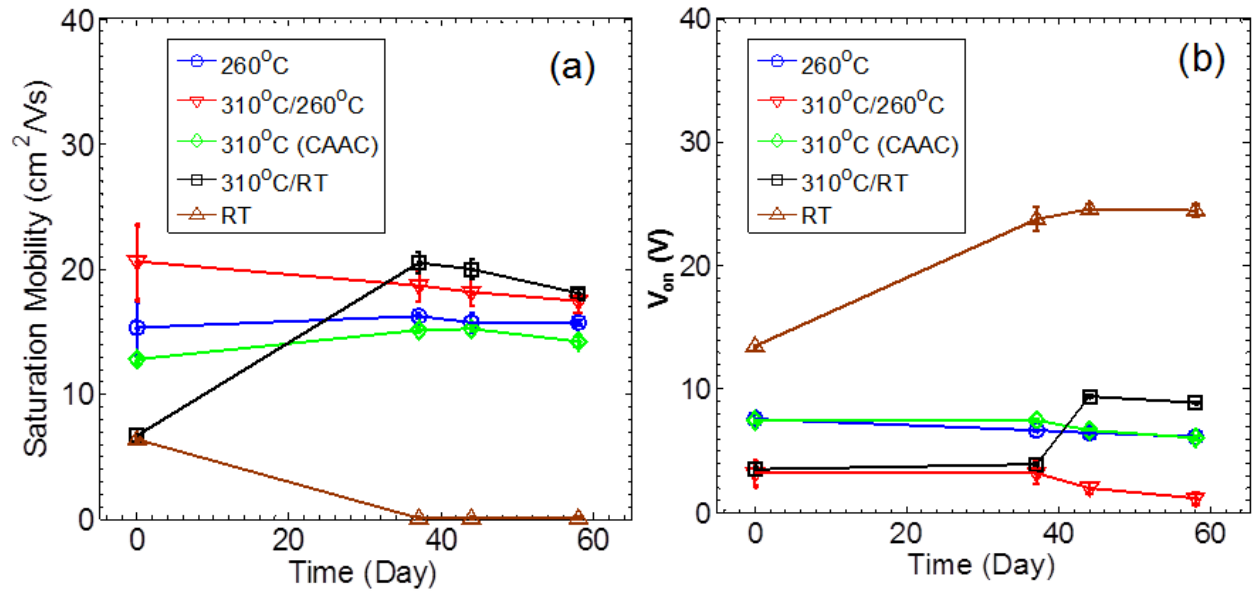


Figure 3-8. Changes in electrical properties over time. (a) Saturation mobility and (b) turn-on voltage of IGZO TFTs deposited at substrate temperature of 310°C (CAAC), 310°C (CAAC)/260°C (amorphous), 310°C (CAAC)/RT (amorphous), 260°C (amorphous) and RT (amorphous) as a function of time stored in dark clean-room air.

3-7 Mechanism of Device Improvement:

This dual-layer device design was motivated by the consideration that impurity solubility in the amorphous phase generally exceeds that in the crystalline phase. This well-known fact is used in the Si semiconductor industry to move impurities from crystalline transport regions to nearby amorphous/disordered regions in a process known as internal gettering [74]. In addition, disordered regions in Si equilibrate point defect concentrations that otherwise would need to

reach the surface to equilibrate. By analogy, we expected that a a-IGZO layer would getter impurities from the nanocrystalline CAAC phase and equilibrate defect concentrations during deposition.

The higher mobility in dual-layer devices as compared to single-layer devices confirms this to be the case when the capping layer is deposited at 260°C. At this temperature, gettering does appear to proceed all the way to the equilibrium since i) the saturation mobility of the $T_{310/260}$ device is stable and ii) the mobility of the ($T_{310/RT}$) TFT, over a period of two months, moves to the value observed in the $T_{310/260}$ sample. We demonstrated that setting up such an equilibrium results in remarkably stable devices in which the channel mobility, over time, no matter how disturbed, returns to an equilibrium value. No such device has been previously reported in the IGZO literature.

3-8 Diffusion model of device stability:

An estimate on the diffusivity of the moving species can be made using the approximation $x = 2\sqrt{Dt}$, in which x is the layer thickness of 20 nm and t is 38 days. This yields a diffusivity of $D_{RT} \sim 10^{-18} \text{ cm}^2/\text{sec}$. As to the temperature dependence of D , one can make a rough estimate from the observation that the \sqrt{Dt} product for the device activation anneal, 350°C for 30 minutes, is insufficient for the two layers to equilibrate in the $T_{310/RT}$ device, whereas they do equilibrate at room temperature over 38 days. The estimate is only first order, as exchange of hydrogen in the CAAC layer to the atmosphere is controlled by the permeability of the amorphous capping

layer, i.e. the product of solubility and diffusivity. As the temperature dependence of the solubility is not known we cannot take it into account. Such an estimate indicates that activation energy of migration E_A of the unknown species must be below ~ 0.2 eV. The activation energy is surprisingly low but is comparable to the value of 0.11 eV measured for the outmigration of hydrogen from IGZO[75] measured by Nomura et al. [76]. During out-diffusion of H from (2:2:1 oxide ratio) IGZO films, they observed two regimes. The estimated diffusivity from measurements below 200°C suggests a room temperature diffusivity of $1.8 \times 10^{-15} \text{ cm}^2 \text{ s}^{-1}$ while measurements above 300°C extrapolate to a room temperature diffusivity of $6.3 \times 10^{-25} \text{ cm}^2 \text{ s}^{-1}$. However, these measurements were made as an exchange rate with deuterium and in a reducing environment (5% $\text{D}_2/95\% \text{ N}_2$), while the current measurements indicate direct loss of hydrogen with no replacement in an oxidizing environment (ambient air). Given these differing conditions, and the approximations made, the current observed H diffusivity of $10^{-18} \text{ cm}^2 \text{ s}^{-1}$ is in a comparable range and reasonably consistent with the higher exchange diffusivity measured by Nomura. The diffusivity derived from layer equilibration kinetics is consistent with the movement of hydrogen. Thus, a model consistent with our observations is that hydrogen movement establishes equilibration between the two phases, and that the amorphous layer, in essence, acts as a “buffer” that keeps hydrogen content in the nanocrystalline CAAC layer at a low and stable value.

The amorphous capping layer has two interfaces, one with the crystalline CAAC layer, and one with the atmosphere. Across either interface, gas adsorption/desorption can take occur. At the surface of the amorphous capping layer, adsorption/desorption can take place. Other groups have seen the effect of O_2 [77] and humidity[78] adsorption/desorption on unpassivated backchannel of IGZO TFT. In our case, the temperature/time changes indicate that hydrogen distributes itself

between CAAC IGZO (known to contain hydrogen at the level of $1 \times 10^{20} \text{ cm}^{-3}$ [26, 27]) and amorphous IGZO, known to contain hydrogen at the level of $5 \times 10^{20} - 1 \times 10^{22} \text{ cm}^{-3}$ [27, 28]. This raises the question if sufficient hydrogen might escape from the free surface such that the capping layer no longer can buffer the hydrogen content of the CAAC. A simple estimate shows that the diffusivity of hydrogen at room temperature is too low to do so to a significant degree. Other observations indicate that the IGZO deposited in our group equilibrates on a similar time scale. For example, after laser annealing, we observe the mobility to decay in a few weeks from ~ 50 to $\sim 30 \text{ cm}^2/\text{Vs}$ [29]. Other groups have seen similar decay constants, for example in the decay of the temporary electric field induced high mobility in TFTs with a half gate top electrode in addition to a conventional gate [30]. The similar relaxation times suggest that the underlying mechanisms may be identical.

The decreased mobility of dual-layer devices with the a-IGZO deposited at room temperature can be understood as a stress effect arising from the two very different deposition temperatures that result in layers with different physical properties. In the language of oxide glass theory, the two layers have very different fictive temperatures but, being bonded together, are forced to thermally expand identically during the 350°C activation anneal, leaving room temperature residual internal stresses after cool down from the activation anneal.

As H migrates, it rearranges strained bonds with in the IGZO glass and hence relieves stresses in the film. The effects of stress and, more generally, the existence of an equilibrium state in IGZO can be accounted for in the modern, constraint based, theory of oxide glasses [31, 32].

3-9 Benefits of dual layer structure:

Further improvements, in particular optimizing the robustness of the equilibrium state, might be achieved by optimizing the deposition conditions of the two layers for other deposition systems. From a process engineering point of view, an additional benefit of the dual-layer device appears to be that the amorphous layer stacked on top of CAAC layer prevents environmental contamination from reaching the active transport layer, as indicated by the constant V_{on} in unpassivated dual layer devices, compared to the drift in V_{on} in single layer room temperature devices. Both the channel (CAAC IGZO) and passivation layer (amorphous IGZO) can be deposited in the same chamber as only the substrate temperatures needs to be changed, and secondly, its use eliminates the need to deposit an etch stop layer. In particular, the reduced sensitivity may be an advantage as the industry moves to eliminate the etch stop layer. The IGZO TFT industry is actively exploring ways to eliminate the etch stop layer as it required additional deposition and lithography step, reducing yield.

One final issue regarding the first 4 nm of the CAAC IGZO layer warrants some discussions. In our dual layer IGZO TFT, we assume that the entire CAAC layer is uniform and electrons are transported in a nearly impurity free region (interface of CAAC IGZO/SiO₂). However, in HRTEM cross section of an unannealed CAAC IGZO film, Lynch et al. [83] observed that the first 4 nm was amorphous and not CAAC. Yoshino et al. [84] observed similar behavior for ZnO. This indicates that, in our dual-layer IGZO TFT, electron transport may occur at an amorphous IGZO/SiO₂ interface and not at a CAAC IGZO/SiO₂ interface. This does not impact the proposed model, as impurities still diffuse from the CAAC layer to the upper amorphous

layer leading to a cleaner channel layer at the IGZO/SiO₂ interface; impurities are still trapped in upper thicker amorphous layer. In addition, potentially, post-annealing may crystallize this interface. Further experiments are necessary to established the impact of this interfacial amorphous layer. (see future work chapter).

3-10 Summary:

CAAC (c-axis aligned crystal)/amorphous IGZO dual-layer IGZO TFTs, with the channel being implemented in the CAAC layer, were fabricated and characterized. These TFTs exhibit saturation field-effect mobilities of $\sim 20 \text{ cm}^2/\text{Vs}$, exceeding that achieved in reference TFTs using either a single layer of CAAC ($\sim 13 \text{ cm}^2/\text{Vs}$) or a single layer of amorphous IGZO ($\sim 15 \text{ cm}^2/\text{Vs}$). The highest mobility of $20.6 \text{ cm}^2/\text{Vs}$ was measured in TFTs in which the amorphous layer and CAAC layers were deposited at 260°C and 310°C , respectively. In samples in which the amorphous IGZO layer was deposited at RT, the mobility improved over a period of months from initially $6.7 \text{ cm}^2/\text{Vs}$ to $20.5 \text{ cm}^2/\text{Vs}$. This observation, and the observation that device-to-device variation in all dual layer devices narrow with time, suggest that equilibrium between the two layers is established at room temperature in $\sim 10^6 \text{ s}$. A model that assumes that the two layers equilibrate by the movement of hydrogen that as it moves, rearranges high stress bonds is consistent with our observations and the published diffusivity of hydrogen in IGZO [75].

CHAPTER IV

IV. STRUCTURAL CHANGES IN IGZO DURING CO₂ LSA AND FURNACE ANNEALING

4-1 Introduction and summary:

Understanding the changes in IGZO structure with annealing temperatures is important. Annealing may lead crystallization of the material, or other changes in the structure of the material. Indeed, the annealing temperature is an important parameter that must be optimized for device fabrication. As an alternative, laser spike annealing (LSA) can also be used to access short time and high temperature regimes.

Recently, Yamazaki et al. reported that the TFT performance could be enhanced by fabricating devices in a nanocrystalline, highly textured, c-axis aligned crystalline (CAAC) IGZO thin film[41]. Compared to a-IGZO TFTs, CAAC TFTs exhibit enhanced reliability, stability, and an extremely low off-state leakage current. CAAC occupies the structural space between a-IGZO and truly polycrystalline films. Ito and Kimizuka concluded from electron-beam diffraction that CAAC consists of 1–3 nm nanocrystals, packed with the c-axis normal to the surface, a-b planes exhibiting a mosaic pattern in-plane, and no clearly defined grain boundaries[68].

Understanding the transition annealing temperature from amorphous to CAAC is important. Nomura et al. showed the XRD figures of a-IGZO films furnace annealed from 400 to 600°C with interval of 25°C and found that the onset of crystallization at ~520°C [85]. Generally, higher annealing temperature (higher kinetic energy) leads to higher crystallinity. Laser annealing with millisecond dwell times will likely require a higher peak temperature to crystallize IGZO compared to furnace annealing as the LSA timescales are so short that structural changes are kinetically suppressed. LSA timescales are also sufficiently short that minimal compositional changes are expected despite the higher temperatures. In contrast, furnace annealing provides sufficient time for both structural relaxation and densification of the films.

4-2 Experimental methods

IGZO films (50 nm thick) were RF sputtered from an oxide target ($\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO} = 1:1:1$) onto Si wafers with a 100 nm thermal oxide (grown in dry O_2 and 3% HCl at 1100°C for 30 min) to serve as the substrate. Films were sputtered using 120 W of RF power and a substrate temperature of 260°C in an Ar: O_2 ratio of 9:1 maintained at 5 mTorr.

To compare the crystallinity of IGZO annealed by furnace and LSA, annealed IGZO films were measured using conventional X-Ray diffractometer. As-deposited IGZO films were split into two samples. One sample was furnace annealed at 350°C for 30min in dry air. The second sample was area annealed by LSA (for whole 2×5 cm sample) at a peak temperature of 430°C

with a 1ms dwell in air. X-ray diffraction (XRD) patterns were obtained before and after annealing using a Rigaku Smartlab X-Ray diffractometer with a Cu K_{α} source.

To further compare unannealed films with LSA annealed films, X-ray measurements were obtained from ss-LSA and area-LSA anneals. Single stripes (ss-LSA) (~700 μm FWHM wide) with peak temperatures of 400, 750 and 800°C scans (dwell time = 1 or 2 ms) were scanned parallel to a reference Cu tape. On the same sample, area-LSA (width overall 2.8mm, 50 μm overlapped) with peak temperature of 400 were also produced. A second sample, from the same IGZO deposition, was area-LSA annealed with a peak temperatures of 1400°C for dwells from 0.75 to 2 ms. These conditions are shown in Fig. 4-1 with details for each scan given in Table 3. X-ray spectra were obtained at the A1 beamline of the Cornell High Energy Synchrotron Source (CHESS). 2D X-ray diffractograms were obtained every 25 μm along LSA annealed samples. For 700 μm FWHM wide ss-LSA scans, this provided X-ray spectra corresponding to the spatial peak temperature profiles. For the 2 mm wide area-LSA scans, X-ray spectra were obtained either every 25 μm (400°C area) or every 250 μm (1400°C area).

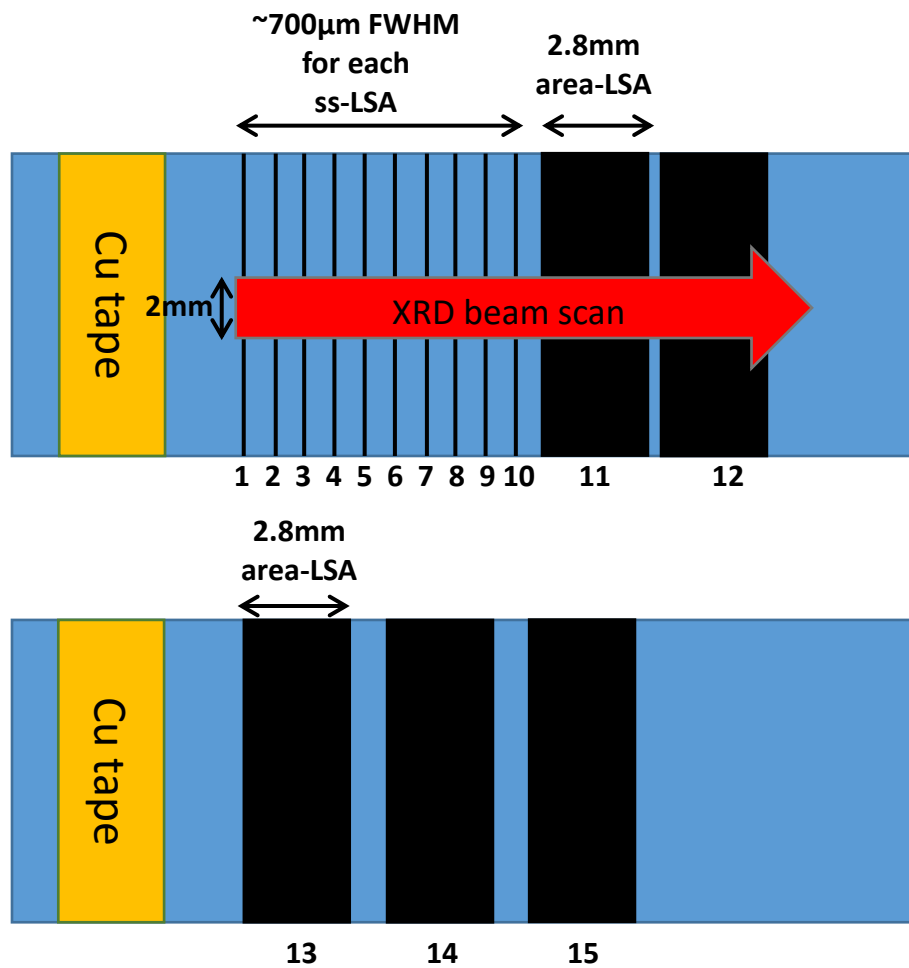


Figure 4-1. XRD beam scan on the ss-LSA and area-LSA IGZO thin films in CHESS.

Table 3. Conditions for each LSA scan on IGZO sample.

Position	Width (μm)	Peak Temperature ($^{\circ}\text{C}$)	Dwell time (ms)	Overlap (μm)	Scan Type
1	700	400	1	N/A	Single
2	700	800	1	N/A	Single
3	700	750	1	N/A	Single
4	700	800	2	N/A	Single
5	700	750	2	N/A	Single
6	700	400	1	N/A	Single
7	700	800	1	N/A	Single
8	700	750	1	N/A	Single
9	700	800	2	N/A	Single
10	700	750	2	N/A	Single
11	2800	400	1	50	Area
12	2800	400	1	50	Area
13	2000	1400	1	50	Area
14	2000	1400	2	50	Area
15	2000	1400	0.75	50	Area

2D X-ray scattering images were collected on the A1 beamline of the Cornell High Energy Synchrotron Source (CHESS) using monochromatic radiation with $\lambda = 0.63 \text{ \AA}$ (X-ray energy of 19.65 keV). The beam size was 25 μm by 2mm and spectra were obtained every 25 and 250 μm at room temperature (1360 spectra). Images were collected using an ADSC Quantum-210 CCD (charge-coupled device) detector with pixel sizes of 102.4 μm by 102.4 μm and a total of 2048 by 2048 pixels. The sample to detector distance was nominally 204 mm. Images were empty field corrected using Igor Pro 6.37 software.

4-3 XRD of as-deposited, furnace annealed and LSA annealed IGZO films:

XRD was used to compare as-deposited IGZO with films annealed by furnace or by LSA (Fig. 4-3). Spectra under all conditions exhibit only a weak, broad diffraction peak ($2\Theta = 31^\circ$) indicating retention of the amorphous phase under both LSA and furnace anneals. There are, however small but significant differences in the peak position between furnace and LSA annealed films. The peak in the as-deposited film is fit well by a Gaussian curve centered at $31.1 \pm 0.1^\circ$ with a FWHM of 2.2° . After LSA, this peak remains essentially unchanged at $31.1 \pm 0.1^\circ$ and with a FWHM of 2.1° . The areas under the curves remain constant as well. In contrast, there is an apparent structural relaxation of the film after furnace anneal, as the X-ray peak shifts to $32.0 \pm 0.1^\circ$ and the area increases by approximately 17%. The increase in 2Θ corresponds to a reduction in the average atomic separation from 0.287 nm to 0.279 nm (2.8% change) and hence a volume reduction of almost 8.5% (through Bragg's formula $n\lambda = 2d\sin\Theta$). These shifts indicate a densification of the film during furnace processing that is absent in LSA. Neither anneal suggests any crystallization, as c-axis aligned film (CAAC) exhibits a significantly sharper peak at 30° [67]. This is consistent with literature data showing that furnace annealing can only crystallize IGZO above 520°C [85].

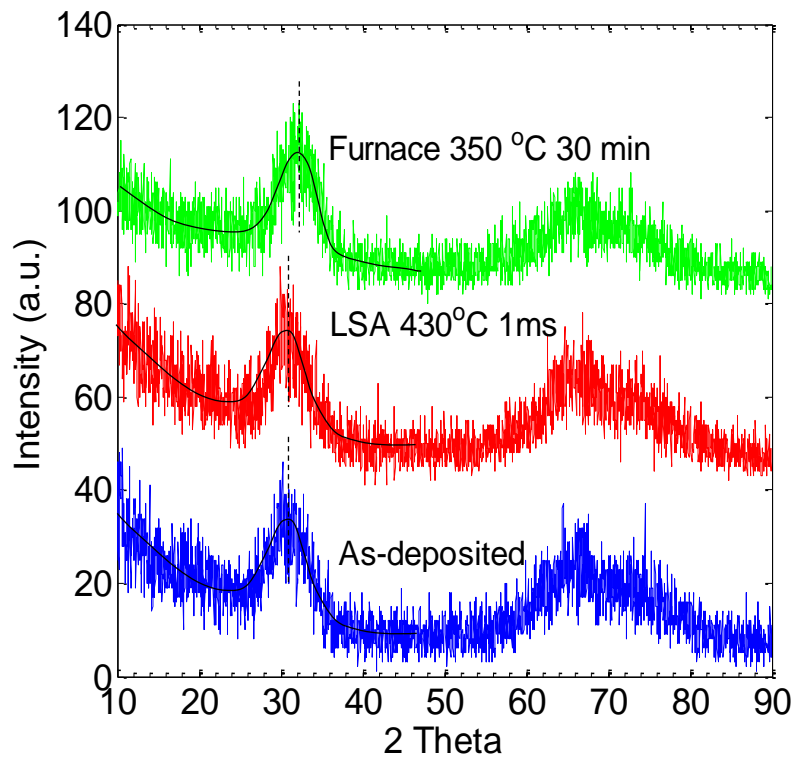


Figure 4-3. XRD of as-deposited LSA annealed, and furnace annealed IGZO films. The broad peak at 31° for as-deposited *a*-IGZO remains essentially unchanged under LSA. The peak shifts to 32° when IGZO is densified by a furnace anneal. The weak peak at 66° is a substrate artifact.

4-4 Analysis of CHESS 2D X-ray patterns:

To further understand the crystallinity difference between LSA and unannealed IGZO films, 2D X-ray scattering images of unannealed, ss- and area- LSA IGZO were collected. Figure 4-4 (a) shows a typical CCD image from an ss-LSA IGZO sample. The high intensity (orange) spots arise from Si diffraction in substrate, with bands (yellow) between them due to thermal diffuse scattering. The conventional scattering angle Θ is proportional to the radius from the origin,

giving rise to circular arcs corresponding to a given lattice spacing. The arc direction, labelled as χ , measures the texture and alignment with the center vertical line corresponding to plane parallel to the sample surface. We integrated the intensity around the dashed black line (between the dashed red lines) which included both the IGZO CAAC ($2\theta = 30^\circ$) and amorphous ($2\theta = 32^\circ$) scattering. This is plotted as a function of the χ direction in Fig. 4-4 (b). The sharp bands around 40° and 140° corresponds to Si diffraction and the weak band from 65° to 120° corresponds to both the amorphous and CAAC structures. The alignment in χ indicates a weak CAAC IGZO structure, presumedly due to elevated substrate temperature (260°C) during IGZO deposition.

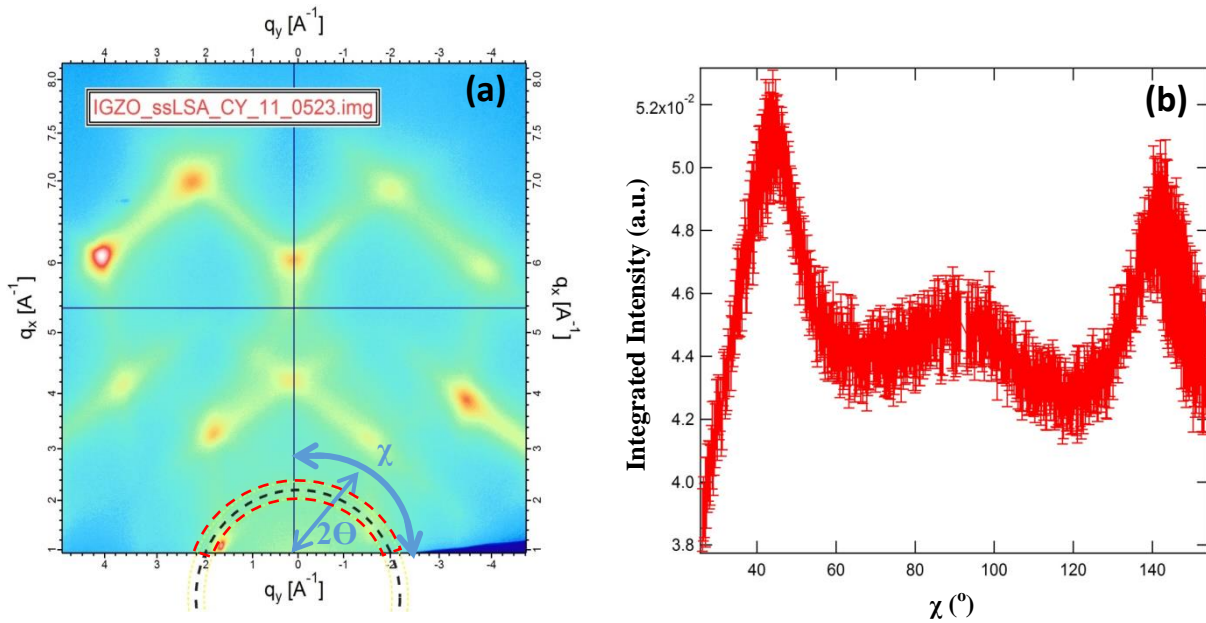


Figure 4-4. (a) Area diffraction pattern recorded with CCD detector in CHESS (b) Integrated intensity v.s. χ angle for the area around black dash line (area in dashed red lines) in area diffraction pattern.

Fig. 4-5 shows the integrated intensity as a function of χ for multiple scans taken across the ss-LSA areas. All of the spectra are essentially identical with no significant changes observed. This indicates that LSA cannot convert IGZO from amorphous to CAAC for any peak temperatures below 800°C with either 1 or 2 ms dwell.

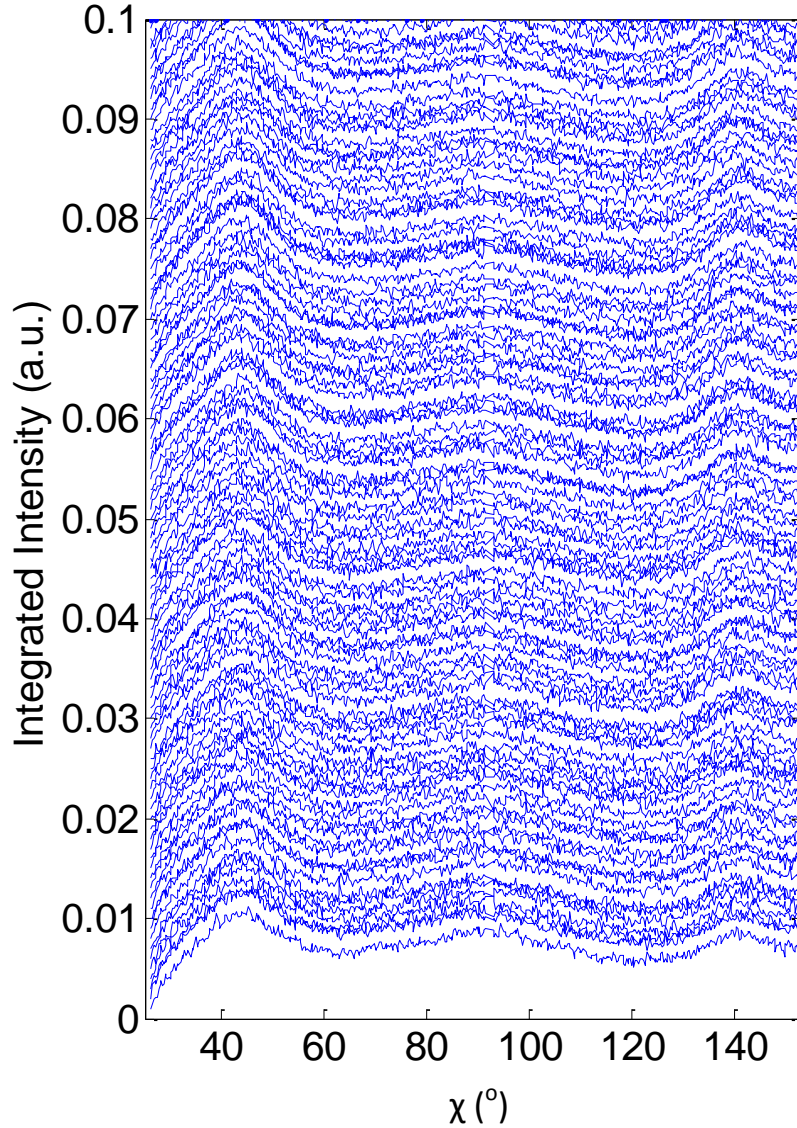


Figure 4-5. Integrated intensity as a function of χ for the first 3 ss-LSA scans in Fig. 4-1. All of the ss-LSA and area-LSA (400°C only) were identical spectra for areas annealed at temperature up to 800°C are indistinguishable from unannealed areas .

To explore potential structural changes between unannealed and LSA IGZO films, we integrated the intensity along the q direction (reciprocal of d space) from 1 to 8 \AA^{-1} for all the ss-

LSA (400, 750 and 800°C), area-LSA (400°C) and unannealed regions in the IGZO sample. These data (Fig. 4-6 (a)) were integrated over a sector $\pm 20^\circ$ wide (between the 2 dashed red lines) with the integrated intensity shown as a function of d spacing in Fig. 4-6 (b). The two sharp peaks near 0.8, 1.1 and 1.6 Å correspond to Si thermal diffuse scattering with the broad peak at ~ 2.9 Å corresponding to IGZO.

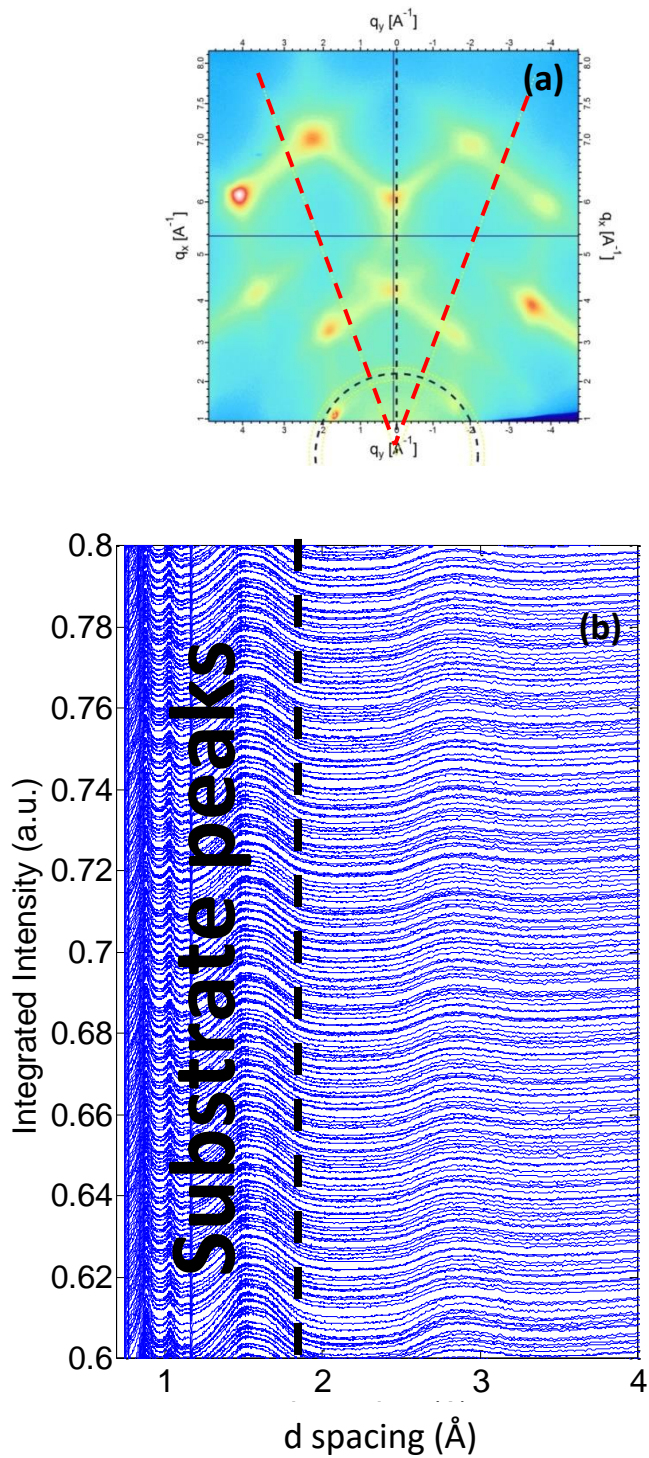


Figure 4-6. (a) Representation area diffraction pattern showing $\pm 20^\circ$ integration sector (dashed red lines) (b) Integrated intensity as a function of d spacing across the first three ss-LSA scans. The IGZO peak near 2.8 \AA is indistinguishable between annealed and unannealed areas up to 800 $^\circ$ C.

The primary IGZO peaks near 2.8 \AA were fit to bi-Gaussian curves with a linear background to determine the centroid. These centroid positions are shown as a function of positions along the first sample in Fig. 4.7. The d-spacing remain essentially constant among unannealed, 400, 750 and 800°C ss-LSA and 400°C area-LSA regions, indicating that there is no significant change in lattice constants during LSA up to 800°C . The slight rise between 13 and 19 mm does not correspond with any annealing structures and is likely an artifact; of the jump indeed is less than the measurement uncertainty. These data are also consistent with the Rigaku comparison of furnace and LSA anneals. At all temperatures below 800°C , there is no evidence of any structural changes in the IGZO network. Only under furnace annealing for 30 min is the sufficient time to observe densification of the films.

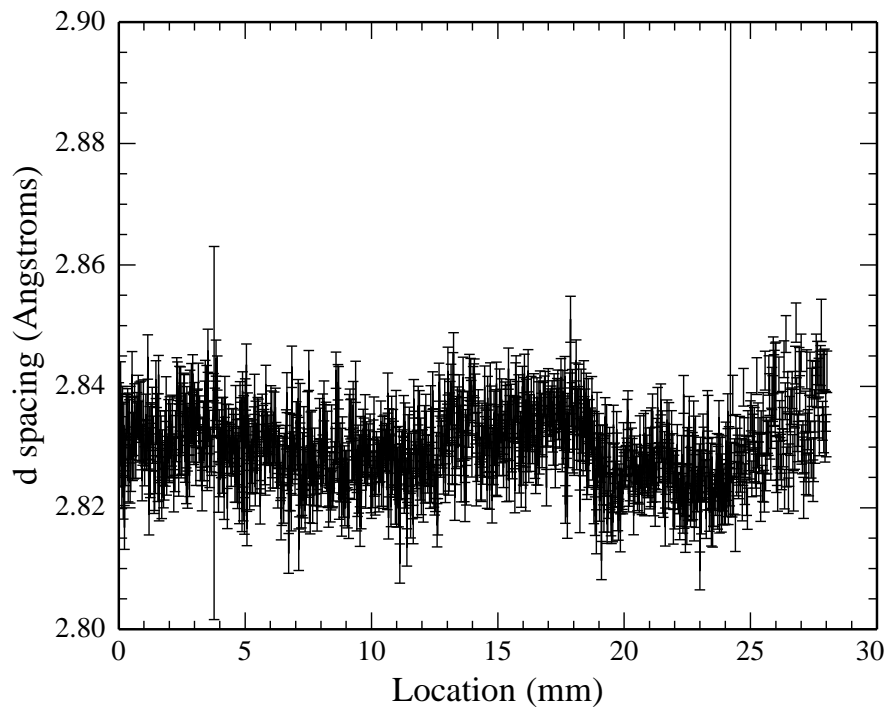


Figure 4-7. d spacing as a function of location along the ss-LSA, area-LSA and unannealed regions of the first IGZO sample. No significant differences are observed.

4-5 Crystallization under LSA:

Under LSA, no CAAC IGZO formed even at 800°C. Eventually CAAC IGZO must crystallize even in the millisecond time frame. To understand this limit, IGZO film were also annealed at 1400°C using dwell times of 0.75 to 2 ms by area-LSA. This is essentially the melting point of silicon (substrate) and damage occurs even at this point. Figure 4-8(a) shows the XRD 2D image of the sample annealed to 1400°C. There are obvious bright spots in the IGZO ring region indicating textured CAAC IGZO formation. We integrated the intensities in the IGZO ring region as a function of χ across both unannealed and 1400°C area-LSA regions as shown in Fig. 4-8 (b). At $\chi = \sim 90^\circ$, the CAAC IGZO intensities gradually increased as the X-ray scan move from unannealed areas to the uniform 1400°C area-LSA region. We cannot precisely determine the transition temperature from these data. However, the data is an existence proof of the annealing threshold for future works.

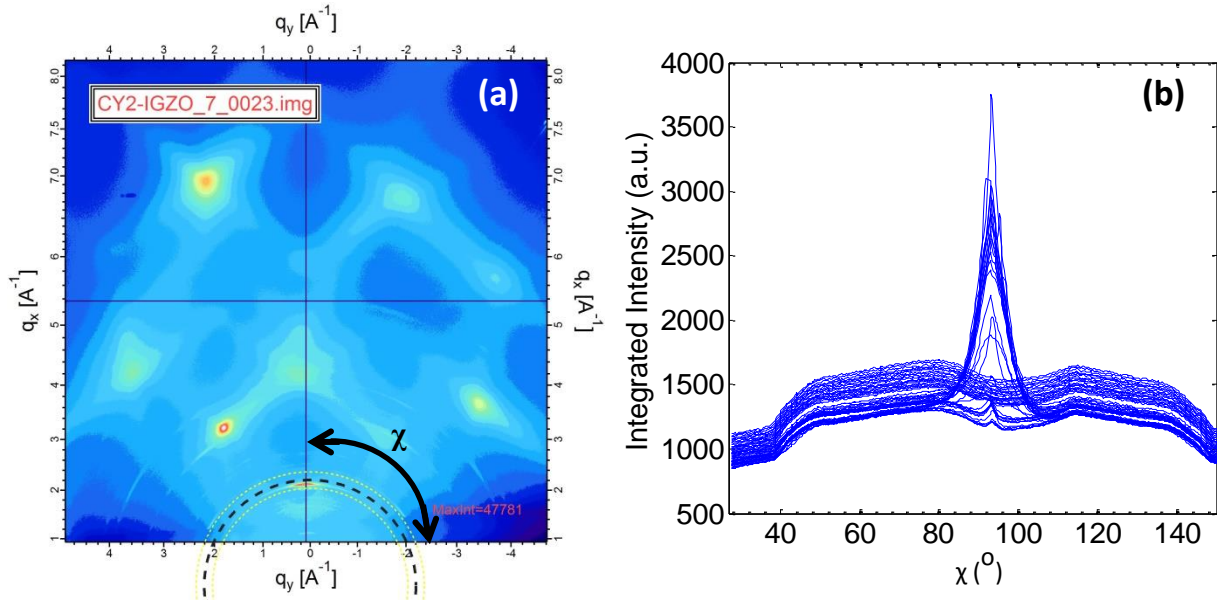


Figure 4-8. (a) Area diffraction pattern of IGZO LSA annealed at 1400°C. (b) Integrated intensity as a function of χ angle for scans spanning the region from unannealed to uniformly annealed at 1400°C.

4-6 Linkage of XRD structure and oxygen vacancies:

Kamiya and Hosono et al.[86] proposed a detailed model for oxygen vacancies in IGZO, postulating the formation of a variety of shallow donor and deep trap states. They suggested that the nature of the oxygen vacancy depends critically on the local environment, specifically the open space (free volume) in the vicinity. Oxygen vacancies in an open environment (large free volume) are associated with deep level trap states while more restricted environments (small free volume) lead to shallow donor states. Thermal annealing can impact both the density of the oxygen vacancies, as well as the distribution of vacancies among the various donors and trap configurations.

Partial O₂ pressure jump experiments have shown that furnace annealing provides sufficient time for significant equilibrium changes in the total density of oxygen vacancies through exchange of oxygen with the annealing ambient [87]. In contrast, LSA timescales are sufficiently short that minimal compositional changes are expected despite the higher temperatures. Furnace annealing also provides sufficient time for structural relaxation and densification of the films, changes which we do not observe on LSA time scales below 800°C. Based on XRD measurements, the average interatomic spacing after furnace annealing is reduced by approximately 2.8% (peak shift from 31° to 32°), corresponding to an 8.5% volume compaction. For LSA, no measurable change was observed. This change may be related solely to structural relaxation, or may be related to loss of volatile species such as hydrogen. In either case, oxygen vacancies following LSA annealing have substantially more free volume compared to furnace-annealed films.

4-7 Summary:

XRD was used to compare structure changes of furnace and LSA annealed IGZO films. Furnace annealing provides sufficient time for structural relaxation and densification of the films, changes which we do not observe on LSA time scales below 800°C. Based on CHES XRD over wide range of conditions, there is no evidence of any structural changes in the IGZO network at all temperatures below 800°C. Finally, we show that CAAC-like crystallized IGZO can be formed in the 1ms time frame with annealing to 1400°C. These data suggest that oxygen vacancies after LSA annealing could have substantially more free volume compared to furnace-annealed IGZO films.

CHAPTER V

V. HIGH MOBILITY a-IGZO TFTs FORMED BY CO₂ LASER SPIKE ANNEALING AND POSSIBLE MODEL

5-1 Introduction:

Amorphous semiconductors are widely used in the fabrication of active matrix displays. For the past 30 years, hydrogenated amorphous silicon (a-Si:H) based TFTs have been used extensively. However, the relatively low mobility ($\sim 1 \text{ cm}^2/\text{Vs}$) and the instability under electric field bias stress and illumination increasingly limits a-Si:H devices use in advanced applications. Compared to conventional a-Si:H, amorphous InGaZnO₄ (a-IGZO) devices exhibit significant improvements in electrical performance and hence are considered to be a promising candidate for future active-matrix flat-panel displays (AM-FPD) [9].

In 2004, Hosono first reported the use of amorphous oxide semiconductors (AOS), specifically a-InGaZnO₄ (a-IGZO), for the fabrication of transparent and flexible thin film transistors (TFTs)[2]. Over the past decade, research has focused on optimizing properties of IGZO by controlling process variables including channel layer stoichiometry [88] and thickness [22], reactive sputtering O₂ partial pressure [89], post-sputter annealing [90] and, in particular, post-deposition annealing. This post-deposition anneal is critical in achieving high mobilities.

The majority of these studies focus on furnace annealing in a controlled ambient [90][25][91][92][93], with the highest reported field-effect mobility for furnace post-annealing of $35 \text{ cm}^2/\text{Vs}$ [94]. Several groups also explored alternate annealing techniques including nanosecond ultra-violet (UV) laser annealing [95][96][97][98][99] and UV lamp irradiation [100]. Nakata et al. achieved mobilities of nearly $16 \text{ cm}^2/\text{Vs}$ using excimer laser annealing with an estimated peak temperature of approximately 1500°C [97]. Similarly, Zan et al. showed improved stability following 266 nm UV laser irradiation or excimer UV lamp exposure [100]. The maximum mobility they were able to achieve was $\sim 8 \text{ cm}^2/\text{Vs}$.

Laser spike annealing (LSA) provides an opportunity to anneal films on sub-millisecond to millisecond time frames using a scanned continuous wavelength (CW) laser source [101]. In this work we explore the use of a CO_2 ($\lambda=10.6 \text{ }\mu\text{m}$) based LSA with millisecond dwell times to anneal a-IGZO TFTs deposited by radio frequency (RF) sputtering. In LSA (Fig. 5-1), a line-focused continuous wave CO_2 laser beam ($\lambda=10.6 \text{ }\mu\text{m}$) is scanned over the substrate, rapidly heating the surface to a peak temperature which subsequently cools by thermal conduction into the substrate as the beam passes. A peak temperature in the range of 300 to 500°C was achieved by scanning a $\sim 90 \text{ }\mu\text{m}$ by $700 \text{ }\mu\text{m}$ beam at 100 mm/s resulting in a dwell time of 1 ms . Peak temperatures reported are based on the measured temperature of blank Si wafers[49]. As the IGZO film were only 50 nm thick, the temperature of the films is expected to be very nearly equal to that of the substrate surface. In addition to rapid heating, LSA samples also cool rapidly at $\sim 350,000 \text{ K/s}$, in contrast to furnace samples that cool at $< 2 \text{ K/s}$. These high quench rates, which enable the retention of metastable structures, result from the bulk of the substrate remaining near room temperature during the heating which subsequently quenches the surface temperature as the laser passes. The thermal diffusion length for millisecond timescales is on the

order of 100 μm compared to a wafer thickness of 450-700 μm . Consequently the substrate remains cold and quenches the surface temperature rapidly in the millisecond timescale.

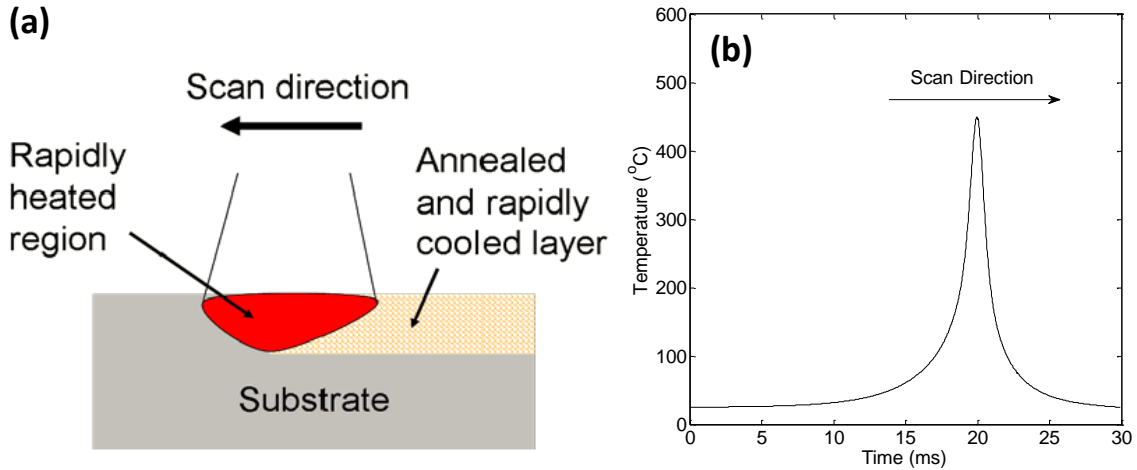


Figure 5-1. (a) Line-focused continuous wave CO_2 laser beam scanning over the substrate surface, rapidly heating the surface to a peak temperature which subsequently cools by thermal conduction into the substrate as the beam passes. (b) Simulation of the film surface temperature as a function of time for a 1 ms dwell scan of a CO_2 ($\lambda=10.6 \mu\text{m}$) laser at a peak power of 400 W/cm.

In this work we report on properties of IGZO TFTs fabricated using laser spike annealing (LSA) with a scanned continuous wave CO_2 laser. For peak annealing temperatures near 430°C and a 1ms dwell, TFTs exhibit saturation field-effect mobilities above $70 \text{ cm}^2/\text{Vs}$ ($V_{\text{on}} \sim -3\text{V}$), a value over 4 times higher than furnace-annealed control samples ($\sim 16 \text{ cm}^2/\text{Vs}$). A model linking oxygen vacancy defect structures with free volume remaining after the LSA anneal, and diffusion of H impurities, is proposed to explain the high mobility. This mobility is also shown to be comparable to the estimated trap-free mobility in oxide semiconductors and suggests that

shallow traps can be removed by transient thermal annealing under optimized conditions.

5-2 Experimental for IGZO TFTs annealed by furnace v.s. CO₂ LSA

Sputter condition to achieve high mobility TFTs with laser annealing were critical. The specific conditions began with the sputter chamber being treated with oxygen plasma clean at 40W with 10 sccm O₂ without moisture trap for 100 min (dummy Si wafer with 100nm thermal oxide) before IGZO deposition. IGZO films (50 nm thick) were RF sputtered from an oxide target (In₂O₃:Ga₂O₃:ZnO = 1:1:1) onto Si wafers with a 100 nm thermal oxide (grown in dry O₂ and 3% HCl at 1100°C for 30 min) to serve as the gate dielectric and substrate. Films were sputtered using 120 W of RF power and a substrate temperature of 260°C in an Ar: O₂ ratio of 9:1 maintained at 5 mTorr. TFTs were formed by wet etching the IGZO in 2 wt% HCl to define W/L = 200/50 μm channel region followed by evaporation and liftoff of Ti/Au (10/100 nm) source/drain contacts (inset in Fig. 5-2). No back channel passivation was used.

We do not fully understand how deposition conditions impact the device performance. To get high mobility devices, the process was tuned to give initially metallic films. This was achieved by an extensive oxygen plasma cleaning (100 min) prior to IGZO sputtering. Without this cleaning, deposited films were semiconducting. This suggests that the oxygen plasma is responsible for doping either via hydrogen impurities or oxygen vacancies.

To look for differences in the chamber conditions, a residual gas analyzer was used to compare chamber cleaning protocols. Two different cleaning protocols prior to IGZO deposition were compared. The dashed curve in Fig. 5-2 shows the P_{H₂O} during IGZO deposition after the LSA cleaning protocol. This protocol is for a 100 min oxygen plasma with the sample holder at

room temperature. The solid curve shows P_{H_2O} after a normal chamber clean which uses a 20 min outgas of the substrate holder at 600°C followed by 10 min oxygen plasma while the sample holder is cooling. For LSA film depositing, the P_{H_2O} is substantially higher leading to the metallic behavior. We speculate that exposed surfaces on the sputter chamber wall continue to outgas H_2O during the subsequent deposition.

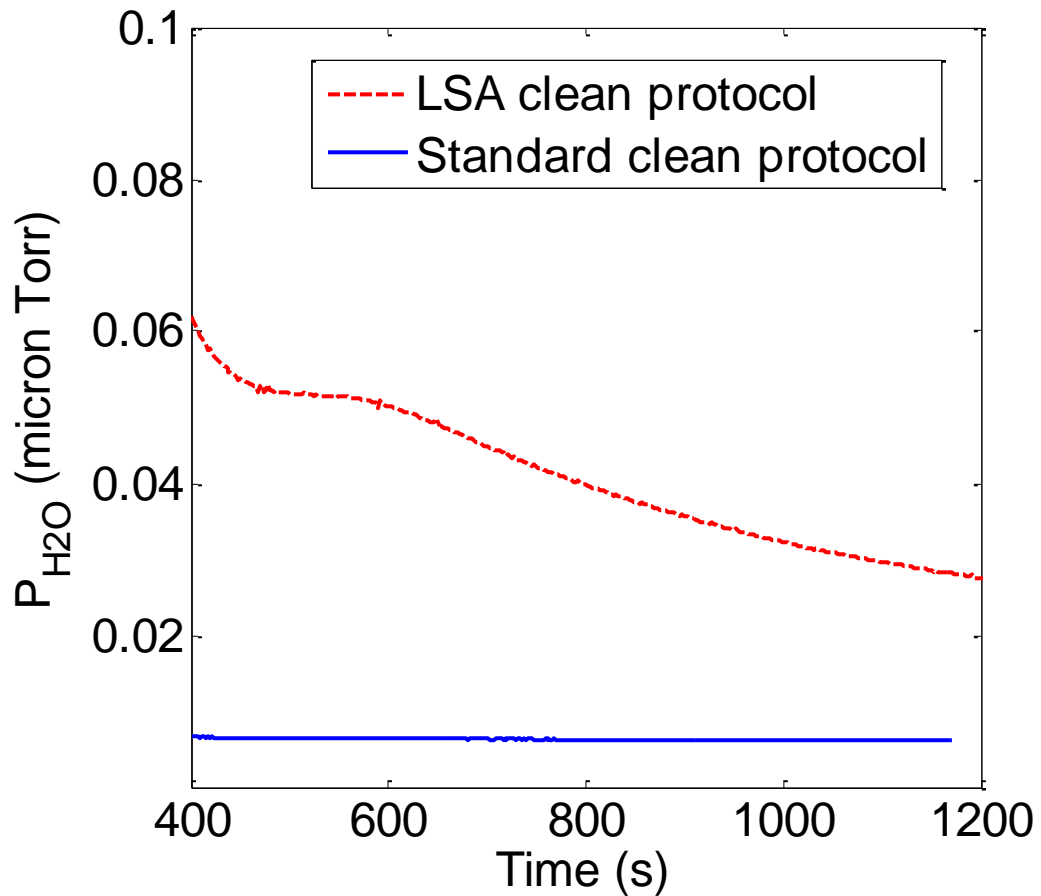


Figure 5-2. Residual gas analysis (RGA) of P_{H_2O} during IGZO deposition after different cleaning protocols. See text for details of the cleaning protocols.

These TFTs were subsequently divided into two groups, with the first furnace annealed at 350°C in dry air for 30 minutes, and the second annealed by LSA at peak temperatures between 300 and 500°C. Electrical measurements were carried out using a Karl Suss PSM6 probe station at room temperature in the dark. The transfer characteristics were measured from $V_{GS} = -20$ to 20 V at $V_{DS} = 10$ V. Saturation field-effect mobility and on voltage were determined by fitting the square root of the saturation current ($I_{DS,sat}$ from 0 to 1 mA) as a function of the gate voltage (V_{GS}) using $I_{DS,sat} = \mu \times C_{ox} \times \frac{W}{L} \times \frac{(V_{GS} - V_T)^2}{2}$, [69] where μ is the saturation field-effect mobility, $W/L = 200/50$ is the channel width to length ratio, and $C_{ox} = 32.3$ nF/cm² is the gate dielectric capacitance.

5-3 Electrical performance of IGZO annealed by furnace v.s. CO₂ LSA:

The saturation mobility of devices fabricated in as-deposited IGZO was typically 10-12 cm²/Vs with a large negative V_{on} (~-20 V). The effects of annealing are shown in Figure 5-3, showing the (a) output and (b) transfer characteristics of devices furnace (350°C) and LSA annealed (peak temperatures of 410, 430 and 455°C). With furnace annealing, the mobility increased to 16 cm²/Vs and the turn-on voltage shifted to +5 V. LSA annealing at a peak temperature of 430°C, in contrast, yielded devices with saturation mobilities above 70 cm²/Vs and turn-on voltages near -5V (Fig. 5-3(a)). The process window to achieve high mobilities is relatively narrow as LSA anneals to peak temperature of 410 and 455°C show mobilities of < 25 cm²/Vs with large negative turn-on voltages. The sub-threshold slope for LSA annealed devices under optimal conditions is large, typically 2300 mV/dec, indicating a large trap density.

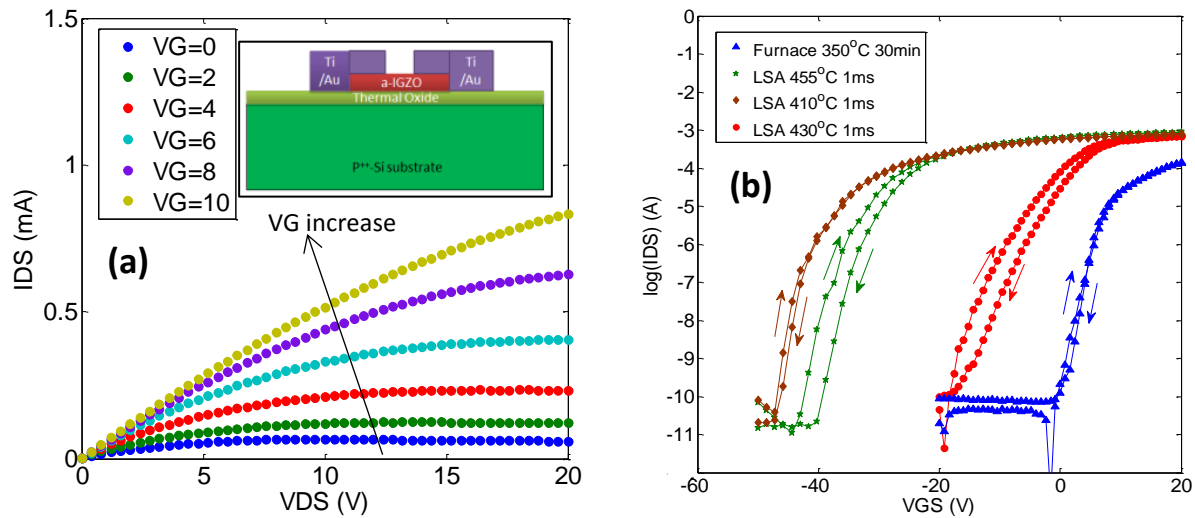


Figure 5-3. (a) Output curves ($V_{GS} = 10$ V) of IGZO TFTs LSA annealed with a peak temperature of 430°C for 1ms with a mobility of $75\text{ cm}^2/\text{Vs}$ and (inset) TFT cross-section structure. (b) Transfer curves ($V_{DS} = 10$ V) of furnace and LSA annealed TFTs at temperatures below, at, and above optimum peak temperature.

Average TFT electrical characteristics across each wafer are summarized in Table 3. These results were reproducible in several independent runs with LSA annealed mobilities (averaged over the wafer) of 43.1, 48.9, 73.5 and $56.4\text{ cm}^2/\text{Vs}$. Inspection of the table shows the high mobility is clearly sensitive to the precise peak LSA anneal temperature, a finding to be discussed later.

Table 4. Electrical performance of as-deposited, furnace annealed, and LSA annealed TFTs. Uncertainties are the standard deviation of devices processed in the same run.

	$\mu_{\text{sat,FET}}$ (cm ² /Vs)	V_{on} (V)	S.S. (mV/dec)
As-deposited	12.0 ± 0.5	-20.0 ± 2.4	940
Furnace (350°C, 30 min, dry air)	16.3 ± 0.7	5.4 ± 0.1	960
LSA (1 ms dwell, $T_{\text{peak}} = 410^\circ\text{C}$, air)	11.6 ± 0.1	-35.3 ± 3.0	730
LSA (1 ms dwell, $T_{\text{peak}} = 430^\circ\text{C}$, air)	73.5 ± 1.7	-3.4 ± 0.4	2300
LSA (1 ms dwell, $T_{\text{peak}} = 455^\circ\text{C}$, air)	20.5 ± 1.2	-19.0 ± 1.3	1320

5-4 Processing window of LSA IGZO TFTs:

To quantify the process window, Figure 5-4(a) shows the saturation mobilities and (b) turn-on voltages of LSA annealed TFTs as a function of peak temperature. High mobilities are observed only in a narrow processing window near 430°C. Beyond $\pm 25^\circ\text{C}$, the mobility returns to essentially the same as for as-deposited samples. The turn-on voltage shows similar behavior reaching ~ -3.5 V at the optimum temperature, but dropping rapidly for temperatures both above

and below 430°C. There is also some evidence of an increase in mobility for annealing at temperatures near 325°C, but devices behavior in this regime was highly inconsistent and the parameter space was not extensively explored due to the variations.

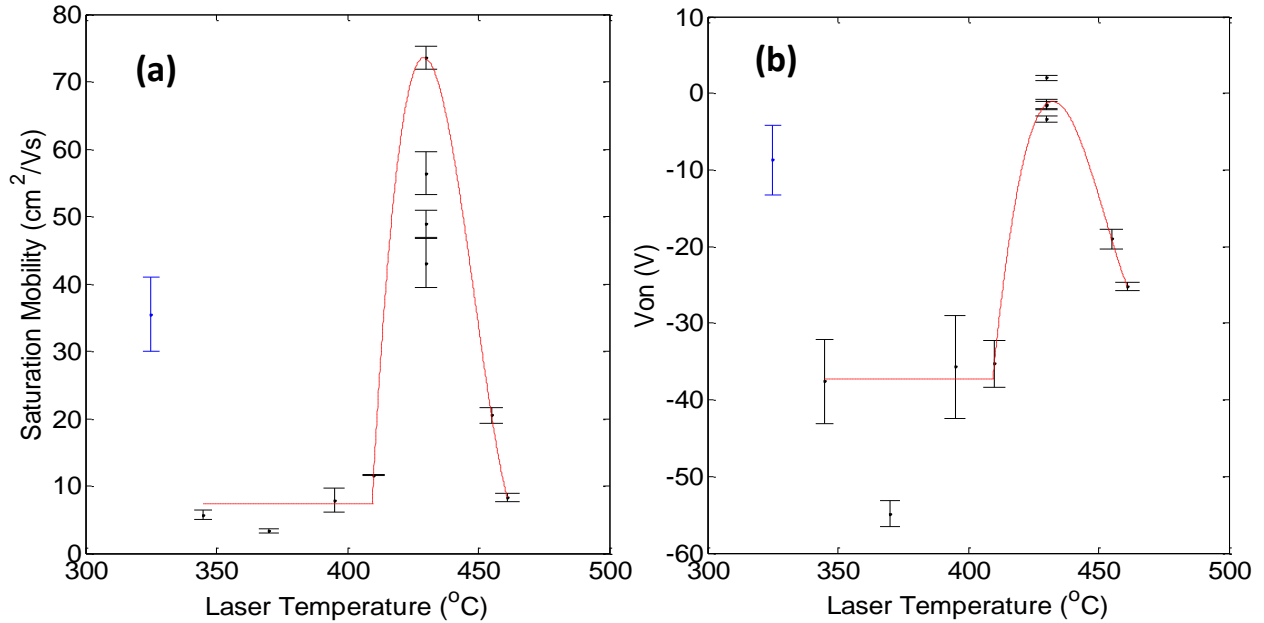


Figure 5-4. (a) Saturation mobilities and (b) turn-on voltages as a function of peak temperature during a 1 ms laser anneal. Error bars are the standard deviation of devices processed in the same run.

5-5 Stability of LSA IGZO TFTs

To determine the stability of the metastable LSA induced state, samples were subsequently furnace annealed at 350°C. Figure 5-5 shows transfer curves for devices post-annealed by LSA alone, furnace alone, and by LSA followed by furnace. The characteristics of LSA + furnace

annealed sample closely resemble those that were only furnace-annealed. From an LSA only mobility of $73 \text{ cm}^2/\text{Vs}$, the mobility and V_{on} for the LSA + furnace conditions were reduced to $15.0 \pm 0.6 \text{ cm}^2/\text{Vs}$ and $10.5 \pm 0.1 \text{ V}$, respectively. This is essentially equal to the characteristic of furnace-annealed only samples with a mobility and V_{on} of $16.3 \pm 0.7 \text{ cm}^2/\text{Vs}$ and $10.0 \pm 0.1 \text{ V}$, respectively. This suggests that any subsequent furnace annealing effectively erased the metastable LSA structure.

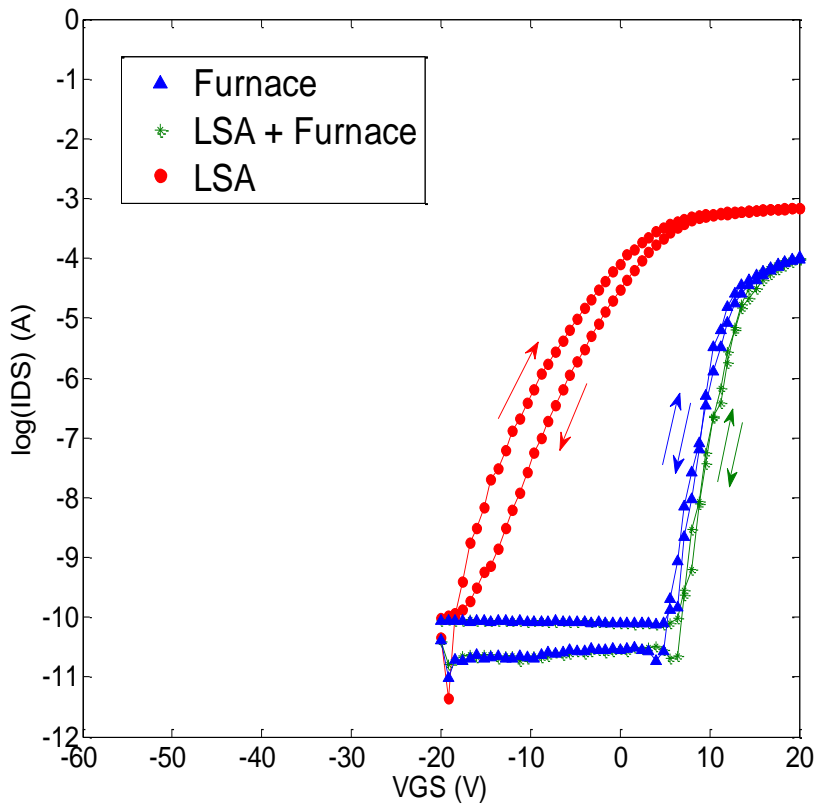


Figure 5-5. Transfer curve ($V_{DS} = 10\text{V}$) of TFTs furnace annealed, LSA annealed and, furnace-annealed after LSA annealing. The subsequent thermal anneal removes the metastable state induced by LSA.

5-6 Long channel LSA IGZO TFTs measured at elevated temperatures:

Contact resistance contribute significantly to the overall channel resistance in the $W/L = 200/50$ devices. To remove this contact resistance effect, we fabricated high mobility a-IGZO TFTs with long channel devices ($W/L = 20/50$) where the channel resistance dominates. The optimized LSA peak temperature for high mobility IGZO TFTs was 400°C (20.6 W, 1 ms). Temperature dependent electrical measurements were performed on these a-IGZO TFTs with probe station temperatures of 25, 40, 50, 60, 70 and 80°C . Prior to each measurement, TFTs were allowed to equilibrate for 10 min on the heated chuck. Figure 5-6 shows transfer curves for furnace and LSA samples measured at various probe station chuck temperatures.

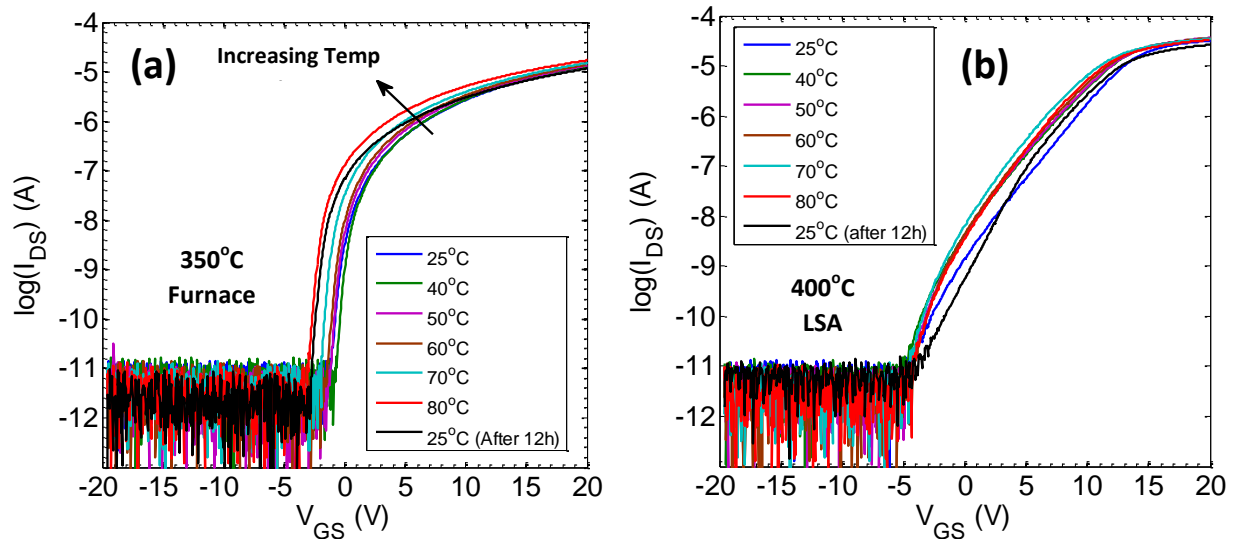


Figure 5-6. Transfer curves for various probe station chuck temperatures ($V_{DS} = 10\text{V}$) of a-IGZO TFTs annealed by (a) furnace and (b) LSA ($T_{peak} = 400^{\circ}\text{C}$, 1ms).

In Fig. 5-6 (a), V_{on} shifts negatively and on current increases for furnace annealed TFTs with increasing chuck temperatures. There is an element of further annealing even at these low temperatures. V_{on} shifts negatively with the chuck temperature but retains the shift as the sample returns to room temperature. Measured 12 hours later, the V_{on} had permanently shifted by 1-2 V. However, the mobility was only slightly degraded ($< 0.3 \text{ cm}^2/\text{Vs}$).

Figure 5-6 (b) shows similar curves for an LSA annealed sample. In contrast to the furnace sample, V_{on} shifts initially at 40°C but then remains constant to the highest temperature. After 12 hours, the V_{on} at 25°C is essentially the same as before chuck heating.

Figure 5-7 shows the output curves of LSA a-IGZO TFTs measured at increasing temperatures from 25 to 80°C , while Fig. 5-8 shows output curves as the sample is cooled from 80 to 25°C .

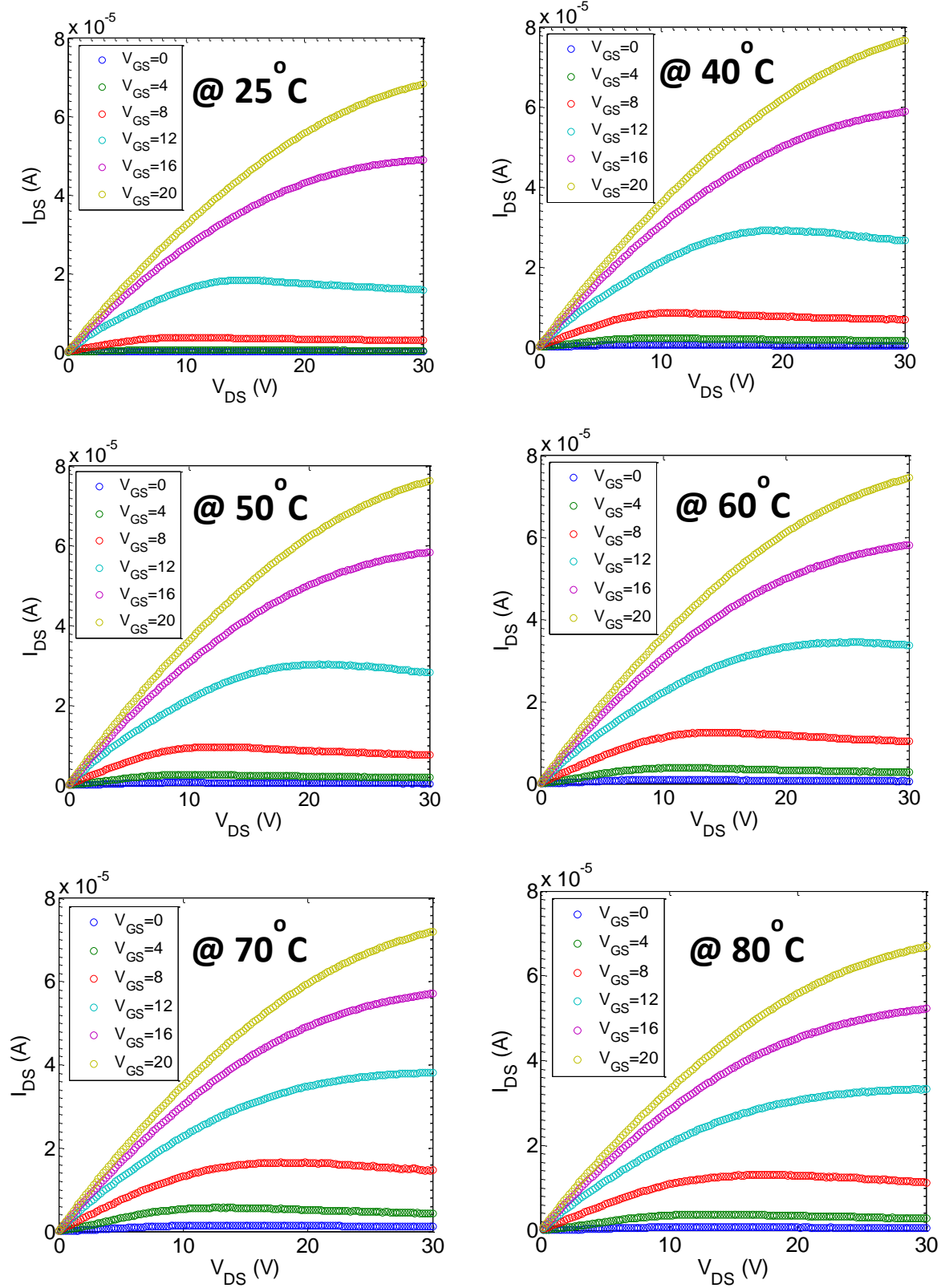


Figure 5-7. Output curves of LSA ($T_{peak} = 400^{\circ}\text{C}$, 1ms) a-IGZO TFTs measured at various probe station chuck temperatures (heated up from 25 to 80°C).

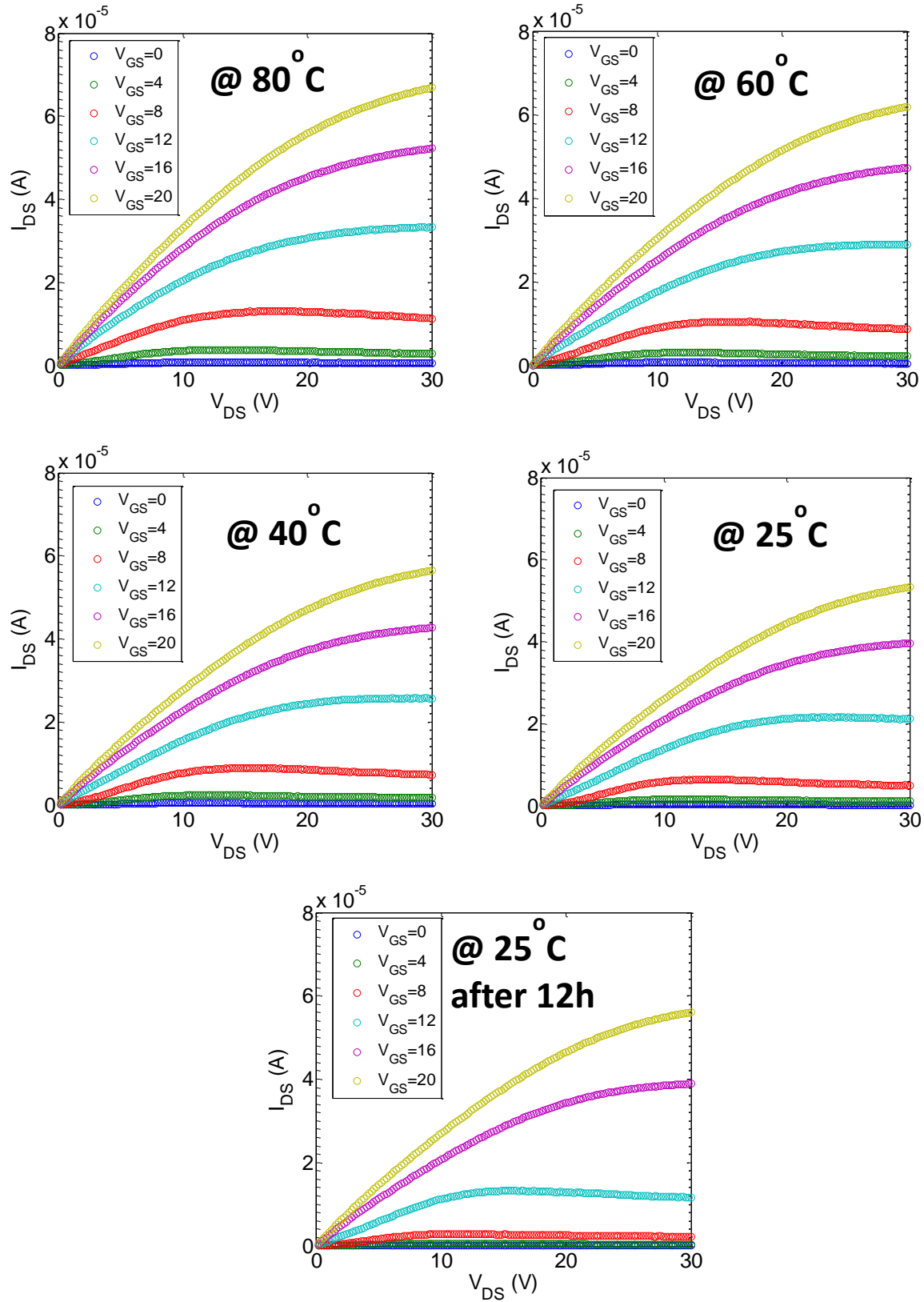


Figure 5-8. Output curves of LSA ($T_{peak} = 400^{\circ}\text{C}$, 1ms) a-IGZO TFTs measured at various probe station chuck temperatures (cooled down from 80 to 25°C).

Figure 5-9 summarizes the temperature dependent (a,c) saturation mobility and (b,d) turn-on voltage of TFTs annealed by furnace and by LSA. For furnace annealed TFTs, the mobility increases with increasing temperature and follows the same trend as the sample cools over the 55°C range. The mobility change is ~20% with the increase likely arising from enhanced transport over the potential energy surface. In general, the mobility is also observed to increase with carrier density; at high temperatures, the carrier density would also be increased [102]. In contrast, V_{on} shifts negatively with increasing temperature with the change becoming permanent as the temperature is reduced back to 25°C. After 12 hours, V_{on} retains this new lower value.

On the other hand, the mobility of LSA TFTs stayed relatively constant below 50°C, decreasing significant for temperatures above 60°C. Cooling back to 25°C, the mobility of these TFTs did not recover even after 12 hours. This suggests some annealing behavior even at these low temperatures. The metastable state of LSA annealed TFTs is very tenuous and relaxation toward the equilibrium structure can occur even at 50°C.

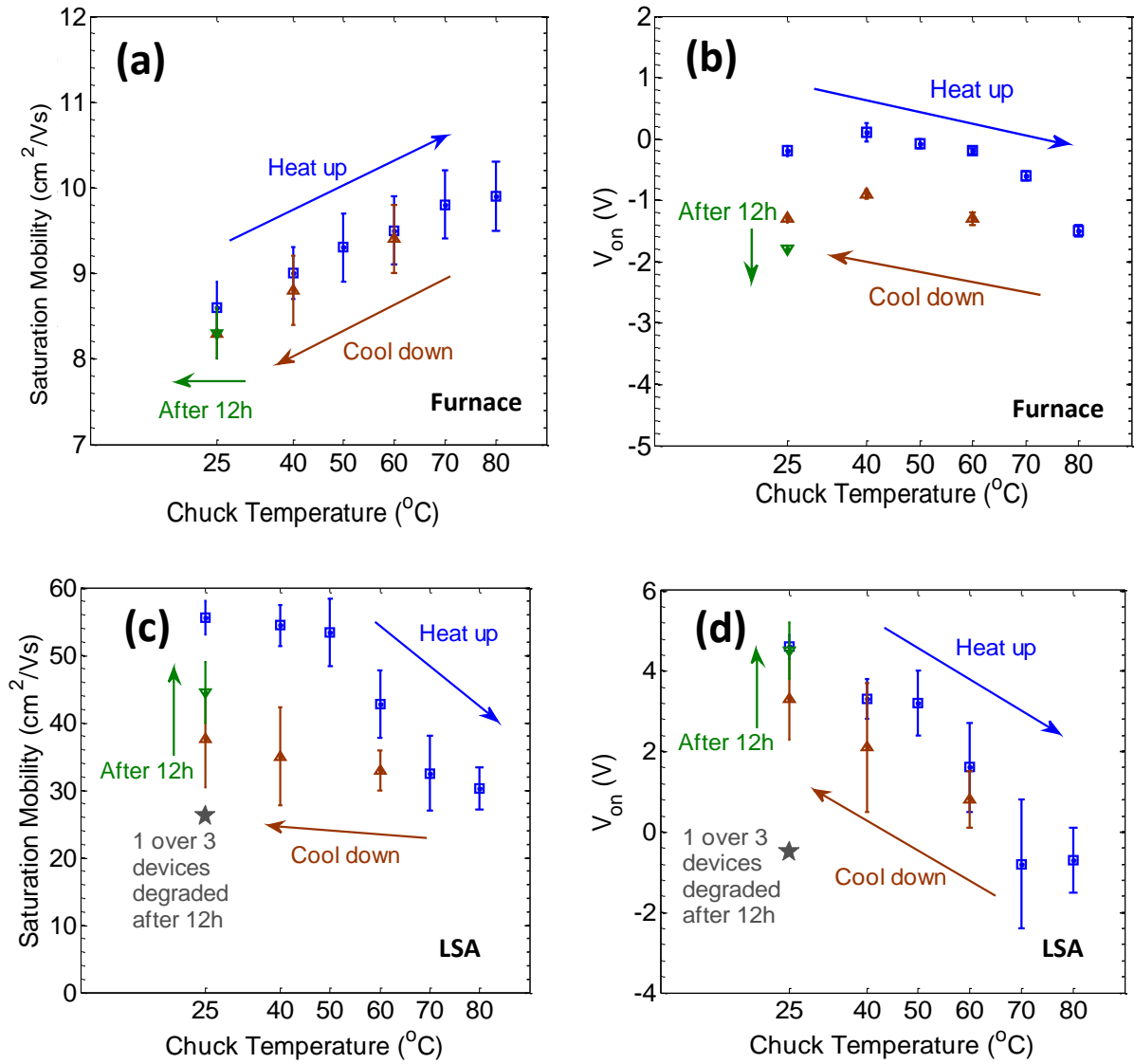


Figure 5-9. (a) Mobility and (b) V_{on} of Furnace annealed a-IGZO TFTs and (c) Mobility and (d) V_{on} of LSA a-IGZO TFTs measured at probe station chuck temperature heated up from 25 to 80°C followed by cooling down back to 25°C.

Figure 5-10 shows an Arrhenius plot of the source-drain current at $V_{\text{DS}} = 0.5 \text{ V}$ as a function of $1/kT$. Curves are shown for various gate voltages from essentially the noise floor. Figure 5-10 (a) shows furnace TFTs with LSA annealed TFTs shown in Fig. 5-10 (b). At $V_{\text{GS}} \gg V_{\text{on}}$

(strong accumulation), the Fermi level will be above the CBM and I_{DS} is nearly independent of temperature. As V_{GS} approaches and falls below V_{on} , the current becomes sensitive to the density of traps near the CBM, ultimately reflecting the sub-threshold slope behaviour. Unfortunately, these data are complicated by the changing V_{on} with temperature and lines at constant $V_{GS} - V_{on}$ cannot be generated easily.

However, we note a significant difference in the trends for the furnace and LSA annealed TFTs. For furnace annealed TFTs at low V_{GS} , the I_{DS} increases rapidly with temperature, while LSA TFTs remain relatively independent of temperature. This may indicate that there are more trap states near the CBM of LSA TFTs than in furnace annealed TFTs, consistent with a large subthreshold slope.

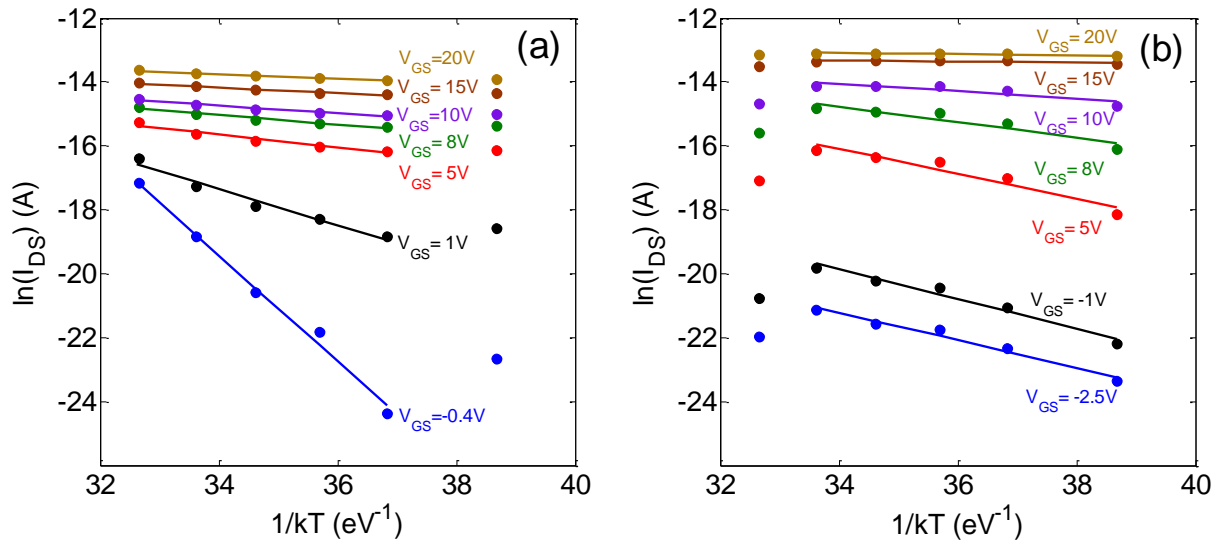


Figure 5-10. $\ln(I_{DS})$ v.s. $1/kT$ @ $V_{DS} = 0.5$ V of *a*-IGZO TFTs annealed by (a) furnace and (b) LSA. T is the probe station chuck temperature.

5-7 Long term stability of LSA IGZO TFTs:

To understand the stability of LSA a-IGZO TFTs, devices were stored at room temperature and on a hot plate at 50°C in normal room air but in a dark ambient and electrically measured periodically over 17 days. The devices behavior at 50°C was similar to that at room temperature, except that the changes occurred more rapidly over the first 2-3 days. Fig. 5-11 shows transfer curves ($V_{DS} = 10V$) of TFTs stored at (a) room temperature and (b) at 50°C. For both, the on current decreased and V_{on} shifted negatively during storage. At room temperature, the devices slowly shifted for the first 8 days before reaching a steady state condition.

Fig. 5-12 and Fig. 5-13 show the output curves after 0, 5 and 10 days, respectively. In Fig. 5-12 (stored at room temperature), TFTs after 0 and 5 days continued to show the expected quadratic increase in $I_{DS,sat}$ as a function of V_{GS} . However, by 10 days, the currents show a nearly linear increase. The peak $I_{DS,sat}$ dropped to half after 5 days with a slight further drop after 10 days. V_{on} initially shifts before positive shifting negatively after 10 days. On the other hand, when stored at 50°C, the output curves transitioned to a linear increase in $I_{DS,sat}$ with V_{GS} after only 5 days. This suggests that elevated storage temperatures (50°C), requires less time to reach the ultimate equilibrium state.

Figure 5-14 summarize the mobilities and turn-on voltages of these TFTs as a function of time. At 50°C, the mobility decayed to $\sim 10 \text{ cm}^2/Vs$ at 50°C after 3 days, while it took 7 days when stored at room temperature. V_{on} in both cases shifted negatively, again within 2-3 days at 50°C but requiring ~ 7 days at room temperature. All mobilities and V_{on} shifted closer to the as-deposited values during this decay, suggesting samples reverted to the original state that existed before the LSA treatment.

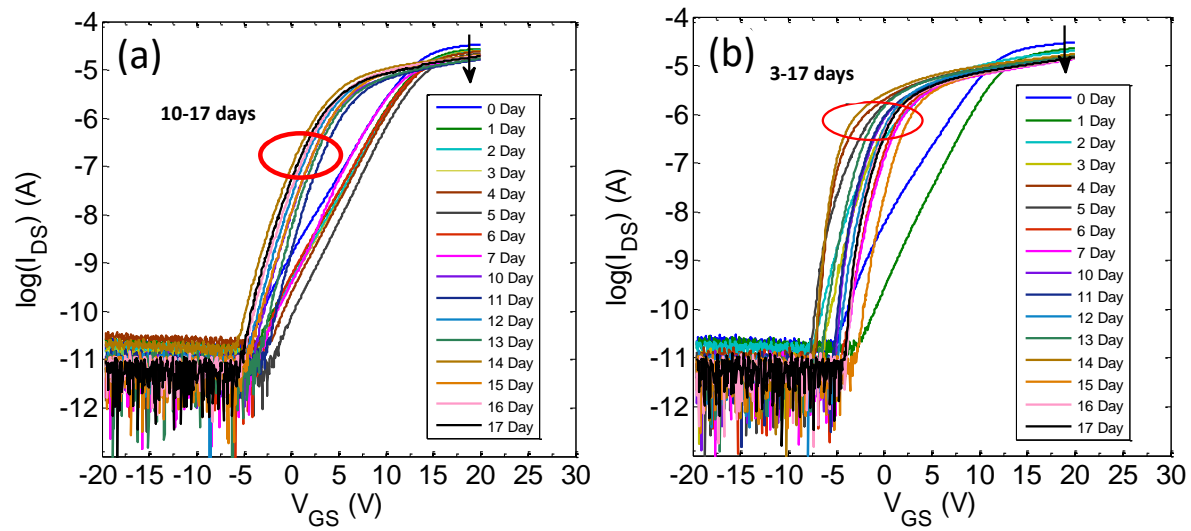


Figure 5-11. Transfer curves ($V_{DS} = 10V$) of LSA a-IGZO TFTs stored in dark at (a) room temperature and (b) $50^{\circ}C$.

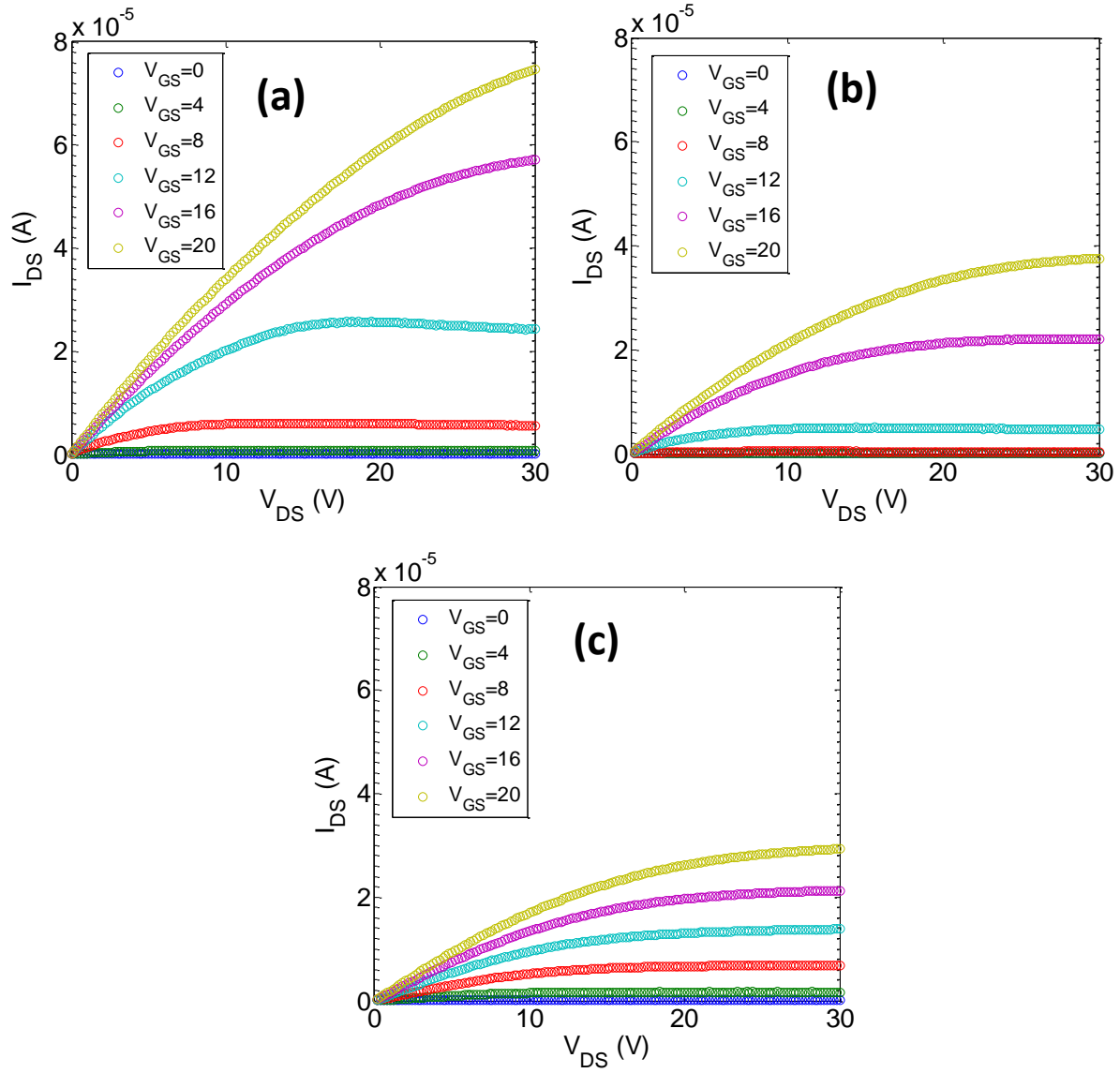


Figure 5-12. Output curves of LSA a-IGZO TFTs stored at room temperature after (a) 0, (b) 5 and (c) 10 days.

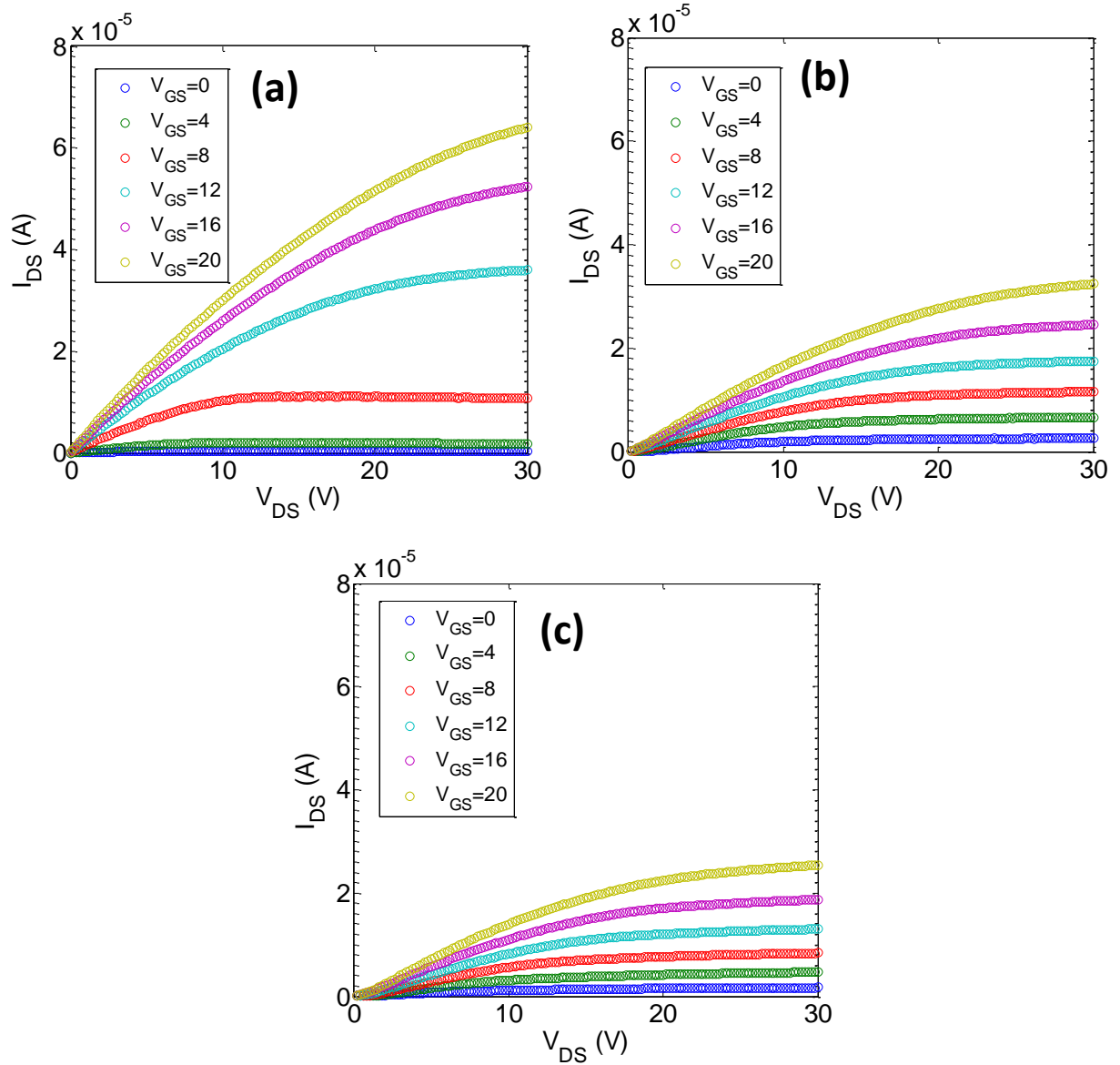


Figure 5-13. Output curves of LSA a-IGZO TFTs stored at 50°C after (a) 0, (b) 5 and (c) 10 days.

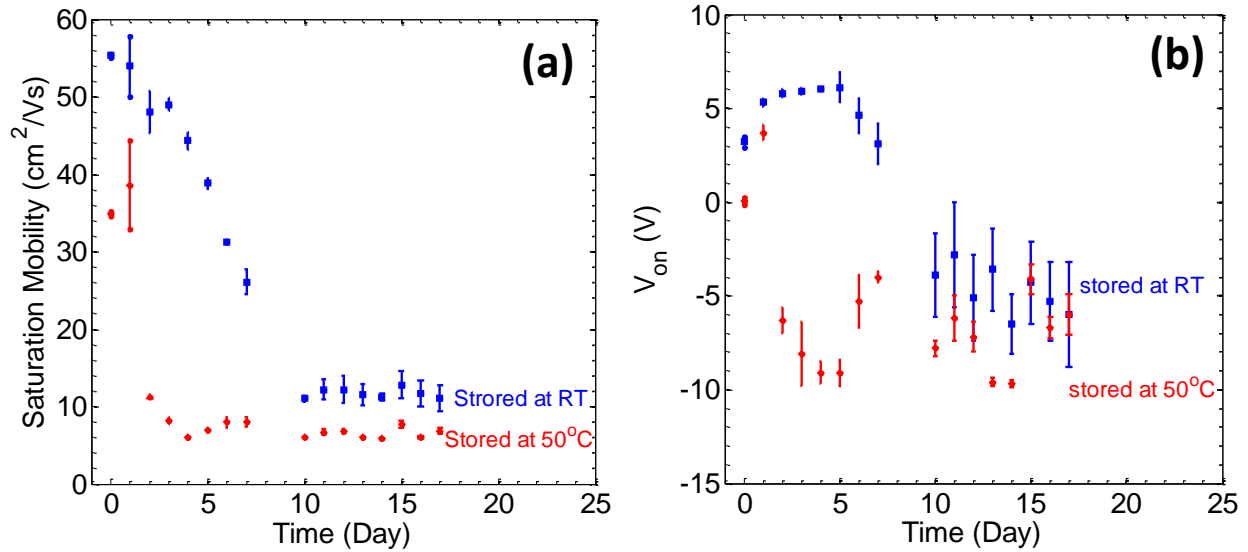


Figure 5-14. (a) Mobility and (b) V_{on} of LSA a-IGZO TFTs stored at room temperature and 50°C from first day to 17 days. (Standard deviation based on 2 devices)

5-8 Estimation of activation energy for mobility decay:

Although we have only two temperatures, we can make an estimate for the activation energy of the mobility decay processes. Figure 5-15 shows $\frac{\mu}{\mu_0}$ as a function of time, where μ_0 is the mobility immediately after the LSA anneal. The decay constant (τ) is extracted using the equation of $\mu = \mu_0 \times \exp\left(\frac{-t}{\tau}\right)$. The decay constant and the corresponding fit for each TFT are shown in Fig. 5-15. Longer decay constants corresponds to more stable device, with devices stored at room temperature shown time constants approximately 5 times longer than those stored at 50°C.

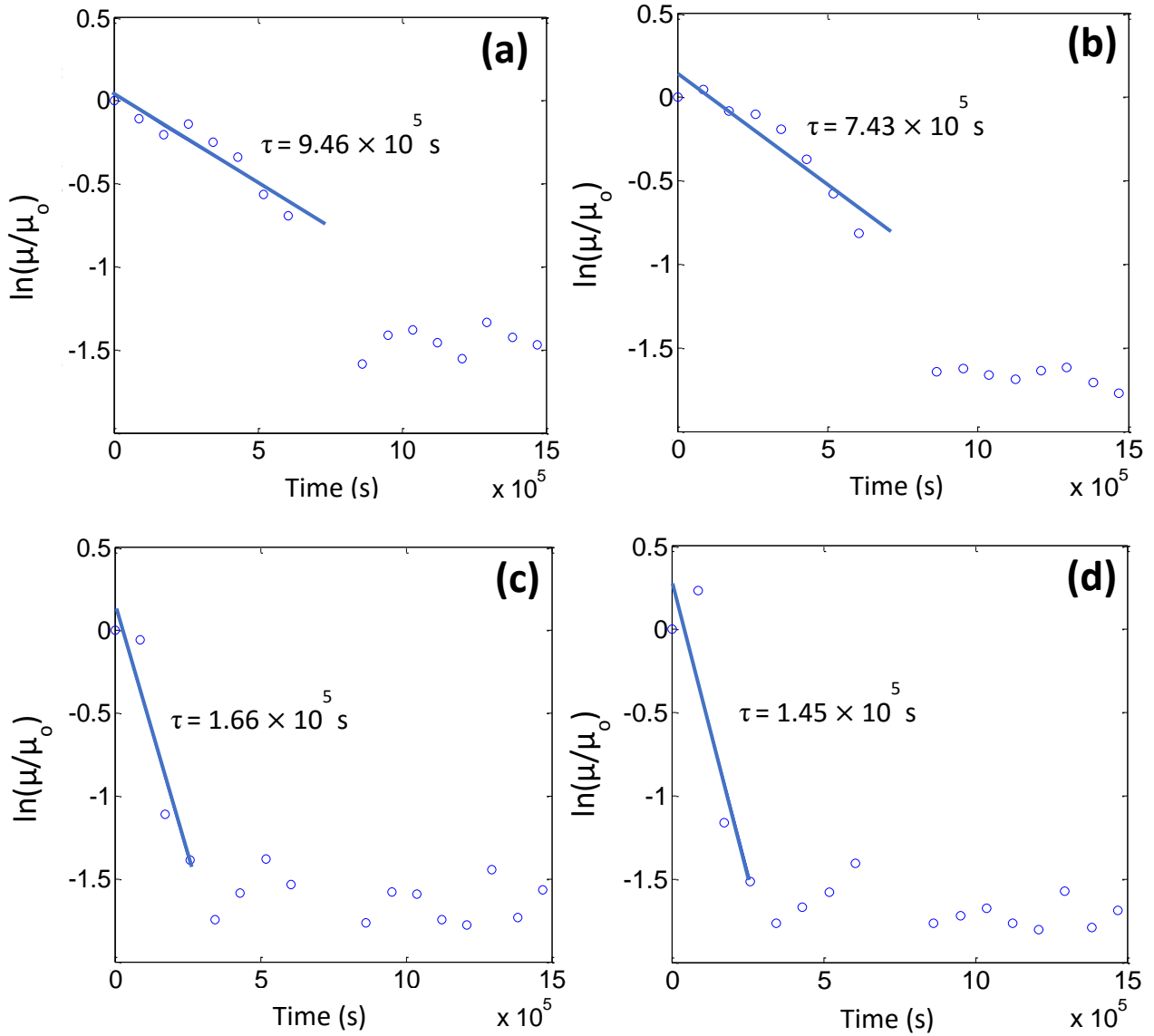


Figure 5-15. Plot of the log of the mobility as a function of time for two LSA a-IGZO TFTs stored at (a, b) room temperature and another two devices (c, d) at 50°C. μ_0 is the initial mobility measured immediately after the LSA treatment.

To estimate the activation energy of this decay constant, we plotted $\ln(\tau)$ as a function of $1/kT$, where k is Boltzmann constant. Data were fit to an Arrhenius form $\tau = \tau_0 \times \exp\left(\frac{E_A}{kT}\right)$ where

E_A is the activation energy. These data are shown in Fig. 5-16. Although there are only two points, the estimated activation energy is 0.6 ± 0.1 eV.

This value (0.6 eV) is comparable to activation energies for hydrogen and deuterium diffusion in a-IGZO (0.11 eV and 0.89 eV) determined by Nomura et al. [76]. Their measurements were for the out-migration of hydrogen and in-migration of deuterium to a-IGZO film (2:2:1 oxide ratio) below 200°C, measured during exchange with deuterium in a reducing environment (5% D₂/95% N₂). The current measurements are for changes which may occur as direct diffusion of hydrogen with no replacement in an oxidizing environment (ambient air). These data suggests that the decay for high mobility LSA a-IGZO TFTs may be related to hydrogen diffusion in a-IGZO, especially since local movement of hydrogen involves bond –OH groups in the structure.

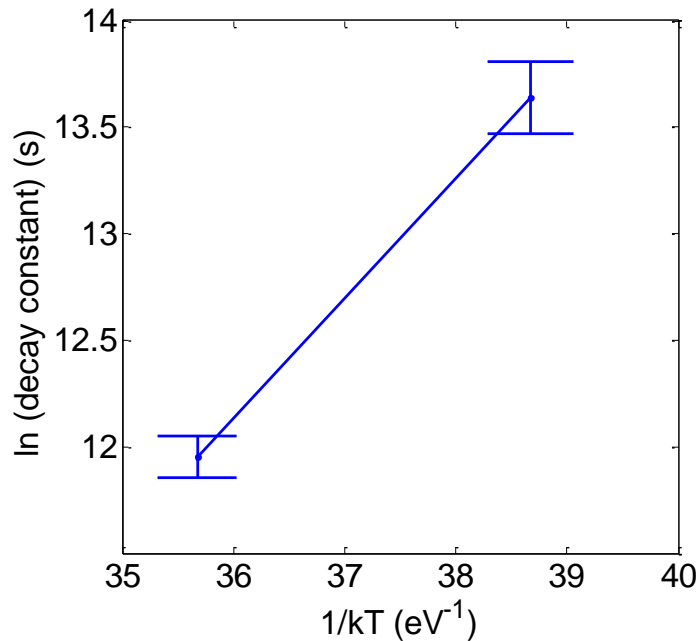


Figure 5-16. Arrhenius plot of the decay time constant with inverse temperature for devices stored at room temperature and at 50°C. The activation energy is approximately 0.6 ± 0.1 eV.

5-9 Role of water vapor on LSA annealed TFTs:

Given the high mobility, it was critical to demonstrate the consistency through multiple process runs. Prior to fall 2015, the LSA annealed films were reproducible with mobilities of 50 – 70 cm^2/Vs . However, after October 2015, we could not reproduce the ultra-high mobility IGZO TFTs after we opened the seal of the main chamber. We tried LSA anneals from 370 to 490°C in 20°C interval but the mobilities were $\sim 10 \text{ cm}^2/\text{Vs}$ with a very negative V_{on} ($\sim -30 \text{ V}$). After October 2015, the oxygen plasma still does produce metallic films with V_{on} of $\sim -30 \text{ V}$. We hypothesized that H_2O (source of hydrogen doping) was critical for LSA devices. To examine the effect of hydrogen on the performance of LSA a-IGZO TFTs, we compared device fabricated on IGZO films sputtered in an ambient with no water vapor to those sputtered in an ambient with 0.5% H_2O ($P_{\text{H}_2\text{O}} \sim 4.5 \text{ Torr}$ in the Ar). Fig. 5-17 shows the set up for IGZO sputter deposition (a) with and (b) without $P_{\text{H}_2\text{O}}$. A thermal bath for the DI water permitted the dew point of the saturated Ar to be 0°C ($P_{\text{H}_2\text{O}} = 4.5 \text{ Torr}$ in the Ar). With no intentional H_2O , the water vapor concentration in the O_2 and Ar gas line are $\sim 1 \text{ ppm}$.

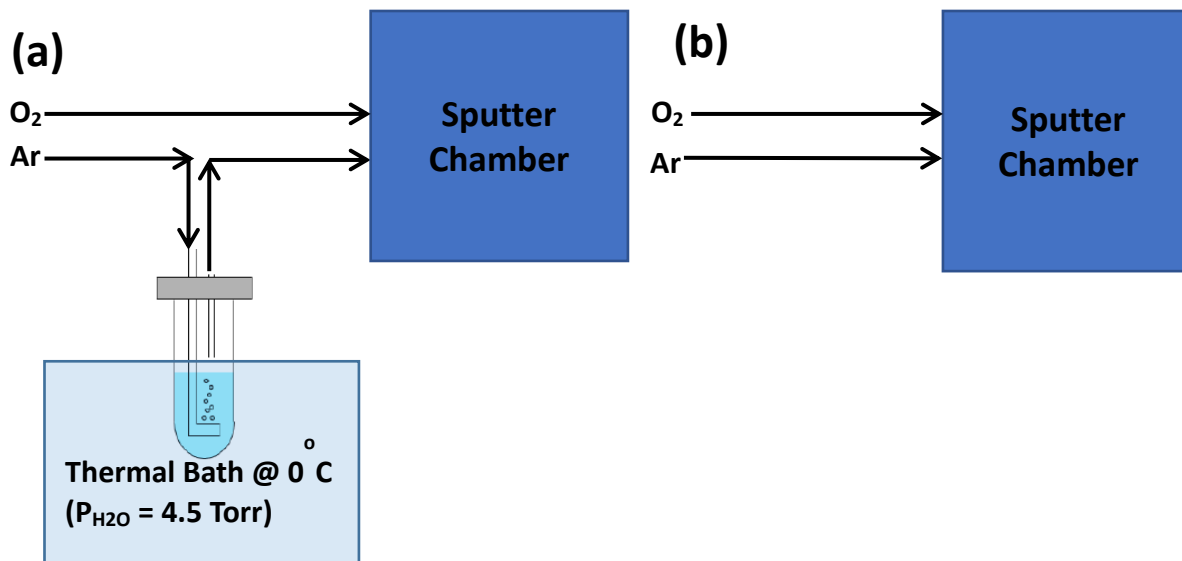


Figure 5-17. Sputter deposition set up (a) with and (b) without water vapor with dilution, the water vapor concentration is approximately 0.5%.

Figure 5-18 shows transfer curves ($V_{DS} = 10V$) of as-deposited a-IGZO TFTs with and without water vapor during IGZO deposition. For the TFTs deposited with water vapor, the dominant effect is a positive shift of V_{on} (toward zero), an increase in the sub-threshold slope, and a slight increase in the hysteresis. Table 5 summarizes the mobility and turn-on voltages of the TFTs shown in Fig. 5-19. Mobilities of TFTs deposited with water vapor were slightly higher than those deposited under dry condition. One possible explanation for these data is that hydrogen passivates the oxygen vacancies and suppresses the electron carrier density. This would explain the V_{on} shift while passivation of dangling bonds in the a-IGZO would explain the enhanced mobility.

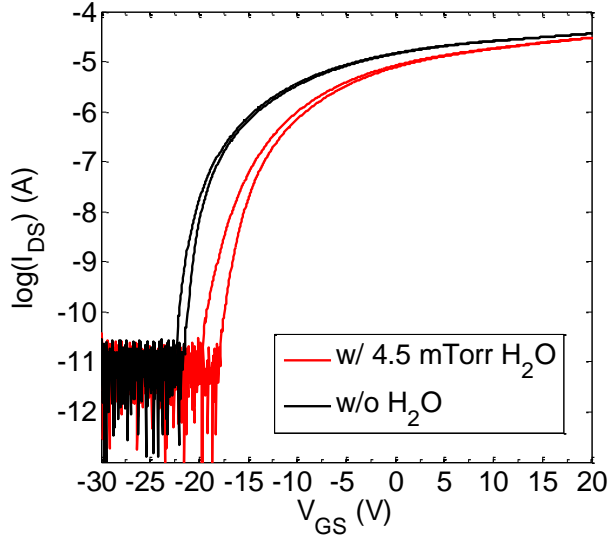


Figure 5-18. Transfer curves ($V_{DS} = 10V$) of as-deposited a-IGZO TFTs with and without 0.5% water vapor during IGZO deposition.

Table 5. Saturation mobilities and turn-on voltages of as-deposited a-IGZO TFTs with and without 4.5 Torr P_{H_2O} during IGZO deposition.

	μ_{sat} (cm^2/Vs)	V_{on} (V)	S.S (mV/dec)
w/ H_2O	8.4 ± 0.0	-14.2 ± 0.3	940 ± 54
w/o H_2O	7.9 ± 0.0	-18.7 ± 0.0	743 ± 36

Figure 5-19 shows transfer curves ($V_{DS} = 10V$) of LSA annealed TFTs (a) without and (b) with water vapor during IGZO deposition. All of the saturation mobilities of curves shown in Fig. 5-19 are ~ 10 cm^2/Vs but V_{on} of TFTs deposited with water vapor have a narrower distribution compared to the TFTs deposited without water vapor. However, no conditions were found to reproduce the high mobility IGZO TFT.

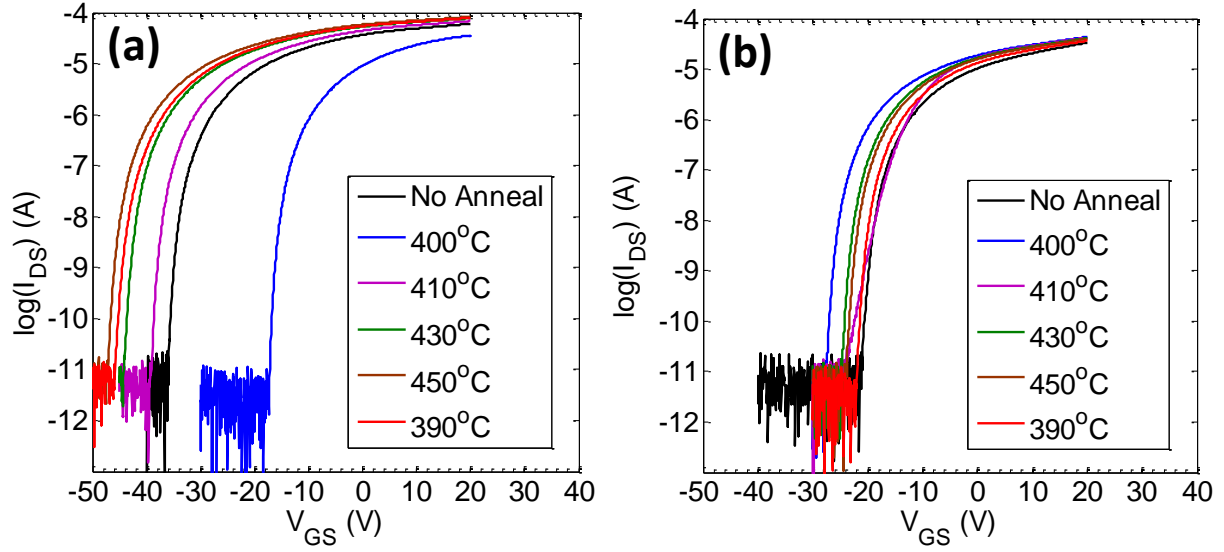


Figure 5-19. Transfer curves ($V_{DS} = 10V$) of LSA a-IGZO TFTs (a) without and (b) with 0.5% water vapor during IGZO deposition after LSA annealing at various peak temperatures.

For possible following work, Table 6 compares the process and performance of LSA and furnace annealed (weekly test device) TFTs.

Table 6. Process and performance comparison of LSA and furnace annealed IGZO TFTs.

Process steps	LSA TFT	Furnace annealed TFT (weekly device)
Moisture trap	Without (bypass)	With
Pre-clean	100 min O ₂ plasma (10 sccm O ₂ at 40W). Substrate at RT	600°C (set point) substrate heating for 20min followed by 10 min O ₂ plasma (10 sccm O ₂ at 40W) while chuck cooling
Load sample	Load substrate sample through load lock	
Pre-sputter	<ol style="list-style-type: none"> 1. Substrate temperature set at 260°C (Set T at 350°C) 2. Pre-sputter at Ar/O₂ = 9:1 sccm, 120 W, 5 min 	
IGZO deposition	Open target shutter and deposit for 15min	
Substrate cooling	Set temperature cool from 350 to 200°C (10min) (Chamber pressure at $\sim 10^{-7}$ Torr)	
Unload sample	Unload the sample to load lock and take out immediately	
Post-deposition annealing	LSA at 430°C for 1ms	Furnace at 350°C for 30min in dry air
Electrical Performance		
As-deposited	$\mu_{\text{sat}} = \sim 10 \text{ cm}^2/\text{Vs}$, $V_{\text{on}} = \sim -30\text{V}$	$\mu_{\text{sat}} = \sim 10 \text{ cm}^2/\text{Vs}$, $V_{\text{on}} = \sim 0\text{V}$
LSA at 430°C for 1ms	$\mu_{\text{sat}} = >50 \text{ cm}^2/\text{Vs}$, $V_{\text{on}} = \sim -3\text{V}$	$\mu_{\text{sat}} = \sim 15 \text{ cm}^2/\text{Vs}$, $V_{\text{on}} = \sim 0\text{V}$
Furnace at 350°C for 30min in dry air	$\mu_{\text{sat}} = \sim 15 \text{ cm}^2/\text{Vs}$, $V_{\text{on}} = \sim 0\text{V}$	$\mu_{\text{sat}} = \sim 15 \text{ cm}^2/\text{Vs}$, $V_{\text{on}} = \sim 0\text{V}$

5-10 Trap-free electron transport environment of LSA IGZO TFTs:

The limited mobility of IGZO is thought to arise from shallow traps that lead to a “bumpy” energy landscape as proposed by Nomura et al [1], with both trap and percolation-limited conduction through the energy valleys. In Hosono’s trap limited mobility model [1], the observed field-effect mobility is degraded by the presence of these unoccupied states near the conduction band minimum. They suggested a form $\mu_{FE} = \mu_o \times \frac{N_{GS} - N_T}{N_{GS}}$ where μ_o is the intrinsic drift mobility, N_T is the unoccupied subgap density of states, and N_{GS} is the electron density induced by V_{GS} . This model suggests that LSA has dramatically reduced the density of trap states leading to an observed value closer to μ_o . Indeed, the observed mobility of $75 \text{ cm}^2/\text{V-s}$ is now a lower limit of μ_o . Alternately, Kamiya and Hosono et. al. suggested a mobility model to fit the temperature dependence of the mobility: $\mu_{obs} = \mu_o \times \exp\left(-e \frac{\Phi_o - e\sigma_\phi^2/2kT}{kT}\right)$ where Φ_o and σ_ϕ are the average height and distribution width of the potential barriers, respectively [103]. Using values of $\Phi_o = 60 \text{ meV}$ and $\sigma_\phi = 15 \text{ meV}$ given by Kamiya and Hosono, and a typical mobility of $8 \text{ cm}^2/\text{Vs}$ for their devices, the estimated value of μ_o is $\sim 70 \text{ cm}^2/\text{Vs}$. This is consistent with the limiting mobility of $75 \text{ cm}^2/\text{Vs}$ observed in this work.

5-11 Model for trap-free transport: Role of oxygen vacancy free volume

There are two possible paths for this near trap-free transport environment. The first one associated with the free volume of oxygen vacancies. Kamiya and Hosono et al.[86] proposed a detailed model for oxygen vacancies in IGZO, postulating the formation of a variety of shallow

donor and deep trap states (see chapter 4 discussion). They suggested that the nature of the oxygen vacancy depends critically on the local environment, specifically the open space (free volume) in the vicinity. Oxygen vacancies in an open environment (large free volume) are associated with deep level trap states while more restricted environments (small free volume) lead to shallow donor states. Thermal annealing can impact both the density of the oxygen vacancies, as well as the distribution of vacancies among the various donors and trap configurations.

Partial O₂ pressure jump experiments have shown that furnace annealing provides sufficient time for significant equilibrium changes in the total density of oxygen vacancies through exchange of oxygen with the annealing ambient [87]. In contrast, LSA timescales are sufficiently short that minimal compositional changes are expected despite the higher temperatures. Furnace annealing also provides sufficient time for structural relaxation and densification of the films, changes which again are unlikely to occur on the LSA annealing time frame. Based on XRD measurements, the average interatomic spacing after furnace annealing is approximately 2.8% less than that of the LSA annealed samples (peak shift from 31° to 32°), corresponding to an 8.5% volume compaction. Consequently, oxygen vacancies following LSA annealing have substantially more free volume compared to furnace-annealed films. Oxygen vacancies under LSA annealing have the freedom to shift their configuration from donor-like or shallow trap states to deeper trap state configurations due to the significant presence of additional free volume. As deeper states, they minimally influence the conduction band edge energy surface allowing devices to exhibit mobilities near the intrinsic drift mobility limit. However, this model cannot explain all the observed data including the narrow processing window and the mobility decay with time.

5-12 Model of trap-free transport: Role of hydrogen

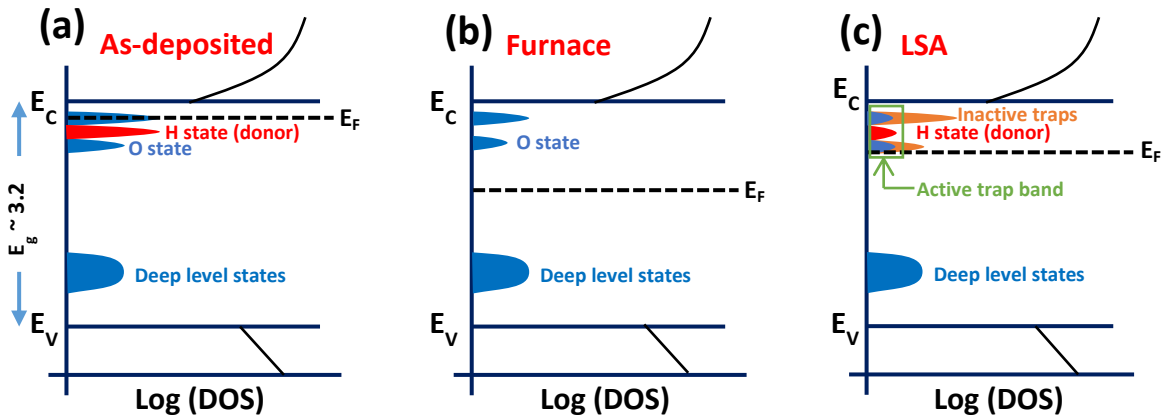


Figure 5-20. Possible energy band diagrams of IGZO TFT (a) as-deposited and post-deposition annealed by (b) furnace and (c) LSA.

The second potential path for this near trap-free transport environment is associated with hydrogen. Although the mobility of LSA a-IGZO TFTs is high, the subthreshold slope is also high compared to furnace annealed TFTs. This suggests that there is a significant trap band below the CBM in the LSA IGZO energy band diagram, as shown schematically in Fig. 5-20 (c). Figure 5-20 shows the possible energy band diagrams of IGZO (a) as-deposited, (b) post-deposition annealed by furnace and (c) by LSA. For as-deposited TFTs (Fig. 5-20 (a)), V_{on} is very negative (~ -20 V) indicating a high concentration of carriers (high Fermi level). These carriers arise from both oxygen vacancy donors and hydrogen donors existing as shallow states

near the CBM. For furnace annealed TFTs (Fig. 5-20 (b)), V_{on} is positive indicating a dramatic reduction in the donor concentration and a Fermi level well below the CBM under no bias conditions. During furnace annealing, we believe that there is both annealing of the oxygen vacancy states and also loss of hydrogen donors to the ambient. In contrast, V_{on} for LSA annealed devices remains near -3V indicating that the Fermi level is closer to the CBM but not as high as the as-deposited state (Fig. 5-20 (c)). The window for this near zero V_{on} is small. Under the optimized LSA condition, we suggest that hydrogen becomes mobile and passivates dangling bonds at oxygen vacancies, effectively neutralizing the oxygen vacancy induced trap states. This would lead to near trap-free transport of carriers as observed. If the LSA temperature is too low, hydrogen does not have sufficient mobility to move and neutralize these dangling bonds. On the other hand, if the LSA temperature is too high, hydrogen likely becomes highly mobile and is not “trapped” at the oxygen vacancies. During the rapid quench, the hydrogen remains randomly interstitial leading to the observed high carrier density above 430°C. Even under optimized conditions, at the oxygen vacancies, not all of the dangling bonds are neutralized leaving a reduced concentration of trap states near the CBM. These form an active trap band that readily pins the Fermi level as it move toward CBM with increasing V_{GS} , causing the high subthreshold slope. However, once the Fermi level moves above the trap band, the electrons transport in a near trap free environment, leading to the observed ultra-high mobility. We believe the role of hydrogen passivation is the main cause of this high mobility with the change of free volume of oxygen vacancy is playing a minor role.

5-13 Stability and decay mechanism of LSA IGZO TFT:

This model is also consistent with the observed mobility decay with time. The high mobility of LSA annealed TFTs is unstable and decays back to essentially the furnace annealed state over an ~10 days period. The activation energy for this decay is on the order of 0.6 eV, consistent with our suggestion that diffusion of hydrogen is key in the process. Other measurements of diffusion in IGZO give similar activation energies for hydrogen (0.11 eV) and deuterium (0.89 eV) by Nomura et al.[76]. LSA annealing leads to hydrogen passivation of miscoordinated cation (oxygen vacancy) neutralizing the trap state. Over time (days), hydrogen diffuses out leaving the oxygen vacancy traps active again. Hydrogen diffusion may also relax the IGZO structure leading back to the equilibrium state (furnace annealed TFT). As traps shift from inactive to active, the mobility of the device decays due to increased scattering near the CBM.

As the LSA induced state is metastable, the mobility decays with time as structural relaxation occurs and the equilibrium between deep traps, shallow traps, and donor shallow states is re-established. This equilibrium would slowly be restored even at room temperature, reminiscent of the “defect pool model” in a-Si:H [104]. Measurements of the mobility decay in unpassivated samples indicates this decay time constant is greater than 10^5 seconds (24 days). Given the relaxation at low temperature and an activation energy near 0.6 eV, we believe that hydrogen is involved as the catalyst allowing bonds to shift into lower energy configurations. Annealing at 350°C in the furnace accelerates relaxation of these trap states, and likely induces densification as the device performance approaches that of furnace annealed films. It would be useful to undertake future experiments to more precisely measure the kinetics of the mobility decay and to link results to atomic models of the structural relaxation.

5-14 Summary

Laser spike annealing (LSA) of IGZO TFTs to 430°C for 1ms is shown to increase the TFT saturation field-effect mobilities to above 70 cm²/Vs ($V_{on} \sim -3V$), over 4 times higher than that of furnace-annealed control (~ 16 cm²/Vs) TFTs. These high mobilities are obtained over a fairly narrow temperature window, which we interpret as an optimized temperature for hydrogen to neutralize the active trap states. The observed mobility of >70 cm²/Vs is now a new lower bound on the trap-free IGZO mobility. The mobility of LSA IGZO TFTs decays from ~ 50 to ~ 10 cm²/Vs over a period of 10 and 3 days when stored at room temperature and 50°C, respectively. The activation energy of this mobility decay is estimated to be ~ 0.6 eV, which is consistent with the activation energy of hydrogen diffusion in a-IGZO, strongly suggesting that hydrogen is involved in the relaxation of laser annealed IGZO devices.

CHAPTER VI

VI. CONCLUSIONS

In this work, we explored the role of processing modifications on the electrical performance of IGZO TFTs with two techniques; dual channel layer device structures and CO₂ LSA post-deposition annealing. Dual layer devices exploiting both c-axis aligned (CAAC) IGZO and amorphous IGZO (a-IGZO) exhibit mobilities up to 20 cm²/Vs, an enhancement of 30% over single layer devices, with potentially greater tolerance for impurities. Similarly, post-annealing of a-IGZO devices with LSA achieved the highest (to date) demonstrated TFT mobility of 75 cm²/Vs.

Controlling impurities and hydrogen diffusion are important in IGZO TFTs. For dual layer TFTs, we fabricated and characterized CAAC/a-IGZO dual-layer devices, with the channel being implemented in the CAAC layer. These TFTs exhibit saturation field-effect mobilities of ~20 cm²/Vs, exceeding that achieved in reference TFTs using either a single layer of CAAC (~13cm²/Vs) or a single layer of amorphous IGZO (~15 cm²/Vs). The a-IGZO layer serves to getter impurities from the nanocrystalline CAAC phase and equilibrate defect concentrations during deposition, leading to a cleaner CAAC channel layer. The highest mobility of 20.6 cm²/Vs was measured in TFTs in which the amorphous layer and CAAC layers were deposited at 260°C and 310°C, respectively. In samples in which the amorphous IGZO layer was deposited at RT, the mobility improved over a period of months from initially 6.7 cm²/Vs to 20.5 cm²/Vs. This observation, and the observation that device-to-device variation in all dual layer devices narrow with times, suggest that equilibrium between the two layers is established at room

temperature in ~ 10 days. A model involving equilibrium between the two layers by the movement of hydrogen which, as it moves, rearranges high stress bonds is consistent with our observations and the published diffusivity of hydrogen in IGZO.

Using CO₂ laser spike annealing (LSA) annealing of a-IGZO TFTs, near trap free electron transport, arising from control of the energy landscape near the CBM, leads to extremely high mobilities. We demonstrated that IGZO TFTs annealed to 430°C for 1ms using LSA increases the TFT saturation field-effect mobility to above 70 cm²/Vs with a V_{on} near -3V. This is over 4 times higher than that of furnace-annealed devices (~ 16 cm²/Vs). Unfortunately, the high mobility of LSA annealed TFTs is unstable and decays back to essentially the furnace annealed state over an ~ 10 days period. The activation energy for this decay is on the order of 0.6 ± 0.1 eV, suggesting again that diffusion of hydrogen is the critical kinetic step in the process. This value (0.6 eV) is consistent with measured activation energies of hydrogen (0.11 eV) and deuterium (0.89 eV) diffusion in a-IGZO from Nomura et al.[76]

We suggest this improvement is a result of hydrogen donors passivating and deactivating the oxygen vacancy induced trap states at the optimized temperature. The observed mobility of >70 cm²/Vs is thus a new lower bound on the trap-free oxide semiconductor mobility.

These LSA induced high mobilities are obtained over a fairly narrow temperature window. As these temperatures were comparable to those at which CAAC IGZO forms, we studied the potential structural changes occurring during LSA using X-ray techniques. Area X-ray diffraction indicated that as-deposited film showed some slight CAAC IGZO characteristics. However, no significant changes were observed even after LSA annealing to 800°C for 1-2 ms. This indicates that the high mobility IGZO TFT behavior under LSA annealing is not related to CAAC texture development. Analysis of amorphous scattering rings also shows no significant

change in d-spacing below 800°C, indicating no significant structural changes. However, CAAC IGZO formation does occur for area-LSA annealed films at 1400°C in 1-2ms. The behavior of LSA annealed films between 800 and 1400°C, forming highly aligned CAAC IGZO, should be prove to an interesting arena for future work.

CHAPTER VII

VII. FUTURE WORKS

7-1 For dual layer IGZO TFTs:

In chapter 3, we demonstrated the high mobility bottom gate dual layer CAAC/amorphous IGZO TFT. Our model explains the improvement as a result of impurity diffusion from the CAAC phase to the amorphous phase leading to a cleaner channel layer. To further verify the model, top and bottom gate dual layer devices should be fabricated and compared. For a bottom gate dual layer device (CAAC/amorphous IGZO), the channel layer is implemented at the CAAC/SiO₂ interface, while for a top gate dual layer device, the channel layer is implemented at the amorphous/SiO₂ interface. The bottom gate dual layer TFTs should exhibit significant improvement over the top gate devices if this model is indeed correct.

7-2 For CAAC/amorphous IGZO transition annealing temperature:

As mentioned earlier, it also would be interesting to evaluate highly aligned CAAC devices, arising from LSA annealing above 800°C. The development of CAAC with temperature above 800°C was not extensively explored with only the ultimate limit at 1400°C measured. The development of the CAAC with annealing temperatures is critical to measure. Equally, understanding the mechanism for CAAC alignment in a post-deposition annealing process is also interesting to explore as CAAC is normally formed via nucleation during sputter deposition. Also, it will be interesting to see the behavior of IGZO devices annealed at 1400°C. With the extremely strong texture, it is likely that devices will exhibit both high mobility and stability.

7-3 Charge distribution for LSA IGZO TFTs:

The model for mobility enhancement under LSA annealing is based on trap redistribution and passivation. These properties should be directly evaluated using advanced CV (capacitance voltage), DLTS (deep level transient spectroscopy), as well as detailed TFT modeling and analysis. Using CV measurement (Metal-Oxide-IGZO device), trap state distributions in the band gap for LSA and furnace annealed IGZO can be obtained by integrating charge density through Poisson equation. It is expected that these measurements would show the LSA induced passivation of oxygen vacancies by hydrogen donors leading to the nearly trap-free electron transport environment as we proposed. Using DLTS (Metal-IGZO device), the defect and trap state characteristics for LSA and furnace annealed IGZO can be measured even more precisely. Understanding the difference between electrostatic charges (from CV) and dynamic charges from TFT properties will be critical to developing a comprehensive model.

7-4 Different laser frequency for LSA IGZO TFTs:

The wavelength of the CO₂ laser (10.6 μm) may be a perfect match to the energy of the hydrogen atoms passivating dangling bond at oxygen vacancy, or to –OH bond breaking for the correlated oxygen vacancies. Laser annealing with other wavelengths would be another interesting topic to consider. For example, the diode laser with a 980 nm wavelength would be a good candidate to verify this hypothesis.

7-5 Advanced electrical characterization for LSA IGZO TFTs:

Conventional semiconductors exhibit a universal mobility curve based on the effective electric field at the interface. Study of the mobility of low effective electric fields in IGZO within this universal mobility curve would help to identify how the mobility is limited by impurity/trap, phonon or surface roughness. Quantifying the deep trap density change of LSA IGZO TFTs, extracted from the subthreshold slope, should also be done. As one example, we have begun characterization of LSA IGZO TFT, yielding the universal relationship shown in Figure 7-1. The mobility increase at low field may due to impurity/trap scattering with the decrease at high field due to surface roughness.

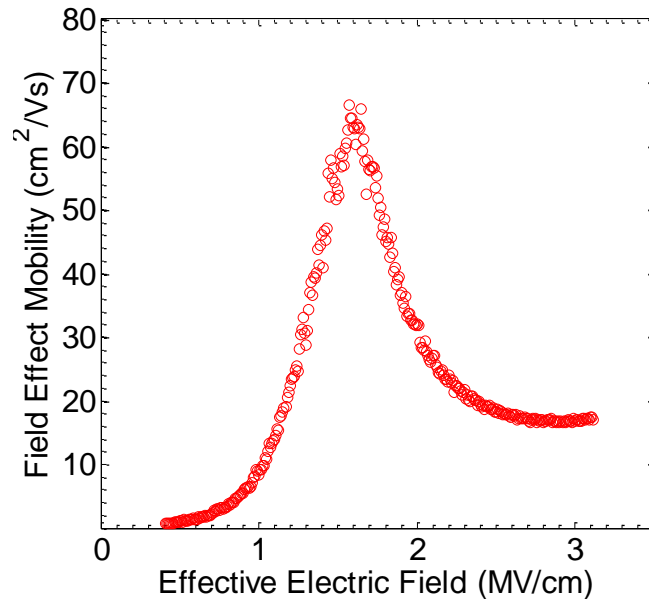


Figure 7-1. Field effective mobility as a function of effective normal electric field for an LSA IGZO TFT.

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