SURFACE/INTERFACE STATES IN GAN-BASED TRANSISTORS: GATE DIELECTRICS AND SURFACE PASSIVATION

A Thesis

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by

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ABSTRACT

GaN has raised wide attention owing to its high breakdown voltage and capability of performing efficiently even at high temperature. However, there are several challenges to overcome for achieving the superior performance of GaN HEMTs, including management and minimization of gate leakage and interface states located at the insulator-semiconductor interface. In this work, I studied several gate insulators readily available at CNF and their insulator-semiconductor interface in the metal-insulator-semiconductor capacitor structure. I found that the Al_2O_3/HfO_2 bilayer is helpful in reducing gate leakage by one order of magnitude and improving the breakdown field from 4.5 MV/cm to 6.5 MV/cm compared to the single HfO_2 layer with a similar equivalent oxide thickness. The observed improvement can be attributed to the large bandgap and excellent conduction band offset of Al_2O_3. Moreover, I found that a UV/ozone oxidation surface treatment prior to dielectric deposition helps to decrease the interface density of states at 0.39 eV below the conduction band to 1.2×10^{12} eV^{-1} cm^{-2} characterized by the frequency-dependent conductance method.

I also studied PECVD SiN_x passivation of AlN/GaN/AlN quantum well HEMTs with several surface treatment methods. With NH_3 plasma pretreatment, I observed an improvement in the maximum drain current by 30 % and peak transconductance by 60 % in these HEMTs. These are positive indicators for the effectiveness of NH_3 plasma pretreatment in managing dispersion in HEMTs.

BIOGRAPHICAL SKETCH

Cheng Wang studied Nano Materials and Science at Soochow University in Suzhou, China for his undergraduate degree. During his four years as undergraduate, he researched on the self-assembly of organic heterostructured materials composed of microcrystals and the synthesize of thermally activated delayed fluorescence emitters for organic light emitting diodes (OLEDs) application.

After finishing his Bachelor's degree, Cheng came to Cornell University to purse Master of Science degree in Materials Science and Engineering. He worked under Professor Debdeep Jena and Professor Grace Xing's guidance on GaN-based electric devices. Cheng is expected to receive his Master of Science degree in May, 2023.

Dedicated for my parents.

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CHAPTER 1

INTRODUCTION

1.1 Overview

With the rapid development of information technology, semiconductors play a critical role in modern society. Many fields, including display, storeage, power supply, integrated circuits and consumer electronic, all aspire novel semiconductor materials to achieve better performance.

The first observation of semiconductors could draw back to 1833. After that, elemental semiconductor materials, such as silicon (Si) and germanium (Ge), emerged as the most well-known platforms for microelectronics. From 1960s, in order to fulfill the demands of information superhighway, compound semiconductors came to scientist's eyes due to its high electron mobility. The most famous materials are GaAs and InP. Yet today, the state of art technology requires electronics to be adapted in harsh environment, which triggered the discovery of wide bandgap semiconductor and ultra-wide bandgap semiconductors, such as silicon carbide (SiC), gallium oxides (Ga_2O_3), aluminium nitride (AlN) and gallium nitride (GaN). Electronic properties of several typical semiconductor materials have been listed in Table 1.1. Among them, GaN combines both wide bandgap and high saturation velocity for high-power, high-frequency applications, establishing it as the a promising candidate for future electronics.

Table 1.1: Electronic properties of typical semiconductor materials [1,2].

Materials	Si	GaAs	4H-SiC	β-Ga_2O_3	GaN	AlN
Bandgap E_{gap} (eV)	1.12	1.42	3.26	4.5	3.39	6.2
Electron Mobility μ ($cm^2/V \cdot s$)	1400	9400	950	200	1500	450
Critical Field E_c (MV/cm)	0.3	0.52	2.2	7	3	15
Saturation velocity v_{sat} ($\times 10^7$ cm/s)	1	0.9	0.8	1.2	2.4	1.4

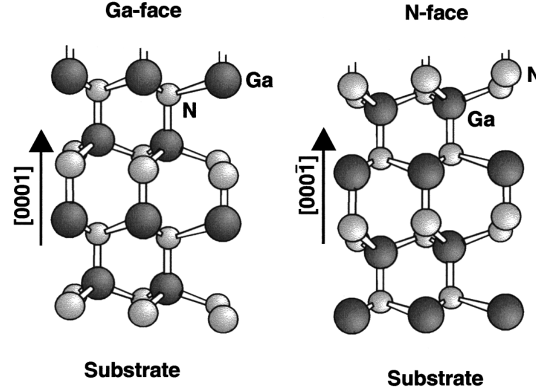

Figure 1.1: Schematic crystal structures of wurtzite Ga-face and N-face GaN [3].

1.2 Spontaneous polarization of GaN

Except for its predominant electronic properties, strong spontaneous polarization and piezoelectronic polarization of GaN also make it a premier material. As shown in Fig. 1.1, the wurtzite GaN lattice has uniaxial and non-centrosymmetry structure, resulting in a large spontaneous polarization along the <0001> direction. The polarization of GaN depends on the orientation of basic building block, which is one Ga atom bounding with four neighboring N atoms. If this building block is pointing upward, there will be negative polarization charges form at the surface and it is referred as metal-polar orientation. In the opposite orientation, the direction of this building block will reverse and positive polarization charges will form at the surface. By connecting to other III-V group seminconductor materials, such as AlGaN and AlN, a 2-

dimentional electron gas (2DEG) will form at the heterojunction interface. Fig. 1.2 shows a a metal-polar AlN/GaN/AlN quantum well high-electron mobility transistor (QW HEMT) and 2DEG forms at its top AlN/GaN interface [4]. Fig. 1.3 shows N-polar GaN/$Al_{0.91}Ga_{0.09}N$/AlN HEMTs on bulk AlN substrates with 2DEG forms at GaN/AlGaN interface [5].

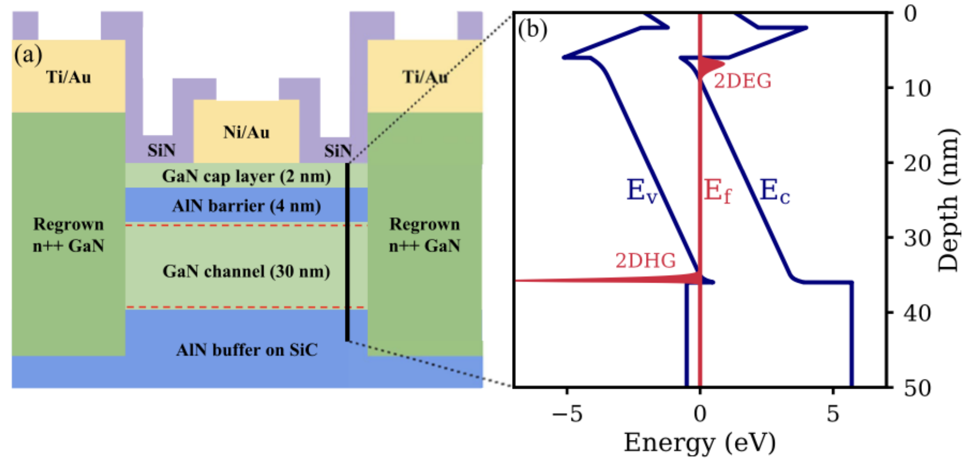

Figure 1.2: (a) Schematic cross section and (b) band diagram of a metal-polar AlN/GaN/AlN quantum well HEMT and the formation of 2DEG at its top AlN/GaN interface [4].

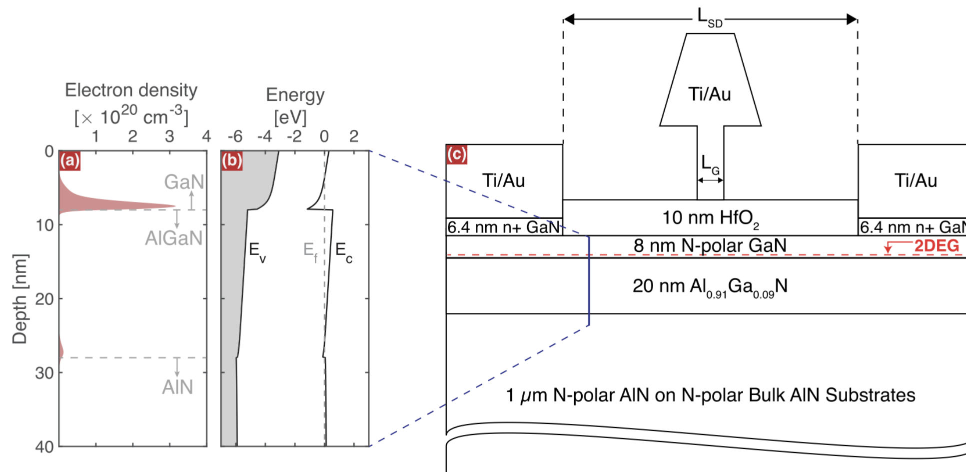

Figure 1.3: (a) Electron density profile, (b) band diagram and (c) cross section of scaled N-polar GaN/$Al_{0.91}Ga_{0.09}N$/AlN HEMTs on bulk AlN substrates with 2DEG forms at GaN/AlGaN interface [5].

1.2.1 The advantages of N-polar GaN HEMTs

Compared with metal-polar GaN HEMTs, N-polar GaN HEMTs has following advantages, making it as an attractive field worth exploring.

1.2.1.1 Low ohmic contact resistance

Theoretically, N-polar GaN HEMTs can achieve better ohmic contact than metal-polar one through advanced device design. The 2DEG formed in N-polar GaN HEMTs can be contacted by depositing gate metals directly on the channel layer which has narrower bandgap and lower barrier for the electron, rather than through the wide bandgap barrier layer that is necessary in a metal-polar GaN HEMT. According to Wong et al., a low contact resistance of 0.16 Ω·mm was realized without any contact annealing on the N-polar GaN/AlGaN/GaN HEMT structure, while the contact resistance is around 0.4 Ω·mm for metal-polar counterparts even after high temperature annealing [9].

1.2.1.2 Strong electron confinement

N-polar heterostructures were found to provide better suppression of short-channel effects [10]. When a negative bias is applied on the gate to turn off the transistor, the 2DEG will be depleted and move away from the gate in metal-polar devices, so a semi-insulating back barrier is typically used. But in N-polar devices, the 2DEG will be confined by the back barrier of AlGaN or AlN and localized at the heterostructure interface. This helps to get better off-state pinch-off and reduce on-state output conductance [11].

1.2.2 The challenges of N-polar GaN HEMTs

Although N-polar GaN brings plenty of opportunities for HEMTs application, there are some challenges need to be overcome. Kim et al. reported the first demonstration of N-polar GaN/AlGaN/AlN HEMT on single crystal AlN substrates [14]. It achieved high drain current exceeding 0.94 A/mm, low contact resistance without the regrowth process, and low buffer leakage, also taking advantages of good thermal management capability of AlN substrate. However, due to the lack of top barrier in this structure and a non-optimized gate dielectric layer, undesired high gate leakage current is observed during measurement, leading to a moderate on/off ratio ~ 12. The excessive leakage current through gate will not only compromise device reliability, but also degrades power efficiency and lifetime in real application. So it is necessary to develop an optimized dielectric layer for better device performance.

1.3 Surface/Interface states issues in GaN-based systems

Dielectric materials are typically used in HEMTs to block the gate leakage current. In GaN-based HEMTs, they are also employed to passivate the regions between the source/drain and the gate. This is important since GaN-based HEMTs are sensitive to the surface states, which is related to either surface dangling bonds or nitrogen vacancies [15, 16]. These surface states will charge and discharge for a relatively long time in comparison to the switching speed of GaN-based HEMTs. As a result, they will behave as a virtual gate in additional to the metal gate, extending the gate into the access region (regions between the gate and source/drain) [17]. Consequently, the control of the on/off state of the

transistors is taken over by the trap/de-trap time of the surface states instead of the gate bias. When the gate pulse time reaches certain short values, surface trapped electrons will not be able to follow the gate bias variation and drain current collapse will occur. This phenomenon is called as DC to RF dispersion and could be characterized by pulsed I_d-V_d measurements. A study about the SiN_x passivation with the help of NH_3 plasma pretreatment has been explored and will be discussed in details in Chapter 3.

Aside from surface states, metal-oxide-semiconductor (MOS) interface trap states will have similar impacts on the transistor performance. However, they are generally easier to control and measure [17]. They can respond to the fermi level modulation arised from the gate bias, which is essential for the characterization of interface trap states. More details about the optimization and characterization of insulator-semiconductor interface quality will be further discussed in Chapter 2.

Nevertheless, it is important to understand the surface/interface situation in GaN-based systems for the benefit of better optimization and reliable function of the transistors.

1.4 Topics covered in this thesis

The primary goal of this thesis is to provide potential solution for high gate leakage current issue appeared in N-polar GaN HEMTs with optimized dielectric materials, which includes choosing suitable dielectric stack, testing the effects of different treatments and improving insulator-semiconductor interface quality. The secondary objective is to investigate the interface states

issues in GaN-based system. Another purpose is to study the effects of surface passivation using SiN_x with plasma pretreatment on metal-polar GaN HEMTs. To be more specific,

In Chapter 2, a study about dielectric materials and oxide-semiconductor interface using metal-polar metal-oxide-semiconductor capacitor (MOSCAP) was proposed. General discussion about dielectric materials and literature review of GaN MOSCAP was first illustrated. After that, experimental methods and fabrication procedure of metal-polar GaN MOSCAP were covered. Characterization setup and results, along with the analysis and discussion, were shown as well.

In Chapter 3, device passivation using SiN_x with the assist of NH_3 plasma pretreatment on metal-polar GaN HEMTs was studied. An introduction about passivation was proposed first then more discussions about experimental methods, results and discussion were demonstrated.

In Chapter 4, a summary about the experiments in this thesis, also suggestions for continued work, was provided.

CHAPTER 2

DIELECTRIC MATERIALS AND INSULATOR-SEMINCONDUCTOR INTERFACE STUDY USING MOSCAPS

2.1 Overview of gate insulator technology on GaN

Although significant progress has been achieved in GaN-based high-power/high-frequency electronic devices, unacceptable schottky gate leakage current remained as a problematic issues. One of the solutions is to grow an insulator layer between the metal and semicondutor materials. Theoretically, insulators have larger bandgap and superior band offset, offering better block to surpress the reversed current and tunneling transport compared with schottky barrier. For Si-based devices, silicon dioxide (SiO_2) was widely applied as gate insulator since it is easy to grow on Si, along with great electrical stability at the interface [18]. However, unlike SiO_2, there have been no suitable native oxides for GaN that can maintain a high quality interface with low density of traps and other kinds of defects, which highlights the importance of proper choice for dielectric materials and interface treatment.

There are some criteria for choosing a gate insulator candidate for GaN. One needs to pay attention to the band alignment. The large conduction band offset is good for blocking electrons, which can potentially reduce leakage current. Meanwhile, the bandgap and the dielectric constant of the materials should also be well considered. Larger bandgap will lead to higher breakdown field, ensuring a wider voltage modulation range for MOS structure devices. For relative dielectric constant, it is commonly believed higher value of dielectric constant could help to get a higher value of transconductance g_m in MOS

transistors [19]. In addition, high-k materials are able to prevent leakage current under an appropriate oxide thickness while also keeping the gate capacitance low. It could be characterized by equivalent oxide thickness (EOT) of the dielectric materials, which is defined by the following equation:

$$EOT = t_{high-k} \frac{k_{SiO_2}}{k_{high-k}} \tag{2.1}$$

where t_{high-k} is the thickness of the dielectric material, k_{SiO_2} is the relative dielectric constant of SiO_2 and k_{high-k} is the relative dielectric constant of the high-k dielectric material.

With a large k_{high-k} compared with k_{SiO_2}, thicker dielectric material could be deposited but maintaining the same EOT. This is important since thicker film is helpful to reduce the leakage of electrons, while achieving the same gate capacitance and being free of any degradation on the control capability of the gate.

Fig. 2.1 presents the plot of the energy bandgap with respect to the relative permittivity for various gate insulators [6]. Fig. 2.2 shows the band offsets at insulator/GaN interface, the data is calculated by Robertson et al. [7] and plotted by Yatabe et al. [6]. The simulation is conducted based on the method using charge neutrality levels (CNLs) as the reference energy, which is commonly used for Si-based systems. Among the insulators shown here, Al_2O_3 and HfO_2 are two of the most attractive candidates for MOS structure devices. Al_2O_3 combines most of the desired properties such as large bandgap, relatively high dielectric constant and significant band offsets alignment. While HfO_2 has acceptable bandgap along with conduction band lineup, the high relative

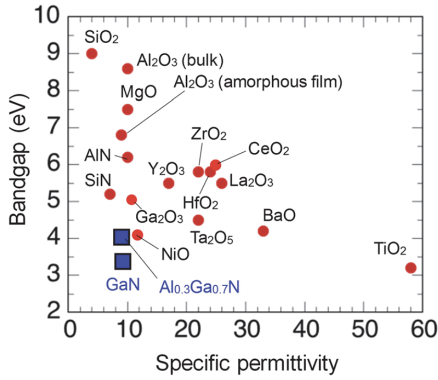

Figure 2.1: Bandgap versus relative permittivity for various insulator materials [6].

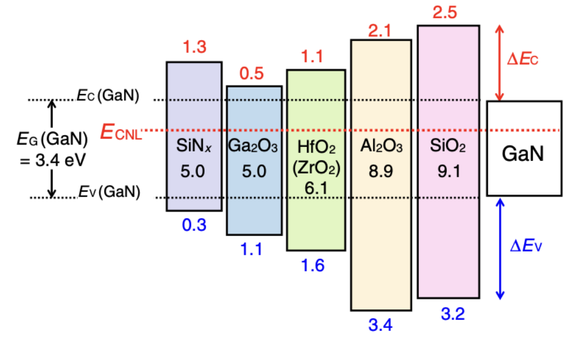

Figure 2.2: Band offsets at Insulator/GaN interface calculated by Robertson et al. [6,7].

dielectric constant makes it stand out for further exploration.

Apart from the intrinsic properties of insulator materials, non-optimized insulator-semiconductor interface, where exists large amount of interface trap states, also result in the poor reliability of the devices. Many methods have been investigated and applied in fabrication to solve this problem. Before we take a look at how people solved this problem, common used approaches to characterize these defects, such as trap state density (D_t) and interface state density (D_{it}), should be first understood.

2.1.1 Background about trap states/interface states measurement

2.1.1.1 Terman method

The idea of this method is to compare the high-frequency Capacitance-Voltage (C-V) measurement with the theoretical C-V curve from simulation, which does not consider any kinds of defect states. The difference in voltage, at a constant

capacitance, yields the amount of interface trap state charges that changed occupancy below the Fermi level associated with that capacitance value [20]. This method is well performed to characterize interface quality in Si-based system. However, it is not the same case in GaN-based device. Due to the large bandgap and extremely low minority carrier concentration, the Terman method is not very helpful at room temperature. But it can be still applied to evaluate the insulator-semiconductor interface quality to some extend [17].

2.1.1.2 Conductance method

Conductance method is to measure the conductance loss arising from the charging and discharging of the interface traps due to the Fermi level scaning from above to below that specific energy level of the trap states. For GaN-based MOS structures, the bulk generation-recombination rate and diffusion-induced inversion are relatively small at room temperature and there is almost no inversion region could be formed during C-V measurement even at lowest frequency 1 kHz [21]. Therefore, a series of peaks in conductance observed when doing frequency-dependent measurement under different gate bias can be ascribed to interface traps and the interface states density could be derived from the curve fitting to the peak values [21]. Unfortunately, for wide bandgap materials such as GaN, it has been reported that a clear defect response is not always observed from every GaN-based sample [22]. The reasons have not been fully understood but few assumptions were made. One possibility for this lack of detection is that interface states in wide band gap semiconductor materials can not lead to strong peaks that can be clearly attributed to a defect response in the frequency range examined [21]. Besides, the trap emission time of GaN

is relatively long, exceeding the effective detection time range of conductance method, which is on the order of 10 ms or faster. As a result, the signal becomes noisy as the capacitance measurement also become noisy at low frequency [17].

2.1.1.3 Photon-assisted C-V method

The High Frequency Photon-assisted Capacitance-Voltage (Photon-CV) method used in GaN systems was comprehensively reported by Swenson [17, 23]. Generally, UV light is applied during C-V measurement to generate electron-hole pairs into the device. The injected holes enable the interface states to change occupancy by allowing the electrons in the interface states to recombine. By comparing the curve under illumination with the one under dark condition, the net added charges originated from the recombination of induced holes with the interface states and trap states could be characterized. One advantage of Photon-CV method is that it is useful at room temperature because plenty of holes to be captured by traps were provided by UV light while minority carrier generation requires high temperature for the other two methods. To be noticed, this method is designed specifically for insulators which have positive conduction band offset and near zero or even negative valence band offset. According to Fig. 2.2, SiN_x is the suitable material that meet all the mentioned requirment, while careful consideration should be taken on Al_2O_3 and HfO_2 when using this method. If a positive valence band offset exists, the generated holes via UV light would be blocked at the insulator-semiconductor interface and screen the interface trap states since they are indistinguishable to C-V measurement. Additionally, the accumulated holes would potentially raise the Fermi level above that of the interface states, thus preventing them from

ionizing.

Aside from the above three mentioned methods, High-Low frequency Capacitance-Voltage, Deep Level Transient Spectroscopy (DLTS), Isothermal Capacitance Transient Spectroscopy (ICTS), Deep Level Optical Spectroscopy (DLOS) et al. could also be employed to evaluate interface quality, while they are not studied in this thesis [17].

2.1.2 Processing optimization on insulator-semiconductor interface

Great efforts have been taken to minimize interface states in GaN-based system. In general, most of the optimization could be done on the following aspects: ex-situ clean, which includes all the processing done outside of deposition chamber; in-situ clean, indicating treatment inside the chamber; deposition methods and variables and post-deposition annealing (PDA). A summary table about different optimization approaches and corresponding results from literatures is attached in Appendix A. It is worth noting that studies mentioned below have been focused on metal-polar GaN.

The main goal of ex-situ/in-situ clean is to modify the surface of GaN. Due to the poor quality of the native gallium oxide at the surface of GaN, as well as other kinds of defects or impurities introduced by air or non-optimized processing procedure, numerous traps and fixed charges are presenting at the insulator-semiconductor interface. To overcome that, plenty of optimization methods have been designed and investigated to remove undesirable element and passivate the surface, which can be generally classified into two kinds of strategies. One is to remove the native oxide through chemical clean or in-situ

plasma clean before the gate dielectric deposition. For example, Chakroun et al. investigated the effect of different chemical clean prior to SiO_2 deposition by comparing the C-V results with the theory. It turned out the MOSCAP treated with 85% potassium hydroxide (KOH) and 40% hydrochloric acid (HCl) for 2 minutes respectively, showing the best capacitance modulation nearly identical to the theoretical one. Based on the Terman method, a D_{it} of 2×10^{10} cm^{-2} eV^{-1} was estimated [24]. There are some other work which highlight the use of ammonium sulfide ($(NH_4)_2S$) for chemical clean. Ren et al. demonstrated that two steps treatment, including 1:5 HF for 3 minutes at room temperature, followed by $(NH_4)_2S$ solution for 30 minutes at 70 °C, could effectively reduce D_{it} to $\sim 10^{11}$ cm^{-2} eV^{-1} on Al_2O_3/GaN MOSCAP [25]. Gu et al. incorporated both $(NH_4)_2S$ and in-situ plasma clean to reduce defect binding on GaN, achieving 9×10^{11} cm^{-2} eV^{-1} of interface states density and lowest frequency dispersion of C-V measurement among all the control groups. Another commonly reported chemical is piranha solution, a mixture of hydrogen peroxide (H_2O_2) and sulfuric acid (H_2SO_4). Hossain et al. found out the Al_2O_3/GaN sample treated by piranha (H_2O_2:H_2SO_4=1:5) shows the lowest hysteresis (0.25 V), as long as the lowest carbon concentration at interface through x-ray photoelectron spectroscopy (XPS) analysis. Photon-CV method is applied to characterize the interface quality and the dropping of D_{it} from $\sim 10^{14}$ cm^{-2} eV^{-1} to 3.7×10^{12} cm^{-2} eV^{-1} is observed comparing the untreated sample with the piranha-cleaned sample.

The other strategy is to grow a high quality Ga_2O_3 layer as the interfacial layer, taking advantage of great lattice match between Ga_2O_3 and GaN. Wang et al. proposed that the Ga_2O_3 interlayer between GaN and Al_2O_3 developed by pulsed laser deposition (PLD) could effectively surpress hysteresis and

frequency dispersion during C-V measurement. Meanwhile, a signficant decrease of D_{it} at 0.36 eV below the conduction band, from 9×10^{12} cm^{-2} eV^{-1} to 2.4×10^{10} cm^{-2} eV^{-1}, is demonstrated by the conductance method due to the introduction of the Ga_2O_3 layer [26].

Aside from the above mentioned treatments, attention has also been paid to the deposition approach of the dielectric materials, as well as the precursors used. Several methods, such as atomic layer deposition (ALD), chemical vapour deposition (CVD), and molecular beam epitaxy (MBE) have been widely employed to deposit the thin films. Yeluri et al. compared the performances of Al_2O_3 deposited by ALD and metalorganic chemical vapour deposition (MOCVD). Based on the photon-CV measurement, two capacitors showed similar level of interface states density ($\sim 2.5 \times 10^{12}$ cm^{-2} eV^{-1}), while the border trap charges induced during MOCVD growth was one order of magnitude lower than that from ALD [27]. Uenuma et al. explored the influence of precursors on ALD Al_2O_3. Secondary ion mass spectrometry (SIMS) was used to check the carbon concentration of different samples. It turned out that a reduction of approximately 50% of the residual carbon was achieved using DMAH as precursor instead of using TMA. As a result, one order of magnitude lower D_{it} was reached by using DMAH through conductance method. Moreover, in order to better understand the impact of impurity, high-pressure water vapor annealing (HPWVA) at 400 °C and 0.5 MPa for 30 minutes was performed to passivate the oxygen vacancies as a control group. The results turned out that it is helpful to reduce flatband shift under high bias stress, however, it has nothing to do with interface traps. To sum up, carbon impurity is more responsible for D_{it} while both carbon impurity and oxygen vacancies could result in flatband shift for Al_2O_3/GaN structure based on their

experiments [28].

After deposition, PDA is usually applied to recover lattice damage and get better contact for insulator/metal-semiconductor interface. Futhermore, PDA conducted with suitable condition could result in the material phase transfermation from amphorous to crystalline, expanding the possibility of insulator materials deposited by low-temperature method. Glaser et al. discovered that a 30 minutes rapid thermal annealing (RTA) at 850 °C in ambient air environment reduced the gate leakage from 10^{-4} to 10^{-8} A/cm^2 for SiO_2/GaN MOSCAP under 5 MV/cm. Annealing to HfO_2 films at 850 °C showed reduction in leakage, but a decrease of 2 MV/cm in critical field was also observed as a trade-off [29].

All the above mentioned studies have been focused on depositing gate dielectrics on metal-polar GaN. However, due to the fact that N-polar GaN surface is more chemically reactive compared with metal-polar one, higher incorporation of impurities and much more surface states is presented on N-polar GaN, calling for superior optimization on N-polar GaN MOS structure. Mohanty et al. conducted a systematical study about various ex-situ surface treatments, in-situ ALD plasma clean, deposition approach, and annealing conditions on the interface quality of HfO_2 on N-polar GaN. The trap states D_t and the interface states D_{it} are characterized by Photon-CV method developed by Swenson [23]. Among all the samples, the one with the following optimization exhibited the best performance among his research: cleaned with 1:5 diluted piranha for 5 minutes and 1:50 diluted buffered hydrofluoric acid (BHF) for 90 seconds followed by ex-situ UV-ozone treatment for 15 minutes to oxidize the surface GaN into Ga_2O_3, then sample was loaded into ALD chamber

with 5 cycles of in-situ TMA/N_2 plasma clean prior to thermal HfO_2 deposition at 250 °C. After that, a PDA at 400 °C in O_2 for one minute was performed. Seperate control experiments were conducted to demonstrate the influence of every step of optimization. The intergration of ex-situ UV-ozone treatment leaded to better interface, shown as an increase of dielectric constant from 15.1 to 15.9 and also a marginal reduction of the average D_t from 5.8×10^{12} cm^{-2} eV^{-1} to 1.6×10^{12} cm^{-2} eV^{-1}. On the other hand, in-situ TMA/N_2 plasma clean improved the dielectric constant from 15.3 to 16.3 and reduced the average D_t from 7.2×10^{12} cm^{-2} eV^{-1} to 6.3×10^{12} cm^{-2} eV^{-1}. Additionally, HfO_2 films developed by the thermal ALD showed higher dielectric constant from 14.5 to 15.1, also with better breakdown field from 2.75 to 3.11 MV/cm over plasma ALD. Moreover, annealing in N_2/O_2 and O_2 gas resulted in a fewer D_{it} and higher dielectric constant and breakdown field compared with annealing in N_2 gas only [30].

2.2 Experimental setups and device fabrication

The device designed in this thesis is metal-oxide-semiconductor capacitors. This structure is relatively easy to fabricate compared with metal-oxide-semiconductor field-effect transistors (MOSFETs) or metal-insulator -semiconductor high-electron-mobility transistors (MIS-HEMTs). But the critical MOS structure could be well characterized based on this device. ALD is chosen for the gate insulators deposition in this thesis because ALD is capable of depositing conformal, uniform and well-controlled films. These advantages make ALD a promising platform for advanced MIS-HEMT structure which requires thin dielectric films (~ 10 nm) and high-aspect-ratio T-gates to reduce

gate–drain capacitance as well as gate length for better current-gain cutoff frequency (f_T) and power-gain cutoff frequency (f_{max}).

2.2.1 Fabrication procedure

The n-GaN/n+GaN epitaxial structures were grown by Dr. Jimy Encomendero via plasma-assisted molecular beam epitaxy (MBE) on metal-polar GaN template on sapphire substrates. From bottom to top, the structure consists of a 300 nm n+GaN:Si layer with a doping concentration of 3×10^{19} cm^{-3}, and a 800 nm n-GaN:Si layer with a doping concentration of 2×10^{17} cm^{-3} confirmed by C-V measurement. The overall processing procedure is shown in Fig. 2.3. Several samples were fabricated with various ex-situ treatments prior to ALD deposition. Then the samples were loaded immediately into ALD chamber to minimize impurities induced by air. In-situ plasma treatments were first implemented, followed by the deposition of dielectric materials via thermal ALD in Oxford FlexAL ALD system. After the deposition, post-deposition annealing was performed for all the samples, and the thickness of the thin film was measured using ellipsometer on a co-loaded Si piece. After that, gate metal stack Ti/Ni (20/60 nm) was patterned by i-line photolithography and deposited by electron-beam evaporator. Standard lift-off procedure was then conducted. The gate metal stack was used as the hard mask for self-aligned etching until the n+GaN layer was exposed via a chlorine-based inductively-coupled-plasma (ICP) dry etcher. Another patterning was done through i-line photolithography and ohmics metal stack Ti/Au (20/100 nm) was deposited by electron-beamevaporator. More details about the fabrication could be found in Appendix B.

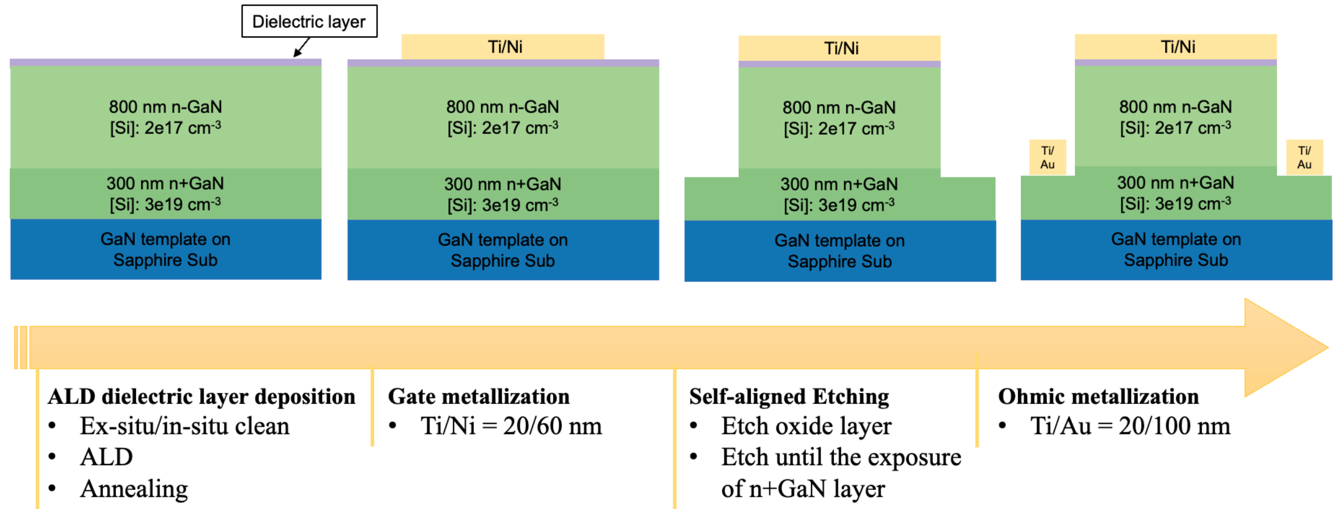

Figure 2.3: The process flow for MOSCAP Fabrication.

2.2.2 Characterization setups

All I-V, C-V and G-f (conductance method) measurements were taken at room temperature using Cascade 11000 probe station coupled with Keithley 4200A-SCS parameter analyzer.

2.3 Results, analysis and discussion

Table 2.1 shows the processing sets selected for the metal-polar GaN MOSCAPs and the corresponding energy band diagrams simulated by 1D Poisson [8] are shown in Fig. 2.4. To be noticed that this group of samples aims at setting baseline for further study, so the main variable locates at the different dielectric materials used. Sample 1 and Sample 2 were both treated with acetone and isopropyl alcohol (IPA) clean to remove any organic contamination. Then immersing the samples into HCl for 3 minutes, followed by an ex-situ Ga_2O_3 oxidation by UV/Ozone machine at 100 °C for 5 minutes. The ozone flux

was set at 5 liter/minute. Samples were then loaded into ALD chamber for thermal HfO_2 deposition. Afterwards, post-deposition annealing at 400 °C in O_2 ambient for 2 minutes was performed in RTA system. The thickness of thin film is ~ 9.3 nm and ~ 23 nm, respectively, based on the ellipsometer measurement on co-loaded Si pieces after PDA. For Sample 3, ~ 3.2/7 nm Al_2O_3/HfO_2 bilayer was grown as insulator layer. Meanwhile, the influence of in-situ N_2 plasma clean was tested on this sample. Sample 4 was treated with UV/Ozone and then deposited ~ 2.4/9.5 nm Al_2O_3/HfO_2 bilayer. All other processing was the same as on Sample 1, 2 and 3.

Table 2.1: Summary of processing employed for metal-polar GaN MOSCAPs.

Sample ID	**Ex-situ clean**	**In-situ clean**	**ALD**	**PDA**
Sample 1	Acetone/IPA+3 mins HCl 100 °C UV/Ozone for 5 mins	-	~ 9.3 nm HfO_2	400 °C in O_2 for 2 mins
Sample 2	Acetone/IPA+3 mins HCl 100 °C UV/Ozone for 5 mins	-	~ 23 nm HfO_2	400 °C in O_2 for 2 mins
Sample 3	Acetone/IPA+3 mins HCl	1 min N_2 plasma clean	~ 3.2/7 nm Al_2O_3/HfO_2	400 °C in O_2 for 2 mins
Sample 4	Acetone/IPA+3 mins HCl 100 °C UV/Ozone for 5 mins	-	~ 2.4/9.5 nm Al_2O_3/HfO_2	400 °C in O_2 for 2 mins

2.3.1 Capacitance-Voltage measurement

Keithley 4200A-SCS parameter analyzer operated at 100 kHz, 500 kHz and 1 MHz was used for C-V characterization. The gate bias was swept from depletion region into accumulation region for all measurements to avoid flatband voltage shifts in accumulation due to charge injection. As shown in Fig. 2.5, all four samples showed negligible frequency dispersion

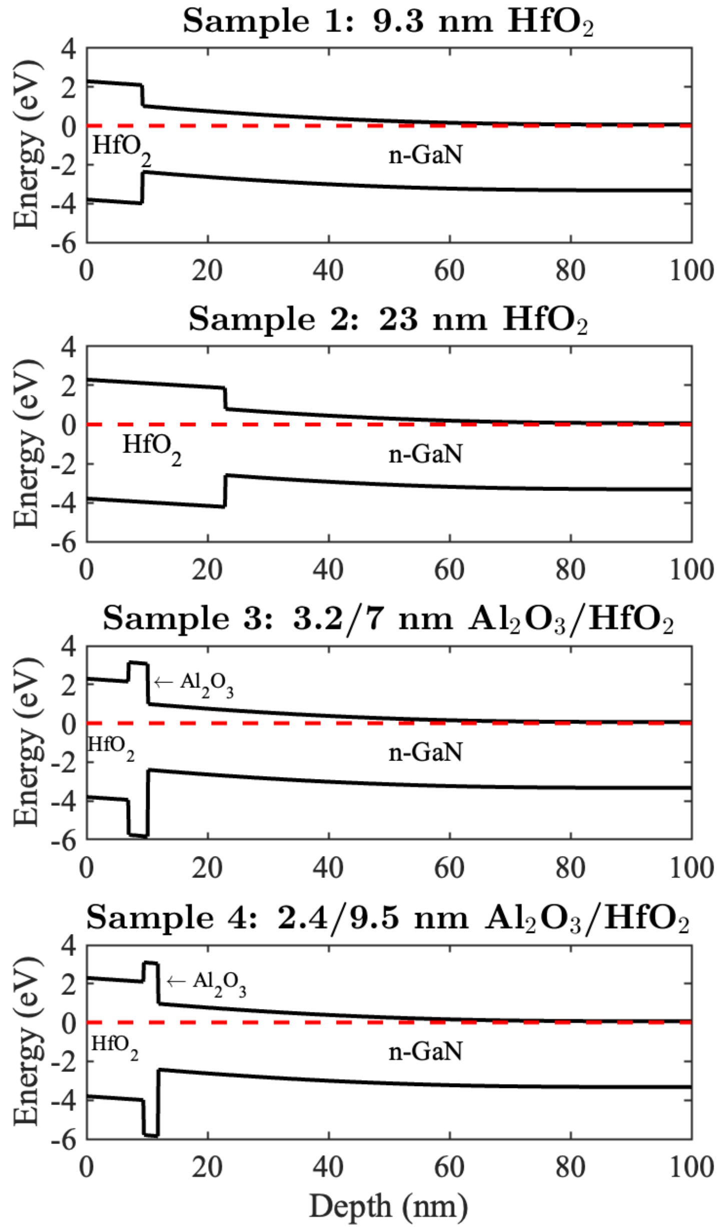

Figure 2.4: Energy band diagrams simulated by 1D Poisson [8].

among four selected frequencys. The relative dielectric constant was derived from the accumulation capacitance, which is based on the assumption that the semiconductor channel capacitance is very large with the Fermi level

near/above the conduction band edge so only insulator capacitance is measured in accumulation region. It can be determined by the following equation:

$$\epsilon_r = \frac{C_{acc} t}{A \epsilon_0} \tag{2.2}$$

where C_{acc} is the accumulation capacitance, t is the thickness of the dielectric material, A is the area of the device and ϵ_0 is the dielectric constant for free space.

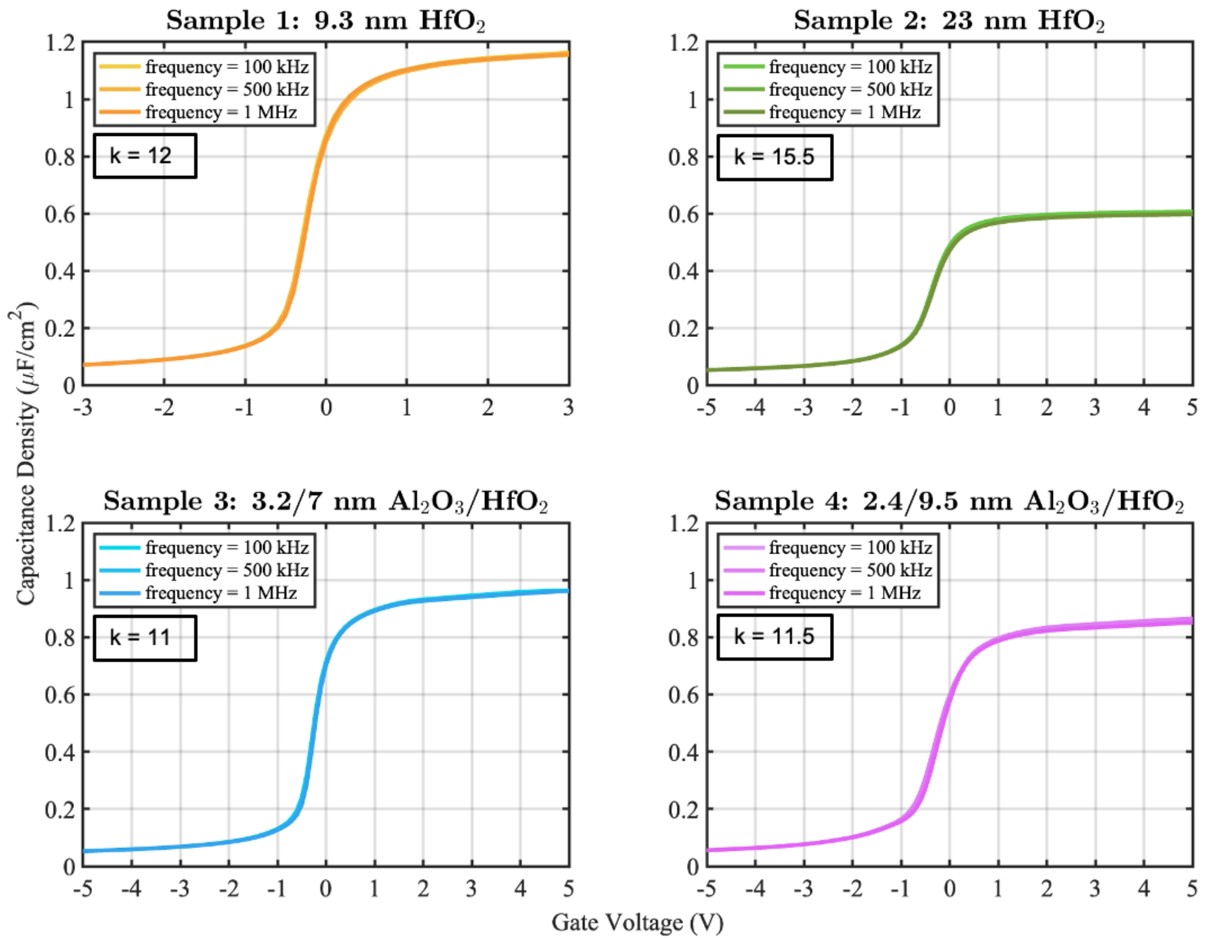

Figure 2.5: C-V characteristics for Sample 1 (a), Sample 2 (b), Sample 3 (c) and Sample 4 (d).

The accumulation capacitances measured at 3 V for Sample 1 and 5 V for

Sample 2, 3, 4 under 1 MHz were used and the relative dielectric constants were calculated to be 12, 15.5, 11, 11.5 for Sample 1, 2, 3, 4, respectively. Sample 3 shows the lowest permittivity due to the incorporation of a thicker Al_2O_3 layer, which has relatively lower k value (~ 8.9) than HfO_2. It is noteworthy that 20 nm thick HfO_2 (Sample 2) presents a higher dielectric constant over 10 nm thick one (Sample 1), although both of them fail to reach the therotical value for bulk HfO_2 (~ 20-25). Several assumptions have been made to explain this phenomenon. The thickness-dependence of dielectric characteristics may be attributed to the formation of a boundary layer at the interface, which has lower dielectric constant and decreases the average dielectric constant [31]. Another possibility is the degradation of the thin dielectric layer yielding a smaller dielectric constant [32]. Or, the reduction in the dielectric constant of the films is thought as a consequence of the size effects [33]. The most practical solution is to transfer the ALD HfO_2 from amphorous to crystalline phase via PDA at temperatures of 400–450 °C. Crystallization could help to better align the dipoles than in amphorous phase, resulting in a higher dielectric constant [34,35]. However, it has been reported that the crystallization may bring about a number of defects to the structure, which causes the increase of leakage current at the grain boundaries [36]. Further investigation is necessary to solve this problem.

2.3.2 Doping profile

The doping profile is obtained from the slope of a C-V curve or from the slope of a $1/C^2$ –V curve. It can be used to check the doping condition with respect to the depth from surface for epitaxial growth technology. The detailed derivation

is shown below

$$C = -\frac{dQ}{dV} = -qA\frac{d}{dV}\int_0^W N_d\,dx = -qAN_d(W)\frac{dW}{dV} \tag{2.3}$$

When considered it a parallel plate capacitor,

$$C = \frac{\epsilon_0\epsilon_r A}{W} \tag{2.4}$$

$$W = \frac{\epsilon_0\epsilon_r A}{C} \tag{2.5}$$

$$\frac{dW}{dV} = -\frac{\epsilon_0\epsilon_r A}{C^2}\frac{dC}{dV} \tag{2.6}$$

Then take Eq. 2.6 back to Eq. 2.3, we get

$$N_d(W) = \frac{C^3}{qA^2\epsilon_0\epsilon_r\frac{dC}{dV}} = -\frac{2}{qA^2\epsilon_0\epsilon_r\frac{d\frac{1}{C^2}}{dV}} \tag{2.7}$$

where $N_d(W)$ is depth-dependent doping concentration, q is the elementary charge, A is the area of the device, ϵ_r is the relative dielectric constant for semiconductor material, ϵ_0 is the dielectric constant for free space.

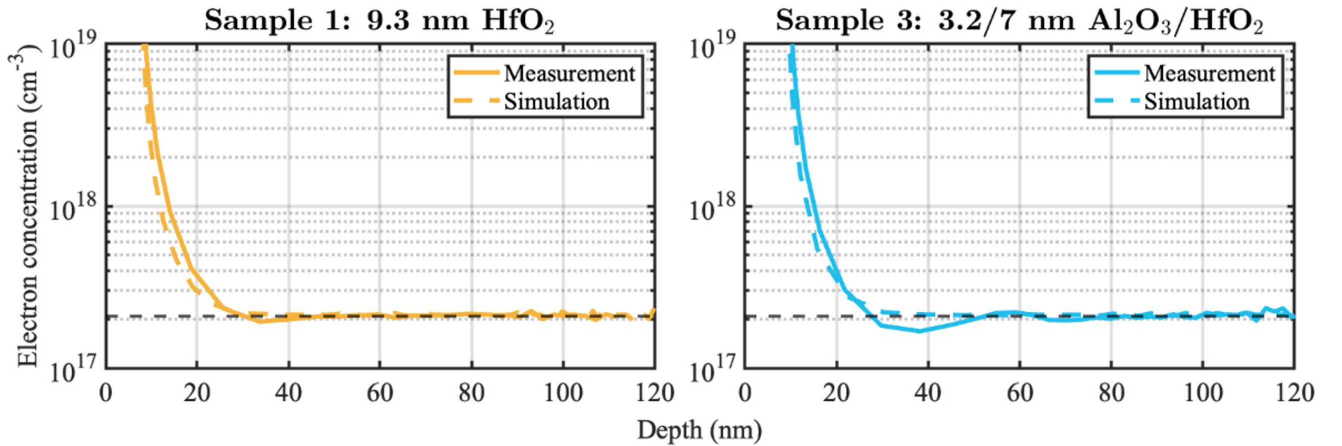

Figure 2.6: Doping profile for samples grown by MBE.

The doping profile for MBE grown samples is shown in Fig. 2.6. The solid lines are extracted from C-V measurement. To double confirm the results, the

1D Poisson simulations were carried out [8] and showed good agreement with the experimental data, both indicating $\sim 2 \times 10^{17}$ cm^{-3} n-type doping in n-GaN layer. Details about the simulation script used in the simulations could be found in Appendix C.

2.3.3 Current-Voltage measurement

The gate leakage currents and critical fields for three samples were characterized by I-V measurement shown in Fig. 2.7. The voltage sweep delay for all measurements was set to be 3 seconds to prevent displacement current. According to Fig. 2.7, 3.2/7 nm Al_2O_3/HfO_2 bilayer structure presents one order of magnitude lower leakage current density ($\sim 10^{-9}$ A/cm^2) even than 20 nm HfO_2 single layer under negative bias, where should be the 'off' state for HEMT application. Meanwhile, insulator heterostructure also shows lower current density compared to HfO_2 single layer with the same level thickness. Furthermore, when comparing sample 3 and 4, the incorporation of thicker Al_2O_3 helps better suppress gate leakage over the thin one and this can be attributed to the improvement in the dielectric quality. The lowest leakage current density under forward bias is observed on 20 nm HfO_2, which double confirms that the thicker film could surpress the gate leakage and highlights the advantage of high-k materials.

Insulator breakdown is defined as an increase about one order of magnitude of gate leakage current density between two voltage sweep points. The forward breakdown field (E_{BD}) was calculated by dividing the breakdown voltage (V_{BD}) with dielectric layer thickness (t) using the following relation:

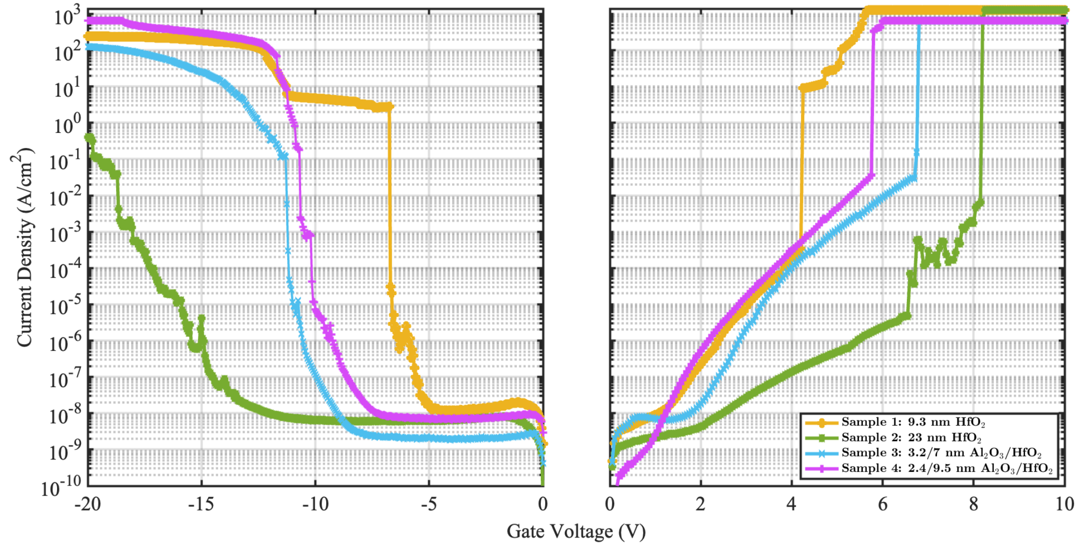

Figure 2.7: Gate leakage current as a function of gate bias for four samples.

$$E_{BD} = \frac{V_{BD}}{t} \tag{2.8}$$

For breakdown field under negative bias, however, Eq. 2.8 is no longer valid due to the partial distribution of field in semiconductor part when MOSCAP is under depletion region. As a result, self-consistent solution of the Poisson and Schrodinger equations [8] was employed instead to simulate the electric field across the insulator layer. All the calculated and measured results are summarized in the Table. 2.2.

Table 2.2: Summary of breakdown characteristics for metal-polar GaN MOSCAPs.

	Sample 1: 9.3 nm HfO_2	**Sample 2: 23 nm HfO_2**	**Sample 3: 3.2/7 nm Al_2O_3/HfO_2**	**Sample 4: 2.4/9.5 nm Al_2O_3/HfO_2**
Positive breakdown field	4.46 MV/cm (4.15 V)	3.5 MV/cm (8.1 V)	6.5 MV/cm (6.65 V)	4.75 MV/cm (5.65 V)
Negative breakdown field*	2 MV/cm (-6.7 V)	1.5 MV/cm (-14.85 V)	2.6 MV/cm (-11.15 V)	2.4 MV/cm (-10.5 V)

* The calculation is based on 1D Poisson, neglecting all interface state charges.

Consistently, Al_2O_3/HfO_2 bilayer structure shows higher breakdown field either under positive bias or under negative bias compared with HfO_2 single layer. The improvement of DC properties could be attributed to the larger bandgap and excellent band alignment of Al_2O_3 over HfO_2, agreed with the statements in section 2.1, the criteria for choosing a suitable dielectric material. Besides, similar to what were observed in gate leakage current characteristics, 3.2/7 nm Al_2O_3/HfO_2 can survive higher field strength than the 2.4/9.5 nm Al_2O_3/HfO_2. Whether thicker Al_2O_3 could get better gate control performance should need further investigation.

2.3.4 Interface trap states characterization

In this thesis, the Terman method and the conductance method were employed to characterize the interface quality. As mentioned in the previous section, the Terman method compares the experimental C-V curve with the theoretical ones at high frequency. As the total capacitance is measured at high frequency, the influence of the interface states on the C-V curve is shown as a stretch-out with gate bias. The stretch-out could be quantified by comparison with an ideal C-V curve, then the D_{it} could be obtained [25]. However, consider that the Terman method is not accurate to estimate interface states density at room temperature, it was only used to derive trap states or fixed charges N_t from the shift of flat band voltage between the measured C-V curve and the simulated one as shown in Fig. 2.8 according to Eq. 2.9. The C-V measurement data under 1 MHz was taken and the theoretical C-V curve was simulated by 1D Possion [8].

$$N_t = \frac{\Delta V_{fb} C_{ox}}{qA} \tag{2.9}$$

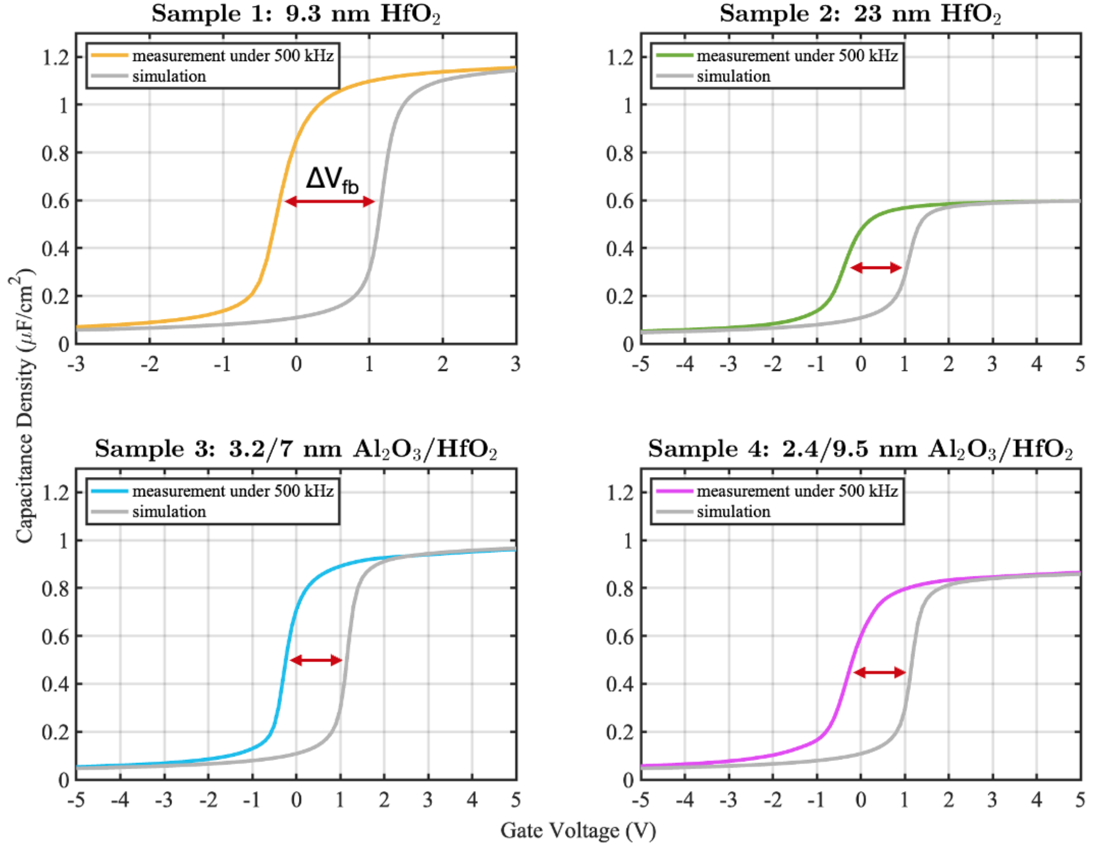

Figure 2.8: The Terman method for MOSCAPs by comparing measurement with simulation.

Instead, conductance method was applied to analyze the interface state density. The equivalent circuit for MOSCAP structure is shown in Fig. 2.9 (a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_s and the interface states capacitance C_{it}. The capture and emission of interface carriers is a lossy process, represented by the resistance R_{it}. To simplify the interface states circuit element from (a) to (b), the admittance Y_p of the parallel circuit and the impedance Z_s of the series circuit were used:

$$Y_p = G_p + j\omega C_p \tag{2.10}$$

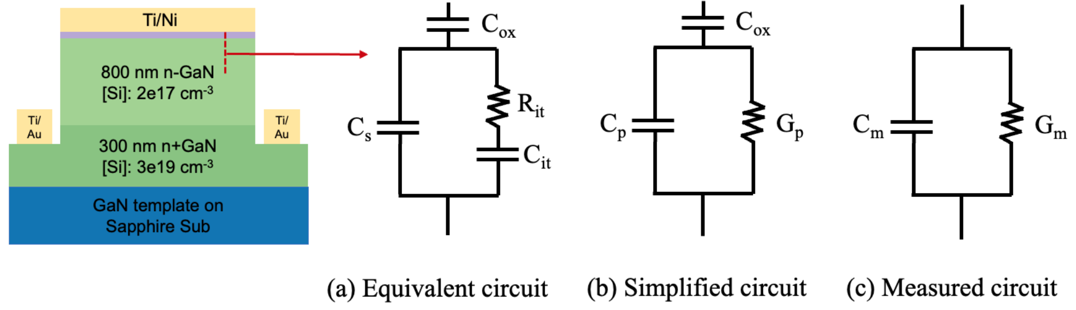

Figure 2.9: (a) The equivalent circuit for MOSCAPs structure when considering interface states, (b) the simplified one after converting interface resistance and capacitance into parallel conductance, (c) the measured circuit identified by the analyzer.

$$Z_s = R_s + \frac{1}{j\omega G_s} \tag{2.11}$$

where $\omega = 2\pi f$ (f is measured frequency).

So the C_p and G_p in Fig. 2.9 (b) were given by the following equations:

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \tag{2.12}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \tag{2.13}$$

where $C_{it} = qD_{it}$ and interface trap time constant $\tau_{it} = R_{it}C_{it}$.

On the other side, the circuit comparsion of Fig. 2.9 (b) and (c) gives the G_p/ω in term of the measured capacitance C_m, the measured conductance G_m and the oxide capacitance C_{ox}, which is

$$\frac{G_p}{\omega} = \frac{\omega G_m {C_{ox}}^2}{{G_m}^2 + \omega^2(C_{ox} - C_m)^2} \tag{2.14}$$

By applying Eq. 2.13 and Eq. 2.14, we closed the loop between the inputs (C_m, G_m, C_{ox}, ω) and outputs (D_{it}, τ_{it}). To be noticed, this model is only useful when oxide leakage current is low (losstan is much less than 0.1). Otherwise

series resistance r_s should also be considered, which is not the case for these four samples.

The conductance is measured as a function of frequency from 1kHz to 10 MHz via Keithley 4200A-SCS parameter analyzer and plotted as G_p/ω versus ω shown in Fig. 2.10. D_{it} and their corresponding energy levels below the conduction band were extracted by fitting the measured data using Eq. 2.13. The extracted D_{it} profile for four MOSCAP samples were plotted in Fig. 2.11. The trap state energy levels were calculated from interface trap time constant τ_{it} accounding to the Shockley-Read-Hall statistics as shown in Eq. 2.15 [37,38].

$$\Delta E_T = k_B T In(v_{th}\sigma_n N_C \tau_{it}) \tag{2.15}$$

where the capture cross section of the traps $\sigma_n = 4 \times 10^{-13}$ cm^{-2}, the electron thermal velocity $v_{th} = 2.6 \times 10^7$ cm/s, the effective density of states at GaN conduction band $N_c = 2.2 \times 10^{18}$ cm^{-3}, the Boltzmann constant $k_B = 1.38 \times 10^{-23}$ J/K and room temperature $T = 300$ K were used for calculation [38].

Table 2.3: Summary of characterization results for MOSCAPs.

	Sample 1: 9.3 nm HfO_2	**Sample 2: 23 nm HfO_2**	**Sample 3: 3.2/7 nm Al_2O_3/HfO_2**	**Sample 4: 2.4/9.5 nm Al_2O_3/HfO_2**
Dielectric constant / EOT	12 / 3 nm	15.5 / 5.7 nm	11 / 3.6 nm	11.5 / 4 nm
Positive breakdown field	4.46 MV/cm (4.15 V)	3.5 MV/cm (8.1 V)	6.5 MV/cm (6.65 V)	4.75 MV/cm (5.65 V)
Negative breakdown field*	2 MV/cm (-6.7 V)	1.5 MV/cm (-14.85 V)	2.6 MV/cm (-11.15 V)	2.4 MV/cm (-10.5 V)
D_{it} at E_c-E=0.39 eV	3×10^{13} eV^{-1}cm^{-2}	1×10^{13} eV^{-1}cm^{-2}	3.6×10^{13} eV^{-1}cm^{-2}	1.2×10^{12} eV^{-1}cm^{-2}
N_t from Terman method	1×10^{13} cm^{-2}	5.5×10^{12} cm^{-2}	8.4×10^{12} cm^{-2}	1×10^{13} cm^{-2}

* The calculation is based on 1D Poisson, neglecting all interface state charges.

The interface state density D_{it} at 0.39 eV below the conduction band and total trap states N_t derived from the Terman method were shown in the Table 2.3.

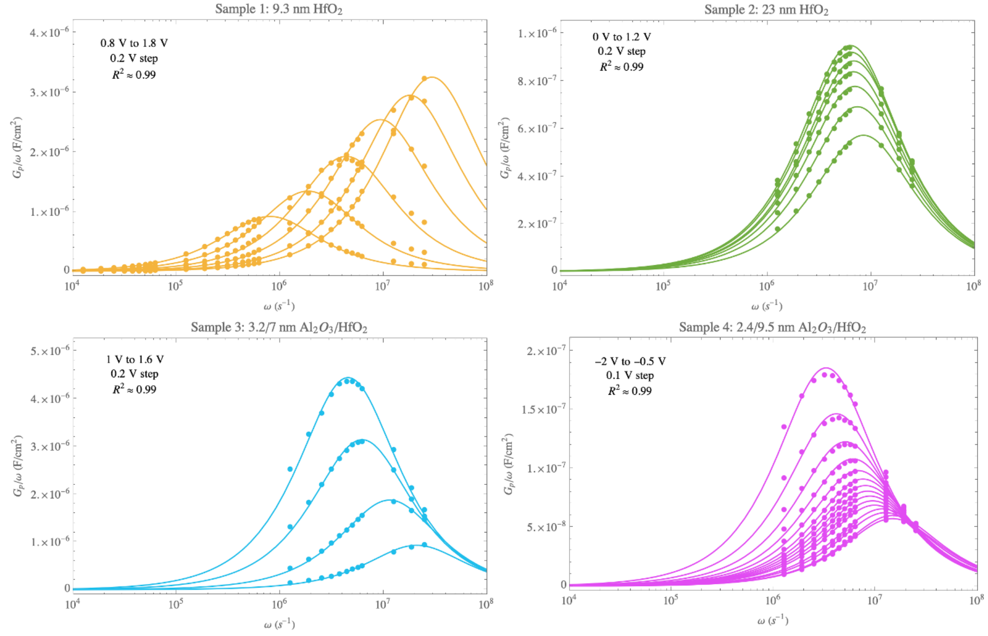

Figure 2.10: Frequency-dependent parallel conductance for MOSCAPs; the dots are the experimental data and the solid lines are fitting curves.

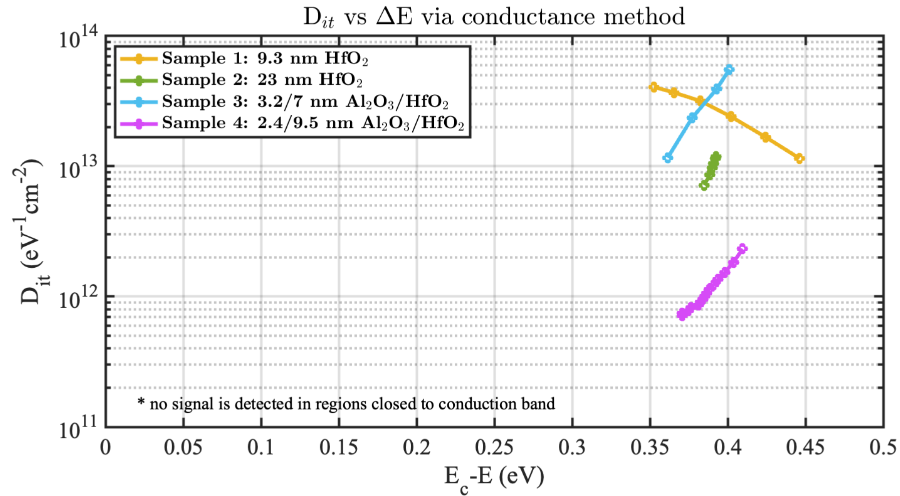

Figure 2.11: Interface state density in term of the energy level depth below the conduction band for MOSCAP samples .

According to the results, 23 nm HfO_2 showed less interface states and trap states than 9.3 nm one. This may because the degradation of thin dielectric material leads to more defects. From Sample 3 and 4, we could tell that bilayer MOSCAPs treated with UV/Ozone presented more than one order of magnitude lower

interface state density than the one with in-situ N_2 plasma clean. Furthermore, Al_2O_3/GaN interface had less interface states but similar level of fixed charges compared with HfO_2/GaN interface.

CHAPTER 3

NH_3 PLASMA ASSISTED SIN_X PASSIVATION ON GAN HEMTS

It is a common practice to passivate the surface of semiconductor devices to prevent the adverse effects on device performance stemming from the charge trapping effects. Passivation layer offers physical protection of the active region of the device, as well as blocking the contamination or moisture to prevent potential degradation of device performance. More importantly, passivation could bring the surface states away from the active region, leading to lower or potentially no DC to RF current dispersion. The choice of passivation layers and processing conditions need to be carefully considered. If the dielectric constant of a passivating material is too high, parasitic capacitances will increase and compromise the speeds of a device. Furthermore, if the passivation layer is highly crystallized, unacceptably high gate leakage current will flow due to grain boundary conductance and then decrease on/off ratio of the device [36]. As a result, researchers have focused on using low-k dielectric materials, along with the technology that allows low temperature deposition to prevent crystallization. The most typical approach is to deposit $\sim$ 100 nm thick SiN_x by plasma-enhanced chemical vapor deposition (PECVD) [39].

Although low-k dielectrics could help reduce parasitic capacitances, there is no promise that it will properly passivate the surface states. So, in-situ plasma treatments prior to the dielectric deposition have been widely used to enhance passivation. For example, N_2 plasma cleaning technique was applied before PECVD SiN_x deposition to improve device performance by removing the surface negative charges and reducing the surface potential [15]. O_2/Ar plasma treatment successfully suppressed both the gate leakage current and the

surface states [39]. It may be note that similar to the optimization of interface quality, surface passivation is also sensitive to epitaxy growth technology and fabrication process. Therefore, despite the numerous passivation techniques reported in the literature, they may not be easily transferable between site to site. In this work, SiN passivation with the aid of NH_3 plasma preclean on metal-polar GaN HEMT is demonstrated, setting the baseline for futher study.

3.1 Tests on AlN/GaN/AlN as-grown samples with Hall measurements

The optimized recipes of NH_3 plasma pretreatment and SiN_x deposition were first tested on as-grown metal-polar AlN/GaN/AlN samples. The characterizations were taken by room temperature Hall measurement system using the Van der Pauw test. The effect of each step is indicated in Table 3.1 by comparing the Hall measurement results before and after process, i.e., sheet resistance R_{sheet}, 2DEG sheet carrier concentration n_s and 2DEG mobility μ. Test 1 is NH_3 plasma pretreatment only, performed by Oxford 100 PECVD system using NH_3 and N_2 gas with power of 10 W for 5 minutes. Test 2 shows the influence of SiN_x deposition only. SiH_4 and NH_3 were used as precursors for deposition with power of 100 W for 3 minutes and 20 seconds. Test 3 combines 10 minutes NH_3 plasma preclean and 3 minutes SiN_x deposition together to demonstrate the final results. Note that 'Improvement' is defined as the trend towards better performance. In the other word, the decrease of R_{sheet}, increase of μ or n_s after the process.

It is clear to identify that all three tests improve the sheet resistance and

Table 3.1: Summary of Hall measurement results on as-grown metal-polar AlN/GaN/AlN samples before and after each processing step.

5 min NH_3 preclean only	R_{sheet} (Ω/sq)	μ ($cm^2/V{\cdot}s$)	n_s (cm^{-2})
Before	436.1	548	2.6e13
After	408.9	504	3.0e13
Improvement	6.24 %	-8 %	15.84 %
177 nm SiN_x deposition only	R_{sheet} (Ω/sq)	μ ($cm^2/V{\cdot}s$)	n_s (cm^{-2})
Before	416.4	620	2.4e13
After	402.8	478	3.2e13
Improvement	3.27 %	-23 %	34.22 %
10 min NH_3 preclean + 105 nm SiN_x deposition	R_{sheet} (Ω/sq)	μ ($cm^2/V{\cdot}s$)	n_s (cm^{-2})
Before	411.5	589	2.6e13
After	391.8	457	3.5e13
Improvement	4.79 %	-22 %	35.42 %

sheet carrier concentration of the as-grown samples, indicative of successfully passivated surface states. The decrease of mobility is also observed as a result of enhanced electron scattering coming from higher electron concentration. To better understand the passivation performance of current recipe, further test was conducted on AlN/GaN/AlN Quantum Well HEMTs.

3.2 Passivation performance on metal-polar AlN/GaN/AlN quantum well HEMTs

NH_3 plasma assisted SiN_x passivation was performed on metal-polar AlN/GaN/AlN HEMTs grown on SiC substrate. The setting for passivaiton is the same as test 3, which is 10 minutes NH_3 plasma preclean using NH_3 and

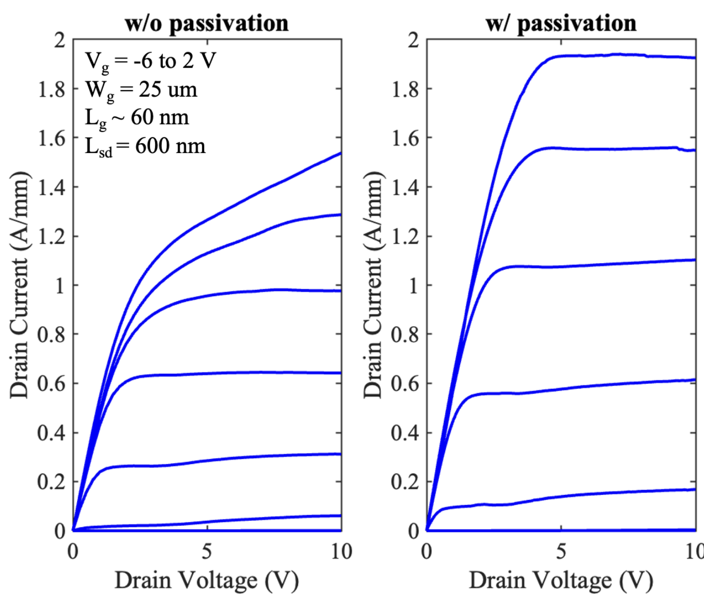

Figure 3.1: Output I_d-V_d curve with and without passivation.

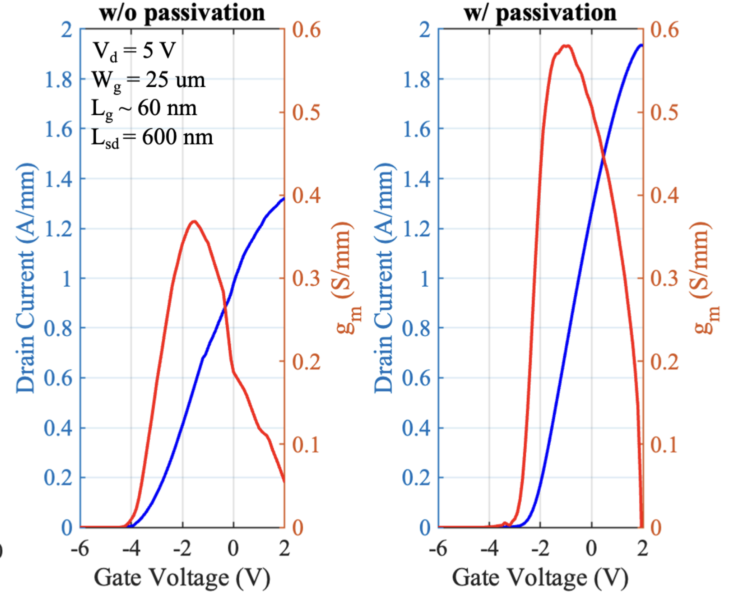

Figure 3.2: Transfer I_d-V_g curve with and without passivation.

N_2 gas with power of 10 W, followed by 3 minutes SiN_x deposition with SiH_4 and NH_3 as precursors under the power of 100 W. More details about the recipe could be found in Appendix D. After the passivation, standard contact hole etching was performed. The SiN_x film optical property was characterized by co-loaded Si piece via ellipsometry, showing an index of refraction of 2.01 at a wavelength of 633 nm, indicative of a Si-rich SiN_x film.

The passivation effect of current recipe is shown in the Fig. 3.1, Fig. 3.2 and Fig. 3.3. An increase of saturation drain current density from 1.5 A/mm to 1.9 A/mm under 2 V gate bias is observed. Meanwhile, the comparasion in transfer IV curve also demonstrates an improvement of transconductance g_m from 0.36 to 0.58, along with a thresthold voltage shift from -4 V to -3 V. All these observations highlight the effect of passivation on removing surface extra charges. However, as shown in Fig. 3.3, the dispersion does not change much after passivation, the reason for this is still under investigation. One

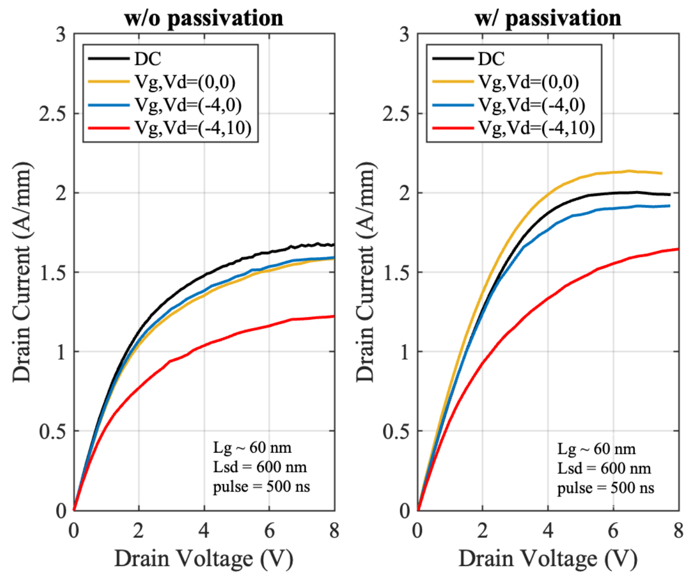

Figure 3.3: Pulsed I_d-V_d curve with and without passivation.

hypothesis is that there might be other mechanisms rather than surface states that are responsible for this dispersion.

CHAPTER 4

SUMMARY AND FUTURE WORK

This study contributes to the understanding of the surface/interface states, as well as insulator materials in GaN-based transistors. The fabrication and characterization of metal-polar MOSCAPs were demonstrated in the first part. The effects of different insulator stacks and process treatments were investigated based on two popular high-k dielectric materials, Al_2O_3 and HfO_2. The thickness-dependence of dielectric constant of HfO_2 was discovered and explained with assumption. Besides, it has been found that Al_2O_3/HfO_2 bilayer is helpful to reduce gate leakage current and critical field of insulator materials, taking advantage of the large bandgap and conduction band offset of the Al_2O_3. The limitation of this structure is also clear, the overall dielectric constant will drop compared with HfO_2 film only due to the incorporation of relatively low-k material Al_2O_3. Furthermore, our study highlights the method using UV/Ozone to oxidize the surface of GaN into Ga_2O_3 as a transformation layer to decrease interface trap states between insulator and semiconductor. In the other hand, in-situ plasma clean also serves as a potential approach to increase interface quality, but it requires further optimization in our case. For future work, first suggestion is to continue the research on optimization options. For example, investigate the influence of different chemical clean, including $(NH_4)_2S$ and piranha solution; further optimize in-situ plasma recipe; try post deposition annealing within suitable temperature windows to crystalize the insulator materials and observe its effects on dielectric constant as well as the gate leakage current. The other suggestion to transfer current technology to other platforms, like N-polar or p-channel GaN. The details would be different from what is illustrated in this thesis, but the main direction would be the same.

In part two, NH_3 plasma assisted SiN_x passivation via PECVD has been developed and discussed. Based on the Hall measurements on metal-polar AlN/GaN/AlN as-grown samples, both in-situ NH_3 plasma clean and SiN_x film deposition showed the same trend to increase carrier concentration and decrease the sheet resistance, indicative of successful passivation of surface states. Then the passivation was performed on metal-polar AlN/GaN/AlN quantum well HEMTs. Both output I_d-V_d measurement and transfer I_d-V_g measurement demonstrated improvement in maximum drain current after passivation. Meanwhile, peak transconductance also increased by around 60 % compared with the unpassivated samples. Although these observations agreed with the results of test samples, showing a higher quality surface, unacceptable dispersion still appeared in pulsed I_d-V_d measurement. The hypothesis is that there might be other mechanisms rather than surface states that are responsible for this dispersion. So in order to solve this problem, one choice is to continue exploring the reason for this dispersion and keep optimizing recipes to get better results. The other way is to try in-situ passivation. Without exposure to ambient air, less contamination will be induced during the fabrication and the active region of the devices will be properly passivated in this passivation-first procedure compared with the current passivation-last processing.

APPENDIX A

SUMMARY OF THE FABRICAITON DETAILS AND CHARACTERIZAITON RESULTS FROM LITERATURES

Ref	Insitution	Year	Structure	Ex-situ clean
Optimized Pre-Treatment Process for MOS-GaN Devices Passivation	University of Sherbrooke	2014	Al/SiO2/n-GaN	85%KOH+40%HCl, each for 2 min
Characterization of interface and border traps in ALD Al2O3/GaN MOS capacitors with two-step surface pretreatments on Ga-polar GaN	University of California, San Diego	2014	Pd/Al2O3/n-GaN	1:3 23%(NH4)2S:deionized H2O for 30 min at 50 C
Interface trap characterization of Al2O3/GaN vertical-type MOS capacitors on GaN substrate with surface treatments	Shenzhen University	2018	Au/Ni/Al2O3/n-GaN	HF:H2O (1:5) for 3 min at RT+(NH4)2S:H2O (1:5) for 30 min at 70 C
GaN MOS Capacitors and FETs on Plasma-Etched GaN Surfaces	Rensselaer Polytechnic Institute	2009	Al/SiO2/n-GaN	1:1 H2SO4:H2O2 for 10 min + 1:3 HCl:H2O for 3 min, chlorine-based inductively coupled plasma (ICP)
Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices	Sandia National Laboratories	2021	Au/Ti/SiO2/n-GaN	NA
Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices	Sandia National Laboratories	2021	Au/Ti/Al2O3/n-GaN	10:1 HF
Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices	Sandia National Laboratories	2021	Au/Ti/HfO2/n-GaN	NA
Effect of GaN surface treatment on Al2O3/n-GaN MOS capacitors	Kansas State University	2015	Au/Ni/Al2O3/n-GaN	piranha (H2O2:H2SO4 1:5)
Influence of carbon impurities and oxygen vacancies in Al2O3 film on Al2O3/GaN MOS capacitor characteristics	Nara Institute of Science and Technology	2018	Al/Al2O3/n-GaN	HF and HCl for 3 min
Highly suppressed interface traps of Al2O3/GaN through interposing a stoichiometric Ga2O3 layer	King Abdullah University of Science and Technology (KAUST)	2022	Au/Ni/Al2O3/n-GaN	piranha + HF for 2.5 min, pulsed laser deposition (PLD) 3 nm Ga2O3
Investigation and optimization of HfO2 gate dielectric on N-polar GaN: Impact of surface treatments, deposition, and annealing conditions	Umich	2021	Au/Ti/HfO2/n-GaN (N-polar)	(1:5) diluted piranha etch + (1:50) diluted BHF solution
Capacitance-voltage characterization of interfaces between positive valence band offset dielectrics and wide bandgap semiconductors	UCSB	2013	Au/Al/Al2O3/n-GaN	NA
Capacitance-voltage characterization of interfaces between positive valence band offset dielectrics and wide bandgap semiconductors	UCSB	2013	Au/Al/Al2O3/n-GaN	NA

In-situ clean	Dep method	PDA	k
NA	16 nm PECVD SiO2 (SiH4, N2O, N2, 900mTorr, 30W, 300C)	30 sec 600 C in N2, I only	NA
Cyclical exposure to TMA and hydrogen plasma	8 nm ALD Al2O3 (300C)	NA	NA
NA	10 nm ALD Al2O3 (TMA, H2O, 300C)	NA	8.9
NA	65 nm PECVD SiO2	30 min 1000 C for I, 30 min 400 C for all	NA
NA	100 nm PECVD SiO2	30 mins 850 C in air, I only	NA
NA	100 nm ALD SiO2	30 mins 850 C in air, I only	NA
NA	100 nm ALD Al2O3	30 mins 850 C in air, I only	NA
NA	100 nm ALD HfO2	NA	8
NA	50 nm ALD Al2O3 (DMAH)	high-pressure water vapor annealing (HPWVA) at 400 C and 0.5 MPa for 30 min	7.6
NA	15 nm ALD Al2O3 (TMA, O2)	5 mins 500 C in N2 for all	7
5 cycles of ALD TMA/N2 plasma at 250C	20 nm thermal ALD HfO2	1 min 400 C in O2, I only	15.9
NA	25 nm ALD Al2O3	NA	NA
NA	25 nm MOCVD Al2O3	NA	11

Gate leakage at 3MV/cm	Critical field	Dit method	Dit at 0.1(0.15)/0.3 eV	Nit	Notes
NA	NA	Terman	NA/2e10 cm-2 ev-1	NA	effective charges density: 4e10 cm-2
NA	NA	Terman	9e11 cm-2 ev-1 at 0.5 eV	NA	border trap density: 2.5e19 cm-3 ev-1
NA	NA	Terman	3.5e12/2.5e11 cm-2 ev-1	NA	border trap density: 1.7e11 cm-2
NA	NA	UV illumination CV	NA/NA	5.8e12 cm-2	fixed oxide charges: 6.6e12 cm-2
1e-8 A/cm2 at 4MV/cm	5 MV/cm	NA			
1e-10 A/cm2 at 4MV/cm	7.5 MV/cm	NA			
1e-8 A/cm2 at 4MV/cm	2 MV/cm	NA			
NA	NA	Photon-CV	1.2e13/4e12 cm-2 ev-1	NA	electron trap density: 1.6e11 cm-2 eV-1
1e-7 A/cm2	NA	Conductance	NA/1.5e10 cm-2 ev-1	NA	NA
NA	NA	Conductance	2.4e10 cm-2 ev-1 at 0.36 eV	NA	NA
NA	3.14 MV/cm	Photon-CV	6.5e12/2e12 cm-2 ev-1	NA	interface states: 1.5e12 cm-2
NA	NA	Photon-CV	1e13/6e12 cm-2 ev-1	NA	total charges: 9.7e12 cm-2, border trap charges: 9.9e12 cm-2
NA	NA	Photon-CV	5e12/3e12 cm-2 ev-1	NA	total charges: 1.4e13 cm-2, border trap charges: 7.2e11 cm-2

APPENDIX B

PROCESS FLOW FOR MOSCAPS FABRICATION

Step	ALD + Gate Contact
1	Sonicated Acetone and IPA, 3 mins each, N2
2	**Pretreatment** for ALD
3	**Deposit dielectric layer** via FlexAL (~10 nm)
4	**RTA** with different temperature, ambient
5	Spin nLOF2020, 7000 7000 30s
6	Bake 115 C, 60 s
7	**Pattern with QVS_TE** mask using stepper
8	Bake 115 C, 60 s
9	Develop in MIF 726, 60 s
10	Optical microscope to observe the pattern
11	Glen 1000 Resist Strip, recipe 3, active mode, 100 100 120 s
12	**Deposit Ti/Ni** (50 nm/60 nm) via odd-hour evaporator
13	Remove PR via sonicated 1165, acetone, IPA, 5 mins each, N2

Step	Mesa Etching
14	Profilometer height check
15	**Etch Oxide** via PT770 using XING1 recipe
16	**Etch GaN** (~850 nm) via PT770 using XING1 recipe
17	Profilometer height check

Step	Ohmic Contact
18	DI water, Sonicated Acetone and IPA, 3 mins each, N2
19	Spin nLOF2020, 7000 7000 30s
20	Bake 115 C, 60 s
21	**Pattern with QVS_BE** mask using stepper
22	Bake 115 C, 60 s
23	Develop in MIF 726, 60 s
24	Optical microscope to observe the pattern
25	Glen 1000 Resist Strip, recipe 3, active mode, 100 100 120 s
26	**Deposit Ti/Au** (50 nm/100 nm) via odd-hour evaporator
27	Remove PR via sonicated 1165, acetone, IPA, 3 min each, N2

APPENDIX C

SCRIPTS USED FOR 1D POISSON SIMULATION

Dielectric material parameters for simulation:

```
Al2O3   binary   GaN    Aluminum oxide on GaN
0.000E+00  0.000E+00  0.000E+00  0.000E+00
eg=8.9
dec=2.1
er=9.0
ed=0.0
ea=0.0
edd=0.0
eda=0.0
me=0.5
val=1.0
mh=0.8
mlh=0.4
mhso=0.8
eso=1.0
emo=0.0
hmo=0.0
tn=0.0
tp=0.0
pol=0.0
al=0.0
end Al2O3
```

```
HfO2   binary   GaN     HfO2 on GaN
0.000E+00  0.000E+00  0.000E+00  0.000E+00
eg=6.1
dec=1.1
er=12
ed=0.0
ea=0.0
edd=0.0
eda=0.0
me=0.11
val=1.0
mh=0.8
mlh=0.4
mhso=0.8
eso=1.0
emo=0.0
hmo=0.0
tn=0.0
tp=0.0
pol=0.0
al=0.0
end HfO2
```

Scripts for band diagram and C-V simulation:

Sample 1

```
# HfO2/GaN MOSCAPs

surface  schottky=2.3 v1
HfO2     t=93    no electrons no holes
Sheetcharge =  1.6875e13  #Charges of SP in GaN
GaN      Nd=2e17  t=8000  no holes
GaN      Nd=3e19  t=3000
substrate

fullyionized
v1 0
temp=300K
dy=1
```

Sample 2

```
# HfO2/GaN MOSCAPs

surface  schottky=2.3 v1
HfO2     t=230    no electrons  no holes
Sheetcharge =  1.6875e13 #Charges of SP in GaN
GaN      Nd=2e17  t=8000  no holes
GaN      Nd=3e19  t=3000
substrate

fullyionized
v1 0
temp=300K
dy=1
```

Sample 3

```
# HfO2/Al2O3/GaN MOSCAPs

surface  schottky=2.3 v1
HfO2     t=70    no electrons  no holes
Al2O3    t=32   no electrons  no holes
Sheetcharge =  1.6875e13 #Charges of SP in GaN
GaN      Nd=2e17  t=8000  no holes
GaN      Nd=3e19  t=3000
substrate

fullyionized
v1 0
temp=300K
dy=1
```

Sample 4

```
# HfO2/Al2O3/GaN MOSCAPs

surface  schottky=2.3 v1
HfO2     t=95    no electrons  no holes
Al2O3    t=24   no electrons  no holes
Sheetcharge =  1.6875e13 #Charges of SP in GaN
GaN      Nd=2e17  t=8000  no holes
GaN      Nd=3e19  t=3000
substrate

fullyionized
v1 0
temp=300K
dy=1
```

APPENDIX D

RECIPE DETAILS OF NH_3 PLASMA ASSISTED SIN_x PASSIVATION USING PECVD

SiN Passivation

Step ***Always run the recipe once before actual deposition to season the chamber***

insert 5 blank steps between PUMP and SiN deposition step

Step		
1	PUMP	leave as default
2	HEAT	leave as default
3	PUMP	leave as default
4	**NH3/N2 preclean** 10 minute NH3 = 100 sccm N2 = 100 sccm press = 1900 mTorr power = 10 W	
5	PUMP	
6	N2 purge 30 sec N2 = 2000 sccm press = 1900 mTorr power = 0	
7	PUMP	
8	**SiN deposition** X minute SiH4 = 25 sccm NH3 = 30 sccm N2 = 1425 sccm pressure = 1900 mTorr Power = 100 W	
9	PURGE	
10	PUMP	

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