TIMING SYSTEM ANALYSIS AND DESIGN FOR CRYSTAL-LESS LOW POWER IMPULSE-RADIOS

A Dissertation

Presented to the Faculty of the Graduate School

of Cornell University

In Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

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August 2012

TIMING SYSTEM ANALYSIS AND DESIGN FOR CRYSTAL-LESS LOW POWER IMPULSE-RADIOS

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Cornell University 2012

Low power radios enable ubiquitous sensor networks that can be used for a variety of applications, such as biomedical monitoring, environmental sensing and intrusion detection. However, existing transceivers have been unable to demonstrate low enough power consumption to fully realize these applications. Low duty cycle impulse radio can offer significant power savings by allowing the transceiver to be turned off between bits. Ensuring that two nodes are sufficiently synchronized to duty-cycle in this fashion is a significant challenge. To solve this problem we used pulse coupled oscillator (PCO) scheme of Mirollo and Strogatz. We performed extensive simulation of the PCO network under a realistic radio parameter space and found synchronization to be robust. We then implemented a low power, aggressively duty-cycled dual-band IR-UWB transceiver in an IBM 90nm CMOS process based on this synchronization mechanism. The transceiver features an energy-detecting front-end, a relaxation oscillator based PCO and a precise edge locking PLL for time bin generation. The time-bins provide our system with 123 unique channels that can be used for multiple access.. We constructed a FPGA based test and measurement setup and implemented a synchronization management finite-state-machine on microprocessor. The PCO network is shown to synchronize nodes robustly with experiments confirming the results of our simulations. We found that the synchronization management scheme allows a four-node system to remain synchronized with duration-of-synchronization

on the order of one second when using 30ns RF-on time windows in a 7.2μs frame. As a result of this aggressive-duty cycle of 0.8%, the total transceiver power consumption is reduced to 119uW while actively communicating. We were able to demonstrate functional radio links transmitting packets of upto 1200bit length over a meter range, proving the viability of the concept. Finally we perform an analysis of a simplified theoretical model of the system which provides fundamental limits to the size of the network that can be supported and the data throughput that can be achieved. The analysis shows that the scheme offers significant power savings benefits for up-to ten nodes if bit-error-rate can be sufficiently controlled.

BIOGRAPHICAL SKETCH

Xiao-Yu Wang was born July 9th 1984 in Jinan, Shandong Province in the People's Republic of China. He immigrated with his mother in May 1987 to Los Angeles, California where his father was a graduate student at the University of Southern California. He lived in the Los Angeles area for the next 18 years, developing a taste for ethnic cuisine and attended college locally at the California Institute of Technology from 2001-2005. At Caltech, Xiao studied Electrical Engineering, spending many a late-night/early morning in the sub-basement of Moore Laboratory working on various problem sets and lab assignments. He did not have a chance to frequent the renowned night-life of Pasadena California much, graduating shortly before his 21st birthday and leaving to the remote town of Ithaca, NY shortly thereafter where he saw real snowfall for the first time in his life. At Cornell University Xiao demonstrated the ability to take his sweet time on things, working on a single project that is the subject of this thesis from August 2005 to the week before he departed in June 2012. At Cornell Xiao spent the vast majority of his time in Duffield Hall, mastering the wonderful world of Cadence, PCB design, and Verilog, C and MATLAB coding. At this point he is hopefully ready to become a productive member of society.

To My Father, Mother, Grandmother and Sister

ACKNOWLEDGMENTS

I had come to Cornell and Ithaca, NY not long after my 21st birthday, a California boy transplanted away from the area that he had grown up in for the first time into somewhere entirely different. It's hard to believe in a way that I'm finally leaving this place after seven great years… and it had taken seven because I suppose that I was happy here and never in a hurry to leave at all. I've had the chance to learn so much and grow so much during my time here, both personally and academically. None of this would have been possible without the support of great friends and teachers during my time here.

I've had the privilege of taking great classes under professors who truly cared about the teaching aspect of their craft: Edwin Kan, Ehsan Afshari, Jiwoong Park, Steven Strogatz, Alex Gaeta, Tim Healey, Richard Rand, Mircea Grigoriu. Having such an open-ended problem for my dissertation research required learning how to think from the very basics, and without the guidance of the people above, it would have been immeasurably difficult to pick up those vital skills. So to them I give my sincerest thanks.

The lab has always been a great environment to discuss and foster ideas I would like to acknowledge everyone I had the pleasure of interacting with as my fellow group-mates during my time here: Anand, Zhongtao, Tony, Silvia, Mustansir, Bo, Carlos, Wacek, Ishita, and Bye-Sah. My gratitude also extends to the M.Eng and undergrad students that have helped me extensively: Brent Watson, Marco Zhang and especially Yi Zhuang and Michael Lyons. Special thanks go out to Rajeev Dokania, whose addition and contributions to the project I had been working on was absolutely vital to its ultimate success. I couldn't have done it without you buddy and you should know that.

I would also like to thank my special committee members Ehsan Afshari and Ao (Kevin) Tang at my B exam, and Al Molnar and Steven Strogatz at my A exam for generously volunteering to spend some of their undoubtedly precious time on me, many times on very short notice.

Of course, the most vital person to this process is my advisor Alyssa Apsel. I am forever grateful to her for not once having to worry about funding. I realize that many students don't have this sort of luxury and it's only possible because of her diligence. She is a truly good person who cares greatly about her students and in this way I was very fortunate to have her.

A person grows not just academically but also personally and spiritually through the people they have the fortune of sharing a friendship with. I've been fortunate also to make many great friends these seven years and grow through them. Milos Sugovic, Felix Lee, Jonathan Shaw, Kate Tang, Chen Chen, Paul George, Laura Fegley, Jared Strait, Haining Wang, Josh Phelps, Piku Ghosh, Gary Peng, Avtar Singh, Srich Murugesan, Rajni Singh, Boram Kim, LiHong Herman, Steve Kim, Eugene Hwang, Makoto Bentz, Fedor Dokshin, Kwame Amponsah, Lillian Hsu , Nichole Nadermann and Jing Ning. I'm sure I'm missing names here so I apologize for any omissions.

Above all none of this would have been possible without the never-ending support I have received all these years from my family. My mother and father, whose hard work and dedication to making our family's lives better was an unbelievably effective example growing up. To my sister who has grown to be quite a sharp and mature young woman. And finally to my late Grandmother who left behind the world she knew to come to this strange country to watch over my sister and myself while we grew up.

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LOW POWER WIRELESS NETWORKS AND SYNCHRONIZATION

1.1 Wireless Sensor Networks

Wireless technology has seen remarkable development and proliferation in the past decade. Driven by advances and scaling in integrated circuit technology - the ever-cheapening cost of computation due to the miniaturization of transistors - integrated wireless transceivers have become cheap enough to be nearly ubiquitous. Popular wireless standards, such as GSM, CDMA, LTE, Wifi 802.11a/b/g/n, GPS, and Bluetooth have become an affordable and essential part of our everyday lives to the point that we have become hard-pressed to remember a time without them.

While the technologies listed above are undoubtedly useful, an exciting new frontier that has yet to be fully developed is in the area of ultra-low-power wireless communication systems. These systems are envisioned to consist of many distributed radio nodes containing some form of integrated sensor that communicate within an ad-hoc network. Each node is expected to be very small, very cheap and communicate over a short range. These type of systems have many potential applications, some examples of which are:

- Health Care: Current electro-cardiogram (ECG) systems are wired skin patches that greatly restrict the patients freedom of movement. A wireless system would be far less cumbersome and would allow more consistent patient monitoring as well as provide immediate alerts for emergency situations.
- Environmental Monitoring: Wireless nodes may be deployed en-masse in a large field to detect the presence of toxins and contaminants. They may also be used in

scientific experiments such as field studies of animals where the nodes may be placed for a long time in a minimally intrusive way.

- Intrusion Detection and Security: Radio nodes may be deployed on the perimeter or interior of a high value space that requires constant surveillance or monitoring. A distributed wireless solution could greatly reduce the cost of implementing such a system.

Since these ad-hoc networks can become very large in number – possibly scaling to hundreds or even thousands of nodes – *low cost* and *energy efficiency* become the overriding design goals. More traditional considerations in wireless networking, such as spectral efficiency and overall network throughput, are much less important. This places stringent design specifications on all aspects of the transceivers. This includes the energy source (energy-scavenging or energy-storage), the sensor, the radio transceiver, processor/microcontroller and finally to the medium-access control and networking algorithms. All the aforementioned areas are critically important to the successful implementation of any such system and have been an active area of research throughout the past 5-10 years. Being primarily an analog circuit design research group, our interest, and the focus of this dissertation, is in the implementation and improvement of radio transceivers targeting this application space. In the rest of this chapter, we will provide a brief introduction to the power requirements needed in implementing these low power transceivers

1.2 Transceiver Specifications for Wireless Sensor Networks

Table 1.1: Power Densities of available energy sources [1][2]

Energy Type	Power Density $\left(\frac{\mu W}{cm^3}\right)$ @ 1 year	Lifetime (100μW)
Lithium Battery	100	1 year
Micro Fuel Cell	110	1 year
Solar Cell	10-15000 $\left(\frac{\mu W}{cm^2}\right)$	∞
Vibrational Converter	375	∞
Air Flow	380	∞
Temperature Gradients	50	∞

Since the overriding design criteria in wireless sensor network (WSN) applications are low cost and small size, significant limitations in form factor and energy storage exist. The small size of the nodes limits the amount of energy storage or energy generation to $1cm^3$. Roundy [1] and Otis [2] performed the earliest surveys on the lifetime and power requirements of WSN nodes based on the form factor requirement and available energy technology. Their findings are summarized in Table 1.1. If pure energy storage is used, transceivers can consume no more than 100μW on average for operating lifetimes of 1 year. If the energy storage system is supplemented with energy harvesting sources such as solar cells or vibrational energy converters, then the node operating lifetime can be extended indefinitely. Nevertheless, these energy scavenging sources also have power generation capabilities on the order of $100\mu W/cm^3$ and the node average power consumption can, as a result, not exceed this amount.

While the power consumption requirements are a significant challenge certain aspects of transceiver design for WSN are less stringent than traditional wireless systems. The most significant of these are the low-data rate requirements. Wireless

sensor network nodes individually do not need to transfer a large amount of data. For example, in environmental sensing and intrusion detection, data transfer occurs only sporadically in response to actions that are sensed by the node. When data transfer occurs, only a few short packets (~200b) need to be generated by any given node. Even for applications such as portable EKG which need a constant stream of real-time data, the rate required is still less than 100Kbps [3]. Furthermore, since the application space assumes a high node-density, the individual radio nodes only need to communicate at ranges of 1-10 meters. The combination of low-data rate and low range of communications makes traditional metrics such throughput and channel utilization relatively unimportant in WSN applications.

Figure 1.1 is an overview of the active power consumption of modern transceivers, including both established commercial radio standards (802.11a, Bluetooth, Zigbee) as well as notable works in the academic literature. Receiver only implementations such as by Lee [4] and Pletcher [5] are marked with an asterisk*. We see that the commercial transceivers' power dissipation is in the range of 10mW – 1W, while even the lowest power transceivers from the academic literature are in the range of 1mW. Pletcher's receiver-only implementation draws only 52μW but is designed to be an always-on wake-up receiver that is part of an asymmetrical data-link where the transmitter transmits more power. Thus it is not a truly ad-hoc solution and it is unclear if the transmitter can also be designed for low power. Figure 1.1 also indicates that high energy-efficiency, in terms of $\frac{\text{Joules}}{\text{bit}}$ is easier to achieve at high data rates as opposed to low data rates. This is due to static power consumption in the oscillators and amplifiers of any radio system which exists regardless of data rate. In low power architectures such as [7], this static power is reduced through clever circuit techniques and careful optimization but can never be fully eliminated

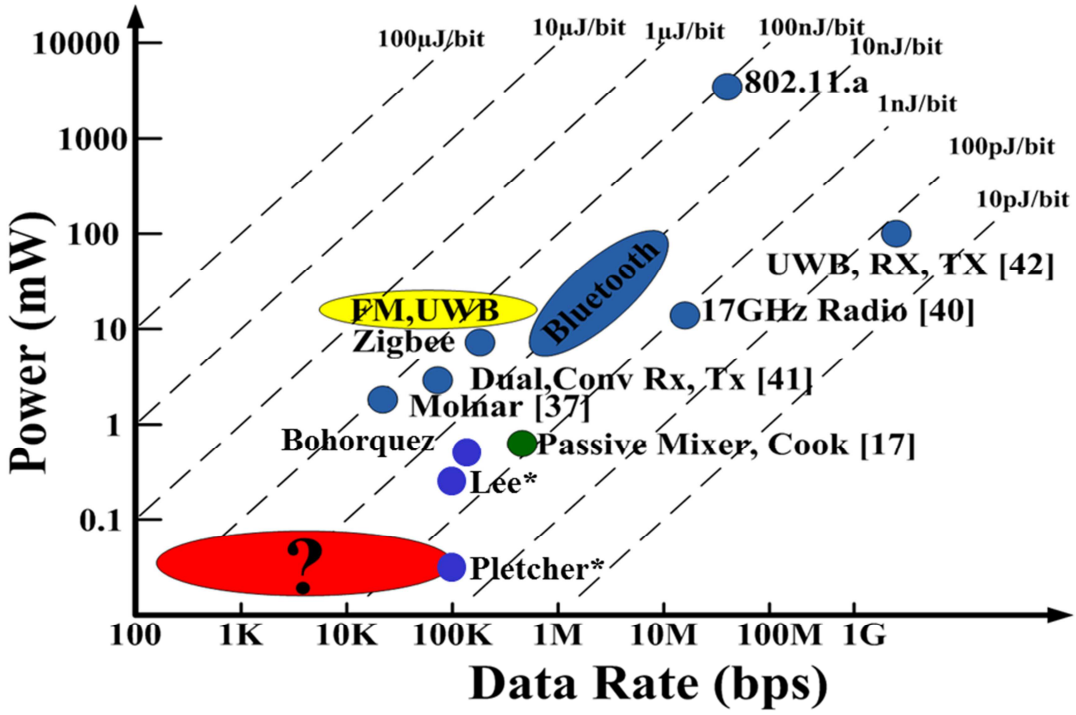


Figure 1.1. Summary of power consumption in modern transceivers. Adapted from [6][28]

1.3 Overview of Past Works in Low-Power Transceivers

Broadly speaking, low power transceivers targeted towards WSN applications target energy-efficiency and low active power consumption while minimally satisfying requirements for sensitivity (so that range is sufficient) and compliance with some form of spectral mask (so that the device can be legally sold and operated). Since these requirements are quite broad, there are many possible ways to implement them. However, implementations generally fall into three distinct types of architectures: energy-optimized traditional I-Q radio architecture, the super-regenerative energy detection architectures, and impulse UWB architectures. We will briefly summarize each type of architecture and recent significant works implementing them.

1.3.1 Optimized Traditional I-Q Radio Architectures

Traditional I-Q radio receiver architecture employs two consistent elements: the use of *amplification* through gain stages and frequency conversion with 90° quadrature VCO oscillators. This type of architecture generally targets the ISM bands at 900MHz or 2.4GHz and outputs in-phase and quadrature signals at an intermediate frequency (IF). Optimization for this type of architecture for low-power WSN applications involves defining the system level parameters, such as modulation-type, in a way that relaxes circuit-level specifications for the receiver and transmitter. Notable examples of this are the works of Cook [7], Molnar [8] where wide spacing 2-FSK is used, trading off spectral efficiency for ease of implementation. Other examples of this are in the energy-detecting uncertain IF architectures of Pletcher [5] and Drago [9], where there is a very relaxed specification of the IF frequency, allowing wider process variation in the local oscillators of each transceiver. These types of systems also emphasize power optimizing the individual components through techniques such as current re-use through component stacking [8]. In recent years, it has been shown that using a passive-mixer first architecture can both reduce power consumption by allowing the gain stages to be designed at lower frequencies while also achieving a suitably low noise figure and a wide ranging input match [10].

1.3.2 Super-regenerative Architectures

While super-regenerative receiver (SRR) architectures were first invented by Armstrong in the 1920's [11], in recent years they have recently seen a resurgence in popularity in integrated designs for low-power WSN applications. The super-regenerative architecture features a receive oscillator biased in weak positive feedback. The RF signal couples to the oscillator, either through an isolation gain stage [2] or directly through the antenna [12], injecting energy into the tank and changing the time

it takes to reach a critical oscillatory threshold. The oscillator is periodically quenched (returned to a non-oscillatory state) and bit decisions are based on the time taken for the oscillator to reach a certain threshold. Thus the SRR architectures are fundamentally a form of non-coherent energy detection. SRR architectures are attractive because they do not require much gain at RF and exploit the positive feedback detection to allow active components, such as the oscillator, to be biased at relatively low levels (>400μW). SRR architectures use long quench periods and narrowband signaling (~500KHz bandwidth) and thus, like traditional IQ architectures are also targeted for the ISM bands.

1.3.3 Ultrawideband Impulse-Radio (IR-UWB) Architectures

In 2002, the FCC sanctioned the use of wideband signaling in the unlicensed 0-1GHz or 3.1-10.6GHz bands provided the transmissions adhere to a spectral mask. In IR-UWB, transmissions consist of 2ns wide Gaussian-like pulses. While IR-UWB signaling was originally envisioned to allow high-data rates due to the extremely wide bandwidth of the signaling, significant challenges with multi-path in the indoor propagation environment in practice limit its usability in that space. A recent development that has gained traction over the past few years has been the use of impulse signaling in short-range, low-power WSN applications. These transceivers use wideband gain stages at RF coupled with non-coherent energy detection. Modulation in these systems is either pulse-position-modulation (PPM) [13][14][15] or on-off-keying (OOK) [16][17]. The short pulse times allows the transmitter to be implemented at very low average power [16][17][18]. Due to the need to amplify and detect a wideband signal, the receiver active power consumption is quite high, in the range of 7.5 – 35mW. However, this is offset by the ability to design these transceivers with nearly instantaneous turn-on times of 1-2ns [13][17] since there is no

need to wait for oscillator circuits to stabilize. Energy efficient IR-UWB systems can be designed for rapid burst data transmissions from 20-40Mbps [14][15] with a low power μW level sleep-mode allowing energy savings through packet level duty-cycling, or to be duty-cycled between low rate (100Kbps – 1Mbps) transmissions of the bits themselves [13][16][17]. In this dissertation, we are particularly interested in the latter form of duty cycling, since it offers the opportunity for power savings while actively communicating, potentially reducing or eliminating the need to implement complicated rendezvous schemes to manage wireless nodes' sleep-wake cycles [19].

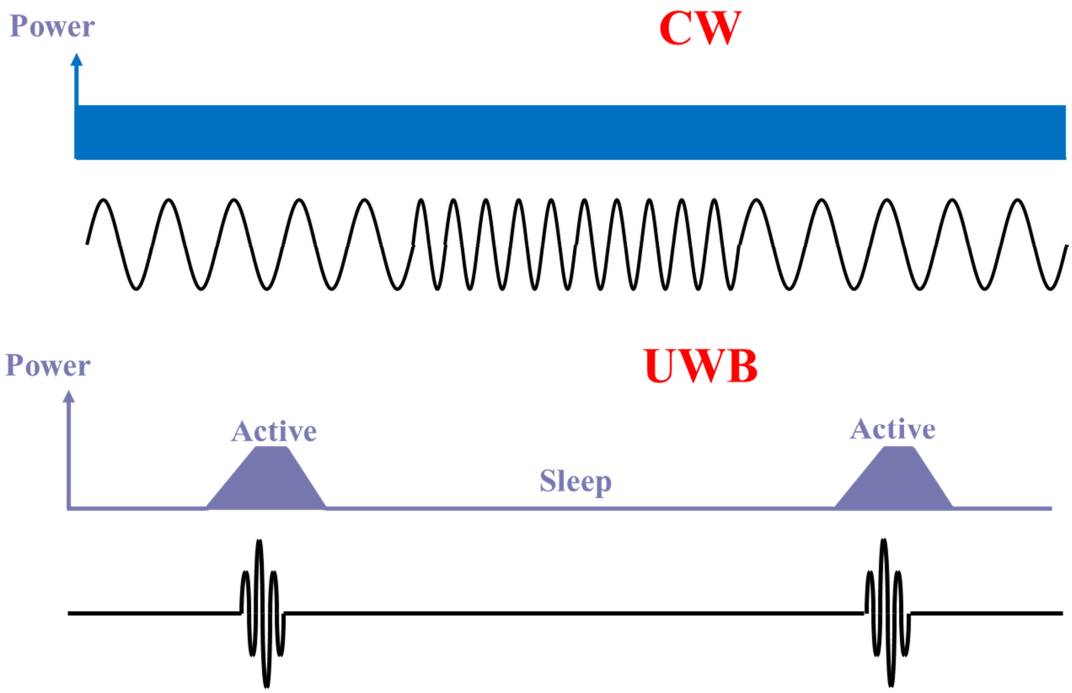


Figure 1.2. Illustration of potential power savings due to bit level duty cycling in IR-UWB vs traditional modulation schemes

1.4 Bit Level Duty Cycling for Power Savings in IR-UWB

The time-limited nature (< 2ns) of IR-UWB transmissions allow the transmitter and receiver circuitry in these systems to, in principle, be duty-cycled at *bit-level,* meaning those circuits only need to be active during bit-transmission and bit-detection. This allows the power savings of duty-cycling while the transceivers are *actively transferring information* as well as the direct tradeoff of data rate vs. power consumption. This type of tradeoff is not possible in traditional continuously transmitted, low-rate modulated signaling such as FSK, where the RF circuitry must be kept on regardless of how slow the data rate is. Intuitively, we would expect the power consumption to look like Figure 1.2. In reality the picture is more nuanced. In narrowband systems, lower data rate implies a lower system bandwidth and a corresponding decrease in the amount of integrated noise, whereas in UWB system, the bandwidth, and hence the noise level, is independent of the data rate. We must account of the possibility that the narrowband continuous wave system does not need to transmit as much power as the UWB system. In [20] my colleague Rajeev Dokania showed that a power optimized IR-UWB TX-RX link employing optimal bit-level duty-cycling consumes substantially less power than the power optimized continuous wave system under the same conditions. In this analysis we assumed that at a degenerate, full data rate of R_0, CW and UWB systems employing the same type of modulation and detectors consume an equivalent power P_{RX0}. We then scaled the two systems' power consumption for a reduced data rate R based on the UWB system duty cycling at transmitter and receiver between bits and the CW system saving power by reducing its transmit amplitude. Dokania derived the following equation relating the relative power consumption of the two systems:

$$\frac{P_{SUM,Impulse}}{P_{SUM,CW}} =$$

$$\frac{\frac{R}{R_0} * \left(2 + \frac{P_{RX0}}{\gamma}\right) P_{RX0} + P_{RXTX,OH} * \frac{R}{R_0} + (P_{RXTX,Leak})}{\frac{R}{R_0} * \left(2\sqrt{\frac{R_0}{R}} + \frac{P_{RX0}}{\gamma}\right) P_{RX0} + (P_{RXTX,OH} + P_{RXTX,Leak})} \quad (1.1)$$

γ is a process dependent scale factor, $P_{RXTX,OH}$ represents static power consumption due to constant operation of essential components such as oscillators and bias circuits and $P_{RXTX,LEAK}$ represents the leakage current which is significant in modern CMOS processes. A plot of Eq. (1.1) in Figure 1.3 shows that duty-cycling in IR-UWB provides a more efficient mechanism for power savings at low-data rates of 50-500Kbps, potentially consuming between 1-10% the power of the equivalently optimized narrowband system.

While the theoretical analysis in [20] shows that bit-level duty-cycling can in principle be an effective tool for lowering power consumption, it also assumed that the duty-cycling can be performed perfectly so that power consumption scales exactly linearly with data rate. This neglects imperfections that exist in the timing circuits, specifically mismatch and phase noise in the transmitter and receiver. Synchronization at the timescales that are needed for significant power savings turns out to be a major challenge. This is further exacerbated by the desire to implement the transceiver at lowest possible cost, which makes eliminating the requirement for an off-chip crystal with precise (<100ppm) specifications extremely desirable [2][9]. As we will see in the next section, bit-level duty-cycling of the type proposed in [20] would seem to be incompatible with the traditional method of synchronization in packet based systems.

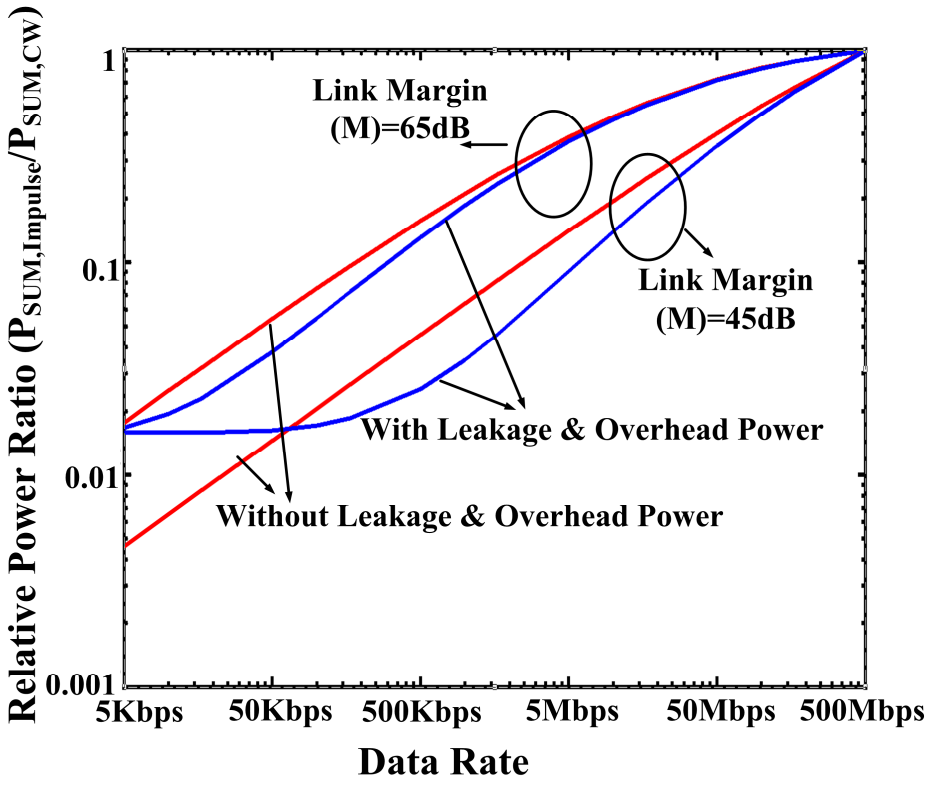


Figure 1.3. Relative power scaling vs data rate for IR-UWB vs CW systems [20]

1.5 Baseband Synchronization in Digital Radio Systems

The transceiver architectures described in section 1.3 are only describe the front-end of the radio system. The outputs of the front end are physical signals that have been converted to a form that can be input into the *baseband*. The baseband is the circuit block that is responsible for extracting data bits from those physical signals. This involves two processes: bit-detection and synchronization. The architectures we detailed in Chapter 1.3 (with the notable exception of [9], which we separately describe) while vastly different in their physical implementations, fit into the traditional baseband paradigm of fixed symbol time for bit detection and burst packet transmissions. In this section we will discuss the importance of using well-matched oscillators (almost always a crystal) within this paradigm. We will see that oscillator

mismatch is a fundamental phenomenon that limits the size of packets that can be transmitted.

1.5.1 Effect of Clock Drift on Digital Baseband Synchronization

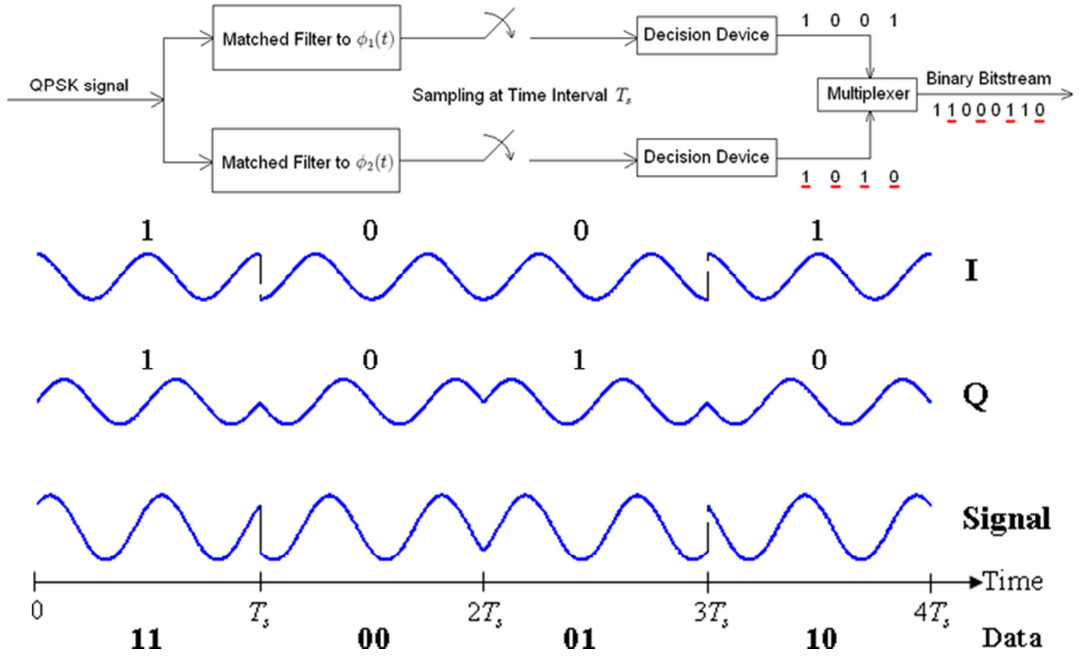


Figure 1.4. Example of a baseband demodulator for QPSK signals [21]

The traditional digital radio receiver has a baseband architecture where an incoming modulated signal is put through input correlator(s) and the result is integrated over the symbol period T_S to arrive at a symbol decision. A symbol can consist of one or more bits, depending on the modulation scheme used. A representative example of the demodulator is shown in Figure 1.4. The data is sent over a packet consisting of many symbol periods (Figure 1.5). In traditional digital transceivers, T_S is assumed to be well-matched between transmitter and receiver

(implying use of an off-chip crystal) so that symbol-level synchronization only requires that the initial phase difference between transmit and receive symbol periods be found and compensated for during the header[1]. However, there is always mismatch between the symbol period of the receiver and the transmitter, which limits the number of symbols that may be transferred in one packet. This time limit may be expressed as:

$$T_{PKT} < \frac{\beta}{\alpha} T_S \tag{1.2}$$

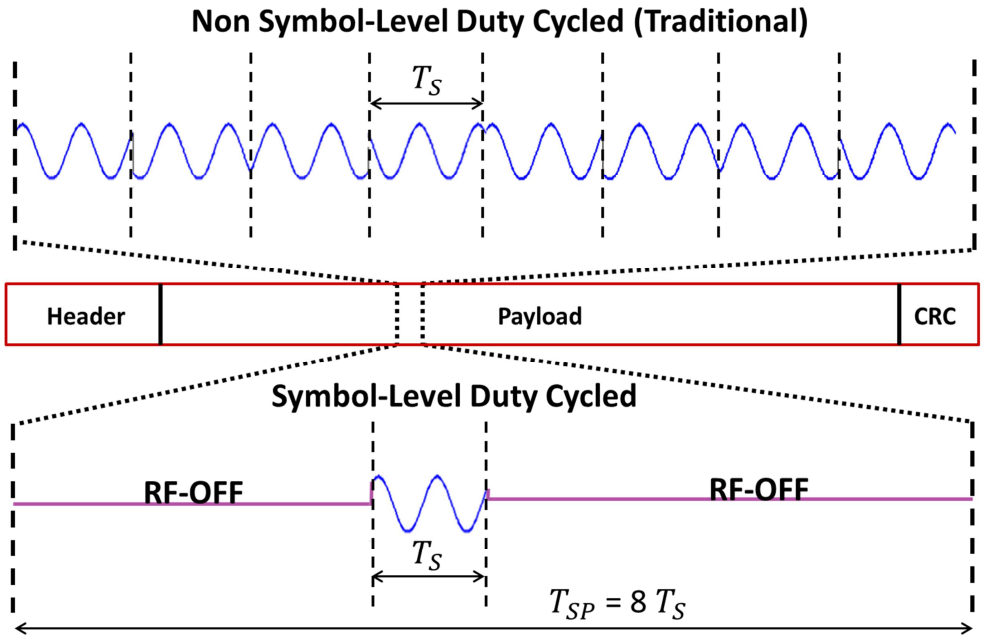


Figure 1.5. Organization of data symbols into a packet for traditional and symbol level duty-cycled cases, d = 1/8.

[1] Other types of synchronization, such as carrier frequency offset estimation may also be performed in the preamble, as in the OFDM 802.11 standards. However, the symbol rate is still a defined parameter in these systems.

$\alpha == \Delta T_S/T_S$ is the finite crystal mismatch between two transceivers and is specified to be between $\pm$20-40ppm in modern communication standards [22][23]. β represents the tolerance in the symbol window timing in the system and is on the order of 10% [9].

In a system where duty cycling is not employed between symbols within the packet, the symbol periods occur with no spacing between them, so that $T_{PKT,ND} = N_{PKT,ND}\, T_S$, where $N_{PKT,ND}$ is the symbol length of the non-duty cycled packet. Thus $N_{PKT,ND} < \beta/\alpha$. If inter-symbol, intra packet duty cycling is employed for active power savings in the fashion proposed in [20], then we have a symbol period, $T_{SP} > T_S$ which may be characterized by a duty-cycle-ratio $d = T_S/T_{SP}$ (Figure 1.5). Thus the packet time becomes $T_{PKT,D} = N_{PKT,D}\, T_S/d$ and $N_{PKT,ND} < d\beta/\alpha$. We find that this duty-cycling scheme leads to a *degradation* of the packet lengths in addition to reducing the overall bit-rate. Radio systems, regardless of their modulation, are clock-mismatch limited to packet payloads up to 1000-2000 symbols [22][23][24] when symbols are sent continuously. Thus, introducing intra-packet duty cycling on the order of 1% in the manner proposed by [20] reduces packet duration to an unreasonably low number of 10-20 cycles within a traditional synchronization framework.

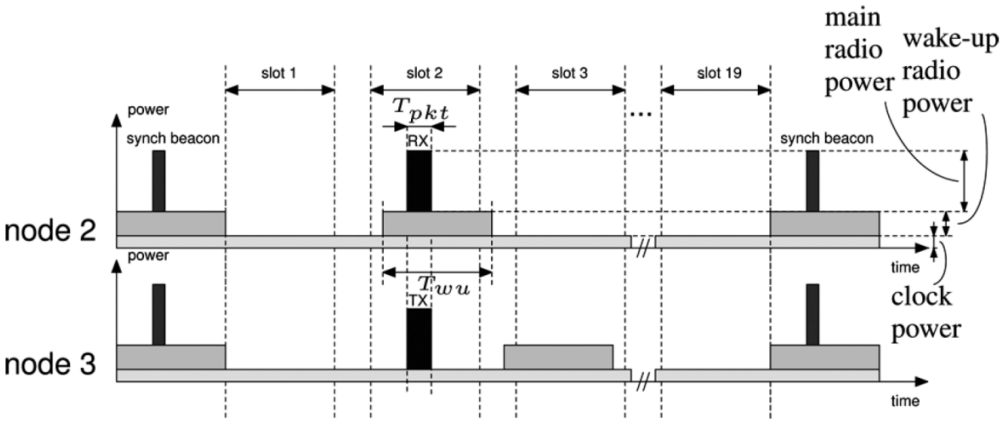


Figure 1.6. Global synchronization to subdivide a time interval into slots for packet transmission [9].

1.5.2 Global Synchronization with Synchronization Beacon Transmissions

An alternative to using well-matched but autonomous oscillators is to create a *globally synchronous* system where a timing beacon is periodically sent throughout the network and all nodes' timings are derived relative to this beacon. The beacon resets the relative phase of all oscillators in the network, so that clock drift due to frequency mismatch only occurs in the time between beacon transmissions. The time between beacon transmissions may then be subdivided into slots for TDMA, as shown in. Nodes are assigned to transmit and listen within the slot only, saving power through duty cycling. This scheme was proposed at packet-level for the 2.4GHz ISM band in the works of Drago et al. MAC-level analysis performed in [9] showed that transceiver symbol-rate clock matching requirements can be reduced to the scale of 0.1-1% with this scheme. Significant design effort was then spent on implementing oscillators to this frequency matching specification [25]. The implemented transceiver front-end was shown in [26]. Since timing in the system is derived from an integrated, CMOS oscillator as opposed to a crystal, the effect of accumulating jitter must be

accounted for over the timescale of the packet, a component of the analysis that was neglected by [9]. In fact, the accumulated jitter over the packet length for the frequency reference in [25] appears to be on the order of the bit-decision period in [9]. This would imply a large error at the output of the correlating bit detector for bits near the end of the packet. We are unaware of any subsequent work addressing this inconsistency. To our best knowledge, results of packet communication tests based on the scheme proposed in [9] were never published, so it is uncertain if it is actually viable in practice. The 0.2Hz beacon rate used in [9] also target extremely low-data rate, latency tolerant applications (10 packets/min at 100b/packet) such as environmental sensing and thus cannot be used for more demanding WSN applications such as portable EKG where a constant stream of higher-rate data is required.

1.6 Contributions of this Dissertation

This dissertation will cover the design and implementation of a transceiver that exploits the wideband characteristics of IR-UWB pulses to create a system that can be duty-cycled within bit transmissions, thereby enabling power savings while actively communicating. The system also overcomes the synchronization problem detailed in Chapter 1.5.1 through the use of global Pulse Coupled Oscillator synchronization. Since the link analysis and front-end design was extensively covered by my college Rajeev Dokania in his dissertation [28], this work will focus on the timing system implementation and the viability of the transceiver synchronization within a wireless radio network. The dissertation is organized as follows:

Chapter 2 will provide an introduction to the Pulse Coupled Oscillator network of Mirollo and Strogatz. This system has been intensely investigated in the field of applied mathematics and non-linear dynamics and is noted for its global synchronization properties. However some instabilities have been noted in the

literature leading to a question as to whether the synchronization is stable if used in a wireless sensor network. We numerically investigate the behavior of the system at timescales relevant to IR-UWB sensor networks and show that the scheme leads to stable synchronization behavior over the realistic parameter ranges. We show that the scheme is able to overcome a wide variety of frequency mismatch if coupling is strong enough and that the synchronization nearly eliminates relative timing jitter. We also describe the implementation and measurement of a first-generation proof-of-concept circuit.

Chapter 3 covers the design, implementation and testing of a communication system based on the PCO synchronization characterized in Chapter 2. The PCO synchronization and UWB signaling are exploited to distribute a global reference clock throughout the system. The time period of the reference clock is sub-divided into time-bins by a phase-locked-loop to form the data channels in our communications system. We perform analysis of the timing system with respect to the synchronization offset and jitter of the PCO and PLL and derive specifications for those blocks. We then describe the design considerations for the circuits that implement the PCO and PLL and their exact implementation. An FPGA based test setup is then used to characterize the synchronization as well as implement a simple demodulator and baseband. Our implementation of a FPGA based finite-state-machine controller also shows that loss-of-synchronization can be recovered. Finally, we demonstrate the overall viability of the system architecture by routing a picture from a source to a destination through two intermediate hops in a four-node network

Chapter 4 draws on the network testing results as a basis for an analytical model for the probability of synchronization. The network is assumed to be in a same state globally and therefore gain and lose synchronization together. The formulation of the model is presented in detail and can be shown to be a Markov chain. Closed form

expressions for the probabilities of the network being in unsynchronized, partially synchronized or fully synchronized states are then derived mathematically. The results for are consistent with our synchronization measurements in Chapter 3. We then derive closed form solutions for the probabilities of successful packet transmission as a function of packet length, thereby establishing the theoretical limits of the synchronization we use.

Chapter 2

PULSE COUPLED OSCILLATOR NETWORK DYNAMICS

2.1 Introduction

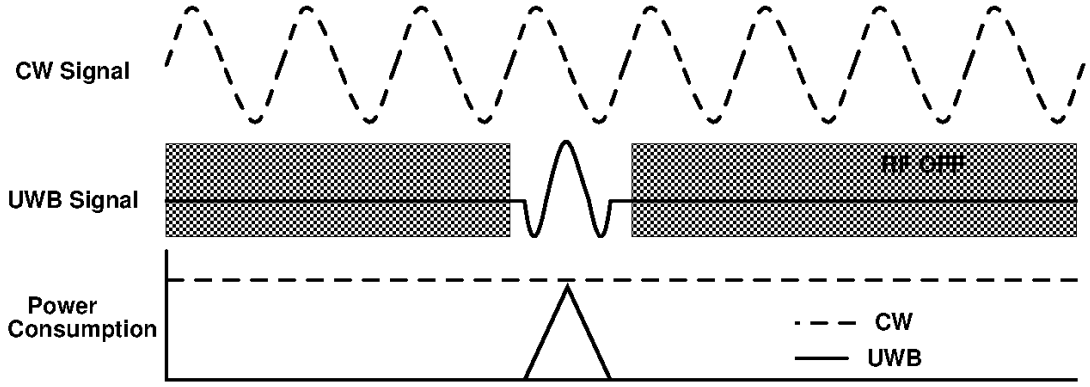


Figure 2.1. Power Savings in IR-UWB systems

In the impulse radio UWB (IR-UWB) scheme, the radio still transmits signals at the same instantaneous power levels as in the CW case. However, because the signal is composed of a short impulse of 1-2ns duration, the *average* power of transmission is much reduced for low data rate systems, since both transmitter and receiver only consume power when actively operating (Figure 2.1).

To communicate correctly in a duty-cycled IR-UWB scheme synchronization between transmitter and receiver is required. Without synchronization, the receiver's duty cycling window will be mistimed relative to the transmitted pulse, causing an error. While recently there have been reasonable synchronization schemes proposed in the literature [4][34], these schemes have only addressed synchronization of two radios [4], or require a master node that only transmits a special synchronization pulse within a localized region [34].Since these schemes are not designed for large multi-hop distributed networks, their scalability is in question.

In this chapter, we show that the Pulse Coupled Oscillator system of Mirollo and Strogatz [35] is a promising scheme for scalable synchronization across an entire network of IR-UWB radio nodes in a cognitive network. Unlike [34], PCO systems do not require a distinctive master node to transmit a synchronization pulse, and instead form a self-organizing network where each node both sends and receives a synchronization pulse. Based on this technique, the radios automatically synchronize, thereby creating a naturally ad-hoc and scalable system that emulates the natural synchronization observed in biological systems. This intrinsic property of the PCO system is particularly well suited for cognitive networks, which are required to be adaptable and easily scalable. We first designed this system for integration on-chip in [36] and [37]. In this paper, we show that the characteristics of the PCO system are particularly well suited for implementation in highly scaled CMOS processes, allowing implementation with simple, low cost analog hardware at acceptable performance levels without the need for off-chip components. We show, through simulation, that for the timescales of low-rate IR-UWB wireless sensor networks, the PCO system does not demonstrate undesirable asynchronous behavior, thereby facilitating aggressive duty cycled pulsed radios. We designed an early implementation of this system in the IBM CMOS9RF process and experimentally demonstrate robust three-node synchronization.

2.2 PCO System Theory – Relevant Results and Considerations

In a seminal 1990 work [35], Mirollo and Strogatz posed a general analytical framework for pulse coupled oscillator systems as a behavioral model for Southeast Asian Fireflies that has subsequently been extensively studied in the fields of mathematics, physics, and non-linear dynamics. The system assumes a network of N

oscillators which interact through impulsive coupling, representing the ``firing" of a firefly. Each oscillator j has an internal state that can be represented by a single phase variable $\phi_j(t)$, which increases in time at a constant rate $\dot{\phi_j} = 1 + \delta_j$, where the parameter $|\delta_j| << 1$ models variability in the natural oscillation period of oscillator j in the absence of coupling. When oscillator j reaches threshold at a time t^*, $\phi_j(t^*) = 1$, and it fires an impulsive coupling ϵ_{ij} to each oscillator i in the network and instantaneously resets so that $\phi_j(t^{*+}) = 0$. The oscillators are assumed to not self couple ($\epsilon_{ii} = 0$) and connectivity between oscillators in the network can be represented by terms such that $\epsilon_{ij} \neq 0$. This impulsive coupling from oscillator j advances the phase of oscillator i by an amount:

$$\phi_i\left(t^* + \tau_{ij}\right)^+ = V^{-1}\left(V\left(\phi_i\left(t^* + \tau_{ij}\right)^-\right) + \epsilon_{ij}\right) \tag{2.1}$$

where τ_{ij} is the time delay from oscillator i to oscillator j and $V(\phi)$ is a voltage-like function determining how much to couple at a given phase of the oscillator (Figure 2.2) If $\phi_i\left(t + \tau_{ij}\right)^+ >= 1$ oscillator i subsequently fires its own coupling to the network and resets to 0. Some works [27] note that a refractory, or blackout period early in the cycle where the coupling is zero (Figure 2.2), is necessary for the network to establish synchronization and avoid positive feedback firing in the presence of propagation delays.

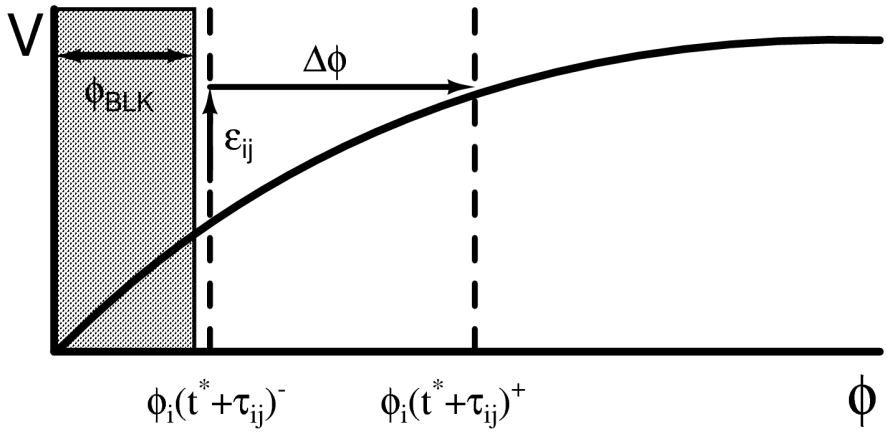


Figure 2.2. Illustration of PCO state function and coupling

In [35], Mirollo and Strogatz investigated the case of equal all-to-all coupling ($\epsilon_{i\neq j} = \epsilon$), uniform natural frequencies ($\delta_j = 0$), and no time delay ($\tau_{ij} = 0$). They rigorously proved that nearly all initial conditions will eventually converge after a transient period t_{sync} to a fully synchronous state $\phi_i(t) = \phi_j(t)\ \forall\ i, j, t > t_{sync}$ provided the following general conditions of the voltage-like function $V(\phi)$ hold.

$$V'(\phi) > 0, \qquad V''(\phi) < 0 \tag{2.2}$$

In the language of non-linear dynamics, this fully synchronous state is referred to as the *period-1 solution*, which is a global attractor for the idealized PCO system and is the single stable state to which all initial conditions converge.

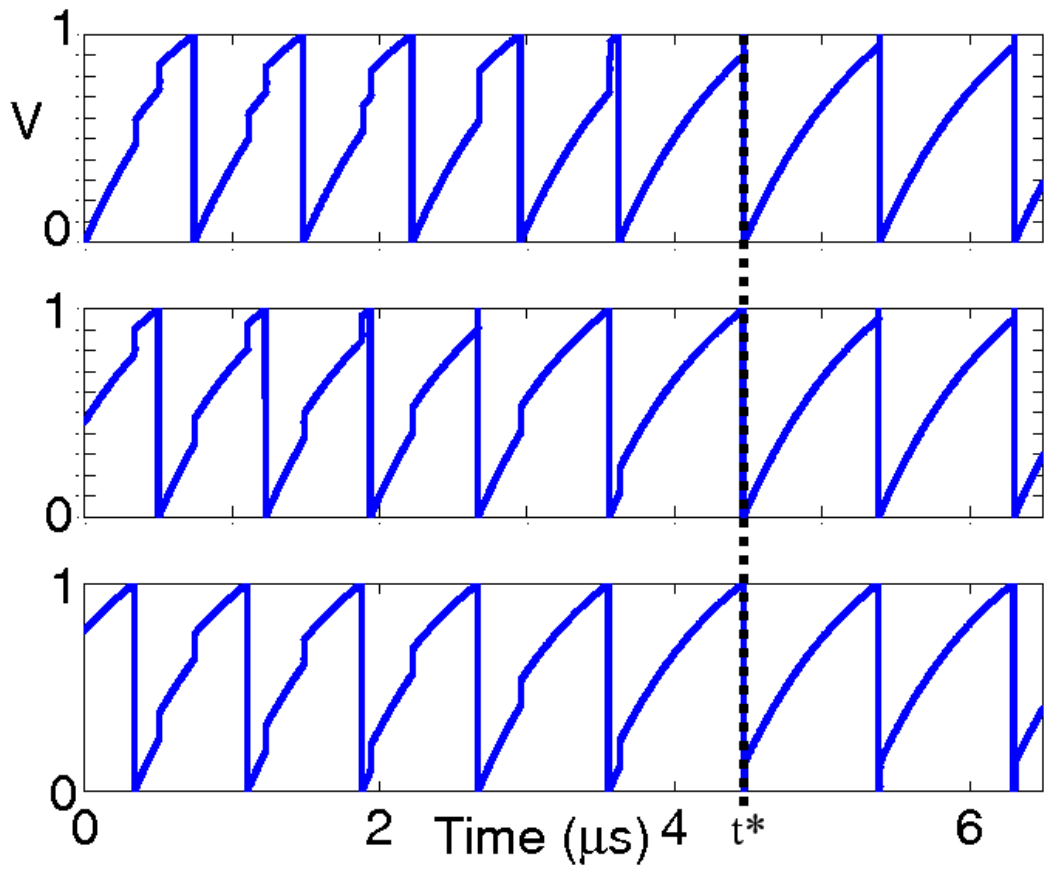


Figure 2.3. Synchronization dynamics in a PCO system with $V_{TH} = 1$. At $t = 0$ the system is initialized with random initial phases and at t^*, the network is synchronized

An illustrative example of the synchronization process of a three PCO system is illustrated in Figure 2.3. At $t = 0$ oscillators are started with random initial phases. When an oscillator reaches the threshold value of $V = 1$, it causes a phase jump of the other oscillators. Each node repeats this process of reaching threshold and coupling to the other nodes, driving their respective phases closer and closer each cycle until at t^* the entire network reaches synchronization. The natural evolution of the system under these simple rules causes synchrony. Impulse radio systems with front ends capable of

distinguishing between two or more pulse types, such as that described in [38] can utilize PCO synchronization to facilitate impulse radio communications. In Figure 2.4, we depict a simple on-off keying (OOK) scheme- illustrating this concept, where a transmitter sends a data pulse a fixed time offset ΔT from the synchronization pulse, and the receiver samples the channel during this time and looks for the presence or absence of this pulse. Previously, we have proposed a detailed system architecture implementing the concept of Figure 2.4 [39]. In this system architecture, the radios only need to be on during the expected pulse arrival, allowing power savings through duty-cycling.

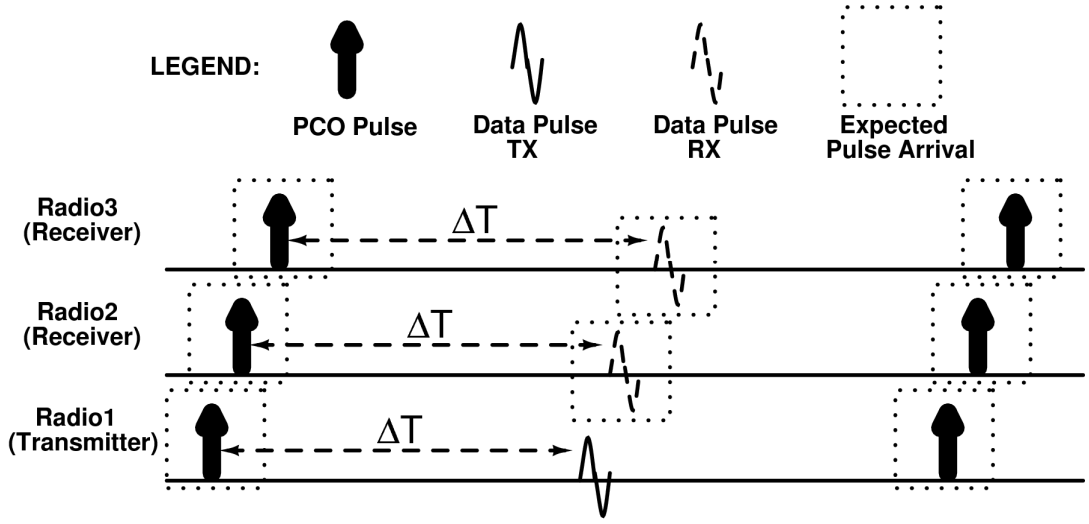


Figure 2.4. Example of Impulse Radio Communications exploiting PCO synchronizations. Data is sent a fixed ΔT from the PCO pulse by a transmitter, where receivers look for the pulse

Although it is not modeled in [35], time delay is unavoidable in realistic sensor network systems, which would couple through a wireless medium, and serves to throw a major complication in the dynamics of the system. The period-1 solution is no longer the only possibility and instead the number of possible equilibriums exponentially

increase with the number of nodes in the system, each attracting some subset of initial conditions [40]. A complete analytical solution becomes totally intractable for the *parameter space* of arbitrary number of nodes, time delays, coupling strengths, frequency mismatches and network topologies. Aperiodic solutions, clustered synchronous solutions and *bifurcations* - sudden changes in the stability of attracting solutions - have been observed in various regions of the parameter space. Theoretical consideration of mechanisms which these asynchronous solutions arise has been an active area of research in non-linear dynamics over the past two decades [40] [42] [43] [44]. While a complete understanding of the set of possible behaviors in the general PCO system is lacking to date, it is noted that some period-1 solution persists and is stable through a large region of the parameter space [40] even in complexly connected networks [41]. Indeed, in Hong and Scaglione's 2004 work [27], it was observed that for fairly ``reasonable'' parameter range of wireless sensor networks (WSNs), the period-1 solution is still prevalent and synchronization robust. However, [27] did not analyze the PCO based WSN specifically for the timescales of short range, low duty cycle impulse radios. Furthermore, since it has been well-established that undesirable asynchronous behavior *is* possible in PCO systems, [27] failed to discuss where the boundary between synchronous and asynchronous behavior lies within the PCO parameter space. Furthermore, [27] did not consider the effect of phase noise in their simulation, which has been shown to cause a synchronized state to lose stability in some part of the parameter space [40][43]. We will show through simulation in subsequent sections that reasonable PCO implementation design parameters for WSNs are well within the boundaries of robust synchronization behavior, and that the incorporation of the blackout period is sufficient to avoid the exotic unstable synchronous states seen in [40] and [43]. From an engineering perspective, this is an

important argument to the feasibility of the PCO system for adoption in scalable distributed sensor networks that has yet to be reasonably investigated in the literature.

2.3 Physical Modeling of the PCO System for IR-UWB Networks

The PCO system was originally conceived as an idealized mathematical model to study dynamic behaviors of biological systems exhibiting long periods but short duration interactions. Since we wish to duty cycle each impulse radio very aggressively, we need a method to methodically and precisely translate our physical implementation of a network of oscillators conceptually shown in

Figure 2.5 to the mathematical model of chapter 2.2 with proper non-ideal effects so that we may understand the precision we may expect for our synchronization.

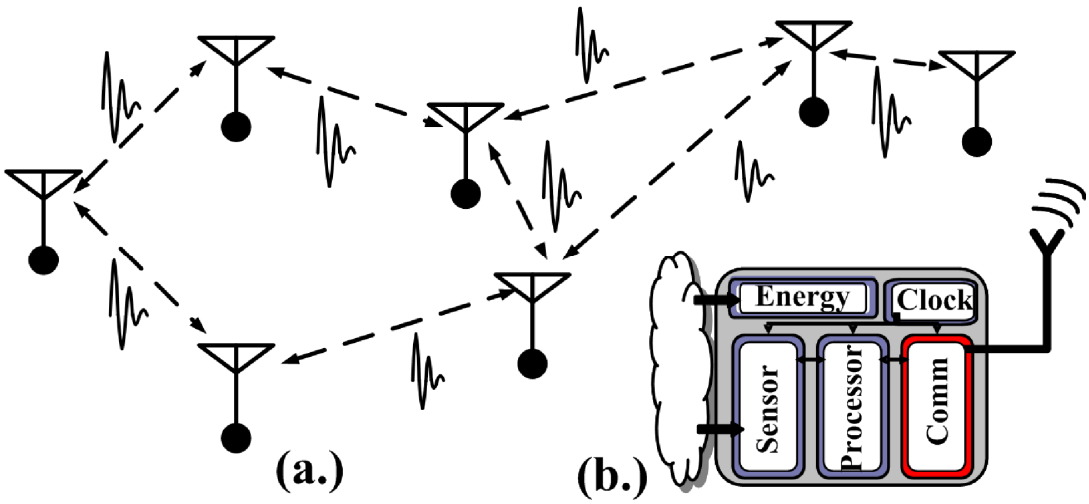


Figure 2.5. (a) Radio network using PCO synchronization, (b) individual node system block

2.3.1 Relevant Timescales for IR-UWB

Practical radio systems in North America must be compliant with FCC mandates. A regulatory order adopted in 2002 created the Part 15 limits for UWB radio, allowing unlicensed use of the 3.1 GHz to 10.6 GHz band provided the bandwidth of the transmitted signal exceeds 500 MHz and be compliant with a mandated spectral mask. For pulsed radios, these mandates necessitate transmitting a short wavelet at most 2ns wide with a smoothly rising envelope to reduce unintentional emissions into more restricted parts of the spectrum. For a periodic pulse train, a fixed pulse shape defines the shape of the spectrum while the the spectrum amplitude linearly scales with pulse repetition rate (PRR). In practical CMOS designs, it has been shown that pulse rates on the order of 100KHz to 1MHz easily fall within the mandated spectral mask [45] at $\sim$1V maximum wavelet amplitude over a 50 Ω antenna. This constraint in peak wavelet amplitude also has the effect of limiting transmission ranges to around 10 meters [4], which implies that time propagation effects are limited to less than $(1/T_{PRR})\ (d/c_l) \approx\ 0.033$ phase units between nodes for the pulse rate of 1 MHz or 0.0033 normalized phase units at 100 KHz, where d is the separation distance and c_l is the speed of light. This sets the time-delay order of magnitudes to consider in these systems.

The power consumption of a duty-cycled IR UWB receiver can be approximated by:

$$P_{RX}\ =\ \left(\frac{T_{pulse}\ +\ T_{uncertainty}}{T_{PRR}}\right)\ P_{RX\_DC} \tag{2.3}$$

where T_{pulse} is the pulse width, $T_{uncertainty}$ is synchronization uncertainty introduced by deterministic or random sources, T_PRR is the repetition rate of the

system and P_{RX_DC} is the steady state power consumption of the RF subsystem, which is on the order of 10mW in high gain, high bandwidth IR-radio implementations [38]

Having established that T_{pulse} is ~2ns and $T_{PRR} > 1\ \mu$s, we see that if $T_{uncertainty}$ can be < 10ns power saving factors on the order of 100 to 1000 can be achieved, thereby enabling *microwatt* radios. However, $T_{uncertainty}$ is dependent on both the random jitter (phase noise) of each radio's local PCO oscillator as well as the stability of the network synchronization. In the following sections, we will show that low-enough-jitter relaxation oscillators compatible with pulse coupling can be implemented in standard CMOS processes and detail design considerations when converting a real oscillator into the phase model of Section 2.2. We will also show that PCO steady-state dynamics are sufficiently stable even with the injection of phase noise to facilitate the aggressive duty cycling that we propose.

2.3.2 Oscillator Implementation: Timescales and Design Considerations

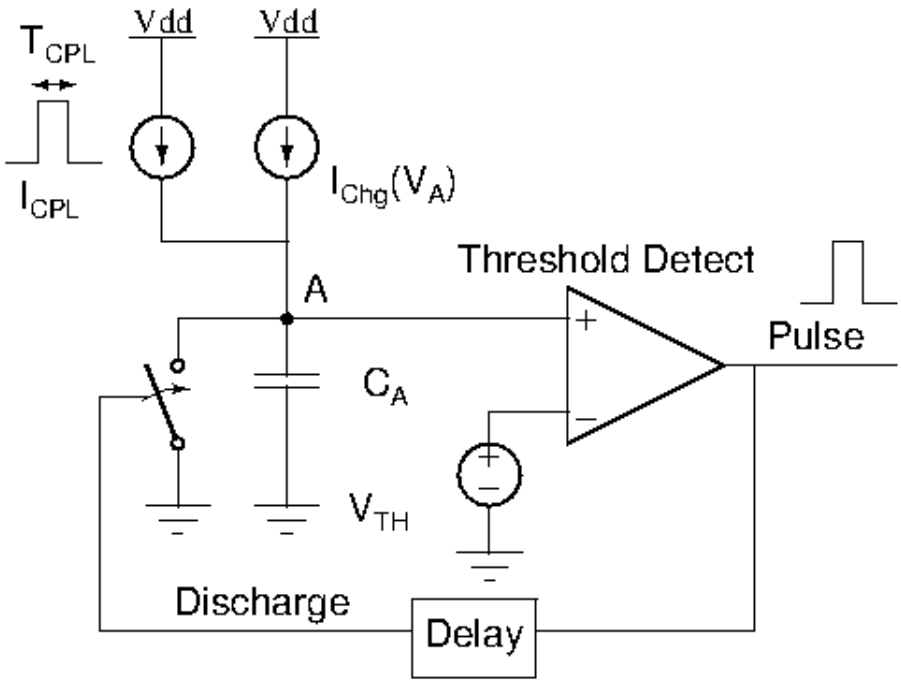


Figure 2.6. General PCO Circuit Implementation

In order to realize a network of PCO IR-UWB radios, we must adapt the mathematical PCO model of Section II into a physical circuit. Intuitively, examining Equations (2.1) and (2.2) leads one to consider an analog circuit implementation like that of Figure 2.6. Assuming a perfect threshold detector and an instantaneous reset, there is a 1-1 correspondence between the phase of the oscillator ϕ and the voltage at node A. In this case, a voltage jump on node A can be unambiguously translated to some phase shift. The monotonicity and concavity condition on the function $V(\theta)$ of Eq. (2.2) implies that excitatory coupling has a stronger effect on the phase shift later in the cycle (ϕ closer to 1) than earlier in the cycle (ϕ closer to 0). We see that if we couple a current pulse of constant charge $Q_{CPL} = I_{CPL}\, T_{CPL}$, this coupling condition can also be met, because an equivalent voltage jump causes a bigger time shift in the oscillator at higher V_A. If we implement I_{Chg} with a resistor, then the RC time constant

sets the oscillator's frequency. On-chip resistances and capacitances on the scale of 10M Ω and 10pF, respectively, are reasonable, setting the minimum oscillation frequency on the order of tens of KHz. Recall that low frequency oscillations facilitate greater power savings through duty-cycling in a synchronized IR-UWB radio node.

Jitter in the oscillator, however, makes it unreasonable to scale the frequency too low. The cycle-to-cycle jitter J_{cc} of an oscillator can be related to its phase noise in a $1/f^2$ region through a single scalar constant c (with units of seconds) [46]. These equations are, for phase noise at $\Delta f << f_0$:

$$L(\Delta f) \approx c\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.4}$$

$$J_{cc} = \sqrt{c\, T_0} \tag{2.5}$$

$$J_{cc} \approx \sqrt{\frac{L(\Delta f)\Delta f^2}{f_0^3}} \tag{2.6}$$

where $L(\Delta f)$ is the ratio of the power in a 1 Hz bandwidth at frequency $f_0 + \Delta f$ to the total power at the carrier.

We implemented the PCO circuit of Figure 2.6 in an IBM CMOS9SF process with $R_1 = 1.75M\Omega$. $C_1 = 7.5$pF. The jitter of this oscillator is 3ns at 150KHz based on Cadence SpectreRF PNOISE analysis and using Eq. (2.6) To ensure that the oscillator is operating in a white noise dominated regime where Eqs. (2.4)- (2.6) are valid, we separate PNOISE by sources and see that at an offset frequency of $\Delta f = \frac{f_0}{20}$ the white

sources contribute approximately 4 times the phase noise of the flicker sources in the IBM9RF process.

It should also be noted that some degree of jitter should *always* be included in a PCO network simulation, since it has been shown that some synchronous states can be unstable to slight perturbations in phase and adding some jitter will expose this instability [43]. In a reasonable duty cycled UWB system at 150KHz, the jitter of the physical oscillator should be allowed to range up to 10ns / 3 = 3.3ns, which is set by giving three-sigma tolerance for the synchronization pulse. Normalized to the period, this implies jitter is on the order of magnitude of 5e-5 - 5e-4 phase units at 150KHz, and should scale inversely proportionally to the root of the period according to Eq. (2.5) as long as the dominant phase noise sources remains white noise.

2.3.3 Coupling Mechanisms

In several PCO network studies, such as [27], the coupling strength is modeled as dependent on the distance of separation between two nodes in the network. For physical implementations of UWB radios however, this model is unrealistic since the detection of a UWB pulse is best done with a threshold detecting circuit. The coupling action is realized as a fixed charge of Q_{CPL} , which is generated at the receiving node and increases the voltage of the oscillator, advancing its phase. Since the coupling pulse is generated *locally* based on the detection of an impulse, it can be made *arbitrarily* weak or strong by the sizing of the coupling transistors and the width of the coupling pulse.

An important aspect of a PCO network implemented in CMOS circuits is that its does not need off-chip timing components. This is because a PCO network has a degree of *natural* tolerance to frequency mismatch effects and certain characteristics in the network, such as relative jitter, actually *improve* with mismatch, which we will

show in the results of Section IV. Simulating the PCO of Figure 2.14 over three-sigma corners in the IBM CMOS9SF process, we see that the natural frequency of the oscillator varies from 142KHz to 166KHz, or around $\pm$10\% variation which we will show can be reasonably compensated with strong-enough coupling.

2.4 PCO Network Simulation

In this section. we will show that IR-UWB networks implemented in CMOS technology with *all* non-idealities modeled can fall within a robust region of the parameter space *provided* that coupling is strong enough to overcome the intrinsic frequency variations within the oscillators and that the blackout period is at least twice the largest delay distance between two directly connected radios in the network.

2.4.1 Normalized Timescales

In chapter 2.3, we detailed the physical constraints imposed by CMOS implementations of radio circuitry and relaxation oscillators and the relevant timescales of these systems due to these constraints. We provide a summary of these physical parameters in Table 2.1. Since the best way to analyze a PCO network is in normalized *phase* units, we need to translate the physical time and distance parameters to normalized parameters. These equations for normalization are detailed below:

$$d_{phase} = \frac{d_{meters}}{c_l}\frac{1}{T_0} \tag{2.7}$$

$$t_{phase} = \frac{t_{seconds}}{T_0} \tag{2.8}$$

where d_{phase} and d_{meters} are normalized and real distance respectively, t_{phase} and $t_{seconds}$ are normalized and real time, respectively, T_0 is the nominal period in real time and c_l is the speed of light in $\frac{m}{s}$.

Table 2.1: PCO Network Simulation Parameters

Parameter	Physical Value	Normalized Value
f_0	100KHz – 1MHz	1
Δf	(0.01 – 0.1) f_0	0.01 – 0.1
Range (d)	3m	0.001 – 0.01
Blackout (T_{blk})	(0 – 0.4) / f_0	$0 - 0.4$
Jcc	0 – 3.3ns	$0 - 3.3 \times 10^{-4}$ ($f_0 = 100KHz$) $0 - 3.3 \times 10^{-3}$ ($f_0 = 1MHz$)
Coupling (a)	arbitrary	Arbitrary
CouplingEvent	100ps – 1ns	$1 \times 10^{-5} - 1 \times 10^{-4}$

2.4.2 Simulation Details

We implemented a comprehensive, event-based simulator for the PCO system in MATLAB. This simulator incorporates frequency mismatch, jitter, propagation delay, variable coupling strengths, arbitrary coupling functions, and arbitrary network connectivities. In this simulation we utilize an array of node phases and an array of propagating signals which stores the time before each propagating signal reaches a destination node. Each step of the simulator, we look for the closest-in-time event, which is either a node reaching threshold and firing or a propagating signal reaching its destination node. We elapse all node phases and propagating signal times by this time. In the case of a node reaching threshold, we add its propagating signals to the propagation array and then reset its phase. In the case of a propagating signal reaching

a destination node, we advance the phase of the destination node by an amount determined by the coupling function of Eq. (2.1), remove the propagating signal from the propagation array and perform the firing and reset procedures if the coupling took the destination node to threshold. Since the time elapsed in the simulation every step is the time until the next event, this simulator is as precise as the double precision floating point numbers used to store the phase and propagating time values in MATLAB. This makes our simulator precise enough to capture the effect of jitter on the order of 1e-5 present in our system.

In this simulator, we modeled variable frequencies by defining a normally or uniformly distributed Δf_i variable of variance $\sigma_{\Delta f}^2$ (in normalized units) for every node i at the beginning of the simulation. We model jitter by dynamically generating a normally distributed random variable $Jcc_i[n]$ of variance Jcc^2 after every firing event. Thus, upon a node reset, the nominal time until the next firing in the absence of coupling for that node is $T_i[n] = 1 + \Delta f_i + Jcc_i[n]$.

Since the coupling event timescales (Table \ref{table_network_parameters}) are small compared to our desired synchronization precision, we are justified in modeling the coupling events as instantaneous. For the coupling function of Eq. (2.1), we defined both linearly and quadratically increasing couplings:

$$\Delta\phi_{linear}(\phi) = a\phi \tag{2.9}$$

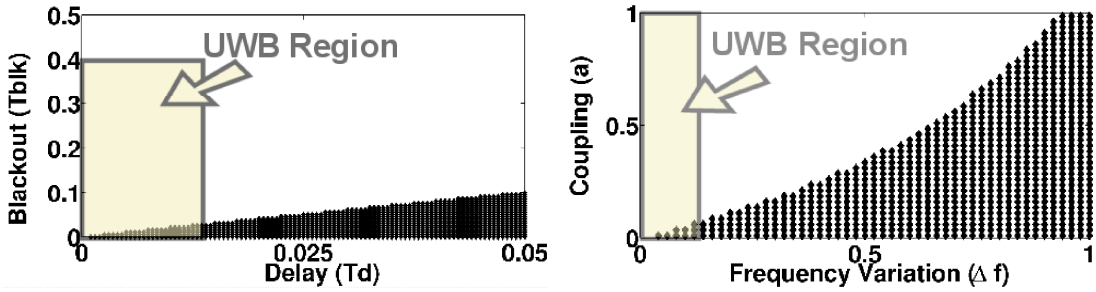
$$\Delta\phi_{quad}(\phi) = a\phi^2 \tag{2.10}$$

where the scaling factor a controls the strength of coupling. A blackout period can be implemented by multiplying the coupling function by 0 on $\phi \in [0, \phi_{blkout}]$. We noted that for either coupling function, the qualitative synchronization behavior was

similar. We chose the quadratically increasing coupling function for the simulations of the next section, though in principle any monotonically increasing convex function should work based on the conditions of Eq. (2.2).

2.4.3 Simulation Results

Four main parameters influence whether a synchronous state can be achieved and they occur in strongly related pairs: transmission range and blackout time (d, T_blk), and frequency mismatch and coupling strength $(\Delta f, a)$. The goal of these simulations is to identify regions of the PCO parameter space in which a stable period-1 solution occurs and determine if we can avoid regions where synchronization fails in a real IR-UWB sensor network.



(a) (b)

Figure 2.7. Synchronization versus parameter space for (a) delay vs blackout (b) coupling vs frequency variation. Black regions indicates where robust synchronization does not occur. The shaded transparent region indicate realistic physical parameters in our proposed network

2.4.4 Synchronization Parameter Space

For the parameter space exploration we simulated a network of 20 nodes, all-to-all coupling, variable propagation delay, and jitter on the order of 1e-3 (corresponding to 6.6ns at 150KHz). We simulated Δf, frequency mismatch, with a uniform distribution on $[-\Delta f/2\,, \Delta f/2]$ so that the frequency variation is bounded and predictable. To generate the plots in Figure 2.7 we performed sets of parameter sweeps where all other parameters in the network were held constant while the selected pair of parameters were allowed to vary and observed if a synchronous state was achieved within 500 simulation cycles. Since the ability of the network to synchronize might be dependent on initial conditions, for each simulated point in the parameter space we perform ten runs with a uniform distribution of initial node phases and consider synchronization to occur at that point in the parameter space only if all ten runs resulted in the period-1 synchronous result. For the parameter pairs of (d, T_{blk}) and $(\Delta f, a)$ we see a clear boundary between the synchronizing region and non-synchronizing region. For the (d, T_{blk}) pair, the boundary lies at $T_{blk} = 2\,d/c_l$ (Figure 2.7a), which is blackout equal to two times the maximum single-hop propagation delay and is independent of other system parameters. An intuitive reason why this boundary exists is because it prevents positive feedback where a node firing triggers the firing of a connected node that subsequently feeds back to the original node and advances its phase, destabilizing the system. We also observed that including sufficient blackout period eliminates the unstable synchronization modes witnessed in [40][43], that did *not* incorporate blackout in their simulations.

A similar boundary exists for the $(\Delta f, a)$ pair that mirrors the quadratic shape of the coupling function (Figure 2.7b), and it too is practically independent of the exact values chosen for (d, T_{blk}) provided they are in a synchronous region. This suggests that for synchronization to be maintained the coupling between nodes needs to be

strong enough to overcome their intrinsic frequency variations. Furthermore, both boundaries appear to be independent of the number of nodes in the network, at least to the scale of hundreds of nodes. The shaded regions in Figure 2.7 indicate the conditions that are realistic in our proposed network and we see that they offer a wide range of operating conditions for robust synchronization.

Based on the results of our simulations, it appears that there is a substantial region of the parameter space to operate a IR-UWB PCO network (Figure 2.7) We also note that the inclusion of jitter in the individual oscillator frequencies on the relevant timescales of IR-UWB does not break the ability of the network to reach a period-1 synchronized state and only affects the *quality* of the synchronization. Once synchronization is established globally, then duty-cycled communications between the nodes can take place as in Figure 2.4.

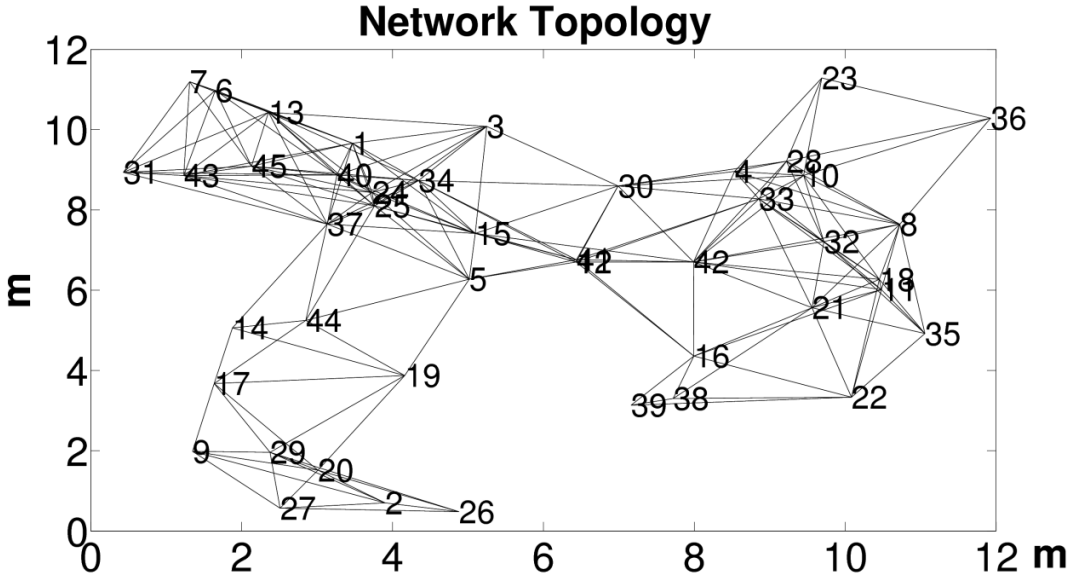


Figure 2.8. Connectivity of the network. Numbers indicate natural frequency ranking of oscillator

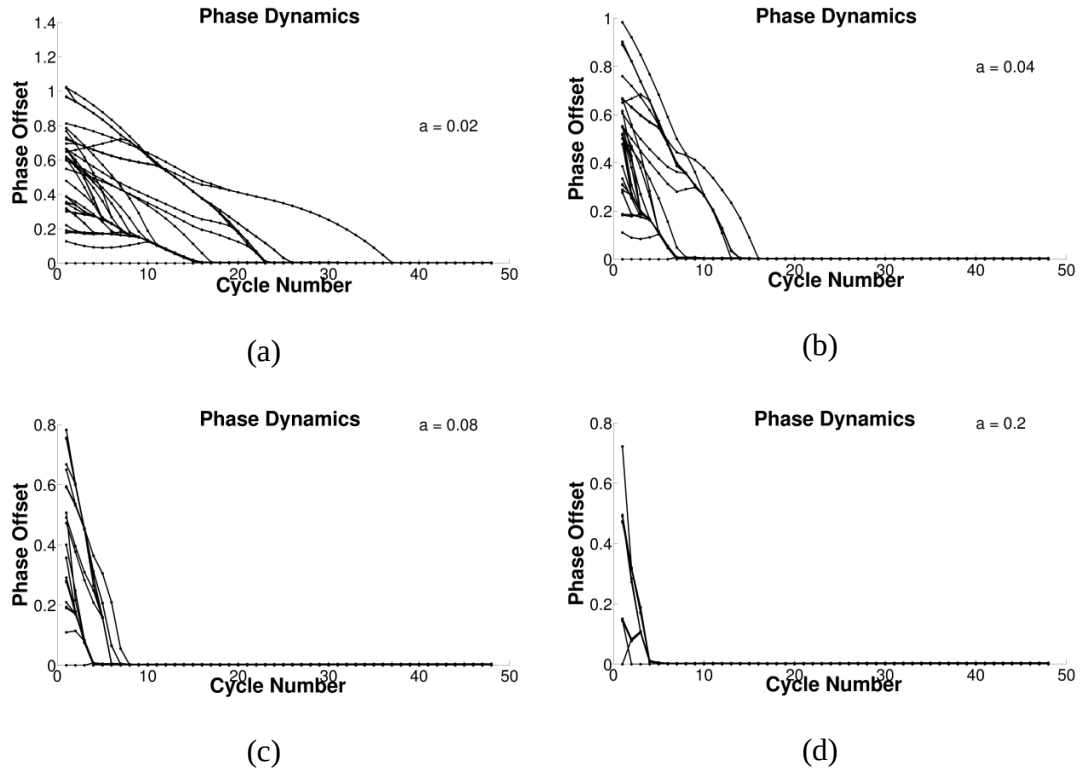
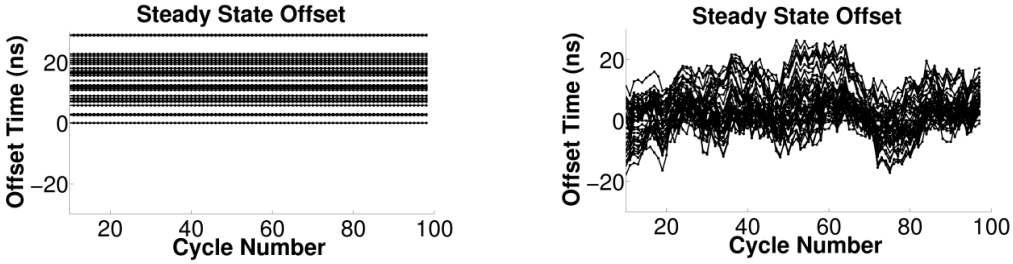


Figure 2.9. Synchronization dynamics with varying coupling strength a, (a) a = 0.02 (b) a = 0.04 (c) a = 0.08 (d) a = 0.2

2.4.5 Synchronization Steady State Dynamics and Quality

To use the PCO network to generate a global timebase for Duty-Cycled IR-UWB applications, we need to assess the synchronization quality of the network with respect to time-offsets as well as jitter. For this, we simulate the network of Figure 2.8 which models a 12m x 12m domain with 45 nodes randomly distributed inside. This network is fully connected in the sense that some path exists between any two nodes. We observed that over the parameter space of Table \ref{table_network_parameters}, synchronization always occurs at the frequency of the fastest node in the system, which we will call the *leader node* Figure 2.9 shows representative dynamics of the synchronization for varying coupling strengths. In this figure, each line represents the

firing time offset of a node in the network relative to the leader node versus the cycle number. The dynamics of the network exhibit the clustering phenomenon first detailed by Mirollo and Strogatz [35] and speed of synchronization in the network increases with increasing coupling and number of nodes.



(a) (b)

Figure 2.10. Steady state relative jitter of the network with normally distributed nominal frequencies (a) $\sigma_{\Delta f}$ = 0.05, (b) $\sigma_{\Delta f}$= 0

Once this steady-state is reached, the *relative* timing jitter between connected nodes in the network becomes the most important metric in an IR-UWB communications system. This is because all data communication between radios in the network must time their communication relative to the synchronization pulse (Figure 2.4). Thus even if jitter is present in an absolute sense, the quality of communication is not hindered if the relative timing is maintained. Figure 2.10a is a plot of the relative firing times of all the nodes in the system relative to the leader for each cycle in steady-state in a simulation with *all* non-idealities included. The frequency of the nodes is normally distributed with 5% variation, coupling is set to α = 0.25 (Eq. (2.10)) and jitter is set to 3.3ns (5e-4 phase units at 150KHz). The relative timing is perfectly stable in this case, since it only depends on the *propagation delay* in the network and not the characteristics of the individual oscillators.

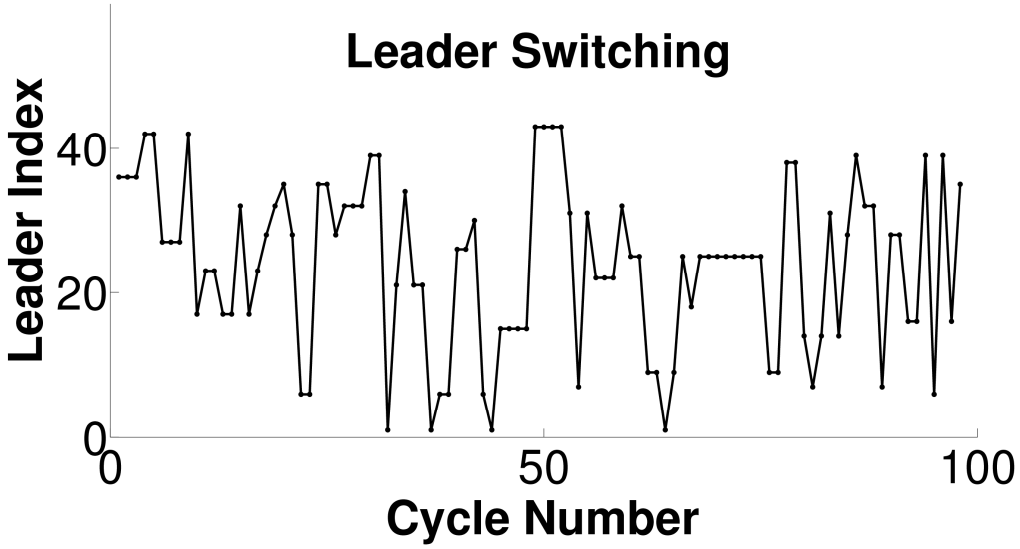


Figure 2.11. Leader switching in a perfectly frequency matched network with Jcc = 3.3ns (on the order of the propagation delay

Somewhat unexpectedly the worst case scenario for relative timing jitter is the situation where all nodes are *perfectly* frequency matched and noisy. A plot of this case is shown in Figure 2.10b, with all other parameters set the same as in Figure 2.10a. This situation arises because of *leader switching* in the network, where each cycle there is a probability that a different node will fire first. In this case the role of the leader is passed around the network, and the network has different orders of firing at different times (Figure 2.11). Leader switching is facilitated when jitter is large enough to overcome the delay separation between closely frequency-matched, adjacently-connected nodes in the network. In our proposed network, jitter and propagation delay are of the same order of magnitude (nanoseconds). Figure 2.12 is a statistical plot of the relative timing jitter between all one-hop connected nodes in the synchronized network as a function of their distance of separation. These statistics were collected by grouping the node pairs in the network by their separation distance

and looking at the relative jitter. We see that the mean of the relative jitter increases as a function of distance and its variance also increases.

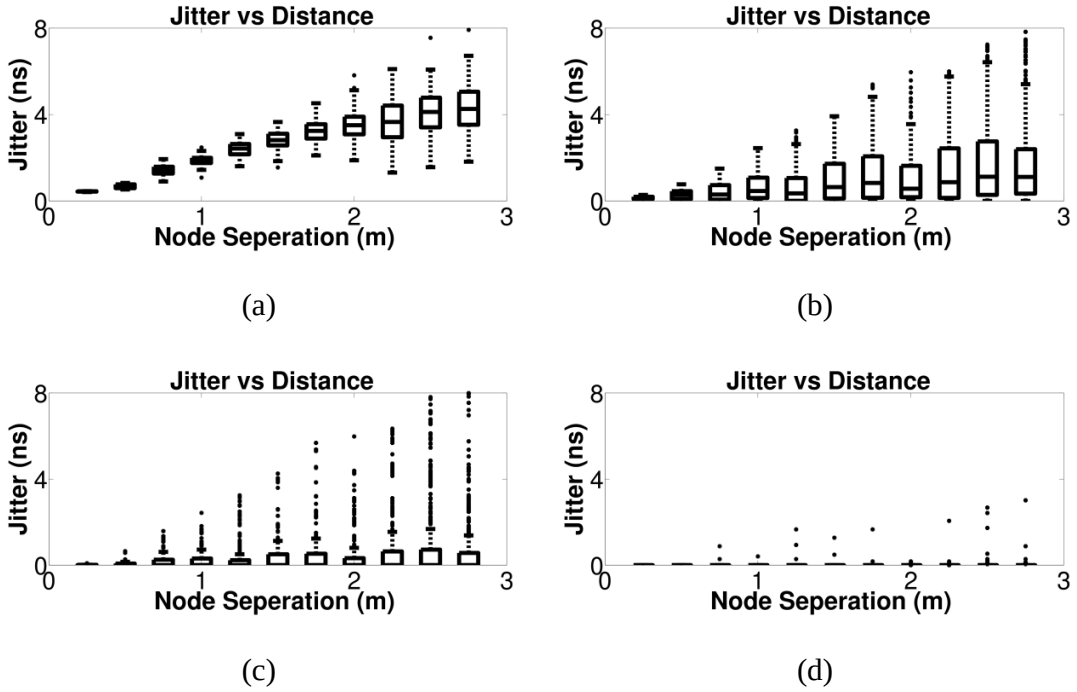


Figure 2.12. Steady state jitter distributions for all adjacently connected nodes in the network as a function of their separation distance. α = 0.25 and Jcc = 3.3ns. (a) $\sigma_{\Delta f}$ = 0%, (b) $\sigma_{\Delta f}$= 0.1%, (c) $\sigma_{\Delta f}$ = 0.3%, (d) $\sigma_{\Delta f}$ = 1%

From our simulations it appears that even a small degree of frequency mismatch in the network makes synchronization far more robust. This is understandable because the frequency of the network is set by the fastest oscillator. Even in networks with oscillators possessing small frequency variance it is unlikely that many nodes in the physical vicinity of the fastest node will have a frequency close enough to switch with it when the node frequencies are gaussian distributed. This explains the rapid decay of relative jitter with oscillator mismatch, being virtually eliminated when it is 1\% or higher (Figure 2.12). Analytically formulating to what degree frequency mismatch

helps synchronization is an interesting open problem that we have yet to analyze. Practically speaking, since CMOS radios exhibit frequency mismatch on the order of 1% - 10%, we do not predict PCO networks to exhibit much relative jitter in steady-state based on the results of these simulation.

2.5 First Generation Implementation of PCO System

In this section we will discuss the design and implementation of simple PCO synchronized radio nodes that we have described in previous sections. The PCO radio system consists of three primary components: the core oscillator, an H-bridge UWB transmitter, and an amplifier chain with peak polarity serving as the RF front-end (Figure 2.13). Using these simple radios, we demonstrate three-node synchronization in a real system of CMOS radio nodes. To the best of our knowledge, this represents the first demonstration of real, scalable multi-node wireless synchronization without a crystal. We will briefly overview the various circuit blocks here, however a more comprehensive description can be found in [38]

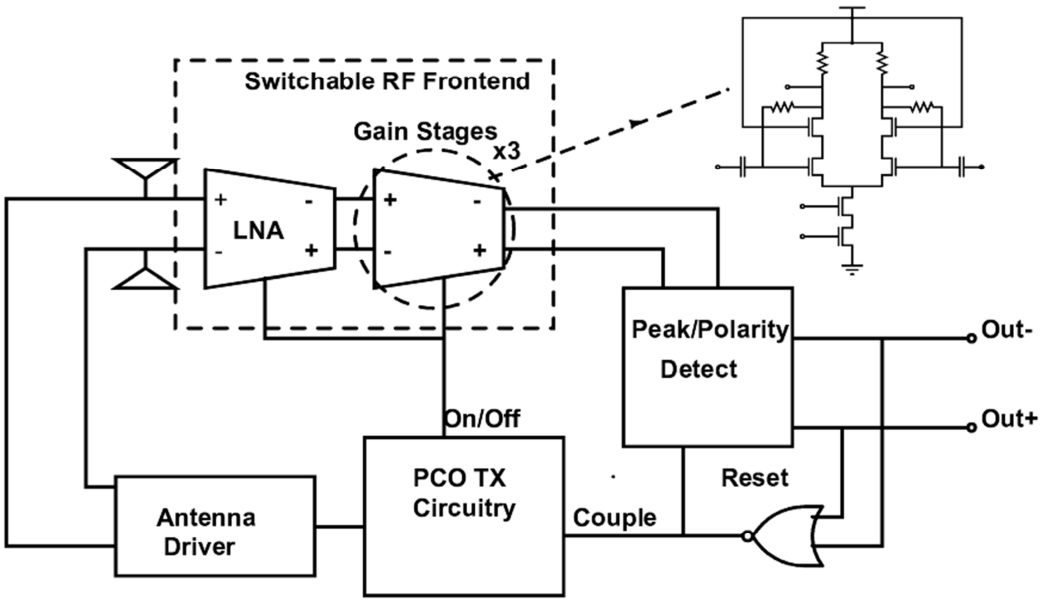


Figure 2.13. System block diagram of PCO synchronization circuit

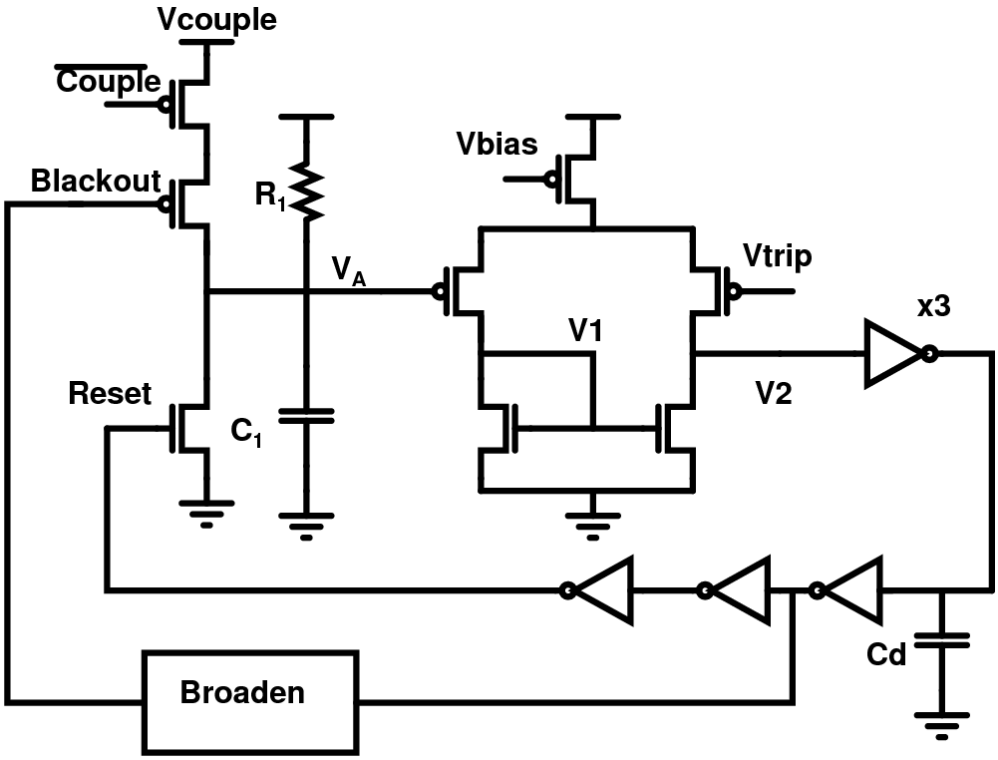
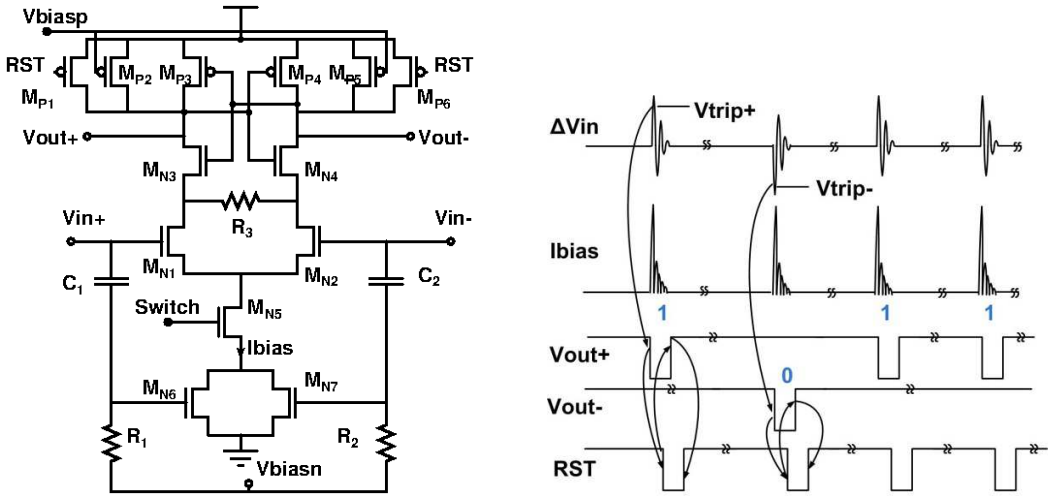


Figure 2.14. CMOS Implementation of PCO circuit



(a) (b)

Figure 2.15. (a) Peak polarity detector circuit (b) Timing waveform

We implemented the PCO oscillator with the comparator as a minimum-sized active current mirror biased at 1μA (Figure 2.14) the delay blocks with minimum-sized inverters, the reset a strong NFET switch and coupling done with PFET transistors. The strength of the coupling is tuned by a combination of increasing the coupling width as well as increasing the supply on the coupling transistors. The maximum coupling at 1ns coupling pulse width is simulated to be $\Delta V = 0.1$ at 1V VDD. We additionally broaden the reset pulse of the oscillator to generate the PCO blackout time, during which coupling cannot occur because the transistors are physically shut off.

We use an H-bridge based antenna-drive scheme for the pulse transmission proposed by Wang et al. [47]. In this scheme the antenna is connected between two strong inverter pairs driven by tapered digital drivers with controlled timing sequence. The key here is to inject a current into the antenna for radiation through its own LC-characteristics and then quench the radiation after small time ($\sim$1ns). A pulse transmission request by the transmit-control circuit controls the inverter pairs in a 3-step process. The radiation characteristics are dependent upon the strength of the current, the rising edge of the signal, as well as the pulse shaping characteristics of the antenna. The design operates at 1.2V supply and is digital in its driving characteristics. At 100kbps it was measured to have a total power consumption of only 4.5μW, with leakage power of 1.5μW.

For the receiver, we used a simple five stage differential amplifier chain followed by a regenerative non-coherent peak polarity detector. The switch-able amplifier stage is implemented as a common source amplifier with resistive feedback (Figure 2.13). Each stage provides 7dB of gain. The gain stages are AC coupled to each other to guard against DC offsets and low-frequency noise. The gain stages are designed to have the same input and output biases, thereby ensuring the same voltage difference

across the coupling capacitors and aids in faster turn-on. Care is also taken to suppress the supply transient by inserting a small resistor in the supply path as well as decoupling the biases and supply from ground.

The peak polarity detector (Figure 2.15a) is used to detect the reception of the pulse by the RF front end and effectively serves as an asynchronous one-bit ADC. This circuit works under the same principles as the regenerative latch commonly found in digital logic circuits, except we use the signal to latch itself. The circuit is biased such that MN7,8 are in subthreshold and that the positive feedback through inverter pairs MN3,4 and MP3,4 is suppressed by the prescence of damping transistors MP2 and MP5. However, upon the prescence of a pulsed signal, the total current through MN7,8 rises exponentially (Figure 2.15b), causing the positive feedback to increase and driving one of Vout+ or Vout- low depending on the input polarity. Resistor R3 ensures the positive feedback works correctly by keeping the sources of MN3, MN4 at nearly the same voltage. After the pulse is detected, RST is asserted, driving the outputs near VDD and allowing this circuit to detect the next pulse. This circuit can also be duty-cycled through the prescence of MN6, which can stop the flow of current in the circuit. Nominal bias current of this circuit is 1 μA when no signal is present.

The receiver was measured to consume 10.5mW in a 90nm process when fully ``on." However, this power is reduced by duty cycling when the Rx and Tx are synchronized. Accounting for synchronization accuracy ($\sim$5ns) the Rx needs to be ``on" only for 10ns for detecting a pulse $\sim$1-2ns wide. At 100kbps this results in a measured power of 14.3μW, where measured leakage power for the receiver is 3.3 μW.

2.6 Measurement Results

To demonstrate the coupled PCO IR-UWB system, we implemented the circuits of section 2.5 in the 90nm IBM9RF process as part of a complete IR-UWB system (Figure 2.16). Each PCO oscillator was wirebonded to a custom designed PCB and connected to wideband monopole antennas which radiate and detect the synchronization pulse. We performed a detailed characterization of the RF front end in an earlier work [38], and in this work we focus on the synchronization behavior of this system. To perform the measurments of three PCO nodes, the outputs of all three oscillators were connected to an Agilent DSO90254A sampling oscilloscope. We are able to observe 5ms of synchronization dynamics with 100ps resolution. This allows us to perform detailed time-domain statistical characterization of the synchronized network of three oscillators. To perform our characterizations, we perform a single 5ms capture, extract the edge times from the resulting data and postprocess in MATLAB. The tests were conducted in our normal laboratory environment with no special provisions for shielding from external sources of RF interference.

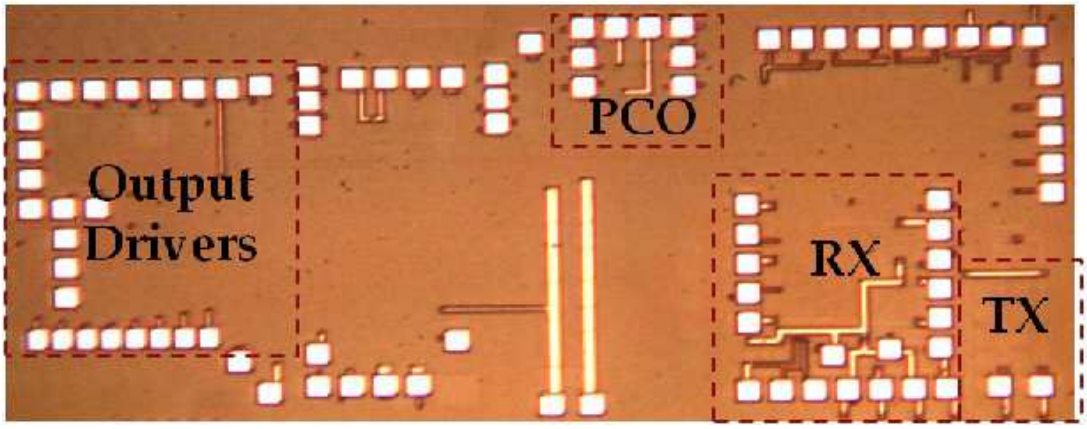
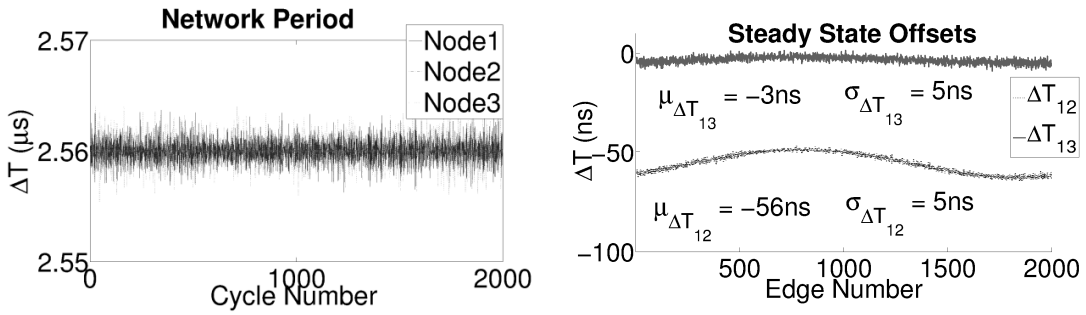


Figure 2.16. Chip Micrograph of a complete IR-UWB system. The synchronization related circuity is boxed



(a) (b)

Figure 2.17. Time domain measurement of three PCO nodes in the synchronized network over 2000 cycles of (a) the cycle-to-cycle period of each oscillator (b) the cycle-to-cycle edge offset relative to node 1.

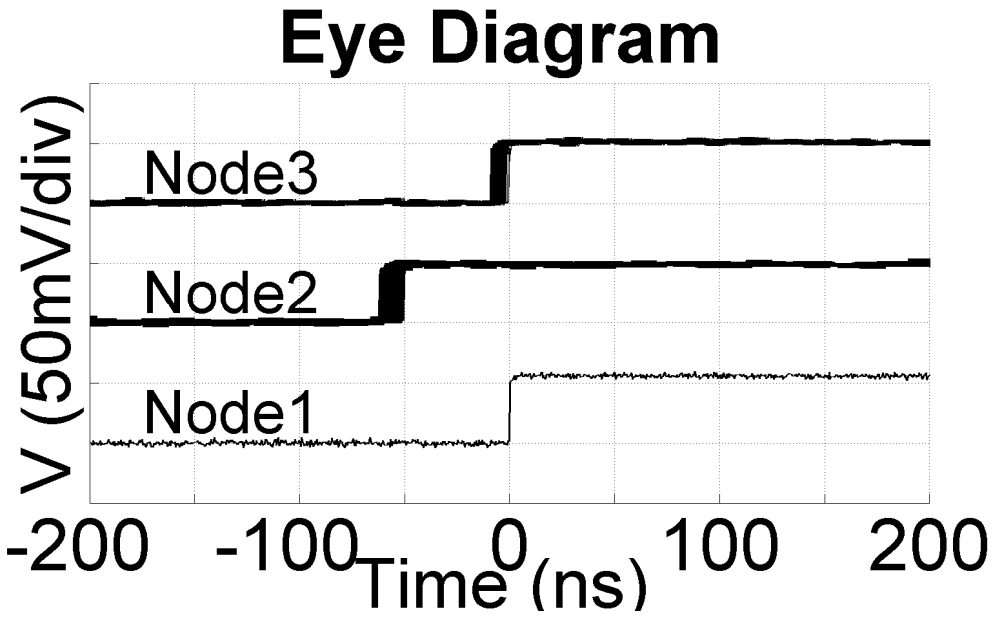
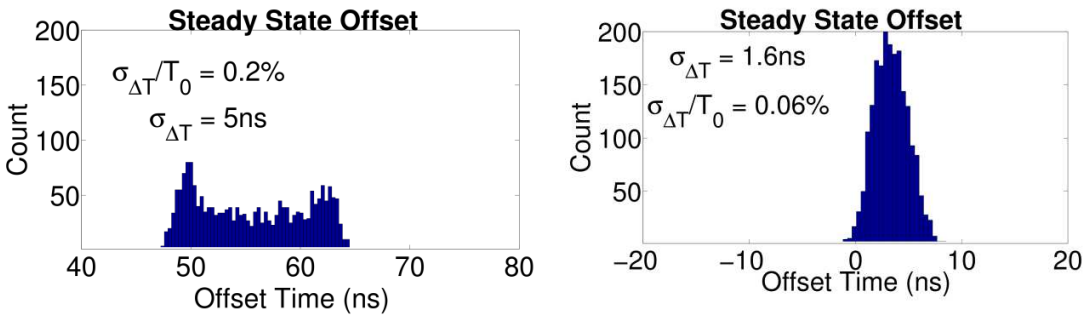


Figure 2.18. Time domain measurement of three PCO nodes in the synchronized network over 2000 cycles of (a) the cycle-to-cycle period of each oscillator (b) the cycle-to-cycle edge offset relative to node 1.



(a) (b)

Figure 2.19. Measured statistics of relative offset timing between oscillators in the PCO network over 2000 cycles. (a) node1 vs node2 (b) node1 vs node3

We measured a three-PCO network implementing the circuit of Figure 2.13 with a low-jitter leader (highest frequency) oscillator in the network. The nodes were seperated by a distance of 8-10 meters (26-33ns). We noted that the presence of the leader in the system prevents the deterministic jitter effect through leader-switching we observed in simulation from manifesting itself In steady-state, the network reaches synchronization with all three nodes settling to a stable network period of 2.56μs (Figure 2.17a). As expected, the oscillators are phase aligned as well as frequency aligned, as shown by the measurement of the relative time offsets of the three nodes' rising edges Figure 2.17b experimentally verifying the synchronization of the system. To further gauge the synchronization quality, we look at the eye diagram of the three node system Figure 2.19a as well as the statistical distribution of the relative offset times (Figure 2.19b). Both the eye and the histogram show a small amount of relative jitter in the synchronized network. This can be explained by the fact that the coupling takes some time to propagate through the noisy amplifier chain and comparator circuits, a source of jitter we did not model in our simulations. However, its low value of 5ns and 1.6ns between oscillator pairs 1,2 and 1,3 respectively is tolerable for

aggressively duty-cycled impulse radio communications. Scaled by to the period of the synchronized system, this jitter is 0.2% and 0.06% respectively, which indicates the degree of power savings that can be achieved through duty cycling. These measurements confirm our simulation's result that relative jitter in the synchronized network should be small and that robust phase-stable PCO synchronization can be achieved in *purely* integrated CMOS. It also shows, experimentally, that we can operate a real system in the robust, period-1 region of the parameter space that simulation suggests should exist.

This is the first CMOS demonstration of a truly ad-hoc scalable synchronization scheme for IR-UWB that requires no explicit differentiation between nodes in the network or costly off-chip crystals, unlike the schemes proposed in [34] and [4] respectively. The impulsive nature of PCO networks is also particularly well suited for IR-UWB and is precise enough for aggressive duty-cycling. Our proposed scheme combines the potential for scalability with this necessary precision and is well suited for a distributed cognitive network.

Chapter 3

TRANSCEIVER ARCHITECTURE, TIMING SYSTEM DESIGN AND IMPLEMENTATION

3.1 Introduction

We have seen in the previous chapter that distribution of the PCO synchronization beacon in a wireless network leads to a globally synchronized network with very stable relative timing, even in the presence of frequency mismatch and jitter. This chapter describes a transceiver system built around the PCO synchronization. The system uses a PLL to partition the PCO period into 128 time bins which are used for multiple access. Detailed analysis is done for the timing system with respect to phase-offset and jitter and specifications are defined.

3.2 PCO IR-UWB Based System

3.2.1 Global Synchronization Beaconing with Pulse Coupled Oscillators

We apply the concept of a global network clock, as in [9], but at *bit* level as opposed to packet level. In our system, the synchronization beacon is sent as a single IR-UWB pulse of ~2ns width. On the transmit side, each node emits the synchronization beacon when its timing oscillator, implemented as a relaxation oscillator, reaches threshold. The synchronization beacon is asynchronously detected by a receiving node, which then injects a pulse into its own relaxation oscillator, advancing its phase. When nodes follow an RC-like state charge-up function and the coupling is impulsive, then networks of oscillators implementing this function achieve phase lock with time-offset equivalent to the propagation and Tx/Rx latency of the pulse processing [27]. We have shown the applicability of this scheme to provide

synchronization for multi-hop IR-UWB networks in the presence of real word nonidealities such as oscillator frequency mismatch and jitter. We found that this scheme can allow dozens of nodes to phase synchronize in a multi-hop network, even with substantial oscillator frequency mismatch as long as coupling strength is sufficiently high to compensate for it. Operating each node in the strong-coupling regime, where detection of the synchronization pulse directly causes the receiving node to fire, causes the fastest convergence to synchrony and can compensate for the most frequency mismatch. We therefore exclusively operate in this regime for the system implemented in this paper. As a result, the system does not require that the symbol rate be well defined a-priori, as it is in traditional transceivers. Since the network is phase locked, synchronization can be maintained indefinitely, as long as the synchronization beacon is reliably detected. Aggressive bit-level duty cycling can be achieved by timing each node's pulse transmission and reception periods relative to its own synchronization pulse.

3.2.2 Physical Layer Description

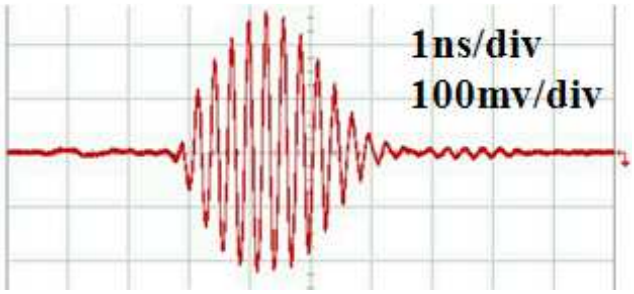


Figure 3.1. Measured pulse time domain waveform. 4.5GHz type.

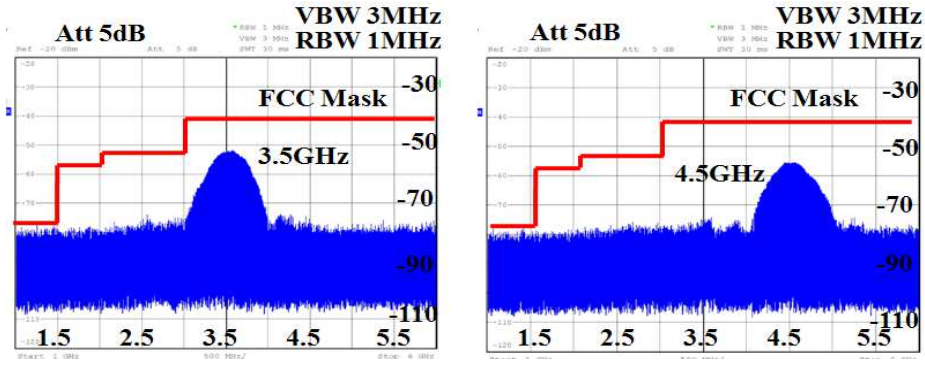


Figure 3.2. Measured transmitter spectrum while periodically emitting the PCO sync pulse at 150KHz for the 3.5GHz and 4.5GHz pulse type.

All transmissions in our system use two types of 2ns IR-UWB Gaussian-like pulses: one with a 3.5GHz carrier and another with a 4.5GHz (Figure 3.1). The frontends of the transceivers are time-multiplexed to one pulse type or the other. We use the 3.5GHz pulse type to broadcast the synchronization pulse in the PCO scheme while using the 4.5GHz pulse for data transmission. We operate the system with PCO pulse repetition at a nominal rate of 150KHz. Periodic transmission of the PCO pulse at these rates imply that its spectrum occupies a 500MHz bandwidth with discrete peaks spaced at $1/t_{FRAME}$, where t_{FRAME} is the PCO period. Measured data from our implemented transmitter shows the PCO scheme is compliant with the FCC UWB spectral mask when periodically transmitting with either pulse type (Figure 3.2)

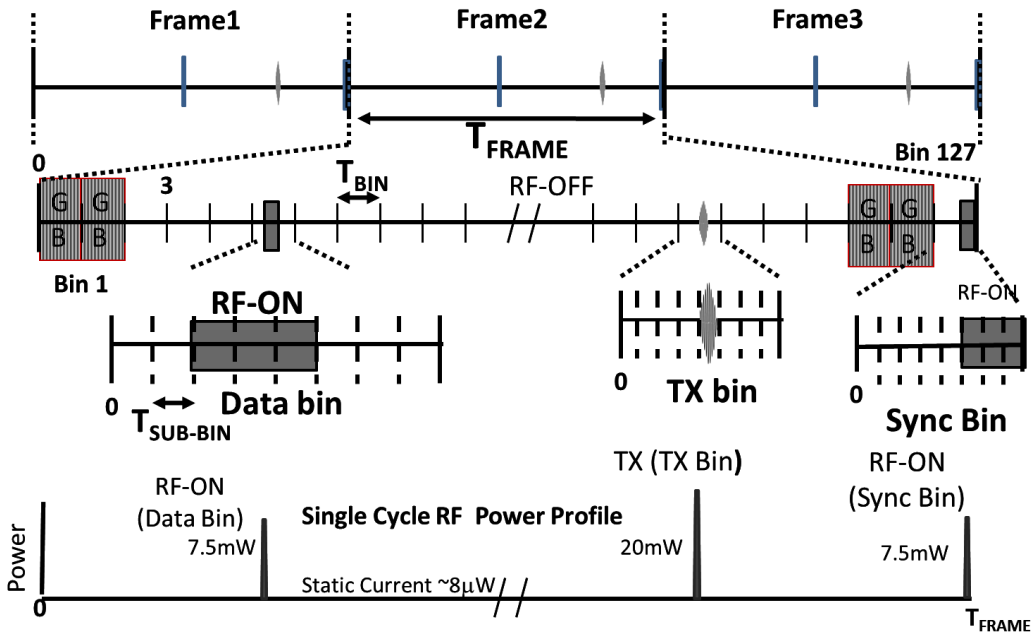


Figure 3.3. System timing structure for the packets in our system

The dynamics of the synchronization process in our network are as follows: Initially the nodes are unsynchronized and their PCO oscillators mismatched in phase and frequency. In this unsynchronized state, nodes only transmit the synchronization pulse and do not duty-cycle. Pulse detection at the receivers is completely asynchronous during this process and is not aligned to any clock. Nodes then acquire phase-lock through the PCO process. Based on simulations in the strong-coupling regime in which we operate, the PCO synchronization completes within 5 cycles for networks of 45 nodes. The PCO period, t_{FRAME} is subdivided into 128 bins of t_{BIN} duration by a PLL circuit. The nodes detect that they are in a synchronized state based their detection of the synchronization pulse and/or a PLL-locked signal (Section 3.5). Once synchronized, nodes may transfer data as well as initiate bit-level duty cycling. A single data pulse is OOK modulated within a time bin. While PPM transmissions are also possible within this framework and equivalent to OOK from a BER vs signal

energy point of view [9], in our bit-level duty cycled scheme, this would incur a 2x energy penalty since it would require two samplings of the RF window per bit.

Since the IR-UWB pulse is much narrower than the bin time in our system, the bins in the system are further divided into 8 sub-bins ($T_{SUB-BIN}$). The sub-bins provide the finest time resolution in our system. The sub-bins are used for pulse offset and jitter estimation and compensation, so that bit-level duty cycling may be done at finer resolution.

Once the time bins are established by the hardware synchronization system, the system can be treated as a generic packet-based digital radio system and use well-established digital synchronization methods for packet-level synchronization. Bin allocation and neighbor discovery may also be performed at the network layer with an algorithm such as SMAC [48]

The time bins form the data-channels in our system. Of the 128 time bins, bin 127 is dedicated to the detection of the synchronization pulse, and bin 0-1 and 125-126 are used as guard bins (Figure 3.3) to allow the front end's transmitter or receiver to switch between the 3.5 and 4.5GHz bands. This leaves 123 data channels for the nodes to use. Since the radio is targeted for short range networks, this number is more than sufficient for node densities in this application space.

Note that the time bins in our system are a part of the *physical* layer and are analogous to the 80 physical frequency channels in the Bluetooth specification, whereas *timeslots* in traditional TDMA are a part of the MAC layer. Nodes can be assigned to time-bins in the same way that they are assigned to frequency channels in Bluetooth. Our system, targeting the lowest absolute power consumption possible, is designed for a data rate of 1 bit per frame per node. Full duplex communications, where two nodes simultaneously communicate, are also possible by picking separate

tx/rx bin pairs within the frame (Figure 3.3). The nominal parameters of our system are shown in Table 3.1 below.

Table 3.1: Physical Layer Specifications

Symbol	Description	Nominal Value
$T_{SP} = t_{FRAME} = t_{PCO}$	Symbol period	6.66μs
T_S	Bit decision window time	Asynchronous (S1) 52ns (S2), 25ns (S3)
t_{BIN}	Bin Time	52ns
$t_{SUB-BIN}$	Sub-bin time	6.5ns
t_{SIGNAL}	Physical signal time	2ns
N_{BINS}	Number of Bins, Total	128
$N_{BINS,Data}$	Bins usable for data communications (data channels)	123
$N_{SUB-BINS}$	Number of sub-bins per bin	8
f_c	Center Frequency	3.5GHz, 4.5GHz
BW	Bandwidth	500MHz
N_P	Pulses per frame	2
	Modulation	OOK

3.2.3 Transceiver Architecture

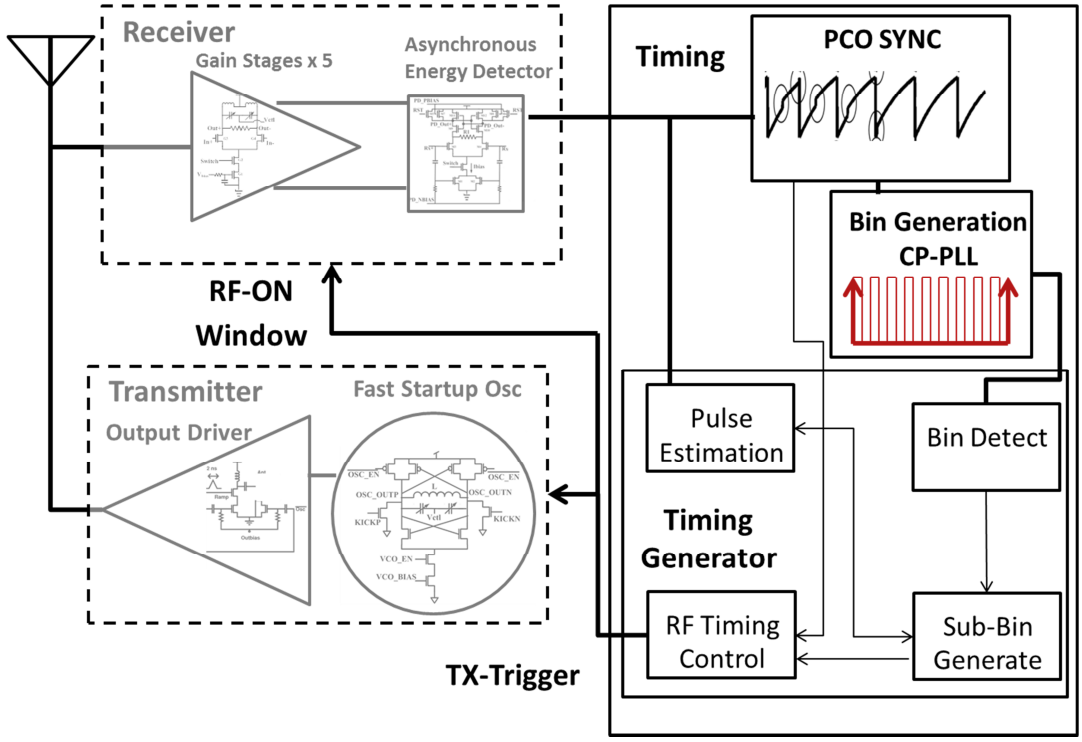


Figure 3.4. Transceiver system top level.

The transceiver (Figure 3.4) consists of the receiver, transmitter, and the timing system. The timing system, which is the focus of this chapter in the dissertation, consists of the PCO (frame generation), PLL (bin generation), and delay-locked-loop (DLL) (sub-bin generation) and dedicated logic for window control, pulse-type switching, and pulse offset estimation. The rx-front end directly couples received synchronization pulses into the PCO oscillator, and the PCO oscillator also directly triggers the transmitter. The PLL phase-locks to the PCO and all data transmission and RF-on window generation timing is derived from the PLL. The receiver and transmitter circuit design have been described and analyzed in my colleague Rajeev Dokania's works [17][20][28]. We instead analyze, design and implement the timing backend (Sections 3.3 and 3.3.2), and investigate the ability of the scheme to recover

from missed detection of the synchronization pulse (Section 3.5) as well as the ability of the transceivers to function within a network environment (Section 3.6).

3.2.4 Transceiver Power Consumption

We exploit the unique nature of pulsed IR-UWB transmissions to trade off active power consumption with data-rate (Figure 3.3). The transmitter only dissipates power when active, while the receiver is only active during the expected arrival time of the pulse. Ideally this will reduce the average power consumption by a ratio of $N_P\ t_{SIGNAL}/t_{FRAME}$ in both the transmitter and receiver, where $t_{SIGNAL} \cong 2ns$ is the pulse width, t_{FRAME} is the period of the system and $N_P = 2$ is the number of pulses within the period. However, in practice the transmitter is limited by leakage current (1-10's of μW) and the receiver is limited by both leakage and, more significantly, by timing uncertainty. Furthermore, a realistic duty-cycled system will also spend time losing and regaining synchronization due to missed detection of the synchronization pulse. If we consider these non-ideal effects, then the receiver power consumption can be expressed as:

$$P_{RX\_DC} = \bar{d}\ P_{RX\_Active} + P_{leakage} \tag{3.1}$$

Where $\bar{d}$ is the average duty-cycle of the system and can be expressed as:

$$\bar{d} = d_1\ Pr(S_1) + d_2\ Pr(S_2) + d_3 Pr(S_3) \tag{3.2}$$

Where d_1, d_2, d_3 are the duty cycles in the unsynchronized, partially synchronized and fully synchronized states, respectively and $Pr(S_i)$ is the probability of being in that state. $d_3 < d_2 < d_1 = 1$. The duty cycle in the S_2 and S_3 states can be expressed by:

$$d_i = \frac{N_P\, t_{RFon}}{t_{FRAME}} = \frac{2\,(t_{SIGNAL} + \alpha_i\, \sigma_T)}{t_{FRAME}}, i \in 2,3 \qquad (3.3)$$

σ_T represents the timing jitter between the transmitter and receiver, and α_i is a constant scale factor we choose to guarantee sufficient probability of remaining in the synchronized states. For the data rates that our applications target, $t_{FRAME} \cong 5 - 10us$. Thus we see that significant savings in active power consumption may be achieved if we can ensure both $\alpha_i \sigma_T \ll t_{FRAME}$ and $\Pr(S_3) + \Pr(S_2) \gg \Pr(S_1)$. Lower σ_T is always beneficial but is constrained by the power budget and circuit topologies available. There is also a trade-off between aggressive duty cycling (low α_i) and the probability of remaining synchronized. Later sections will describe the design choices influencing the σ_T (Section 3.3) and α_i (Section 4.2) parameters.

Eq. (3.3) also indicates that power consumption can be traded off with data rate provided that σ_T accumulates slower than t_{FRAME}. This implies that we should operate the PCO and PLL oscillators in a frequency where white phase noise sources dominate in order to gain the maximum benefit from duty cycling, since at lower frequencies, correlated noise sources cause σ_T and t_{FRAME} to scale at the same rate [49][50].

3.3 Timing System Analysis

In an ideal implementation of our system, the transmitter will transmit a data pulse in the middle of a bin and the receiver will expect the pulse in the middle of its bin. Due to propagation delay and non-idealities in the PCO and PLL circuitry however, a time offset develops between the transmitter and receiver bins. Also, due to jitter (phase noise) in the PCO and PLL circuitry, there is also some randomness in the time offset. The timing offset must be significantly less than a bin in width, while the timing jitter must be made as small as possible for our RF bit-level duty cycling to be

maximally effective. We analyze these effects in detail and their implications on the circuit design

3.3.1 PCO Offset and Jitter

Recall from Chapter 2 that the synchronized PCO network converges to a periodic steady state where the node with the highest nominal frequency oscillator (the synchronization master) fires first each cycle, which triggers the firing of other nodes that detect the synchronization pulse (synchronization slaves) . These slave nodes may be connected to the master through multiple hops. Consider the slave nodes i directly connected to the master node M. The master PCO node has a period of $t_M + Jcc_M$, where t_M is the average period and Jcc_M is the master cycle to cycle jitter. The time of firing of the slave node relative to the master in each cycle can be modeled as:

$$d_i = \frac{N_P\, t_{RFon}}{t_{FRAME}} = \frac{2\,(t_{SIGNAL} + \alpha_i\, \sigma_T)}{t_{FRAME}}, i \in 2,3 \tag{3.4}$$

Where Δt_{Mi} is a constant representing the deterministic time delay due to propagation (d_{Mi}/c) and pulse processing (τ_i), and Γ_{Mi} is a zero-mean Gaussian random variable modeling the time-uncertainty in that path, which we will call the *propagation* jitter.

Since the PCO network is *phase-locked* Γ_{Mi} does not accumulate. The period of the slave is then

$$T_i = t_M + \Delta t_{Mi} + Jcc_M + \Gamma_{Mi} \tag{3.5}$$

The total cycle-to-cycle jitter of the slave node $i's$ PCO oscillator may then be expressed as:

$$Jcc_i = Jcc_M + \Gamma_{Mi} \approx Jcc_M \tag{3.6}$$

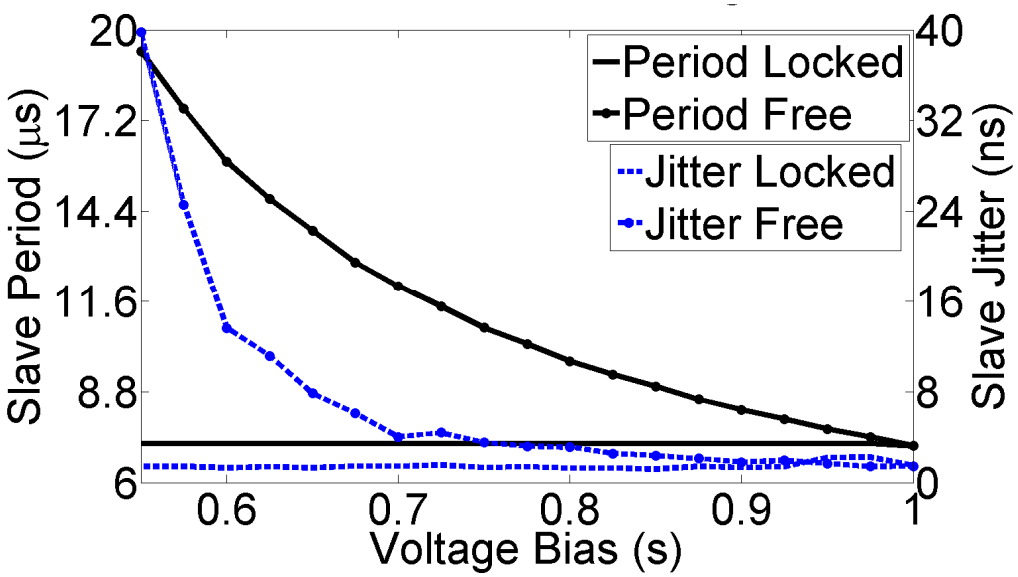


Figure 3.5. PCO slave oscillator period and jitter characteristics as a function of voltage bias when free running vs locked to another PCO.

The previous approximation can be made because $t_M \gg \Delta t_{Mi}$ so that the period jitter accumulates over a much longer timescale than the propagation jitter. This implies that both the period and period jitter of all nodes in the system are essentially set by the jitter of the master node. This is supported by the synchronization measurement of Figure 3.5 where we observe the period jitter characteristics of the slave oscillator in free-running versus frequency locked (to a master) mode. For this test we reduce the slave PCO's frequency by reducing the voltage bias. It is clear that the PCO master essentially eliminates the slave's oscillator's characteristics when pulse coupling is enabled.

Experimental measurements of the 4-node network support the PCO jitter and offset model above. Figure 3.6 shows typical values of the relative timing offset,

period and propagation jitter and long term frequency stability in our implementation of a synchronized four PCO system. The measured parameters are $t_{M=1} = 6.2us$, $\Delta t_{12} = 14.5ns$, $std(Jcc_1) = 1.1ns$ and $std(\Delta T_{12}) = 0.15ns$

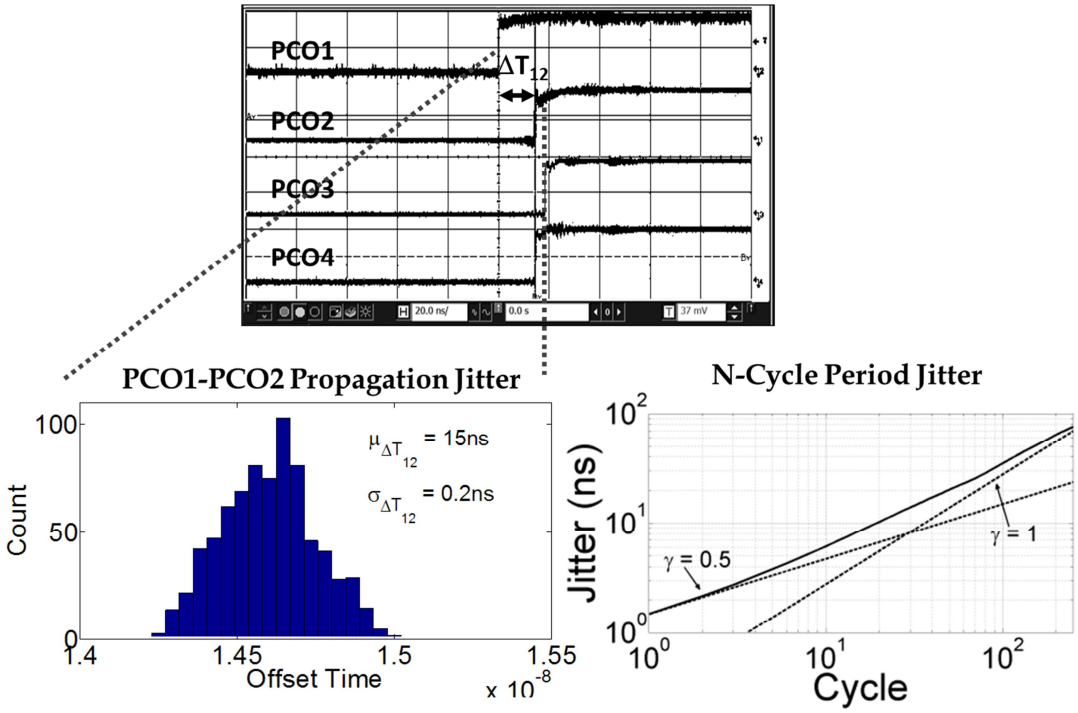


Figure 3.6. Long term jitter characteristic of a four node synchronized network. PCO1 is the master

3.3.2 PCO-PLL Locking Offset and Jitter

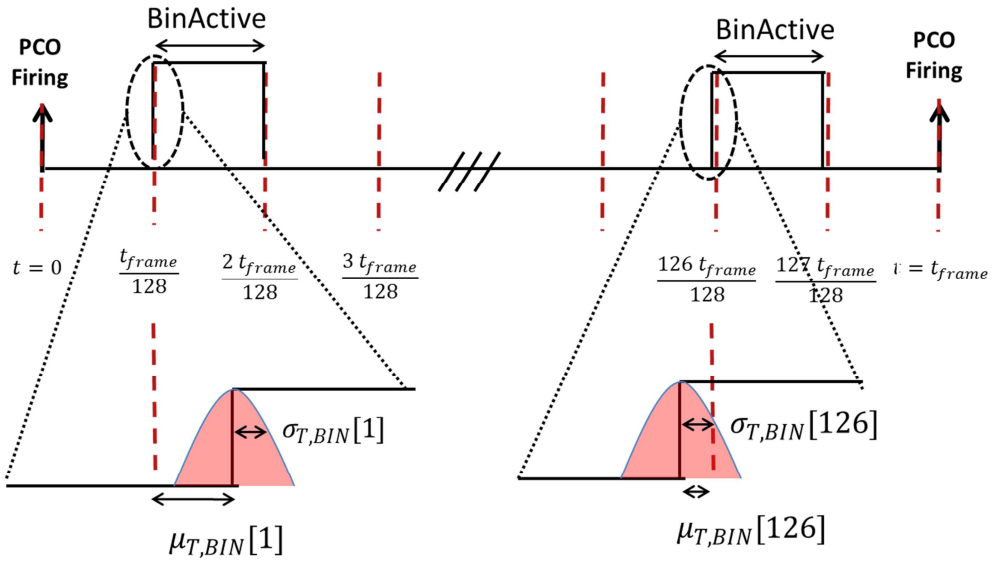


Figure 3.7. Illustration of the PLL locking metric

We use a charge-pump phase locked loop with second order loop filter and integer-128 (counter based) divider to segment the PCO period t_{FRAME} into 128 time-bins of equal width. Using the PLL in this fashion necessitates that it locks to the reference clock (the PCO) with high-enough time (phase) accuracy so that the boundaries of the bins are in the appropriate location. Since the PLL edge locking is both imprecise and jittery, these bin boundaries will have some offset from and distribution around the ideal bin boundary time. Use of the PLL in this manner is unconventional, so we must derive an expression of the precise accuracy of the PLL phase-locking in the presence of phase noise and offset sources.

Setting $t = 0$ at the time of the PCO firing of the node, we may define the time-error of the n^{th} bin relative to an ideal partitioning as follows (Figure 3.7):

$$T_{ERR,PLL}[n] = T_{BIN,ST}[n] - n\ \frac{t_{FRAME}}{128} \tag{3.7}$$

$T_{BIN,ST}[n]$ is a Gaussian random variable modeling the start time of the the n^{th} bin. The n^{th} bin offset and may be expressed as:

$$\mu_{Terr}[n] = E(T_{BIN,ST}[n]) - n\ \frac{t_{FRAME}}{128} \tag{3.8}$$

Where $E(.)$ Is the expectation. We define $\sigma_{BIN}[n]$, the n^{th} bin rms-jitter relative to the PCO edge at $t = 0,$ as:

$$\sigma_{T,BIN}[n] = std\big(T_{ERR,PLL}[n]\big) = std\big(T_{BIN_{ST}}[n]\big) \tag{3.9}$$

$std(.)$ above is the standard deviation.

$\mu_{Terr}[n]$ can be made small by minimizing the PLL locking offset to the PCO. Phase locking offset in this PLL topology is well known to be due implementation non-idealities, namely loop filter leakage current, charge-pump charge-injection and current mismatch. We describe the circuit design choices minimizing these in Section 0.

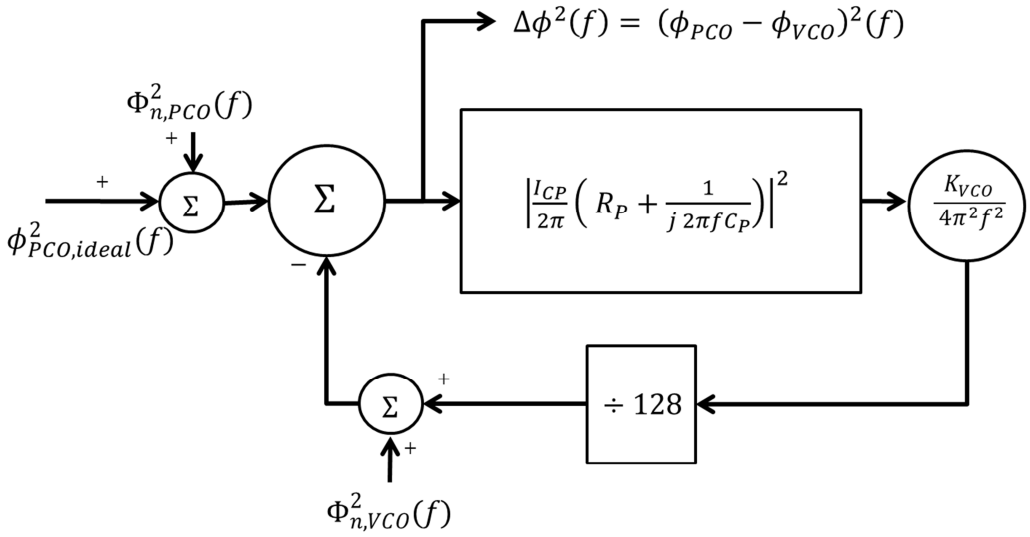


Fig. 3.8. PLL phase domain noise model.

The bin jitter will be dependent on the noise of the PCO reference, the VCO oscillator within the PLL and the loop filter parameters chosen. We use the continuous time phase-domain model of the PLL (Fig. 3.8) considering independent phase noise sources $\Phi^2_{n,PCO}(f)$, $\Phi^2_{n,VCO}(f)$ from the PCO and the VCO after the divider chain, respectively. Since the bin-jitter is defined relative to the PCO reference, the quantity we wish to find is

$$\bar{\sigma}_{T,BIN} = \frac{t_{FRAME}}{2\pi}\sqrt{E[(\phi_{PCO} - \phi_{VCO})^2]} \tag{3.10}$$

Where $\bar{\sigma}_{T,BIN}$ is the average PCO-PLL relative jitter and is a an approximation of $\sigma_{T,BIN}[n]$.

Noise sources $\Phi^2_{n,PCO}(f)$, $\Phi^2_{n,VCO}(f)$ see the same closed-loop transfer function $\left|H_{PLL,CL}(f)\right|^2$ the output $\Delta\phi^2(f)$, so that the transfer function may be written as:

$$\Delta\phi^2(f) = \left|H_{PLL,CL}(f)\right|^2 \left(\Phi^2_{n,PCO}(f) + \Phi^2_{n,VCO}(f)\right) \quad (3.11)$$

We define $\Delta\phi^2(f) = (\phi_{VCO} - \phi_{PCO})^2(f)$. $\left|H_{PLL,CL}(f)\right|^2$ is

$$\left|H_{PLL,CL}(f)\right|^2 = \frac{(f/f_n)^4}{1 + 2(f/f_n)^2(2\pi^2 f_n^2 \tau_{LF}^2 - 1) + (f/f_n)^4} \quad (3.12)$$

Where $f_n = \frac{1}{2\pi}\sqrt{K_V I_P / C_P}$ $K_V = K_{VCO}/128$ in units of Hz/V, and $\tau_{LF} = R_P C_P$. Assuming white-noise sources dominate, we may relate the phase noise sources of the PCO and PLL VCO to their free-running jitter accumulated over a period t_{FRAME} [51] by[2]:

$$\Phi^2_{n,VCO,PCO}(f) = \frac{E\left[Jcc^2_{VCO,PCO}\right]}{t^3_{FRAME}} \frac{1}{f^2} \quad (3.13)$$

Putting Eqs (3.12) and (3.13) together and integrating to find the variance, we may express the average relative jitter as

$$\bar{\sigma}_{T,BIN} = \frac{t_{FRAME}}{2\pi} \sqrt{\int_{-\infty}^{\infty} \Delta\phi^2(f)\, df}$$

[2] The Brownian motion phase noise process $\Phi_n(t)$ is non-stationary and its spectrum $\Phi_n(f)^2$ does not formally exist. This expression is a commonly used approximation over bounded observation intervals [50]

$$= \sqrt{\frac{1}{4\,\pi^2 t_{FRAME} f_n^2}\int_{-\infty}^{\infty} \frac{(E[Jcc_{VCO}^2] + E[Jcc_{PCO}^2])\ (f/f_n)^2\ c}{1 + 2(f/f_n)^2(2\,\pi^2\, f_n^2\, \tau_{LF}^2 - 1) + (f/}}$$

$$= \kappa(f_n, \delta, t_{FRAME})\ \sigma_{T,Source} \tag{3.14}$$

$\kappa(f_n, \delta, t_{FRAME})$ can be seen as a jitter multiplying factor of the source rms-jitter $\sigma_{T,Source} = \sqrt{E[Jcc_{VCO}^2] + E[Jcc_{PCO}^2]}$. We plot $\kappa(f_n, \delta, t_{FRAME})$ over normalized loop-bandwidth $f_n\ t_{FRAME}$ for a set of damping factors $\delta = \pi\ f_n\ \tau_{LF}$ (Figure 3.9) and $t_{FRAME} = 6.6\mu s$. κ decreases with higher damping and loop bandwidth. This is because the PLL locks the VCO phase tighter to the reference as damping and loop bandwidth increase. $\kappa < 1.6$ is achievable for $f_n\ t_{FRAME}$ = 0.1 for $\delta > 0.25$. The parameters we chose for the loop are shown in Table 3.2. The high loop bandwidth also increases the transient locking speed of the PLL to the PCO, reducing the time spent in the unsynchronized state.

Table 3.2. Nominal PLL Parameters

Parameter	NOMINAL VALUE	PARAMETER	Nominal Value
$\boldsymbol{R_P}$	680KΩ	$\boldsymbol{1/t_{frame}}$	150KHz
$\boldsymbol{C_P}$	10pF	$\boldsymbol{\delta}$	0.28
$\boldsymbol{I_P}$	250nA	$\boldsymbol{f_n}$	13KHz
$\boldsymbol{K_V}$	270KHz/V	$\boldsymbol{\kappa}$	1.3

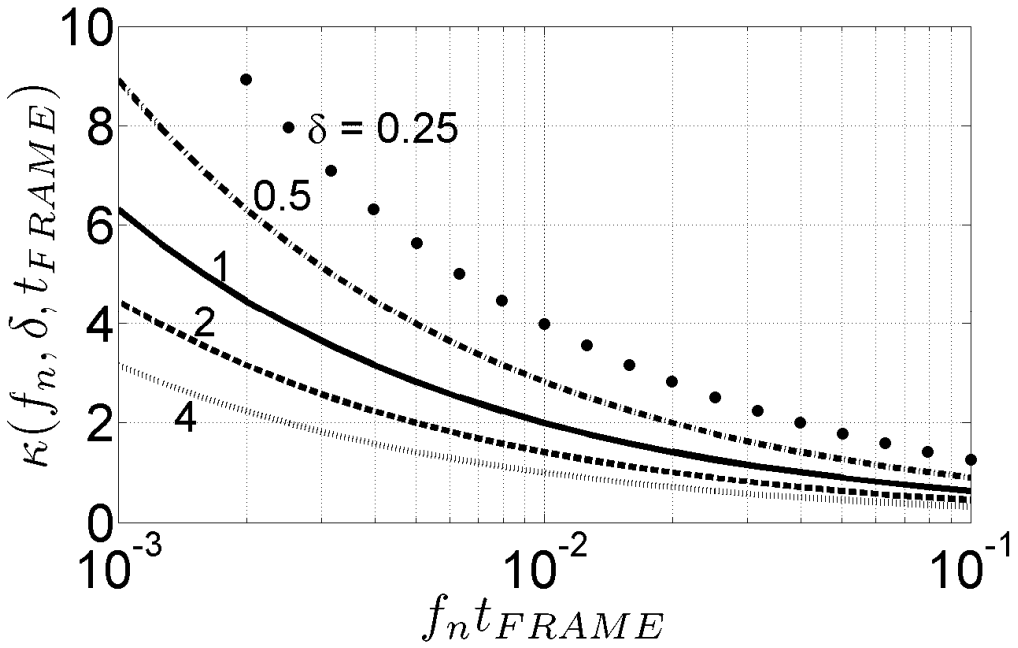


Figure 3.9. Theoretical PLL jitter multiplication factor $\kappa(f_n, \delta, t_{FRAME})$ as a function of normalized loop bandwidth $f_n t_{FRAME}$, for varying δ.

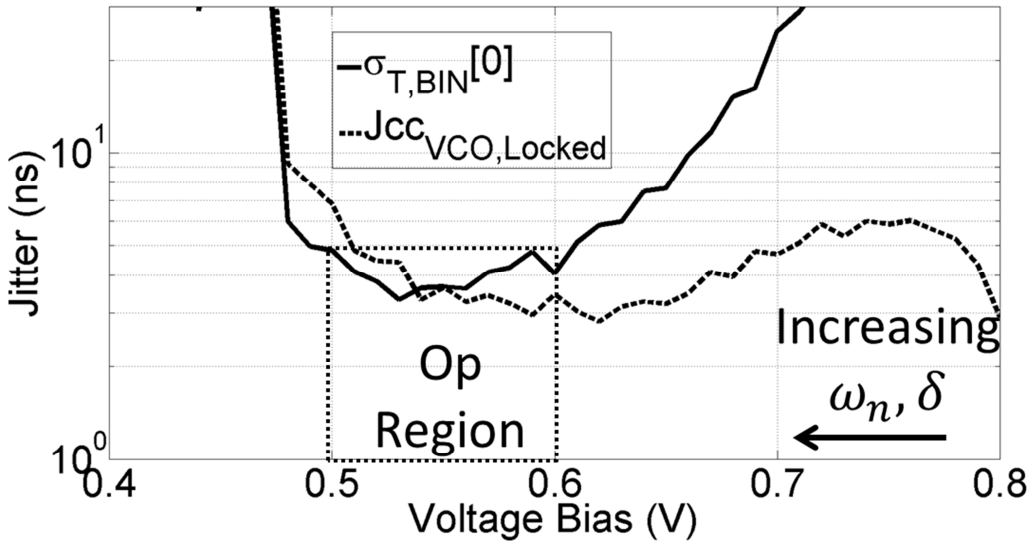


Figure 3.10. Measured PLL offset jitter and period jitter vs PLL charge pump bias voltage.

Figure 3.10 shows measurement data of the bin jitter for the 0th bin, $\sigma_{T,BIN}[0]$. We swept the charge pump bias voltage with higher I_P corresponding to lower voltages. We see drastic improvement in the offset jitter as I_P increases. The period jitter $Jcc_{VCO,Locked}$ on the other hand remains small as the loop bandwidth decreases. This is because the loop has little effect on the VCO jitter at timescales of one reference cycle. Thus $Jcc_{VCO} \approx Jcc_{VCO,Locked}$. In the nominal operating region between 0.50 - 0.6V, $\sigma_{T,BIN}[0]$ < 5ns, $\min(\sigma_{T,BIN}[0]) = 3.3ns$, while $\sigma_{T,Source} > Jcc_{VCO} \approx 3ns$, implying κ < 1.6 and validating our analysis. Jitter degradation occurs at high I_P because $f_n t_{FRAME} \rightarrow 1$, causing the discrete-time dynamics of the CP-PLL to become significant, invalidating the continuous model we used in the analysis [52].

3.3.3 DLL Offset and Jitter

We use a simple first-order DLL to segment the bin into 8 sub-bins. Jitter is accumulated though the delay line stages of the DLL. This additional jitter contribution is insignificant because it accumulates over the timescale of the bin, which is much shorter than the frame. Measurements of the DLL jitter relative to the start of the bin edge support this fact, showing that the additional jitter contribution is less than 20ps.

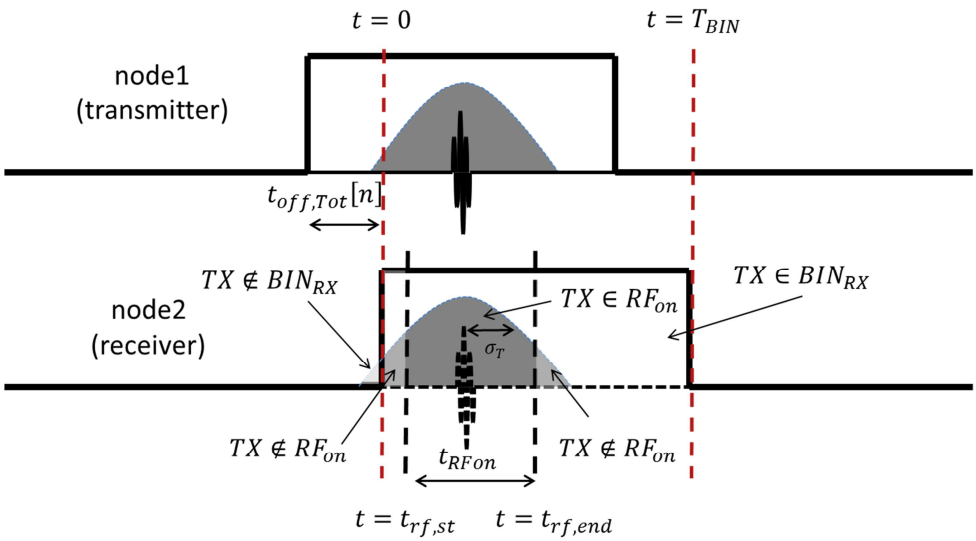


Figure 3.11. Transmit timing picture for node1 transmitting to node2.

3.3.4 Node to Node Timing Analysis

Consider two nodes in a synchronized state communicating in the n^{th} bin (Figure 3.11). Due to synchronization offsets and jitter, the bin times for the nodes will have some error. Assume that node1 is transmitting to node2, and that node1 is transmitting in the middle of its own bin. We wish to find the probability that this pulse is also in node2's n^{th} timing bin. To do this, we first find the n^{th} bin time offset, which is a sum of the PCO synchronization error ΔT_{12} and difference of the PLL locking errors of each node:

$$\Delta T_{BIN1,2}[n] = \Delta T_{12} + T_{ERR,PLL1}[n] - T_{ERR,PLL2}[n] \tag{3.15}$$

This can be broken down into deterministic offset and random jitter components as follows:

$$\Delta T_{BIN1,2}[n] = \Delta t_{12} + \mu_{Terr,PLL1}[n] - \mu_{Terr,PLL2}[n] + \Gamma_{12} + J_{Rel,PLL1}[n] - J_{Rel,PLL2}[n]$$

$$= t_{off,Tot}[n] + J_T[n] \tag{3.16}$$

Γ_{12} is the propagation jitter and $J_{Rel,PLL}[n] = T_{ERR,PLL}[n] - \mu_{Terr,PLL}[n]$ is the relative-jitter of the PLL derived previously. We've lumped all offset sources into $t_{off,Tot}[n] = \Delta t_{12} + \mu_{Terr,PLL1}[n] - \mu_{Terr,PLL2}[n]$ and all jitter sources into $J_T[n] = \Gamma_{12} + J_{Rel,PLL1}[n] - J_{Rel,PLL2}[n]$. Centering our time of reference at the start of the receiver's bin (Figure 3.11), we calculate the probability that the pulse lies in the bin as:

$$P(TX \in BIN_{RX}) = \int_0^{T_{BIN}} pdf_{\Delta T_{BIN1,2}[n]}(t)\, dt$$

$$= \int_0^{T_{BIN}} \frac{1}{\sigma_T \sqrt{2\pi}}\, e^{-\frac{(t - T_{BIN}/2 - t_{off,tot})^2}{2\sigma_T^2}}\, dt \tag{3.17}$$

Where $\sigma_T = std(J_T)$.

$P(TX \notin BIN_{RX}) = 1 - P(TX \in BIN_{RX})$ represents the bin *timing error rate* (TER) in our system and is a critical design parameter since it reflects the integrity of our data channels. We plot $P(TX \notin BIN_{RX})$ as a function of jitter for varying offsets

$t_{off,Tot}$ (Figure 3.12), assuming T_{BIN} = 52ns. We see that for TER < 10^{-3} the system requires σ_T < 8ns even for $t_{off,tot}$ = 0. Naturally, as the offset increases, then the jitter requirement becomes more stringent. If offset is excessively large, then the transmitter must mitigate this effect by using a different sub-bin to transmit.

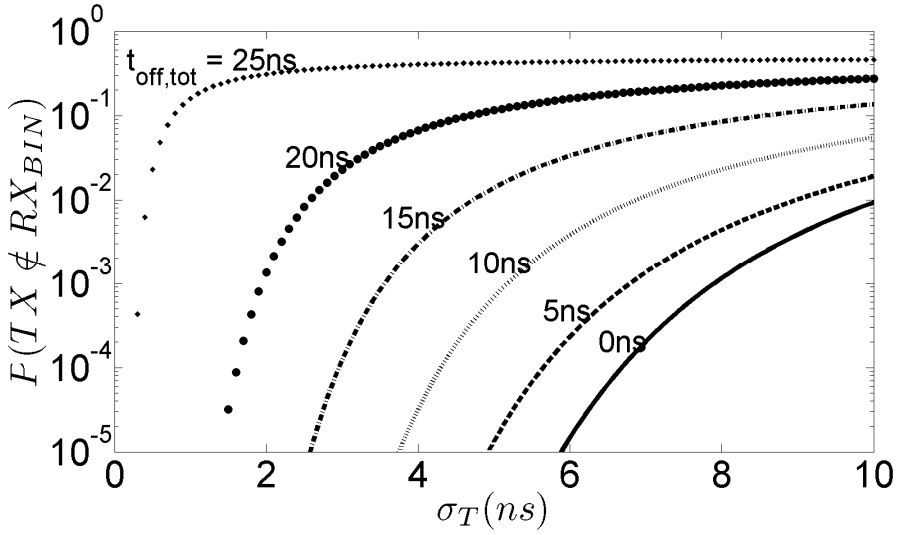


Figure 3.12. Timing error rate $P(TX \notin BIN_{RX})$ as a function of jitter for varying offset times $t_{off,tot}$.

In the highly duty-cycled *S*3 state, the RF-on window is shorter than a bin time in duration. If the RF turns on at $t_{rf,st}$ and turns off at $t_{rf,end}$ then we may similarly express the probability of bit detection in the *S*3 state as (Figure 3.11):

$$P(TX \in RF_{on}) = \int_{t_{rf,st}}^{t_{rf,end}} pdf_{\Delta T_{BIN1,2}[n]}(t)\, dt \tag{3.18}$$

Naturally $P(TX \notin RF_{on}) > P(TX \notin BIN_{RX})$ and is an additional mechanism to the overall bit-error-rate of the system. This error-rate in the sync bin also determines how long we can maintain synchronization. We measure $P(TX \notin RF_{on})$ through our synchronization duration tests in Section 3.6.3.

Assuming that jitter sources are uncorrelated, node1 and node2's PLLs have approximately the same characteristics, and recalling that propagation jitter is small compared to the period jitter, then σ_T may be expressed as[3]:

$$\sigma_T = \sqrt{\sigma^2_{T,BIN.PLL1} + \sigma^2_{T,BIN.PLL2} + \sigma^2_{T,\Gamma_{12}}}$$

$$\approx \sqrt{2\,\sigma^2_{T,BIN.PLL}}$$

$$\approx \sqrt{2}\,\kappa(f_n, \delta, t_{FRAME}) \sqrt{E[Jcc^2_{VCO}] + E[Jcc^2_{PCO}]} \qquad (3.19)$$

Recall from Eq. (3.2) that the duty cycle in the $S3$ state largely determines average power consumption and from Eq. **Error! Reference source not found.** that jitter in the timing system degrades the amount of duty cycling achievable in the $S3$ state. With Eq. (3.19) we may therefore relate the period jitter of the free-running PCO and VCO to the power saving that can be achieved via duty-cycling.

[3] This is in fact pessimistic. $J_{Rel,PLL1}[n]$, $J_{Rel,PLL2}[n]$ are positively correlated since they share the same PCO noise source so that $\sigma_T = std(J_T) < \sqrt{\sigma^2_{T,BIN.PLL1} + \sigma^2_{T,BIN.PLL2} + \sigma^2_{T,\Gamma_{12}}}$

3.4 Timing System Implementation

Based on the analysis of Section **Error! Reference source not found.**, we found that implementing ns-scale offset and jitter timing blocks is of critical importance to power-efficiency and communication robustness of our duty-cycled scheme. In this section we specifically describe the design considerations for the circuits that allows us to achieve those goals. These circuits dissipate nearly no static power and are implemented at low frequencies of 150KHz – 19.2MHz so that the combined power consumption is 25μW at $t_{FRAME} = 6.66\mu s$.

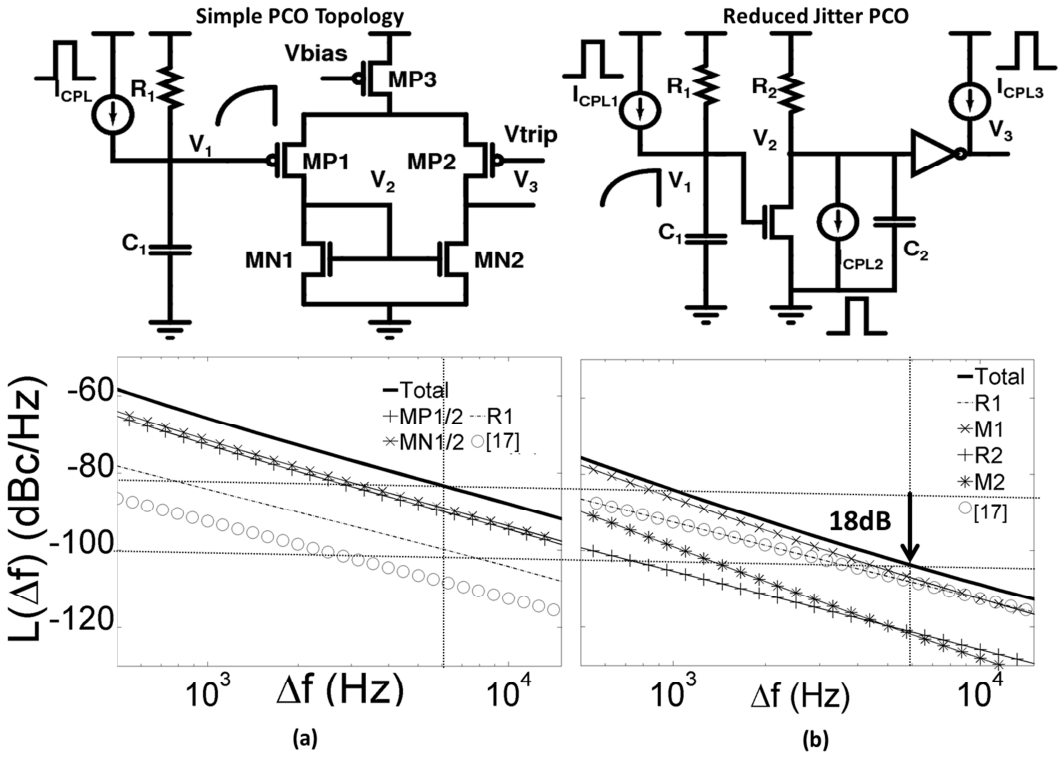


Figure 3.13. PCO circuit topology noise comparison between (a) the simple PCO implemented in Section 2.5, (b) modified reduced jitter PCO

3.4.1 PCO Circuit Design and Implementation

For the data rates we desire in the system using 1 data pulse per frame, the PCO must operate between $100 - 200\ KHz$.. The oscillator must also implement impulsive coupling to implement the PCO synchronization. These requirements strongly suggest we use the relaxation oscillator topology shown in Figure 3.13a with coupling implemented as direct charge injection into oscillation node. The phase noise of this topology is known to be dominated by the phase noise contribution of the comparator [53]. A SpectreRF simulation of phase noise contributors confirms this observation (Figure 3.13a), where it can be seen that the phase noise contribution of each of the comparator transistors is 15dB in excess of that of the resistor in the white noise

region of the phase noise spectrum. The theoretical contribution [53] from the resistor alone is plotted in white circles as well. Replacing the comparator with a common source-amplifier-inverter cascade greatly increases the signal swing at V2 from 20mV to 400mV. We also introduce 2pF of capacitance to further stabilize the node. The corresponding effect on the phase noise can be seen in Figure 3.13b where the phase noise contribution from the transistors is reduced so that overall phase noise is 5dB in excess of that of the resistor. We also design the oscillator so white noise sources contribute 4x more phase noise than the $1/f$ sources at an offset $f_0/25$ from the carrier. This guarantees that the jitter *time* corner, where the regions of 0.5 and 1 slope jitter accumulation intersect, is longer than the PCO period [50]. We accomplish this by using 1μm length transistors for the first three stages.

Since the phase noise is dominated by white sources, the rms period jitter of the PCO may be calculated from the phase noise $L(\Delta f)$ by [54]:

$$\sigma_{JCC,PCO} \approx \sqrt{L(\Delta f)\,\frac{\Delta f^2}{f_0^3}} \tag{3.20}$$

The overall phase noise of the design was simulated to be $10\log\big(L(\Delta f)\big) = -103\ dBc/Hz$ at $\Delta f = f_0/25 = 6KHz$, corresponding to a jitter of ~700ps. The measured result (Figure 3.7) is 1.1ns, in fair agreement. The 0.5 slope jitter accumulation persists on the order of a few cycles as well (Figure 3.7), indicating our circuit is operating in the white noise dominated region. Measured power consumption of this circuit was 3μW at 150KHz.

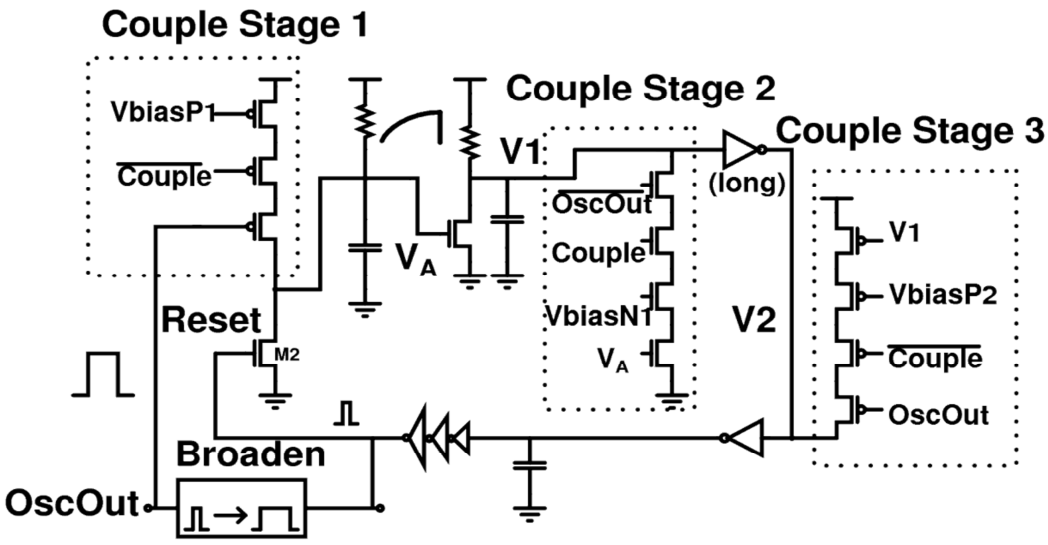


Figure 3.14. Complete PCO implementation showing implementation of the coupling branches and the reset path

The full implementation of the PCO oscillator circuit is shown in Figure 3.14. The coupling is implemented by multi-node current injection. The polarity of the current injection is chosen to advance the phase of the oscillator (shorten the period). The transistors are chosen to be strong enough to immediately couple the node to threshold upon detection of the synchronization pulse. Care must be taken to fully discharge node V_A at the end of every PCO cycle, since a partial discharge is highly detrimental to the jitter.

3.4.2 PLL Design and Implementation

While we use the standard CP-PLL architecture the requirements of low synchronization offset and jitter influence the design considerably. From our analysis in Section 3.3.4, there are rather stringent requirements on the timing offset, which is partially dependent on the PLL timing offset. This motivates us to precisely quantify the effect of the different sources of locking-time offset at circuit level.

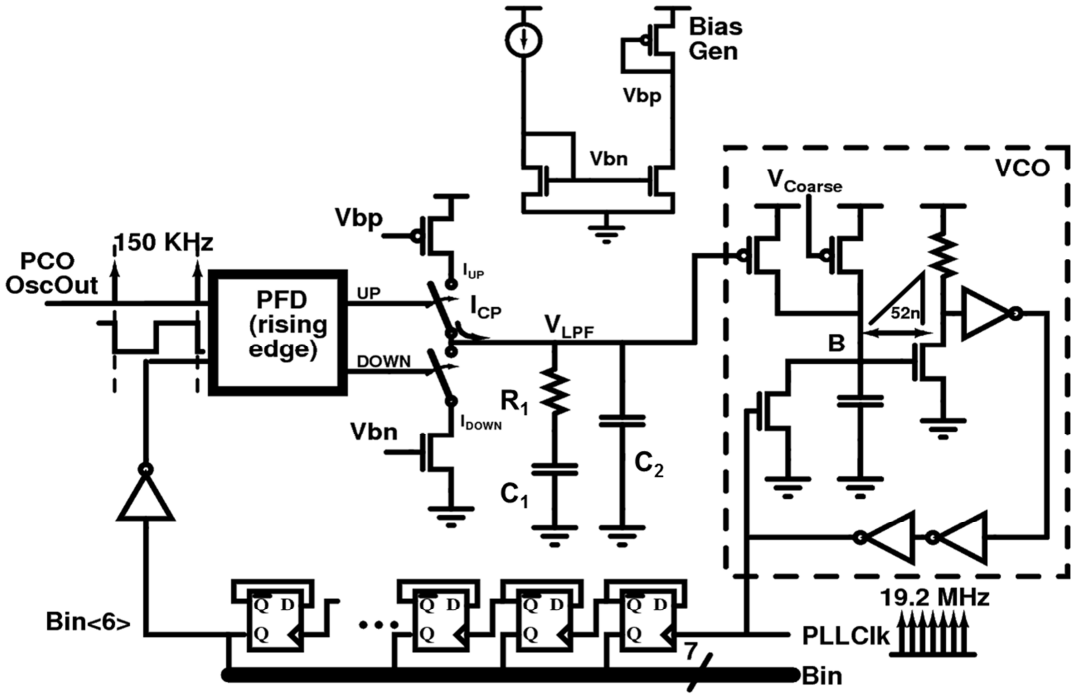


Figure 3.15. PLL Implementation with relaxation-oscillator based VCO

In a periodic steady state the total charge in the loop filter must be conserved at the end of a cycle such that:

$$\int_{0^-}^{t_{frame}} \left(I_{CP}(t) + I_{inj}(t) + I_{mis}(t) + I_{leak}(t)\right)dt = 0 \qquad (3.21)$$

If we assume the charge pump current $I_{CP}(t)$ is a constant I_P or I_N for up/down phase-frequency detector for a phase error time $\mu_{Terr}[0]$, a mismatch current of $I_{mis} = (I_P - I_N)$, during the overlap time of t_{ov}, charge injection that occurs nearly instantaneously such that $I_{inj}(t) = Q_{inj}\delta(t)$ and constant leakage current such that $I_{Leak}(t) = I_L$, then we may write

$$\mu_{Terr}[0] = \frac{Q_{err}}{I_{PN}} = \frac{-(I_L t_{frame} + I_{mis} t_{ov} + Q_{inj})}{I_{PN}} \quad (3.22)$$

where $I_{PN} = I_P$ or $-I_N$ depending on the sign of $\mu_{Terr}[0]$. Eqn. (14) shows that increasing charge pump current I_P or I_N reduces the time error for an given amount of error charge Q_{err}. Q_{err} contains leakage, mismatch and charge injection components. If we assume α mismatch in I_P, I_N such that $I_P = \alpha\, I_N$, Q_{inj} to be estimated by $Q_{inj} = (C_{db-p} + C_{db-n})VDD/2$. We plot the components of t_{err} based in Eq. (3.22) in Figure 3.16 versus leakage current (from 0-1nA), mismatch factor (α = 0.25-10) and charge-pump transistor width (from 0-1 μm) assuming $VDD = 1, C_{db} = 1fF/\mu m$, $t_{ov} = 25ps$ and $I_P = 300nA$. The plot shows that leakage current and charge injection sources contribute ns-scale offset components whereas mismatch current is much lower. This can be explained by the combination of long t_{frame} and small I_P unique to our application. This leads us to use minimum *width*, 1μm length transistors in the charge pump with simple mirroring biasing, which reduce charge injection and leakage current. We also use thick-oxide devices for the VCO control gate, since standard thickness devices have excessive leakage around $1nA$ / μm in this process. The measured result of the PLL timing error for each bin is shown in Figure 3.17. Bin timing error is less than 5ns for all bins.

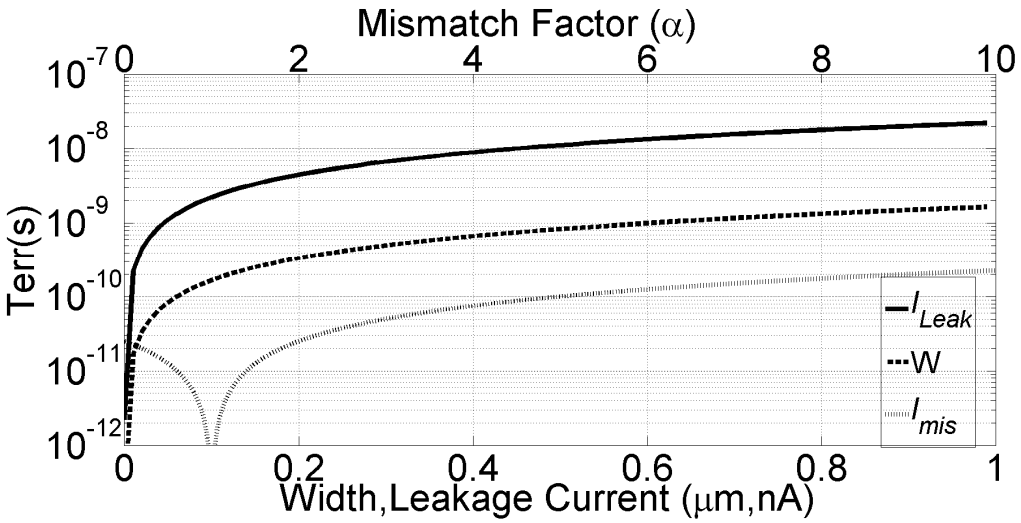


Figure 3.16. CP-PLL offset time dependence on the various circuit-level non-idealities.

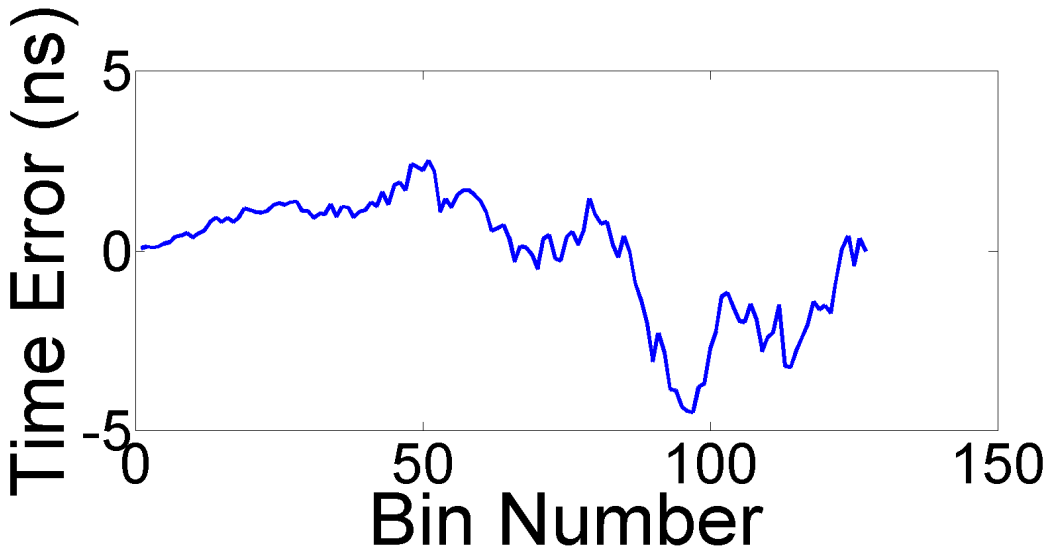


Figure 3.17. Measured timing offset vs bin number

3.4.3 Timing Generator Circuit

The PLL subdivides the PCO frame into time bins of 52ns through the 128 unique states of the counter output. When a bin is active, a pulse of width 52ns is sent to a delay-locked-loop (DLL) which subdivides the bin into 8 sub-bins of 6.5ns by delay-locking the rising edge of bin to its own falling edge. The sub-bin interval is the time window between rising edges of successive stages of the delay line (Figure 3.18). The same bias voltage output of the DLL is used to bias three seperate delay lines, generating dedicated sub-bin intervals for data (RX) and synchronization (SYNC) pulse reception and pulse transmission (TX). For the RX and Sync bins, the taps of the delay-line are fed into a 8-bit DFF register and clocked with the received pulse, providing the means to estimate the received pulse to within 6.5ns precision. For the *TXBin*, the delay-line taps are fed into an 8-1 mux whose output is used to trigger the transmitter. This allows data to be transmitted at the leading edge of any of the 8 sub-bins which can be used to compensate static synchronization phase offsets. OOK modulation is accomplished by masking the transmit trigger with the data bit. RF receiver duty-cycling control in the RX and Sync bins is implemented off the *Data/SyncBinActive* edge. First the rising edge of the active bin is pushed back through a voltage-controlled delay line. The rising edge generates a glitch which is then broadened by voltage controlled pulse-widening circuit. The result is a RF-On window that is used to control the fast turn-on receiver. The duty-cycling mechanism is only active when the system is in the synchronized state. Once synchronized, the system switches from being sensitive to the synchronization pulse to being sensitive to the data pulse at conclusion of Bin 0 (first bin) in the cycle, and switches back again after the Tx/Rx bin within the frame.

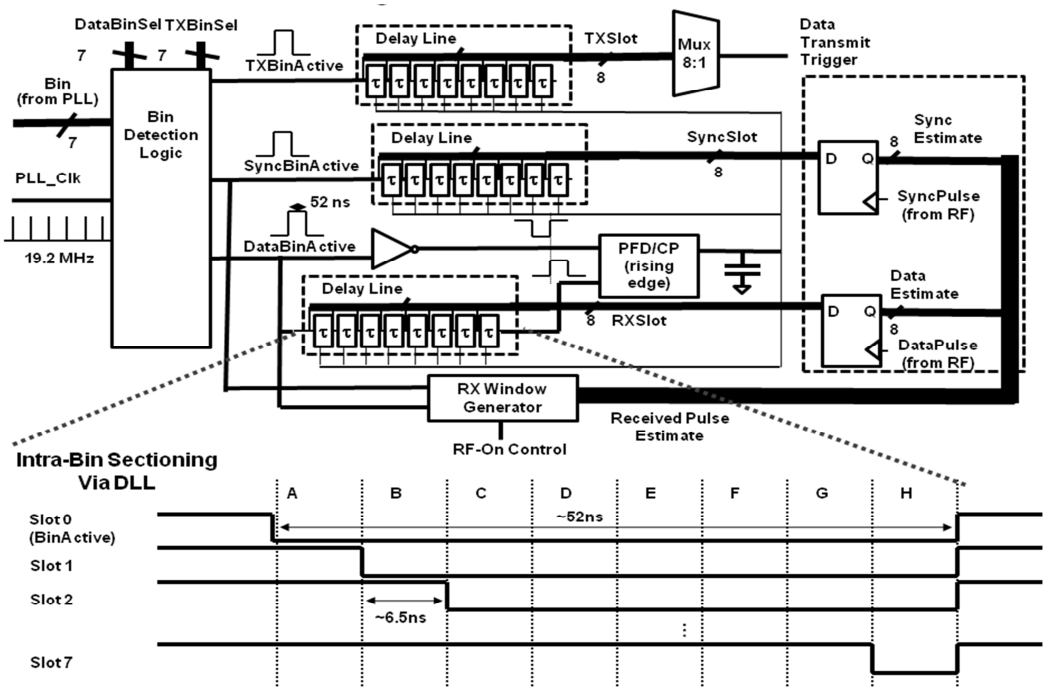


Figure 3.18. Sub-bin generation circuit for transmission control and pulse offset estimation

3.5 Loss of Synchronization and Recovery Transients

When the network is synchronized, the PLL of each node will be phase locked to its PCO. Each node implements an integrated PCO/VCO overlap monitoring circuit as well as a sync pulse detected signal to decide its duty cycling state. These signals are the input to a synchronization management finite state machine implemented on FPGA as in Figure 3.19 to detect synchronization and recover from its loss.

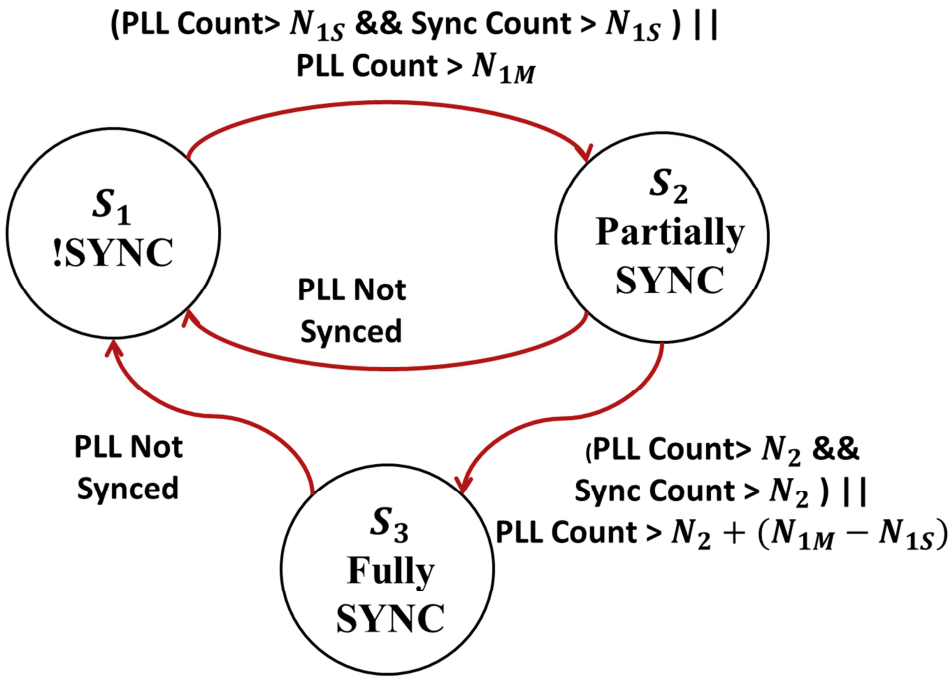


Figure 3.19. Synchronization Control FSM

Nodes transition from the unsynchronized state S_1 to the partially synchronized state S_2 if the PLL has been locked for N_{1S} consecutive cycles and the sync pulse has also been detected for N_{1S} consecutive cycles. The master node will not detect the synchronization pulse in the synchronized state however since the slave nodes fire in its refractory period. Thus the master node transitions to the synchronized state if the PLL is locked for $N_{1M} > N_{1S}$ cycles. In the S_2 state, the node transmits both data and sync pulses and uses the full bin width for pulse detection. During the S_2 state, we estimate the offset of the sync pulse in slave nodes. This estimation phase takes $N_2 - N_{1S}$ cycles to complete. Once offset estimation for the sync pulse is completed, the node transitions to the S_3, fully synchronized state, where the RF-window is active for less than a bin in width.

If a node does not detect the sync pulse for a single cycle, then the PCO will not be coupled during that cycle and will have a longer period as a result. The PLL locking to the PCO will detect this as a large step-phase jump at its input and will undergo a transient response. Any node synchronized through this node will then have its synchronization thrown off as well and therefore also undergo its own transient. If no subsequent missed detection of the PCO occurs, then PLL eventually locks to the synchronized PCO and the system returns to a synchronized state. Figure 3.20 shows a measurement of the re-synchronization transient process in a two node system operating with t_{FRAME} = 7.2us. At ~2.1093s, the PCO pulse is misdetected by the slave, which causes a ringing second-order phase-step transient response in the PLL. The PCO synchronization is then recovered and the PLL regains lock to the PCO after 85us. The node can gauge its synchronization status based on whether its PLL is locked and if sync pulses were detected.

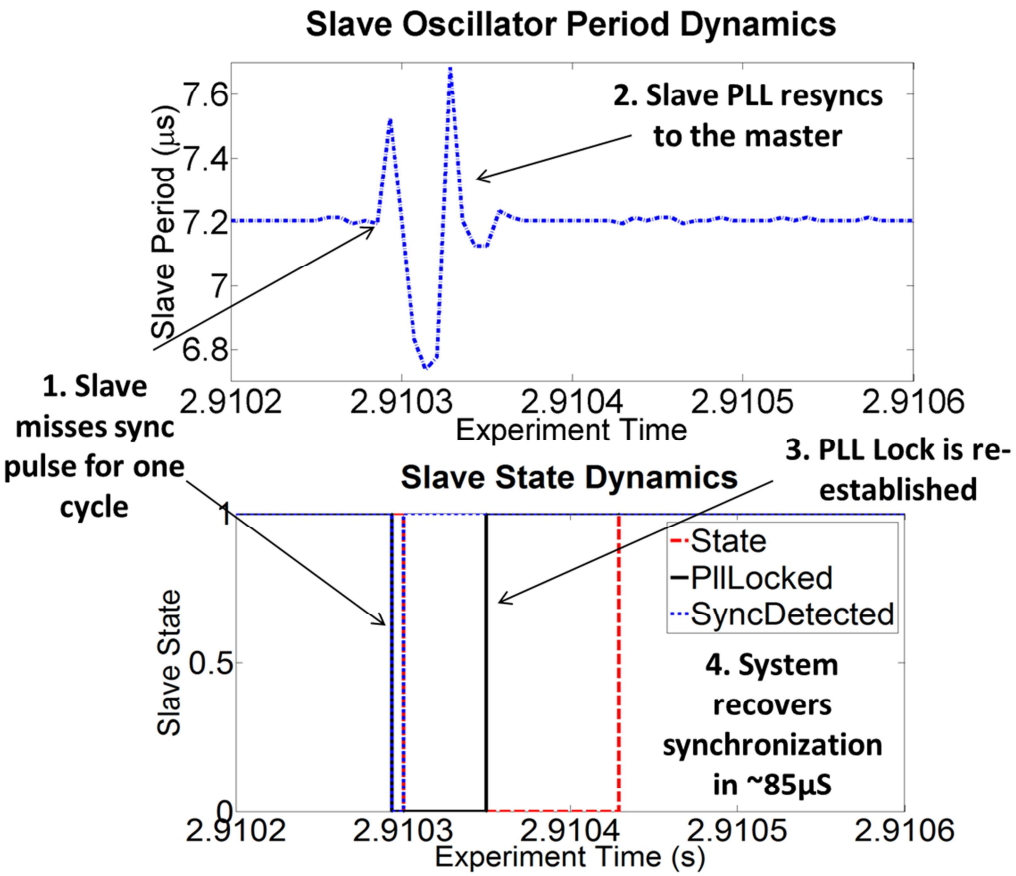


Figure 3.20. Measured system resynchronization dynamics with state-machine

We took the synchronization measurement over 65 seconds of a wireless 4-node PCO system described in this paper and fabricated in IBM 90nm process. (Figure 3.21) The 4-node PCO system is connected in a line configuration. We induced sporadic bit detection errors in the system by reducing the receiver sensitivity. We found that the global synchronization can be maintained and recovered by the FSM we described. The time of desynchronization events in the slave nodes are also highly correlated, suggesting that the slaves go out of sync and in-sync all together. This motivates the analytical model we will describe in Chapter 4.

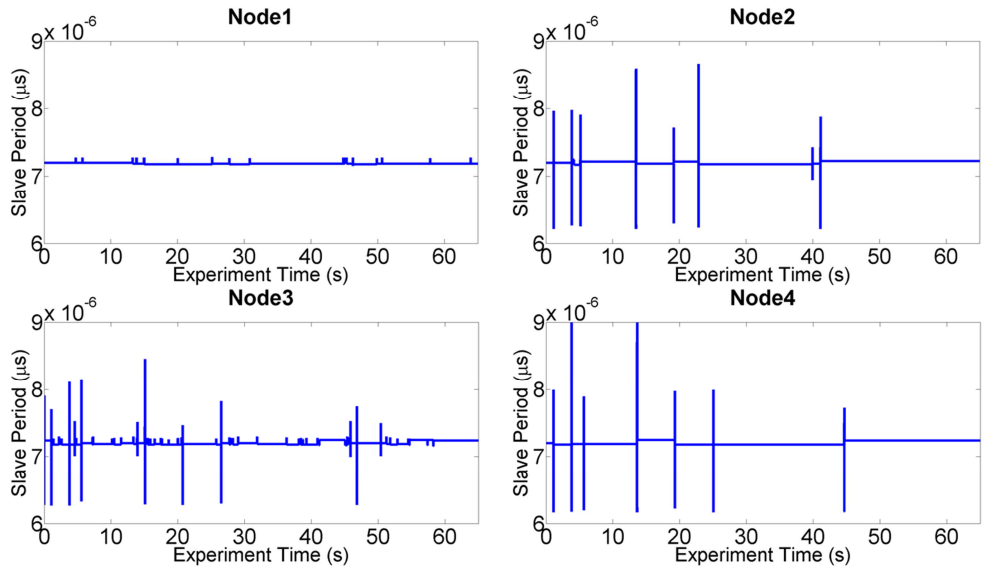


Figure 3.21. Four node synchronization transient measurement over 65 seconds using S_1 and S_2 states of the synchronization FSM.

3.6 Transceiver System and Network Testing

Our transceiver system was fabricated on the IBM CMOSRF process and wirebonded on a 144-PGA package mounted on a FR-4 PCB board connecting to a DE2-70 FPGA development board utilizing an Altera Cyclone-II FPGA with an on-board NIOSII processor (Figure 3.22). The FR-4 board includes SMA connectors for the rx/tx antennas. The chip uses a standard 3-wire SPI control interface for setting configuration and control bits for the system. We output the PLL 150KHz clock in order to synchronize the radio chip with FPGA system. We also provide digital pll-lock status and the synchronization-detected signals as inputs to the FPGA-based synchronization management FSM as well as the raw data stream received. The NIOSII processor communicates via RS-232 to a MATLAB control terminal and translates MATLAB commands into SPI writes to the radio. The FPGA implements a Verilog recorder module which is used to record the digital events in the system as

well as measure the period of the oscillators. The recorder is capable of 5ns precision and its outputs are stored in 64MB of SDRAM. With event-based data recording, measurements can be conducted over timescales of minutes. Measurements demanding more timing precision than this were performed by an Agilent DSO90254A real-time oscilloscope with 20GSPS sampling rate and 52Msamples memory depth.

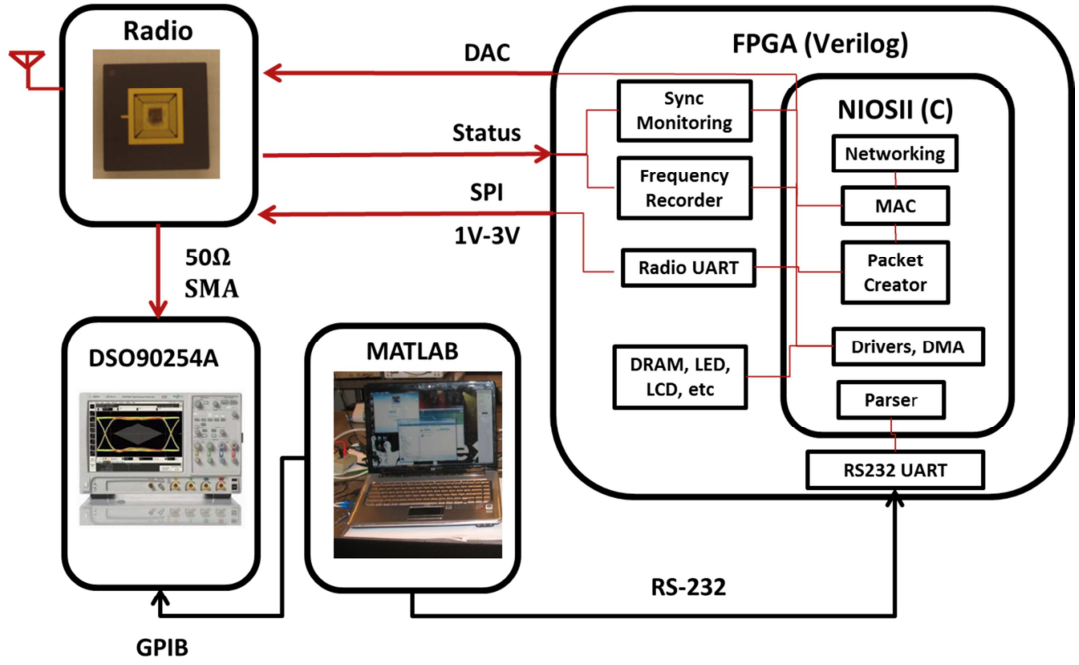


Figure 3.22. Block diagram showing the component of each radio board in our test setup.

3.6.1 Packet Structure

We show that the system built around PCO synchronization is viable and compatible with traditional digital radio data transfer concepts by defining a simple

packet structure to organize data transfer. We created two types of packets, a 13-byte data request packet and a configurable-length payload data transfer packet, as well as 2-byte acknowledgement packets for each. Each packet type has a dedicated 48-bit start-of-packet symbol. The request and transfer packets also contain a 16-bit CRC to check for packet integrity. For additional robustness, each data bit was encoded with an $R(1,3)$ repetition code.

3.6.2 Backend Blocks

We implemented a simple receiver baseband block on FPGA in Verilog. The baseband block consists of four parallel digital correlation circuits which correlate an incoming raw data-stream against known start-of-packet values. When the correlation peak is greater than the threshold, a correlation valid signal is sent to the FPGA which then enables the majority-vote decoder. On the transmit side, the parallel data from the FPGA is sent to an $R(1,3)$ encoder and serialized into our transceiver. The logic blocks we implemented in FPGA are of low-complexity and are clocked off the 150KHz PLL output. Thus we expect the power penalty to implementing these circuits on chip should be minimal.

The NIOSII processor on the FPGA implements the synchronization FSM of Section **Error! Reference source not found.** as well as separate state machines controlling data rx/tx, and packet processing. If PCO synchronization is lost in the middle of a data-packet the packet is retried from the beginning.

3.6.3 Synchronization and Data Transfer Tests

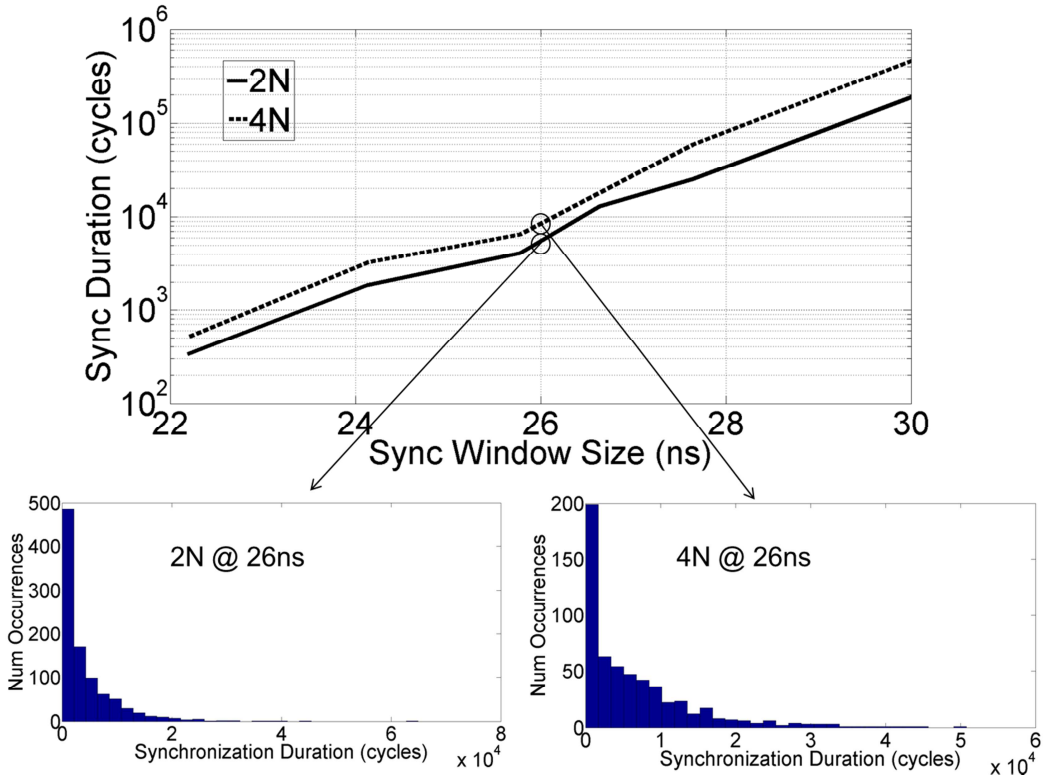


Figure 3.23. Average duration of a node in the S_2 (synchronized) state vs RF-on window size

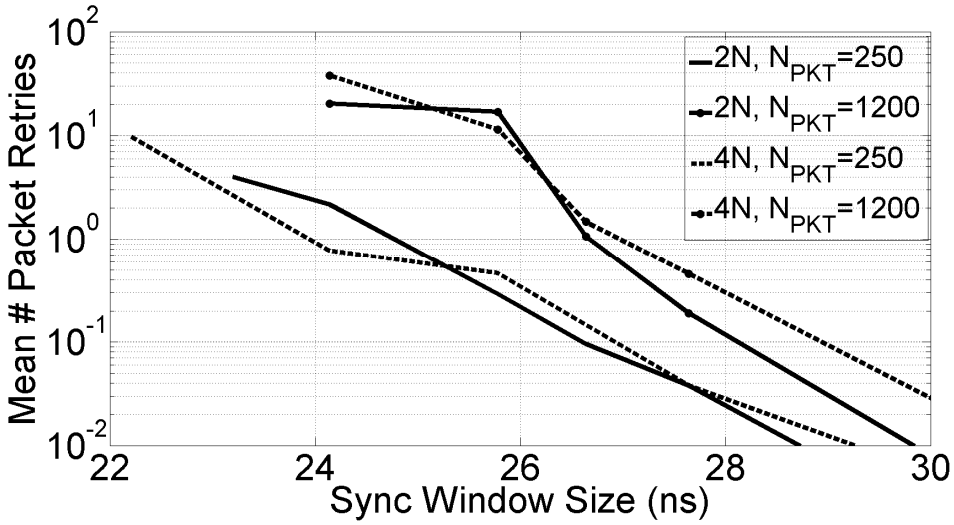


Figure 3.24. Average number of packet retries due to loss of PCO synchronization for $N_{PKT} = 250, 1200$ in two node and four-node PCO networks

We performed characterization of the synchronization using a two-node and four-node PCO synchronized transceiver system connected in a line configuration. If a nodeB is synchronized to the master through another nodeA, then we say that nodeB is downstream of nodeA. The PCOs were synchronized with the PCO master clock period of 7.2μs (140KHz) and operate with a simplified version of the synchronization FSM with states S_1 and S_2. The RF-on window time in the S_2 state is a fixed value. We first operate the transceivers in a region where there are reliably no loss-of-synchronization events during a 10 million cycle (72 second) test, under a condition of no-duty-cycling. This allows us to estimate nominal sync-error-rate due to bit-energy for the individual links at $< 10^{-7}$. We then gradually introduce synchronization errors in the network by reducing the RF-on window time (t_{RFon}) in the S_2 state of the slave closest to the master (Figure 3.23). We see that in the range from 22-30ns the average duration of synchronization increases immensely with increasing RF window

widths due to the Gaussian distribution of the jitter. At 30ns RF-on window times, the synchronization duration is on the order of seconds. The result is similar for both two-node and four-node cases, indicating loss of synchronization of downstream nodes does not affect up-stream nodes. The time spent in the synchronized state follows an exponential distribution (Figure 3.23), suggesting that the synchronization may be modeled by a Poisson process

We quantify the effect of the probabilistic loss of PCO synchronization on packet transmissions by measuring the average number of packet retries per packet transmitted. We perform this measurement on packets with lengths N_{PKT} of 250 and 1200 coded bits (Figure 3.24). The results are consistent with the measurement of the average time of synchronization, showing that two-node and four-node networks have similar characteristics. Unsurprisingly, the longer packet type suffers from a higher number of retries. The transmission retries become exponentially more frequent as the average synchronization duration approaches the packet duration. The number of packet retries becomes negligible when $t_{RFon} > 30ns$ for both packet lengths and synchronization network sizes. The measured combined timing jitter for this test was $\sigma_T = 4.1ns$, suggesting that the RF window size should be set to at least 9-10 times the timing jitter to maintain robust synchronization.

As a final test of the robustness of our communication system, we successfully transmitted a 36KB image file using 64 byte packet payloads down the entire line of nodes through multiple hops. Each node was duty cycled with full-bin RF windows on sync and data bins.

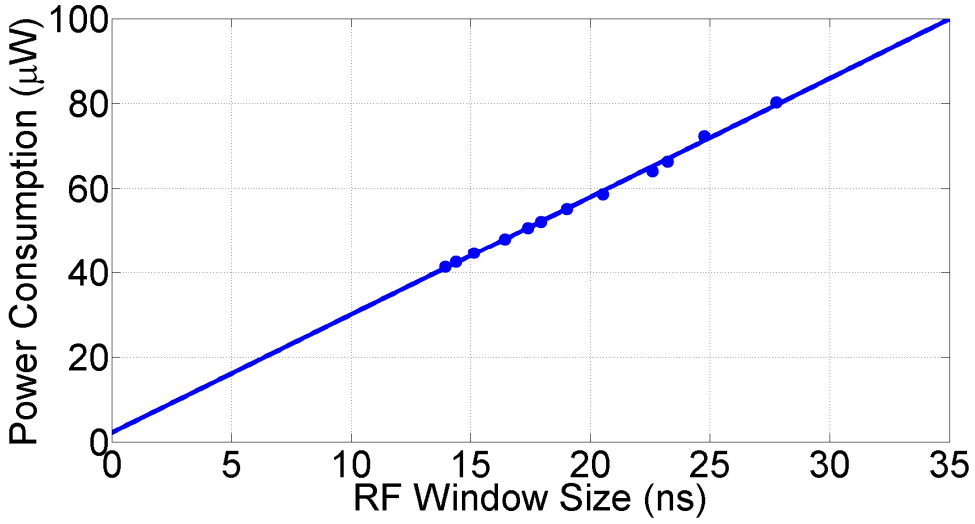


Figure 3.25. Power consumption at 140KHz as a function of RF window size

Table 3.3. Component Power Breakdown

Block	Power @ 140KHz	Block	Power
RX	86μW	$Timing$	10μW
TX	8.5μW	PCO	6.5μW
PLL	7.5μW	TOTAL	119$\boldsymbol{\mu W}$

3.6.4 Power Consumption

We measured the power consumption of the receiver designed by my colleague Rajeev Dokania [17] for varying RF-on window times at our operating rate of 140KHz (Figure 3.25). For this measurement, we performed two RF window openings of equal width, once for the data bin and once for the sync bin. A line of best fit with $R^2 = 0.998$ is also shown. Receiver power consumption is under $100\mu W$ for $t_{RFon} < 35$ns. Power consumption at $t_{RFon} = 30ns$, the operating point where we measured robust performance in the two and four node cases, is $86\mu W$ and thus this is the power

that we quote for our RF receiver. The power breakdown by component is shown in Table 3.3. Overall transceiver power consumption while actively transferring data through sending and receiving packets is $119\mu W$. Power consumption is dominated by the receiver, even with the duty cycling enabled. The limiting factor in this case appears to be the PLL cycle-to-cycle jitter. We believe that this scheme is capable of achieving sub-100 μW overall power consumption with the jitter more tightly controlled.

A comparison with other recent works in low power transceivers is shown in Table 3.4. Our work achieves the lowest total power consumption of any complete transceiver, with competitive RX sensitivity and energy per bit. In terms of receiver power consumption, only the wake-up receiver of [5] is lower. However, [5] is designed for asymmetric links where the transmitter is assumed to be of higher power so the power of the complete transceiver system is unknown. The use of IR-UWB allows much lower overall power consumption at the transmitter due to the inherently efficient duty-cycling

Our low-leakage, simple pulse-shaping transmitter shows the great benefit of UWB-IR on the transmission side, consuming about 40 times less overall power relative to narrowband transmitters [2][7][12] for similar instantaneous power levels. This is a direct consequence of the 2ns pulse duration of UWB-IR and potentially allows us to compensate our lower sensitivity receiver with a higher transmitter output level in the overall link-budget. FSK-CW transmitters [7] by contrast cannot be duty cycled at the bit level, while narrowband OOK systems such as [2][12] allow only limited duty cycling of the transmitter, since the signal duration must be at least on the order of the inverse of the bandwidth of the system, (a few µs). As a result, our overall power consumption is the lowest reported of any complete transceiver.

Table 3.4. Power Comparison With Recent Low-Power Transceivers

Work	RX Type	BW	RX + Timing Power	Data Rate	RX (E/b)	RX Sens.at Data Rate	RX Sens. (100K)	TX Power
[7]	2-FSK-CW	1MHz	330μW	300K	1.1nJ	-98	-98	0.7mW
[5]	OOK-CW	600KHz	52μW	100K	0.5nJ	-72	-72	NA
[2]	OOK-SR	500KHz	400μW	5K	80nJ	-101	-88	1.6mW
[55]	OOK-SR	900KHz	2.8mW	500K	5.6nJ	-80	-87	NA
[12]	OOK-SR	300KHz	400μW	120K	3.3nJ	-93	-94	350uW
[26]	PPM-IR-CW	17.7MHz	415μW	500K	0.8nJ	-82	-90	NA
[13]	PPM-IR-UWB	500MHz	250μW	100K	2.5nJ	-98	-98	NA

[16]	PPM-IR-UWB	500MHz	1.64mW	1M	1.64nJ	-65	-75	250uW
[14]	PPM-IR-UWB	500MHz	11mW	16M	0.7nJ	-50	-72	NA
[15]	PPM-IR-UWB	500MHz	4.2mW	19.5	0.2nJ	-69 @ 1.3Mbps	-82	NA
This Work	OOK-IR-UWB	500MHz	110μW	140K	0.8nJ	-85	-87	8.5uW

Chapter 4

UWB NETWORKING ANALYSIS

4.1 Introduction

This chapter investigates the network-wide effects of UWB synchronization in globally duty cycled IR-UWB networks where a reference clock is transmitted and the periods are subdivided into time bins. We assume in this network that there are two major error mechanisms: the missed detection of the pulse due to inadequate signal energy, and a synchronization error, causing the RF-ON window to be turned on at the wrong time. We assume that these mechanisms are present for both the SYNC and DATA pulses. We denote the probability of failure due to those two mechanisms BER and SER respectively.

For the simple first order analysis, we assume a discrete model for the network. Each cycle the nodes probabilistically detect a pulse with a finite probability of error. The probabilities of errors are given by the parameters BER, a fixed bit error rate, and $ser(D)$ the sync error rate as a function of the RF duty cycle D

4.2 Probability of Network Synchronization with Finite Bit and Sync Error

We derive the UWB network properties with communications between the nodes abstracted as follows:

Assume that the bit transmissions have the following properties:

- Two types of pulses are present in the system and orthogonal to each other: The synchronization pulse and the data pulse
- Two error mechanisms are present: a Bit-Error, due to the traditional missed detection of the pulse and a Sync-Error due to a timing error

- Assume that bit and sync errors are independent of each other.
- Assume that each cycle is independent of the previous cycle.

Assume we have an N Node PCO network with the following properties:

- Each cycle, every node in the network must detect a synchronization pulse to remain synchronized. If one node fails then the network loses synchronization
- Nodes can only transmit and receive data if synchronized
- Network consists of three states *S1, S2, and S3*:
- The network has a $count$ variable. $count$ is increased by one each time all nodes hear the synchronization pulse and thus models the synchronization duration of the network. If the network loses synchronization then count is reset to 0.
- In State S_1 there is no synchronization error (reflecting that the node is fully on), so the error only consists of the bit error. We jump from S1 to S2 after $count = N_1$. We assume that when $count = N_1$ that the network still has the probabilities of the $S1$ state.
- In State S_2, the nodes are open for a duty cycle of 1 bin. Communication of data packets starts in $S2$. There is SER due to the finite bin width, but by design, the bin width should be large enough that SER is small compared to BER in this state. This SER is dependent on the offset of the pulse from the bin edge. Transition from S2 to S3 occurs after $count = N_2$, so $count = N_2$ retains the probabilities of the S2 phase. State $S2$ models a *synchronization estimation* period
- In State S_3, the nodes are aggressively duty cycled **after an estimation phase.** In this state, SER is allowed to be larger than BER, and our goal is to find how large a SER is tolerable.

4.2.1 Network Error Rate

Based on the properties of the network above, we will now derive the single-cycle network error-rate (NER) for a network of N nodes as a function of the BER and duty cycle (D), offset estimation error μ and network timing jitter σ. The timing jitter is assumed to be a Gaussian random variable. The parameters are defined as follows:

- BER : The bit-error rate of the system
- D : The single rf-bit event duty cycle of the system. Thus if the system has an average period $T_0 = 10\ \mu s$ and an RF-on time $T_{RF} = 10ns$ to detect a bit, then $D = 0.001 = \frac{T_{RF}}{T_0}$
- σ : The rms single-cycle jitter of the network.
- μ : The offset of the pulse from the center of the RF opening.

The synchronization error rate $SER(\mu, \sigma, D)$ is a function of μ and D. Since D depends on the state of the network, the NER changes with the state of the network as well. We assume that each node in the network is in error independently from the other nodes in the network so that

$$NER = 1 - (1 - TER)^N \tag{4.1}$$

Where TER is the single node total error rate for one cycle. TER assumes that bit-error and sync-error are independent events such that:

$$TER = 1 - (1 - BER)(\ 1 - SER(\mu, \sigma, D)\ ) \tag{4.2}$$

SER is found by integrating a $N(\mu, \sigma)$ distributed random variable from $(-\infty, -\frac{D}{2})$ to $(\frac{D}{2}, +\infty)$. This models the probability of a pulse of offset μ and jitter σ falling out of the RF-on range of $[-\frac{D}{2}, \frac{D}{2}]$. This turns out to be:

$$SER(\mu, \sigma, D) = 1 - \frac{1}{2}\, Erf\left(\left(\frac{\frac{D}{2} - \mu}{\sqrt{2}\,\sigma}\right) + Erf\left(\frac{\frac{D}{2} + \mu}{\sqrt{2}\,\sigma}\right)\right) \tag{4.3}$$

Where $Erf(x)$ is the standard error function.

States 1 , $S2$, and $S3$ in this model are distinguished by their different μ and σ. Thus the NER is a function of the state the system is in. Define the network bit detection probability:

$$P_i = 1 - NER(S_i)\,, \quad i = 1, 2, 3 \tag{4.4}$$

Note that in state S_1: $D = \infty$ so that $SER = 0$, while in state S_2 we assume $D \gg \mu, \sigma$. For state S_3, we make no assumptions about the scale of the parameters. Thus we insist that:

$$P_1 > P_2 > P_3 \tag{4.5}$$

4.2.2 Markov Chain Model for Synchronization State

Recall that in the network, we have a $count$ variable describing the number of consecutive cycles of synchronization. $count$ passing thresholds N_1, N_2 determine the transition from $S_1 to\ S_2$ and S_2 to S_3 respectively. If synchronization is lost at any point, then $count$ resets to 0. Based on this definition of count in the system, we can model the synchronization state dynamics with a Markov Chain. Define the following Markov Chain based on the $count$ variable as follows:

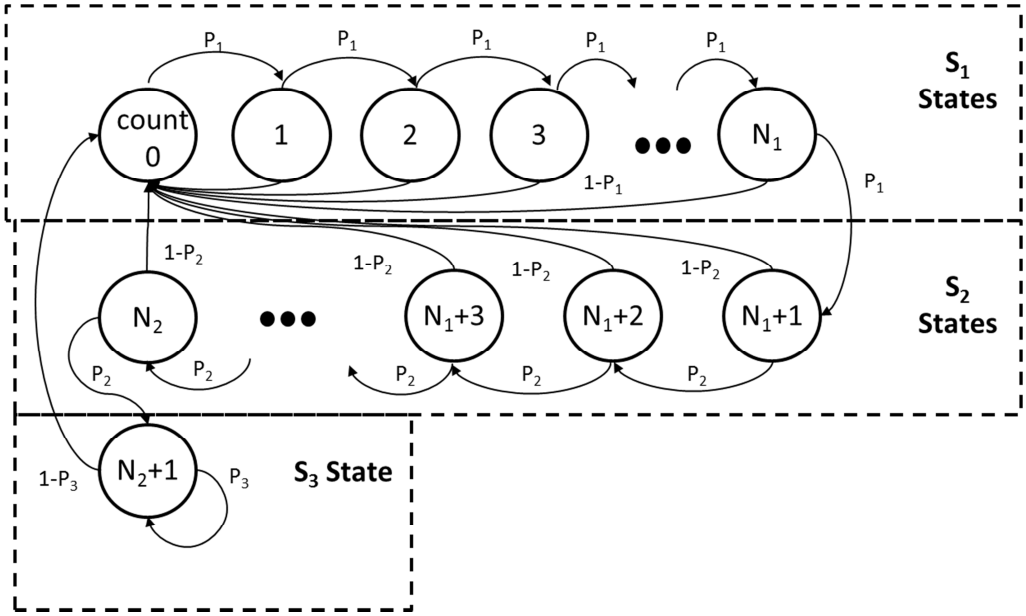


Figure 4.1: Markov chain for the count variable modeling the system synchronization

We define the system as being in:

State S_1 : $count \leq N_1$,

State S_2 : $N_1 < count \leq N_2$,

State S_3 : $count > N_2$

By inspection, we can see that the Markov chain above is *irreducible* and *recurrent*, and thus must admit a stationary (steady-state) probability distribution vector $\underline{\pi} = \left(\pi_0, \pi_2, \ldots \pi_{N_2+1}\right)^T$, $\underline{\pi} \in \mathbb{R}^{N_2+2}$ where each component $\pi_i = Pr(\ count = i)$. We see that the probability of each network state is then:

$$Pr(S_1) = \sum_{i=0}^{N_1} \pi_i \tag{4.6}$$

$$Pr(S_2) = \sum_{i=N_1+1}^{N_2} \pi_i$$

$$Pr(S_3) = \pi_{N_2+1}$$

The Markov chain in Figure 4.1 can be expressed as the following $\mathbb{R}^{N_2+2 \text{ X } N_2+2}$ matrix:

$$\underline{M} = \begin{pmatrix} 1-P_1 & 1-P_1 & \dots & \dots & \dots & 1-P_2 & 1-P_2 & 1-P_3 \\ P_1 & 0 & \dots & \dots & \ddots & 0 & 0 & 0 \\ 0 & P_1 & \ddots & \dots & \ddots & 0 & 0 & 0 \\ \vdots & \vdots & \dots & \ddots & \ddots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & \dots & \ddots & P_2 & 0 & 0 \\ 0 & 0 & \dots & \dots & \dots & 0 & P_2 & P_3 \end{pmatrix} \quad (4.7)$$

With the Markov matrix defined as such, we know this matrix has a 1 eigenvalue and all other eigenvalues < 1. The steady state distribution is the eigenvector corresponding to the 1 eigenvalue, expressed as:

$$\underline{\pi} = \underline{M}\underline{\pi} \quad (4.8a)$$

Subject to the condition:

$$\sum_{i=0}^{N_2+1} \pi_i = 1 \quad (4.8b)$$

Eq. (4.8a) has a closed form solution. Start with the equation in (4.8a) corresponding to the last row of $\underline{\underline{M}}$:

$$\pi_{N_2+1} = P_2\pi_{N_2} + P_3\pi_{N_2+1}$$

$$\pi_{N_2} = \frac{1-P_3}{P_2}\,\pi_{N_2+1}$$

Continuing to solve backwards, we find the following recurrence relationship holds:

$$\pi_i = \frac{\pi_{i+1}}{P_2}\,, \qquad N_1 < i < N_2$$

$$\pi_i = \frac{\pi_{i+1}}{P_1}\,, \qquad 0 \le i \le N_1$$

So that the closed form solution for the probabilities can be found to be:

$$\begin{aligned} \pi_i &= \frac{1-P_3}{P_1^{N_1+1-i}P_2^{N_2-N_1}}\pi_{N_2+1}, \;\; i \le N_1 \\ \pi_i &= \frac{1-P_3}{P_2^{N_2+1-i}}\,\pi_{N_2+1}, \qquad N_1 < i \le N_2 \end{aligned} \tag{4.9}$$

Finally we use the normalization condition of Eq. (4.8b) to determine π_{N_2+1}:

$$\pi_{N_2+1}\left(1 + (1-P_3)\left(\sum_{i=0}^{N_1}\frac{1}{P_1^{N_1+1-i}\,P_2^{N_2-N_1}} + \sum_{i=N_1+1}^{N_2}\frac{1}{P_2^{N_2+1-i}}\right)\right) = 1 \tag{4.10}$$

$$\pi_{N_2+1} = \frac{1}{\prod}$$

Where the normalization factor $\prod$ is:

$$\prod = 1 + (1 - P_3)\left(\sum_{i=0}^{N_1} \frac{1}{P_1^{N_1+1-i} P_2^{N_2-N_1}} + \sum_{i=N_1+1}^{N_2} \frac{1}{P_2^{N_2+1-i}} \right) \tag{4.11}$$

Using the well-known formula for geometric series:

$$\sum_{i=m}^{n} a^i = \frac{a^m - a^{n+1}}{1 - a}$$

We may simplify Eq. (4.11) to the following:

$$\prod = 1 + (1 - P_3)\left(\begin{array}{c} \frac{1}{P_2^{N_2-N_1}} \frac{1}{P_1^{N_1+1}} \left(\frac{1 - P_1^{N_1+1}}{1 - P_1} \right) + \\ \frac{1}{P_2^{N_2-N_1}} \left(\frac{1 - P_2^{N_2-N_1}}{1 - P_2} \right) \end{array} \right) \tag{4.12}$$

With that, we may explicitly evaluate the probabilities given in Eq. (4.6):

$$\pi_{N_2+1}\, Pr(S_1) = \frac{1-P_3}{P_2^{N_2-N_1}\ P_1^{N_1+1}}\left(\frac{1-P_1^{N_1+1}}{1-P_1}\right)\frac{1}{\prod}$$

$$Pr(S_2) = \frac{1-P_3}{P_2^{N_2-N_1}}\left(\frac{1-P_2^{N_2-N_1}}{1-P_2}\right)\frac{1}{\prod}$$

$$Pr(S_3) = \frac{1}{\prod} \tag{4.13}$$

With Eq (4.13) we can find the average duty cycle $E[D]$ in the network, accounting for loss-of-synchronization effects:

$$E[D] = D_1\, Pr(S_1) + D_2\, Pr(S_2) + D_3 Pr(S_3) \tag{4.14}$$

D_i in this case is the duty cycle in the S_i state. D_1 = 1 by the assumptions in our network analysis. The average RF power consumption, $E[P_{RF}]$ is simply:

$$E[P_{RF}] = P_{RF-DC}\ E[D] \tag{4.15}$$

Where P_{RF-DC} is the fully on, DC power consumption of the RF front-end.

We evaluate the equations derived above for a system with the following nominal parameters, unless otherwise stated:

Table 4.1: System Parameters for Plots

Parameter	Value	Description
Nodes	10	Number of nodes in the system
N_1	14	Amount of cycles to synchronize
N_2	114	Amount of cycles before reaching S_3 state
P_{RF-DC}	$7.5mW$	DC Power Consumption
T_0	$6.667\mu s$	Time of each cycle
N_{BINS}	128	Number of bins in the system
T_{RF_S2}	T_0/N_{BINS}	RF window size in S_2 state
T_{RF_S3}	$25ns$	RF window Size in S_3 state
μ_{S2}	$16ns$	μ from Eq. (4.3) in the S_2 state
μ_{S3}	$1ns$	μ from Eq. (4.3) in the S_3 state
σ	$2.1ns$	Oscillator period jitter from Eq. (4.3)
BER	10^{-5}	Bit-Error Rate
D	T_{RF}	D from Eq. (4.3)
D_2	$2\,T_{RF\_S2}/T_0$	Total RF Duty Cycle in S_2 state
D_3	$2\,T_{RF\_S3}/T_0$	Total RF Duty Cycle in S_3 state

We first plot the expected state occupancy percentages and total system duty cycle as a function of T_{RF_S3} for the network described above in Figure 4.2 below. At duty cycles around $T_{RF} = 5\sigma$ we see that the network has a very small probability of remaining in the power saving S_3 state, and hence the overall duty cycle is greater than 10%. Thus we see that very small RF windows are detrimental to overall system power consumption since the network is then spent constantly losing and regaining synchronization. As T_{RF} increases, $P(S_3)$ also increases where at $T_{RF} = 10\sigma$ the network remains in the S_3 state more than 98% of the time.

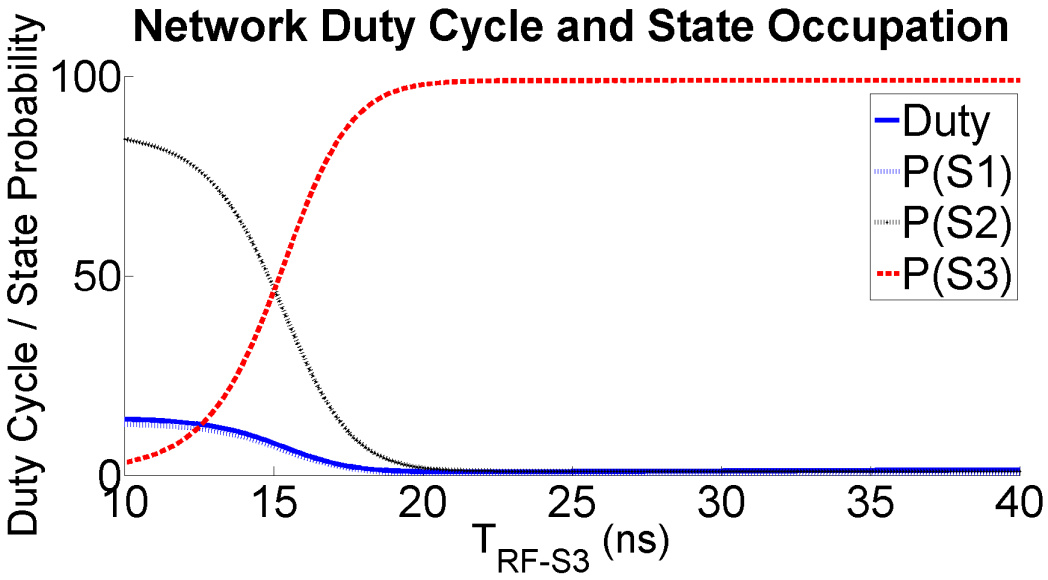


Figure 4.2: network state occupancy and average duty cycle $E[D]$ as a function of the RF window time. $\sigma = 2.1ns$ in this network

Since the system stays in the power saving S_3 state, the average duty cycle $E[D]$ becomes very low, around 1-2% in the range of T_{RF} from 20 to 40ns. We plot how this average duty cycle translates to real work power savings in Figure 4.3 below:

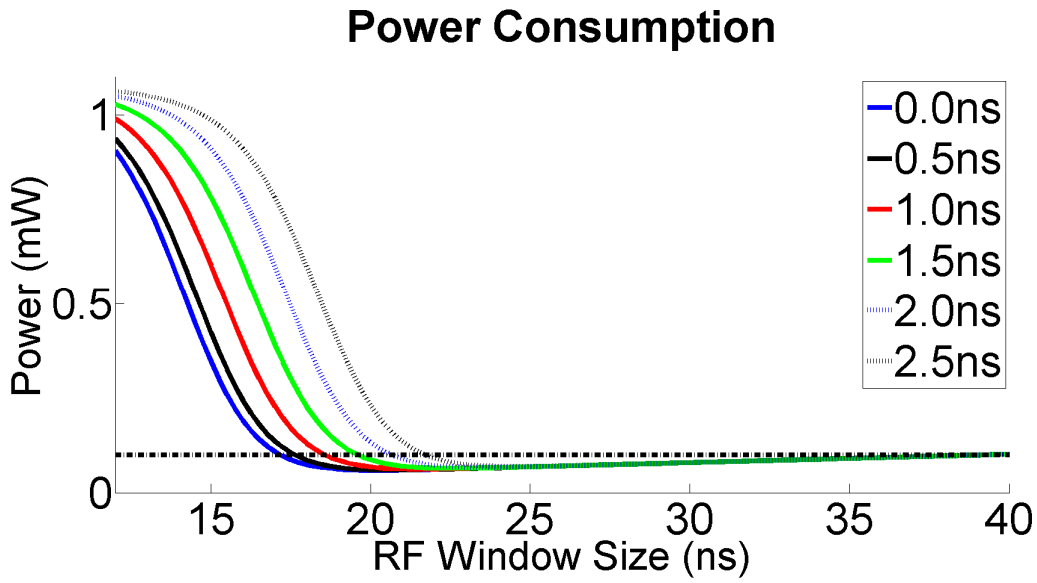


Figure 4.3: Network power consumption vs RF window size. Dotted line is $100\mu W$. Multiple plots are generated with varying μ_0 from 0ns to 2.5ns

We see that average RF power consumption rapidly increases if the system is too aggressively duty cycled, but can be maintained at less than $100uW$ on average for RF windows greater than 25ns. This is true even if the pulse offset position is misestimated by 2.5ns.The average power consumption also grows slowly as a function of the window size. In practical systems we would desire to choose a RF window size far from the steep "waterfall" region to account for any misestimation of offset and jitter we may make in the S_2 state. However, we see that sub-$100\mu W$ power consumptions are still possible even with substantially "safe" choices of T_{RF} in the S_3 state.

We also evaluate the sensitivity of the system to BER. A plot of this is shown in Figure 4.4. T_{RF_S3} is fixed at $25ns$ in this case. We find that the system at $BER = 10^{-5}$ stays in the S_3 state nearly all the time, however as BER degrades, the probability of being in S_2 increases while the probability of being in S_3 degrades. At

roughly $N * BER = N_2, P(S_2) = P(S_3)$. This establishes the rule of thumb limit for the size limit of the network. This also means that BER estimation and management is critically important in practical systems, so that connections between nodes with less than sufficient BER need to be found and dropped. This also implies that a gradual BER versus distance rolloff in these systems are undesirable, contrary to traditional systems. Instead, the ideal BER characteristic should resemble a step response with respect to distance as much as possible

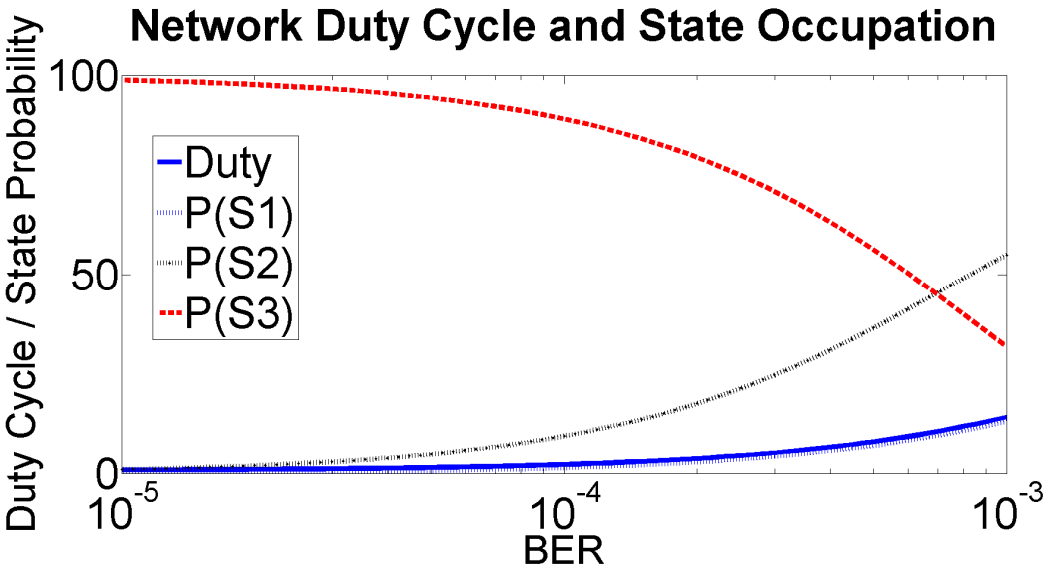


Figure 4.4: Network duty cycle and state occupation probability as a function of BER.

4.3 Network Data Rate

Having calculated the probability of maintaining synchronization in our system, the logical next step is calculating the possible data rates the network can sustain. In this section we will analyze a simplified model of data transmission in the network. We assume the following about the network:

- All nodes in the network try to send out packets of length L continuously.
- The packet transmission request can come at any time in the network and are not synchronous to any state of the network.
- Packet transmission can only occur in the S_2 and S_3 states, since the S_1 state is an unsynchronized state.
- Packet is successfully transmitted if synchronization is maintained for L consecutive cycles in the S_2 and S_3 states.
- If synchronization is lost in the middle of packet transmission, the packet is discarded and retried from the beginning.
- A node will continuously retry a packet if it fails.

With these assumptions we may commence analyzing the theoretical network throughput. The first quantity of interest is the expected packet duration, $E[N_{PACKET}]$ in terms of the number of cycles. The packet duration is simply the packet length plus the sum of the length of all n_R failed transmissions. We model the length of each failed transmission with a random variable $L_{ERR} \in (0, L]$

$$N_{PACKET} = L + \sum_{i=1}^{n_R} L_{ERR} \tag{4.16}$$

Since we have assumed each bit detection is an independent event, it follows that the number of packet transmission failures (packet transmission retries), n_R is independent of the length of each packet that is in error L_{ERR}, and that the length of each L_{ERR} is independent of each other. Thus we can express the expectation as follows:

$$E[N_{PACKET}] = E\left[L + \sum_{i=1}^{n_R} L_{ERR}\right] = L + E[n_R]\,E[L_{ERR}] \qquad (4.17)$$

We first solve for $E[n_R]$. The probability distribution of the number of packet retries is itself conditional on which state the system was in when the packet transmission started. Thus we want to first solve for the conditional probability distribution:

$$Pr(n_R \mid count = i)$$

To find this condition distribution, we observe the following characteristics of the network:

- n=0 if the first packet in the network succeeded without errors.
- The first packet is started with the network in any state.
- For all subsequent retries, we start the transmission in the $count = 0$ state.

We can write the probability the first packet is transmitted successfully, given that the packet transmission request started in the i^{th} state as:

$$Pr(n_R = 0 \mid count = i) = \begin{cases} P_1^{N_1+1-i} P_2^{N_2-N_1} P_3^{L-(N_2-N_1)} & i \le N_1 \\ P_2^{N_2+1-i} P_3^{L-(N_2+1-i)} & N_1 < i \le N_2 \\ P_3^{L} & i = N_2 + 1 \end{cases} \qquad (4.18)$$

For notational convenience, let's define $P_{i|j} = \Pr(n_R = i | \, count = j)$

We can define the probability of an additional packet retry, given that we had n packet retries already as:

$$Pr(n_R = n+1 \,|\, n_R = n) = \begin{cases} 1 - P_{0|i} & n = 0 \\ = 1 - P_{0|0} & \\ = 1 - P_1^{N_1+1} P_2^{N_2-N_1} P_3^{L-(N_2-N_1)} & n \geq 1 \end{cases} \quad (4.19)$$

The probability of packet success given that we have had $n_R = n$ retries is:

$$Pr(Success | \, n_R = n) = \begin{cases} P_{0|i} & n = 0 \\ = P_{0|0} & n \geq 1 \end{cases}$$

$$Pr(Success | \, n_R = n) = P_{0|i} \quad n = 0 \quad (4.20)$$

We may find the conditional probability distribution for the number of retries of a packet transmission by noting that each packet transmission is independent of past packet transmissions and that if the number of packet retries were n, then transmission must have failed n times while succeeding on the $n + 1^{th}$ transmission such that :

$$P_{n|i} = \quad Pr(Success\ |n_R = n) \prod_{i=0}^{n-1} Pr(n_R = i+1 \mid n_R = i)$$

$$= \quad P_{0|i} \qquad n = 0$$

$$= \quad P_{0|0}\left(1 - P_{0|0}\right)^{n-1}(1 - P_{0|i}) \qquad n \geq 1 \qquad (4.21)$$

Hence, the expected number of retries n_R, given that the packet transmission started in state i is:

$$E[n_R \mid count = i] = \quad \sum_{n=0}^{\infty} n\, P_{n|i}$$

$$= \quad P_{0|0}\left(1 - P_{0|i}\right) \sum_{n=1}^{\infty} n \left(1 - P_{0|0}\right)^{n-1}$$

$$= \quad \frac{\left(1 - P_{0|i}\right)}{P_{0|0}} \qquad (4.22)$$

Finally we use conditional expectation to find $E[n_R]$:

$$E[n_R] = E[E[n_R \mid count]]$$

$$= \sum_{i=0}^{N_2+1} E[n_R \mid count = i\,]\,\pi_i$$

$$= \sum_{i=0}^{N_2+1} \frac{(1 - P_{0|i})}{P_{0|0}}\,\pi_i \qquad (4.23)$$

Where π_i are the steady state probability distributions derived in Eq. (4.9). To further simplify the analysis, we may look at the upper-bound on $E[n_R]$, which represents the worst-case number of packet retries. We note that $E[n_R \mid count = i]$ is maximized over i by minimizing $P_{0|i}$. Due to our requirement that $1 > P_1 > P_2 > P_3$, $P_{0|i}$ monotonically increases on $i \in [0, N_1]$ and decreases on $i \in [N_1, N_2 + 1]$. This means $P_{0|i}$ takes its minimum at $i = 0$ or $i = N_2 + 1$. We may relate these two quantities by noting:

$$P_1^{N_1+1}\left(\frac{P_2}{P_3}\right)^{N_2-N_1} P_{0|N_2+1} = P_{0|0} \qquad (4.24)$$

And hence $P_{0|N_2+1} < P_{0|0}$ if

$$P_1^{N_1+1} > \left(\frac{P_3}{P_2}\right)^{N_2-N_1} \qquad (4.25)$$

Thus we may bound $E[n_R]$ by:

$$E[n_R] \leq \frac{(1 - P_{0|NMAX})}{P_{0|0}} \sum_{i=0}^{N_2+1} \pi_i$$

$$\leq \frac{(1 - P_{0|NMAX})}{P_{0|0}}$$

$$E[n_R] \leq \frac{(1 - P_{0|NMAX})}{P_{0|0}} \sum_{i=0}^{N_2+1} \pi_i \qquad (4.26)$$

Where

$$NMAX = \begin{cases} 0, & P_1^{N_1+1} < \left(\frac{P_3}{P_2}\right)^{N_2-N_1} \\ N_2 + 1, & P_1^{N_1+1} > \left(\frac{P_3}{P_2}\right)^{N_2-N_1} \end{cases} \qquad (4.27)$$

Under normal operating conditions, $NMAX = N_2 + 1$ since we desire N_1 to be small (short synchronization times) and $P_1 \approx 1$, thus $P_1^{N_1+1} \approx 1$, and P_3 is substantially smaller than P_2 (aggressive duty cycling).

We next solve for $E[L_{ERR}]$, which represents the average length of those packets which are in error. We first note that:

$$E[L_{ERR}] = E[L_T \mid Error]$$

$$= \quad \mathrm{E}[E[L_T \mid count \mid Error]$$

$$= \quad \sum_{i=0}^{N_2+1} \pi_i \, E[(L_T \mid count = i) \mid Error] \qquad (4.28)$$

L_T is a random variable representing the transmission length of the packet.

We see that once again, L_{ERR} is found using conditional expectation on the $count$ state i in which the packet transmission was started. The quantity $E[L_T \mid count = i \mid Error]$ represents the average length of error, given that the packet transmission was started with $count = i$. This quantity is:

$$E[L_T \mid count\ i \mid Error] = \quad \sum_{j=1}^{L+N_1+1} j \Pr(\ (L_T = j \mid count = i) \mid Error)$$

$$= \quad \sum_{j=1}^{L+N_1+1} j \, \frac{\Pr(\ (L_T = j \mid count = i) \cap Error)}{\Pr(Error)}$$

$$= \quad \sum_{j=1}^{L+N_1+1} j \, \frac{\Pr({L_T}' = j \mid count = i\ )}{1 - P_{0|i}} \qquad (4.29)$$

Where $\Pr(L_T{}' = j \mid count = i)$ is the probability that the transmission failed on the j^{th} transmission. L_T' is a random variable on the set of $L_T \cap Error$. The complete expression for $\Pr(L_T{}' = j \mid count = i)$ is given in Appendix I

In Eq. (4.29) above, the index *j* represents the cycle within the packet in which the synchronization error event occurred. Since the network cannot successfully transmit data while unsynchronized, *j* subsequently ranges from 1 to $L + N_1 + 1$. Once again we are interested in the upper bound on the expected error length over the count variable i. From Eq. (4.29), this is found by maximizing $P_{0|i}$ and $Pr(L_T{}' = j \mid count = i)$ for any given j. $\Pr(L_T{}' = j \mid count = i)$ is maximized for $i = 0$ (Appendix I), while from (4.18) we know that $P_{0|i}$ takes its maximum at $i = N_1$. If we assume that $P_1^{N_1} \approx 1$, a reasonable approximation for normal operation of our network then $P_{0|0} \approx P_{0|N_1}$. Hence the worst case bound for the network data rate is approximately:

$$E[L_T \mid count = i \mid Error] \lesssim \sum_{j=1}^{L+N_1+1} j \, \frac{\Pr(L_T{}' = j \mid count = 0\,)}{1 - P_{0|0}} \qquad (4.30)$$

With $\Pr(L_T{}' = j \mid count = 0)$ given by (Appendix I):

$$\Pr(L_T{}' = j \mid count = 0) = \begin{cases} (1 - P_1)\, P_1^{j-1} & j \le N_1 + 1 \\ (1 - P_2) P_2^{j-1-(N_1+1)}\, P_1^{N_1+1} & N_1 + 1 < j \le N_2 + 1 \end{cases}$$

$$= \quad (1 - P_3) \times \quad j > N_2 + 1 \quad (4.31)$$
$$\left(P_3^{j-1-(N_2+1)} P_2^{N_2-N_1} P_1^{N_1+1}\right)$$

Hence, we can lower bound the transmission time in (4.29) by:

$$E[L_{ERR}] \lesssim \quad E[L_T \mid count = 0 \mid Error] \quad (4.32)$$

With the derivation above, we can then lower bound the data rate for the entire network by:

$$R \gtrsim \frac{L}{T_0 \left(L + \frac{\left(1 - P_{0|NMAX}\right)}{P_{0|0}} E[L_T \mid count = 0 \mid Error]\right)} \quad (4.33)$$

In Figure 4.5, we plot (4.33) for the system described in Table 4.1 as a function of T_{RF_S3} . We find that the data transmission results mirror that of the power consumption. We see that in the regime from 15-25ns T_{RF_S3}, the number of retries for a packet rises rapidly. This is because we are unlikely to remain in a synchronized state throughout the duration of the packet transmission. As a result data rate and power consumption both suffer. In Figure 4.6 and Figure 4.7, we perform the same plot for the family of $BER's: BER = 10^{-3}, 10^{-4}$ and 10^{-5} for $L = 1000$ and $L = 200$ respectively. We find that at higher bit error rates, longer packets are detrimental to the overall system performance and short packets are more likely to get successfully transmitted. However, shorter packets imply more packet overhead and less effective payload bits transferred. Thus a radio network based on this

synchronization system should ideally adjust its data payload lengths as the link status changes.

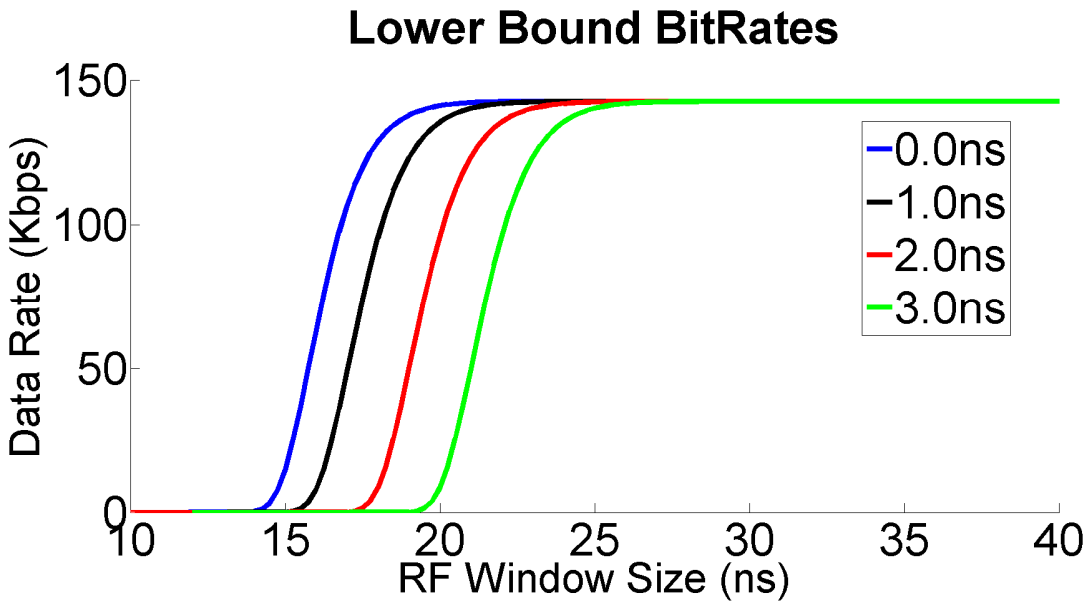


Figure 4.5: Lower bound on bitrates as a function of the RF Window size for varying estimation offsets. 10 node network. $L = 1000$, $BER = 10^{-5}$

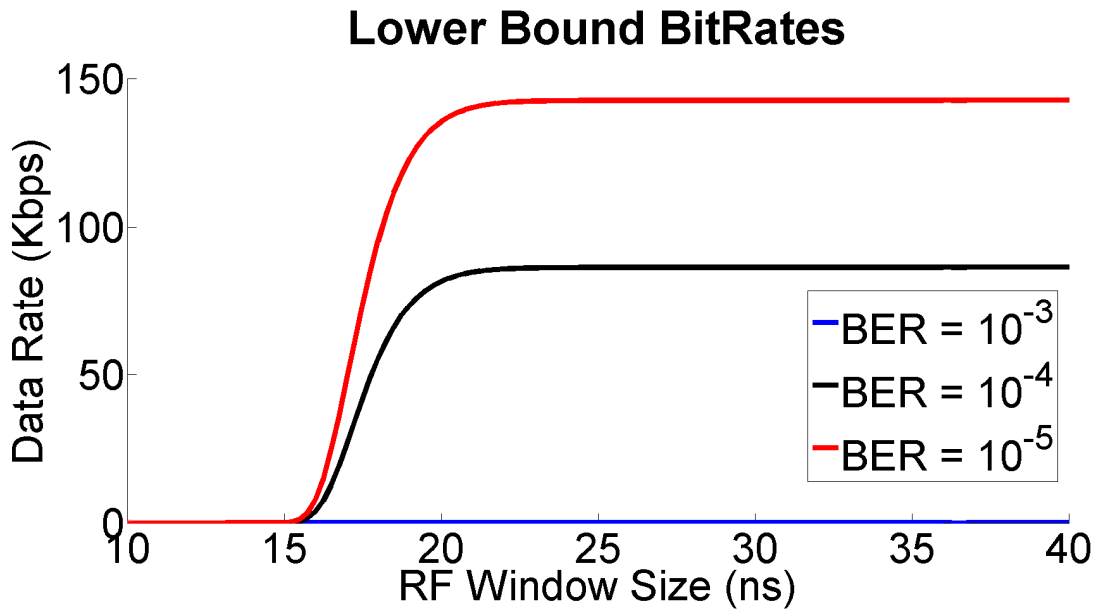


Figure 4.6: Lower Bound on Bitrates as a function of the RF Window size for varying BER. 10 Node network, L= 1000. $\mu = 1ns$

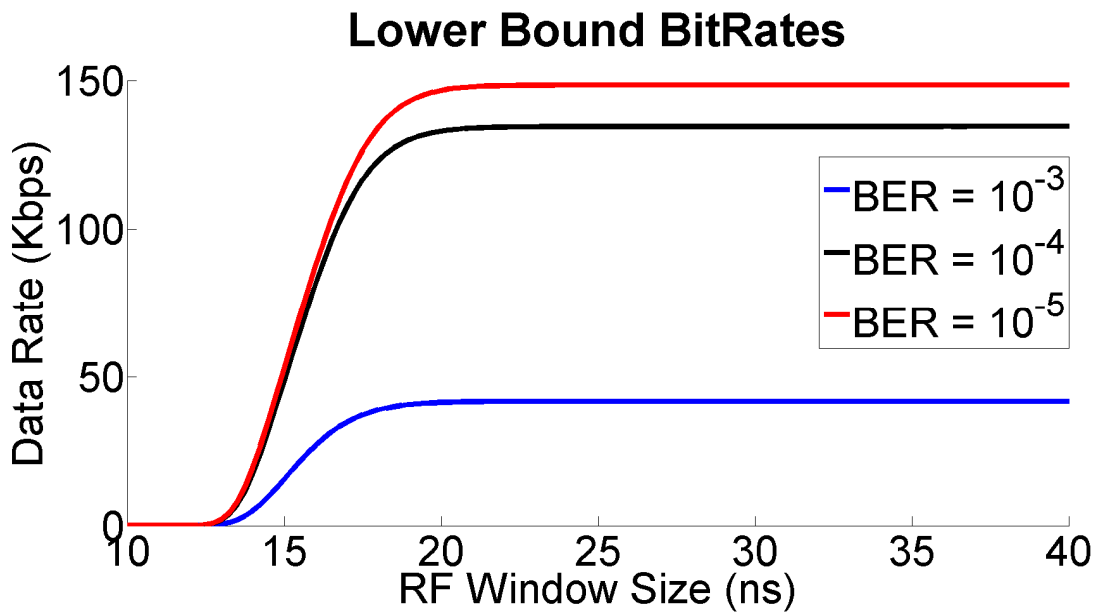


Figure 4.7: Lower Bound on Bitrates as a function of the RF Window size for varying BER. 10 Node network, L= 200. $\mu = 1ns$

Chapter 5 APPENDIX

I. Derivation of $Pr(L_{T'} = j \mid count = i)$

In this section, we derive the conditional probability distribution $\Pr(L_{T'} = j \mid count = i)$, which is the distribution that a packet transmission failure occurred on the j^{th} bit transmission within a data packet. $L_{T'}$ is a random variable of the length of the transmission errors. The key observation is that for $L_{T'} = j$, the bit error occurred on the j^{th} transmission while each of the $j - 1$ prior transmissions were not in error. The $j - 1$ successful transmissions will be composed of a combination of P_1, P_2 and P_3 depending on the initial state i. The full expression for $\Pr(L_{T'} = j \mid count = i)$ is:

For $i \in [0, N_1]$:

$$\Pr(L = j \mid count = i) = \begin{cases} (1 - P_1)\, P_1^{j-1} & i + j \leq N_1 + 1 \\ (1 - P_2) P_2^{j-1-(N_1+1-i)} P_1^{N_1+1-i} & N_1 + 1 < i + j \leq N_2 + 1 \\ = \end{cases}$$

$$= \begin{cases} (1-P_3)\times & i+j > N_2+1 \\ P_3^{j-1-(N_2+1-i)} P_2^{N_2-N_1} P_1^{N_1+1-i} & \end{cases} \quad (5.1)$$

$$\Pr(L=j \mid count=i) = \begin{cases} (1-P_2)P_2^{j-1} & i+j \leq N_2+1 \end{cases}$$

$$= \begin{cases} (1-P_3)P_3^{j-1-(N_2+1-i)}\, P_2^{N_2+1-i} & i+j > N_2+1 \end{cases} \quad (5.2)$$

For $i = N_2 + 1$:

$$\Pr(L=j \mid count=i) = (1-P_3)P_3^{j-1} \quad (5.3)$$

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