MONOLITHIC INTEGRATION OF JUNCTION FIELD EFFECT TRANSISTOR AND NANOELECTROMECHANICAL SYSTEMS

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The mechanical motion of most NEMS/MEMS devices has to be transduced to electrical domain by using active or passive components. In passive transduction, resistors, capacitors and inductors are used to sense the motional current which is then converted to voltage. In active sensing, transistors are also used for the conversion process. Since transistors can offer enhanced gain through transconductance, they can increase small signals into larger signals that can be less susceptible to systematic and innate noise sources.

The active components can be integrated into the NEMS device either by monolithic integration or through a two chip solution. In monolithic integration, both the active device and the NEMS devices are fabricated on the same substrate, using short thin film interconnects, minimizing parasitics. In the two-chip solution, the active and NEMS components are fabricated on separate wafers and the individual dices are wire-bonded, or flip chip bonded which can have higher parasitics and generate mismatches in the system. One of the goals of this thesis is to monolithically integrate JFETs into N/MEMS components to enhance signal transduction.

The dissertation begins with the characterization of an SOI pre-biased NEMS electrostatic switch with a pre-biased voltage of 54.8 V and a switching voltage as low as 300 μV. The contact resistance of the switch was 4.3 MΩ due to the Si-to-Si contact used in the switch. Later, to reduce the contact resistance, $MoSi_2$ was used as a

structural layer and Cr and Pt were sputtered on the switch to produce Pt-to-Pt contact. The measured contact resistance was reduced to 1 KΩ.

A Junction Field Effect Transistor (JFET) was integrated into the switches to enable the sensing of the displacement of the moving structure. The JFETs had a pinch-off voltage of -19 V (at V_{DS}=10 V) and a transconductance parameter of 1.9 mA/V^2 (at V_{DS}=10 V). These JFETs were monolithically integrated into the switch to minimize parasitics. The JFET was then incorporated into a nanoscale multiple-tip prober which was used for atomic imaging of Highly Ordered Pyrolytic Graphite (HOPG) as well as performing conductance measurements of HOPG. The JFET along with capacitive sensing was used to sense the motion of the movable tip. The resonating tip had a resonance frequency of 293 kHz and the tip radius of <50 nm. Currently, commercial Scanning Probe Microscopes (SPM) such as STM and AFM use a single tip for scanning which limits its use to static electrical measurements. This dissertation presents the development of a novel SPM that uses the multiple tips for scanning and performing dynamic transport measurements.

BIOGRAPHICAL SKETCH

Kwame Amponsah was born on April 18th 1981 in Sekondi, a small city located in the Western Region of Ghana. However, he grew up in Takoradi, a few minutes' drive from Sekondi, with his seven siblings. Kwame did high school at Mfantsipim School which is an all-boy boarding school located in Cape Coast in the central region of Ghana. After graduating from high school, he worked with his dad, who was then involved in the export industry, and subsequently decided to pursue an undergraduate education in the United States of America. He started his undergraduate education at Cornell University in 2003 and quickly fell in love with Ithaca. Ithaca has since been his home away from home where he has enjoyed the eateries, the beautiful sceneries, the locals and frequenting the Commons. At Cornell, he worked as a research assistant at the Cornell Nanoscale Facility and it was this exposure to undergraduate research that motivated him to pursue graduate school. He joined Prof. Edwin Kan's group for his Masters of Engineering degree in 2007 for which he investigated the use of flash memory technology for biological sensing. In 2008, he began his doctoral education under the supervision of Prof. Amit Lal. He has since been researching the monolithic integration of Junction Field Effect Transistors into MEMS/NEMS platforms.

To My Dada and Mama

ACKNOWLEDGMENTS

Ithaca…my home away from home. I have benefited vastly from the people I have met and the generosity of various funding institutions and agencies. I remember back home in Ghana, I could only dream of travelling to the land of opportunity to pursue a college degree and let alone an advanced degree. Yet, the dream became reality the moment I received my offer from Cornell University to pursue my undergraduate degree. In that regards, the International Students Office was very generous in offering me a full tuition scholarship for which I am very grateful. I quickly assimilated to the American culture thanks to my undergraduate friends (Shawn Darrah, Alex O'Day, my roommate Soutrik Pramanik and many more).

My real interest in research started in the summer of 2004 when I wandered around the offices of the Cornell Nanoscale Facility looking for a summer job. I was hired by Dr. Mandy Esch to assist her in microfluidic research. Little did I know that my path forward would be engulfed with countless hours in the cleanroom, having midnight conversations with frustrated doctoral students who were waiting eagerly to jump on the equipment of individuals who had reserved spots, but had failed to show up. At that point, I realized I enjoyed research very much and decided to continue on that path. I am very grateful to Dr. Esch for offering me that opportunity which became a life changing event for me.

Being home away from home could sometimes be very lonely and that is when the Ghanaian community at Cornell was there to support me. Thank you Betsy Ampofo, Robert Mereku, David Agyeman-Budu, Obafemi Otelaja, Dela Kusi-Appouh, Nii Lante Amissah, Naa Lante Amissah, Oluranti Campbell, and David Korda for all the cooking and the good times we shared. I also enjoyed the pleasant company of Chimaobi Onuchekwuah, Majed Al-Mashad and Xiao Wang. We had fond memories and hopefully we will meet again on the Hill at subsequent reunion events. Special

thanks to Yamilet Echeverria for being there for me during the good and bad times. I enjoyed your delicious cooking, travelling together to conferences and spending quality time together. I appreciate all the love and support which made my graduate school experience less stressful and amazing one!

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Throughout my time here, I have grown personally and professionally and the most important person attributable to this growth process was my academic advisor Prof. Amit Lal. I am forever grateful to you for serving as an amazing advisor and a great mentor, especially for exercising extreme patience in reviewing my publications and providing feedback. I would additionally like to thank you for all the personal advice and coaching you offered me which at times proved to be life changing. Your intelligence is unmatched and I am happy to have worked under your leadership. I would also like to thank my committee members, Prof. Sandip Tiwari, Prof. Clifford Pollock and Prof. Alyosha Molnar for their support and advice.

Furthermore, I would like to thank my funding agencies since without their support it would have been nearly impossible to pursue this advanced degree. Thanks to the Institute for African Development (IAD), Cornell Center for Materials Research (CCMR) and United States Army Research Laboratory (ARL).

Finally, I would like to thank my dad, mom and siblings for their unwavering love and support throughout the years. Irene and Eric, I am eternally grateful for all the Ghanaian food that you provided when I got home-sick. Mama, thank you for the spiritual support and I would like you to know that I am still holding on to the Biblical verse:

"Finally, brothers and sisters, whatever is true, whatever is noble, whatever is right, whatever is pure, whatever is lovely, whatever is admirable—if anything is excellent or praiseworthy—think about such things."

Philippians 4:8

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INTRODUCTION

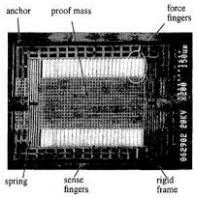
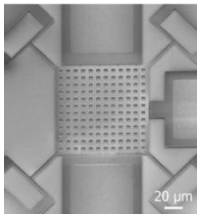
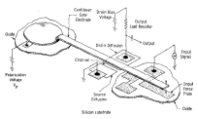
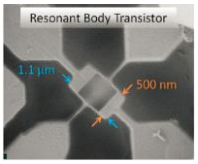
1.1 *Integration of Transistors into Nano-Electro-Mechanical-Systems*

Most commercial MEMS sensor solutions use the two-chip solution for electrical interface and signal conditioning. The two-chip solution is often justified as a way to reduce complexity of CMOS integration with SOI-NEMS. Although the hybrid technique offers the advantage of independent optimization of the integrated circuit and NEMS fabrication process flows, the cost for assembly and packaging can be higher than the monolithic integration [1]. Especially as the critical gate length of CMOS gets smaller and CMOS only gets less expensive, the two chip solution is more commercially viable. However, for higher performance, monolithic approaches may prove to be better than the two chip solution. The two-chip solution introduces parasitics and mismatches during the assembly and packaging of the ASIC and NEMS components due to the wire bonds that connects the two dies and prevents the SOI-NEMS/MEMS from fully realizing its highest performance.

To sense small signals such as the motion of a NEMS/MEMS device, JFETs are preferred over other transistors such as MOSFETs and BJTs because of their low 1/f noise, low-mask count, no parasitic diodes in isolation junctions, and insensitivity to electrostatic discharge [2], [3]. Furthermore, the yield issues with CMOS-oxide-silicon interfaces are eliminated in JEFTs. However, JFETs have the disadvantage of lower transconductance, higher process variations and higher gate leakage current.

Previously, various research groups have monolithically integrated MOSFETs into NEMS/MEMS devices for signal transduction [4]-[7] but this dissertation is focused on monolithic integration of JFETS and NEMS for motion sensing.

Table 1.1. Previous transistor integration efforts

	Device	Resonant Frequency	Quality Factor	MEMS Material
H. Luo et.al [4]		6.1 KHz		Composite of metal and dielectric layers
D. Grogg et al. [5]		32 MHz	4000	Silicon
H. C. Nathanson et al. [6]		1KHz to 100 KHz	500	Gold
D. Weinstein et al. [7]		11.72 GHz	1830	Silicon

1.2 *Passive Sensing (two-chip Solution: Sensing of micro transducers)*

Passive sensing, also known as the two-chip solution is when the NEMS and front end electronics are not fabricated on the same wafer die. Wire-bonds are used to connect the two dice as shown in Figure 1.1. Some of the advantages of this form of integration are the independent scaling of the NEMS and CMOS electronics with lithography scaling, its potentially lower cost, and its design simplicity. However, the wire-bonds that are introduced during packaging cause parasitic feedthrough, lower signal-to-noise ratio and higher packaging cost.

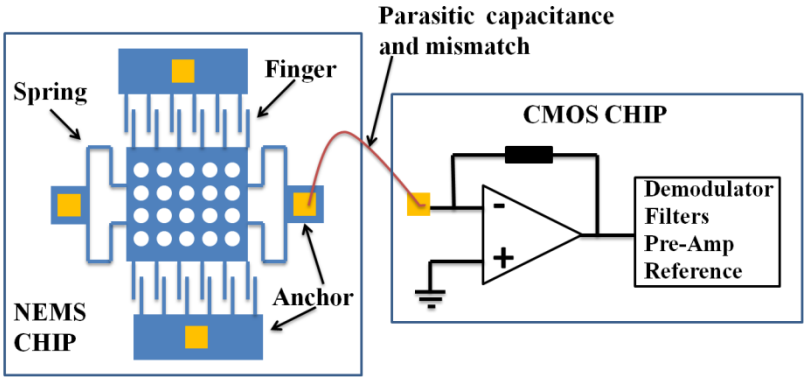


Figure 1.1. Two-chip solution resulting in the integration of NEMS and ASIC. The wire bond introduces capacitive parasitic as well as mismatch at the input port of the amplifier.

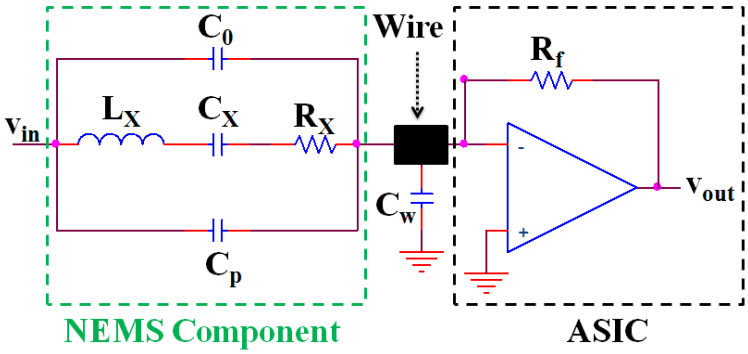


Figure 1.2. Schematic of the two-chip solution where the NEMS component is wire-bonded to an off-chip transimpedance amplifier.

Capacitive coupling and low signal-to-noise ratio leads to passive NEMS devices generally having lower performance. Figure 1.2 shows the small signal electrical equivalent circuit of the NEMS structure that is wire-bonded to an off-chip transimpedance amplifier. The resonator can be modeled as a typical Butterworth–Van Dyke equivalent circuit as shown in Figure 1.2 where L_x, C_x, and R_x represent the

motional inductance, capacitance and resistance respectively. C_0 is the parasitic DC capacitance of the resonator and C_p represents the total parasitic capacitance introduced from the wirebonds, circuit board and packaging. If C_p is large, it will generate large amounts of current that will obscure the motional current from the NEMS component [8]. There is also a parasitic capacitor (C_w) from the bonding wire (at the negative input of the operational amplifier) to ground. This capacitor in most cases is assumed to have negligible effect on the transduction process because it is connected from a virtual ground to the earth ground. In reality, the operational amplifier is non-ideal and there is a Common Mode Rejection Ratio (CMRR). Small voltages differences between the (+) and (-) terminals is amplified. Hence and noise coming through the wirebond (i.e., 60 Hz noise) will leak into the signal chain.

Since the gate of the TIA is held at a virtual ground, the effect of the gate capacitance is ideally nullified. The admittance of the NEMS component with the parasitic capacitance (C_p) is given by:

$$Y = SC_p + SC_0 + \frac{SC_X}{S^2 L_X C_X + SR_X C_X + 1} \tag{1.1}$$

The impedance including the effect of C_w is:

$$Z = \frac{1}{SC_w} + \frac{1}{S(C_P + C_0 + C_X)}\left[\frac{S^2 L_X C_X + SR_X C_X + 1}{S^2 L_X C_Z + SR_X C_Z + 1}\right] \tag{1.2}$$

$$C_Z = \frac{C_X(C_P + C_0)}{C_P + C_0 + C_X} \tag{1.3}$$

As C_w becomes large, it will change the phase of the impedance and resonance frequency detection becomes difficult. Using typical resonator parameters [9], C_x= 1.9 aF, L_x= 1.3 H, R_x= 82 KΩ, and C_0= 1.2 fF, C_w was swept to investigate its effect on the phase angle of the resonator. From Figure 1.3, the phase of the impedance changes from -88 degrees to +63 degrees at which point the resonance is non-detectable [10].

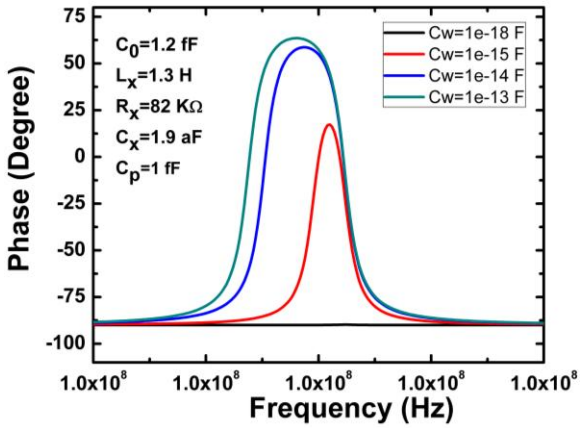


Figure 1.3. Plot of phase vs. frequency illustrating the effect of the parasitic capacitance on the resonance frequency of the NEMS resonator. The parasitic capacitance tends to shift the resonance frequency as well as decreases the phase shift at resonance of the resonator.

The output current which is a combination of the motional current and the parasitic current through C_p, is given by Equation (1.4) while the transfer function is given by Equation (1.5):

$$i_d = \frac{v_{in}}{Z} = -\frac{v_{out}}{R_f} \tag{1.4}$$

$$\frac{v_{out}}{v_{in}} = -R_f[S(C_P + C_0 + C_X)]\frac{S^2L_XC_Z + SR_XC_Z + 1}{S^2L_XC_X + SR_XC_X + 1} \quad (1.5)$$

1.3 *Active Sensing: Transistor Level Motion Transduction*

To improve the signal integrity during the transduction process, it is recommended that the front-end transistor or electronics be monolithically integrated with the NEMS component as shown in Figure 1.4 . In this way, the front-end transistor will serve as a current buffer offering current amplification as well as improving noise immunity at the output node. Capacitive transduction is mostly favored due to its temperature stability, lack of 1/f noise, and ease in fabrication and its repeatability as compared to resistive transduction [9]. Piezoelectric, piezoresistive, thermal and magnetostrictive are other modes of transduction that are less commonly used.

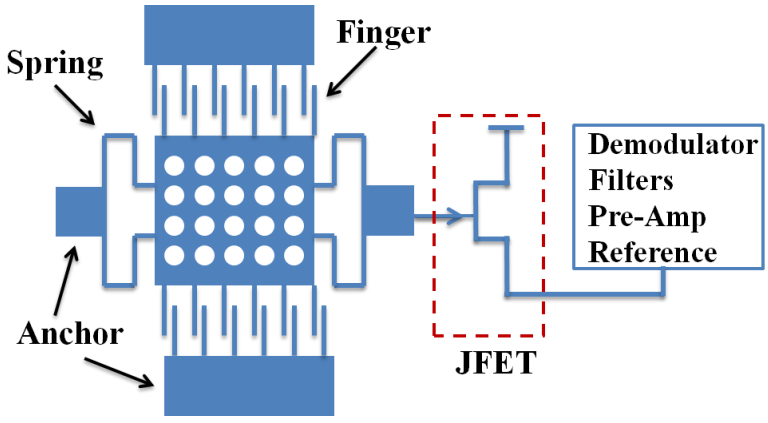


Figure 1.4. Monolithic integration of MEMS accelerometer structure with FETs results in the elimination of the wire-bond parasitic, replaced by the much smaller interconnect parasitic capacitance.

There are many advantages to using a single front-end transistor to transduce the motional current of the M/NEMS component as compared to using an operational amplifier [8]. It is not only lithographically simple to do this form of integration, but it is also less insensitive to process variation. C_t represents all the capacitances connecting the resonator to the gate of the JFET and it includes the gate-to-source capacitance, gate-to-drain capacitance and any substrate capacitances [8]. g_m is the transconductance of the JFET.

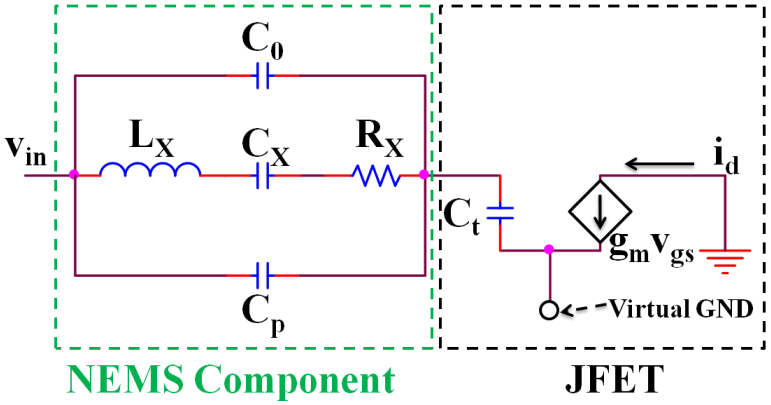


Figure 1.5. Small signal electrical equivalent of the JFET integrated with the NEMS resonator.

The movement of the NEMS component produces a motional current that is converted into gate voltage (V_{gs}) by the capacitor C_t. The JFET then converts this gate voltage into output current (i_d) and in the process provides current amplification. Figure 1.5 can be simplified into a voltage divider circuit as shown in Figure 1.6. Z_1 and Z_2 represent the total NEMS impedance and input impedance at the gate of the JFET respectively.

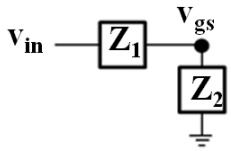


Figure 1.6. The JFET gate voltage results from the voltage divider between the JFET and NEMS impedances.

The impedance of the NEMS component is given by:

$$Z_1 = \frac{1}{S(C_0 + C_X)}\left[\frac{S^2 L_X C_X + S R_X C_X + 1}{S^2 L_X C_{P1} + S R_X C_{P1} + 1}\right] \tag{1.6}$$

$$C_{P1} = \frac{C_0 C_X}{C_0 + C_X} \tag{1.7}$$

The impedance at the gate of the JFET is given by:

$$Z_2 = \frac{1}{S C_T} \tag{1.8}$$

Using a voltage divider at the gate:

$$Z_T = \frac{Z_2}{Z_1 + Z_2} \tag{1.9}$$

$$Z_T = \frac{S^2 L_X C_{P1} + S R_X C_{P1} + 1}{\frac{C_0 + C_X + C_T}{C_0 + C_X}\left(S^2 L_X C_{p2} + S R_X C_{p2} + 1\right)} \tag{1.10}$$

$$C_{P2} = \frac{C_X(C_0 + C_T)}{C_0 + C_X + C_T} \tag{1.11}$$

$$I_d = g_m \left(\frac{(C_0 + C_X)(S^2 L_X C_{P1} + S R_X C_{P1} + 1)}{(C_0 + C_X + C_T)\left(S^2 L_X C_{p2} + S R_X C_{p2} + 1\right)} \right) V_{in} \tag{1.12}$$

The amplified current (I_d) could then be put into a transimpedance amplifier that converts the motional current into appreciable voltage.

1.4 ***Scope of Dissertation***

This dissertation presents a novel monolithic integration of JFET into MEMS and NEMS based systems. The JFET is used to sense the motion of the NEMS component. The simulation, fabrication and electrical characterization of both the JFET and the NEMS structures will be explored. Details will also be given on a new multiple-tip Scanning Probe Microscope that was developed to use the JFET-NEMS devices for atomic imaging and charge transport measurement experiments. The dissertation is organized as follows:

Chapter 2 will provide research effort into the design and characterization of NEMS switches for digital computation using SOI structures. The two main types of NEMS switches are the series and shunt capacitive switches [11]. This dissertation will focus on DC ohmic switches for ultra-low switching voltage applications. For ohmic switches, a figure of merit (FOM) is the contact resistance and lifetime. To improve the FOM, a new generation of all-metal switches were developed using Molybdenum Disilicide ($MoSi_2$) as the structural material and coating the switches with a layer of Cr and Pt.

Chapter 3 will delve into the monolithic integration of JFET into the SOI NEMS switches. As voltage ramps were applied to close the switch, the JFET was used to sense the motion of the cantilever. The device was fabricated onto an SOI platform and to reduce the JFET source and drain resistances, $MoSi_2$ was used as the contact metal and Rapid Thermal Annealed (RTA) to enhance good ohmic contact.

Chapter 4 will demonstrate an application of the JFET-NEMS integration technology where the JFET was further integrated into a multiple-tip NEMS device for scanning probing measurements. The nanoprober has two fixed side tips and the middle tip is capable of being displaced in both the x and y directions using electrostatic comb actuators. The JFET was used to sense the motion of the movable tip. The nanoprober was used to image atomic arrangement of carbon atomic lattices in Highly Ordered Pyrolytic Graphite (HOPG) as well as perform in-situ SEM conductance measurement of the HOPG film. For applications where the JFET was not required, $MoSi_2$ tips were fabricated and used for mapping the conductance of the surfaces at nanoscale.

Chapter 5 will detail the development and assembly of a *Sonic*MEMS Scanning Probe Microscope. This instrument accepts the multiple tips and was used to perform resistance map measurements of HOPG film.

Chapter 2

NON-PULL-IN PRE-BIASED NANO-ELECTRO-MECHANICAL SWITCH WITH PRE-BIASING

2.1 *Introduction*

Nanomechanical switches in series with transistor technologies (BJTs, CMOS, or MESFETs) can facilitate ultra-low-power circuits by eliminating leakage current in transistor circuits [12]. Furthermore, NEMS switches could facilitate all-mechanical digital logic that might consume even less power than hybrid solutions, and the switches are naturally radiation hard.

Nano and micro electromechanical switches are making entry into areas such as mechanical computation, telecommunication, automotive and biomedical fields [13], [14]. NEMS switches, with gas or vacuum in the gaps between the source and drain offer the ideal zero standby leakage power, important for ultra-low power circuits [15], [16]. This is particularly important as deeply scaled transistors have high leakage currents. However, NEMS switches suffer from stiction, arcing, and high switching and pull-in voltages [17].

Generally, MEMS switches have a finite lifetime not capable of trillions of cycles needed for computation. For example, a CMOS switch operating at 1 GHz for 1 year should go through a total number of ~$3x10^{16}$ cycles. The best switching cycle lifetime for MEMS switches is around 10^{10} cycles. One exception is the mirrors in Digital Light Processing (DLP) displays by Texas Instruments that can operate for tens of years at kHz switching rates.

It is important to design NEMS switches to increase contact lifetime. Previous work by Yang et al., demonstrated the maneuvering of pull-in voltage in a

microswitch by pre-charging the gate electrode and modulating the pull-in voltage by charging a floating gate potential through the body bias. With their technique, they were able to greatly reduce the pull in voltage from 48 V to 3 V [18].

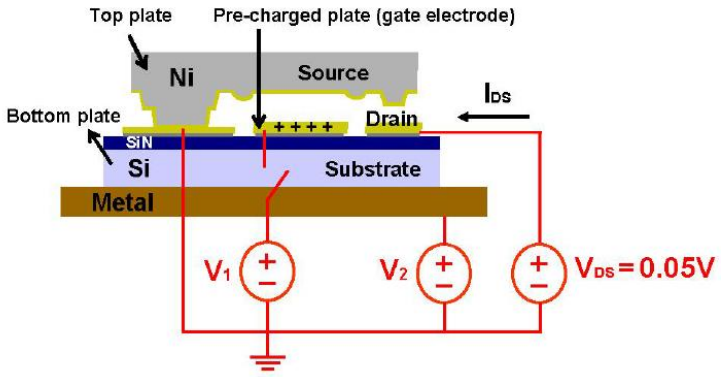


Figure 2.1. Schematic of the switch architecture demonstrated by Yang et al. The gate electrode was pre-charged and the voltage that is applied to the substrate increases the charge on the pre-charge electrode [18].

In a paper reported by Mercado et al., the authors overcame the stiction problem by parametrically varying switch design parameters such as length, width, actuation gap and actuation voltage. To alleviate stiction, they suggested that the restoring force should be greater than the stiction force by applying actuation voltages higher than the pull-in voltage so that in the case there is stiction, there will be enough restoring force to break the welded contact [19].

2.2 *Non-Pull-In Nano-Electro-Mechanical Switch*

We demonstrate an SOI multi-gate NEMS switch as shown in Figure 2.2, which has a switching voltage of 300 μV and greatly reduces the stiction problem. The gaps in the switch were designed in such a way that there was no pull-in in its mode of

operation, eliminating contact degradation due to high velocity impact during contact. Furthermore, a counter-force generating electrode was used to pull-back the cantilever once the bias provided by the actuating gate was removed, to facilitate higher reliability switch operation mitigating stiction.

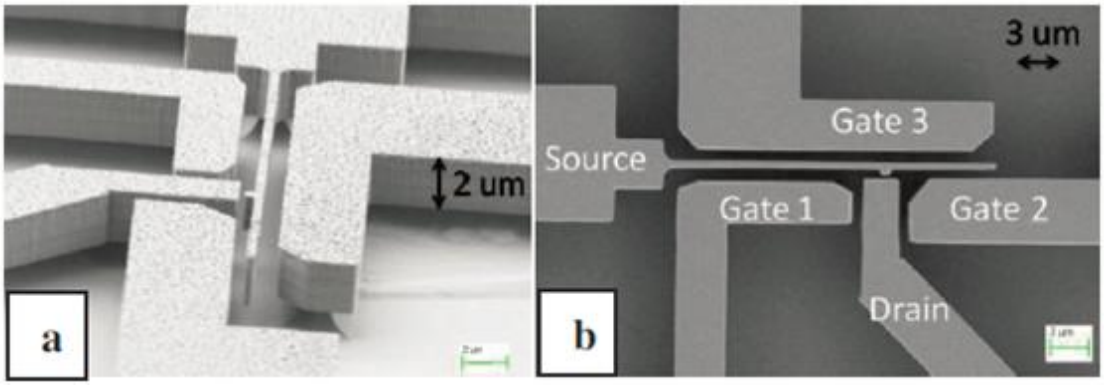


Figure 2.2. (a) and (b) show the side and top views of the nanoswitch with a contact gap of about 300 nm.

Pull-in is an instability where in a parallel plate capacitor with the bottom plate fixed and the top moves under electrostatic spring force displaces one-third of the actuation gap, the electrical force becomes larger than the mechanical restoring force. At that point, the top plate is pulled-in under the higher electrostatic force till it impacts the bottom plate [20].

The pull-in voltage is given by

$$V_p = \sqrt{\frac{8}{27}\frac{Kd_0}{\varepsilon A}} \tag{2.1}$$

where V_p represents the pull-in voltage, K is the spring constant of the cantilever, d_0 is the initial actuation gap, ε is the permittivity of the dielectric in the actuation gap, and

A is the actuation area. Equation (2.1) stipulates that to increase the V_p greater than a set value, the gap d_0 can be increased.

Figure 2.3 is a schematic of the device which shows multiple electrodes and air gaps. The contact gap (g_{sd}) was designed to be (300 nm) such that the source is fully in contact with the drain before pull-in at either g_{01} (900 nm) or g_{02} (700 nm). The source cantilever is 25 µm long, 300 nm wide and has a thickness of 2 µm.

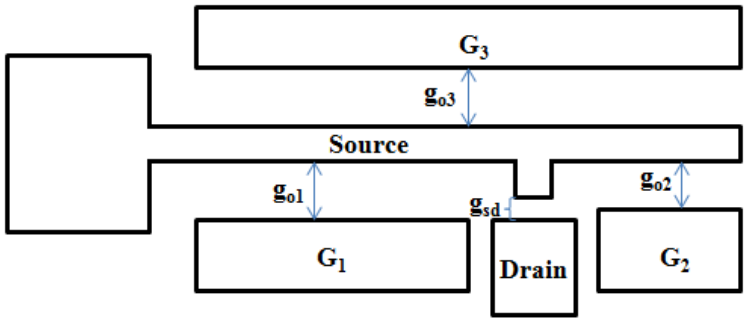


Figure 2.3. The schematic of the NEMS switch which shows the source, drain and gate terminals as well as the air gaps.

The device operation is as follows:

1. The source and G_2 are grounded and G_3 is floating. The drain is set at a potential.
2. Sweep G_1 until the device switches. This is the gate contact voltage (V_c).
3. Pre-bias the device to V_{g1} less than V_c
4. Apply switching voltage (V_{sh}) to G_2 to usher full contact.

The advantage of pre-biasing the device is that the switching voltage of the switch can be dramatically decreased to sub-1 V because the contact gap that needs to be closed is very small and as a result, small voltage on G_2 causes switching. Pre-bias is similar to the back-bias used in CMOS for adjusting the transistor threshold voltage.

Using the pre-bias scheme, we have demonstrated sub- 500 μV switching voltages [21]. Also, since the silicon structure is formed on an oxide layer, voltage transients applied to G_1 feedthrough the buried oxide layer and air to G_3 to generate a floating potential. Figure 2.4 shows the electric field distribution when G_1 voltage is ramped to 50 V which is simulated in COMSOL®. With 50 V applied to G_1, G_3 acquires a floating potential of 11 V which serves as an additional restoring electrostatic force on the source cantilever when G_1 voltage is switched off. This automatic pull-back mechanism might mitigate the stiction problem which plagues NEMS switches.

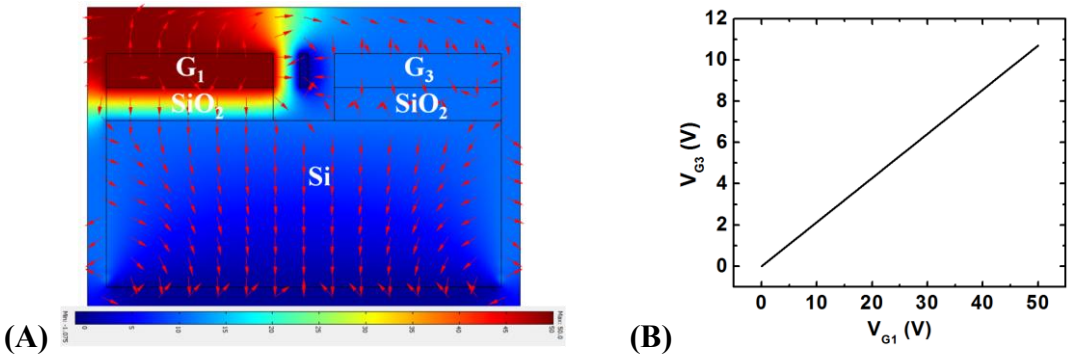


Figure 2.4. (A) COMSOL® electrostatics simulation of the feedthrough effect that is generated when voltage ramps are applied to G_1. The electric field lines couple through air and the SiO_2 layer to terminate on G_3. The acquired floating potential on G_3 provides additional restoring force to the cantilever. (B) As V_{G1} is ramped, electrode G_3 acquires a floating potential V_{G3}.

2.3 *Fabrication of Switch*

The fabrication of the device is illustrated in Figure 2.5 which consists of two levels of phosphorus ion implantation at 185 keV and 135 keV both with $5x10^{15}$ ions/cm^2. This is followed by dopant annealing, e-beam patterning, RIE and DRIE etching, and device release using critical point drying (CPD).

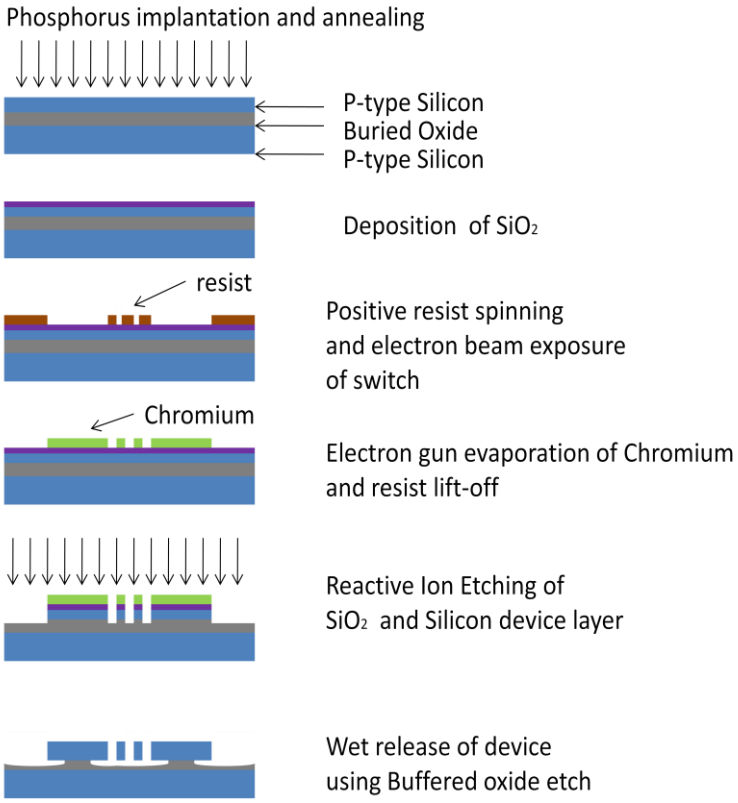


Figure 2.5. Fabrication steps for the Si-Si switch which involves e-beam patterning, metal lift-off, etching and CPD. The phosphorus implantation of the p-type device layer forms a PN-junction in the device layer of the SOI wafer.

2.4 *Measurement Results*

To test the DC performance of the switch, all contacts except G_3 was buffered with a resistor and connected to the Source Measuring Unit (SMU) on the Keithley 4200 Parametric Analyzer as shown in Figure 2.6. The source and drain resistors reduced the kinetic energy and velocity of the device during switching due to the reduction in the voltage drop across the switch when the contact capacitance changes swiftly [22]. To determine $V_{G1,contact}$, 0 V was applied to the source and G_2. The drain was maintained at 5 V and G_1 was swept until the source contacts the drain. During

contact, current moved from the drain to the source, under a compliance of 10 µA. With the contact voltage determined, the source and drain were maintained at 0 V and 5 V respectively and G_1 was pre-biased ($V_{G1,prebias}$) very close to $V_{G1,contact}$ such that $V_{G1,prebias} < V_{G1,contact}$. Now, G_2 is swept in steps of 10 µV to achieve contact. Voltages as low as 300 µV could cause switching. All of the measurements were carried out in vacuum at $4x10^{-4}$ mbar.

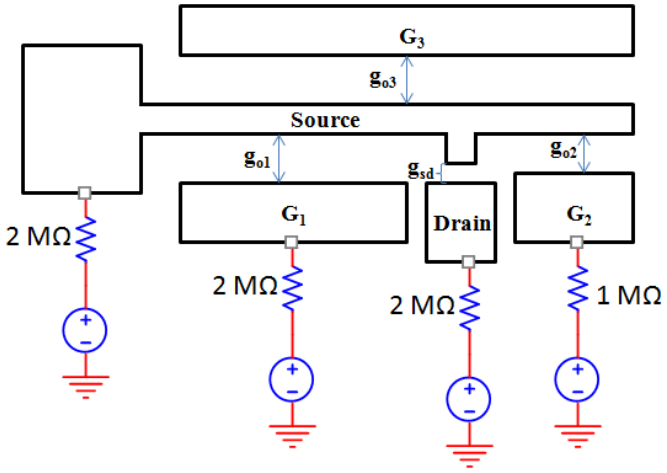


Figure 2.6. Testing scheme for the nanoswitch which shows the biasing of the terminals with current limiting resistors.

2.4.1 Full-Contact Voltage

To investigate the gate contact voltage, the source was grounded and 5 V applied to the drain. G_2 and G_3 were made to float and a 10 µA current compliance set for the drain and source currents. Voltage ramps were applied to G_1 until the source contacted the drain. Both the source and drain currents were monitored. Figure 2.7 is the measured gate contact voltage of 54.82 V with an OFF state drain current of 0.2 nA and I_{ON}/I_{OFF} ratio was 3000. I_S is negative of I_D as expected. The peak ON current under 5 V V_{DS} is 0.6 µA.

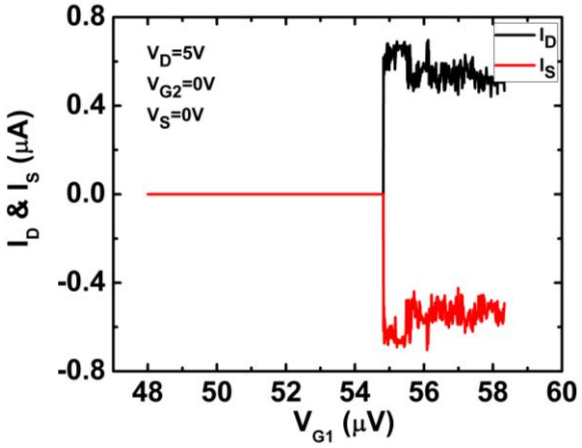


Figure 2.7. I_d versus V_{G1} for device 2. $V_{G1,Contact}$ is measured to be 54.82 V.

The fluctuations in I_{ON} could be due to the smoothing of asperities at the contact, electrical, thermal and structural effects at the contact. G_3 plays a key role in the operation of the device. We also made devices without G_3. Without a floating G_3, switches would easily stick due to adhesion forces. However, the parasitic capacitance between G_1, the cantilever, and G_3, results in a charge distribution that leads to an attractive force between G_3 and the cantilever. This attractive force pulls back the cantilever, when G_1 voltage is removed. The charge on G_3 takes longer time to dissipate than the charge on G_1.

2.4.2 Switching Voltage

With the gate contact voltage determined as 54.82 V, the device was pre-biased to voltages close but smaller than this voltage, such that a smaller voltage on G_2 can make the contact. For example, when 54.80 V was applied as a pre-bias, and voltage ramp is applied to G_2 to usher in full contact. Figure 2.8 is the measured switching voltage of 300 μV. This switching voltage is scalable depending on the gate contact voltage. So as the pre-bias voltage is increased, less voltage is required by G_2 for switching. The switching value of V_{G2} must be above the voltage needed to overcome

the displacements due to Brownian motion of the switch, to ensure that the device does not self-switch.

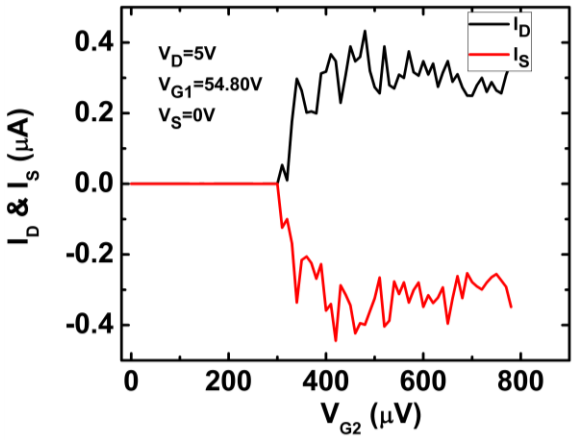


Figure 2.8. With $V_{G1,prebias}$ = 54.80 V and switch contacts at V_{G2} =300 μV.

The lower peak current of 0.3 μA is due to the lower contact force that is generated by G_2. The contact resistance of a NEMS switch is given by

$$R_c = \frac{\rho}{\pi r} \propto \frac{1}{A^{0.5}} \tag{2.2}$$

where ρ is the resistivity of the contact material, r is the contact radius and A is the contact area [13]. For a contact force, F, and a material hardness, H, the contact area can be derived as

$$A = \pi r^2 = \frac{F}{nH} \tag{2.3}$$

where n is an empirical factor. The direct relationship between the contact force and resistance is

$$R \propto \frac{1}{F^b} \tag{2.4}$$

where the value of the factor *b* depends on the regime (elastic, plastic or compressive) of the contact [13]. From Equation (2.4), the ultralow voltage (300 μV) applied at G_2 will produce a low contact force therefore producing a higher contact resistance and a lower ON current.

Using the resistive model as depicted in Figure 2.9, the contact resistance of the switch was ~ 4.3 MΩ, with 5 V S-D voltage. The contact resistance was high due to silicon-to-silicon contact and low contact forces. This problem was partially resolved by fabricating $MoSi_2$ switches using Pt overcoats to realize metal-to-metal contact as discussed below.

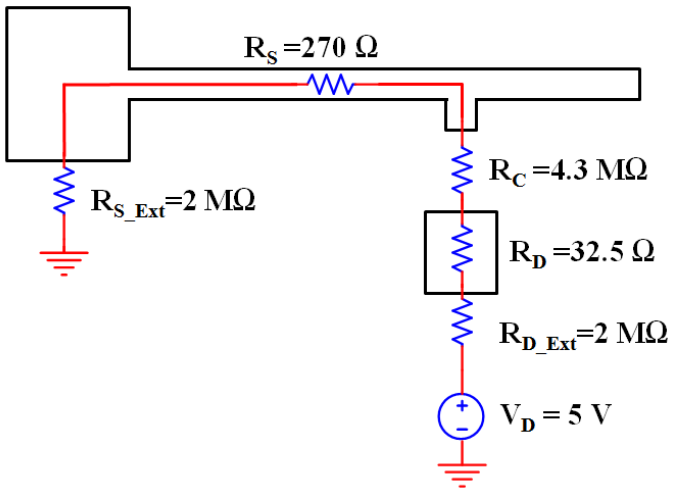


Figure 2.9. Resistive model used to evaluate the contact resistance of the switch.

2.5 *Energy Consumption in Switch*

The energy consumed in the switching process can be approximated as the sum of the electrical and mechanical energy. In the pre-bias phase, applied voltage to G_1 generates a distributed load as indicated in Figure 2.10. The spring constant for the cantilever and the energy consumed are evaluated using Equation (2.5) and Equation (2.6) respectively [23].

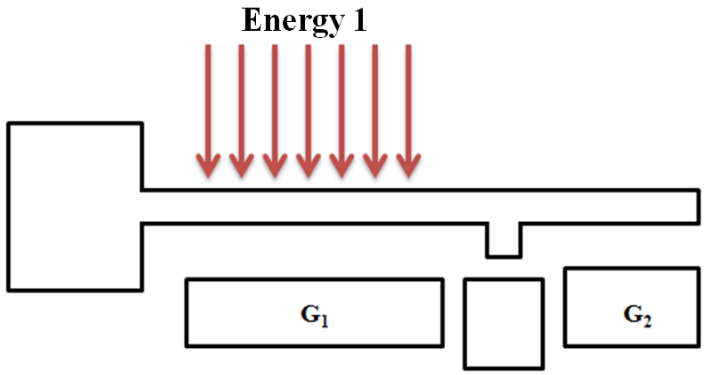


Figure 2.10. When V_{G1} is applied, there is a distributed load on the cantilever just opposite to the electrode G_1.

$$k_1 = \frac{2Ewt^3}{{x_1}^3 + 6x_1 l^2 - 4{x_1}^2 l} \tag{2.5}$$

$$Energy_1 = \frac{1}{2}\varepsilon_0 \frac{A_1}{(g_{01} - y_1)}\left(\frac{y_1}{g_{01}}\right){V_1}^2 + \frac{1}{2}k_1{y_1}^2 \tag{2.6}$$

where V_1 is the applied voltage, E is the Young's Modulus, w is the width, t is the thickness, l the length of the cantilever and x_1 is the actuation length. The actuation area is A_1, the initial gap is g_{01}, and the displacement caused by the applied voltage is

y_1. Using the values in Table 2.1, Matlab® was used to calculate the pre-bias energy to be 86 fJ. Appendix 6.1 is the Matlab® code used to calculate the switching energy.

Table 2.1. Parameters used to calculate the switching energy of the NEMS switch.

Name	Symbol	Value	Unit
Length of cantilever	l	25	μm
Width of cantilever	w	2	μm
Thickness of cantilever	t	250	nm
Effective Young's Modulus	E	194	GPa
G_1 actuation length	x_1	15	μm
Loaded spring constant at G_1	k_1	5.4	μN/m
G_1 gap	g_{01}	900	nm
G_1 displacement	y_1	150	nm
G_1 Voltage	V_1	54	V
G_2 actuation length	x_2	7	μm
Loaded spring constant at G_2	k_2	0.12	N/m
G_2 gap	d_{02}	100	nm
G_2 displacement	y_2	20	nm
G_2 Voltage	V_2	300	μV

The switch was simulated in COMSOL® multiphysics software to determine the relationship between the displacements at different points on the cantilever. Using the schematic in Figure 2.11 and evaluating the displacement values at points A and B, the

simulated results in Figure 2.13 is extrapolated and the following displacement relationship assumed,

$$B = \frac{A}{2} \ and \ C = \frac{B}{2} \tag{2.7}$$

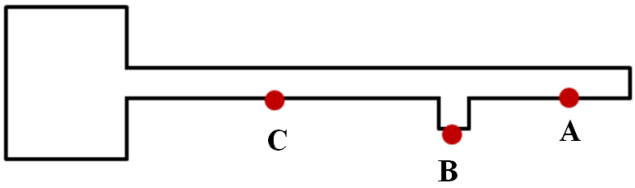


Figure 2.11. The displacement values at G_2 (A), at the contact dimple (B) and at G_1 (C).

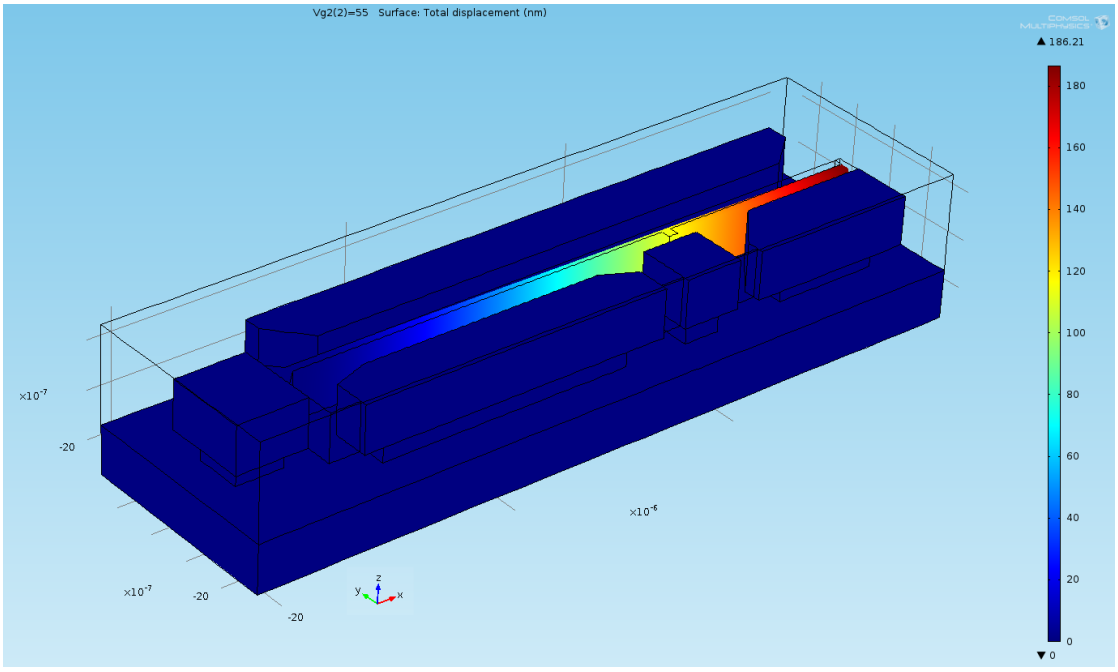


Figure 2.12. 3D COMSOL® simulation to evaluate the displacement of the cantilever with applied voltage to G_1. The device layer of the switch is silicon and it sits on a SiO_2 layer.

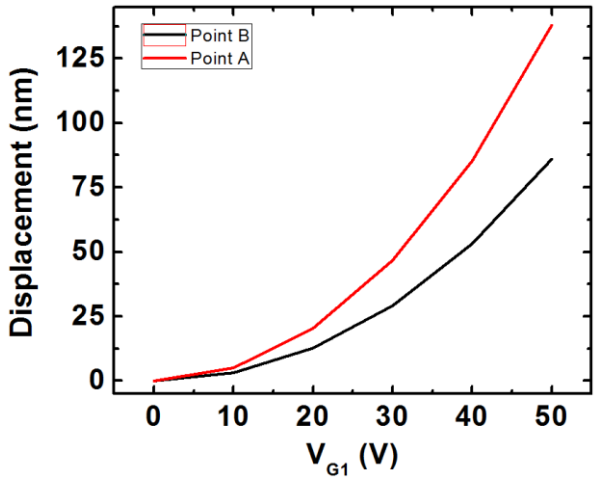


Figure 2.13. The displacement relationship between the tip of the cantilever and the contact dimple.

To fully close the 300 nm contact gap at point B, point A has to be displaced ~600 nm and point C about 150 nm. The pre-bias voltage moves the cantilever very close to full contact such that, the remaining contact gap is assumed to be 10 nm. During pre-bias, the final gap at G_2 is reduced to ~100 nm. Applied switching voltage at G_2 will cause the final closing of the 10 nm contact gap. Since the cantilever is distributively loaded at G_1 and G_2 as shown in Figure 2.14, the spring constant and energy consumption at G_2 are given in Equation (2.8) and Equation (2.9) respectively.

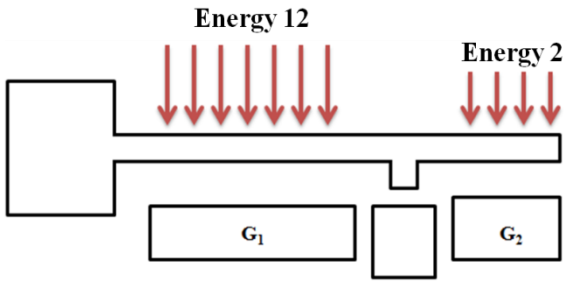


Figure 2.14. Energy distribution along the cantilever. As V_{G2} is applied, there is additional energy, Energy 12, generated at electrode G_1.

$$k_2 = 2Ew\left(\frac{t}{l}\right)^3\left[\frac{1-\left(\frac{l-x_2}{l}\right)}{3-4\left(\frac{l-x_2}{l}\right)^3+\left(\frac{l-x_2}{l}\right)^4}\right] \tag{2.8}$$

$$Energy_2 = \frac{1}{2}\varepsilon_0\frac{A_2}{(d_{02}-y_2)}\left(\frac{y_2}{d_{02}}\right){V_2}^2+\frac{1}{2}k_2{y_2}^2 \tag{2.9}$$

where x_2 is the actuation length at G_2 and d_{02} is the gap at G_2 after pre-biasing the switch. The switching energy at G_2 is calculated to be 24.5 aJ. Also, there is an additional finite amount of energy that is consumed at G_1 due to the applied voltage at G_2. If the gap to close is 10 nm, the displacement at G_1 will be ~5 nm. The energy consumed for 5 nm displacement is 2.9 fJ and it was evaluated using Equation (2.10)

$$Energy_{12} = \frac{1}{2}\varepsilon_0\frac{A_1}{(g_{01}-y_1-\frac{y_2}{4})}\left(\frac{\frac{y_2}{4}}{g_{01}-y_1}\right){V_1}^2+\frac{1}{2}k_1\left(\frac{y_2}{4}\right)^2 \tag{2.10}$$

Total switching energy is

$$Energy = Energy_2 + Energy_{12} = 2.93\ fJ \tag{2.11}$$

The OFF state leakage current ~0.2 nA with pre-bias voltage of 54 V produces a static power dissipation of 10.8 nW. The low switching energy provided at G_2 will enable this switch to find applications in ultra-low powered switching networks. In this case, the device will be powered by pre-biasing all the switches and computation carried out with activation of G_2. The dynamic power depends on the switching

voltage, capacitance of the actuation gap, average switching activity factor and clock frequency [24] .

2.6 *$MoSi_2$ Based NEMS Switches*

The contact resistance for the silicon based switches was high (4.3 MΩ). Hence different metals were investigated to substitute for silicon as the switch structural material. Some of the initial metals that were investigated were Pt, Pd, Ni and Al. The Pt and Pd switches had noticeable stress gradients while the Ni and Al switches did not survive Hydrofluoric Acid (HF) release. $MoSi_2$ was chosen as the structural platform for the switches because it forms good ohmic contact to the source and drain terminals of N-channel JEFT as well as it is a material that is found in CMOS foundries. To reduce gate leakage current and polydepletion effects in future generations of advanced transistors such as the FinFET or Ultrathin-Body MOSFET, the International Roadmap for Semiconductors (ITRS) has suggested the use of high-k gate dielectrics and dual-metal-gate electrodes [25]. $MoSi_x$ and pure Mo seem to be the ideal metal gate stack because of the appropriate work functions to n-channel and p–channel devices respectively [25].

At the same time, MEMS devices are leveraging various materials such as silicon, silicon dioxide and $MoSi_2$ as structural and sacrificial layers that are present in CMOS technology. Besides $MoSi_2$ being a great midgap metal for the next generation of transistors, it has a high Young's modulus (430 GPa) which makes it ideal as a structural material for nanostructures such as accelerometers, switches and gyroscopes. $MoSi_2$ also exhibits a superb etch resistance to HF and Buffered Oxide Etch (BOE). Given all these great attributes of $MoSi_2$, it is well suited as a structural material for the NEMS switch discussed above.

The fabrication of the device is detailed in Figure 2.15. An n-type silicon wafer was oxidized to grow 1.5 μm of SiO_2. A 1 μm thick film of $MoSi_2$ was sputter deposited on the wafer in the presence of Ar gas. Standard photolithography steps were used to pattern the switches. With the resist serving as an etch mask, the $MoSi_2$ layer was dry etched by Cl_2/O_2 chemistry. The stress is reduced by an optimum selection of chamber pressure (2 mTorr), and DC power (1.5 KW). The devices were released by Buffered Oxide Etch (BOE 6:1) and finally dried with a critical point dryer to prevent stiction.

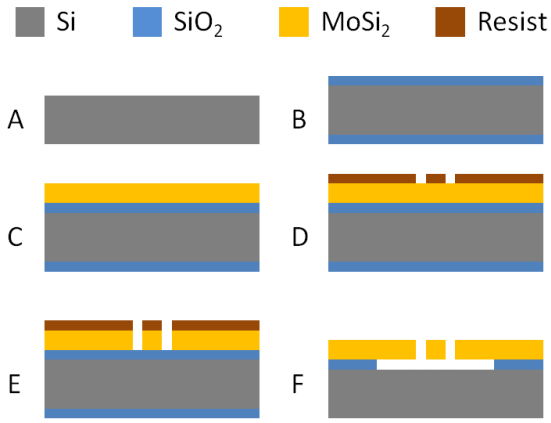


Figure 2.15. Fabrication of the $MoSi_2$ NEMS switch. A) n-type silicon wafer B) LPCVD oxide was grown on each side of the wafer at a temperature of 1100 ºC with 5% HCL. C) $MoSi_2$ was sputter deposited on the wafer at a chamber pressure of 2 mTorr and DC power of 1.5 KW. Ar gas was introduced during the deposition. D) Negative tone resist was spun and exposed with ASML 300C DUV stepper. E) The $MoSi_2$ layer was dry etched with Cl_2/O_2 chemistry. F) Resist strip and device release was carried out using Buffered Oxide Etch (BOE 6:1) and after rinsing in de-ionized water, the device was dried in a critical point dryer.

Figure 2.16 is the SEM micrograph of the device. The device was first tested in ambient to investigate its switching behavior. It was optically observed that even though there was full contact of the source to the drain, no current would flow. It has been well documented in literature that freshly sputtered $MoSi_2$ when exposed to air for 5 minutes forms SiO_2 and a miniscule amount of MoO_2, and after 24hrs exposure the SiO_2 content increased and the MoO_2 was converted to MoO_3 [26]. A proposed reaction that occurs at the $MoSi_2$ interface is given by Equation (2.12) and Equation (2.13) [26].

$$\frac{1}{3}MoSi_2 + O_2 = \frac{2}{3}SiO_2 + \frac{1}{3}MoO_2 \tag{2.12}$$

$$2MoO_2 + O_2 = 2MoO_3 \tag{2.13}$$

The $MoSi_2$ surface was believed to be covered with a duplex oxide layer of SiO_2+MoO_3. This duplex layer could easily absorb carbonaceous contaminants as well as water vapor and hydrocarbons [27].

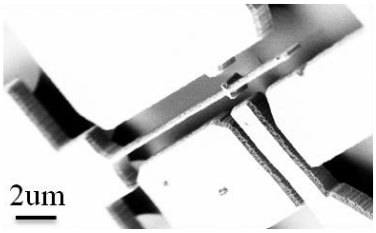


Figure 2.16. SEM image of the fully released free standing $MoSi_2$ switch. As seen in the image, there is minimal stress gradient in the source cantilever.

The drain and source contact areas were insulated with this duplex layer, water vapor and hydrocarbons. Figure 2.17 is the X-ray Photoelectron Spectroscopy (XPS) analysis of the $MoSi_2$ film which was conducted with Surface Science Instrument using a monochromated Aluminum K-alpha x-rays. A 300-µm beam spot size was used for scanning and a flood electron gun was used to neutralize the charges due to the X-ray exposures. Oxygen was used as a reference peak in analyzing the data. As seen in Figure 2.17, the spectra display the presence of the adventitious hydrocarbon (C 1s at 284.6 eV) as well as a high peak of oxygen (O 1s at 532 eV). The highest peak of Mo 3d occurs at 228 eV. The data presented suggests that the oxide formation contributed to the reduce conductance.

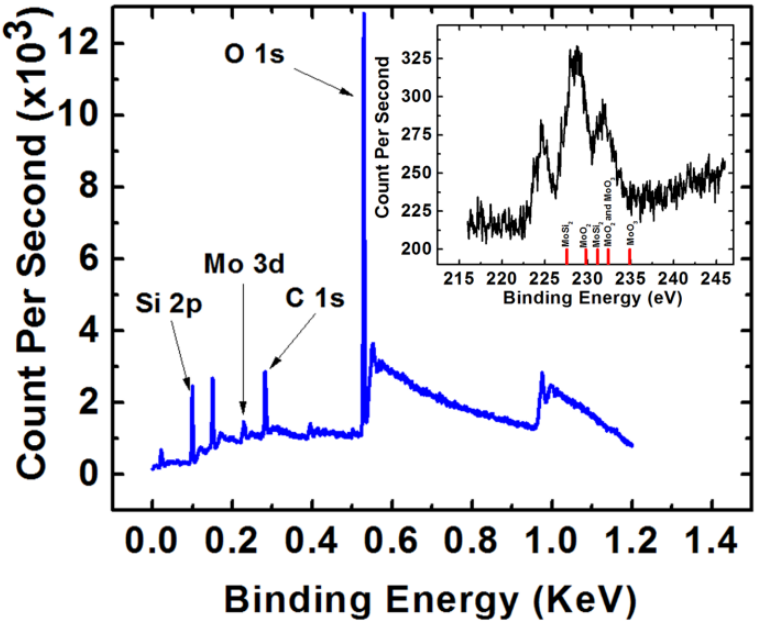


Figure 2.17. XPS scan of the $MoSi_2$ surface shows peaks for silicon, Mo 3d, oxygen and the adventitious hydrocarbon. The 2.95 eV shift in the O 1s peak was used to compensate for this measured results. The inset is a high resolution scan which shows the presence of the Mo $3d_{5/2}$ and Mo $3d_{3/2}$ of the consolidated $MoSi_2$.

2.6.1 Drain Voltage Modulation of Turn-on Voltage

With insight into the formation of the duplex layer at the contact area of MoSi2 switches, we decided to test these devices in vacuum. When the switch was tested in a vacuum probe station, at low pressures of 0.1 mbar, there was insignificant current flow from the drain to the source until the pressure was reduced to ~ $4x10^{-4}$ mbar. At pressures below this value, the water vapor and the hydrocarbons desorbed from the contact area. The device was pre-biased and G_2 ramped to initiate full contact. The drain voltage has an effect on the switching voltage as it also forms an electrostatic actuator. In fact the gate and the drain terminals can be interchanged in this switch. However, by the choice of gaps between the gate and the drain, we do not observe the pull-in instability encountered in MEMS switches. Figure 2.18 shows the effect of the drain voltage on the switching voltage of the device. From Figure 2.18, the switching voltage could be tuned from 8 V to 6.1 V by increasing the drain voltage from 5 V to 8 V.

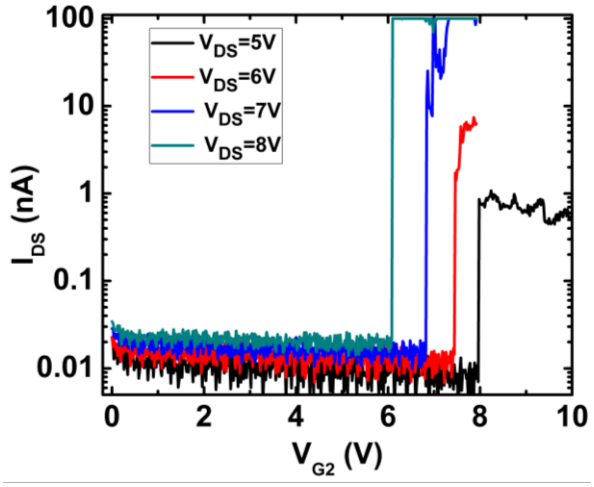


Figure 2.18. Increasing the drain voltage generates additional electric field that attracts the source to contact the drain terminal.

Figure 2.18 also shows that I_{DS} increases 100 folds from V_{DS}=5 V to V_{DS}=8 V. This drastic increment in drain current could be attributed to the fact that as V_{DS} was increased, the electric field at the source and drain contact was also increased to a point where there was a partial breakdown of the SiO_2+MoO_3 duplex layer. To further investigate the possibility of the partial breakdown of the duplex layer, the switch was fully closed and the drain voltage ramped from 0 V to 8 V. Figure 2.19 shows that substantial current conduction begins at V_{DS}=7.3 V where we believe the duplex layer was partially broken down. The duplex layer is broken down and current begins to flow and the linear IV characteristics from 7.3 V to 8 V shows that an ohmic contact is established between the source and drain contacts. The source-drain current conduction path is very resistive (80 MΩ) which is due to the formation of the duplex layer and high contact resistance.

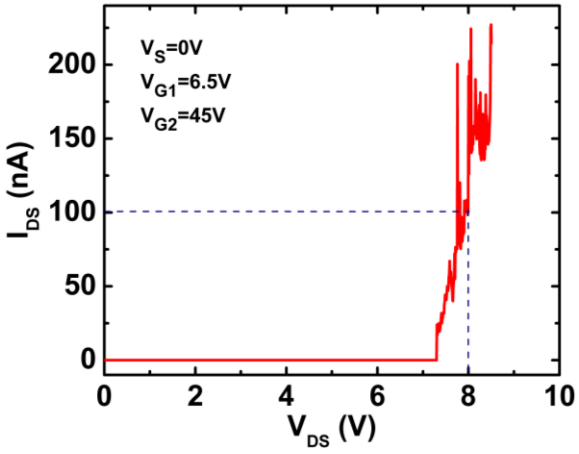


Figure 2.19. Current-Voltage measurement of the source-drain terminals of the closed switch shows that active current conduction begins at V_{DS}=7.3 V.

2.6.2 Endurance Test

The reliability of one the $MoSi_2$ switches was tested by pre-biasing G_1 at 45 V and 8 V applied to the drain with the source grounded. A 50% duty cycle AC signal was applied to G_2 with a peak-to-peak voltage of 18 V, running at 10 kHz. The drain current was sampled every 2 seconds and the experiment terminated when the value of the drain current reduced 8 times. A total of 302,240 cycles where accrued when the switch was stuck. The failure mechanism is not well understood. The failure of the switch could be due to dielectric charging of the duplex layer which caused the source to be stuck to the drain. The failed device was inspected in the SEM but showed that the source was separated from the drain. It is speculated that during the transfer of the switch to the SEM, the dielectric layer could fully be discharged causing the source to separate from the drain. Further research has to be carried out to determine the failing mechanism of the $MoSi_2$ based switch.

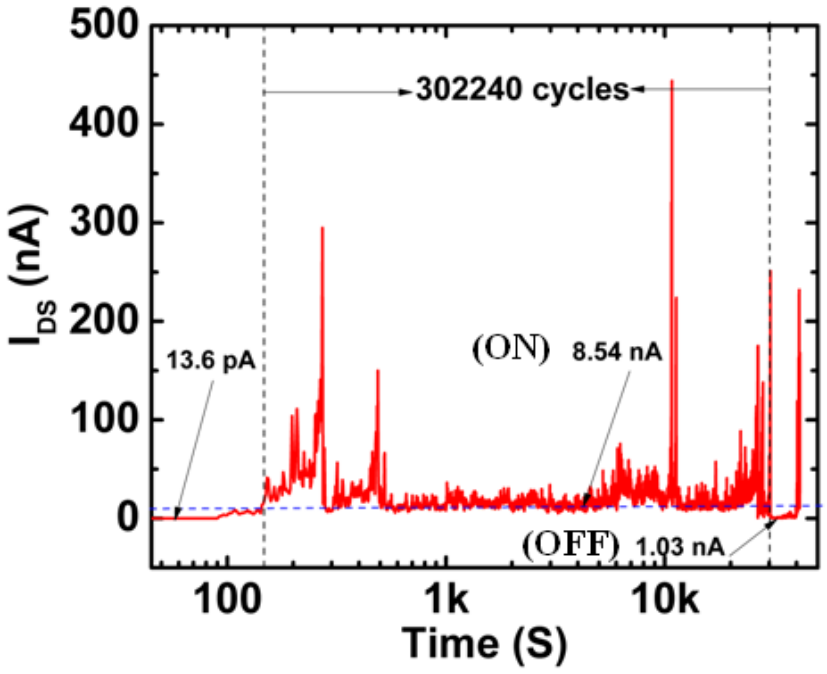


Figure 2.20. Endurance test of the switch.

2.6.3 Pt Coated Electrostatic Switches

The contact resistance of the $MoSi_2$ based switches was too high (80 MΩ). In order to reduce the contact resistance, 10nm/200nm of Cr/Pt respectively was sputter coated on the switches. The fabrication process for the switches is the same as outlined in Figure 2.15. After sputtering Cr/Pt on the switch, all the terminals were "shorted". The device was ion-milled to open up the "shorts." Figure 2.21 shows the SEM image of the Pt coated switch and Figure 2.22 and Figure 2.23 show the switching performance of the Pt coated switches. It should be stated that these measurement were carried out in ambient air and also without any resistor biasing. In Figure 2.23, there is hysteresis which comes from the fact that energy needed to close the switch is different from that needed to open the switch. The switch could sustain 1 mA of current from the drain to the source at a V_{DS} of 1 V reducing the contact resistance to 1 KΩ.

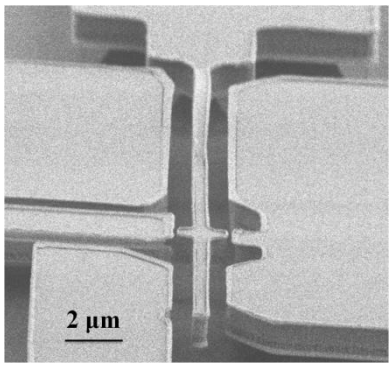


Figure 2.21. SEM image of the $MoSi_2$ switch which is coated with 10nm/200nm of Cr/Pt.

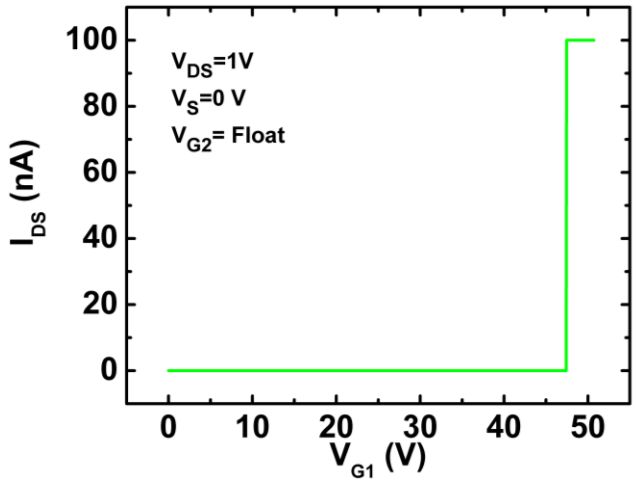


Figure 2.22. Voltage ramps were applied to G_1 until the source was in full contact with the drain. The G_1 contact voltage was 47.5 V and the OFF state drain current was 1.4 pA. The current compliance was set to 100 nA.

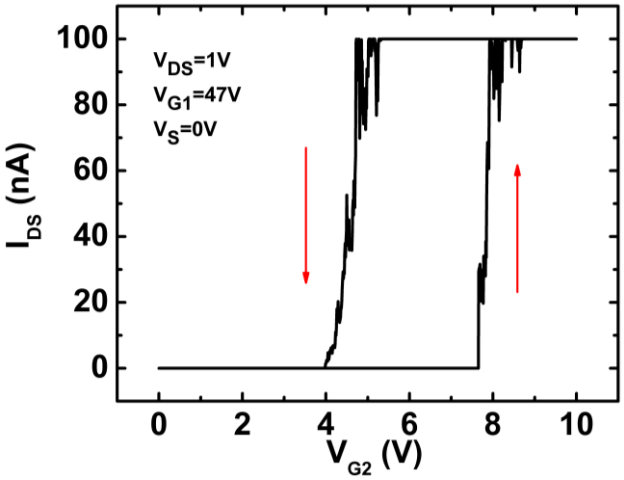


Figure 2.23. With the device pre-biased at 47 V, voltage ramps were applied to G_2 to fully bring the source in contact with the drain. The current compliance was set to 100 nA.

2.7 ***Conclusions***

A new multistep switching scheme is proposed and demonstrated by using multi-gated switch configuration. The switching scheme involves pre-biasing the switch very close to full mechanical contact and finalizing full contact by applying small voltages on another gate. The switch architecture addresses several problems inherent to resistive nanoscale switches such as stiction, contact area degradation and high switching voltages. To reduce the contact resistance, Pt-to-Pt contact was explored. However this work demonstrates a very low sub-KT voltage switch which can be useful for many nanoscale applications.

Chapter 3

JFET INTEGRATION INTO NEMS COMPONENTS

3.1 *Introduction*

In the previous chapter, SOI NEMS switches were fabricated and characterized. In this chapter, Junction Field Effect Transistors (JFETs) are monolithically integrated into the NEMS switch. JFETs tend to be the preferred front-end transistor for signal amplification due to its low noise characteristics. JFETs are volume conduction devices and do not suffer from interface trap and release current noise that exists in MOSFETS thus offering very low 1/f noise spectrum. The JFET can be integrated into the NEMS device either by monolithic integration or through the two chip solution. In monolithic integration, both the active device and the NEMS devices are fabricated on the same wafer where as in the two-chip solution, the active and NEMS components are fabricated on separate wafers and the individual dies are wirebonded together. Monolithic integration is preferred to the two-chip integration due to reduced parasitics and mismatches, and overall effort to decrease system size.

3.2 *Integrated Junction Field Effect Transistor with NEMS*

A JFET is a majority carrier drift conduction based transistor where electrons and holes flow from the source to the drain. Figure 3.1 (A-C) shows the cross-section of a 4-terminal n-channel JFET. The cross-section shows the gradual increase in the depletion width as V_{DS} is increased [28]. The source, G_1 and G_2 are tied to ground. With a small drain voltage applied, the channel acts like a resistor and current flows from the drain to the source and the I_D versus V_{DS} characteristic is ohmic as illustrated

in region I of Figure 3.1(D). As the drain voltage is increased, the reverse bias on the PN- junction between the drain and the gates are further reverse biased. The depletion region between the gate-to-channel increases due to this reverse bias [28]. The widening of the gate-to-channel depletion region into the channel area causes the resistance of the channel to increase as represented in Figure 3.1(B) and region II on the I_D versus V_{DS} curve in Figure 3.1(D). As the drain voltage is further increased, the depletion regions from both gates meet at the drain and the channel is "pinched-off." The drain current saturates and any further increase in the drain voltage does not introduce considerable change in the drain current.

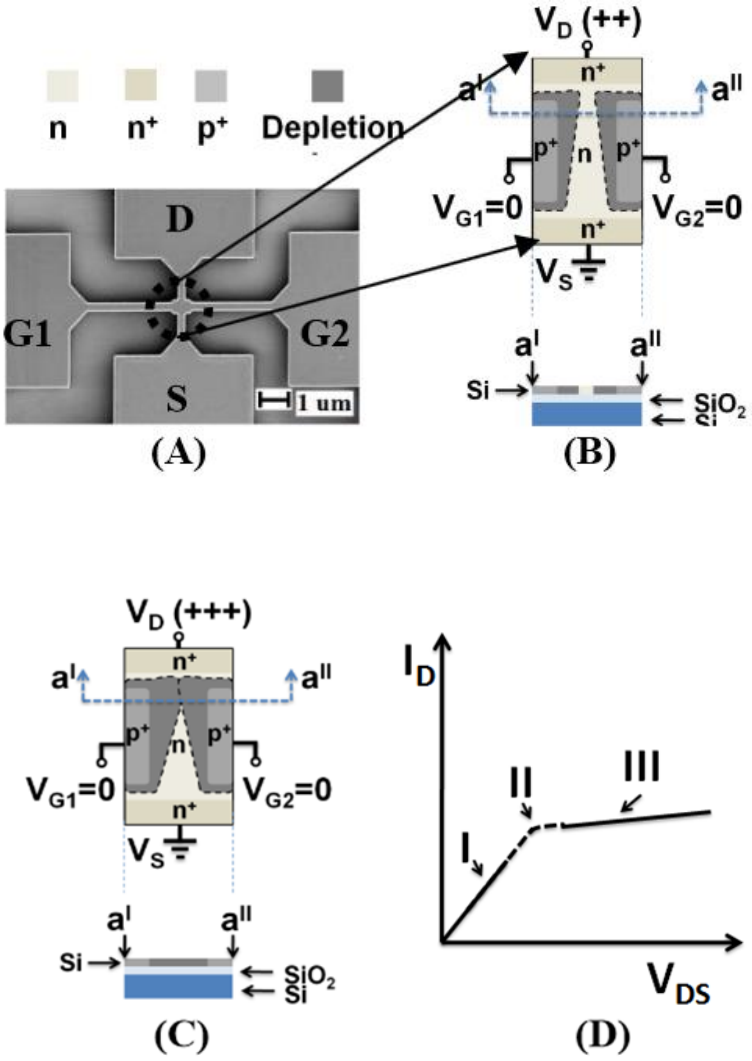


Figure 3.1. (A) SEM image of 4-terminal JFET. (B) As a lager V_{DS} is applied, the gate-channel depletion region gets wider and pushes into the channel as a result increasing the channel resistance. (C) Pinch-off is reached when the area around the drain is fully depleted and further increase in V_{DS} has insignificant change in the drain current. The drain current saturates. (D) IV characteristics for zero gate voltage. Region I is for case (A), region II is for case (B) and region III represents the situation in (C).

At pinch off, the electrons are swept across the pinched off region under the electric field. At higher than pinch off voltage, the effective length of the device decreases which in turn increases the channel current, causing an increase in the effective output resistance of the transistor in conduction mode. Figure 3.1(C) and Region III on Figure 3.1(D) demonstrate the saturation phenomenon.

The saturation current can be approximated as

$$I_D(sat) = I_{DSS}\left(1 - \left(\frac{V_{GS}}{V_P}\right)\right)^2 \tag{3.1}$$

where I_{DSS} is the maximum current when V_{GS}= 0 V and V_P is the pinch-off voltage. Relying on the working principles of the n channel JFET, the motion of a NEMS cantilever was sensed using an integrated JFET. The schematic of the JFET-NEMS device and its SEM image are shown in Figure 3.2 (A) and (B).

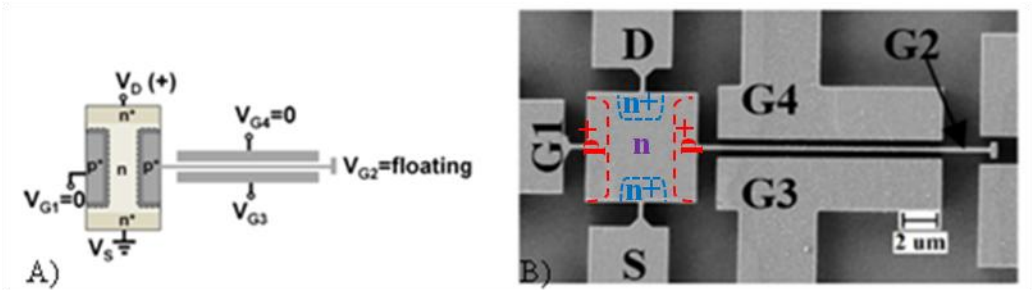


Figure 3.2. (A) Schematic of the JFET-MEMS device. With applied V_{G3}, G_2 (cantilever) acquires a floating potential, which is able to modulate the channel conductance of the JFET. (B) SEM image of the device.

The conducting channel is lightly n-type doped. The gates are p+ doped and the source and drain are n+ doped. The JFET portion is made up of G_1, Drain (D) and Source (S) and the NEMS portion consists of a 250 nm wide cantilever (G_2) which is surrounded by G_3 and G_4.

3.2.1 Device Modeling of JFET

The pinch-off voltage was modeled using Atlas® software. Modeling the 3-terminal JFET, the source terminal was placed at 0 V and +10 V applied to the drain. G_1 was swept from 0 V to -30 V. When V_{G1} was 0 V, the area around the drain was more reversed biased than at the source as shown in Figure 3.3 . The orange region indicates the concentration of majority electrons. As V_{G1} is increased to -16 V, the gate depletion region extends into the channel. Further increasing V_{G1} to -24 V fully depletes the channel. The pinch-off voltage extracted from this simulation was -22.5 V as shown in Figure 3.4 which is close to the measured value of -19 V as will be shown later.

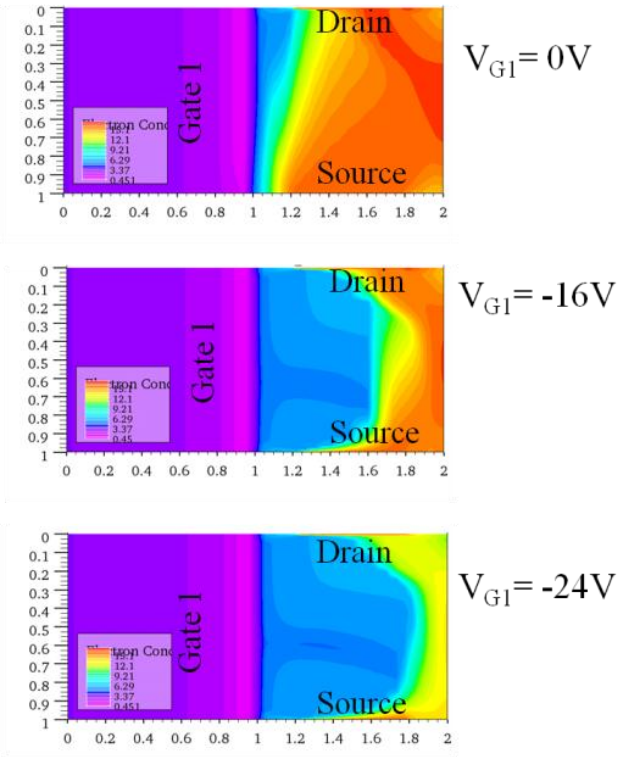


Figure 3.3. Atlas® software was used to evaluate the pinch-off voltage of the JFET. The channel area was 1 µm by 1 µm with an n-type channel doping of 4.16×10^{14} ions/cm^3. The source, drain and gate doping were degenerate (1×10^{20} ions/cm^3).

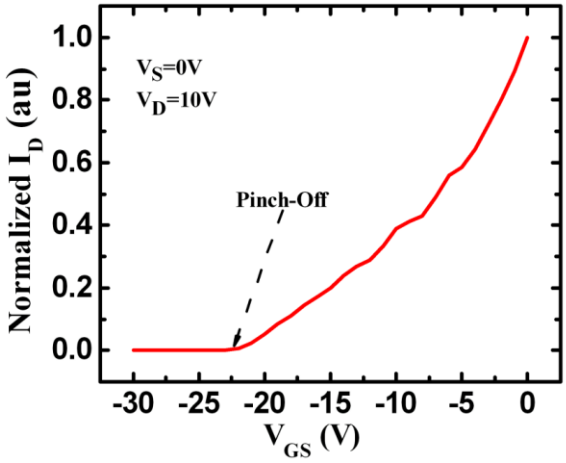


Figure 3.4. The pinch-off voltage was simulated to be -22.5 V which is close to the measured value of -19 V.

3.2.2 Device Modeling of NEMS

To investigate the displacement of the cantilever, COMOL® multiphysics software was used to simulate the structural and electrostatic properties of the cantilever. Figure 3.5 is the schematic of the device and since this simulation was 2D, it did not include the effect of the capacitive coupling from G_3 through the oxide layer to G_4 generating a floating potential on G_4. However, it does predict the floating potential on the cantilever which is due the capacitive coupling through air. Figure 3.6 is the capacitive model of the device and Figure 3.7 shows the deflection of the cantilever as voltage ramps were applied to G_3. Figure 3.8 is a plot of the cantilever tip displacement with applied V_{G3}. Using Equation (2.1) and Table 3.1, the pull-in voltage was calculated to be 33 V.

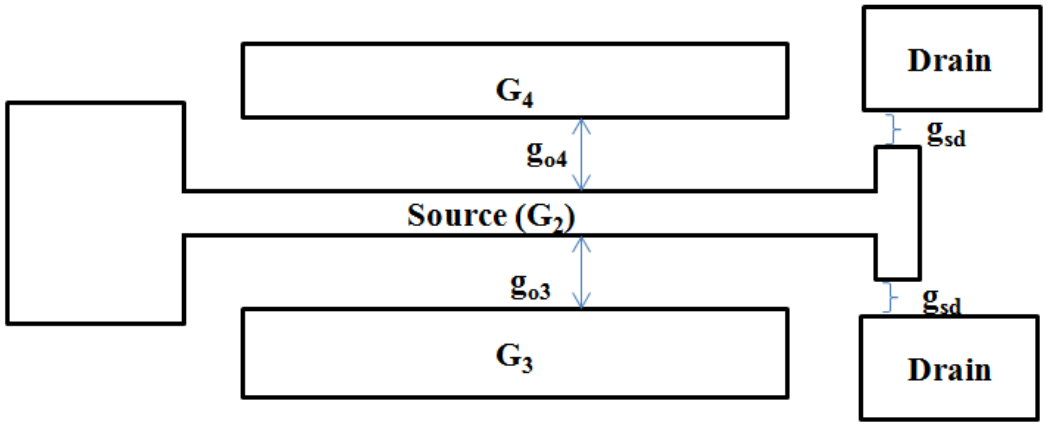


Figure 3.5. Schematic of the NEMS switch showing the gates, source, drain and air gaps.

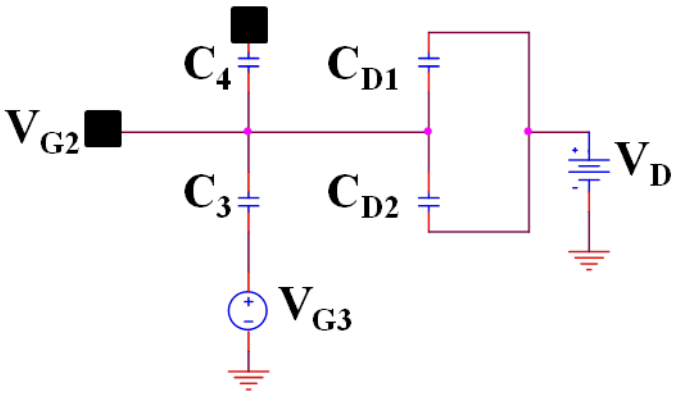


Figure 3.6. Capacitive model for the NEMS component of the device. The cantilever and electrode G_4 are electrically floating.

Table 3.1. NEMS switch parameters

Parameter	Value (μm)
Length	20
Width	2
Thickness	0.25
$g_{03}=g_{04}$	0.45
g_{sd}	0.30

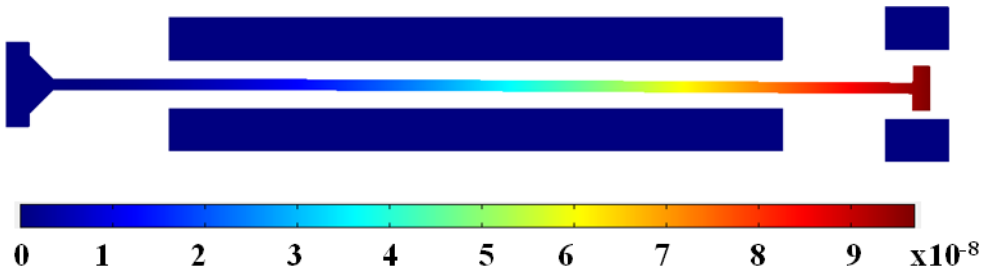


Figure 3.7. COMSOL® multiphysics software was used to simulate the bending of the cantilever as voltage ramps were applied to G_3. With V_{G3}= -16 V, the free tip of the cantilever displaces 60 nm.

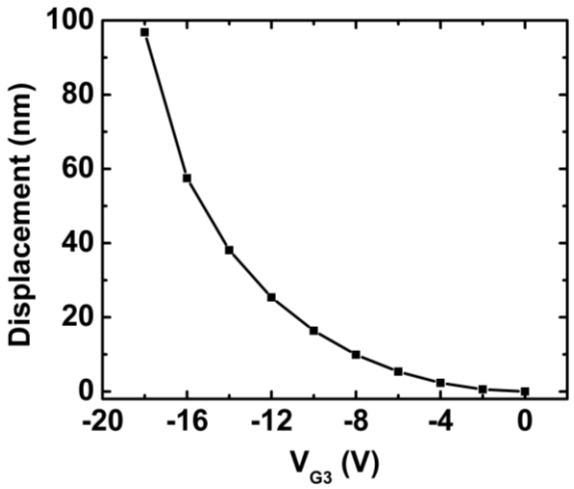


Figure 3.8. A plot of cantilever tip displacement vs. V_{G3} as voltage ramps are applied to G_3.

As voltage ramps were applied to G_3, a floating potential was mirrored onto G_2 (cantilever). This floating potential modulates the channel conductance of the JFET. Hence, there is a correlation between the displacement of the cantilever and the modulated drain current. Figure 3.9 is the simulated electrostatic potential on the switch. With -16 V applied to G_3, the floating potential generated on the cantilever was -7.3 V as shown in Figure 3.10 which modulated the channel of the JFET.

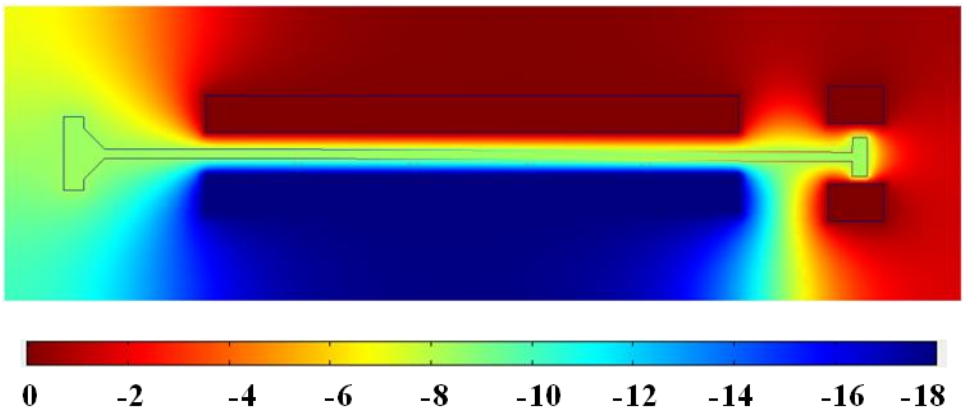


Figure 3.9. The electrostatic potential distribution surrounding the switch when voltage ramps were applied to G_3.

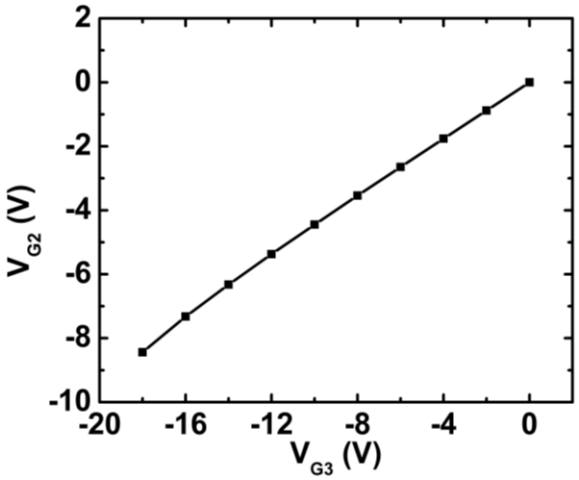


Figure 3.10. A plot of the floating potential on the cantilever as voltage ramps were applied to G_3.

3.3 *JFET/NEMS Fabrication*

The devices were realized in 2 μm-device layer n-type SOI wafer with resistivity of 10 Ω-cm . The key feature in the fabrication process was that both the JFETs and the NEMS components were simultaneously patterned on the same wafer using electron beam lithography which eliminated the conventional post-processing of the NEMS components on a CMOS chip. The fabrication steps are presented in Figure 3.11. The contact electrodes were silicidated with $MoSi_2$. This was done to ensure that there was ohmic contact between the Si and the probing pads. $MoSi_2$ is sputtered and Rapid Thermal Annealed (RTA) at 750°C in Ar gas to form the ohmic contacts [29]. The fabrication process used 4 levels of electron beam lithography and 5 levels of photolithography. The mask count could be drastically reduced to 4 if DUV lithography was used for the exposures.

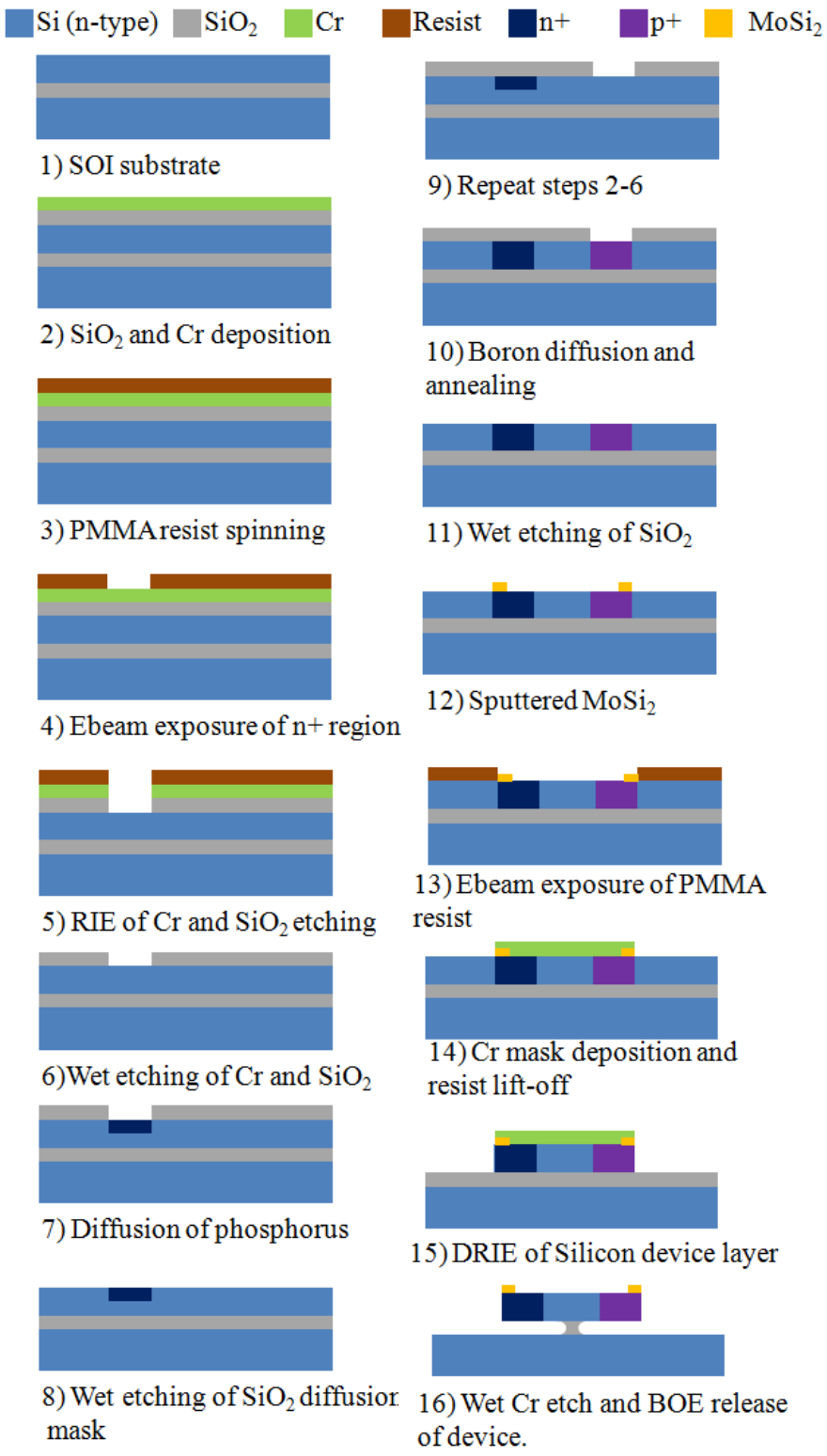


Figure 3.11. Fabrication of JFET/NEMS device using SOI wafer.

3.4 *Measurements*

3.4.1 DC Measurements

All IV measurements were carried out in vacuum (~4x10^{-4} mbar) to enhance the high Q for the NEMS beams. The measurements described here are for the device shown in Figure 3.2 (B). Figure 3.12 is the plot of I_D versus V_{DS} and it shows saturation as the channel is pinched-off. Figure 3.13 is a graph of I_D versus V_{G1} which shows the expected pinch-off voltage V_p= -19 V. I_{DSS} was measured to be ~700 nA when V_{GS}= 0 V and V_{DS}=10 V.

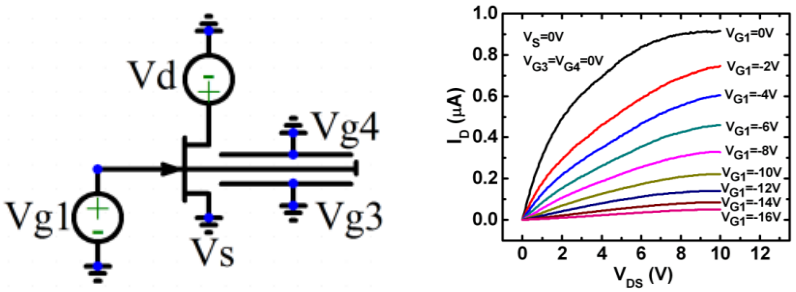


Figure 3.12. Measured I_{DS} vs. V_{DS} output curves for JFET/NEMS device. The measured low current is due to the high drain and source resistances.

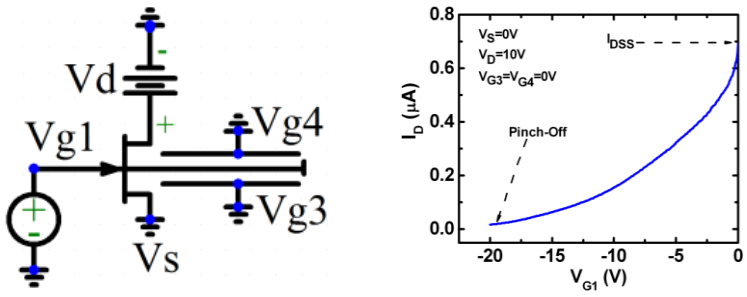


Figure 3.13. Transfer curve for the JFET/NEMS device biased at V_{DS}=10 V.

Since the gate-channel was reverse biased, the gate leakage current should be minimal and it was measured to be ~70 pA at V_{GS}= -19 V as illustrated in Figure 3.14.

For a PN junction of area 4 μm^2, this corresponds to a leakage current of 17.5 pA/ μm^2.

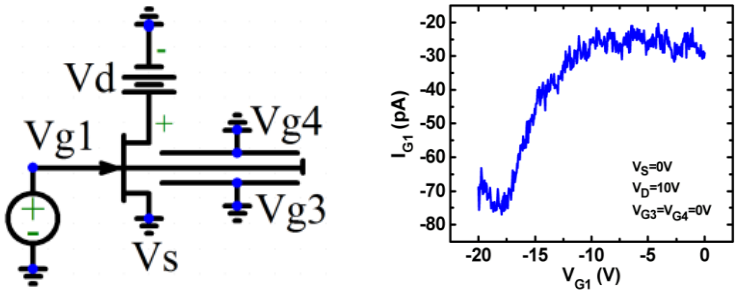
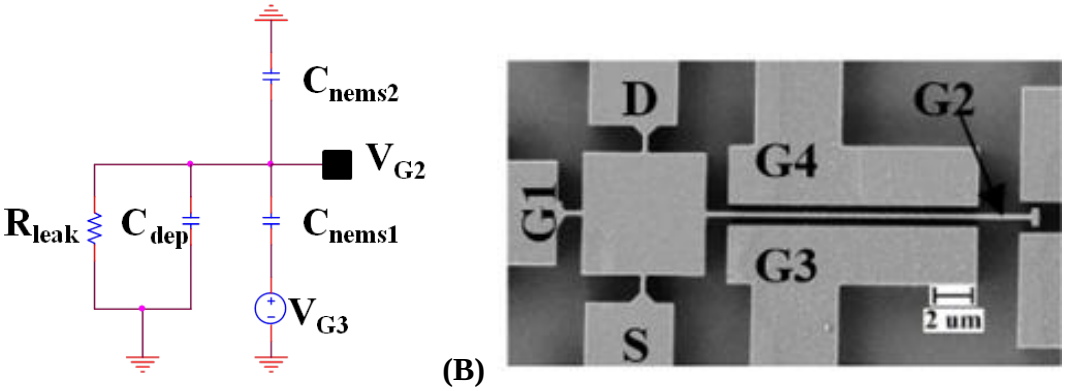


Figure 3.14. The gate leakage current when the JFET was turned off was ~70 pA.

3.4.2 Motion Sensing

When the G_1-to-channel junction is reversed biased, its junction depletion width increases. With further increment in the reverse bias voltage, the channel could be "pinched-off". G_3 and G_4 are used to actuate the cantilever, with G_2 affecting the channel conductance. Figure 3.15 (A) and (B) are the equivalent electrical model and SEM image of the JFET-NEMS device respectively.



(A) **(B)**

Figure 3.15. (A) Equivalent electrical model of JFET-NEMS device. The gate potential at JFET G_2 is due to capacitive divider from G_3 to JFET source (B) SEM micrograph for the JFET-NEMS device.

When a voltage is applied to G_3, the cantilever moves closer to G_3 due to electrostatic force of attraction. The electrostatic force between G_3 and the cantilever is given by Equation (3.2) and the force between the cantilever and G_4 (assumed to be grounded in this analysis) is given by Equation (3.3)

$$F_1 = \frac{1}{2}\frac{\varepsilon_0 A}{(d-x)^2}(V_{G3} - V_{G2})^2 \tag{3.2}$$

$$F_2 = -\frac{1}{2}\frac{\varepsilon_0 A}{(d+x)^2}(V_{G2})^2 \tag{3.3}$$

where ε_0 is the permittivity of vacuum, $A=8x10^{-8}\ cm^2$ is the actuator area, $d=350\ nm$ is the initial gap, and x is the beam displacement.

$$F_3 = F_1 + F_2 \tag{3.4}$$

Using Taylor series approximation,

$$F_3 = \frac{1}{2}\frac{\varepsilon_0 A}{(d)^2}\left[(V_{G3} - V_{G2})^2\left(1 + 2\frac{x}{d}\right) + (V_{G2})^2\left(-1 + 2\frac{x}{d}\right)\right] \tag{3.5}$$

F_3 is a parasitic force which is a negative spring and it's known as spring softening. At equilibrium, the electrostatic force, F_3 and any applied force, F is equal to the spring force, kx.

$$F + F_3 = kx \qquad F = m.a \tag{3.6}$$

where *m* is the mass, *a* is the acceleration. Here, *k* (0.22 N/m) is the spring constant of the cantilever. From Equation (3.6), the displacement of the cantilever can be written as

$$x = \frac{F + F_3}{k} \tag{3.7}$$

The equivalent large signal capacitive model for the JFET-NEMS device is a simple capacitive divider as illustrated in Figure 3.15 (A). From the capacitive model and neglecting the leakage resistor R_{leak}, the floating potential V_{G2} of the cantilever is given by Equation (3.8).

$$V_{G2} = \left(\frac{C_{nems1}}{C_{nems1} + C_{nems2} + C_{dep}}\right) V_{G3} \tag{3.8}$$

where C_{nems1} is the capacitance between G_3 and cantilever, C_{nems2} is the capacitance between the cantilever and G_4 and C_{dep} is the depletion capacitance at the cantilever-JFET junction. C_{nems1} and C_{nems2} are approximated as under small displacement assumption.

$$C_{nems1} = \frac{\varepsilon_0 A}{d - x} \approx C_0 \left(1 + \frac{x}{d}\right) \tag{3.9}$$

$$C_{nems2} = \frac{\varepsilon_0 A}{d + x} \approx C_0 \left(1 - \frac{x}{d}\right) \tag{3.10}$$

Eq. (3.7) can be substituted into Eq. (3.9) and Eq. (3.10). At the cantilever-JFET junction, the depletion capacitance is given by

$$C_{dep} = \left(\sqrt{\frac{q\varepsilon_{si}N_d}{2(V_{bi} - V_{G2})}} \right) A \tag{3.11}$$

$$V_{G2} = \left(\frac{C_0\left(1 + \frac{x}{d}\right)}{C_0\left(1 + \frac{x}{d}\right) + C_0\left(1 - \frac{x}{d}\right) + \left(\sqrt{\frac{q\varepsilon_{si}N_d}{2(V_{bi} - V_{G2})}} \right) A} \right) V_{G3} \tag{3.12}$$

where C_0 is the nominal capacitance, q is the electron charge, ε_{si} is the permittivity of silicon, $N_d = 4.16x10^{14}\ ions/cm^3$ is the doping concentration in the channel assuming a one-sided junction and $V_{bi} = 0.81\ V$ is the built-in potential. V_{G2} can be determined numerically by substituting Equations (3.9), (3.10) and (3.11) into Equation (3.8) and the result is illustrated in Figure 3.16. The numerical simulation is in agreement with the result that was obtained in the COMSOL® simulation in Figure 3.7 and Figure 3.9. The Matlab® code for the numerical evaluation is outlined in Appendix 6.2 and 6.3.

Table 3.2. Capacitance values of the JFET-NEMS device.

	Area (m^2)	**Permittivity (J/V^2)**	**Capacitance(@ V_{G3}= -26 V)**
C_{dep}	$2x10^{-12}$	$1.05x10^{-10}$	45.1 aF
C_{nems1}	$40x10^{-12}$	1	0.96 fF
C_{nems2}	$40x10^{-12}$	1	0.61 fF

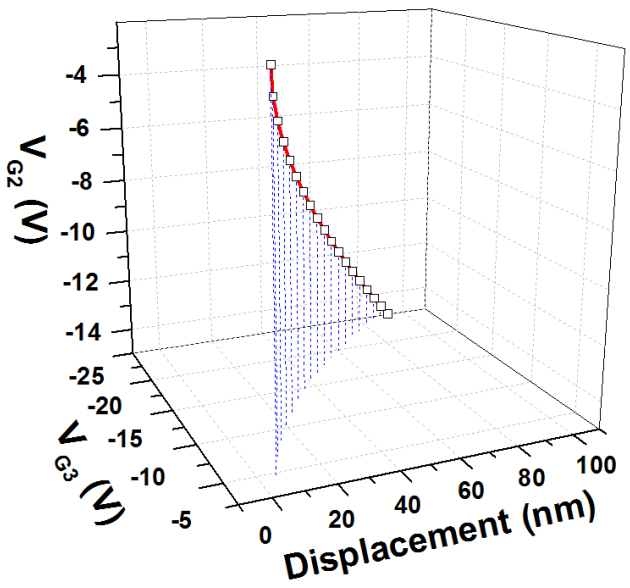


Figure 3.16. The applied voltage V_{G3} generates an electrostatic force of attraction between the cantilever and G_3. This electrostatic force causes the cantilever to displace and the capacitive coupling in the air gaps produces a floating potential V_{G2}. As V_{G3} increases, the displacement of the cantilever also increases and the floating potential V_{G2} increases.

To sense the motion of the cantilever, the drain voltage is swept from 0 to 3 V. The source, G_1 and G_4 voltages are placed at 0 V. As V_{G3} is decreased, the cantilever moves closer to the G_3 electrode due to electrostatic force. Since the cantilever beam is floating, during the motion of the beam, it acquires a floating potential through capacitive coupling. This floating potential (V_{G2}) modulates the channel conductance. As the cantilever moves closer to G_3, C_{nems1} increases and it results in the increase of V_{G2}. Since V_{G3} is negative, V_{G2} is also negative according to Equation (3.8) and it reverse biases the cantilever-JFET junction. Figure 3.17 shows the plot of the response of the JFET to the motion of a clamp-free cantilever.

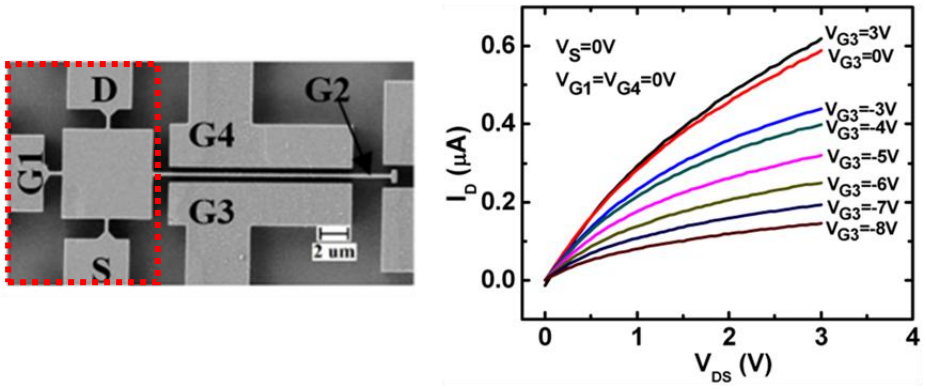


Figure 3.17. The JFET-NEMS device is able to sense the motion of the clamp-free cantilever as voltage ramps are applied to G_3.

The movement of a clamp-clamp cantilever was also investigated illustrated in Figure 3.18. Since the clamp-free cantilever has a higher displacement with the same V_{G3}, its V_{G2} is higher than the case of clamp-clamp beam and it is able to modulate the drain channel conductance better. The drain current modulation could be also partly due to piezoresistive effect at the cantilever-channel junction that occurs as the beam bends. Table 3.3 shows some of the device parameters of the JFET-NEMS device.

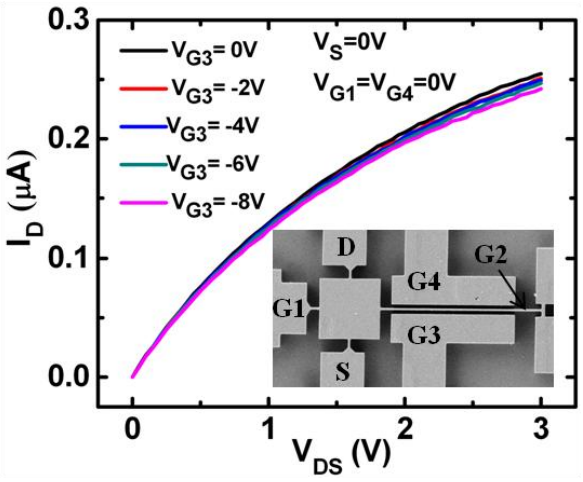


Figure 3.18. The JFET-NEMS device is able to sense the motion of clamp-clamp cantilever.

Table 3.3. JFET/NEMS device parameters

Parameter	Value
Length of cantilever	20 μm
Width of cantilever	250 nm
Thickness	2 μm
Vpull-in	21 V
Resonance Frequency	753 kHz
G_3 and G_4 air gaps	350 nm
JFET channel area	16 μm^2
Vp (V_{DS}=10V)	-19 V
I_{DSS}(V_{DS}=10V)	0.69 μA
$\beta(I_{DSS}/Vp^2)$	1.9 mA/V^2

3.5 ***Noise in JFET***

Fundamental electronic noise is due to stochastically random processes which mean that the exact value of noise cannot be known at any given time [30]. To determine the noise in a device or circuit, its characteristics has to be observed over time and averaged. There are various types of noise in transistors and the most common ones are: Shot noise, Thermal or Johnson noise, Flicker noise, Pink noise, popcorn noise, and etc.

Shot noise: This comes about as a result of discrete changes in current flow. In PN-junctions, electrons need enough energy to jump over barriers. As the electrons gather enough potential energy, they cross the barrier by converting this potential energy into kinetic energy [30]. The charges come in discrete packs and are discontinuous. The randomness of the arrival time of the charges across the barrier generates a "pop" sound.

$$\overline{\iota_s^2} = 2qI_G BW \tag{3.13}$$

where q is the charge of an electron, I_G is the measured DC operating gate current and *BW* is the measuring bandwidth.

Thermal or Johnson noise: The thermal energy drives movement of electrons at temperatures above absolute zero generating a statistical variation of the number of electrons in any given volume. This random number of carriers creates a current variation which leads to an effective noise voltage across a resistor. This voltage noise is dependent on the temperature but independent of the current flow [30].

$$\overline{\iota_t{}^2} = 4K_BT\left[\frac{2g_m}{3}\right](BW) = 4K_BTR(BW) \tag{3.14}$$

where K_B is the Boltzmann constant, T is the temperature, g_m is the transconductance of the JFET.

Flicker noise: There are two schools of thought for the origin of Flicker noise. The first is the Number Fluctuation Model which stipulates that flicker noise is a surface effect. When electrons migrate on the surface of the channel, some of these electrons tunnel into the gate and the electrons are released with different times. The longer one waits, more exchange of charge with traps can occur. On the other hand, the Bulk Mobility Model postulates that the Flicker noise is a volume effect [31] . As electrons migrate in the channel, they interact with the lattice vibrations which are phonons in this case. This interaction leads to a fluctuation in the mobility of the carriers and results in flicker noise.

$$\overline{\iota_f{}^2} = \frac{K_f I_D}{f} BW \tag{3.15}$$

where K_f is flicker noise coefficient, I_D is the drain current and f is the frequency.

Since JFETs are known to be volume conduction devices, the major noise components are thermal and flicker noise. Figure 3.19 shows the equivalent noise circuit for the JFET where it is assumed that the shot noise is negligible. $\overline{\iota_t{}^2}$ and $\overline{\iota_f{}^2}$ are the mean square thermal and flicker noise respectively.

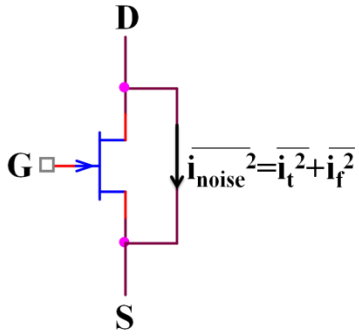


Figure 3.19. Equivalent noise circuit for the JFET.

The total noise is:

$$\overline{\iota_{noise}{}^2} = \overline{\iota_t{}^2} + \overline{\iota_f{}^2} \qquad A^2/_{Hz} \tag{3.16}$$

3.5.1 Noise Measurement

To determine the total noise of the JFET, both the transfer and output characteristics of the JFET were measured using the Keithley 4200. At V_{DS}=2 V, the transconductance (g_m) and output conductance (g_{out}) of the transistor was 11 µS and 1 µS respectively. Before measuring the noise of the JFET, the noise floor of the measuring setup was measured. This noise flow was subtracted from the measured JFET noise. Figure 3.20 is the schematic of the measuring setup.

The gate and source terminals of the JFET were shorted to the ground terminal on the Keithley 4200. Since the SR570 could only accept 5 mA maximum input current, the JFET was biased with V_{DS}=+2 V and V_{GS}=0 V. For proper operation of the JFET, the output conductance of the JFET must be less than the selected sensitivity of the low noise transimpedance amplifier (SR570) [32].

$$g_{out} < Sensitivity \tag{3.17}$$

The sensitivity was selected to be 50 μA/V since the output conductance was measured to be 1 μS. To compensate for any background noise and the input offset current of the transimpedance amplifier (TIA) used in the SR570, an offset current of 1 pA was introduced at the input of SR570 to cancel the input offset current of the TIA. If the offset current is not applied, the drain noise current will sink into the gate of the TIA without going through the feedback resistor to be converted into a voltage noise.

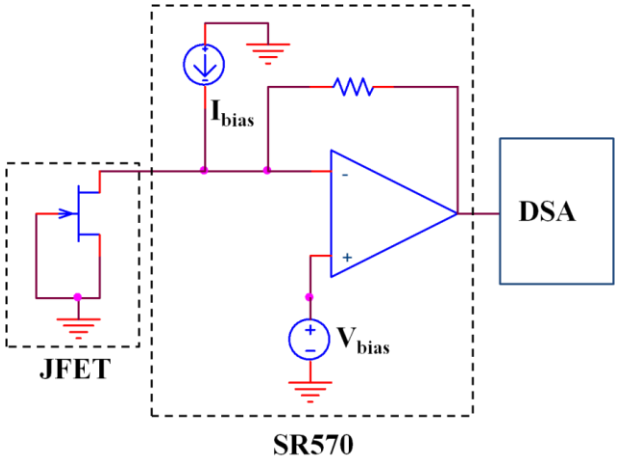


Figure 3.20. Schematic showing the connection of the JFET to the SR570 and finally to the Digital Spectrum Analyzer (DSA). The source and gate terminals of the JFET were shorted to the ground terminal of the Keithley 4200.

When the SR570 was used to provide a drain bias voltage, it generates a DC voltage at the input of the SR570. This bias voltage (V_{bias}) produces an offset current that has to be compensated for. Figure 3.21 shows the current flow in the JFET and the SR570.

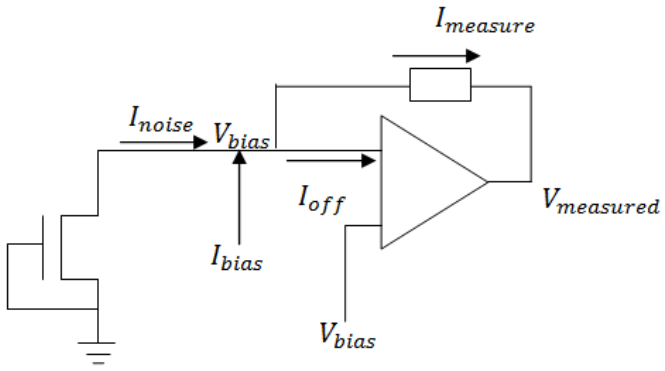


Figure 3.21. Schematic that shows the various currents from the JFET to the SR570. The bias current cancels the current offset.

I_{noise} - noise from JFET

I_{bias} - SR570 bias current

I_{off} - current offset of the SR570 opAmp

$I_{measure}$ - measured current

V_{bias} - SR570 voltage bias that is applied to the drain of JFET.

$$I_{noise} + I_{bias} = I_{off} + I_{measured} \tag{3.18}$$

$$I_{noise} = I_{measured} \tag{3.19}$$

$$\overline{I_{noise}{}^2} = S^2 * \overline{V_{noise}{}^2} \tag{3.20}$$

S represents the sensitivity (A/V) setting of the SR570. The current noise ($\overline{\iota_{noise}{}^2}$) spectrum was computed by multiplying the voltage noise spectrum ($\overline{V_{noise}{}^2}$) with the square of the sensitivity (S) of the SR570. The JFET noise spectrum ($\overline{V_{noise}{}^2}$) is shown in Figure 3.22 with the background noise subtracted from the measured noise.

$$\overline{V_{noise}{}^2} = \overline{V_{measured}{}^2} - \overline{V_{background}{}^2} \qquad V^2/_{Hz} \tag{3.21}$$

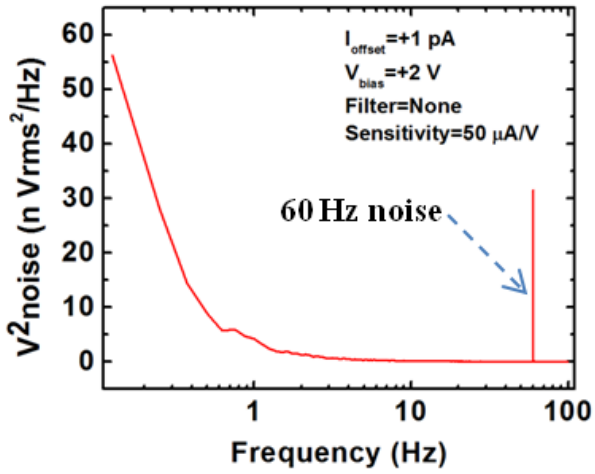


Figure 3.22. The JFET noise spectrum with the background noise subtracted from the measured noise.

Figure 3.23 is the total current noise spectrum of the JFET. The JFET exhibits a low noise performance which would make it an ideal candidate as a front-end transducer. At frequencies below 1 Hz, the noise spectrum does not contain solely *1/f* noise and thermal noise contribution, but due to temperature drift there are additional noise sources [33]. Typical 1/f noise is found between frequency ranges of 1 Hz to 10 Hz and also as shown in Figure 3.23. The corner frequency (f_c) occurs at 3.7 Hz.

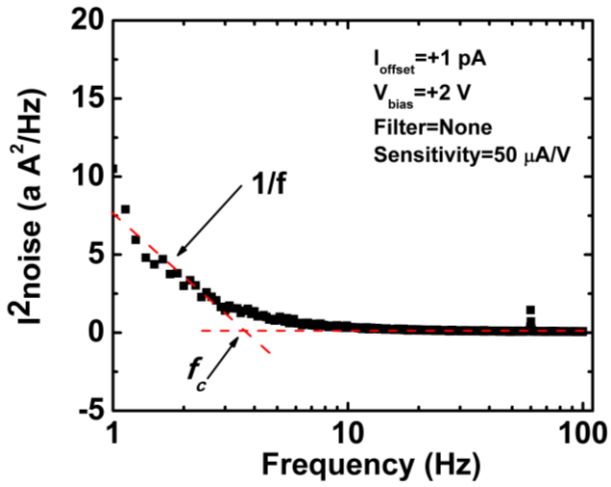


Figure 3.23. The total output current noise of the JFET when it is operating in the saturation region.

From Equation (3.22), the measured Flicker voltage noise spectrum is inversely proportional to both the length and width of the transistor and directly propositional to the channel resistance [33].

$$\frac{S_R}{R^2} = \frac{\alpha}{f}\frac{1}{nWLt} = \frac{\alpha q \mu R}{L^2 f} \tag{3.22}$$

where S_R is the spectrum noise, the channel resistance R , a dimensionless parameter α, carrier concentration n, width W, length L, the electronic charge q, mobility μ, and frequency f. Below is the measured voltage noise spectrum of commercially available JFETs (IF9030, 2N4338 and 2N4118A) that was measured by [33]. The relatively higher Flicker noise voltage of our JFET compared to the commercially available JFETs could be attributed to its higher channel resistance, shorter channel length (2 μm) and shorter width (2 μm**)** [33].

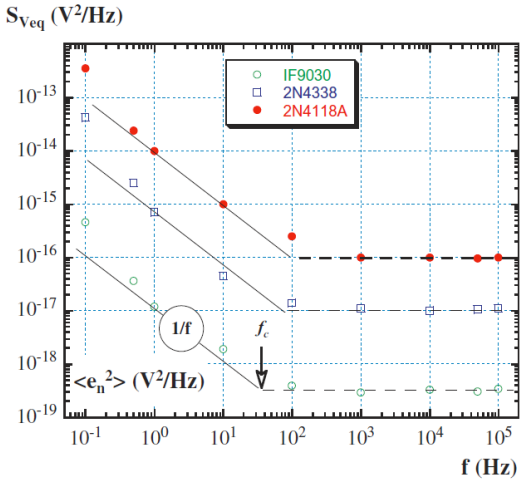


Figure 3.24. Equivalent input noise voltage of JFETs 2N4338, 2N4118A and IF9030.

Table 3.4. Noise performance of JFETs at 1 Hz

JFET	Width (μm)	Length(μm)	<e^2> (V^2/Hz)
IF9030	44,400	12	9.8×10^{-16}
2N4338	400	12	3×10^{-15}
2N4118A	28	13	1×10^{-14}
Our JFET	2	2	55×10^{-9}

3.6 *f_T of the JFET*

The front-end JFET needs to have sufficient bandwidth and gain to efficiently transduce signals. The unity current gain (f_T) of the JFET was measured by carrying out microwave measurements. The high frequency performance of the JFET is either limited by the channel transit time or the capacitance charging time [28]. If we assume electrons move at their saturation velocity, ϑ_s, through the channel length, L, the transit time is

$$\tau_t = \frac{L}{\vartheta_s} = \frac{2 \text{ x } 10^{-4}}{1 \text{ x} 10^7} = 20 \text{ ps} \tag{3.23}$$

In JFETs, the transit time is normally not the dominant limiting factor. On the other hand, the capacitance charging time involves the charging of the input capacitances of the JFET where the output current becomes a function of frequency. The maximum intrinsic cutoff frequency of the JFET is based on its device dimensions and doping and can be derived as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{q\mu_n N_d w^2}{2\pi\varepsilon_{si} L^2} = 24 \; GHz \tag{3.24}$$

where C_{gs} is the gate to source capacitance, C_{gd} is the gate to drain capacitance, q is the electronic charge, μ_n is the electron mobility, N_d is the doping of the JFET channel, w is the width of the channel, ε_{si} is the permittivity of silicon and L is the length of the channel [28].

To measure the high frequency performance of the JFET, the parasitic effects of the Network Analyzer (NWA), cables and probes were de-embedded by performing standard Short-Open-True-Load (SOTL) measurements using a CS-5 calibration substrate from GGB Industries. Figure 3.25 is an optical image of the JFET showing its Ground-Signal-Ground (GSG) pads. A bias-T was used to combine the microwave signal from the NWA (Agilent 8753 ES) and DC voltage source (HP 4142). The source terminal of the JFET was connected to ground on the HP 4142.

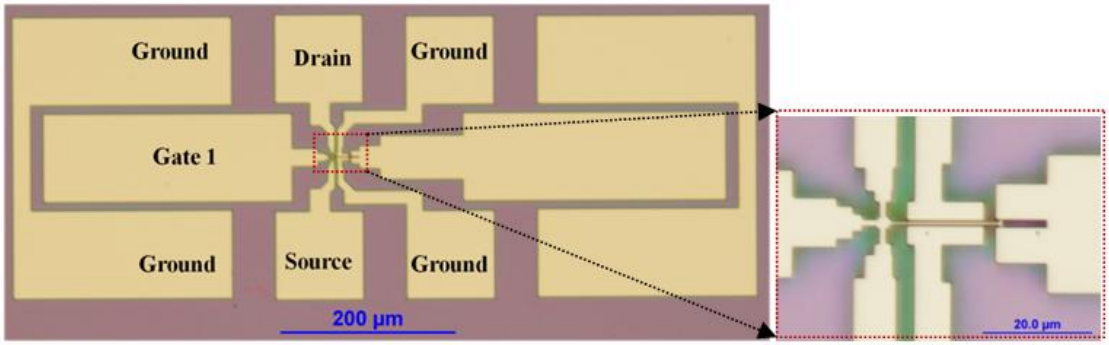


Figure 3.25. Optical image of the device showing the GSG probing pads.

The JFET was biased in saturation by applying 0 V to both the source and gate and the drain placed at 3 V. Using a 0 dBm input signal over a frequency range of 80 kHz to 5.45 GHz, the extrinsic f_T of the JFET was measured as shown in Figure 3.26. Since most MEMS devices operate in the kHz and MHz ranges, the f_T *(380 MHz)* value coupled with the low noise performance of the JFET suggest that this transistor could serve as a good front-end transistor for signal transduction. The intrinsic f_T can be measured by de-embedding the parasitic pad capacitances and resistances of the JFET [34].

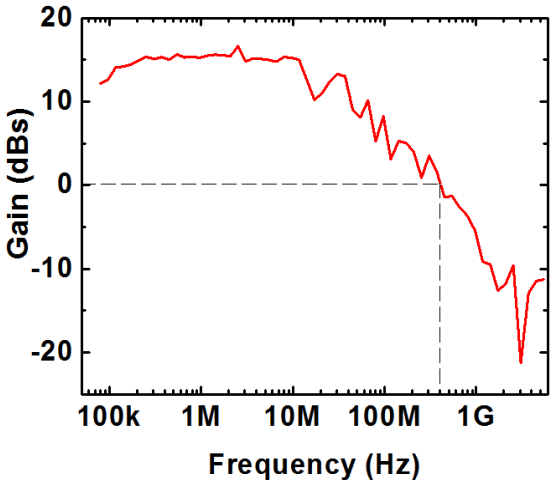


Figure 3.26. Plot of current gain (f_T) vs. frequency of the JFET.

3.7 ***Conclusions***

The chapter explored the monolithic integration of JFET with moving gates that could be NEMS or MEMS. The fabrication of the devices utilized embedded JFET junctions at cross-points of SOI beams. The DC device performance of the JFET was characterized and the JFET was used in sensing the motion of a cantilever. The cantilever could be replaced with inertial sensors, resonators, switches, for tightly coupled NEMS/MEMS and electronics. The noise performance and unity current gain of the JFET were also evaluated. Since SOI beams are common to many MEMS devices, the JFETS could be used to sense and amplify motion for increased signal and reduce effect of parasitic capacitances encountered in two-chip MEMS and NEMS.

Chapter 4

MULTIPLE TIP NANO PROBE ACTUATORS WITH INTEGRATED JFETS

4.1 *Introduction*

Two-dimensional materials such as graphene and MoS_2 hold the promise for realizing nanoscale electronics and sensors [35] [36]. However, these materials can have grain-boundaries and defects that are deep sub-nm, and thus very hard to detect with precision. Yet, for most electronic applications, it is the electrical conductivity of the surface of these devices, since they are mostly surface, that is of importance to device designers. Quantifying film conductance and surface morphology at the nanoscale level, therefore, is important to realizing high yield and performance circuits and sensors of the future.

Measuring electrical conductivity requires that probes be brought into close proximity or contact with the thin film. In order to measure the effect of defects on conductivity at deep sub-nm scale, the probes need to be separated by a few nanometers from each other to constrain the current flow around the defects. Traditional four-point probes enable measurements of conductivity on the surface with probe spacing of 1.25 mm [37], and a few nanoscale four-point probes have also been implemented [38] [39] [40]. However in these cases the probe spacing is fixed and cannot be adjusted. Nevertheless, tunability of spacing is necessary to enable the investigation of transport mechanism such as ballistic, diffusive, and localize. Ballistic transport occurs when the distance between the two probes is less than both the momentum relaxation length and the phase relaxation length. There is no scattering

and when the Fermi wavelength is comparable to the spacing, quantized conductance occurs [41]. In the case the spacing is greater than the momentum relaxation length, there is scattering and reduced transmission and this regime is diffusive. In localize transport regime, the spacing is greater than the phase relaxation length. In addition, the phase relaxation length is greater than the momentum relaxation length [41].

Atomic probing is conducted using microfabricated probes in Scanning Tunneling Microscopy (STM) or Atomic Force Microscopy (AFM) mode. In either, the probes are navigated using PZT actuators that carry out mechanical or electrical measurements, leading to a bulky actuator. AFM and STM allow conductivity measurements through the tip and the film connected to the stage; they do not allow the measurement of conductivity on the film surface.

The major problems with executing nanoscale electrical conductivity measurements are the difficulties in positioning the independent probes with precise separation and the need for an SEM or TEM for visualization. Moreover, the size of the tip handling actuator prevents the two tips from being placed within a few tenth of a nanometer apart to accomplish nanoscale conductivity measurement. Previous related efforts by other investigators include tip arrays made using the SCREAM process that led to out-of-plane tips that did not allow for co-viewing of the sample and tips in an SEM [42]. More recently other researchers have made lateral single tips from SOI wafers where the tips were used for tunneling experiments [43] [44].

This chapter will explore a multiple-tip probe system for probe-based sensing with integrated JFETs as preamplifiers. The tips are lithographically separated in the nanometer range (300 nm) and the tip separation can be further reduced to sub 50 nm gaps using electrostatic actuation. System level instrumentation was also developed

where tunneling current from the side tips was placed through a feedback loop for alignment purposes to offer precise positioning of the tips and to enable electrical characterization without the need for SEM or TEM.

4.2 *Nanogap Multi-Electrode Atom and Conductivity Prober*

The device performance of a nano-electromechanical scanning three-probe system with monolithically integrated JFETS was investigated. JFETs could be used to pre-amplify differential tunneling currents and atomic forces. To accomplish this, the JFET was integrated directly into the probes to reduce parasitics and mismatches and to provide enhanced signal transduction and low noise operation. JFETs are ideal candidate for N/MEMS signal transduction due to their low 1/f noise, high gain, low-mask count, no parasitic diodes and insensitivity to electrostatic discharge [2]. Three probes are co-fabricated, where the center probe being able to move relative to the two fixed probes using electrostatic actuators as shown in Figure 4.1. The middle probe can be displaced 200 nm in both longitudinal and lateral directions in the plane of the wafer, and this motion is sensed through a capacitively coupled JFET preamplifier.

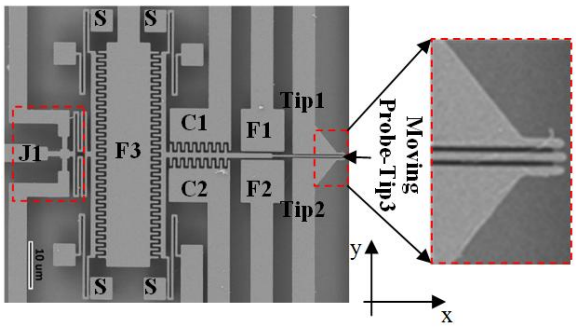


Figure 4.1. Top view of the device with the probe, JFET (J1), meander and stoppers (S). The stoppers restrict motion of the probe and JFET.

The center probe could be actuated along the y-axis using the electrostatic plate actuators F1and F2. The probe can be moved in the x-direction using the electrostatic forces between F3 and Tip 3. The JFET (J1) is suspended and capacitively connected to the actuator F3 through a meander spring. Voltage ramps applied to electrode F3, induces electrostatic force of attraction of the middle tip as well as the embedded JFET which is shown in Figure 4.2 and Figure 4.3.

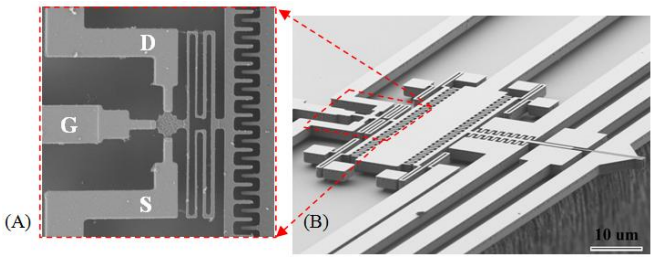


Figure 4.2. (A) SEM micrograph of the suspended JFET with meander (B) Side view SEM micrograph of device.

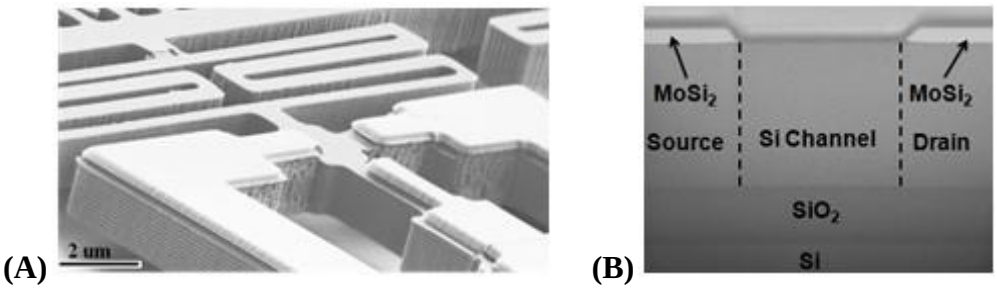


Figure 4.3. (A) SEM micrograph of the suspended JFET with $MoSi_2$ source, drain and gate metallization. (B) SEM cross-sectional view of the region between the source and drain of the JFET. Focused Ion-Beam (FIB) was used to cut the beam to obtain the cross sectional view.

The probe beam position is coupled to electrodes through electrostatic energy sustaining gaps, and can be sensed by the JFETs in two ways. First, the electrostatic force on the JFET induces a strain in the channel which tends to enhance the channel mobility of the JFET [45] [46]. Second, the applied electrostatic potential generates a floating potential on the spring of the JFET, which modulates the channel current. The change in the drain current of the JFET directly corresponds to the motion of the middle probe.

4.2.1 JFET Current Contribution due to Floating Potential

The JFET channel was lightly n doped (~$3.11x10^{15}cm^{-3}$), the gates were p^+ doped (~$10^{20}cm^{-3}$), and the source and drain were n^+ doped (~$10^{20}cm^{-3}$). Figure 4.4 is a schematic of the JFET that depicts not only the JFET, but also the connection to the serpentine springs that connect one of the gates to the electrostatic actuator F3. The sense 1 part of the JFET is biased in saturation by reverse biasing Gate 1. The saturation current is [28].

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{4.1}$$

where I_{DSS} is the saturation current when $V_{GS} = 0$ and V_P is the pinch-off voltage. When negative DC voltage ramps were applied to F3, the JFET meander extends as the probe recesses in the x-direction. Since the JFET meander-spring is electrically floating, the applied voltage on F3 induces a negative floating potential on the spring.

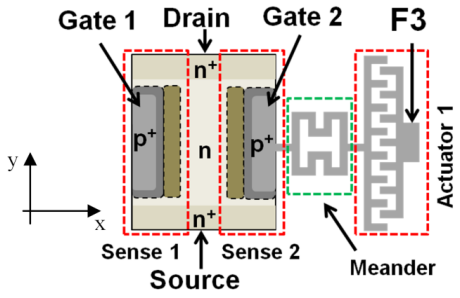


Figure 4.4. Schematic of the actuation and sensing of displacement by the JFET.

The potential reverse biases the JFET Gate 2 and acts to further pinch-off the channel. Thus the floating potential modulates the channel conductance allowing the new saturation current in the JFET to be written as

$$I_{DD} = I_{DSS}\left(1 - \frac{(V_{GS} + \Delta V_{FG})}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\left[1 - \frac{\Delta V_{FG}}{V_P - V_{GS}}\right]^2 \tag{4.2}$$

$$I_{DD} = I_D\left[1 - \frac{\Delta V_{FG}}{V_P - V_{GS}}\right]^2 \tag{4.3}$$

where ΔV_{FG} is the floating potential. If $V_P - V_{GS} > \Delta V_{FG}$, the drain current will decrease as the floating potential is increased.

4.2.2 Current Contribution due to Strain

When a voltage is applied to F3, the extension of the meander spring pulls on the Gate 2, inducing strain at the P^+N-junction between the channel and the meander [47]. The strain in the depletion region generates tensile stress in the channel of the JFET.

The effect of the tensile stress is to enhance the channel mobility [45]. In saturation, the drain current is [28].

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{4.4}$$

$$I_{DSS} = \frac{\mu_n (qN_d)^2 tW^3}{6\varepsilon_o \varepsilon_{si} L}\left\{1 - 3\left(\frac{V_{bi}}{V_{PO}}\right)\left(1 - \frac{2}{3}\sqrt{\frac{V_{bi}}{V_{PO}}}\right)\right\} \tag{4.5}$$

where W is the width, t is the JFET thickness, and L is the length. If the small change in mobility is represented by Δμ, the new current is

$$I'_{DD} = (\mu + \Delta\mu)\frac{(qN_d)^2 tW^3}{6\varepsilon_o \varepsilon_{si} L}\left\{1 - 3\left(\frac{V_{bi}}{V_{PO}}\right)\left(1 - \frac{2}{3}\sqrt{\frac{V_{bi}}{V_{PO}}}\right)\right\}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{4.6}$$

$$I'_{DD} = I_D\left[1 + \frac{\Delta\mu}{\mu}\right] \tag{4.7}$$

From Equation (4.7), the change in mobility increases the drain current in the JFET. In contrast, the increasing floating potential tries to pinch-off the channel and decrease the current. However, due to the small piezoresistive coefficients, the floating potential effect on the channel conductance is dominant.

4.2.3 Mechanical Actuation Simulation

Since the JFET responds to the movement of the probe, the change in drain current can be used to characterize this movement. Figure 4.5 illustrates the COMSOL® simulation of the structural and electrostatic behavior of the device.

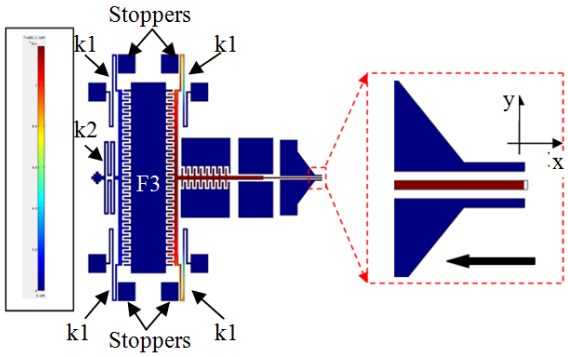


Figure 4.5. COMSOL® simulation of displacement of probe tip and JFET meander spring (k2). The probe tip can move in both the x and y directions.

The total effective spring constant (2k1+ k2) for the meander springs attached to the JFET was designed to be stiffer than those connected to the moving probe (2k1). Figure 4.6 illustrates the relationship between the x-movement of the probe and the JFET-meander spring (k2) as voltage is applied to F3. Stoppers are implemented to prevent the extreme crushing of the probe and JFET during pull-in. The moving tip is 100 nm longer than the stationary tips. The probe and JFET meander move in opposite directions when voltage is applied to electrode F3.

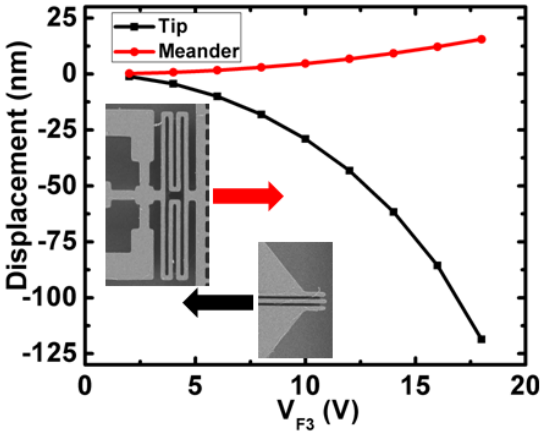


Figure 4.6. COMSOL® simulation results for the model in Figure 4.5. Actuation voltage of 18 V at F3 generates a displacement of 120 nm at the probe tip and 15.5 nm at the transistor meander. The meander and probe move in opposite directions.

4.3 *Prober Fabrication*

The fabrication of the devices follows the procedure in [48]. The devices were fabricated on 2 μm thick n-type SOI wafers with resistivity of 2 Ω-cm. The source and drain were doped using PH-1025 solid source diffusion targets while the gates were doped with BN-1250 solid source diffusion targets. The doped wafer was furnace annealed to drive-in the dopants. $MoSi_2$ was used for the metallization and the devices were etched by DRIE. Release of the devices was carried out in buffered oxide etch (BOE 6:1) and dried using critical point drying to prevent stiction.

4.4 *Prober Characterization*

4.4.1 Resonance Frequency Measurement

The device could be used in both AFM and STM applications. In these applications, the middle tip can be excited in resonance and scanned along the sample [49]. Using the setup in Figure 4.7, the resonance frequency of the middle tip was measured in a vacuum at 1.9×10^{-3} mbar.

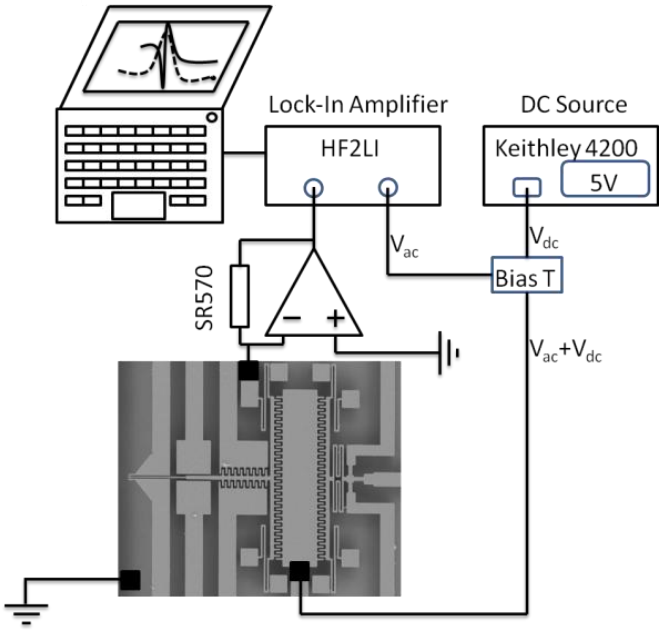


Figure 4.7. Electrical setup for resonance frequency measurement of the middle tip.

With the SOI substrate grounded, the Lock-In amplifier from Zurich Instruments (HF2LI), was used to create an AC sweep that was combined with DC voltage through a bias-tee and launched on electrode F3. The displacement current through the middle

tip was fed into a SR570 low noise transimpedance amplifier (TIA) with sensitivity set to 5 nA/V. The output of the TIA was fed back into the lock-in amplifier for frequency domain analysis. Figure 4.8 displays the measured fundamental resonance frequency of the middle tip.

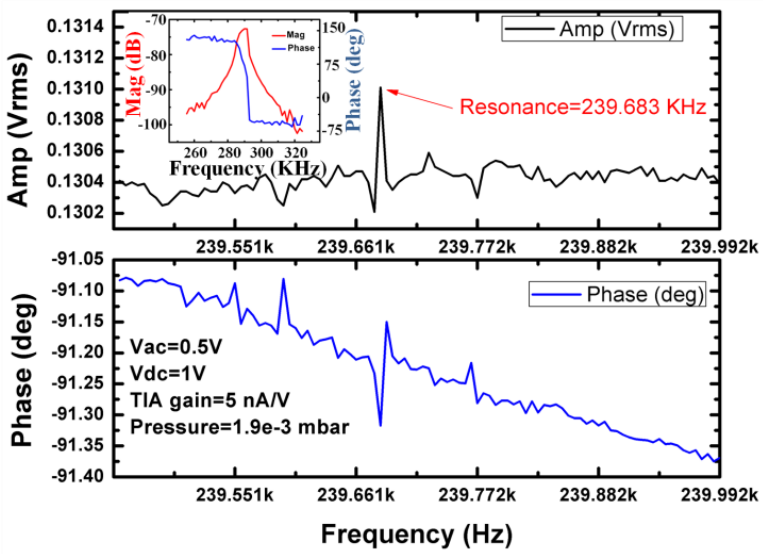


Figure 4.8. Resonance frequency measurement of the moving tip in vacuum at a pressure of 1.9×10^{-3} mbar.

The resonance frequency of the tip was measured to be 239.7 kHz as illustrated in Figure 4.8. The inset in Figure 4.8 is the optical measurement of the resonance frequency which was 291.5 kHz. The calculated resonance frequency of 310 kHz was in agreement to the optically measured results. Appendix 6.4 shows the Matlab® code used to calculate the resonance frequency. The spring constant of the middle tip was 2.56 N/m, indicating that sufficient stiffness was obtained for precision placement and contact force without buckling the tip.

Table 4.1. Parameters used to calculate the resonance frequency of the probe tip.

Parameter	Value	Unit
Length of probe tip	72	μm
Width of probe tip	1	μm
Thickness of probe tip	2	μm
Width of meander spring	300	nm
Effective Young's modulus	194	GPa
Effective spring constant	2.56	N/m
Mass of probe tip	6.71×10^{-13}	Kg
Resonance frequency	310	kHZ

The Brownian noise displacement was evaluated using Equations (4.8):

$$\bar{x} = \sqrt{\frac{4k_B T b}{k^2}\left\{\frac{1}{\left[1-\left(\frac{\omega}{\omega_O}\right)^2\right]^2 + \frac{\omega^2}{(Q\omega_O)^2}}\right\}} \quad {}^{m}/_{\sqrt{Hz}} \tag{4.8}$$

where k_B is the Boltzmann constant (1.38066×10^{-23} J/K), T is the temperature (300 K), b is the damping coefficient (1.31×10^{-7} N s/m), k is the spring constant (2.56 N/m), ω_O is the measured resonance frequency (1.95×10^{6} rad/s) and Q is the quality factor (~10). At resonance, the Brownian noise force is expected to be 46.6×10^{-15} $N/\sqrt{Hz}$ and the mean noise displacement 1.82×10^{-13} $m/\sqrt{Hz}$. Assuming the bandwidth of measurement of 100 Hz, the displacement of the probe by Brownian noise will be 1.8 picometers. The Brownian noise displacement on the tip is two orders of magnitude lower than the inter-atomic distance of 2D thin films providing sufficient SNR for lateral measurement.

4.4.2 Inter-Tip Gap Modulation

The gap between the middle tip and either of the side tips can be reduced by applying voltage ramps to either electrode F1 or F2. Also applying voltages to Tip 1 and Tip 2 laterally would deflect the middle tip. Figure 4.9 shows the in-situ SEM actuation of the middle tip with voltages applied to the side tips while the middle tip is grounded. By modulating the gap, transport phenomena such as transitions from localized, diffusive and ballistic transport can be investigated [50].

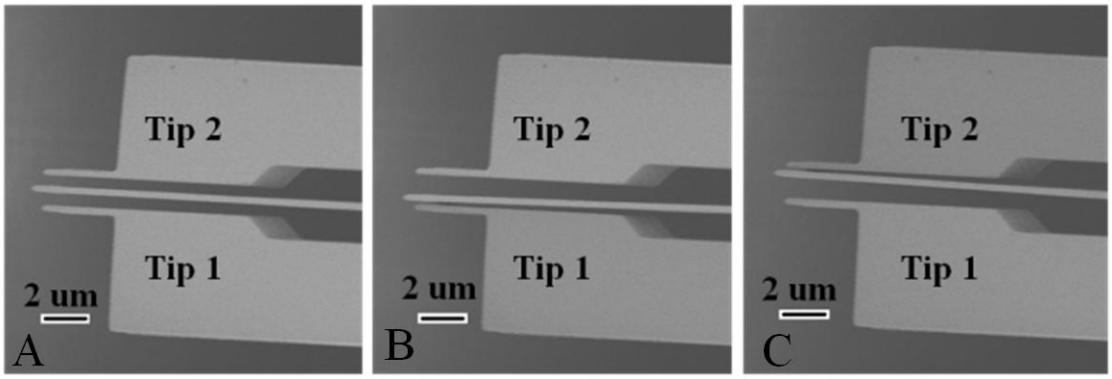


Figure 4.9. (A) All tips are grounded. (B) +3.5 V applied to tip 1. (C) +3.5 V applied to tip 2.

The probe motion was confirmed by applying a ramp voltage to the F3 electrode. Figure 4.10 shows the measured displacement current between F3 and Tip3. With a ramp voltage of different peak voltages (x-axis on Figure 4.10), and with a ramp rate of 0.8 V/s, we measured the displacement current due to tip motion. This displacement current could be used to measure tip-motion independently to calibrate the JFET transducer.

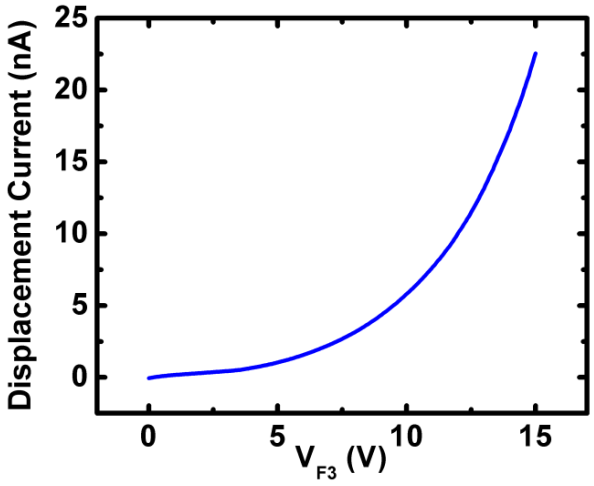


Figure 4.10. Sweeping the voltage applied at F3 in ramps, the displacement current due to motion is measured between the moving probe and F3.

4.4.3 IV Characteristics of the JFET

The IV measurements of the devices were conducted in air using a Keithley 4200 parametric analyzer. Figure 4.11 shows the plot of the drain current versus drain-source voltages for the JFET. The transconductance and transconductance parameter (β) were measured to be 0.2 μS and 4.1 nA/V^2 respectively. Table 4.2 illustrates the device parameters.

Table 4.2. Device parameters of prober

Parameter	Symbol	Value
Spring Constant for Tip 3 meanders	$2k1$	2.56 N/m
Pinch-off voltage	V_P	-25 V
Transconductance at V_{DS}=10 V and I_{DSS}	g_m	0.2 μS
Transconductance parameter	β	4.1 nA/V^2
JFET channel width	W	2 μm

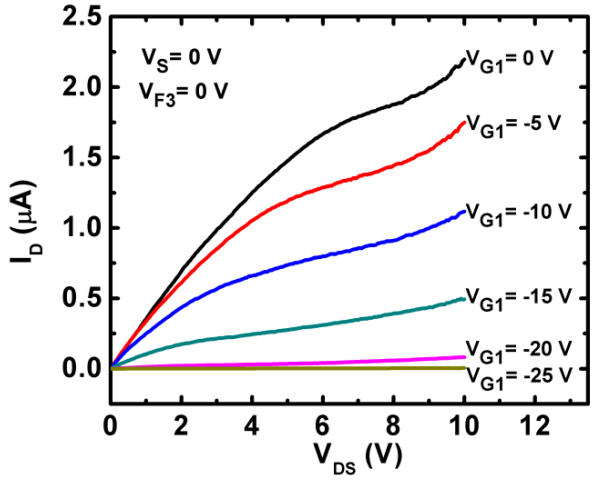


Figure 4.11. Measured I_{DS} vs. V_{DS} output curves for the JFET. V_{G2} was floating, while V_{G1} was varied.

The pinch-off voltage which is given by Equation (4.9), was measured to be -25 V at V_{DS}=10 V as illustrated in Figure 4.12.

$$V_p = V_{bi} - V_{po} \tag{4.9}$$

$$V_{po} = \frac{qW^2 N_d}{2\varepsilon_o \varepsilon_{si}} \tag{4.10}$$

where V_{bi} is the built-in potential, V_{po} is the internal pinch-off voltage, W is the channel width, N_d is the doping concentration of the channel and ε_{si} is the permittivity of silicon.

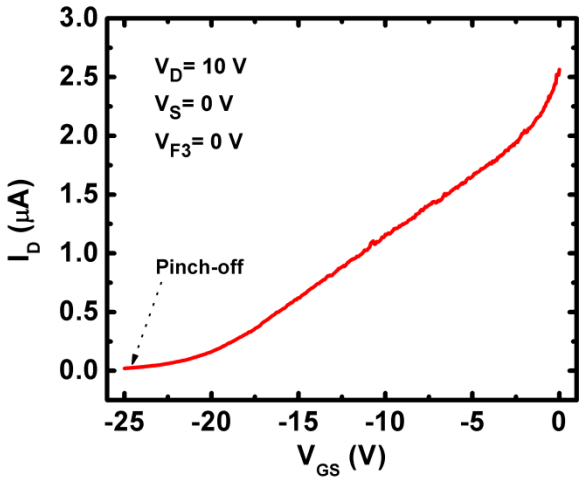


Figure 4.12. Transfer curve for the JFET biased at V_{DS}=10 V. The I_{on}/I_{off} ratio was 126.

From Equation (4.9) and (4.10), it can be seen that the pinch off voltage is directly proportional to the doping concentration. Thus decreasing the pinch-off voltage of the device by lightly doping the channel will decrease both the drive current and transconductance. The tradeoff between pinch-off voltage and current characteristics illustrates the design issues for optimizing operation with electrostatic actuation with high operating voltages.

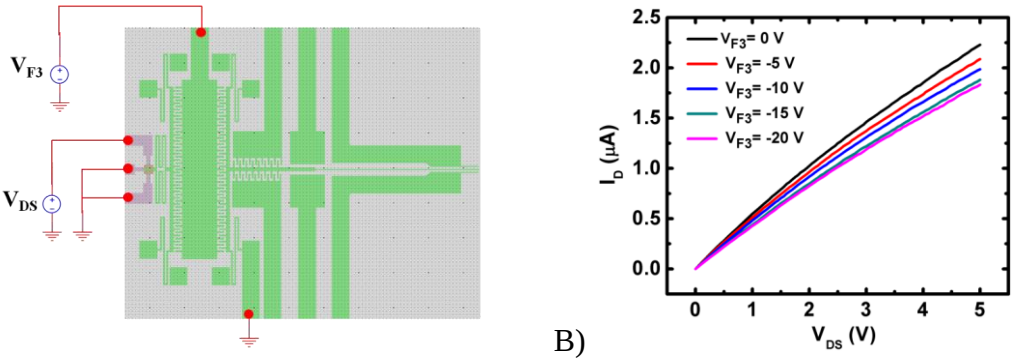
4.4.4 Sensing the Motion of the Moving Probe through the JFET

In Scanning Tunneling Microscopy (STM), the tunneling current is a function of the distance between the tip and the sample. The tunneling current is derived as

$$I = V_a\, K(z) e^{-2\sqrt{2\varphi} z} \tag{4.11}$$

where V_a is the applied voltage, z is the tip-sample distance, $K(z)$ is a function z and φ is the mean barrier height [51]. In order to maintain a constant current for imaging atomic lattices, the z position needs to be monitored and adjusted accordingly. The embedded JFET could be used to sense the tip position and provide a feedback signal to adjust the tip position accordingly.

To sense the motion of the probe, the Gate 1 and source of the JFET were placed at ground and different negative voltages applied to F3. The drain current modulation was monitored as shown in the output curves in Figure 4.13. The applied voltage induced strain and mirrored a floating potential onto the JFET that modulated the channel conductance to a higher degree. For V_{F3}=-20 V, the change in current was 0.4 μA from V_{F3}=0V, indicating an effective potential of -2.3 V at Gate 2 of the JFET.



A) B)

Figure 4.13. (A) The biasing schematic for sensing the motion of the probe. (B) Both the probe and transistor moved as an actuation voltage was applied and the JFET was able to sense the motion of the probe. The induced floating potential and strain on the JFET modulated the drain current. For these experiments V_{G1} and source terminals were set at 0 volts.

4.4.5 Atomic Imaging

The fabrication of the multiple-tip prober device was described in Chapter 3 [48]. To use the tips for atomic imaging, Focused Ion Beam (FIB) was used to sharpen the tips from 300 nm to sub 50 nm radii. Figure 4.14 (A) and (B) illustrate the top and side views of the middle tip after FIB etching.

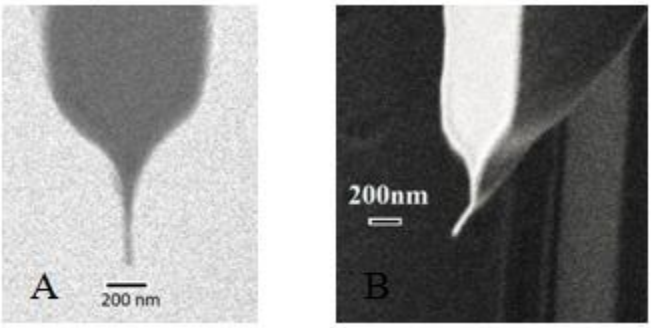


Figure 4.14. (A) Top view of the sharpened tip to sub 50 nm radius. (B) Side-view of the sharpened tip.

To investigate the atomic arrangement of Highly Ordered Pyrolytic Graphite (HOPG), devices were fabricated without the two stationary tips. The middle tip was sharpened with FIB and wire-bonded to a PCB board as shown in Figure 4.15. The board together with the NEMS-prober were inserted into the JEOL 4210 SPM system. With the middle tip grounded and 350 mV applied to the HOPG sample, the sample was brought into close proximity with the tip until 500 pA of current was sensed. This was followed by a 5 nm by 5 nm scan in ambient air. Figure 4.16 (A) and (B) show the scan results obtained using a commercial Pt-Ir tip and NEMS-prober, respectively.

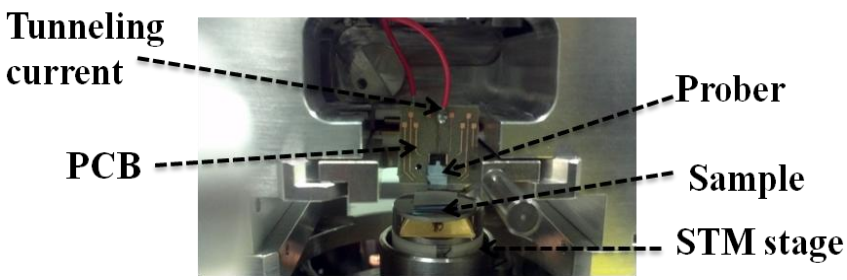


Figure 4.15. Assembled NEMS-prober on PCB board that is finally mounted in JEOL SPM system. The HOPG sample sits below the NEMS-prober.

The inter-atomic distance of HOPG along the same plane for the commercial tip and NEMS-prober scans was measured to be 3.54Å and 3.32 Å respectively which was closely in agreement as shown in the plots of Figure 4.16 (A) and (B). As it can be seen, since the commercial tip has an atomic sharp radius, it was able to resolve the carbon lattice better than the NEMS-prober which had a sub-50 nm atomic radius.

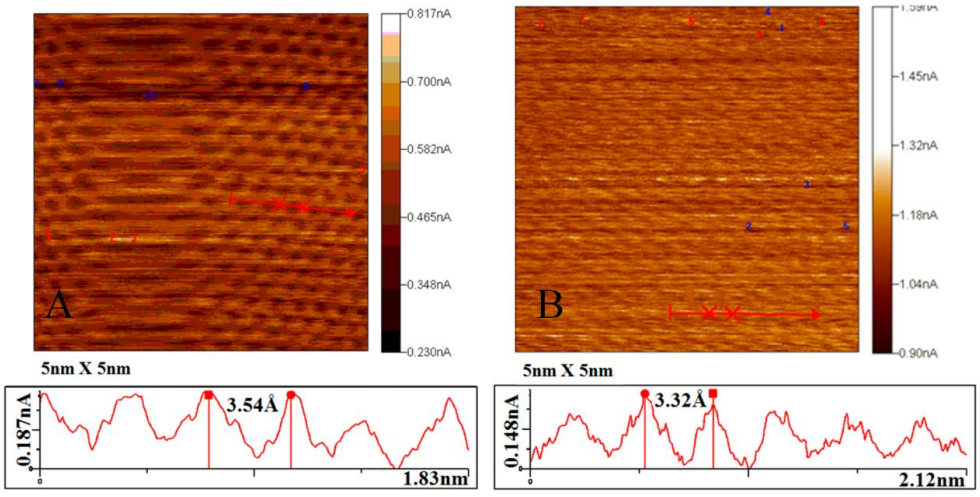


Figure 4.16. (A) Using a commercial Pt-Ir tip to scan HOPG sample. (B) The NEMS-prober is used to scan HOPG.

4.4.6 Conductance Measurement

The NEMS-prober and HOPG sample were mounted onto a Zyvex® SEM manipulator as shown in Figure 4.17. The navigation of the prober towards the sample was viewed in real time in the SEM to avoid overdrive of the prober into the sample since it had the tendency to break the tips. Once in soft contact, a voltage ramp was applied to the middle tip and current flow was recorded from the side tips, providing differential conductance measurements.

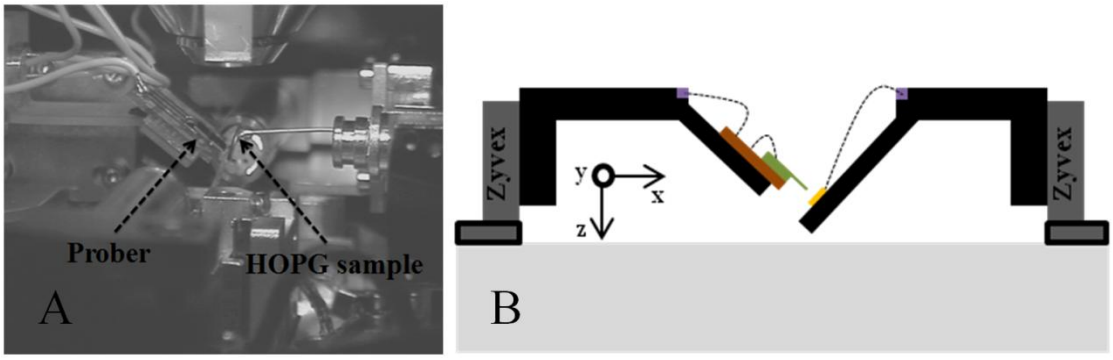


Figure 4.17. (A) The prober and HOPG sample were mounted in SEM for in-situ conductance analysis of HOPG. (B) Schematic of the testing assembly in the SEM using the Zyvex® nanopositioners.

Figure 4.18 and Figure 4.19 show the soft contact and current-voltage characteristics of the sample respectively. The extracted resistance between the middle tip and the right tip was 0.4 Ω/nm^2. It was also observed that during hard contact that, the two outermost tips were capable of bending about 30 degrees without breaking while the middle tip retracted.

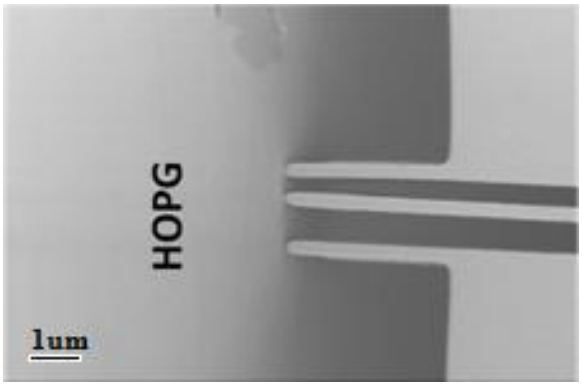


Figure 4.18. SEM micrograph of the tips in soft contact with HOPG sample.

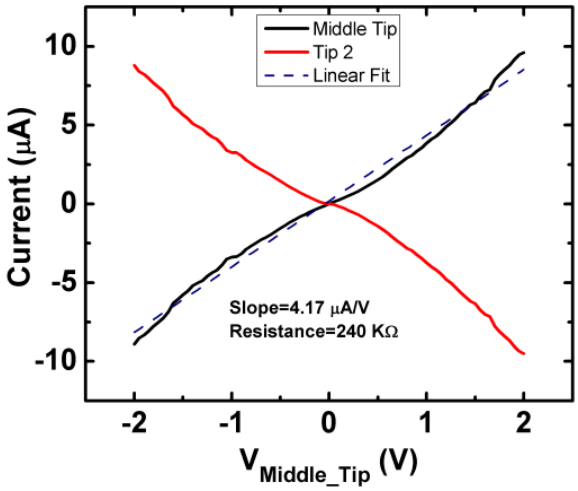


Figure 4.19. The conductance characteristics of HOPG sample. The dashed line is a linear fit to the middle tip current and the resistance of the HOPG sheet is determined from the inverse slope of this line.

4.5 *Conclusions*

Active JFETs, electrostatic sensors and actuators have been integrated into a three-probe scanning probe device where two probes are fixed and the third is movable. As

the probe moves, the floating potential the JFET acquires further reverse biases the JFET. The change in the depletion width modulates the channel conductance of the JFET, enabling the direct pre-amplification of probe motion. Also, the stretching out of the meander springs induces a strain in the channel of the JFET. Although the strain and floating potential effects act in opposition, the floating potential is the dominant mechanism in this device. The NEMS multiple tip prober was used for atomic imaging and conductance measurements. The prober has an integrated JFET for motion sensing and actuators for nanogap modulation. Besides atomic scanning, the probe could also be used to probe electrical properties of thin films.

Chapter 5

5.1 *Scanning Probe System (SPS)*

Thus far, atomic imaging and electrical probing have been carried out using different equipment. In response, this section of the thesis will focus on current efforts toward developing a Scanning Probe System that can accomplish both atomic imaging and nanoscale electrical probing without the use of an SEM. The motivation for such a system stems from its theoretical capacity (based on spatial measurements of trans-conductance between tips) to image the single electron Green function, to determine the scattering matrix at impurity atoms, and to image the inelastic processes limiting electronic mean free path in modern, complex electronic matter materials. Hence, the ultimate goal is to unravel the nature of electronic excitations in unconventional materials. Although double-tip STM systems have been proposed for more than a decade as a next generation tool for basic research into complex electronic matter, engineering challenges have prevented their implementation.

Today, the single tip STM continues to have a profound impact on the investigation of structural and electronic properties of thin films, however, it is limited to static measurements such as the local density of states and near sample surfaces [50]. As stated by Q. Niu et. al., the single tip STM cannot be used to determine the energy dispersion in band structures because it lacks the k-resolution [50]. Because of this, the ability to probe the single-electron Green function will not only revolutionize material science, but will also allow for a deeper understanding of how electrons transport and interact with their surroundings.

To fully investigate the single electron Green function of a sample surface, a minimum of two tips are required. Electrons are tunneled from tip 1 and are collected by tip 2. The measured transconductance or Green function contains information about the local density of states, tip sample coupling, transport mechanisms, scattering phase shifts and inelastic free mean paths of electrons [50][52].

This section of the thesis will explore the development of a multiple tip scanning probe microscope for use in imaging and performance of nanoscale transconductance measurements to probe defects and the single electron Green function of thin films. The full microscope will consist of laserless AFM, multiple-tip STM and Tip Enhanced Raman Spectroscopy (TERS) modules. Since the measured transconductance is strongly influenced by grain boundaries and defects in the thin film, the AFM/STM module will be used to acquire the atomic images that will in turn shed light onto the lattice arrangement and grain boundary locations. The topographical image will then be used as feedback for positioning the side tips for the performance of transconductance measurements.

5.1.1 Overview of the Scanning Probe System

The operation of the SPS involves recording the tunneling current from the side tips of the NEMS prober and using the current measurement as feedback to align the tips perpendicularly to the sample surface. Once the tips are aligned, conductance or resistance map measurements of thin films may be carried out. Atomic imaging of thin film is left for future work.

5.1.2 Hardware

The hardware consists of a header that hosts decoupling capacitors for the power rails and a transimpedance amplifier to convert the tunneling current into voltage. The header is mounted onto a rotating stage and a second XY stage translates the header. The nanoprober is wirebonded to a PCB and mounted into the SPS as shown in Figure 5.1. To perform a transconductance measurement, the sample stage is electrically floated by connecting the stage to a relay. When the relay is closed, sample bias is applied to initiate STM measurement and once the relay is opened, the stage becomes electrically floated for transconductance measurements.

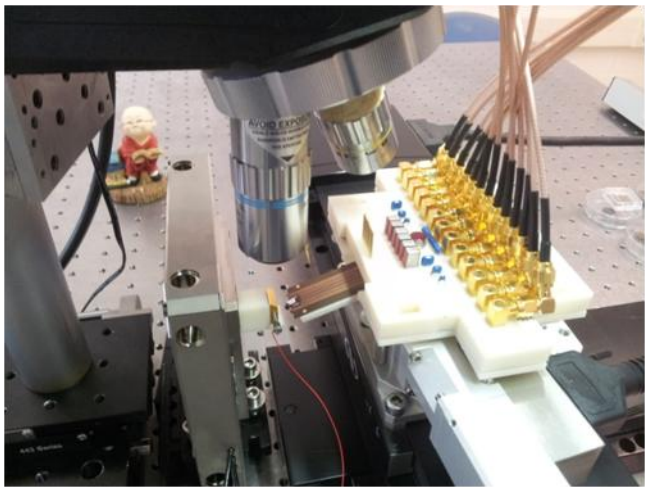


Figure 5.1. Hardware of the SPS.

5.1.3 Operation of SPS

The sample-tip approach mechanism used in the SPS is similar to that used in the conventional STM operation. The major difference is the alignment routine that is

done in the SPS to align the side tips of the nanoprober to the sample. The thin film is placed on an XYZ PZT stage. The side tips of the nanoprober are grounded and a voltage is applied to the thin film. As the sample approaches the tips, electrons tunnel from the tip to the sample or vice versa. The tunneling current is converted into a tunneling voltage by a transimpedance amplifier (TIA). The output of the TIA is connected to a Data Acquisition (DAQ) system and sampled at a rate of 2 kHz. The sampled voltages undergo signal processing by first being filtered with a bandstop filter that removes 60 Hz noise and then their mean voltage value is evaluated. The mean voltage values from Tip1 and Tip2 are then put into the "control box" which implements the state machine illustrated in Table 5.1.

Table 5.1. State machine for the alignment of the side tips

Tip 1	Tip 2	Output	Instruction
0	0	No tunneling	Move Z until tunneling
0	1	Tunneling from Tip 2	Retract Z and rotate CW, lateral compensation
1	0	Tunneling from Tip 1	Retract Z and rotate CCW, lateral compensation
1	1	Tunneling from Both tips	Tips are aligned, perform measurements

With 1 V applied to the sample, a tunneling current of about 1 nA is expected. This tunneling current is converted by the 1 GΩ feedback resistor in the TIA to generate an output voltage of 1 V. A tolerance of 0.1 V is set such that if the voltage is 10% away from the setpoint (1 V), the tip is considered to be in the tunneling regime. Relying on Table 5.1, when there is no tunneling current sensed, the Z actuator of the

PZT sample stage moves 50 nm where the DAQ then samples the tunneling current from both tips. If there is no tunneling current, the PZT stage continues to move 50 nm until tunneling current is sensed from either tip or both tips. If current is sensed at either tip, the Z actuator retracts and the header rotates clockwise or counterclockwise away from the tip that generated the tunneling current.

The rotation places the tips at different locations relative to their original position on the sample. XY translation of the header is carried out to bring the tips back to their original location. The Z movement, rotation and lateral compensation is carried out until equivalent current is sensed at both tips, indicating a successful tip-alignment. To have good sample-tip contact, the Z actuator is moved-in an extra 50 nm before electrical characterization is carried out. Once it is in hard contact, the sample bias is turned off and the stage is electrically floated. Current-Voltage (IV) measurements are conducted by grounding tip 2 and applying voltage ramps to tip 1.

5.1.4 Software

The software that controls the SPS was written in LabView®. Figure 5.2 and Figure 5.3 are images of the input and output panels of the software. The various sections are explained below:

A: Field allows a user to specify the scan area as well as the number of data points.

B: The section controls the Z-movement of the sample stage. The tunneling voltage and the set points must be specified. During each sampling cycle, if there is no tunneling current, the user can modify the displacement of the sample stage in the Z increment slot. To compensate for tip misalignment, the holder rotates a specified amount when tunneling current is sensed from either tip.

C: The sample bias is applied for alignment and STM mode of operation. Once the tips are fully aligned, voltage sweeps can be carried out.

D: Slot allows a user to monitor the sample current.

E: Frame displays the Z-movement of the sample stage, the rotation of the header and the tunneling voltages.

F: Frame promulgates graphical images of the tunneling voltages.

G: PID control feedback for the response of the PZT sample stage.

H: Start button.

I: Graphical representation of the resistance map.

J: Visual display and data for the current and voltage measurement.

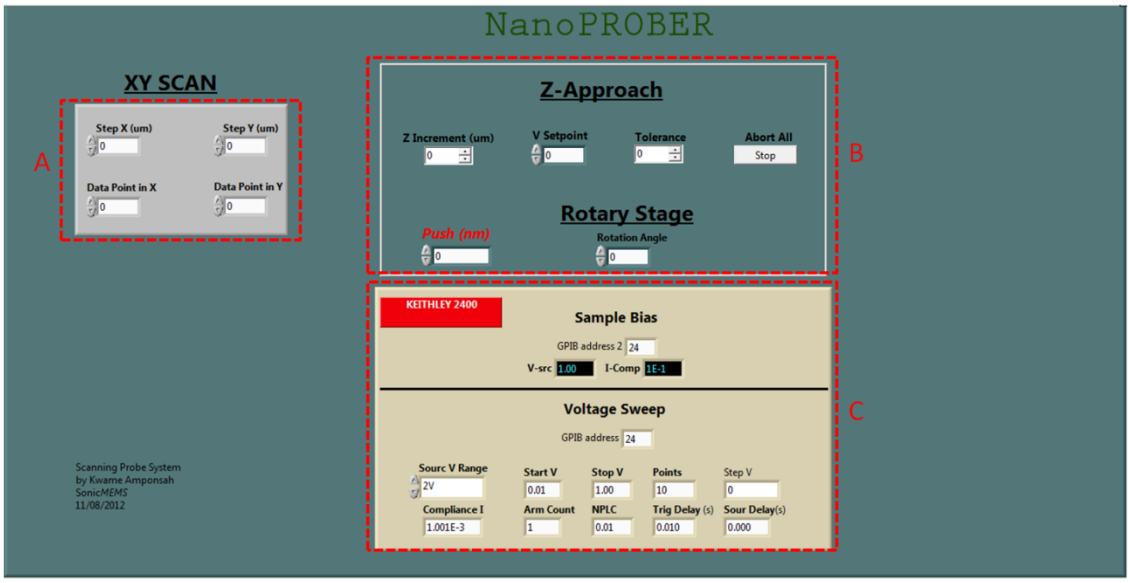


Figure 5.2. Input panel of the GUI.

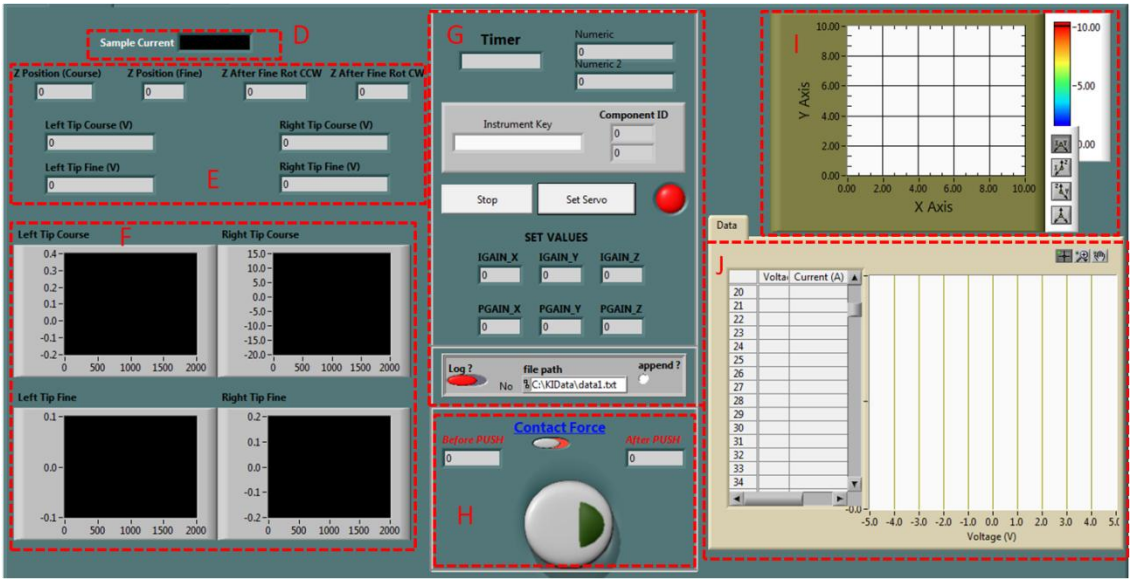


Figure 5.3. Output panel of the GUI.

5.1.5 Results

The SPS was used to perform a resistance map of a HOPG sample using $MoSi_2$ based tips as shown in Figure 5.4. The sample bias was 1 V and the voltage sweep was from -2 V to +2 V. The measured results are shown in Figure 5.5 and Figure 5.6.

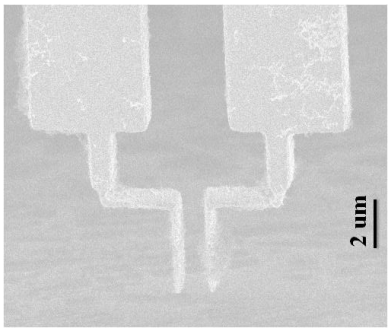


Figure 5.4. Spring compliant double-tip for resistance mapping HOPG film.

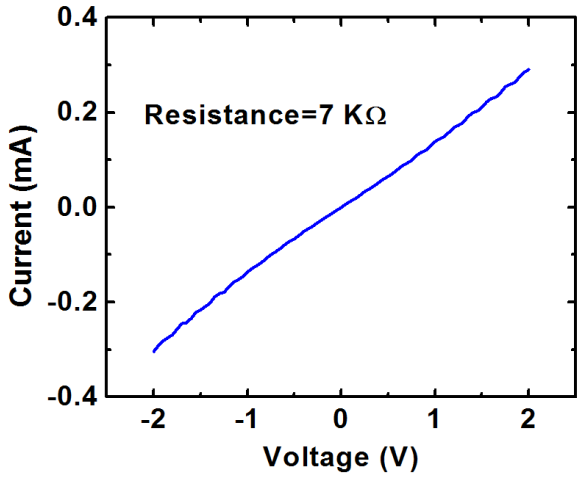


Figure 5.5. Current-voltage characteristic of a continuous region of HOPG.

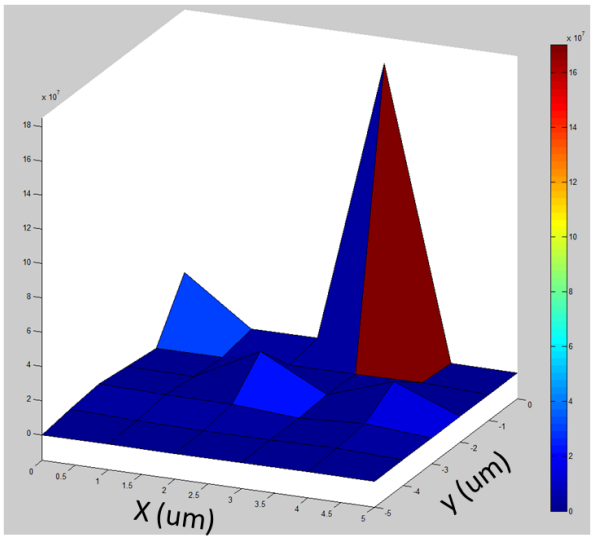


Figure 5.6. A 5µm by 5µm resistance map of HOPG film. The measured resistance values range from 7 kΩ for continuous regions and 170 MΩ for non-continuous regions.

5.2 ***Future Work***

Laserless AFM and Reconfigurable 3D probing

With the semiconductor industry continuously scaling transistors to sub-22 nm node and beyond, it has become increasingly difficult to probe 3D structures such as FinFETs. Due to the physical dimensions of the transistors, SEMs are required to view the location and to assist the nanopositioners in probing. This results in a long cycle time for testing the FinFETs due to the loading of the wafer into the SEM and the need to pump down to a high vacuum. The measurement results recorded in vacuum could substantially differ from those taken in ambient air. Also, due to the intrinsic overdrive in the nanopositioners, it will be tough to bring two probes very close to each other without crushing them. Because of this, we propose to use the NEMS prober for imaging the FinFET as well as electrically probing the source, gate and drain terminals.

Most traditional AFMs excite the cantilever tip with a piezoelectric actuator and then the vibration of the cantilever is tracked by an incidence laser and photodetectors. But, laser systems are bulky and expensive. In contrast, with the NEMS prober, the middle tip can be excited in resonance using the capacitive combdrive actuators and the changes in resonance frequency, amplitude and phase, can be electrically sensed [49]. This form of electrical-in and electrical-out transduction mechanism, which eliminates the use of lasers, allows the AFM system to be compact and cost effective. Moreover, the image acquired from the AFM scans could be used in a feedback loop to position the three tips for the 3D structure probing.

5.3 ***Conclusions***

A *Sonic*MEMS lab built Scanning Probe System was developed which uses the multiple tip prober to perform resistance map of HOPG film. The results presented lay the experimental foundation for sequential scanning and probing of nanoscale activities using a multiple-tip prober without the need for SEM or TEM. The system is being developed to a stage where various scanning probe modules such as laserless AFM, Tip Enhanced Raman Spectroscopy (TERS) and multiple-tip STM will be tightly integrated into a compact instrument.

Chapter 6 Appendix

6.1 *Energy Consumed in the Switching Process of a NEMS Switch*

```
%%%%%%%%%%%%%%%%%%%%Energy Consumption in Nanoswitch%%%%%%%%%%%%%
lb=25e-6 %length of the cantilever
tb=250e-9 % thickness of cantilever
wb=2e-6 %width of cantilever

Ib=(wb*tb^3)/12 %moment of inertia
EE=180e9 %Young's Modulus
vv=0.27 %Poisson ratio
E=EE/(1-vv^2) %Effective Young's modulus
rho=2330 %Density of Silicon
m=rho*lb*wb*tb % mass of cantilever
e0 = 8.85*10^-12 %permittivity

%%%%%%%%%%%%%%%%%%%%%%Prebias energy at Gate 1%%%%%%%%%%%%%%%%
l1=15e-6 %length of actuation region
w1=2e-6 % width of actuation region
A1=l1*w1 %Actuation area
g01=900e-9 %Initial gap at gate 1
x1=150e-9 % Displacement at gate 1
k1=24*E*Ib/(l1^3+6*l1*lb-4*(l1^2)*lb) %Spring constant by gate 1 actuation
v1= 54 %Applied voltage at gate 1
```

```
Energy_g1=((e0*A1)/(2*(g01-x1)))*(x1/g01)*v1^2+(0.5*k1*x1^2)  %Consumed energy


%%%%%%%%%%%%%%%%%%%%%%Energy consumed at Gate 2%%%%%%%%%% %%%%%%
l2=7e-6 %length of actuation region
w2=2e-6 % width of actuation region
A2=l2*w2 %Actuation area
g02=100e-9 %gap at gate 2
x2=20e-9 % Displacement at gate 2
v2= 300e-6 %Applied voltage at gate 2
k2=2*E*w2*((tb/lb)^3)*((1-((lb-l2)/lb))/(3-(4*((lb-l2)/lb)^3)+((lb-l2)/lb)^4))%Spring constant by gate2
Energy_g2=((e0*A2)/(2*(g02-x2)))*(x2/g02)*v2^2+(0.5*k2*x2^2) %Consumed energy


%%%%%%%%%%%%%%%%Effect of Gate 1 actuation on Gate 2%%%%%%%%%%%%%%%%%%
l1=15e-6 %length of actuation region
w1=2e-6 % width of actuation region
A1=l1*w1 %Actuation area
g01=900e-9 %gap at gate 1
x1=150e-9 % initial displacement at gate 1
x12=x2/4 % Displacement at gate 2 caused by gate 1 actuation
k1=24*E*Ib/(l1^3+6*l1*lb-4*(l1^2)*lb) %Spring constant at gate 1
v1= 54 %Applied voltage at gate 1
Energy_g12=((e0*A1)/(2*(g01-x1-x12)))*((x12)/g01-x1)*v1^2+(0.5*k1*(x12)^2) %Consumed energy
```

6.2 *Newton Method for Solving the Floating Potential on the Cantilever.*

```
e0=8.85e-12 % Permittivity of free space (J/V^2)

l=20e-6 %length of cantilever (m)

vbi=0.81 %Built-in voltage of JFET (V)

m=6.8e-15 %effective mass of cantilever (kg)

g=9.8 %acceleration due gravity (m/s)

k=0.22 %effective spring constant of cantilever(F/m)

d=450e-9 %Gate 3 initial gap(m)

q=1.6e-19 %electonic charge (C)

esi=1.05e-10 % permittivity of Silicon (J/V^2)

Nd=1e21 %doner doping of JFET channel(ion/m^3)

A1=40e-12 %actuation area (m^2)

A2=2e-12 % depletion region area (m^2)


x=(5:5:100)*1e-9 % displacement of cantilever


for i= 1:20

   syms vg2 vg3 % Symbolic variables for voltages at Gate2 and Gate3  respectively

   F1(i)=(0.5*e0*A1/(d-x(i)).^2).*(vg3-vg2)^2; %Force between gate3 and gate2

   F2(i)=(-0.5*e0*A1/(d+x(i)).^2).*(vg2)^2; %Force between gate2 and gate4

   F3(i)=F1(i)+F2(i); % Sum of forces

   F=m*g; % Gravitational force

   x1(i)=(F+F3(i))./k; % Displacement of cantilever by applied Vg3
```

```
    c0=e0*A1/d; %Norminal capacitance
    c1(i)=c0.*(1+x(i)./d); %Capacitance between gate2 and gate4
    c2(i)=c0.*(1-x(i)./d); %Capacitance between gate3 and gate2
    cdep=(sqrt(q*esi*Nd/(2*(vbi-vg2))))*A2; %Depletion capacitance of the JFET
    vg2_1(i)=vg3.*(c1(i)./(c1(i)+c2(i)+cdep)); %Floating voltage on gate2

    Eq1(i)=x1(i)-x(i); %x1(i)=x(i)
    Eq2(i)=vg2_1(i)-vg2; %vg2_1(i)=vg2

    tolerance= .01; %maximum tolerable RSS of errors in output vector
    initial_est= [-4,-10]; %row vector of initial estimate for Vg2 and Vg3 respectively
    sol(i,:) = newton_n_dimx(tolerance,initial_est,[vg2,vg3],[Eq1(i);Eq2(i)]); %row vector of
                                %solution. The function newton_n_dimx is coded by Kyle Drerup below.
end
plot(sol(:,2),sol(:,1))
```

6.3 *Newton Method for Solving a System of >=n Nonlinear Equations for n Variables by Kyle J. Drerup*

```
function [X] = newton_n_dimx(tolerance_rss,initial_estimate,sym_variables,sym_equations)
%% newton method for solving a system of >=n nonlinear equations for n variables
% Given n equations, the function performs the newton method, converging to the exact solution.
% Given >n equations, the function converges to the solution which minimizes the least squared
% error of the given equations.
%input:    tolerance_norm :       maximum tolerable RSS of errors
```

```
% in output vector
%          initial estimate :      row vector of initial estimate
%          sym_variables:          row vector of n symbolic variables
%          sym_equations:          column vector of >=n symbolic equations
%output:    solution:               row vector of solution.

%assumptions:   1.  Input sym functions are differentiable
%               2.  Convergence is dependent on the functions.
%                  -check convergence constraints.
%                   -http://en.wikipedia.org/wiki/Newton's_method
%
% %%   Example:
%         syms a b
%         F1 = a-15;             %(15 = a)
%         F2 = b^2-10;           %(10 = b^2)
%         tolerance = .1;
%         initial_est = [10,1];
% %with n equations and n unknowns:
%         solution = newton_n_dimx(tolerance,initial_est,[a,b],[F1;F2]);
% % %with >n equations and n unknowns:
% % %        F3 = sqrt(a^2 + b^2)-15.5; (third equation, (15.5 = sqrt(a^2 + b^2)))
% %        solution = newton_n_dimx(tolerance,initial_est,[a,b],[F1;F2;F3]);

%Kyle J. Drerup
```

```
%Ohio University EECS

%11-9-2010

%%  the code...


H = jacobian(sym_equations,sym_variables);

X = initial_estimate;

n_equations = 0;

if length(sym_equations)==length(sym_variables),

   n_equations = 1;

end

stop = 0;

while ~stop,

       F_X = subs(sym_equations,sym_variables,X);

       F_prime_X = subs(H,sym_variables,X);

       if ~isnumeric(F_prime_X),

          F_prime_X = eval(F_prime_X);

       end

   if n_equations ==1,

       d_X = (F_prime_X^-1)*F_X;

   else %overdetermined solution, use generalized inverse matrix

       d_X = ((F_prime_X.'*F_prime_X)^-1)*F_prime_X.'*F_X;

   end

   X = X - d_X.' ;

   if (sqrt(sum(d_X.^2)) < tolerance_rss),
```

```
        stop = 1;
    end
end
end
```

6.4 *Resonance Frequency of the STM Probe Tip*

```
%%%%%Resonance Frequency of STM Probe tip%%%%%%%%%%

lp=72e-6 %length of the probe
wp=1e-6 % width of the probe
tp=2e-6 % thickness of the probe

ts=2e-6 % thickness of meander spring
ws=300e-9 %width of meander spring

Is=(ts*ws^3)/12 %moment of inertia of the springs

EE=180e9 %Young's Modulus
vv=0.27 %Poisson ratio
Eff=EE/(1-vv^2) %Effective Young's modulus

rho=2330 %Density of the silicon device layer
m1=rho*lp*wp*tp % mass of probe tip
m2=m1 %mass of comdrive fingers plus attachement
```

```
l2=9.2e-6 %length of shorter section of the spring

l3=19.5e-6 %length of the longer section of the spring

k2=(12*Eff*Is)/l2^3 %spring constant for the shorter section of the spring

k3=(12*Eff*Is)/l3^3 %spring constant for the longer section of the spring

keff=2*((k2*k3)/(k2+k3)) %Total spring constant for the springs on both sides of the probe


f0=(1/(2*pi))*sqrt(keff/(m1+m2)) %Fundamental resonance frequency
```

Chapter 7 References

[1] A. Witvrouw, “CMOS-MEMS Integration: Why, How and What” *ICCAD'06*, San Jose, CA, pp. 826-827, Nov. 2006.

[2] D. Chang, M. Lee, D. Chen and V. Liva, “Power junction FETs (JFETs) for very low-voltage applications,” *Applied Power Electronics Conference and Exposition*, Twentieth Annual IEEE, Vol.3, pp. 1419- 1423, Mar 2005.

[3] K. Akarvardar, S. Cristoloveanu, P. Gentil, R. D. Schrimpf, and B. J. Blalock , “Depletion-All-Around Operation of the SOI Four-Gate Transistor,” *IEEE Transactions on Electron Devices*, Vol.54, No.2, pp. 323-331, Feb. 2007.

[4] H. Luo, G. K. Fedder, and L. R. Carley, "A 1 mG lateral CMOS-MEMS accelerometer," *Micro Electro Mechanical Systems*, pp.502-507, Jan. 2000.

[5] D. Grogg, D. Tsamados, N. D. Badila, and A.M. Ionescu, “Integration of MOSFET Transistors in MEMS Resonators for Improved Output Detection," *Solid-State Sensors, Actuators and Microsystems Conference*, pp. 1709-1712, Jun. 2007.

[6] H. C. Nathanson, W. E. Newell, R. A. Wickstrom, and J. R. Davis, Jr., “The resonant gate transistor,” *IEEE Transactions on Electron Devices*, Vol. 14, No. 3, pp. 117-133, Mar. 1967.

[7] D. Weinstein, S. A. Bhave, “ The Resonant Body Transistor,” *Nano Letters*, Vol. 10, No. 4, pp. 1234-1237, Feb. 2010.

[8] M. W. Putty, “Polysilicon Resonant Microstructures,” Master of Science Thesis, University of Michigan, Ann Arbor, MI, 1988.

[9] C.T-C. Nguyen, “ Micromechanical Signal Processors,” Ph.D dissertation, University of California at Berkeley, Berkeley, CA, 1994.

[10] J. H. Lee, “An On-Chip Test Circuit for Characterization of MEMS Resonators,” Master of Science Thesis, Massachusetts Institute of Technology, Cambridge, MA, 2011.

[11] P. Braghetto and L.C. Kretly, “Hysteresis in RF MEMS shunt switch: Simulation and measurements,” *Microwave and Optoelectronics Conference*, pp. 136-140, Oct.-Nov. 2007.

[12] A. Lal, S. Radhakrishnan, N. Yoshimizu, and S. Ardanuc, “Relay-connected semiconductor transistors,” Patent No. US 7, 495,952 B2, Feb. 2009.

[13] G. M. Rebeiz, “RF MEMS Theory, Design, and Technology,” New Jersey: J. Wiley & Sons, 2003, pp. 4.

[14] M. L. Roukes, “Mechanical Compution Redux?,” *Proc. IEEE International Electron Device Meeting*, San Francisco, CA, pp. 539-542, Dec. 2004.

[15] V. Vijay, K. J. Vinoy, and K. A. Jose, “RF MEMS and their Applications,” John Wiley & Sons, 2003, pp. 109.

[16] A. P. De Silva, C. Vaughan, D. Frear, L. Liu, S.M. Kuo, J. Foerstner, J. Drye, J. Abrokwah, H. Hughes, C. Amrine, C. Butler, S. Markgraf, H. Denton, and S. Springer, “Motorola MEMS switch technology for high frequency applications,” *Microelectromechanical Systems Conference*, pp. 22-24, Aug. 2001.

[17] A. Grandaldi and P. Decuzzi, “The dynamic response of resistive microswitches: switching time and bouncing,” *Journal of Micromechanics and Engineering*, Vol.16, No. 7, pp. 1108–1115, April 2006.

[18] H. H. Yang, J. O. Lee, and J. B. Yoon, “Maneuvering Pull-in Voltage of an Electrostatic Micro-switch by Introducing a Pre-charged Electrode,” *Proc. IEEE International Electron Device Meeting*, Washington, DC, pp. 439-442, Dec. 2007.

[19] L. L. Mercado, S. M. Kuo, T. Y. T. Lee, and L. Liu, “A Mechanical Approach to Overcome RF MEMS Switch Stiction Problem,” *Electronic Components and Technology Conference*, New Orleans, LA, pp. 377-384, May 2003.

[20] K. O. Owusu and F. L. Lewis, “Solving the “Pull-in” Instability Problem of Electrostatic Microactuators using Nonlinear Control Techniques,” *IEEE International Conference on Nano/Micro Engineered and Molecular Systems*, Bangkok, Thailand, pp. 1190-1195, Jan. 2007.

[21] K. Amponsah, N. Yoshimizu, S. Ardanuc, and A. Lal, "Near-kT switching-energy lateral NEMS switch," *IEEE International Conference on Nano/Micro Engineered and Molecular Systems*, Xiamen, China, pp. 985-988, Jan. 2010.

[22] J. B. Muldavin and G. M. Rebeiz, "Nonlinear electro-mechanical modeling of MEMS switches," *Microwave Symposium Digest, IEEE MTT International*, Phoenix, AZ, Vol. 3, pp. 2119–2122, May 2001.

[23] V. Kaajakari, "Closed form expressions for RF MEMS switch actuation and release time," *Electronics Letters*, vol.45, No.3, pp.149-150, 2009.

[24] E. N. Shauly, "CMOS Leakage and Power Reduction in Transistors and Circuits: Process and Layout Considerations," *Journal of Low Power Electronics and Applications*, Vol. 2, No. 1, pp. 1-29, 2009.

[25] L. Tzung-Lin, H. Wu-Lin, C. Hung-Bin, H. C. H. Wang, C. Chun-Yen, and H. Chenming, "Novel dual-metal gate technology using Mo-$MoSi_x$ combination," *IEEE Transactions on Electron Devices*, Vol. 53, No. 6, pp. 1420-1426, Jun. 2006.

[26] L. Shaw and R. Abbaschian, " Chemical states of the molybdenum disilicide (MoSi2) surface," *Journal of Materials Science*, Vol. 30, No. 20, pp. 5272-5280, Oct. 1995.

[27] P. J. Cumpson and M. P. Seah, "Stability of reference masses. IV: Growth of carbonaceous contamination on platinum-iridium alloy surfaces, and cleaning by UV/ozone treatment," *Metrologia*, Vol. 33, No. 6, pp. 507-533, 1996

[28] D. A. Neamen, Semiconductor Physics and Devices, 3rd Ed. McGraw-Hill, NY, 2003, pp. 571-574.

[29] H. Li-Wen and C. T. C. Nguyen, "Silicide-based release of high aspect-ratio microstructures," *IEEE International Conference on Micro Electro Mechanical Systems*, Wanchai, Hong Kong, pp. 120-123, Jan. 2010.

[30] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill Company, 2001, pp. 201.

[31] T. H. Morshed, "Measurement and Modeling of *1/f* noise in MOSFET devices with high-k material as the gate dielectric," Ph.D dissertation, The University of Texas, Arlington, TX, 2007.

[32] SR570 User Manual [Online]. Available: www.thinksrs.com/downloads/PDFs/Manuals/SR570m.pdf, Accessed on 12th May 2013.

[33] F. A. Levinzon, L. K. J. Vandamme, "Comparison of 1/f Noise in JFETs and MOSFETs with Several Figures of Merit," *Fluctuation and Noise Letters*, Vol. 10, No. 4, pp. 447-465, 2011.

[34] J. R. Shealy, J. Wang, and R. Brown, "Methodology for Small-Signal Model Extraction of AlGaN HEMTs," *IEEE Transactions on Electron Devices*, Vol. 55, No. 7, pp. 1603-1613, Jul. 2008.

[35] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnology*, Vol. 6, No. 3, pp. 147-150, 2011.

[36] H. Hosseinzadegan, C. Todd, A. Lal, M. Pandey, M. Levendorf, and J. Park, "Graphene has ultra high piezoresistive gauge factor," *IEEE International Conference on Micro Electro Mechanical Systems*, Paris, France, pp. 611-614, Jan.-Feb. 2012.

[37] Fast, accurate and reliable resistivity testing [Online]. Available: www.cmicro.com/products/probes/custom/specialty/resistivity, Accessed on 12th May 2013.

[38] J. W. Wells, K. Handrup, J. F. Kallehauge, L. Gammelgaard, M. B. Balslev, J. E. Hansen, P. R. E. Petersen, P. Bøggild, and Ph. Hofmann, "The conductivity of Bi(111) investigated with nanoscale four point probes," *Journal of Applied Physics*, Vol. 104, No. 5, pp. 053717, 2008.

[39] J. C. Li, Y. Wang, and D. C. Ba, "Characterization of semiconductor surface conductivity by using microscopic four-point probe technique," *Physics Procedia*, Vol. 32, pp. 347-355, 2012.

[40] S. Hasegawa and F. Grey, "Electronic transport at semiconductor surfaces-from point-contact transistor to micro-four-point probes," *Surface Science*, Vol. 500, No. 1–3, pp. 84-104, Mar. 2002.

[41] Tutorial on electronic transport [Online]. Available: http://nanotube.msu.edu/nt05/abstracts/NT05tutor-Nygard.pdf, Accessed on 15th November 2013.

[42] J. J. Yao, S. C. Arney, N. C. MacDonald, "Fabrication of high frequency two-dimensional nanoactuators for scanned probe devices," *Journal of Microelectromechanical Systems,* Vol. 1, No. 1, pp. 14-22, Mar. 1992.

[43] H. Toshiyoshi, M. Mita, M. Goto, G. Hashiguchi, P. Fujita, D. Kobayashi, J. Endo, and Y. Wada, "Micromechanical tunneling probes and actuators on a silicon chip ," *Microprocesses and Nanotechnology Conference*, Yokohama, Japan, pp. 180-181, Jul. 1999.

[44] M. Mita, H. Kawara, H. Toshiyoshi, J. Endo, and H. Fujita, "Bulk micromachined tunneling tips integrated with positioning actuators," *Journal of Microelectromechanical Systems*, Vol.14, No.1, pp. 23- 28, Feb. 2005.

[45] L. Shi, G. Lorito, V. Jovanović, S. Fregonese, and L. K. Nanver, "JFET test structures for monitoring strain-enhanced mobility," *Proceedings of 9th Annual Workshop on Semiconductor Advances for Future Electronics and Sensors*, Veldhoven, Nizozemska, pp. 432-435, 2006.

[46] R. Rochette, M. Cassé, M. Mouis, A. Haziot, P. Pioger, G. Ghibaudo, and F. Boulanger, "Piezoresistance effect of strained and unstrained fully-depleted silicon-on-insulator MOSFETs integrating a HfO_2/TiN gate stack," *Solid-State Electronics*, Vol. 53, No. 3, pp. 392-396, Mar. 2009.

[47] J. H. T. Ransley, C. Durkan, and A. A. Seshia, "A Depletion Layer Actuator," *Solid-State Sensors, Actuators and Microsystems Conference*, Lyon, France, pp. 1393-1396, Jun. 2007.

[48] K. Amponsah and A. Lal, “Multiple tip nano probe actuators with integrated JFETs,” *IEEE International Conference on Micro Electro Mechanical Systems*, Paris, France, pp. 1356-1359, Jan.-Feb. 2012.

[49] E. Algre, X. Zhuang, M. Faucher, B. Walter, L. Buchaillot, and B. Legrand, “MEMS Ring Resonators for Laserless AFM With Sub-nanoNewton Force Resolution,” *Journal of Microelectromechanical Systems*, Vol. 21, No. 2, pp. 385-397, Apr. 2012.

[50] Q. Niu, M. C. Chang, and C. K. Shih, “Double-tip scanning tunneling microscope for surface analysis,” *Physical Review B*, Vol. 51, No. 8, pp. 5502 - 5505, 1995.

[51] J.M. Pitarke, P.M. Echenique, F. Flores, “Apparent barrier height for tunneling electrons in STM,” *Surface Science*, Vol. 217, No. 1–2,, pp. 267-275, 1989.

[52] T. Nakanishi and T. Tsuneya, “Conductance between Two Scanning-Tunneling-Microscopy Probes in Carbon Nanotubes,” Journal of the Physical Society of Japan, Vol. 77, No. 2, pp. 024703, 2008.