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THE ELECTRONIC PACKAGING PROGRAM

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Cover: Professor Che-Yu Li, director of the Electronic Packaging Program. The gold microbump connector in the background is enlarged approximately forty times.

THE ELECTRONIC PACKAGING PROGRAM

For a microelectronic system to work, each microchip must be protectively nestled on a carefully engineered carrier made out of plastic, composite, or ceramic. This carrier contains hundreds of tiny metal interconnects that feed power to the chips and transfer data among them. The carrier must also remove chip-killing heat, and the interconnects must withstand the strains of thousands of cycles of thermal expansion and contraction. An interconnected array of chip carriers may be mounted on a computer card, and several of these cards may be plugged into a larger circuit board. The technology that results in this hierarchy of chips, carriers, cards, and boards is the province of electronic packaging.

The importance of electronic packaging cannot be overstated. The gross annual revenue of the data-processing industry already exceeds that of the automobile industry, and it is growing at a faster pace. Electronic packaging is crucial to this whole enterprise, accounting for about 60 percent of the cost of a computer.

A relentless reduction in the size of components plus the demand for continual improvement in performance present many challenges. The Cray 1 supercomputer, designed by Seymour Cray in the late 1970s, filled an entire factory hall. Today, the same computational power is provided by the Alpha machine, an engineering workstation built by Digital Equipment Corporation. The Alpha can be packaged in a single deskside cabinet with a volume comparable to a medium-sized suitcase. According to projections made by the Semiconductor Industry Association, the size of the smallest features on silicon chips will continue to shrink throughout the 1990s, while the size of the chips themselves is expected to grow. This means that more and more integrated electronic circuits can be placed on individual chips, and electronic systems will become yet more compact. Currently, portable systems represent the fastest-growing segment of the industry.

An Electronic Packaging Program has been set up to coordinate a range of activities that take place at Cornell. Under the directorship of Professor Che-Yu Li, of the Department of Materials Science and Engineering, the program encompasses the Semiconductor Research Corporation (SRC) Packaging Program and the Industry–Cornell University Alliance for Electronic Packaging.

The SRC is a consortium of leading United States semiconductor and systems companies, dedicated to supporting research that both increases the knowledge base and provides for the training of new researchers in fields of engineering and the physical sciences that are involved with semiconductors and related technologies. The SRC Packaging Program is a comprehensive, interdisciplinary research program that was established at Cornell in 1986. It is supported by more than twenty companies and has an annual budget of $600,000.

To expand Cornell's research in electronic and optoelectronic packaging, the Industry–Cornell University Alliance for Electronic Packaging was formed in 1990. Participating in this partnership are several companies, some of which are also members of the SRC. A goal of the alliance is to achieve a membership that spans the whole gamut from suppliers of materials and components through companies that design and manufacture systems. The mission of the alliance is to perform basic, precompetitive, and directed research that will help the United States to achieve worldwide leadership in electronic packaging.

Current members of the alliance include Akzo Electronic Products, Inc.; AMP, Inc.; the Carborundum Company; Digital Equipment Corporation; and IBM. The member companies contribute funds to support the research of the alliance and assign industrial residents, who spend a major part of the year at Cornell participating in specific research projects. In addition to developing new materials and technologies, the alliance provides valuable research experience and continued education for the industrial residents, increases the number of students who graduate with interests and backgrounds in electronic packaging, and facilitates technology transfer. The annual budget of the alliance is currently about $875,000.

To provide a dedicated space for research, the Advanced Electronic Packaging Facility is being established in an 8,000-square-foot area on the first floor of Kimball Hall. The National Science Foundation and Cornell University are sharing the expense of renovating this area. Equipment will be donated by the Digital Equipment Corporation and IBM, and operating expenses will be partly defrayed by the State of New York. A Class-1,000 clean room will take up 1,000 square feet of the area, and there will be a complete line of equipment for fabrication, characterization, and testing. The renovations are scheduled for completion in December 1993.

Cornell is also committed to making a sound education in electronic packaging available to interested students. Che-Yu Li, together with two coauthors from IBM, wrote the first comprehensive textbook on this subject. Three special courses, focusing on electrical, thermal, materials, and manufacturing
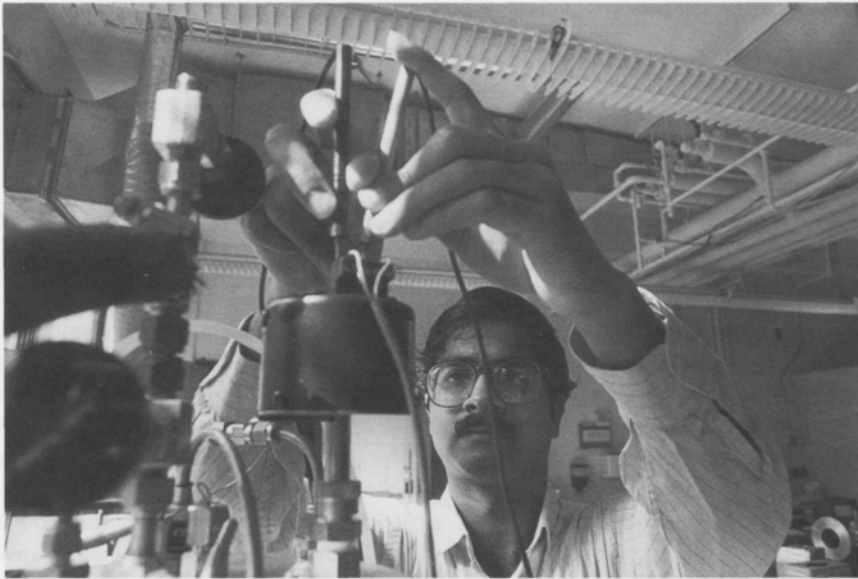
Left: Postdoctoral research associate Sourav Bhunia evaluates the performance of a heat pipe intended to help prevent overheating in electronic packages.

Below: Graduate student Yoke Chung uses a specially designed apparatus to determine the thermal diffusivity of thin films.

aspects, make possible a concentration in electronic packaging in the Master of Engineering degree program. The first Joint Conference on Electronic Packaging Education, held at Cornell on October 5 and 6, 1992, was attended by representatives from eighteen colleges and universities and a large number of industries.

This issue of the *Quarterly* presents an overview of some of the research that is being conducted with support from the SRC program and the electronic packaging alliance. The engineering of electronic packages involves attacking electrical, thermal, mechanical, and materials problems, as well as devising efficient and reliable manufacturing processes. A full range of materials must be used, including organic polymers, metals, and ceramics. The articles that follow reflect the diversity of the electronic-packaging research that is taking place at Cornell.

Christopher K. Ober and Nancy C. Stoffel describe research on polymeric materials, especially efforts to improve the adhesion of polyimide interlayers and to develop block-copolymer resists. Michael W. Russell, Gerald T. Kraus, and Emmanuel P. Giannelis write about their efforts to use spin-on technology to prepare thin films of high-dielectric-constant oxides, which can be used to make capacitors. Che-Yu Li describes research on ways to make reliable electrical connections between very small contacts in very dense arrays. C. Thomas Avedisian and Kenneth E. Torrance give an overview of work on techniques for removing heat from
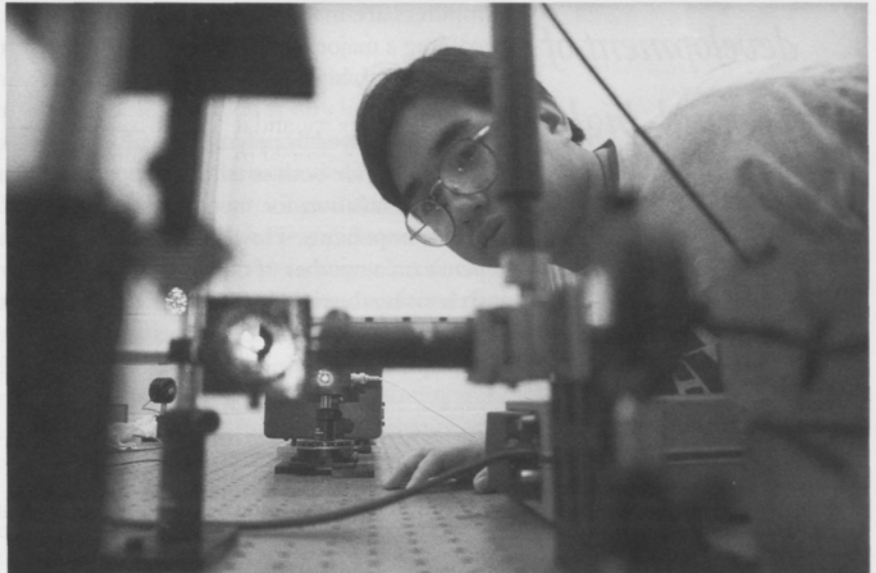
electronic packages. And J. Peter Krusius describes AUDiT, a simulation tool that makes it possible to assess the costs and benefits of different combinations and different arrangements of components.

All the research in electronic packaging at Cornell is designed to solve common technological problems. The precompetitive nature of the projects encourages multi-company participation, facilitates the formation of strategic alliances in key research areas, and allows a mutually beneficial utilization of the resources of the university and the participating companies. With the establishment of a dedicated facility and a strong commitment to education, the program of electronic packaging at Cornell is poised to expand rapidly in the near future and make a major contribution to United States industry.

THE IMPORTANCE OF POLYMERS IN PACKAGING

by Christopher K. Ober and Nancy C. Stoffel

"polymers are becoming a major factor in the development of economical, high-performance, electronic packaging."

A remarkably large fraction of the components in a modern computer are made of polymers. Printed wire boards, cards, modules, flex circuits, and even chips employ different kinds of polymers, carefully tailored to the tasks they are expected to perform. Still other polymers, though not present in the final products, are used in the manufacturing processes through which computers are made. Indeed, polymers are becoming a major factor in the development of economical, high-performance, electronic packaging.

The role played by polymers involves their ability to provide both structural support and electrical insulation for metal and semiconductor components. How well they do this depends on a number of different properties, and choosing the right polymer for each job is one of the most important exercises in improving computer design. In comparison with other materials, such as metals and ceramics, polymers are very good insulators, both electrical and thermal—they have low dielectric constants and conduct heat poorly. They can be processed at relatively low temperatures, in the range of 350° to 400°C—versus 660° for aluminum and about 1,200° for silica. Their coefficient of thermal expansion is much greater than that of most ceramics and metals, and designers are challenged by the need to make interfaces that allow different materials to expand and contract at different rates without generating destructive mechanical stresses. Nevertheless, they are indispensable as electrical insulators.

Polymer research conducted under the electronic packaging alliance aims to develop new materials and processes tailored to meet the needs of the packaging industry. Two specific initiatives, discussed here, involve polyimide interlayers and block-copolymer resists.

resist used in processing chip

polyimide dielectric layers in module
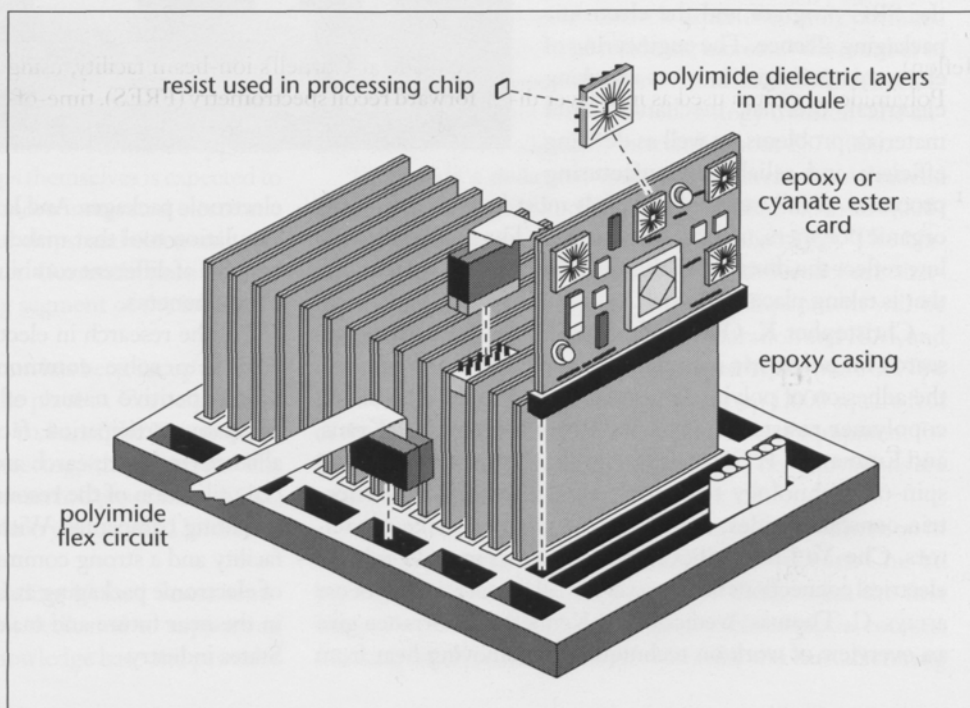
epoxy or cyanate ester card

epoxy casing

polyimide flex circuit

Figure 1. The use of polymers in computers. As this schematic view of the inside of a computer shows, polymers play many important roles.
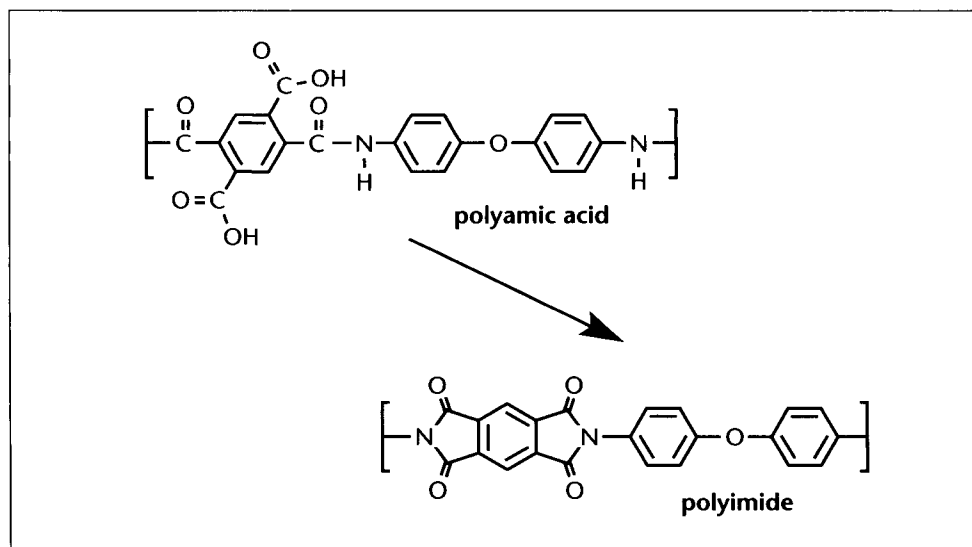
Improving Adhesion between Polyimide Layers

A group led by Edward J. Kramer is investigating adhesion between polyimide layers. Polyimides are a class of polymers with good thermal stability and desirable mechanical properties, as well as a relatively high glass-transition temperature. This makes them especially suitable for applications requiring high-temperature processing, so they are used in the chip-on-board mounting technology, despite their somewhat high dielectric constant (as compared with polymers such as Teflon).

Polyimides are often used as interlayer dielectrics, with a series of thin layers deposited sequentially to form a microelectronic structure. Unfortunately, these layers display poor self-adhesion, and their propensity to delaminate complicates processing and adversely affects reliability. The difficulty arises, in part, from the way in which polyimide layers are prepared. Polyimide is not soluble in common solvents, so it must be processed in a precursor form such as polyamic acid or polyamic alkyl ester. Using these materials, uniform films can be cast from solution, dried, and thermally treated to create the final polyimide structure via a ring-closing reaction (see Figure 2). If the first layer is fully converted to polyimide, subsequent layers spun-cast on top of it will bond poorly. The adhesive strength between the layers is related to the amount of interdiffusion across the interface, and since the polyimide and its precursor are essentially immiscible, diffusion is very limited.

The Kramer group is investigating the factors controlling the amount of interdiffusion in the hope of improving adhesion between polyimide layers. The way different polymer architectures and spin-casting solvents affect the amount of imidization and interface properties is being explored using several depth-profiling techniques. The material in one of the layers is labeled by replacing some of the hydrogen atoms of the polymer with deuterium. Diffusion measurements can then be made at Cornell's ion-beam facility, using forward recoil spectrometry (FRES), time-of-flight FRES, and nuclear-reaction analysis (see *Quarterly* 26(1):29-35). The depth resolution of these techniques varies between 150 and 600 Å. If higher resolution (in the vicinity of 10 Å) is needed, neutron reflectivity measurements are made at either Argonne National Laboratories or at the National Institute of Standards and Technology.

Kramer and his coworkers have found that small changes in the architecture of the polyamic ethyl ester can have a profound effect on imidization kinetics, even though they lead to the same polyimide. For example, the para-isomer has a higher degree of conversion to polyimide than the corresponding meta-isomer after identical thermal treatments. It was also found that the imidization reaction did not proceed uniformly as a function of depth. Rather, there was less conversion in the

region within 2,000 Å of the surface than in the bulk (see Figure 3). In contrast, the meta-isomer had a uniform degree of imidization as a function of depth. It may be possible to intentionally tailor the imide fraction at the surface and thus improve adhesion.

For the polyamic ethyl precursors of the polyimide, PMDA/ODA, the amount of interdiffusion depends on temperature and degree of conversion to polyimide in the base layer. The interfacial fracture energy decreases rapidly from 1,500 to 200 joules per square meter as the degree of conversion increases from 50 to 100 percent (see Figure 4). In other words, the amount of energy required to pull the layers apart depends primarily on the amount of interpenetration of the top layer and the bottom layer. This is, in turn, dependent on how thoroughly the base layer has turned to imide.

The research group is currently exploring several methods of strengthening the polyimide-polyimide interface by altering the region near the surface. The improvement in self-adhesion that is expected to result will be critical for several emerging electronic-packaging technologies.

Block Copolymers for Superior Resists

Another research effort, led by the senior author, involves the development of block copolymer resists. Resists, which are used to produce the fine topological features required in microelectronics, are polymers that are sensitive to a specific type of radiation, becoming either soluble or insoluble as a result of exposure. In postexposure processing, the soluble portions are removed, leaving either a positive or a negative mask to protect underlying material during further processing.
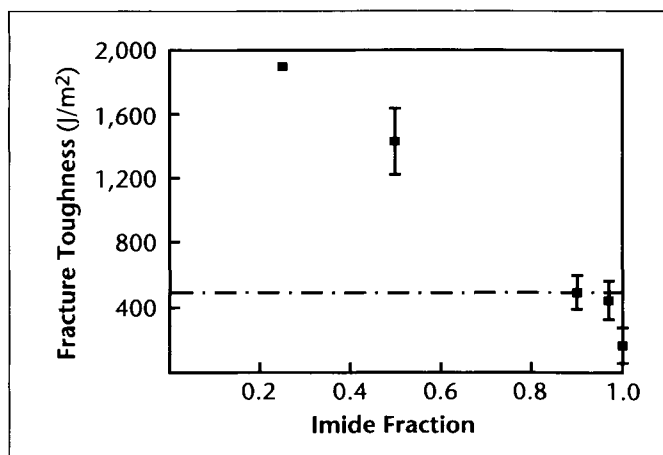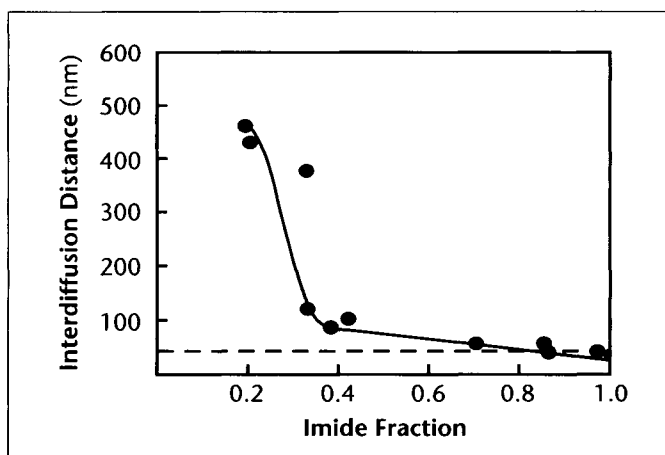
Polymeric resists are commonly used to produce microcircuitry by masking metallic surfaces which are then etched away, leaving narrow strips that conduct electricity between devices. It would be advantageous if polymeric resists could also be used to shape other polymer films used as insulators. Graduate students Allen Gabor and Eric Lehner took up the challenge, with support from the Semiconductor Research Corporation's Microscience and Technology Program.

Their solution is to use a block copolymer, which is a hybrid of two dissimilar polymers linked by a covalent bond. One block produces a phase with a high glass transition temperature that can be imaged with an electron beam. The other block is rich in silicon, which makes it able to resist reactive ion etching (RIE) in an oxygen plasma, although it has a low glass transition temperature and lacks the dimensional stability needed to make a good resist. By using the two phases together, inextricably linked, it is possible to take advantage of their strengths, while suppressing their weaknesses (see Figure 5). The resulting material is much like a composite in which one phase provides the etch resistance and the other provides the imaging capability.

Block copolymer resists can be imaged, then processed to remove unexposed portions, and will form a clean, hard mask over the polymer film to be etched. Evaluation at the National Nanofabrication Facility showed that

Figure 3 (left). Interdiffusion distance as a function of base-layer imide fraction. The penetration of the top layer into the bottom layer decreases as the bottom-layer imide fraction increases.

Figure 4 (right). Fracture as a function of imidization. Interfacial fracture energy decreases as degree of conversion increases.

electron radiation

silicon-rich phase →

high-Tg phase →

Exposed regions
are crosslinked
to form an
insoluble network.

substrate

Unexposed polymer is
removed by developing.

High-Tg phase gives
dimensional stability
to submicron images.

High silicon concentration
at surface gives exceptional
oxygen RIE resistance.

substrate

Oxygen RIE exposes resist
and planarizing layer
to oxygen plasma.
Anything without silicon
is eaten away.

Silica layer protects
underlying polymer.

planarizing layer

substrate

Figure 5 (left). A bilayer resist based on block copolymers. The two halves of the block copolymer endow it with exceptional resistance to reactive ion etching as well as dimensional stability.

Figure 6 (below). Features produced with block copolymer resists. After processing, the planarizing layer protected by the resist has been formed into strips only 0.17 µm thick (seen in top view and from an angle).

these resists have a high etch-rate selectivity with respect to a polymer such as polyimide; in an oxygen plasma the polyimide is consumed fifty times faster than the resist. Moreover, the approach can produce features with a resolution of less than 0.1 micron, which is far superior to current requirements for processing materials such as polyimides. The resists have been used to produce lines 0.3 microns wide with an aspect ratio of 4.5 (shown in Figure
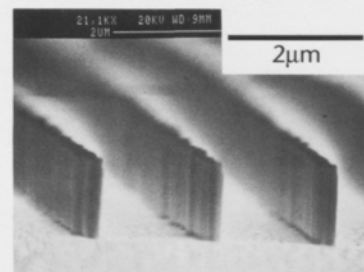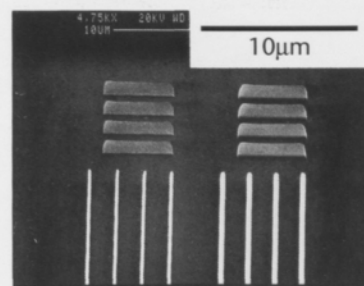
6). Continuing research involves block copolymer resists that can be imaged with ultraviolet radiation and developed in an alkaline environment.

**The Promise
of Further Research**

The continuing development of new and improved polymers for printed wire boards, adhesives, and flexible circuits can be expected

"line dimensions for electronic packages will soon be in the range of 25 microns"

to lead to further improvement in the performance of computers. Refinements in resists will make possible more sophisticated electronic packaging and yet smaller and denser integrated circuits.

According to current projections, electrical line dimensions for electronic packages will soon be in the range of 25 microns (or 1 mil). On materials with a lower dielectric constant, these lines could be placed closer together. The delay time would be shorter, and computers would be smaller and faster. The FR-4 epoxy currently used in printed wire boards has a dielectric constant of about 4. But Teflon has a dielectric constant of only 2.2, and its use in boards could lead to a whole new generation of computers.

The fact that polymers are relatively inexpensive and easy to process will lead to a wide range of new applications. Potential uses for polymers include optoelectronic interconnects and, perhaps one day, polymer-based photonic computers. As the computer industry continues to develop, it will be increasingly dominated by those who can produce the materials needed to implement new technologies, and many of these materials will be polymers.

Christopher K. Ober is an associate professor in the Department of Materials Science and Engineering. Born in Canada, he received his undergraduate education at the University of Waterloo, and earned the doctorate, granted in 1982, at the University of Massachusetts. He then worked at the Xerox Research Centre of Canada for four years, investigating particulate polymerization and liquid-crystalline polymer synthesis. He joined the Cornell faculty in 1986. An expert in tailoring the mechanical, thermal, and optical properties of polymers for specific industrial applications, he is a member of the American Chemical Society and the Materials Research Society.

Nancy C. Stoffel is a Ph.D. candidate working with Professor Edward J. Kramer. She holds a bachelor's degree from the University of Virginia and two master's degrees—one from Columbia University, where she studied chemical engineering and applied chemistry, and one from Cornell, in materials science and engineering. From 1984 through 1989 she worked at IBM's East Fishkill Facility, first as a process engineer and then as a staff engineer. While there, she was part of a team that received a patent for developing a method for forming cofired glass-ceramic multichip modules.

SPIN-ON OXIDES
FOR MICROELECTRONICS

by Michael W. Russell, Gerald T. Kraus, and Emmanuel P. Giannelis

Technological advances in integrated circuits have stimulated rapid growth in the microelectronics industry. In the 1950s, the bipolar transistor replaced the vacuum tube, and since 1975, the semiconductor integrated circuit has for the most part replaced discrete devices. Device miniaturization, with its advantages of low power consumption and high yield, has propelled digital integrated circuits to the forefront of the market.

More than one million devices can already be put on a single chip, and further miniaturization presents a challenge to designers and materials engineers. Reducing the size of very-large-scale integrated (VLSI) devices means reducing the area of capacitor structures such as the storage capacitor in a dynamic random access memory (DRAM). The capacitance of these structures is directly proportional to dielectric constant and area, but inversely proportional to film thickness. As components are packed closer together, the area available for each capacitor is reduced. In order to maintain the same capacitance, film thickness must also be reduced.

In traditional DRAM architectures, the dielectric medium is silicon dioxide (SiO_2). The storage capacitor of a one-million-bit DRAM requires a silicon dioxide layer that is only 10 nanometers thick. Unfortunately, when silicon dioxide films are made this thin, problems with defects, electrode sensitivity, and breakdown begin to occur. To overcome these difficulties, researchers are investigating insulators that have a higher dielectric constant. Such insulators would make it possible to use thicker films and still achieve the required capacitive density. Materials with a high dielectric constant are also needed for "decoupling capacitors," which decrease inductance and control the switching-noise level in a package.

The Advantages of the Spin-on Process

The challenge is to make acceptable thin films from materials that have appropriately high dielectric constants. Thin films can be deposited by either physical or chemical techniques. With physical techniques, such as sputtering and laser ablation, it is difficult to control film stoichiometry. Other drawbacks are the difficulties of conformal deposition in deep submicron applications and the difficulties of adapting processes to large-scale manufacturing. In contrast, chemical techniques, such as spin-on processes and chemical vapor deposition, offer greater control of stoichiometry and better step coverage. And of the two, spin-on techniques have the advantage of simplicity and low cost; wafers spin-coated with a thin film of silicon dioxide, for example, can be produced for only 10 or 20 percent of what they would cost if produced by chemical vapor deposition.

Spin-on deposition is a process of solution casting in which a liquid precursor applied to a substrate is thinned out by centrifugal force and then thermally cured. The heat drives off the solvent and transforms the precursor into an oxide. Spin casting produces films of uniform thickness over the substrate. Because of the spin-induced flow of the precursor solution, the cured layer is smoother than the underlayer. This is highly desirable in a multilayer structure because it eliminates problems from underlying topography in high-density packaging.
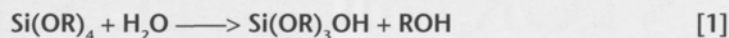
The Polymer Precursor: Synthesis of the Sol

To make high-dielectric-constant oxide films, our group begins with an inorganic polymer prepared by hydrolysis and condensation of a metal alkoxide. Hydrolysis results in the formation of reactive monomers, and during condensation these mono-
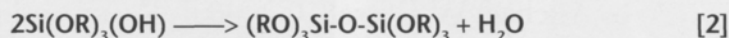
"*spin-on techniques have the advantage of simplicity and low cost*"

Figure 1: Hydrolysis and condensation reactions. These are the two basic steps in the formation of inorganic polymers.

Hydrolysis:

$$Si(OR)_4 + H_2O \longrightarrow Si(OR)_3OH + ROH \qquad [1]$$

Condensation:

$$2Si(OR)_3(OH) \longrightarrow (RO)_3Si\text{-}O\text{-}Si(OR)_3 + H_2O \qquad [2]$$

Figure 2. Steps in the preparation of spin-on thin films. After the liquid is thinned out by spinning, it is heated to evaporate the solvent and condense the film.

1. Spin coat

2. Evaporate solvent

3. Densify and crystallize

mers join together to form polymers (see Figure 1). In contrast to the linear carbon chains of organic polymers, the ability of the central metal atom to form several oxygen bonds (e.g., three for aluminum, four for silicon and titanium, five for tantalum and niobium) can result in an extended three-dimensional network.

The condensation reaction produces a sol whose viscosity increases as the reaction proceeds. Gelation of this polymer precursor may occur if a spanning network of chemical bonds is formed. The extent of hydrolysis and condensation is affected by the pH of the solution and other reaction conditions.

For a multicomponent oxide such as $PbZr_xTi_{1-x}O_3$, more elaborate methods have been devised to synthesize a precursor that contains each of the metal atoms on the same molecule with the appropriate stoichiometry. When the addition of dopants is called for, they are dispersed uniformly throughout the liquid.

Polymers ranging from weakly branched molecules to colloidal particles can be obtained under different synthesis conditions. The structure and morphology of the polymer network influence properties of the film, including the microstructure, thickness, and porosity.

Film Deposition by Spin Casting

To spin cast thin films deposited from alkoxide solutions, our group uses a commercially available spinner intended for the deposition of photoresists. The thickness of the films produced is proportional to the weight fraction of solids in solution, and inversely proportional to the square root of the speed at which the substrate is spun.

In order to assure defect-free films, spin-casting is performed in a clean room and the precursor solution is filtered to remove foreign particles. It has been found that films thicker than 0.5 micron are prone to cracking, so deposition is usually held to about 0.2 micron. Multiple coating can be used to build up thicker films.

During the final stages of film deposition, densification due to solvent evaporation coincides with continuing condensation reactions. Evaporation assists condensation by bringing polymeric species into closer proximity. The result is a contest between
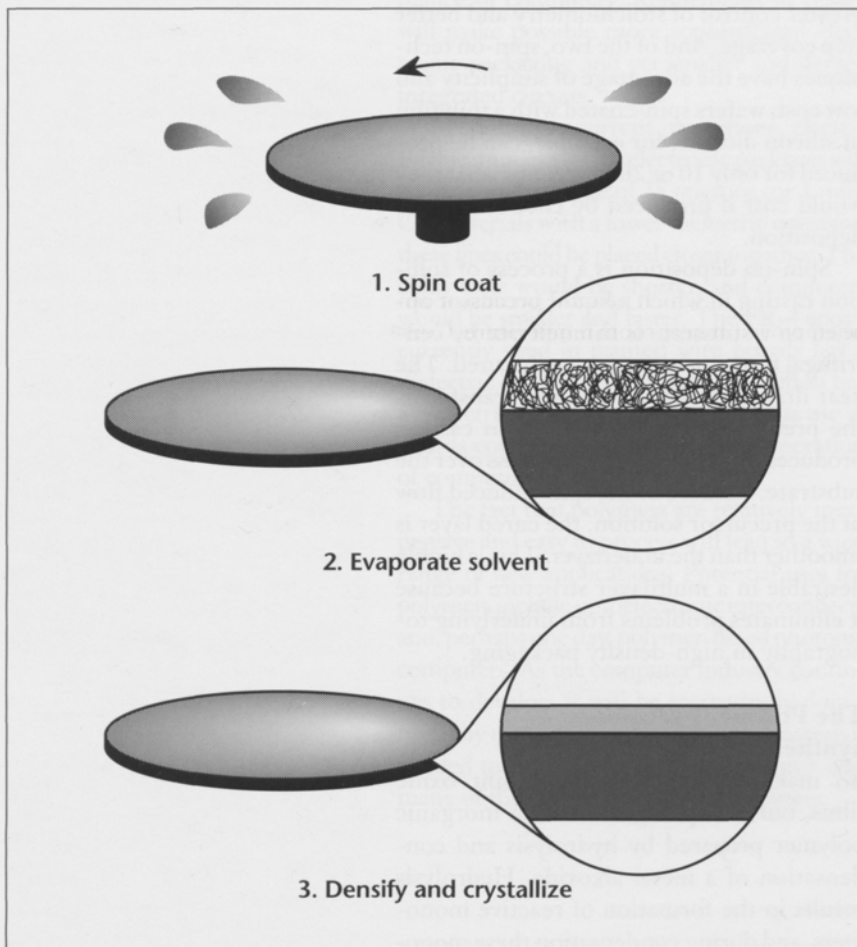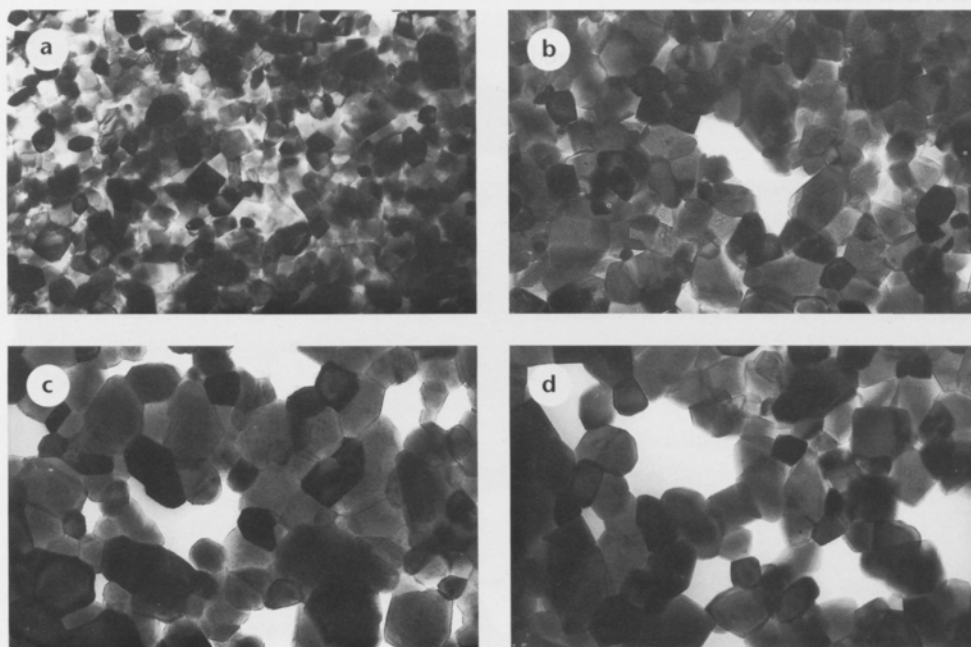
Figure 3. Bright-field TEM micrographs of free-standing TiO_2 films heated to 750°C in air and held at that temperature for 5 minutes. Density is a function of heating rate; the samples shown were heated at (a) 0.2°C per minute, (b) 1°C per minute, (c) 10°C per minute, and (d) 1,000°C per minute. The field in each photograph is about 2 microns wide.

evaporation, which compacts the film, and condensation, which stiffens it, increasing its resistance to further compaction.

If the condensation rate is high, polymers react quickly, before they attain the most efficient packing, and the result is a porous structure. If, on the other hand, the condensation rate is low, not every encounter leads to a reaction, and the system has time to achieve a denser final structure.

Thermal Processing and Densification

The deposition process produces a porous, amorphous film. Heating aids the mechanisms of condensation, producing additional oxygen bridges and eliminating remaining alkoxy and hydroxyl groups. Elimination of free volume within the film is accomplished through a rearrangement of atoms and molecules. Viscous sintering eliminates porosity, thereby creating a denser film.

Densification is critical to the microstructure and properties of the film. During heat treatment in some systems, crystallization takes place at the same time as densification, impeding the process of sintering and eventually bringing it to a halt. In other systems, such as SiO_2 and Ta_2O_5, this is not a problem. But in systems where crystallization and densification are concurrent, the rate of sintering is retarded because mass transport by diffusion through impinging crystals is slower than transport by viscous flow. The result is a porous, crystalline film. This effect can be avoided, however, by rapid heating to prevent crystal nucleation, which allows densification to occur prior to extensive crystallization. The result is a dense, crystalline film (see Figure 3).

Recently, we have found that spin-on thin films can be densified by ion implantation instead of conventional thermal annealing. This alternative holds great promise because it can be employed at near room temperature. Conventional thermal annealing involves temperatures that sometimes exceed 400°C, which is deleterious to many potential substrates. Densification by ion implantation may allow thin films to be prepared on metals with low melting temperature and even on some polymeric substrates.

Research on Thin Films of Tantalum Pentoxide

One focus of our research has been tantalum pentoxide (Ta_2O_5) which is commonly used as a dielectric in precision capacitors. Due to its high dielectric constant (20 to 40), Ta_2O_5 is under consideration as a replacement for SiO_2 in integrated circuits. Its use would increase capacitive density by a factor of six, allowing a significant reduction in the area used for capacitors.
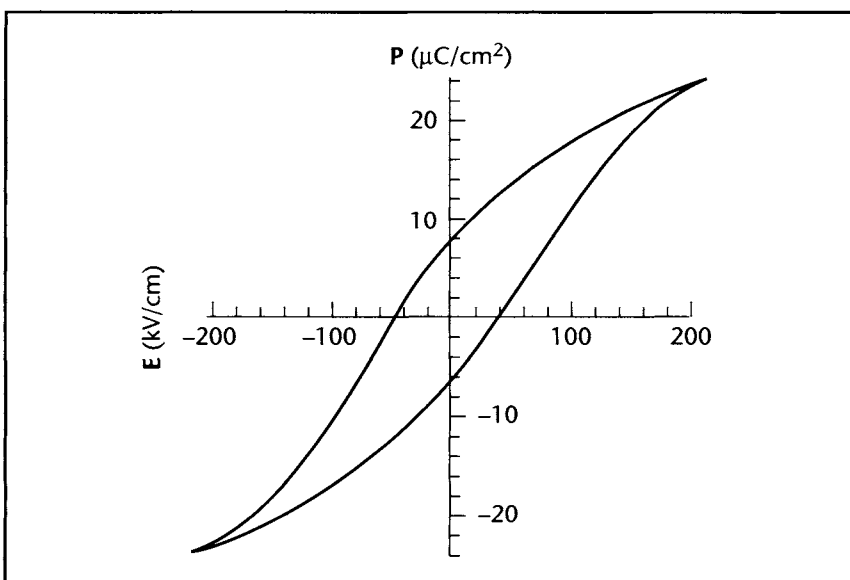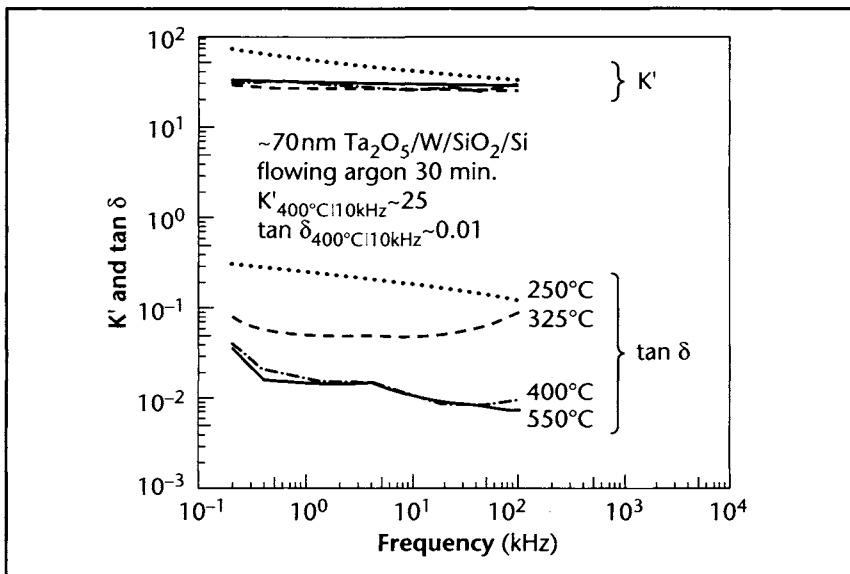
Films approximately 70 nanometers thick were formed by spin-casting on base electrodes of metallized silicon and processing at temperatures in excess of 250°C. Tantalum oxide capacitors were then created by evaporating gold top electrodes, and the dielectric behavior of these films was investigated (see Figure 4). Over a large frequency range (from 0.1 kilohertz to 10 megahertz), the dielectric constant remained at 25 for films processed at temperatures of 400°C and above. Leakage current is no greater than in Ta_2O_5 films prepared by other processes.

Densification and crystallization of sol-gel-derived tantalum-oxide thin films were also achieved using ion implantation in place of conventional heat treatment. Transmission electron microscopy (TEM) revealed the onset of crystallization for implant doses greater than $1x10^{15}$ Xe^+ ions per square centimeter. Electron diffraction patterns were indexed to orthorhombic β-Ta_2O_5. The electrical properties of films implanted with a dose of $5x10^{15}$ Xe^+ ions per square centimeter were comparable to films processed by conventional heat treatments.

Research on the Deposition of Ferroelectric Thin Films

Another research objective has been to develop spin-on techniques for depositing ferroelectric thin films. Ferroelectrics have a dielectric constant that is several times that of Ta_2O_5, which would allow a further reduction in the area of capacitors. In addition, they exhibit reversible spontaneous electric polarization that results in a hysteresis loop. This feature can be exploited to store information in nonvolatile memory, which retains information even when power is lost.

The ferroelectric used for spin-on experiments was $PbZr_{0.3}Ti_{0.7}O_3$ (PZT), a compound that contains a relatively low zirconium content and may have good long-term resistance to fatigue induced by switching. Fatigue resistance is a critical obstacle that must be overcome in order to develop practical materials for nonvolatile memories. Sol derived PZT films have a dielectric constant of 650 and show characteristic hysteresis in the plot of polarization versus electric field (see Figure 5).

Crystalline ferroelectric films have also been formed by ion implantation. Combining ion implantation with low temperature annealing may diminish the processing incompatibility of PZT and aluminum. Current work includes studying the stability of PZT films in contact with metal electrodes and further investigation of the mechanisms of densification.

Potential Impact of Spin-On Technology

The research conducted by our group has made a significant contribution to knowledge of the fundamental physics and chemistry of spin-on film deposition. As a result, novel spin-on materials and processes that are suitable

Figure 4 (top). Dielectric constant and dielectric loss for tantalum oxide thin films.

Figure 5 (bottom). Hysteresis of a MOD $PbZr_{0.3}Ti_{0.7}O_3$ thin film, rapidly thermally annealed at 700°C.

"spin-on technology will play an important role in the fabrication of future VLSI systems."

for use in VLSI systems have been developed. The range of useful spin-on materials includes both high-dielectric-constant oxides and conducting thin films. Improved process control, coupled with the low cost and ease of planarization, guarantee that spin-on technology will play an important role in the fabrication of future VLSI systems.

Michael W. Russell is a graduate student in the Department of Materials Science and Engineering. While earning the bachelor's degree in materials science at the Massachusetts Institute of Technology, he worked as a research assistant in both ceramics and metallurgical laboratories. He was also a summer intern at McDonnell Douglas Research Laboratories in St. Louis, Missouri, and at the General Electric Company's Thomson Laboratory in Lynn, Massachusetts. He was awarded a Corning Glassworks Fellowship in 1988 and an IBM Graduate Fellowship in 1989 and '90. This article is adapted, in part, from material in his doctoral disseration.

Gerald T. Kraus is also a graduate student in the Department of Materials Science and Engineering. He graduated with honors from the Pennsylvania State University, where he majored in engineering science and mechanics. He served as a summer software engineer at General Electric Transportation Systems in Erie, Pennsylvania, and as a research assistant in the study of point defects in oxynitride thin films at Pennsylvania State University. He also engaged in research as a co-op student at the IBM facility in Essex Junction, Vermont, during the summer and fall of 1990 and the summer of 1991. He was awarded a Department of Education Fellowship for 1991–93.

Emmanuel P. Giannelis is an associate professor in the Department of Materials Science and Engineering. His research focuses on the employment of chemical processing to fabricate low-dimensional materials like thin films and multilayer structures for electro-optic and high-temperature structural applications. He received the bachelor's degree from the University of Athens, in his native Greece, and the doctorate, granted in 1985, from Michigan State University. He is a member of the American Chemical Society, the American Ceramic Society, and the Materials Research Society.

DEPENDABLE CONNECTIONS
Getting the Signal In and Out

by Che-Yu Li

"Within the present decade, requirements for input and output will exceed two thousand connections per chip."

One of the most important aspects of electronic packaging is getting the signal in and out of modular components with a high degree of reliability. It is not enough to design good chips, carriers, cards, and boards; it is also necessary for electrical impulses to pass among them without interruption and without causing degradation. This means that ways must be found to make thousands of tiny connections between very small components. Some of these connections must be permanent, while others must be detachable, making it possible to remove and replace modules. All must be extremely dependable or the complex electronic equipment of which they form a part simply will not work.

My research group is studying three ways of making large numbers of very small connections. One project involves flip-chip solder joints, and another involves adhesive-based interconnects—both ways of making connections that are supposed to be permanent. A third project involves separable connectors made with flex circuits.

Flip-Chip Solder Joints
### for a High-Density Area Array

Electrical devices on chips are continually getting smaller, and at the same time, the chips themselves are getting bigger. Both trends contribute to an increase in the density as well as the total number of connections required for each chip. Within the present decade, requirements for input and output will exceed two thousand connections per chip. As the number of interconnects in a typical chip becomes increasingly dense, the size of each connection will have to decrease. This poses a tremendous challenge to design engineers, who must maintain reliability and devise suitable manufacturing processes.

One promising solution is the use of a dense area array of flip-chip solder joints. Area arrays can accommodate a much larger number of interconnects than conventional, wired interconnects, which utilize only the perimeter of the chip. In flip-chip construction, beads of solder are placed on contact pads on the chip to be attached. The chip is then flipped over, positioned, and heated, melting the solder to make the connections. Graduate students Jeffrey G. Maggard, Scott Bolton, and Dirk D. Brown, as well as staff engineer Boris Yost and senior research associate Peter Børgesen, are involved in research on the use of area arrays of small solder joints for attaching chips to substrates such as alumina (Al_2O_3) and aluminum nitride (AlN). The metallurgical properties of such joints and their relation to thermal fatigue are of vital interest.

We have been engaged in research on flip-chip solder joints for nearly fifteen years and have developed the capability to deposit, align, and reflow solder joints in the

Figure 1. A flip-chip solder joint between two surfaces. The solder is 97 percent lead and 3 percent tin; the surfaces are 32.7 microns apart.
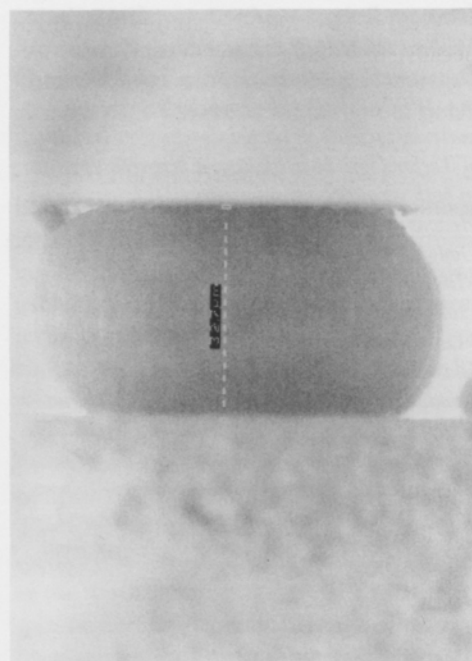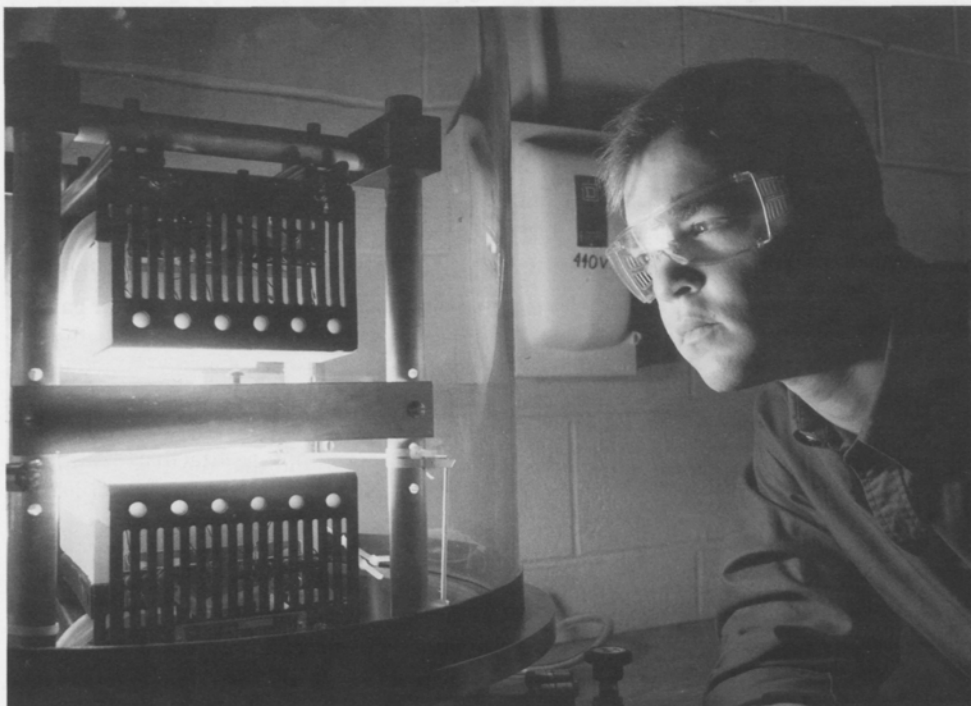
one-to-two-mil size range. To determine their low-cycle fatigue properties, arrays of solder joints are attached to a substrate and tested on our ultrasensitive micromechanical testing apparatus. By taking advantage of our unusual capabilities in this area, we have accumulated a large body of data on the mechanical properties of solder joints under a wide variety of conditions.

We are interested in aluminum nitride because of its coefficient of thermal expansion, which is nearly the same as that of silicon. When a chip is attached to an aluminum nitride substrate, the thermal strain on the soldered connections between them is much reduced. There is a problem, however, in getting metal to adhere to the aluminum nitride. We have developed a special metallization scheme that involves sputter deposition of aluminum in a nitrogen atmosphere of gradually decreasing pressure. This first layer is then metallized with chromium, copper, and gold in a procedure commonly used for contact pads on chips. We have patterned the metallization by photolithography and ion milling to form 1.4 mil contact pads, and then deposited and reflowed solder joints to connect two substrates to each other. When samples were subjected to shear stress, they failed at 14.6

megapascals—and through the solder joints, not the aluminum nitride–metal bond. We have filed for a patent on our approach.

Deformation of a Thin Epoxy Film Used for Adhesive-Based Connections

Adhesive-based interconnects are emerging as a high-performance, low-cost alternative to interconnects currently in use. One scheme consists of substrates with gold microbumps that are brought into contact by a thin film of epoxy adhesive that holds the substrates together. The reliability of such interconnects is crucially dependent on the mechanical performance of the adhe-
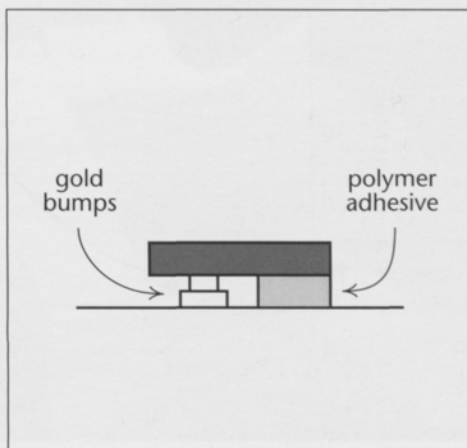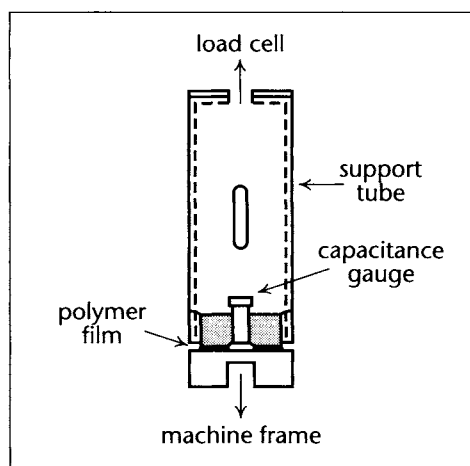

gold bumps

polymer adhesive

Figure 2. Schematic view of a microbump-type adhesive-based interconnect.

Figure 3. Capacitance gauge for measuring out-of-plane displacement of thin polymer adhesives. The way capacitance varies with load makes it possible to measure displacement with nanometer resolution.

sive. Especially important is the adhesive's out-of-plane or thickness distortion and the way this dimension changes with repeated heating and cooling.

Excessive increase in the thickness of the adhesive film is undesirable because it can open the contact between the gold bumps. In order to make such interconnects reliable, we need to know the coefficient of thermal expansion and the elastic modulus of the adhesive film in the thickness direction. Because the of thinness of the film, the measurement of these properties has not previously been possible. But the challenge was taken up by a team including John Dion (an industrial resident from Digital Equipment Corporation), senior research associate Peter Børgesen, and staff engineer Boris Yost.

We have developed an innovative device to measure the out-of-plane displacement of thin polymer adhesives. Two rigid steel substrates are glued together with a ring of epoxy such as Araldite. An opening in the middle of the upper substrate makes it possible to mount a capacitance gauge close to the film. The capacitance in the air gap between the gauge and the bottom substrate changes linearly with distance, providing an indicator of displacement in the thickness direction (see Figure 3).

We have found that the elastic modulus of a thin film is significantly less than that of the same material tested in bulk, and the coefficient of thermal expansion increases as thickness diminishes. Both phenomena seem to be related to fundamental changes in the morphology and structure of the polymer chains. Polarized microscopy reveals that the observed structural changes are associated with an increase in the orientation of polymer molecules when films are thinner than 4 mils (see Figure 4).

These findings have definite implications for the design of adhesive-based microbump interconnects. It seems clear that the compressive stress generated during the curing of the adhesive is sufficient to produce good electrical contacts, but it is not clear that good elec-

Figure 4. Effect of adhesive thickness on elastic modulus. The largest value, at 4 mils, agrees quite well with predictions based on bulk modulus and mechanical constraint.
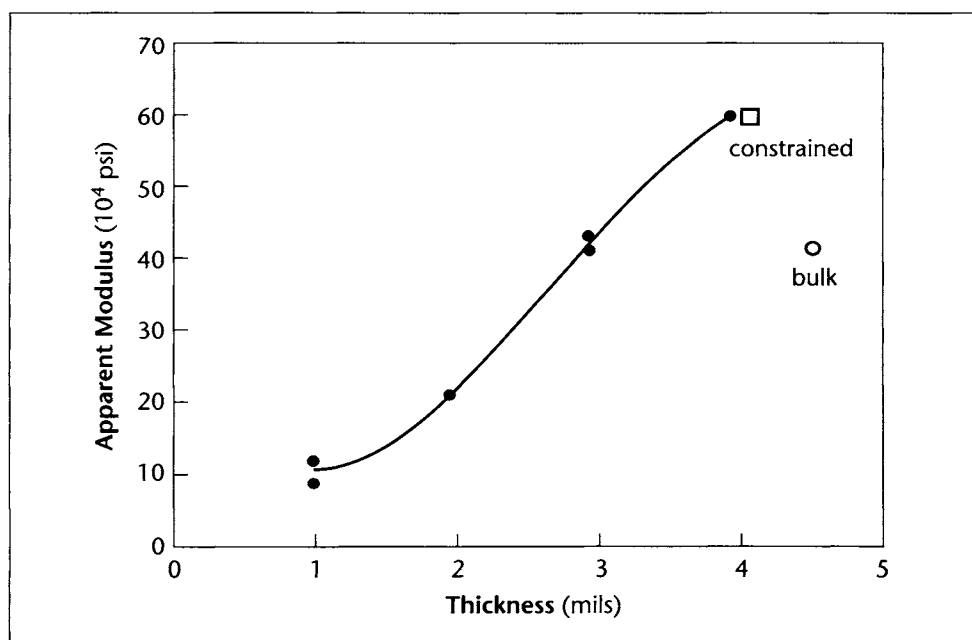
trical contact can be maintained during subsequent thermal excursions. We have developed a theoretical model that will predict the evolution of contact force in relation to time and temperature during service. The data we have obtained on materials properties are essential to the development of a cost-effective and reliable alternative approach to the problem of interconnects.

Flex Circuits Used As Separable Connectors

Separable connectors of the pin-and-socket type are commonly used to plug circuit cards into circuit boards. But such connectors do not offer a sufficiently large number of inputs and outputs to meet burgeoning interconnect requirements. A new approach that will allow a greater density of interconnects

Graduate student Dirk Brown uses a pad aligner, which positions components on substrates for microbump and flip-chip fabrication.
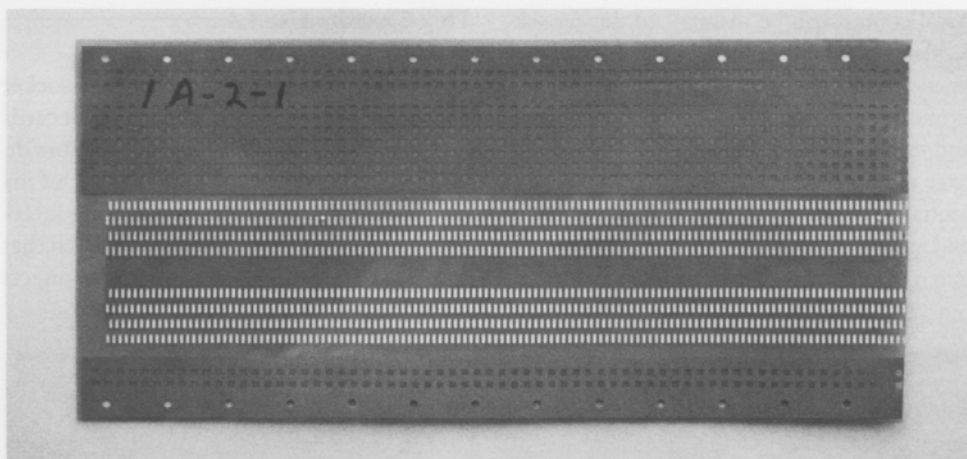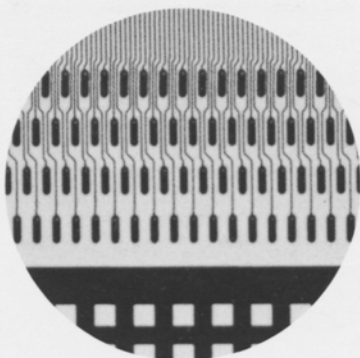
involves the use of a flexible circuit containing an area array of contact pads that are squeezed up against a matching set of contact pads on the card and the board.

This technology is being studied by a group including John Dion, Boris Yost, Peter Børgeson, and graduate assistant Janet Hill. We have been examining a prototype connector supplied by AMP, Inc., which consists of gold contact pads on a copper-polyimide carrier. The contact pads measure 25 by 100 mils and are raised a half mil above the carrier surface (see Figure 5). Electrical connections are made by compressing the flex circuit between a card or board and a massive backing.

Poor contact and high resistance between the pads are a primary concern because they would result in heating, voltage drops, distortion, signal loss, and a reduction in operating speed. To determine how much compressive force is necessary to assure reliably low contact resistance, we mounted the sample in our micromechanical test apparatus, to measure the contact resistance of a single pad as a function of simultaneous contact force. We found that acceptable contact could be attained with a relatively low force on the individual contact pad, which means that the performance of the assembly would be limited primarily by the uniformity of the load distribution over the

Industrial resident John Dion uses a microindenter to measure load and displacement of thin films.
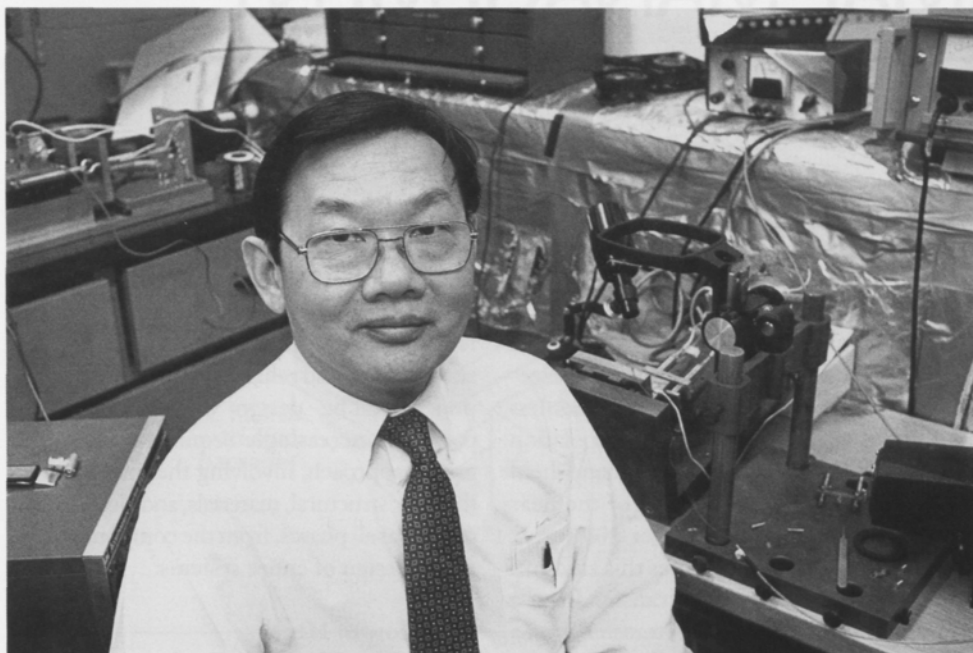
contact-pad array. This, in turn, depends on the method by which the load is applied and on manufacturing tolerances. Long-term reliability would also be affected by the relaxation of stresses in the assembly.

To investigate these factors, we studied the compressibility of the polyimide film with the aid of our out-of-plane thin-film testing apparatus. We found that even an extreme improvement in dimensional tolerances would not ensure physical contact across the entire array of pads, so long as the flex circuit is the most compliant component in the assembly. We are now exploring a range of mechanical designs intended to ensure the maintenance of a uniform contact force over the entire array. Our micromechanical testing capabilities provide the necessary data on the components of the assembly.

Continuing Research on Dense Connections

Over the years, we have found that a basic, mechanistic approach to the problems of electronic packaging has paid off. Our accumulated knowledge of flip-chip solder joints, for example, has allowed us to develop a general methodology based on a damage-integral theory that can be used for both mechanical design and reliability as-

sessment. Our experience, particularly with regard to micromechanical testing, puts us in a position to face the challenges presented by current technological trends and make substantial contributions to the field of electronic packaging.

Che-Yu Li came to the United States after earning the B.S.E. degree at the Taiwan College of Engineering in 1954, and received the doctorate from Cornell in 1960. After two years as a postdoctoral research associate, he was appointed to the faculty. During 1965-66, he was a Ford Foundation Resident in Engineering at the U.S. Steel Research Center, and he spent a two-year leave in 1969-71 at the Argonne National Laboratory. His research specialty is the mechanical properties of micromaterials, and over the past few years he has focused more and more on electronic packaging. He coauthored, with Donald P. Seraphim and Ronald Lasky of IBM, the first college textbook in the field—Principles of Electronic Packaging *(McGraw-Hill). He is currently director of both the Electronic Packaging Program and the Department of Materials Science and Engineering.*

THERMAL MANAGEMENT OF ELECTRONIC PACKAGES

by C. Thomas Avedisian and Kenneth E. Torrance

"hand-held communicators and computers of the near future could dissipate well over 100 watts"

A key limitation on the performance of electronic packages is the removal of unwanted thermal energy. The heat flux of today's highest performance electronic chips is only about twenty times less than at the surface of the sun. Extrapolation from current trends suggests that hand-held communicators and computers of the near future could dissipate well over 100 watts, and possibly up to several times this amount. Both the local rate of heat transfer from a chip and the total rate of heat transfer from a package present significant challenges to thermal engineers. At Cornell, a program to address these challenges has been underway for several years, involving research at the Sibley School of Mechanical and Aerospace Engineering undertaken in collaboration with colleagues in the Department of Materials Science and Engineering and the School of Electrical Engineering.

Since the failure rate of microelectronic circuits increases dramatically with temperature—doubling with every 20°C rise in the temperature of a device—engineers must make the best possible use of all modes of heat transfer to keep temperatures down and help ensure long life and reliability of electronic components. The design of microelectronic packages increasingly requires a fully integrated approach, involving the interaction of thermal, structural, materials, and electrical engineers at all phases, from the component level to the design of entire systems.

The Flow of Heat through an Electronic Package

In simple terms, the heat transfer in an integrated-circuit package is like an electrical-resistance network. A typical package and its thermal constituents are shown in Figure 1. Heat generated in the active-circuit plane of a semiconductor chip may be conducted either to the surrounding protective package or through solder mounting balls to the substrate of the protective package. The package, in turn, may be cooled by a heat sink mounted on top of it or by conduction through electri-
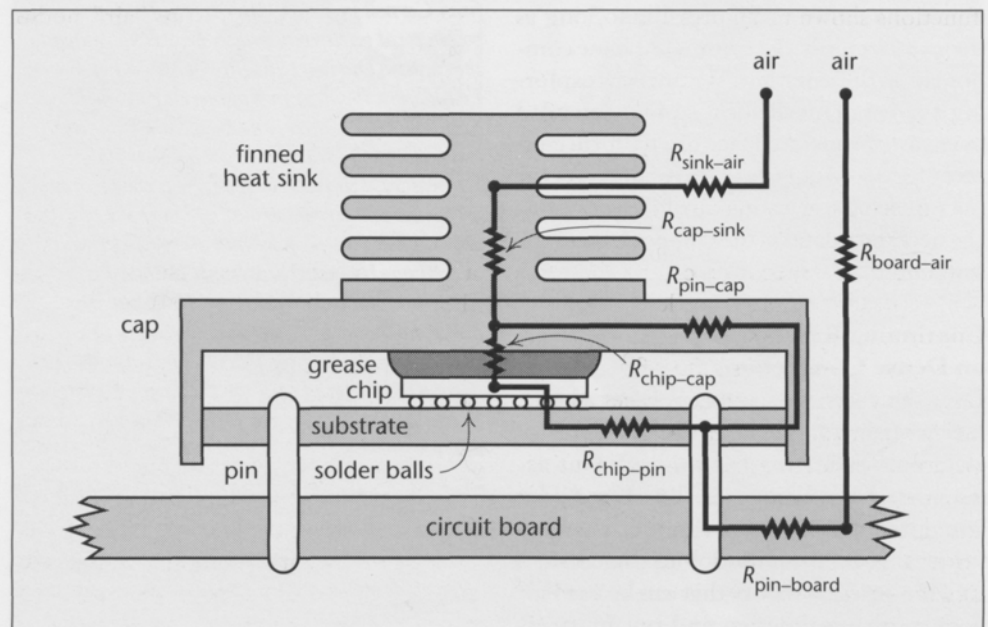

Figure 1. Chip package showing thermal resistance network. Heat produced in the chip is transported through this network to the ambient air.
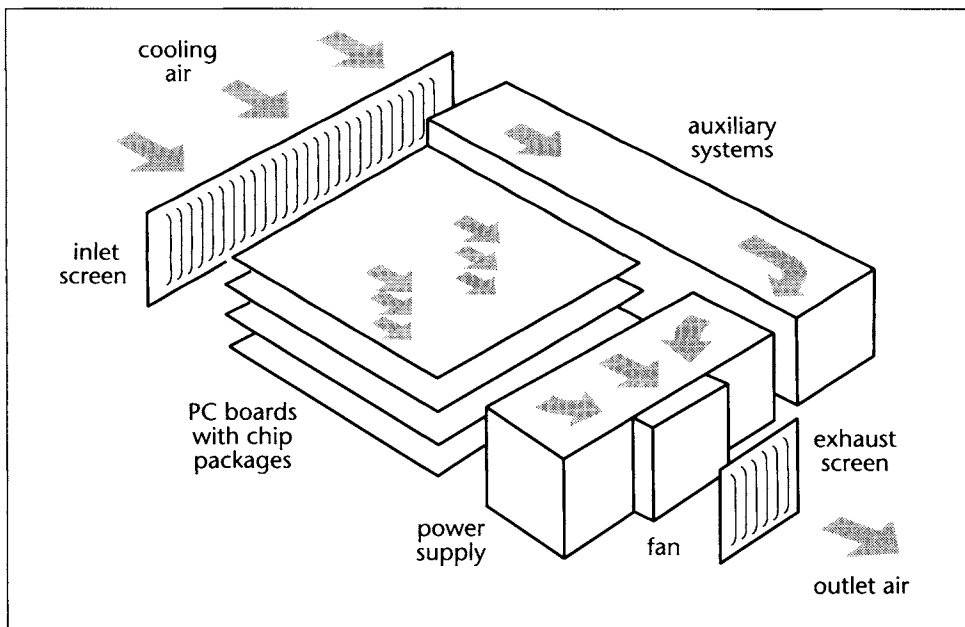
cal connection pins to the underlying circuit board. In this illustration, the heat sink and the circuit board are cooled by ambient air. Higher-performance packages typically have multiple chips, multilayer ceramic substrates, and forced air or liquid as a cooling medium.

The integrated-circuit package and board may be assembled into a further level of packaging, as in the personal computer shown in Figure 2 (where air-cooling paths are shown schematically). In the future, the functions shown in Figures 1 and 2 will be compressed into ever smaller electronic packages, with heat flows of several hundred watts. Applications involving automotive control and combustion will require such packages to operate in hostile environments, and cooling fans are likely to diminish in size. The interrelationships between the support structure and the cooling-air paths will represent a major challenge for thermal design engineers.

Resistance networks and air flow systems, such as those illustrated in Figures 1 and 2, are crucial to an understanding of the temperature distribution and heat-transfer paths in an electronic package. The chips generate thermal energy as a result of electrical losses due to switching and to the distribution of power and signal in the microelectronic circuitry. The thermal energy may be

thought of as emanating from the node located at the center of the chip in Figure 1. A network of thermal resistors in series and parallel then carries the heat through the structure to the ultimate thermodynamic heat sink, represented by the two nodes marked "air." Since heat only flows from regions of high temperature to regions of low temperature, in accordance with the Second Law of Thermodynamics (when no external work is done on the system), the highest temperatures occur at the "chip" node and the lowest at the "air" nodes, where the ambient atmosphere picks up the heat generated by the package.

Efficient Dissipation of Heat: A Challenge for Thermal Engineers

To minimize the operating temperatures within the package, it is necessary to reduce as much as possible the resistances in the thermal network, and to optimize the network geometry. The network resistors represent heat conduction paths within the solid structures and heat convection paths to the ambient air. Finite-element models are often used to estimate thermal resistances for the conduction paths. Structural materials with high thermal conductivity (aluminum, copper, aluminum nitride, silicon carbide), or thin films of very high conductivity, such as those made of diamond,

are used to lower the resistance to thermal conduction in critical regions.

The resistances due to convective heat transfer from the heat sink or the circuit board to ambient air depend on the air-flow paths in the environment surrounding the package. To estimate these resistances, which are often the largest in a thermal network, computational fluid dynamics or laboratory experiments may be used. Much effort has been directed to improving air-cooling systems, resulting in better ways to distribute air, better designs for fins that transfer heat to the air, and the development of high-performance, self-contained thermal modules, which may employ internal jets or phase-change heat transfer.

The research group focusing on the ther-mal aspects of electronic packaging has been involved in finding solutions to a wide range of design problems. Studies have ranged from direct numerical simulation of the thermal performance of packages to the design and testing of specific cooling schemes. Configurations under study (shown in Figure 3) include cooling schemes that are an integral part of an electronic packaging substrate as well as separate modules designed to be attached to microelectronic devices. Yet other work aims to develop methods for measuring the thermal properties of materials used in microelectronic packages, especially thin-film structures.

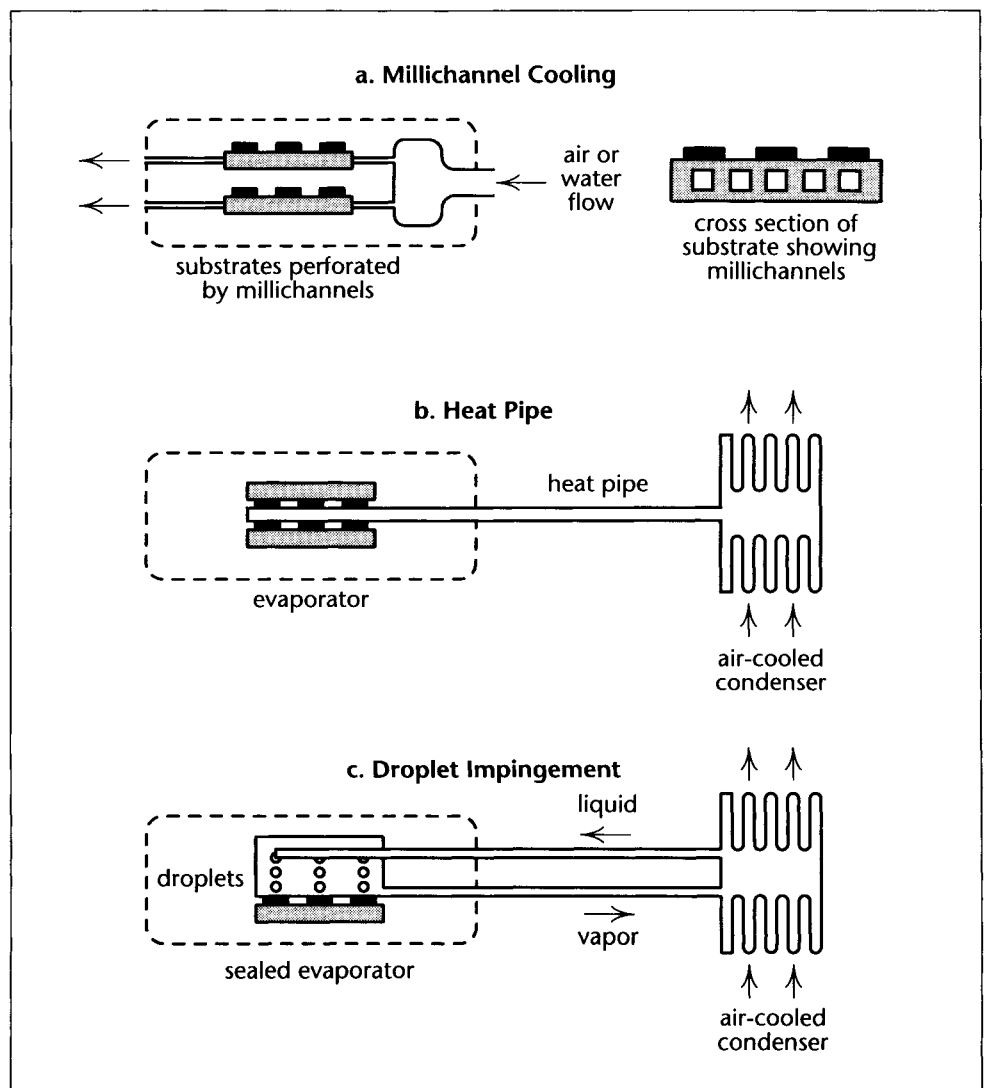One way of making cooling an integral part of the microelectronic package is illus-

Figure 3. Three approaches to cooling. Millichannel cooling allows a cooling fluid to circulate through the substrate; heat pipes conduct the heat away from the chips to a heat sink where it is dissipated; and droplet impingement focuses a cooling spray right where it is needed.
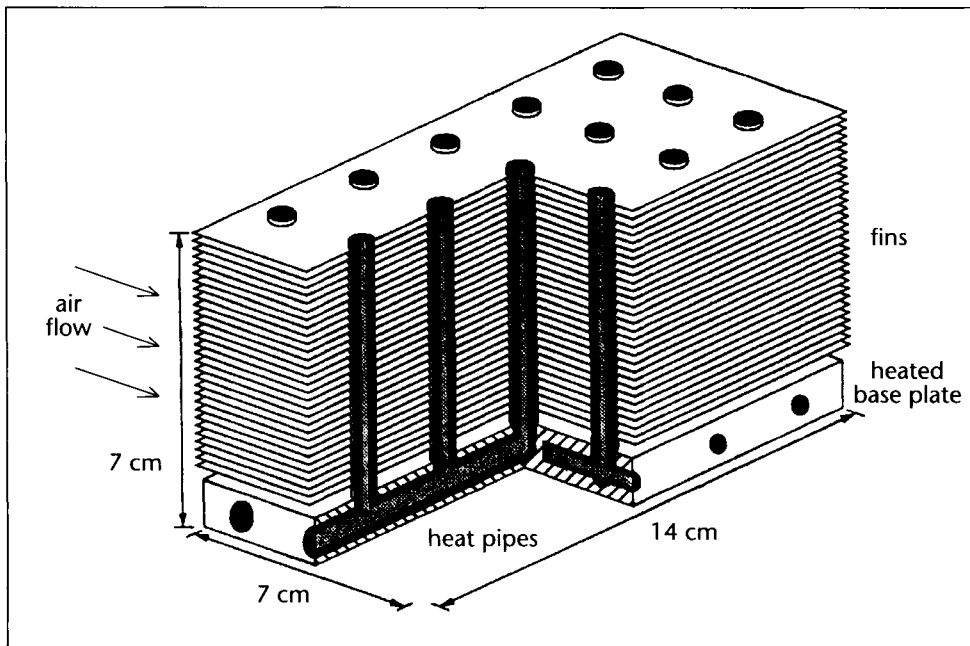
trated in Figure 3a. In this approach, air or water is pumped through millimeter-sized channels in the substrate to provide efficient, localized heat removal. This technique was studied in an undergraduate project carried out on the Cornell supercomputer by Timothy S. Fisher. Subsequent geometric optimization of the flow channels by undergraduate David E. Hall and Stephen J. Kostera, an industrial resident from IBM, has led to improved designs that can hold the temperature of chips mounted on a 10-centimeter-square substrate under 100°C. The heat-removal rate, with air cooling, is up to 1,000 watts, and with water cooling, 10,000 watts.

## Heat Pipes and Impingement Cooling

Self-contained cooling modules that may be attached to microelectronic packages that are manufactured separately make use of "heat pipes" and "impingement cooling" (see Figure 3b,c). A heat pipe is a pathway with very high thermal conductivity that leads directly from a heat source to a heat sink. The heat pipe employs a contained working fluid (water under low pressure or various fluid mixtures) that is evaporated at the heat source and condensed at the heat sink, with the condensate returning to the

evaporator section by a wicking action in the containing walls. Well-designed heat pipes have an effective thermal conductivity many times that of diamond, the material with the highest known passive thermal conductivity. This makes heat pipes attractive for enhancing the thermal conductivity of less expensive materials such as copper, silicon, or aluminum nitride.

Experimental heat pipes developed by graduate student Mark North support finned arrays that are cooled by ambient air (see Figure 4). Testing in a specially constructed wind tunnel revealed heat-removal rates of nearly 1,000 watts for surface temperatures under 100°C, which is often considered the limit of reliable operation for semiconductor chips. The prototype measures about 7 by 7 by 14 centimeters, but much smaller versions are currently under development. Such self-contained and extensible modules are being considered for use in future high-performance workstations.

Impingement cooling involves heat transfer through direct contact between a jet of cool fluid and a hot surface. Current research includes studies of air jets, liquid sprays, and droplets. The way droplets collapse against an obstacle, with a jet of liquid spreading rapidly at the surface, greatly

Figure 5. The evolution of droplet shape during impact on a stainless-steel surface. The rapidly expanding bulge increases the contact area, making droplets unexpectedly efficient at dissipating heat.
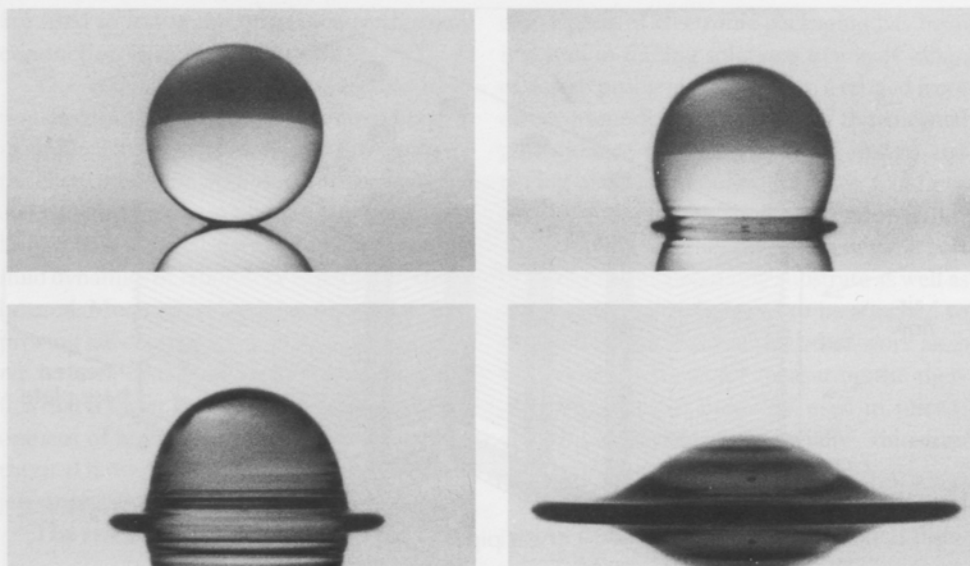
enhances their ability to dissipate heat. Some of the phases of liquid-droplet impingement are illustrated in Figure 5.

Evaluating the Thermal Properties of Microelectronic Materials

Accurate thermal modeling of electronic packages at all levels—but especially in the immediate neighborhood of high-performance microelectronic circuits—depends on a detailed knowledge of the thermal properties of materials. The increasing use of thin-film materi-

als (often less than one micron thick) raises a host of new issues, for if a film is thin enough, its properties may differ significantly from bulk values for the same material. Molecular processes that would otherwise be inconsequential can exert a profound influence on heat conduction when a film is sufficiently thin. The internal structure of thin films is also important and can create anisotropic effects so that thermal conductivity is greater in one direction than another. The coefficient of thermal expansion may also be affected.

Figure 6. Measuring the thermal diffusivity of thin films. The sample is heated with a laser beam. A probe beam skimmed along the surface is deflected by the hot gas it encounters. The direction and degree of deflection can be interpreted to calculate the thermal diffusivity.
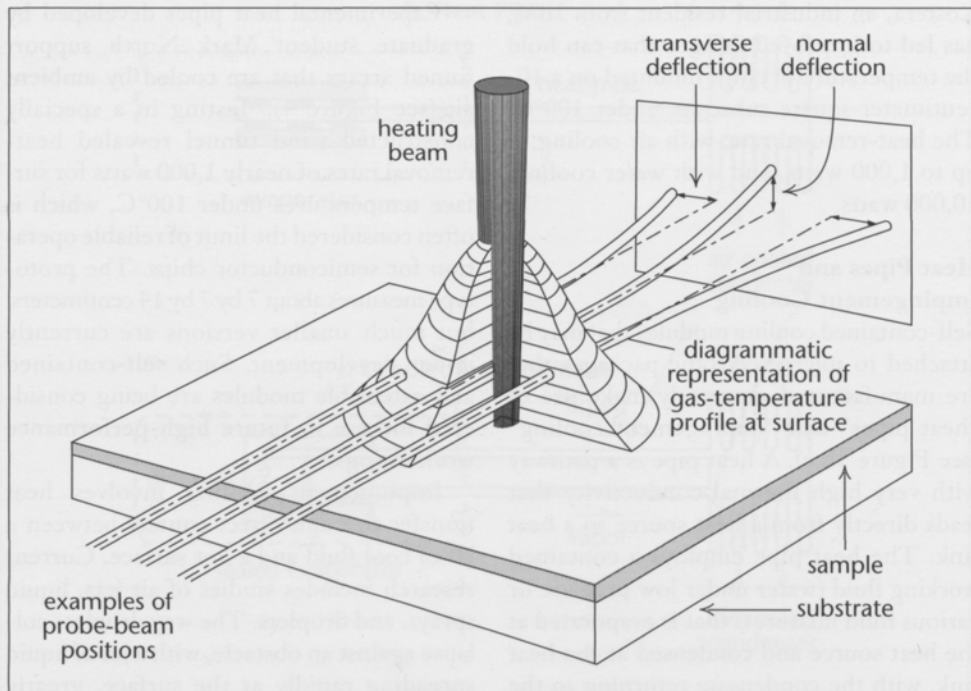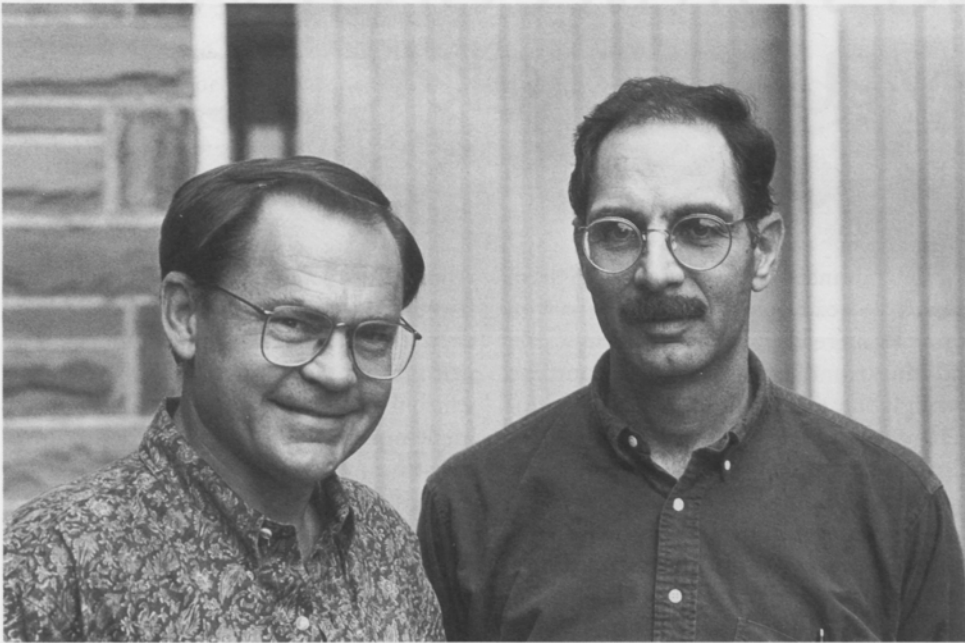
It is difficult to measure the thermal diffusivity of thin-film materials because they do not lend themselves to conventional methods, which make use of thermocouples. To overcome this difficulty, graduate student Yoke Chung is working on a technique (see Figure 6) that will measure the deflection of a laser beam that is skimmed past a heated surface. The amount of deflection makes it possible to determine the anisotropic thermal conductivity of the solid through the use of a model that takes into account the conduction processes in the thin film, the substrate, and the air above the film.

With the continuing trend toward miniaturization, thermal design engineers will be increasingly called upon to integrate a thermal solution with an electrical configuration. This process is facilitated by looking at microelectronic packaging as a field in which engineers from various disciplines work toward a common goal. At Cornell, this process has been promoted through the Industry–Cornell University Alliance for Electronic Packaging, as well as through collaborative research projects among faculty in several departments of the College of Engineering under the sponsorship of the Semiconductor Research Corporation, the National Science Foundation, and other organizations.

C. Thomas Avedisian and Kenneth E. Torrance are both professors in the Sibley School of Mechanical and Aerospace Engineering.

Avedisian has focused his research efforts primarily on experimental aspects of heat transfer and combustion. After an undergraduate career at Tufts and a master's degree from MIT, he earned the doctorate from Princeton and joined the Cornell faculty in 1980. He received a Presidential Young Investigator award in 1985 and spent a sabbatical at the National Institute of Standards and Technology in 1988. In 1991 he was elected a fellow of the American Society of Mechanical Engineers.

Torrance's research interests are heat transfer, fluid mechanics, and computer graphics. In addition to electronic packages, he has studied boiling, natural convection, destructive fires, and geothermal flows. Educated at the University of Minnesota (Ph.D., 1966), he joined the Cornell faculty in 1968. He spent a sabbatical leave in 1974–75 at the National Center for Atmospheric Research in Boulder, Colorado. He is a fellow of the American Society of Mechanical Engineers and a member of the Combustion Institute, the American Geophysical Union, and the American Physical Society.

"thermal design engineers will be increasingly called upon to integrate a thermal solution with an electrical configuration."

SIMULATING SYSTEM CONSTRAINTS IN COMPUTER PACKAGING

by J. Peter Krusius

"we are trying to achieve a better understanding of the way the physical structure of a computer affects its functionality, performance, cost, and reliability."

A dvances in miniaturization have already shrunk computers to a mere fraction of their former size, and this trend is expected to continue through the next decade. Such a radical change in scale implies a series of other systemic changes that require a complete rethinking of the physical structure of all computers, including supercomputers, mainframes, workstations, personal computers, notebooks, and hand-held units.

A research group that I lead is examining the impact of changing constraints on the packaging of computer systems with the aid of computer simulation. Graduate students who have been involved in this work during the past academic year are Lipeng Cao, Bruce Hahne, Henry Lin, and David O'Brien. Together, we are trying to achieve a better understanding of the way the physical structure of a computer affects its functionality, performance, cost, and reliability. To do this, we build a large set of linked models describing every conceivable characteristic of the system, whether physical or functional, and then simulate their interaction. The program we have developed is called AUDiT, for Automated Design Trade-off Simulator. Similar methods of system simulation have been applied to complex problems involving airline traffic, urban infrastructure, weather, and planetary ecosystems. (The computer game SimEarth allows players to design and manage entire planets.) What we do follows the same principles, although the content differs: We use computers to simulate computers.

A Demonstration of the Technique Using a Model Computer

To illustrate how we study the system constraints of physical structure—or, more precisely, of packaging architecture—I will describe the thermal constraints on engineering workstations patterned after the IBM RS/ 6000. This machine has been designed as a

reduced-instruction-set computer (RISC) and has nine silicon integrated-circuit chips in its central computational complex. This chip set performs all the computational functions of which the computer is capable. The chips are implemented in a complementary metal-oxide-semiconductor (CMOS) circuit technology with a 1-micron minimum feature size. CMOS is currently the dominant integrated-circuit technology, and it is expected to maintain this position throughout the 1990s.

Each of the chips has a specific function: an instruction cache unit (ICU) stores instructions temporarily; a fixed-point unit (FXU) executes commands applied to integer numbers; a floating-point unit (FPU) executes commands on floating-point numbers; four data cache units (DCU) store temporary data; a storage control unit (SCU) controls the storage of data in the temporary and permanent memories of the computer; and an input/output interface unit (I/O) controls all input/output operations (see Figure 1).

The performance of this RISC computer is limited primarily by a single signal path, called the critical path, which runs from the FXU to one of the DCUs. Data travels on this path when the FXU chip reads it from or writes it back to the temporary storage (DCU). It
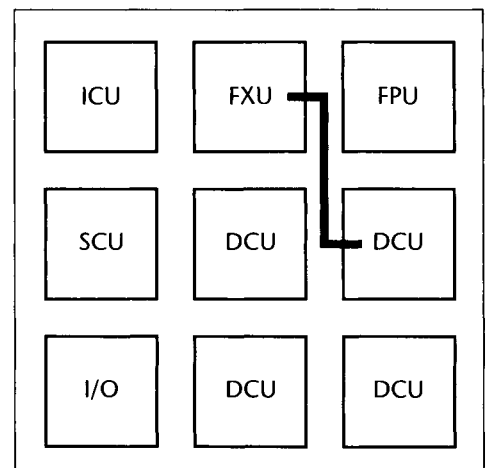

Figure 1. Chip set for a model RISC workstation. The nine chips are attached to a substrate with an array of solder bumps. The heavy black line shows the critical path, whose length limits the computer's speed.
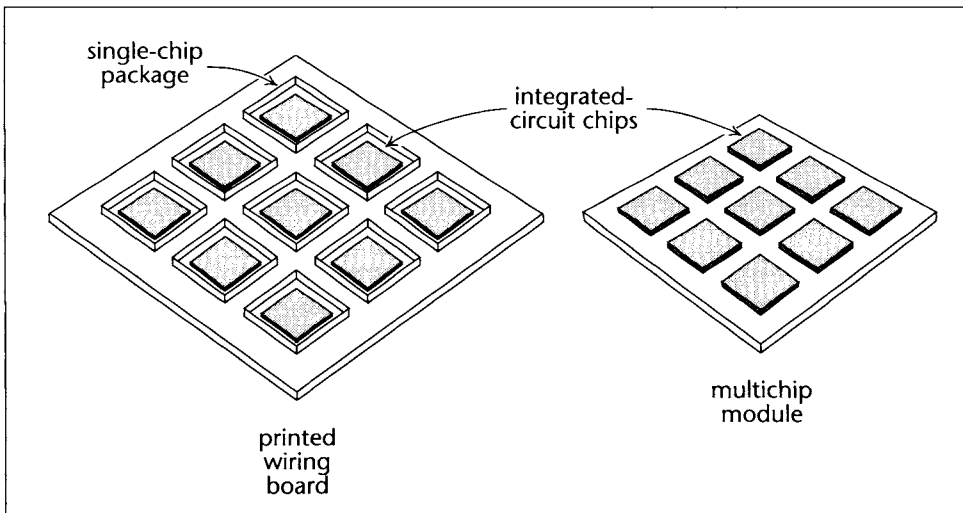
Figure 2. Competing architectures for the RISC workstation chip set. Each chip on the printed wiring board is in its own package, while all the chips on the multichip module are in a single package.

should be noted that the critical path runs on two chips (FXU, DCU) and on the packaging medium between the chips.

For purposes of demonstration, we will consider two different ways of packaging this chip set. The first alternative involves placing each chip in its own package, which must provide the required signals, electric power, and cooling functions. The single-chip packages (SCPs) are then placed on a printed wiring board (PWB) in a three-by-three array as shown in Figure 2. The board provides all signal wires (interconnects) and electrical power leads that are required between the chips. The second alternative involves placing all chips on a single substrate, called a multichip module (MCM), in a three-by-three array with no intervening package walls. The whole MCM is placed in its own package.

MCMs differ in the combination of materials from which they are made. We will consider three possibilities:

1. tungsten metal interconnects laminated with a ceramic material such as aluminum nitride into a multilayer ceramic structure (MCM-C)

2. copper metal interconnects deposited on organic polyimide insulator layers in a multilayer structure on top of a ceramic substrate (MCM-D)

3. copper interconnects laminated with organic layers into a multilayer organic structure (MCM-L)

Key characteristics for each of these three interconnect technologies are shown in Table 1. Values given for the line width and line space of metal interconnects reflect current manufacturing capability. Permitivity depends on the dielectric between the metal lines and is determined by the specific ceramic or organic materials used. Commercial MCM workstations of this type are not yet on the market.

Results of the Simulation: Size and Performance

AUDiT was used to generate key characteristics of the RISC workstation under discussion, implemented according to the four packaging architectures outlined above. Of particular interest are the relationships between size, performance, and cooling.

The relationship of system size to packaging efficiency and cycle time is given in Table

A Comparison of Four Substrates				
	SCP/PWB	MCM-C	MCM-D	MCM-L
Line width	150 μm	100 μm	12 μm	100 μm
Line spacing	225 μm	100 μm	16 μm	125 μm
Layers	4	4	4	4
Permitivity	4.8	8.9	3.5	3.9

Table 1. Key parameters vary depending on the substrate used for the interconnect lines between the chips. The four packaging architectures are described in the text.

A Comparison of Four Packaging Architectures				
	SCP/PWB	MCM-C	MCM-D	MCM-L
PWB or MCM size (cm^2)	1,672	205	17.2	100
Packaging efficiency (%)	1.03	8.4	99.9	17.2
Interchip path length (cm)	19.3	6.75	1.96	4.72
Cycle time (ns)	16.1	12.1	7.36	8.03
Overall power density (W/cm^2)	0.017	0.082	1.34	0.27

Table 2. Performance, system size, and packaging efficiency vary according to the implementation of the model workstation.

2. System size is the area of the printed wiring board or the multichip module (which determines the external size of the computer). Packaging efficiency is the ratio of the total area of the silicon chips to the system size. The cycle time, which is the usual measure of the speed of a computer, is the time it takes for a signal to travel the full length of the critical path. The shorter the cycle time, the more instructions the computer can process in a given interval and the faster the computer.

All MCM-based implementations are much smaller than the PWB with single-chip packages because the interconnect line pitch is finer and no package structures intervene between the chips. Consequently, the length of the critical path is greatly reduced and the cycle time is less than half as long (see Figure 3).

The Dissipation of Heat in Different Packaging Strategies

When executing the instructions of a stored program, computer chips generate heat, which must be dissipated for them to function reliably. If chips are run at temperatures above 85°C for extended periods, their lifetime is shortened considerably. Cooling strategies are a major consideration in computer design, as indicated in the previous article.

Several different cooling methods are analyzed in the present exposition. All techniques employ a forced fluid, which flushes the exposed surfaces of the packages. The fluid may cool packages either directly or via heat sinks attached to their upper surface. Heat sinks are formed from thermally conductive metal, typically aluminum or copper, and their function is to increase the area of the package so that heat can be removed more effectively. We assume, for purposes of illustration, that heat sinks are made of aluminum and that the fins are 20 millimeters high. Two coolants, air and fluorocarbon, are modeled.

Overall power densities and chip temperatures for the packaging architectures under analysis demonstrate the energy-balance con-
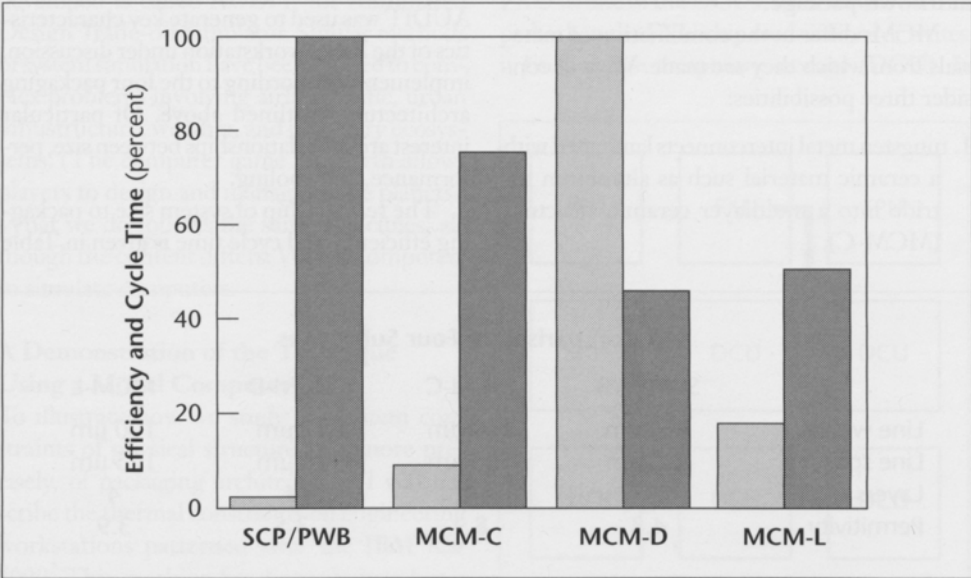
Figure 3. Efficiency and cycle time for a model workstation implemented with different packaging architectures. Results have been normalized so that the longest cycle time (dark gray) and highest packaging efficiency (light gray) equal 100 percent.
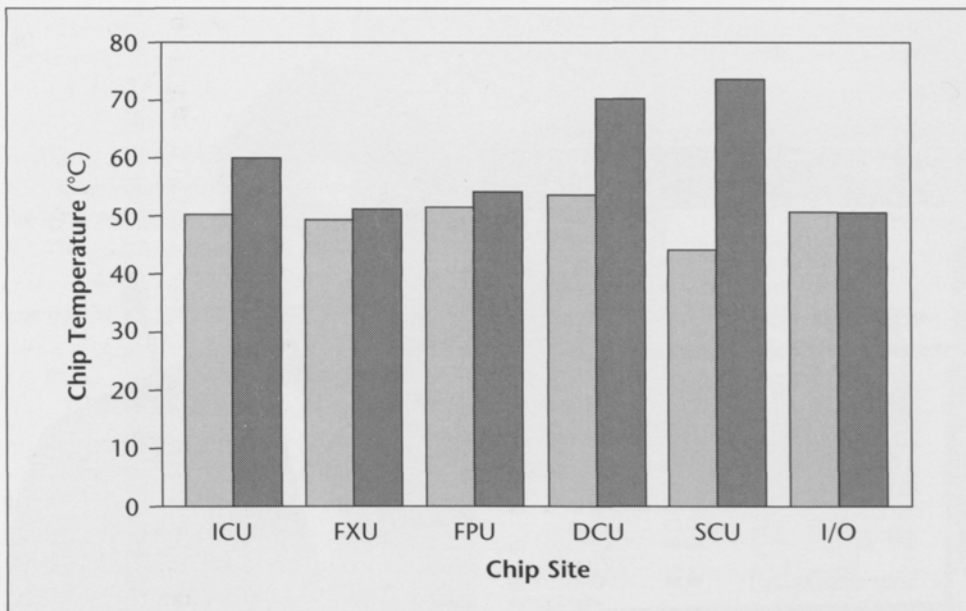
Figure 4. Chip-temperature maps for two packaging configurations. The light gray bars show the temperature of individual chips in the SCP/PWB architecture cooled by direct forced air, but without heat sinks. The dark gray bars show the temperature of the same chips in the McM-D architecture, cooled by forced air *with* heat sinks. Both alternatives remain under the 85°C reliability ceiling.

straint. Power density is the ratio of the electric power dissipated by the circuits to the total area of the system. Chip temperatures are computed by AUDiT using two-dimensional thermal network models describing heat removed via the conduction and convection mechanisms. The inlet temperature of the coolant is taken to be 27°C—the temperature of office air on a hot day. Maximum and minimum chip temperatures for each packaging architecture and cooling technology are shown in Table 3. Thermal maps showing the temperature of individual chips for single-chip packaging and multichip modules are given in Figure 4.

Without tall heat sinks, direct forced air cannot cool organic MCMs to chip temperatures less than 85°C. Indeed, chip temperatures may rise to 223°C—far in excess of the desired ceiling. But forced air with heat sinks or forced liquid fluorocarbon without heat sinks can drop all chip temperatures into the acceptable range. The combination of forced air and heat sinks is the most practical cooling method, commonly employed in office environments. It is able to cool the model workstation even at cycle times of 8 nanoseconds, which are not yet available on the market.

The maximum heat flux produced by commercial workstations is 30 watts for Digital Equipment's Alpha chip, which measures 16.8 by 13.9 millimeters. This corresponds to a chip-level power density of 12.8

Power Density and Chip Temperatures

	SCP/PWB	MCM-C	MCM-D	MCM-L
Overall power density (W/cm^2)	0.017	0.082	1.34	0.27
Direct forced air:				
Max. chip temperature (C)	53.6	39.6	223	131
Min. chip temperature (C)	44.1	46.6	153	63.6
Forced air with heat sinks:				
Max. chip temperature (C)	36.5	33.2	73.1	61.1
Min. chip temperature (C)	33.1	30.6	50.3	45.8
Direct forced fluorocarbon:				
Max. chip temperature (C)	33.6	31.6	47.4	48.0
Min. chip temperature (C)	31.2	29.7	36.5	34.3

Table 3. Power density and chip temperatures for different packaging architectures vary with different types of cooling.

watts per square centimeter, which is within a factor of one hundred from the largest cooling flux ever demonstrated for temperatures below 100°C—about 1,000 watts per square centimeter.

Future Research on Optimal Packaging

The AUDiT-based simulations described here show quantitatively the relationship of computer performance to packaging density and energy balance. It is clear that these and other considerations must be incorporated into future computers early in the design process, together with more traditional issues such as functional architecture, instruction set, and cache access.

Continuing work in my research group will focus on placement optimization and system partitioning, with attention to both physical and functional factors. The study of placement optimization will help determine where in the system circuits should be placed in order to meet specified levels of performance without violating constraints imposed by size, form, energy balance, electrical noise, and the costs of manufacturing and assembly. Since the descriptions of packaging architecture used in AUDiT extend from on-chip functional units to the full system, placement optimization covers not only chips and packages, but also functional units within chips. These functional units can be moved from one chip to another, even when the chips are in different packages. Issues related to chip integration, chip-to-package tradeoffs, and partitioning of parallel computers may thus be studied in a systematic fashion. We hope our optimization studies will contribute to the design of packaging architectures for all kinds of formats, from compact modules to hand-held units, notebooks, desktops, PCs, workstations, and large parallel computers.

J. Peter Krusius is a professor in the School of Electrical Engineering. After receiving a doctorate in electron physics from the Helsinki University of Technology in 1975, he conducted research at the Institute of Physics of the University of Dortmund in Germany, the Electron Physics Laboratory at Helsinki University of Technology, and the Semiconductor Laboratory at the Technical Research Center of Finland. He first came to Cornell on a Fulbright fellowship and joined the faculty in 1981. His research in solid-state electronics focuses on ultrahigh density nanoelectronics, femtosecond carrier processes in semiconductor heterostructures, and integration and packaging of high-speed computers. He is a member of the Institute of Electrical and Electronics Engineers, the Materials Research Society, and the American Physical Society.

Six members of the College of Engineering faculty retired at the end of the 1992–93 academic year. They were Franklin K. Moore, Edwin L. Resler, and Kuo-King Wang, of the Sibley School of Mechanical and Aerospace Engineering; Tor Hagfors, of the School of Electrical Engineering; Mark S. Nelkin, of the School of Applied and Engineering Physics; and Jack E. Oliver, of the Department of Geological Sciences.

Moore

■ *Franklin K. Moore* has been named the Joseph C. Ford Professor of Mechanical Engineering, Emeritus. A specialist in fluid mechanics, turbomachinery, and heat transfer, Moore has played a significant role in the development of aerospace engineering.

After receiving the B.S. and Ph.D. degrees from Cornell, Moore was an aeronautical research scientist at the National Advisory Committee for Aeronautics, which later became the National Aeronautics and Space Administration (NASA). He then directed the Aerosciences Division of the Cornell Aeronautics Laboratory and headed the former Department of Thermal Engineering from 1965 to 1973. He served on the Aeronautics and Space Engineering Board of the National Research Council and spent sabbatical years at the General Electric Company and at NASA, which honored him with its Distinguished Scientific Achievement Medal. He is a member of the National Academy of Engineering and a fellow of the American Institute of Aeronautics and
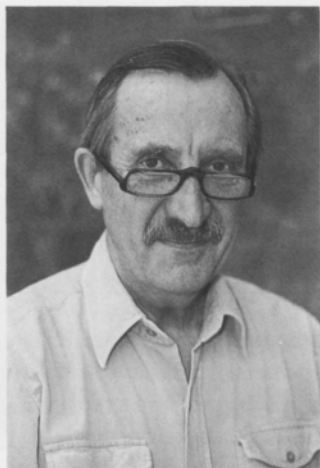
Astronautics and the American Society of Mechanical Engineers.

■ *Edwin L. Resler, Jr.* has been named the Joseph Newton Pew, Jr. Professor of Engineering, Emeritus. He was in the first class to enter Cornell's newly established Graduate School of Aeronautical Engineering (after an undergraduate career at

Notre Dame), and he received the Ph.D. in 1951. Except for a period at the University of Maryland's Institute for Fluid Dynamics and Applied Mathematics (1952–56), he has remained at Cornell, playing a leading role in aerospace engineering.

A researcher with wide-ranging interests, Resler has been involved in studies of wave engines, shock tubes, magnetohydrodynamics, and ferrohydrodynamics. He has made substantial contributions to reducing the sonic boom of jet aircraft and the pollution caused by automobile engines, and he holds a number of patents. In addition, he directed the Graduate School of Aerospace Engineering from 1963 to 1972, and after the merger that established the Sibley School of Mechanical and Aerospace Engineering, he served as director of that school for five years.

Resler has been a consultant to many industries; an editor of *Astronautics*, the *AIAA Journal*, and *Physics of Fluids*; and chair of NASA's Advisory Committee for Fluid Mechanics and of the American Rocket Society's Magnetohydrodynamics Committee. He is a fellow of the American Institute of Aeronautics and Astronautics.

■ *Kuo-King Wang* has been named the Sibley Professor of Mechanical Engineering, Emeritus. An internationally renowned expert on manufacturing processes, he founded and directed the Cornell Injection Molding Program, which has done much to put the molding of plastics on a rational scientific footing.

After earning the B.S. degree at the National Central University in his native China, Wang worked for shipbuilding companies in

Resler

Wang

Hagfors
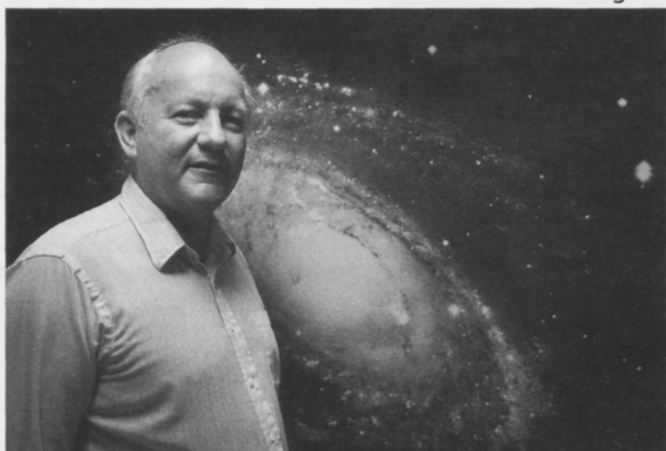
Shanghai and Taiwan for thirteen years, serving in several different capacities, from plant and design engineer to supervisor of planning and scheduling. He came to the United States in 1960, and after a year supervising a project for the United Tanker Corporation, he earned a master's degree at the University of Wisconsin. He then spent four years in process development at Walker Manufacturing Company before returning to the University of Wisconsin for a doctorate.

When Wang joined the Cornell faculty in 1970, he brought with him eighteen years of industrial experience, and his ability to broker relations between industry and academia has been a key to the success of his injection molding program. He has received several prestigious awards; he is a fellow of the American Society of Mechanical Engineers and the Society of Manufacturing Engineers, and a member of the National Academy of Engineering.

■ *Tor Hagfors,* who directed the National Astronomy and Ionosphere Center, has also been named professor, emeritus. An able administrator as well as a specialist in radar and radio astronomy and ionospheric physics, Hagfors has managed some of the world's leading research facilities in these fields.

After receiving the doctoral degree from the University of Oslo in his native Norway, Hagfors worked for the Norwegian National Defense Research Laboratory. From 1966 to 1969 he directed the Jicamarca Observatory near Lima, Peru. From 1971 through 1973, he was director of operations at the Arecibo Observatory in Puerto Rico. He was appointed professor at the University of Trondheim in 1973, and in 1975 he became director of the European Incoherent Scatter Radar Observatory. He came to Cornell in 1982 as a member of both the Department of Astronomy

and the School of Electrical Engineering. He is a fellow of the International Union for Radio Science, from which he received the 1987 van der Pol gold medal.

■ Also named professor, emeritus, was *Mark S. Nelkin* of the School of Applied and Engineering Physics. A theoretical physicist by inclination, Nelkin contributed significantly to an understanding of neutron thermalization and thermal spectra. He became interested in phenomena that exhibit "a subtle interplay between ordered and chaotic behavior," particularly voltage fluctuations in solid-state devices and fluctuating velocity in turbulent fluid flow.

Nelkin received the B.S. from MIT and the Ph.D. from Cornell. After working for two years at the Knolls Atomic Power Laboratory in Schenectady, New York, and for five years at the General Atomic Division of General Dynamics in San Diego, California, he returned to Cornell in 1962, and joined the faculty. Dur-

ing academic leaves he has been a visiting professor or visiting scientist at the University of Paris, Harvard University, the College de France, the National Bureau of Standards, the University of Paris VI, and the Courant Institute of Mathematical Sciences at New York University. He is a fellow of the American Physical Society.

■ *Jack E. Oliver* has been named the Irving Porter Church Professor of Engineering, Emeritus. He came to Cornell in 1971 as first chair of the reorganized Department of Geological Sciences (which was given a position in the College of Engineering), and presided over its growth as a department devoted to research in the then-new paradigm of plate tectonics, with special attention to the processes involved in the building of the continents.

Before coming to Cornell, Oliver served for sixteen years on the faculty at Columbia University, where he had earned the B.A. and Ph.D degrees. He directed the department at Cornell for ten years,

Nelkin
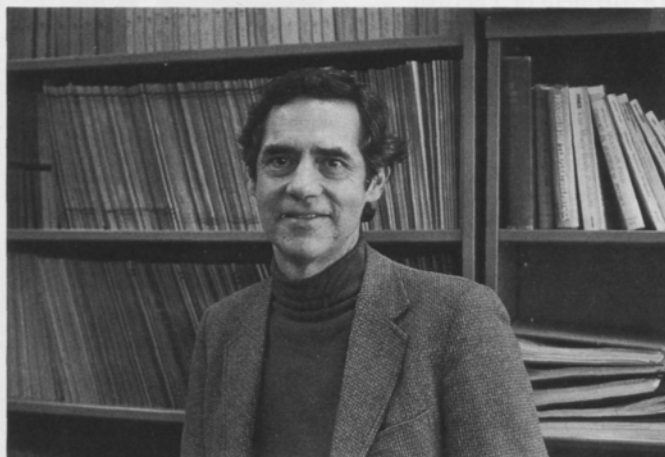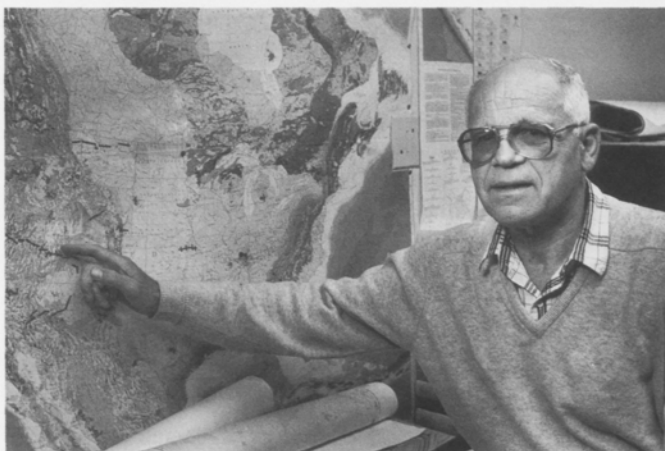
and then directed the associated Institute for the Study of the Continents, which he founded, for five years. He served as president of both the Seismological Society of America and the Geological Society of America (GSA). He is a member of the National Academy of Sciences and a fellow of the American Geophysical Union, the GSA, and the American Association for the Advancement of Science. He has served as a consultant to various government agencies and chaired the U.S. Geodynamics Committee of the National Research Council. He has received a number of awards, including the Virgil Kauffman Gold Medal from the Society of Exploration Geophysics.

A panel of distinguished geologists assembled for festivities that took place August 28 in honor of Oliver's retirement included Frank Press, former president of the National Academy of Sciences; Charles L. Drake, a former member of the President's Council of Advisors on Science and Technology; and Frank H. T. Rhodes, president of Cornell University.

Three new members have joined the faculty of the College of Engineering.

■ New in the Department of Geological Sciences is *Kodjopa Attoh,* who joins the faculty as an associate professor. Born in Ghana, he attended the University of Ghana in Legon, receiving the B.Sc. degree in 1968. He earned the M.S. degree at the University of Cincinnati in 1970, and the Ph.D. at Northwestern University in 1973. He remained at Northwestern as a postdoctoral fellow during the 1973–74 academic year, and then returned to Ghana as a lecturer at the Univer-

sity of Ghana. His research interests involve Precambrian geology and metamorphic petrology; the opportunity to compare the greenstone belts of Canada with those in West Africa led him to take a position as visiting scientist with the Geological Survey of Canada in Ottawa in 1978–80. He then joined the faculty of Hope College in Holland, Michigan, where he chaired the geology department from 1985 through 1989. He is a member of the Geological Society of America, the American Geophysical Union, and Sigma Xi.

■ *Iain D. Boyd* began his appointment as an assistant professor in the Sibley School of Mechanical and Aerospace Engineering last January. Born in Paisley, Great Britain, he earned the B.Sc. degree in 1985 at the University of Southampton, where he majored in mathematics. Graduate study in aeronautics and astronautics followed at the same institution, where he received the Ph.D. degree in 1989. He

then worked as a research scientist at NASA's Ames Research Center until coming to Cornell. Boyd's research interests include gas dynamics, nonequilibrium flows, and numerical methods. He is an expert in the application of particle simulation techniques to problems involving nonequilibrium gas dynamics. Applications include aerodynamics of hypersonic vehicles and rocket propulsion on spacecraft. He is a member of the American Physical Society and the American Institute of Aeronautics and Astronautics.

■ *Thorsten von Eicken* has joined the Department of Computer Science as an assistant professor. After an undergraduate major in computer science at the Federal Institute of Technology in Zürich, Switzerland, where he became a diplomate in 1987, von Eicken spent nine months as a member of the technical staff at AT&T Bell Laboratories Computing Research Center in Murray Hill, New Jersey. He then undertook graduate study at
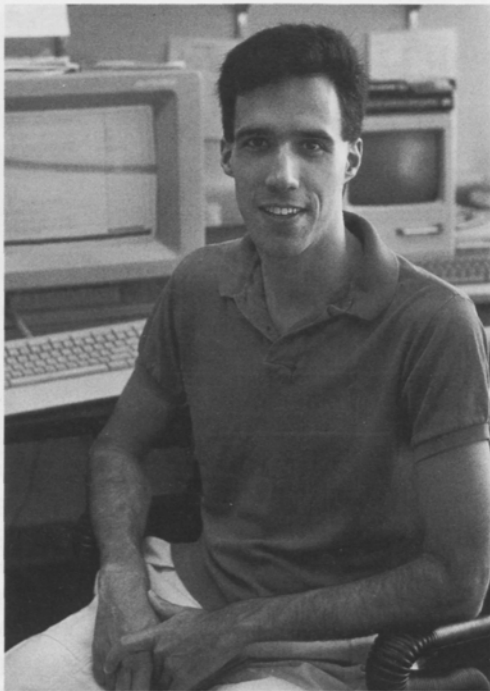
the University of California at Berkeley, where his research involved developing efficient communication architectures for multiprocessors. He returned to AT&T Bell Laboratories as a student intern in the summer of 1989, and spent a month as a visiting scientist at the Thinking Machines Corporation in Cambridge, Massachusetts, in 1992. He received an outstanding paper award at the 19th International Symposium on Computer Architecture in May 1992. He is a member of ACM SIGARCH and SIGPLAN, and the IEEE Computer Society.

■ *Daniel P. Huttenlocher,* an assistant professor in the Department of Computer Science, has won three awards for his teaching. Last spring he won the Excellence in Engineering Teaching Award, which is given annually by the Cornell Society of Engineers and Tau Beta Pi. He also won the Russell Distinguished Teaching Award from the College of Arts and Sciences. He is the first professor to have won the highest teaching award from two colleges, a feat made possible by the fact that computer science has departmental status in both arts and engineering. But this noteworthy achievement was eclipsed this fall, when the Council for the Advancement and Support of Education (CASE) selected Huttenlocher as New York State Professor of the Year.

Huttenlocher joined the Cornell faculty in 1988 after receiving the doctorate from MIT. A respected researcher as well as a teacher, he won a coveted Presidential Young Investigator award in 1990. His specialty is computer vision, and one of his accomplishments has been the establishment of a robotics and vision laboratory for undergraduate and graduate instruction. He was nominated for the Case Award by Professor David Gries, who says, "He has complete command of the classroom. His enthusiasm for what he is teaching is infectious."

Four schools or departments are under new leadership.

■ *William L. Olbricht* has taken over from Claude Cohen as director of the School of Chemical Engineering. A specialist in fluid mechanics, his research has involved the movement of blood cells through capillaries and the motion of multiphase fluid systems through porous media. He came to Cornell in 1980, after finishing his graduate studies at the California Institute of Technology. He is a member of the American Institute of Chemical Engineers and the Society of Rheology.

■ *Robert L. Constable* is acting chair of the Department of Computer Science while Juris Hartmanis is on sabbatical leave. Constable joined the Cornell faculty in 1968, after receiving the doctorate from the University

Olbricht

Constable
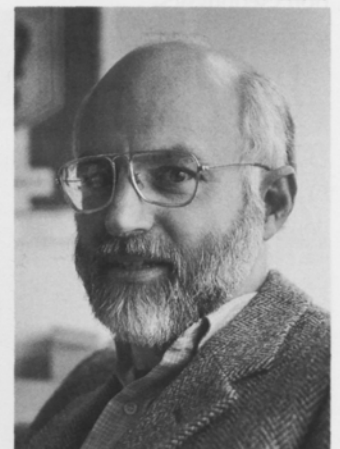
of Wisconsin. He has devoted his career to developing computer systems to make the formalization of mathematics feasible and useful, including PL/CV, PRL, and Nuprl. He is a member of the Association for Symbolic Logic and the Association for Computing Machinery. In 1990 he won a Guggenheim fellowship.

■ *Che-Yu Li,* who has succeeded Jack M. Blakely as director of the Department of Materials Science, is a specialist in the mechanical properties of materials. He earned the doctorate at Cornell, and after two years as a postdoctoral research associate, he became a member of the faculty. He spent a two-year leave at the Argonne National Laboratory, and he has worked closely with industrial groups on a variety of topics. He also directs the Electronic Packaging Program.

■ *David A. Caughey* has taken over the reins of the Sibley School of Mechanical and Aerospace Engineering from Franklin K. Moore, who was acting director for the

past year. Caughey earned the doctorate at Princeton University and joined the Cornell faculty after a year as an exchange scientist at the Soviet Academy of Sciences in Moscow, and four years at the research laboratories of the McDonnell Douglas Corporation. His research has focused on the development of computational techniques for the solution of problems in compressible aerodynamics. He received the 1977 Excellence in Engineering Teaching Award, and he served as acting director of the Center for Theory and Simulation in Science and Engineering (the Theory Center) in 1988-89.

■ *Michael S. Isaacson* is the new associate dean for research and graduate studies, replacing S. Leigh Phoenix, who stepped down in June. Isaacson is a professor in the School of Applied and Engineering Physics, where he has been involved in research on electron-optical instrumentation and design, near-field optics, nanolithography and mesoscopic physics. A graduate of the University of Illinois (B.S.) and the University
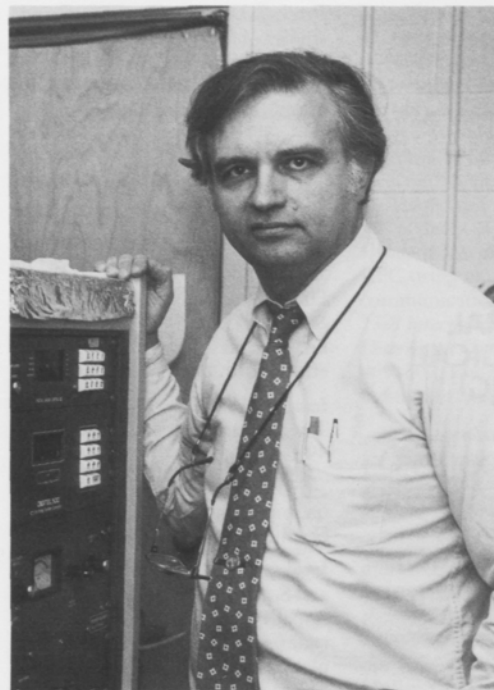
of Chicago (S.M., Ph.D.), Isaacson joined the Cornell faculty in 1979 after serving as a staff scientist in the biology division at the Brookhaven National Laboratory and as an assistant professor in the Department of Physics at the Enrico Fermi Institute and the College of the University of Chicago. He has been an Alfred P. Sloan Foundation faculty fellow and was awarded the Burton Medal by the Electron Microscopy Society of America. He has also received an Alexander von Humboldt Senior Scientist Award. He is an associate editor of *Ultramicroscopy,* and has served on the editorial boards of several other journals. Currently, he is president of the Microscopy Society of America.

Li
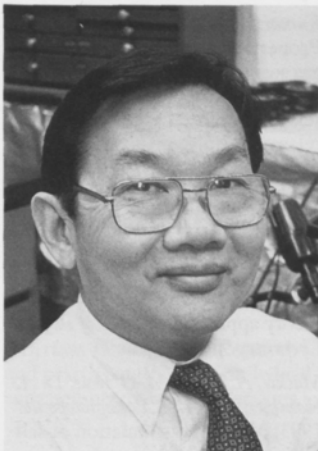
Caughey

Current research activities in the Cornell College of Engineering are represented by the following publications and conference papers that appeared or were presented during the four-month period January through April 1993. (Earlier entries omitted from previous Quarterly *listings are included here with the year of publication in parentheses.) The names of Cornell personnel are in italics.*

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Ralph, D. C., K. S. Ralls, and *R. A. Buhrman*. 1993. Ensemble studies of non-linear conductance fluctuations in phase coherent samples. *Physical Review Letters* 70:986–89.

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___. 1993*c*. Liquids and liquid mixtures. Paper read at Symposium on Statistical Mechanics of

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___. 1993*d*. Molecular simulation of fluid phase equilibria. *Pure and Applied Chemistry* 65:935–40.

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