DYNAMIC CAPACITIVE WIRELESS POWER TRANSFER SYSTEMS

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DYNAMIC CAPACITIVE
WIRELESS POWER TRANSFER SYSTEMS

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Dynamic wireless power transfer (WPT) systems that effectively charge electric vehicles (EVs) while in motion can reduce EV costs, eliminate charging time, and enable unlimited range. This thesis introduces innovative architectures, circuit topologies, design techniques, and control methodologies for large air-gap kW-scale high power-transfer-density efficient dynamic capacitive WPT systems operating at multi-MHz frequencies that maintain constant power across wide variations in misalignment and air-gap. A new design approach for large air-gap capacitive WPT systems is proposed that utilizes split-inductor matching networks to absorb the parasitic capacitances of the charging environment that can otherwise severely degrade power transfer and efficiency. This approach also enhances the system's reliability by eliminating the need for discrete high-voltage capacitors. Two 6.78-MHz 12-cm air-gap prototype capacitive WPT systems are designed using this approach, with the first prototype achieving an efficiency of 88.4% and the second prototype achieving a power transfer density of 51.6 kW/m^2. This thesis also presents a new approach to designing multistage matching networks in capacitive WPT systems which maximizes the network efficiency while providing the required overall gain and compensation. Compared to the conventional approach to designing matching networks, the proposed approach offers a better trade-off between efficiency and power transfer density while meeting electric field safety requirements. The proposed design approach is validated using three capacitive WPT prototypes, one of which is also demonstrated to achieve substantially higher efficiency than a conventionally designed prototype. Furthermore, this thesis introduces a novel variable compensation technique – the active variable reactance (AVR) rectifier – that enables WPT systems to maintain a constant power transfer for widely varying coupling conditions expected in a dynamic charging scenario.

A 13.56-MHz 12-cm air-gap prototype capacitive WPT system incorporating the AVR rectifier is demonstrated to achieve constant power transfer for up to 45% misalignment between the charging pads and up to 45% increase in the air-gap. A control strategy for the AVR rectifier is developed that can dynamically compensate for coupling variations without the need for high-frequency sensing, and is experimentally demonstrated. Finally, capacitive WPT systems are compared with inductive WPT systems in terms of the theoretical limits on their power transfer capabilities and efficiencies.

BIOGRAPHICAL SKETCH

Sreyam Sinha received the B. Tech. degree in electrical engineering from the Indian Institute of Technology (IIT) Kharagpur in 2015, the M.S. degree in electrical engineering from the University of Colorado Boulder in 2017, the M.S. degree in electrical engineering from Cornell University in 2019, and is currently working towards his Ph.D. degree in electrical engineering at Cornell University. His research interests include the development of high frequency power converters for wireless power transfer. He received a Highlighted Paper honor in the IEEE Transactions on Power Electronics, and the Best Paper Award at IEEE COMPEL 2016 and IEEE COMPEL 2017.

Dedicated to my parents
and Piyali

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TABLE OF CONTENTS

CHAPTER

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

Wireless power transfer (WPT) is the method of transferring energy from one point to another without any physical contact between them, but rather using electromagnetic or acoustic waves. These waves, and the energy contained in them, propagate through the medium between the transmitting and the receiving points, such as air or water. WPT holds the potential to improve the quality of our lives while also propelling us towards a greener future, but also comes with its unique challenges.

1.1. Motivation

The concept of transferring large amount of energy through air has existed since the pioneering work of Nikola Tesla in the 1890's [1]. Tesla's attempt was based on the principle of maximizing the electromagnetic coupling between the transmitting and the receiving devices by matching their resonant frequencies. Following a stall for over a century, a resurgence in WPT research occurred when scientists at the Massachusetts Institute of Technology were able to transfer 60 W of power across a distance of 20 cm using a pair of self-resonating coils [2]. WPT has since undergone extensive research, targeting small-range low-power applications such as biomedical implants [3] and consumer electronics [4] to medium-range medium-to-high-power applications such as electric vehicles (EVs) [5], buses [6] and trains [7].

In biomedical implant applications, effective WPT can enable artificial heart pumps that do not have to use electric cords which penetrate abdominal walls, avoiding discomfort and potential infections. Furthermore, WPT can eliminate the need for surgeries that replace batteries of cardiac pacemakers by enabling charging from outside the patient's body. When applied to phones, laptops and other daily used electronic equipment, wireless charging can enhance consumer convenience and safety, and eliminate the wear and tear of cables associated with wired charging. The most transformative power of WPT, however, lies in its application in electrified transportation.

Electric vehicles, combined with self-driving technology and the concept of ridesharing, can significantly reduce our carbon footprint and propel us towards a cleaner and greener future. Today's main hurdle for EV adoption is its expensive battery, long charging time, and range anxiety. The battery cost can be as high as half the car price, whereas charging times can be as high as eight hours (for example, an 85-kWh battery being charged with an 11 kW charger). Significant reduction in charging time is achieved by the introduction of fast chargers (for example, Tesla supercharger operates at 250 kW and takes half an hour to charge a Model S from 2% to 80%), however these chargers are installed sparsely and in limited areas – practically limiting travel distance and viable routes.

Wireless power transfer can dramatically improve this situation by transferring power to the EV battery from the roadway through air. This is enabled by embedding charging pads in the roadway that electromagnetically couple to charging pads attached underneath the vehicle chassis. EVs can be charged wirelessly in a stationary, semi-dynamic, or dynamic manner. In the stationary mode, the EVs would be charged when it is parked. Stationary charging has its advantage in terms of convenience and safety, but still suffer from some of the drawbacks of wired charging such as large battery requirement. In the semi-dynamic mode, EVs would be charged while waiting on a traffic signal, and the EV battery would store only an energy that is sufficient to propel the vehicle to the next charging pad. This can significantly bring down the size and cost of the batteries and potentially enable unlimited range; however, its effectiveness still depends on the frequency at which the car is able to stop. In the dynamic mode, EVs would be charged on-the-go from a series of charging pads in the roadway, with the separation between consecutive pads and their power transfer capabilities designed so as to ensure a steady propulsion. Dynamic charging can therefore truly relieve the downsides of today's EVs by enabling drastically reduced storage, zero charging time, and unlimited range.

Wireless power transfer can similarly transform other applications that involve electrically powered automobiles, for example, autonomous material handling vehicles (AMHVs) used in warehouses and factories. These AMHVs are used to swiftly pick up and carry material from one place to another, dynamically navigating obstacles and human co-workers. Currently, the batteries of these vehicles are replenished by offline charging or swapping drained batteries with pre-charged ones, imposing substantially added cost and space requirements. With WPT, these AMHVs can be charged from the floor while they are in operation, in both semi-dynamic and dynamic manner, dramatically increasing productivity and reducing the need for on-board batteries.

Wireless power transfer, therefore, holds the potential to improve quality of life by increasing convenience and safety in the use of biomedical implants and consumer electronics, enhancing productivity in factories and warehouses, and reducing air pollution by facilitating EV adoption.

1.2. WPT Technologies

1.2.1. Far-Field (Radiative) WPT

Traditionally, radiative techniques are used to transfer power wirelessly over long distances, spanning several meters and even kilometers, for cellular network [8], underwater energy harvesting [9], and space applications [10]. Techniques for such long-distance power transfer include the use of radio-frequency electromagnetic waves [11], THz-frequency laser beams [12], and acoustic waves generated through piezoelectric devices [13]. Although capable of long-distance power transfer, systems using these techniques suffer from poor efficiency and high cost.

1.2.2. Near-Field (Non-Radiative) WPT

Research in WPT has more recently been focused on medium-range (near-field) applications, where the distance between the transmitter and the receiver is of the same order as the size of the charging pad. Medium-range WPT is achieved using two techniques: inductive WPT – which utilizes time-varying magnetic fields coupled between conducting coils [14], and capacitive WPT – which utilizes time-varying electric fields coupled between conductive plates [15].

Hereinafter, the transmitting side of the WPT system will be referred to as primary side, and the receiving side will be referred to as secondary side.

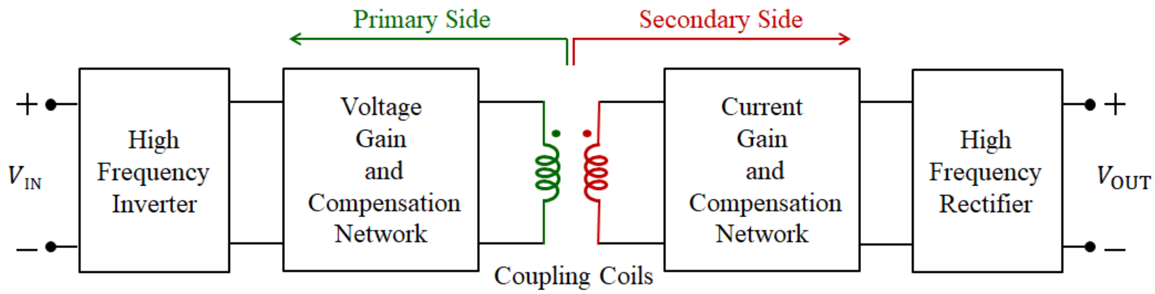


Fig. 1.1: Architecture of an inductive WPT system.

A. Inductive WPT

The pair of coupling coils used in medium-range inductive WPT systems are loosely coupled, resulting in a relatively small mutual inductance. This necessitates large coil currents to transfer substantial power across the air-gap, generating high fringing magnetic fields [16]. In applications where human and animals can potentially be exposed to such high fields, such as EV charging, it is imperative to keep the fringing fields within safety limits [17]. Furthermore, due to loose coupling, the coils have a high leakage inductance, resulting in high circulating currents and reduced efficiency [18]-[19]. The issues of high fringing fields and high circulating currents are addressed by employing an inductive WPT architecture as shown in Fig. 1.1. A high-frequency inverter converts the dc input voltage (which is obtained by rectifying the grid voltage) into a high-frequency ac voltage. This ac voltage is fed to the primary-side matching network, which steps it up to create a high voltage across the primary-side coil. This enables large power transfer with relatively small currents through the coil, and hence small fringing magnetic fields. A matching network on the secondary side then steps this current back up and the voltage down to the level required at the output. The two matching networks also provide capacitive reactances that compensates for the coil reactance. This ensures that the impedance seen by the inverter is near-resistive, thus minimizing circulating currents and associated losses. Finally, a high-frequency rectifier interfaces the system to the load, which in many applications is a battery.

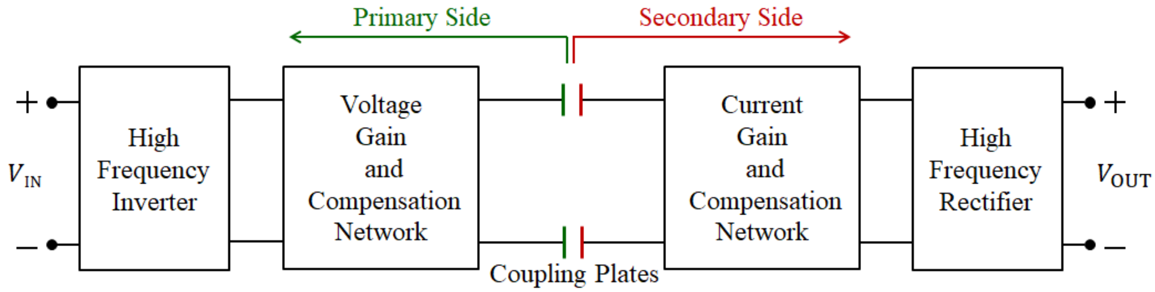


Fig. 1.2: Architecture of a capacitive WPT system.

B. Capacitive WPT

Owing to the limited coupling area and relatively large air-gap, the coupling capacitance in a medium-range capacitive WPT system is low, resulting in a large capacitive reactance. Transferring substantial power through such a large reactance requires a large voltage across the air-gap, generating fringing electric fields that can surpass the safety limit. Furthermore, similar to inductive WPT systems, the large reactance of the coupler also increases circulating currents and losses in the system. These issues are addressed by employing a capacitive WPT architecture similar to inductive WPT. The voltage step-up provided by the primary-side matching network creates a large voltage across the primary-side coupling plates, ensuring larger power transfer with relatively small displacement current through the plates, and hence, small air-gap voltage and fringing electric fields. The secondary-side matching network then provides the necessary current step-up and voltage step-down as per the output requirement. The matching networks also provide the inductive reactance required to compensate for the capacitive reactance of the coupler, making the impedance seen by the inverter near-resistive and minimizing circulating currents.

1.3. State of the Art

Initial research on inductive WPT systems focused on small air-gap low-power applications such as transcutaneous energy systems [20] and biomedical implants [21]-[25]. These systems transferred sub-watt level power through a distance ranging from 0.5 cm to 2 cm with efficiencies reaching up to 50%.

Small air-gap but relatively higher power (5 W − 70 W) inductive WPT systems targeting consumer and portable electronic devices [26]-[30] attracted attention in the early 2000's. Due to a larger area to gap ratio combined with higher power levels, these systems achieve higher efficiencies (in the range of 70% − 85%) than those used in biomedical applications. Inductive wireless charging technology for portable electronics applications have now reached commercialization stage through the introduction of 'Qi' standard [31]. An application area that is recently gaining interest is unmanned aerial vehicles (UAVs) [32] and unmanned underwater vehicles (UUVs) [33] used for surveillance purpose, having power requirements of the order of a few hundreds of watts. Stationary wireless UAV charging systems have reported efficiency in excess of 90% [34], however, research on charging UAVs on the fly, which can drastically increase their productivity, is still in a nascent stage.

Medium-range relatively high-power inductive WPT have initially been employed to charge material handling vehicles in factories [35]-[37]. These vehicles are wirelessly charged while stationed on a track comprising a long transmission coil. The air-gap in these applications can vary from 5 cm – 15 cm, and power level from few hundreds of watts to a few kilowatts. Due to the existence of a single long transmission coil simultaneously charging a varying number of MHVs, these systems suffer from the need for overdesign, and reliability issues [37]. However, since the ground clearance and charging power levels of MHVs are similar to EVs, research in wireless charging of MHVs also paved the way for wireless EV charging systems.

WPT for EV charging has become popular since early 2010's [38]-[39]. Due to its potential impact on accelerating EV adoption and reducing air pollution, wireless charging for EVS has undergone extensive research over the last decade. Through innovations in the design of coupling coils and compensation networks [40], stationary EV charging systems have achieved power transfer levels of up to 50 kW, with efficiencies as high as 97% [41]-[44]. Wireless EV chargers with power transfer levels up to 11 kW have already been commercially available [45]. This success has also prompted research in inductive wireless charging of electric bus, with power levels up to 250 kW [46], and railway systems, with power levels up to 1 MW [47].

Although high-power stationary systems can charge EVs faster, the true potential for storage reduction and range extension for EVs still lies in dynamic charging. Despite a few experimental demonstrations [47], dynamic WPT for EVs is yet to be commercially viable, the main reason of which is the need for ferrite blocks in inductive WPT systems for magnetic flux guidance and shielding [48]-[49]. Ferrite blocks are heavy, bulky, expensive and brittle, making them difficult to embed in roadway. Furthermore, losses in ferrites increase exponentially with operating frequency, limiting the potential for the WPT system's size reduction. On the other hand, capacitive WPT systems, which utilize relatively directed electric fields for power transfer, do not need dielectric material for flux guidance. Therefore, they can be operated at high frequencies, reducing their size, weight and cost. Furthermore, compared to their inductive counterparts, capacitive WPT systems generate substantially lower eddy-current-induced heating and losses in surrounding metallic structures, and have higher tolerance to coupling variations [50]. These advantages make capacitive WPT an attractive alternative for dynamic EV charging and other applications.

Capacitive WPT research has so far been limited to low-power small air-gap applications such as biomedical implants [51]-[54], consumer electronics [55]-[58] and robots [59], achieving efficiencies in the range of 50% – 80%. When air-gap is increased, the coupling capacitance diminishes, drastically increasing the compensation requirement. In large air-gap capacitive WPT systems such as the ones targeted to charge EVs and MHVs, lowering this compensation requirement necessitates operating at very high frequencies, making efficient design of these systems very challenging. Furthermore, EVs and MHVs also have a limited area available underneath their chassis, triggering the need for high power transfer through a relatively small coupling area, i.e., a high power transfer density. A higher power transfer (while maintaining the same air-gap voltage) increases the gain required from the matching networks, whereas a smaller coupling area increases the coupling reactance and the required compensation, both reducing efficiency. Furthermore, power transfer and efficiency falls substantially when the coupling capacitance changes, either due to misalignments of charging pads during dynamic charging, or variations in air-gap due to different vehicle ground clearances (although the fall in power transfer is less severe than inductive WPT systems). This reduces the energy delivered to the battery from a single charging pad, requiring more charging pads to be installed, thus increasing infrastructure and maintenance cost. Therefore, there is a need for large air-gap high power-transfer-density high-efficiency capacitive WPT systems that can maintain power transfer even with misalignments or air-gap variations.

1.4. Contributions of the Thesis

This thesis introduces the topology and associated design and control techniques for multi-MHz high-power-transfer-density capacitive WPT systems that can efficiently transfer kW-level power across a large air-gap, and can also maintain a constant power transfer over a wide range of misalignments and air-gap variations.

In a large air-gap capacitive WPT system such as the ones used for EV charging, the parasitic capacitances present in the charging environment (e.g., those introduced by the vehicle chassis and the roadway) can overwhelm the coupling capacitance and severely degrade power transfer and efficiency. This thesis introduces a new design approach to mitigate the effect of parasitic capacitances and achieve high performance in large air-gap capacitive wireless power transfer (WPT) systems. The proposed approach addresses the challenge by employing split-inductor matching networks, which allow the complex network of parasitic capacitances to be simplified into an equivalent four-capacitance model. The shunt capacitances of this model are directly utilized as the matching network capacitors, hence, absorbing the parasitic capacitances and utilizing them in the power transfer mechanism. This also eliminates the need for discrete high-voltage capacitors, enhancing the efficiency and reliability of the system. A systematic procedure is developed to accurately measure the equivalent capacitances of the model, enabling the system's performance to be reliably predicted. The proposed approach is used to design two 6.78-MHz 12-cm air-gap prototype capacitive WPT systems with capacitor-free matching networks. The first system transfers up to 590 W using 150 cm^2 square coupling plates, and achieves an efficiency of 88.4%. The second prototype system transfers up to 1217 W using 118 cm^2 circular coupling plates, achieving a power transfer density of 51.6 kW/m^2. The measured output power profiles of the two systems match well with their predicted counterparts, validating the proposed design approach.

Once the model of the capacitive coupler is developed, the next challenge is to design the matching networks of the capacitive WPT system so as to efficiently transfer substantial power across the air-gap. This thesis introduces an analytical optimization approach for the design of L-section matching networks in capacitive WPT systems, which maximizes the network efficiency while achieving the required overall gain and compensation. The proposed approach identifies the optimal number of matching network stages, and the optimal distribution of gains and compensations among these stages. Compared to the conventional approach to designing matching networks for capacitive WPT systems, the proposed approach results in a higher and flatter efficiency for a wide range of air-gap voltages. The proposed approach also offers a better trade-off between efficiency and power transfer density, while meeting electric field safety requirements. The efficiency predictions of the proposed design approach are experimentally validated using three 6.78-MHz, 100-W prototype capacitive WPT systems, one with single-stage matching networks, one with two-stage matching networks, and another with three-stage matching networks. The measured matching network efficiencies of the prototype systems are in close agreement with the theoretical predictions. The prototype system with two-stage matching networks is also compared with a prototype system designed using the conventional approach, and is shown to achieve significantly higher efficiency.

Next, this thesis addresses the challenges related to misalignments and air-gap variation in a dynamic charging scenario by introducing the active variable reactance (AVR) rectifier – a new approach to continuously compensate for coupling variations in WPT systems. The AVR rectifier operates at a fixed frequency and incorporates a power-splitting resonant network. By controlling the ratio of the split powers in its branches, the AVR rectifier continuously compensates for large misalignments and distance variations between couplers, while maintaining full power transfer. A comprehensive methodology is presented that maximizes the tolerable range of misalignments in an AVR-rectifier-enabled capacitive WPT system while meeting efficiency targets. The proposed approach is validated using a 13.56-MHz, 300-W, 12-cm nominal air-gap prototype capacitive WPT system, which incorporates an AVR rectifier and can be scaled up in power for dynamic electric vehicle (EV) charging applications. The prototype system maintains full power transfer for up to 45% lateral misalignment in the coupler and up to 45% increase in the vehicle's road clearance. In a dynamic EV charging scenario, the AVR-rectifier-enabled system transfers 80% more energy during a single pass of the vehicle over the charging pad, as compared to a system without the AVR rectifier. The measured performance of the prototype system is in good agreement with the predictions.

Next, this thesis develops a closed-loop control strategy to dynamically compensate for coupling variations in capacitive WPT systems utilizing the AVR rectifier. The proposed control approach utilizes a decoupled-dual-loop strategy to regulate the power in the two branches of the AVR rectifier. This approach enables dynamic reactive compensation and output power recovery under varying coupling conditions without having to sense any high-frequency voltage or current. A comprehensive small-signal model of the AVR-rectifier-based capacitive WPT system is developed and the controller design method is discussed. A 6.78-MHz scaled capacitive WPT prototype, incorporating an AVR rectifier controlled using the proposed approach, is designed, built and tested. The proposed closed-loop control strategy enables the prototype system to maintain constant output power for large misalignments between the coupling pads.

Finally, this thesis presents a theoretical comparison between inductive and capacitive WPT systems and discusses their projected performances. The maximum power transfer capabilities of the two WPT systems are formulated while adhering to their physical limits, with the limit set by saturation of the magnetic core in inductive WPT systems, and by electric breakdown of air in capacitive WPT systems. The efficiency of inductive and capacitive WPT systems are formulated in terms of the system specifications, and the tradeoff between efficiency and power transfer density are compared. It has been shown that capacitive WPT systems are favored by a higher operating frequency, while inductive WPT systems are favored by a larger gap to area ratio. Introduction of multistage compensation networks are shown to increase the efficiency of both systems, with the improvement being significantly higher for capacitive WPT systems, resulting in a better tradeoff between efficiency and power transfer density.

1.5. Thesis Organization

The remainder of the thesis is organized as follows. Chapter 2 discusses modeling of the capacitive coupler in a large air-gap capacitive WPT system, and the proposed techniques to accurately measure the model parameters. Chapter 3 describes and validates the proposed matching network design approach and compares it with the conventional approach. Chapter 4 introduces the AVR rectifier, details its design method and demonstrates its effectiveness through experimental results. Chapter 5 deals with the proposed control strategy for the AVR rectifier in a capacitive WPT system. Chapter 6 theoretically compares capacitive and inductive WPT systems, and highlights their projected performances. Finally, Chapter 7 summarizes and concludes the thesis.

CHAPTER 2

MODELING OF THE CAPACITIVE COUPLER

Before designing a large air-gap capacitive WPT system, it is important to know an accurate model of the charging environment. This chapter develops such a model in context of an EV charging system, however, it is generally applicable to any large air-gap capacitive WPT system. Owing to the limited area available underneath the vehicle chassis and the large air-gap between the chassis and the road, the coupling capacitance in a capacitive EV charging system is small (of the order of a few pF). Furthermore, the parasitic capacitances present in an EV charging environment, including the capacitances from the coupling plates to the vehicle chassis and roadway, can be comparable to or even larger than the coupling capacitance. Previous works on capacitive EV charging systems [60] model the capacitances between the coupling plates, however, they do not model the additional parasitic capacitances arising due to the presence of the roadway or the vehicle chassis. Hence, these models are not fully representative of a practical EV charging environment. These additional parasitic capacitances can substantially degrade power transfer capability and efficiency of a capacitive WPT system, and must be factored into its design.

This chapter presents a new approach to designing capacitive WPT systems for EVs in the presence of parasitic capacitances introduced by the charging environment. The proposed approach creates circuit symmetry through the use of split-inductor matching networks. The resultant circuit symmetry ensures that no parasitic currents flow from the roadway back to the inverter's ground plane, from the roadway to the vehicle chassis, and from the vehicle chassis to the rectifier's ground plane. The absence of these parasitic currents further allows the complex network of parasitic capacitances to be simplified into a four-capacitance model. The shunt capacitances of this simplified model are then used to entirely realize the matching network capacitances. Hence, the parasitic capacitances are incorporated into the power transfer mechanism, and on-board discrete capacitors are eliminated, improving the reliability and efficiency of the system. Furthermore, a comprehensive methodology is developed to accurately determine the equivalent capacitances of the four-capacitance model. In this methodology, the capacitance values are determined using a set of practical measurements, in a manner that the system's power transfer is minimally impacted by measurement errors.

The proposed approach is utilized to model the coupling environment, measure the equivalent capacitances of the model, and design capacitor-free matching networks for two high-performance 6.78-MHz 12-cm air-gap prototype capacitive WPT systems. The first system utilizes 12.25-cm $\times$ 12.25-cm square coupling plates and transfers 590 W with an efficiency of 88.4%, achieving a power transfer density of 19.6 kW/m^2. The second system utilizes 12.25-cm-diameter circular coupling plates and transfers up to 1217 W with an efficiency of 74.7%, corresponding to a power transfer density of 51.6 kW/m^2. The measured output power of these prototype systems is shown to be in excellent agreement with the model-based predictions. Furthermore, to the authors' best knowledge, the power transfer densities of these systems are more than a factor of 5 higher than those reported in previous journal publications [60]; hence, illustrating the effectiveness of the proposed approach in enabling high-performance capacitive WPT for EVs.

2.1. Large Air-gap Capacitive WPT Systems

An example implementation of the capacitive WPT architecture described in the previous chapter is shown in Fig. 2.1 in the context of EV charging. It comprises a full-bridge inverter, a roadway-side matching network with one resonant L-section stage, a vehicle-side matching network with another resonant L-section stage, and a full-bridge rectifier. The capacitive coupling mechanism is modeled in this circuit using two capacitors, shown as C_S in Fig. 2.1. This simple representation is found to be inadequate when a practical EV charging environment is considered, as shown in Fig. 2.2. It can be seen that, apart from the desired capacitance between the coupling plates (C_S), 15 additional parasitic capacitances exist in this system. These additional capacitances originate from cross-coupling between

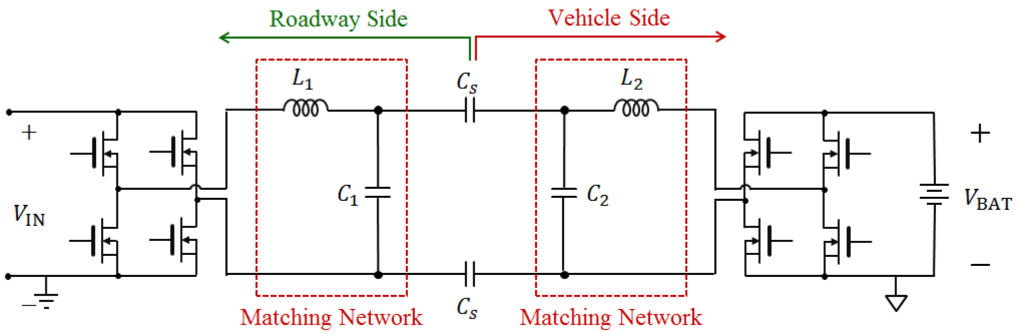


Fig. 2.1: An example implementation of a large air-gap capacitive WPT system suitable for EV charging, comprising a full-bridge inverter, a full-bridge rectifier, and single-stage L-section matching networks on the roadway side and the vehicle side.

the plates (C_d), as well as from coupling between two plates on the same side ($C_{pp,r}$ and $C_{pp,v}$), the plates and the roadway (C_{pr} and $C_{pr}{}'$), the plates and the vehicle chassis (C_{pv} and $C_{pv}{}'$), the roadway and the vehicle-chassis (C_{rv}), the roadway and the inverter ground ($C_{r,gnd}$), and the vehicle chassis and the rectifier ground ($C_{v,gnd}$). Many of these parasitic capacitances (for example, the capacitance C_{pr} between the roadway-side plates and the roadway) can be comparable to or even higher in magnitude than the coupling capacitance C_s, and hence, cannot be ignored while modeling the coupler. The circuit schematic of a capacitive WPT system incorporating all the parasitic capacitances is shown in Fig. 2.3.

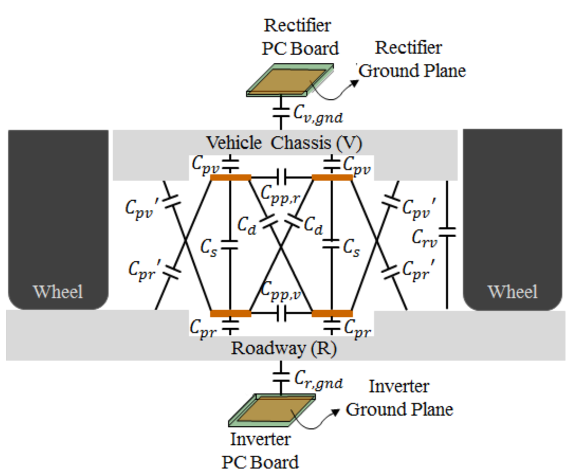


Fig. 2.2: A practical EV charging environment for a capacitive WPT system showing the various existing parasitics. The brown rectangles represent the roadway-side and vehicle-side coupling plates.

The next section presents a modeling and design approach that enables the capacitive WPT system of Fig. 2.3 to achieve high performance despite the presence of these parasitics.

2.2. Simplified Model and Absorption of Parasitic Capacitances

The complex network of parasitic capacitances as described above makes it challenging to design the matching networks of the capacitive WPT system of Fig. 2.3 so as to achieve a desired power transfer. Therefore, there is a need to reduce the high-order capacitive network to a simpler, more tractable equivalent model. This section presents an approach that enables this high-order system to be represented by a simple four-capacitance model that can be easily used in designing the matching networks. As shown in Fig. 2.2 in the previous section, the parasitic capacitance $C_{r,gnd}$ in the EV charging environment arises from the proximity between the roadway and the inverter ground (including the ground plane in the inverter PCB and other ground interconnects). We envision the inverter power electronics being embedded as a package within the roadway. Hence, there is likely to be significant overlap between the inverter ground and the roadway, and the capacitance $C_{r,gnd}$ can be relatively large. Similarly, the capacitance $C_{v,gnd}$ arises from the proximity between the vehicle chassis and the rectifier ground. Due to on-board size constraints, the chassis and rectifier power electronics will also be in close proximity, resulting in a relatively large value of $C_{v,gnd}$. Finally, the capacitance C_{rv} is the outcome of the overlap between the roadway and the vehicle chassis. The roadway and vehicle chassis are separated

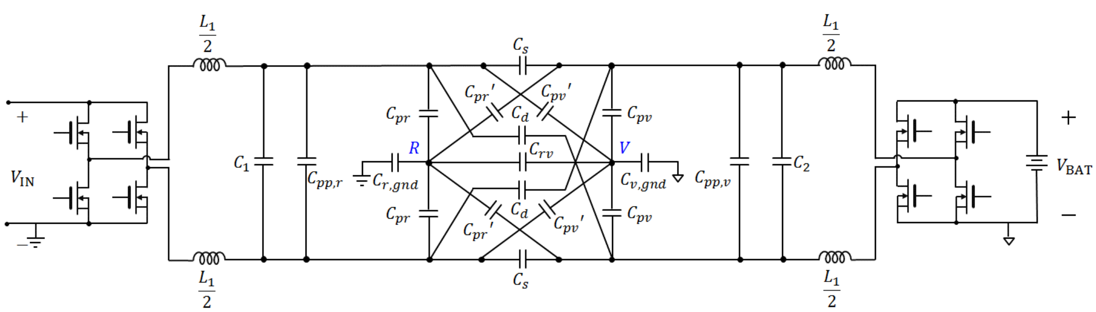


Fig. 2.3: A capacitive WPT system incorporating the parasitic capacitances present in a practical EV charging environment.

by the vehicle's ground clearance, but have large areas which contribute to a relatively large value of C_{rv}. These three parasitic capacitances provide relatively low impedance paths for the inverter output current to return to inverter ground, without charging the EV battery. Therefore, any currents through these capacitances will cause the power transfer to fall.

To ensure that no current flows through the parasitic capacitances $C_{r,gnd}$, $C_{v,gnd}$, and C_{rv}, the inductors of the matching networks are split symmetrically into two halves, with one half placed in the forward path, and the other in the return path, as shown in Fig. 2.4. In this symmetric circuit, the ac component of the voltages appearing across the capacitances $C_{r,gnd}$, $C_{v,gnd}$, and C_{rv} are zero, which prevents any parasitic currents from flowing through them. To further understand this, consider Fig. 2.5, which is a fundamental-frequency equivalent circuit of the capacitive WPT system of Fig. 2.4. Here the voltages at the two switch nodes of the full-bridge inverter and the two switch nodes of the full-

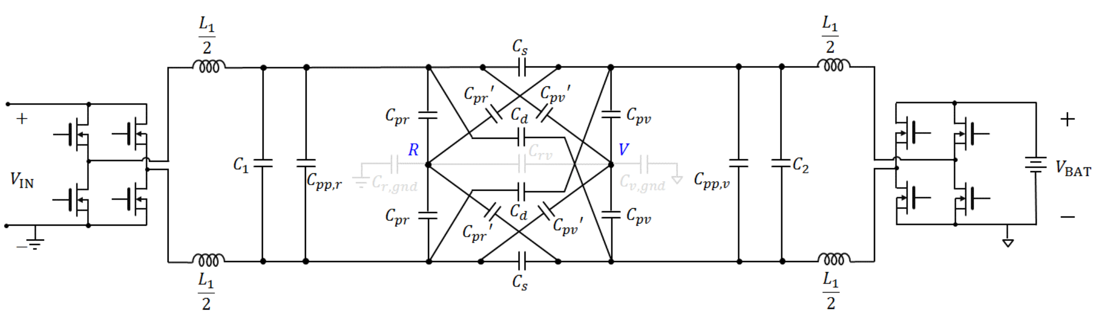


Fig. 2.4: A capacitive WPT system incorporating split-inductor matching networks. The circuit symmetry effectively eliminates the capacitances $C_{r,gnd}$, $C_{v,gnd}$, and C_{rv}.

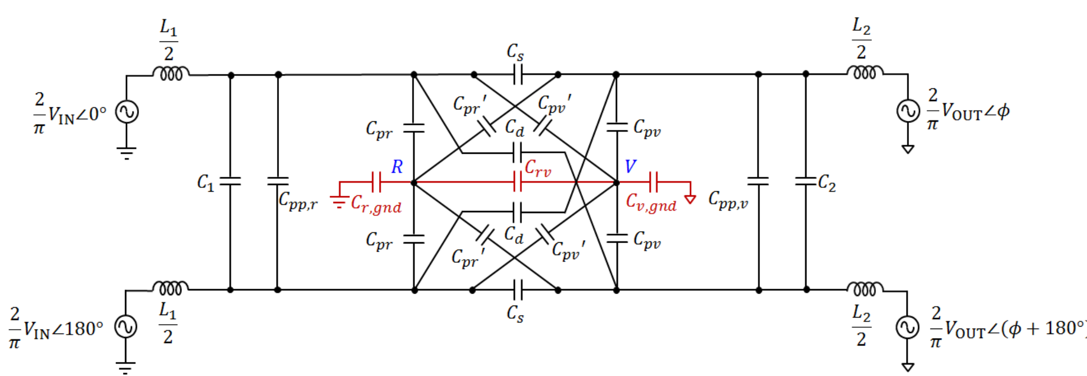


Fig. 2.5: Equivalent model of the capacitive WPT system of Fig. 2.4 under fundamental frequency analysis.

bridge rectifier are modeled as four equivalent sinusoidal voltage sources. Note that the dc components of these voltages are not modeled, since they do not contribute to capacitor currents. Also, since the two inverter legs are switched 180° out of phase with respect to each other, their equivalent sinusoidal sources are outphased by the same amount. The same applies to the rectifier sources. The currents flowing through the parasitic capacitances in this circuit can be obtained using the principle of superposition.

First, all sources except the top inverter source are shorted, as shown in Fig. 2.6(a). In this configuration, a current $i_{r,gnd1}$ flows through the capacitance $C_{r,gnd}$, a current $i_{v,gnd1}$ flows through the capacitance $C_{v,gnd}$, and a current i_{rv1} flows through the capacitance C_{rv}. Next, all sources except the bottom inverter source are shorted, as shown in Fig. 2.6(b). In this configuration, a current $i_{r,gnd2}$ flows through $C_{r,gnd}$, a current $i_{v,gnd2}$ flows through $C_{v,gnd}$, and a current i_{rv2} flows through C_{rv}. As

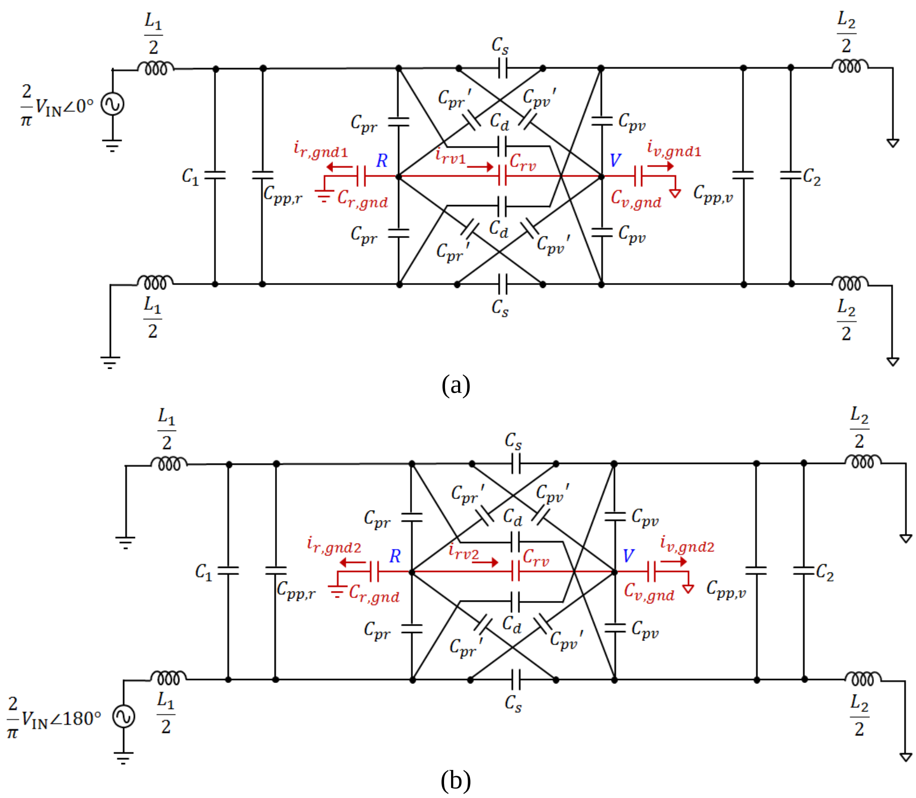


Fig. 2.6: Equivalent circuits obtained by applying superposition to the capacitive WPT system of Fig. 2.5, with: (a) only the top inverter source active, and (b) only the bottom inverter source active.

can be seen from Figs. 7(a) and 7(b), the capacitances $C_{r,gnd}$, $C_{v,gnd}$ and C_{rv} are located symmetrically with respect to the two inverter voltage sources. This symmetry is made possible by splitting the matching network inductors into two equal halves. Furthermore, the two inverter sources have equal magnitude (= $2V_{\mathrm{IN}}/\pi$). Hence, they induce currents of equal magnitude in the symmetrically located $C_{r,gnd}$, $C_{v,gnd}$ and C_{rv}, i.e., $|i_{r,gnd1}| = |i_{r,gnd2}|$, $|i_{v,gnd1}| = |i_{v,gnd2}|$ and $|i_{rv1}| = |i_{rv2}|$. However, the two voltage sources are 180° out of phase, so the current induced by one source cancels the other, i.e., $i_{r,gnd1} = -i_{r,gnd2}$, $i_{v,gnd1} = -i_{v,gnd2}$ and $i_{rv1} = -i_{rv2}$; resulting in zero total current through these capacitances because of the inverter sources. Similar arguments show that the two rectifier sources also induce zero total current through these capacitances. Therefore, the circuit symmetry enforced by splitting the matching network inductors prevents parasitic currents from flowing through $C_{r,gnd}$, $C_{v,gnd}$ and C_{rv}.

This analysis is validated using LTspice simulations for a 6.78-MHz 1-kW 12-cm air-gap capacitive WPT system. Figure 2.8 shows the voltages across the three capacitances $C_{r,gnd}$, $C_{v,gnd}$ and C_{rv}. As can be seen, they stay fairly constant, suggesting that they have very small ac components. Figure 2.9 shows the currents through these capacitances. It can be seen from Fig. 2.8 that the magnitude of these currents are all less than 0.5 mA. The effectiveness of the split-inductors matching network in such a system is illustrated in Fig. 2.9. It can be seen that without split inductors, substantial currents flow

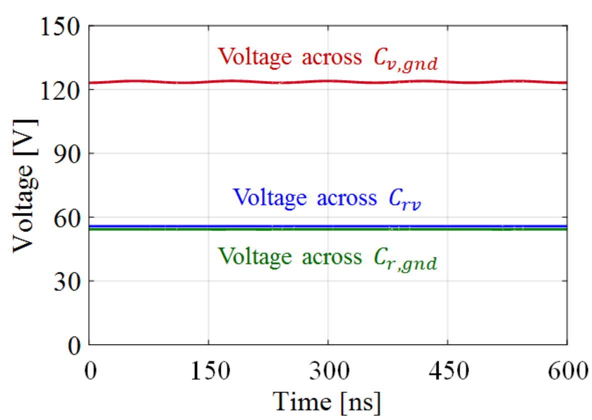


Fig. 2.7: Voltages across the parasitic capacitances $C_{r,gnd}$, $C_{v,gnd}$, and C_{rv} in a 6.78-MHz 1-kW 12-cm air-gap capacitive WPT system that utilizes split-inductor matching networks.

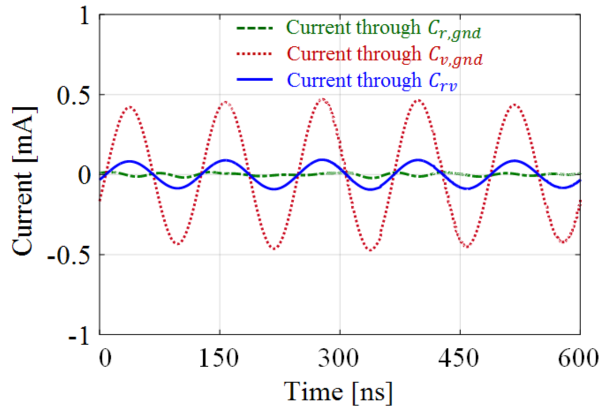


Fig. 2.8: Currents through the parasitic capacitances $C_{r,gnd}$, $C_{v,gnd}$, and C_{rv} in a 6.78-MHz 1-kW 12-cm air-gap capacitive WPT system that utilizes split-inductor matching networks.

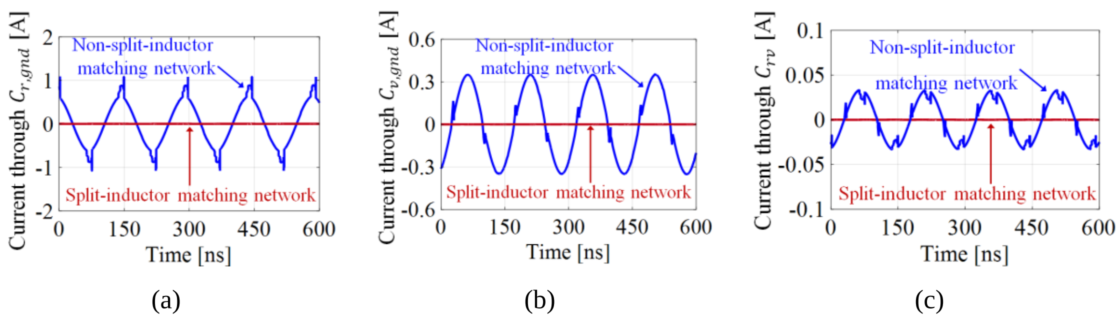


Fig. 2.9: Current through the parasitic capacitances (a) $C_{r,gnd}$, (b) $C_{v,gnd}$, and (c) C_{rv} in a 6.78-MHz 12-cm air-gap capacitive WPT system while utilizing split-inductor and non-split-inductor matching networks, simulated in LTspice.

through the three parasitic capacitances, whereas when the inductors are split, these currents are eliminated. The impact of inductor splitting on the system's power transfer is shown in Fig. 2.10 for example ranges of the parasitic capacitances $C_{r,gnd}$ and $C_{v,gnd}$. As can be seen, the split-inductor approach allows the system to maintain a flat power transfer even for relatively large parasitic capacitance values. In contrast, with non-split inductors, the power transfer degrades rapidly. Therefore, split-inductor matching networks are not only effective but essential for kilowatt-scale power transfer in capacitive WPT systems for EV charging.

With the split-inductor matching networks, and the capacitances $C_{r,gnd}$, $C_{v,gnd}$, and C_{rv} eliminated, the resultant circuit of Fig. 2.4 can be simplified in the following manner. Owing to the symmetry of this circuit, the voltages across the two capacitances C_{pr}'s on the roadway side, and hence the currents

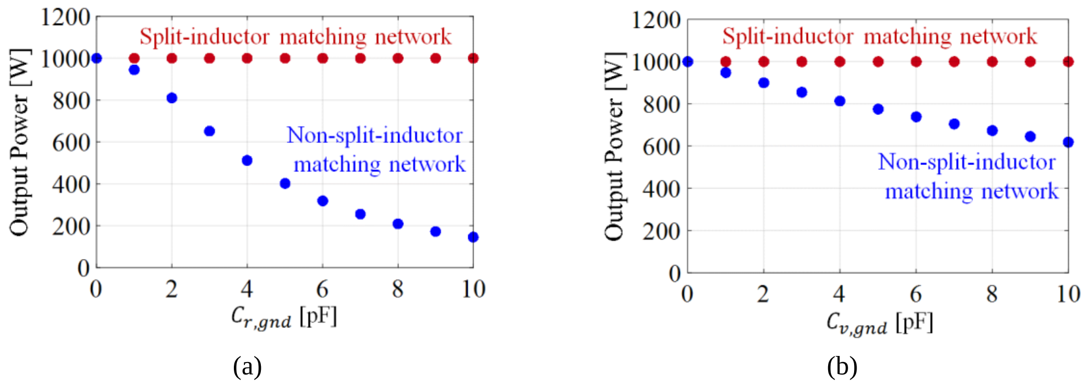


Fig. 2.10: Output power of a 6.78-MHz 12-cm air-gap capacitive WPT system as a function of the parasitic capacitance (a) $C_{r,gnd}$, and (b) $C_{v,gnd}$ while utilizing split-inductor and non-split-inductor matching networks, simulated in LTspice.

flowing through them, are equal, as shown in Fig. 2.11(a). Therefore, these two capacitances are effectively in series, forming a capacitance of $\frac{C_{pr}}{2}$, as shown in Fig. 2.11(b). Similarly, the two capacitances C_{pv}'s, the two capacitances $C_{pr}{}'$'s, and the two capacitances $C_{pv}{}'$'s are also in series, forming effective capacitances $\frac{C_{pv}}{2}$, $\frac{C_{pr}{}'}{2}$ and $\frac{C_{pv}{}'}{2}$, respectively, as shown in Fig. 2.11(c). Furthermore, the effective capacitance $\frac{C_{pr}}{2}$ is in parallel with the effective capacitance $\frac{C_{pv}{}'}{2}$, which is further in parallel with the plate-to-plate parasitic capacitance $C_{pp,r}$ on the roadway side. These three capacitances in parallel form an equivalent capacitance of $C_{pp,r} + \frac{C_{pr}}{2} + \frac{C_{pv}{}'}{2}$, as shown in Fig. 2.11(d). Similarly, the effective capacitances $\frac{C_{pv}}{2}$, $\frac{C_{pr}{}'}{2}$, and the plate-to-plate capacitance $C_{pp,v}$ on the vehicle side form an equivalent capacitance of $C_{pp,v} + \frac{C_{pv}}{2} + \frac{C_{pr}{}'}{2}$, as also shown in Fig. 2.11(d). The complicated network of parasitic capacitances in Fig. 2.4 is now reduced to the equivalent six-capacitance model of Fig. 2.11(d). This six-capacitance model can then be further simplified to the four-capacitance model shown in Fig. 2.11(e) using two-port network theory, as derived in Appendix A.

The four equivalent capacitances in the circuit model of Fig. 2.11(e) can be expressed in terms of the original parasitic capacitances as:

$$C_{s,eqv} = C_s - C_d, \tag{2.1}$$

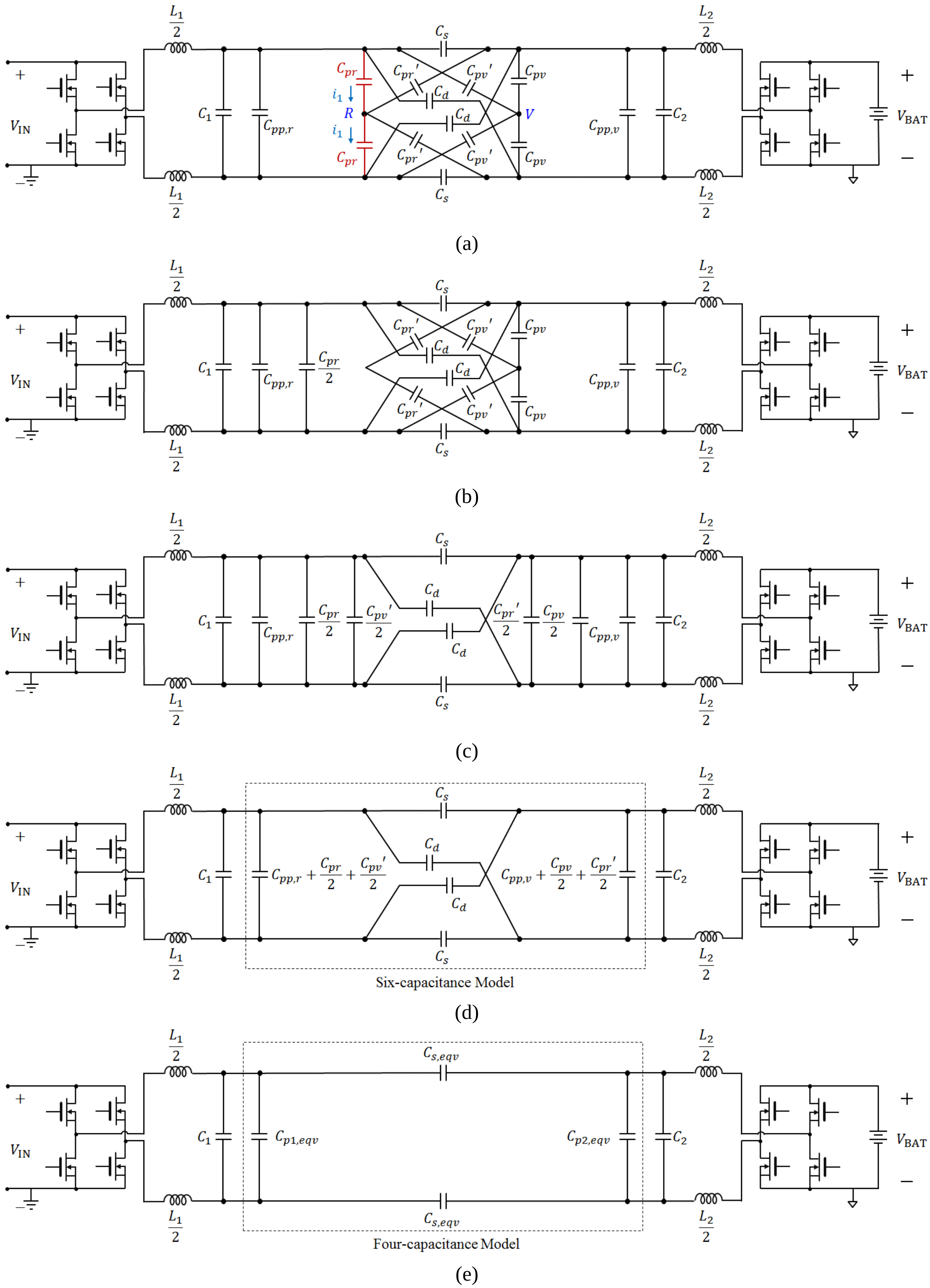


Fig. 2.11: Reduction of the complex capacitance matrix of Fig. 2.4 into a simple four-capacitance model.

$$C_{p1,eqv} = C_{pp,r} + \frac{C_{pr}}{2} + \frac{C_{pv'}}{2} + C_d, \tag{2.2}$$

$$C_{p2,eqv} = C_{pp.v} + \frac{C_{pv}}{2} + \frac{C_{pr'}}{2} + C_d. \tag{2.3}$$

It can be seen that the shunt capacitance $C_{p1,eqv}$ of this model is in parallel with the matching network capacitor C_1 on the roadway side, and similarly, the shunt capacitance $C_{p2,eqv}$ is in parallel with the matching network capacitor C_2 on the vehicle side. These shunt capacitances can therefore be absorbed into the matching networks by appropriately modifying the matching network capacitor values. Since the shunt capacitances $C_{p1,eqv}$ and $C_{p2,eqv}$ represent the parasitic capacitances present in the EV charging environment (see (2.2) and (2.3)), this modeling approach enables the parasitic capacitances to be absorbed in the matching networks and utilized in the power transfer mechanism of the capacitive WPT system.

The efficiency and reliability of the capacitive WPT system of Fig. 2.11(e) can be further enhanced by fully realizing the required matching network capacitances using the shunt capacitances $C_{p1,eqv}$ and $C_{p2,eqv}$ of the four-capacitance model. This eliminates the need for discrete high-voltage capacitors in the matching networks, which introduce losses and may be prone to dielectric breakdown. Such a capacitive WPT system not requiring any discrete matching network capacitors is shown in Fig. 2.12.

In this system, given the series equivalent capacitance $C_{s,eqv}$ (which arises from the geometry of the four-plate coupler structure, as can be seen from Fig. 2.2 and (2.1)), values for the matching network inductances L_1 and L_2, and the matching network capacitances $C_{p1,eqv}$ and $C_{p2,eqv}$, can be obtained using the design methodology provided in the next chapter. The required matching network capacitances can then be realized solely from the parasitics by appropriately spacing the coupling plates from the

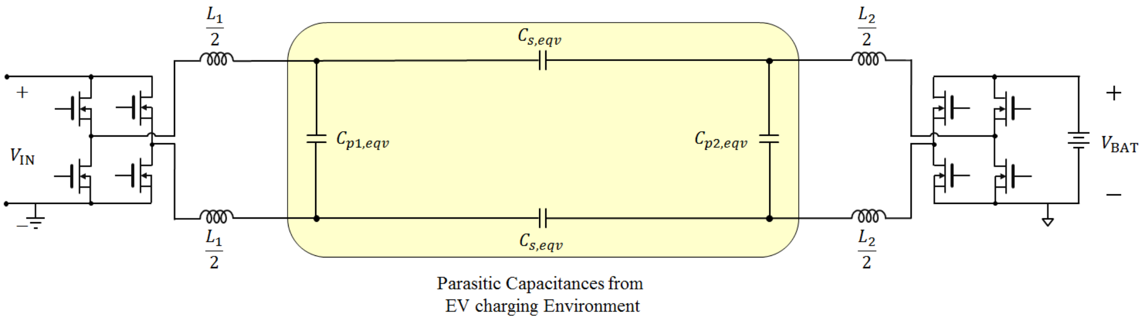


Fig. 2.12: A capacitive WPT system with the matching network capacitors realized entirely using the parasitic capacitances present in an EV charging environment.

roadway and the vehicle chassis, as will be demonstrated for two prototype capacitive WPT systems in Section 2.4.

In practical capacitive WPT systems for EVs, both stationary and dynamic, the vehicle-side plates can be misaligned from the roadway-side plates. Such misalignments change the coupling capacitance and some of the parasitic capacitances of the EV charging environment. Nevertheless, the modeling methodology of Fig. 2.11 can still be applied in an approximate but reasonably accurate manner, as discussed in detail in Appendix B.

2.3. Determination of Equivalent Capacitances in Four-Capacitance Model

The capacitive WPT system of Fig. 2.12 is effectively a resonant converter that is tuned to operate at a fixed frequency (for example, an ISM-band frequency of 6.78 MHz or 13.56 MHz). To reliably predict the performance of this resonant converter and to correct for deviations from the predicted performance, the inductance and capacitance values in the circuit must be known to a high degree of accuracy. This is illustrated in Fig. 2.13, which shows the deviation in the output power of a 6.78-MHz 1-kW capacitive WPT system from its expected value due to errors in the measured value of the equivalent capacitance $C_{p1,eqv}$. The percentage deviation in the output power ($\Delta P_{\mathrm{OUT}}/P_{\mathrm{OUT}}$) can be expressed in terms of the percentage deviation in the value of $C_{p1,eqv}$ as:

$$\frac{\Delta P_{\mathrm{OUT}}}{P_{\mathrm{OUT}}} = -\frac{1}{\left(1+\frac{V_{\mathrm{IN}}V_{\mathrm{OUT}}\omega_s C_{s,eqv}}{2P_{\mathrm{OUT}}\left(\frac{\Delta C_{p1,eqv}}{C_{p1,eqv}}\right)^2}\right)}. \tag{2.4}$$

A derivation of (2.4) is provided in Appendix C.

As can be seen from Fig. 2.13, a 10% error in the value of $C_{p1,eqv}$ can result in an 80% deviation in the output power. Similar large deviations can result from relatively small errors in measuring the other capacitances and inductances. The inductance values can be reliably measured using well-established high-frequency measurement techniques [61]. However, measuring the equivalent capacitances shown in Fig. 2.12 is more challenging, since they originate from the complex configuration of parasitic capacitances shown in Fig. 2.3. This section provides a systematic methodology to accurately determine the equivalent capacitances in the system of Fig. 2.12.

The four-capacitance model of the EV charging environment shown in Fig. 2.12 is a two-port network comprising three different capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$. The values of these three capacitances can be determined using three independent measurements. An important consideration for any such measurement is that it must preserve the circuit symmetry discussed in Section III, so as to maintain the validity of the four-capacitance model. It can be shown that there are six such symmetric

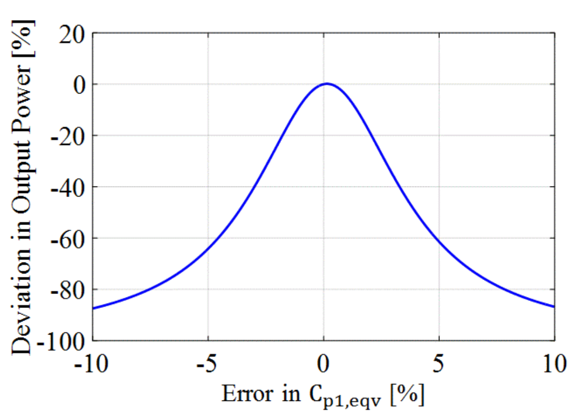


Fig. 2.13: Deviation in the output power of a 6.78-MHz 1-kW capacitive WPT system from its expected value due to errors in the measured value of the equivalent capacitance $C_{p1,eqv}$. As can be seen, a 10% error in the value of $C_{p1,eqv}$ can cause the output power to deviate by more than 80%.

measurements, as illustrated by the test setups shown in Fig. 2.14. In these tests, different pairs of nodes in the four-capacitance network are kept open / short, and the input capacitance (C_{in}) of the network is measured from one of the ports. In tests A and B, none of the node-pairs is shorted, and C_{in} is measured from the roadway side and the vehicle side, respectively. In test C, the vehicle-side plates are shorted

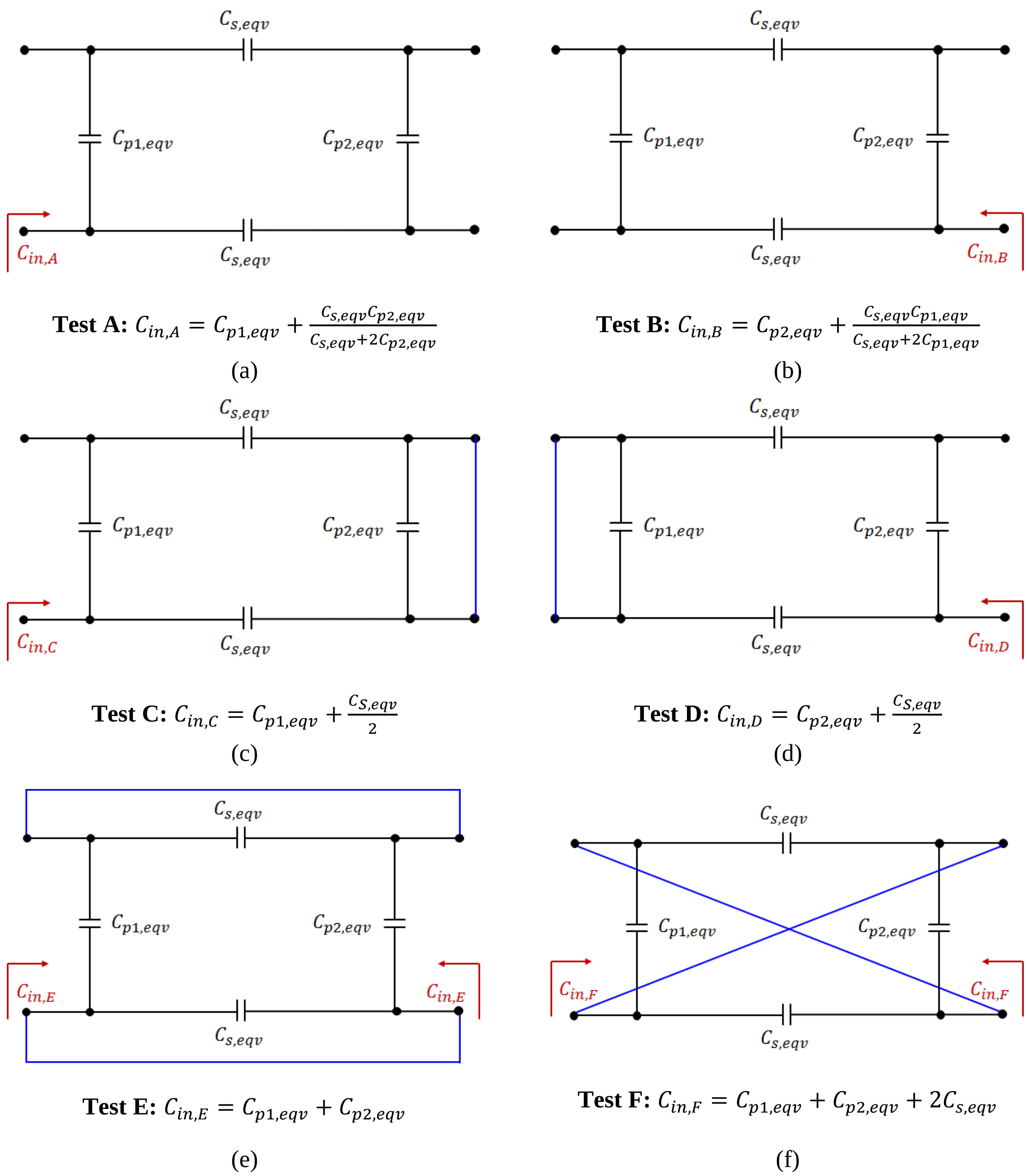


Fig. 2.14: Six possible two-port measurements in order to determine the values of the equivalent capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$ of the four-capacitance model of Fig. 2.6, while maintaining symmetry to ensure the validity of the four-capacitance model.

and C_{in} is measured from the roadway side; and in test D, the roadway-side plates are shorted and C_{in} is measured from the vehicle side. In test E, the two plates in the forward path, as well as the two plates in the return path are shorted; and finally, in test F, the plates located diagonally from one another are shorted. Note that in tests E and F, the input capacitance C_{in} is the same when measured from either the roadway side or the vehicle side. Expressions for the input capacitance C_{in} measured in each of these tests are also provided in Fig. 2.14, in terms of the equivalent shunt and series capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$.

Any three of the six tests shown in Fig. 2.14 can be used to determine the values of the three equivalent capacitances. This three-test combination can be chosen out of the six tests in twenty possible ways. However, since the capacitance values being measured are small (of the order of a few to low-tens of pF), measurement errors are likely to occur, for instance, due to equipment parasitics. These will lead to errors in the calculated values of $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$, which in turn, will cause the output power of the system to deviate from its predicted value. Therefore, it is desirable to select the three-test combination such that the measurement errors will minimally impact the output power of the capacitive WPT system. An analysis to this end is performed next.

Figure 2.15 shows the percentage errors in the values of the equivalent capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$ resulting from a 1% error in the measured value of the input capacitances (i.e., $\left|\frac{\Delta C_{in}}{C_{in}}\right| = 0.01$) for the twenty possible three-test combinations, for an example 6.78-MHz 1-kW capacitive WPT system having an input and output voltage of 300 V. Analytical expressions for the errors in $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$, and their derivations, are provided in Appendix D. As can be seen from Fig. 2.15, the measurement inaccuracies cause a much larger error in the value of the series capacitance $C_{s,eqv}$ than in the shunt capacitance $C_{p1,eqv}$ or $C_{p2,eqv}$. This is because the small value of $C_{s,eqv}$ is calculated by subtracting two larger values of measured input capacitances (C_{in}'s) from one another (for example, in

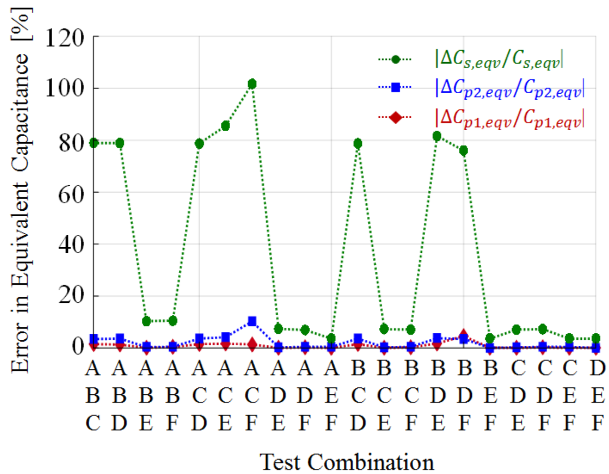


Fig. 2.15: Percentage error in the equivalent capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$ due to a 1% error in measuring the input capacitances in the twenty possible test combinations in a 6.78-MHz 1-kW capacitive WPT system having an input and output voltage of 300 V. As can be seen, the measurement error cause a much larger error in the value of the $C_{s,eqv}$ than in the other capacitances.

test combination (D, E, F), $C_{s,eqv} = \frac{1}{2}(C_{in.E} - C_{in,F})$). Therefore, a small percentage error in the measurement of each of these input capacitances causes a large percentage error in the calculated value of $C_{s,eqv}$. On the other hand, the values of $C_{p1,eqv}$ and $C_{p2,eqv}$ are close to the values of the measured input capacitances (for example, $C_{p1,eqv} = C_{in,C} - \frac{C_{s,eqv}}{2} \approx C_{in,C}$, since $C_{s,eqv}$ is very small), allowing $C_{p1,eqv}$ and $C_{p2,eqv}$ to have the same order of percentage errors as those in the measurement of C_{in}'s.

Errors in the equivalent capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$ as illustrated in Fig. 2.15 lead to deviations in the capacitive WPT system's output power. These deviations, computed numerically for the twenty possible test combinations, are shown in Fig. 2.16. As can be seen, the output power deviates the least from its predicted value for four of the test combinations: (A, E, F), (B, E, F), (C, E, F), and (D, E, F). Figure 2.16 also indicates that choosing any test combination arbitrarily may cause a significantly more deviation in the output power as compared to the prescribed four combinations (for example, choosing the combination (B, D, F) would cause a 10 times greater deviation). Any of the four combinations: (A, E, F), (B, E, F), (C, E, F), and (D, E, F) may be used to measure the values of the series and shunt equivalent capacitances ($C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$) of the four-capacitance model of

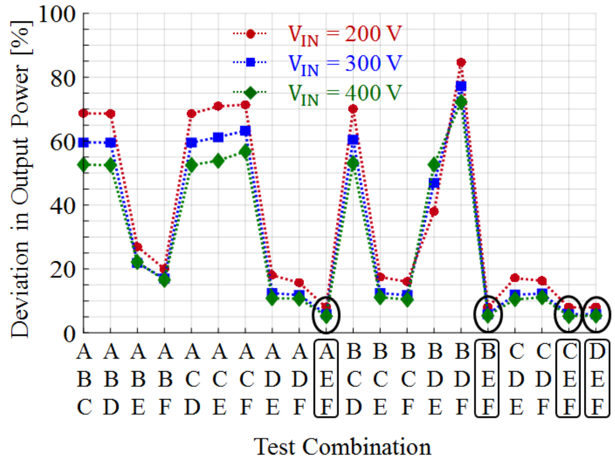


Fig. 2.16: Percentage deviation in the output power due to a 1% error in measuring the input capacitances in the 20 possible test combinations in a 6.78-MHz 1-kW 300-V-output capacitive WPT system, for three different input voltages. For all three input voltages, the test combinations (A, E, F), (B, E, F), (C, E, F), and (D, E, F) result in least deviation in output power.

Fig. 2.12. Expressions for the equivalent capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$ as obtained from these four test combinations are provided in Table 2.1.

It is interesting to note that all four prescribed test combinations include the two tests E and F (the series-short and diagonal-short tests). Any one of the remaining tests A, B, C, and D can be selected as

TABLE 2.1: EXPRESSIONS FOR THE SHUNT AND SERIES EQUIVALENT CAPACITANCES OF THE FOUR-CAPACITANCE MODEL FOR THE FOUR PRESCRIBED TEST COMBINATIONS

Test Combination	$C_{p1,eqv}$	$C_{p2,eqv}$	$C_{s,eqv}$
A, E, F	$\frac{1}{2}\left(C_{in,A}+C_{in,E}-\sqrt{(C_{in,E}-C_{in,A})(C_{in,F}-C_{in,A})}\right)$	$\frac{1}{2}\left(-C_{in,A}+C_{in,E}+\sqrt{(C_{in,E}-C_{in,A})(C_{in,F}-C_{in,A})}\right)$	$\frac{1}{2}(-C_{in,E}+C_{in,F})$
B, E, F	$\frac{1}{2}\left(C_{in,E}-C_{in,B}+\sqrt{(C_{in,E}-C_{in,B})(C_{in,F}-C_{in,B})}\right)$	$\frac{1}{2}\left(C_{in,B}+C_{in,E}-\sqrt{(C_{in,E}-C_{in,B})(C_{in,F}-C_{in,B})}\right)$	$\frac{1}{2}(-C_{in,E}+C_{in,F})$
C, E, F	$\frac{1}{4}(4C_{in,C}+C_{in,E}-C_{in,F})$	$\frac{1}{4}(-4C_{in,C}+3C_{in,E}+C_{in,F})$	$\frac{1}{2}(-C_{in,E}+C_{in,F})$
D, E, F	$\frac{1}{4}(-4C_{in,D}+3C_{in,E}+C_{in,F})$	$\frac{1}{4}(4C_{in,D}+C_{in,E}-C_{in,F})$	$\frac{1}{2}(-C_{in,E}+C_{in,F})$

the third one; however, either test C or test D are recommended since these generate the values of $C_{p1,eqv}$ and $C_{p2,eqv}$ with simpler calculations (see Table 2.1). It is also interesting to observe from Figs. 2.15 and 2.16 that the output power deviates more from its expected value for those test combinations where the error in $C_{s,eqv}$ is higher, and deviates the least for the four prescribed test combinations, where the error in the value of $C_{s,eqv}$ is also the smallest; indicating that the error in $C_{s,eqv}$ is the dominant factor behind the output power deviation.

To understand why the error in $C_{s,eqv}$ is the smallest for the four prescribed test combinations, the twenty test combinations of Fig. 2.16 can be divided into three categories: lowest-error combinations (AEF, BEF, CEF, DEF), medium-error combinations (ABE, ABF, ADE, ADF, BCE, BCF, CDE, CDF), and large-error combinations (ABC, ABD, ACD, ACE, ACF, BCD, BDE, BDF). Reasons for the errors in $C_{s,eqv}$ for these three categories can then be analyzed as follows.

a) Lowest-error combinations: For all these combinations, $C_{s,eqv}$ depends only on the measured input capacitances of tests E and F, and can be expressed as:

$$C_{s,eqv} = \frac{1}{2}(-C_{in,E} + C_{in,F}). \tag{2.5}$$

Therefore, the maximum possible error in $C_{s,eqv}$, as discussed in Appendix D, is given by:

$$\left|\Delta C_{s,eqv}\right| = \frac{1}{2}\left(\left|\Delta C_{in,E}\right| + \left|\Delta C_{in,F}\right|\right). \tag{2.6}$$

b) Medium-error combinations: In all these combinations, the value of $C_{s,eqv}$ depends on the measured input capacitances in all three tests. For example, for the test combination CDE, $C_{s,eqv}$ can be expressed as:

$$C_{s,eqv} = C_{in,C} + C_{in,D} - C_{in,E}. \tag{2.7}$$

The corresponding maximum error in $C_{s,eqv}$ is given by:

$$\left|\Delta C_{s,eqv}\right| = \left|\Delta C_{in,C}\right| + \left|\Delta C_{in,D}\right| + \left|\Delta C_{in,E}\right|. \tag{2.8}$$

c) Large-error combinations: In these combinations, the value of $C_{s,eqv}$ depends on the measured input capacitances of either tests A and C, or tests B and D. For example, let us consider the test combination ABC. The capacitance $C_{s,eqv}$ for this test combination can be approximated as:

$$C_{s,eqv} \approx 2\sqrt{C_{p2,eqv}\left(C_{in,C} - C_{in,A}\right)}. \tag{2.9}$$

The maximum error in $C_{s,eqv}$ can then be expressed as:

$$\left|\Delta C_{s,eqv}\right| \approx \left(2\frac{C_{p2,eqv}}{C_{s,eqv}}\right)\left(\left|\Delta C_{in,C}\right| + \left|\Delta C_{in,A}\right|\right) + \frac{C_{s,eqv}}{2}\left(\frac{\Delta C_{p2,eqv}}{C_{p2,eqv}}\right)$$

$$\approx \left(2\frac{C_{p2,eqv}}{C_{s,eqv}}\right)\left(\left|\Delta C_{in,C}\right| + \left|\Delta C_{in,A}\right|\right). \tag{2.10}$$

The above approximation in (10) is valid since the term $\frac{C_{s,eqv}}{2}\left(\frac{\Delta C_{p2,eqv}}{C_{p2,eqv}}\right)$ is a product of two small quantities, $C_{s,eqv}$ (which is small in a large air-gap capacitive WPT system), and the relative error $\left(\frac{\Delta C_{p2,eqv}}{C_{p2,eqv}}\right)$ (which is small as can be seen from Fig. 2.16), and can be neglected.

Assuming that all input capacitance measurements have the same error, it is easy to see that the error in $C_{s,eqv}$ as given by (2.6) is less than that given by (8): (2.6) is one half the sum of two input capacitance errors, whereas (8) is the full sum of three input capacitance errors. Similarly, (2.6) also represents a smaller error in $C_{s,eqv}$ than (10). In this case, the two equations both involve the sum of two input capacitance errors; however, in (2.6) this sum is multiplied by a factor of ½, whereas in (10) it is multiplied by a factor of $2\frac{C_{p2,eqv}}{C_{s,eqv}}$. In a capacitive WPT system for EV charging, the air-gap is much larger than the distance between the vehicle-side plates and the vehicle chassis. Therefore, for such systems, $C_{p2,eqv}$ is typically much larger than $C_{s,eqv}$, making the factor $2\frac{C_{p2,eqv}}{C_{s,eqv}}$ much greater than 2.

Hence, the error in $C_{s,eqv}$, and consequently, the deviation in output power, is least for the test combinations AEF, BEF, CEF and DEF.

The test combinations prescribed above minimize the deviation in output power for a given percentage error in the measured value of the input capacitance C_{in} (1% in the above examples). This deviation can be further reduced by reducing the error in measuring C_{in} itself. A measurement method to achieve this is shown in Fig. 2.17. In this proposed method, first the symmetrically split inductors of the matching networks of the system of Fig. 2.12 are built and connected to the coupling plates. Next, a sinusoidal voltage of variable frequency is applied at the input terminal of the inductors, and the frequency is varied until resonance is achieved. An effective way to sense the resonance is to observe when the inductor current is maximized. If the resonant frequency of the system is f_0, the input capacitance can be determined from:

$$C_{in,i} = \frac{1}{4\pi^2 f_0^2 L}, \tag{2.11}$$

where $C_{in,i}$ is the input capacitance for test i, and L is the total matching network inductance. An advantage of this measurement technique is that it is not affected by the stray capacitance between the leads of the variable frequency source, since this stray capacitance does not take part in the resonance. Furthermore, since the matching network inductors are already included in the test setup, any additional parasitic capacitance arising from their connection to the coupling plates in the actual EV charging

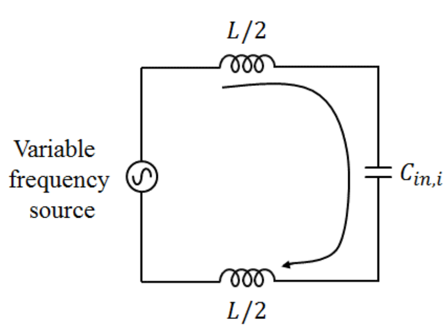


Fig. 2.17: Proposed method to measure the input capacitance in the proposed tests.

system is already accounted for in these measurements. Therefore, the proposed methodology significantly reduces errors in measuring the equivalent capacitances of the four-capacitance model.

2.4. Prototype Design and Experimental Results

In order to validate the proposed modeling and measurement approaches, two prototype capacitive WPT systems based on the topology shown in Fig. 2.12 are designed, built and tested. The schematic of the prototypes is shown in Fig. 2.18, and photographs of the prototypes, including their coupling plates, are shown in Fig. 2.19. The capacitive coupler of the first prototype system comprises 12.25 cm × 12.25 cm square copper plates with a plate area of 150 cm^2, while the second prototype uses 12.25-cm diameter circular coupling plates with a plate area of 118 cm^2. The plate-pairs in both the prototypes are vertically separated by a 12-cm air-gap. The practical EV charging environment is emulated by placing the coupling plates between two 1 m × 1 m aluminium sheets that model the roadway and the vehicle chassis. The matching network inductances and capacitances, along with the dimensional parameters of the two prototype systems, are listed in Table 2.2. The matching networks are designed using the methodology presented in the next chapter. The vertical and lateral spacing of the coupling plates and the aluminium sheets is adjusted to obtain the desired values of the shunt capacitances $C_{p1,eqv}$ and

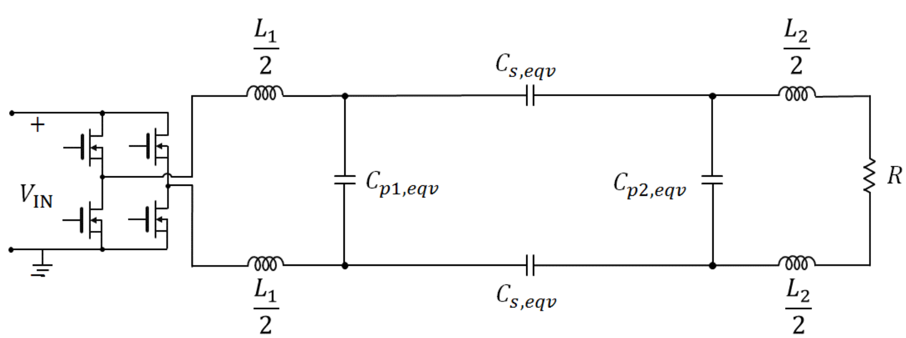
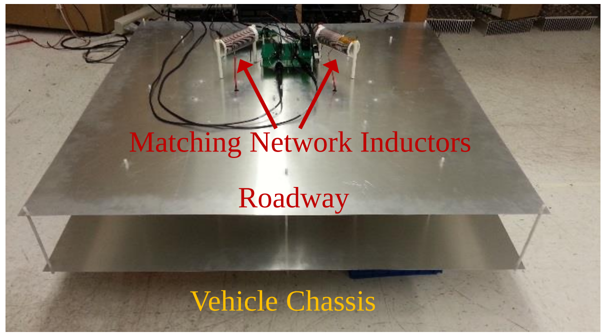
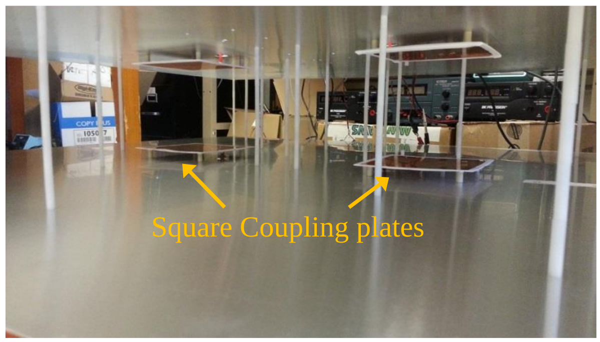


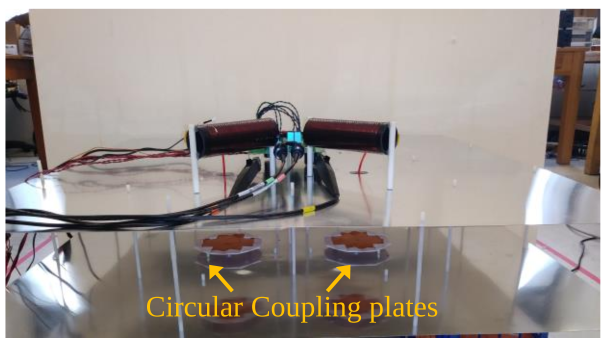
Fig. 2.18: Circuit schematic of 6.78-MHz, 12-cm air-gap prototype capacitive WPT systems.



(a)



(b)



(c)

Fig. 2.19: Photographs of the prototype capacitive WPT systems: (a) Top-view of the prototype system showing the inverter and the inductors of the roadway-side matching network, and (b) the square coupling plates of the first prototype system, and (c) the circular coupling plates of the second prototype system.

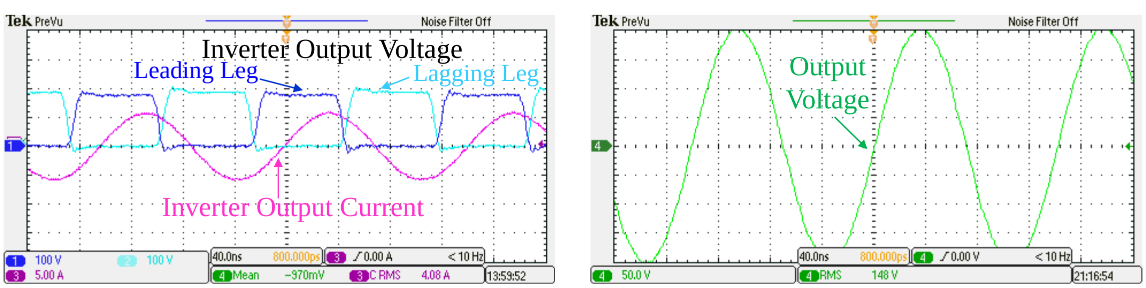
$C_{p2,eqv}$ of the four-capacitance model, which are then used to realize the matching network capacitances entirely, eliminating the requirement for any discrete capacitors. The values of these equivalent shunt capacitances $C_{p1,eqv}$ and $C_{p2,eqv}$ and the equivalent series capacitance $C_{s,eqv}$ are measured using the test combination (D, E, F), as outlined in Section 2.3. The matching network inductors are realized as air-core single-layer solenoids based on the design guidelines presented in [62]. The full-bridge inverters

TABLE 2.2: CIRCUIT PARAMETERS OF THE TWO PROTOTYPE CAPACITIVE WPT SYSTEMS

Prototype	Plate Shape	Plate Area [cm^2]	Plate-to-Aluminum Sheet Distance	$C_{s,eqv}$ [pF]	L_1 [μH]	L_2 [μH]	$C_{p1,eqv}$ [pF]	$C_{p2,eqv}$ [pF]
1	Square	150	1.27 cm	0.88	53	53	9.58	9.58
2	Circular	118	1.27 cm	0.7	69.2	69.2	7.95	7.95

are implemented using 650-V 30-A GaN transistors GS66508T, while the rectifier and the load are emulated by a 45-Ω resistor.

The first prototype system operates at 6.78 MHz and transfers 590 W across its 12-cm air-gap with an efficiency of 88.4%. The measured waveforms of the inverter switch-node voltage and the inverter output current are shown in Fig. 2.20(a), and the load voltage is shown in Fig. 2.20(b). It can be observed from the smooth transitions in the inverter switch-node voltages that the inverter transistors achieve zero-voltage switching (ZVS) and near-zero current switching (near-ZCS). Figure 2.21 shows the measured voltages between the roadway and the inverter ground (i.e., across the capacitance $C_{r,gnd}$), and between the roadway and the vehicle chassis (i.e., across the capacitance C_{rv}) when this prototype system is transferring 500 W. As can be seen, both the voltages are very low: the rms ac voltage across $C_{r,gnd}$ is 3.42 V, and that across C_{rv} is 3.75 V. This indicates very small parasitic currents through these capacitances, validating the effectiveness of the split-inductor matching networks as predicted in Section 2.3.



(a) (b)

Fig. 2.20: Measured waveforms of the 6.78-MHz, 12-cm air-gap, 590-W prototype capacitive WPT system: (a) inverter switch-node voltages and inverter output current and (b) load voltage.

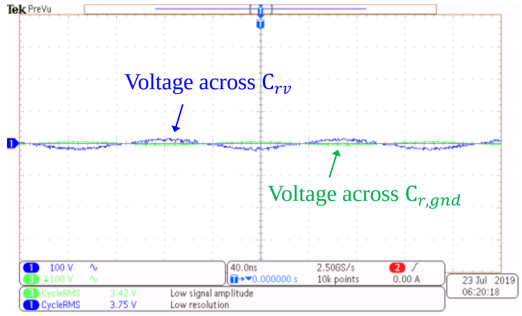
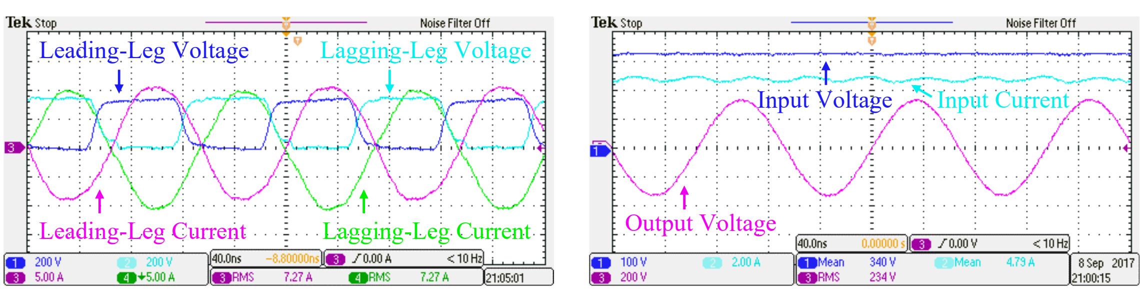


Fig. 2.21: Measured voltages across the parasitic capacitances $C_{r,gnd}$ and C_{rv} in the 6.78-MHz 12-cm air-gap 12.25 cm × 12.25 cm square-plate capacitive WPT prototype while transferring 500 W. The low values of these voltages indicate the effectiveness of the split-inductor matching networks as predicted in Section 2.2.

The second prototype also operates at 6.78 MHz and transfers up to 1217 W with an efficiency of 74.7%, achieving a power transfer density of 51.6 kW/m^2. The measured waveforms for its inverter switch-node voltage, inverter output current, and load voltage are shown in Fig. 2.22. It may be noted that the second prototype achieves ~2.6 times higher power transfer density by transferring ~ 2.1 times the power using 25% smaller coupling plates, but at the cost of ~14% reduced efficiency. The increased power transfer results in 1.8 times increased inductor currents (for example, compare the current waveforms in Figs. 2.20(a) and 2.22(a)); whereas the smaller plate area necessitates larger compensating inductors (see Table II) that have higher ac resistances. The combined effect of higher inductor currents and higher inductor resistances increases the matching network losses and lowers the system's efficiency. Figure 2.23 shows a comparison between the measured output powers of the two prototype



(a) (b)

Fig. 2.22: Measured waveforms of the 6.78-MHz, 12-cm air-gap, 1217-W prototype capacitive WPT system: (a) inverter switch-node voltages and inverter output current and (b) load voltage and dc input voltage and input current.

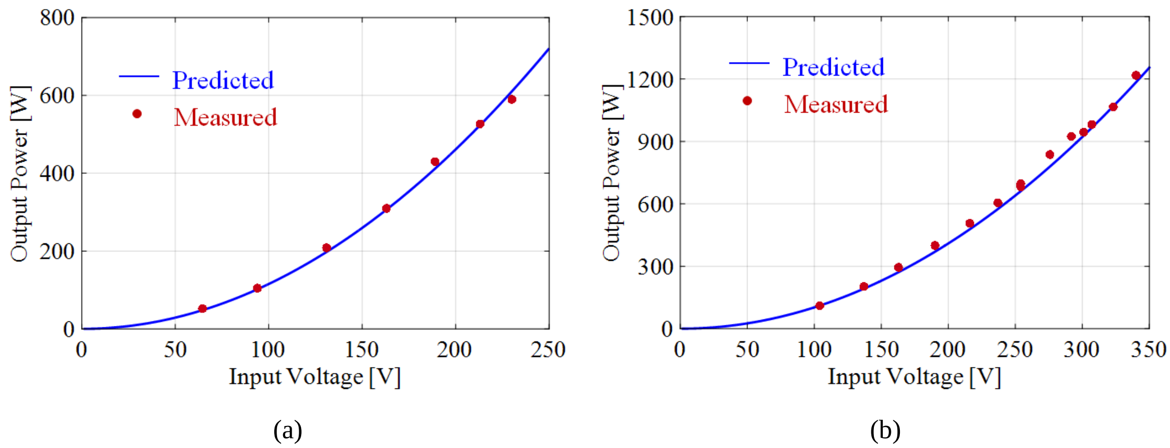


Fig. 2.23: Comparison of the measured and predicted output powers of the two prototype capacitive WPT systems: (a) 6.78-MHz 590-W prototype 150-cm^2 square coupling plates, and (b) the 6.78-MHz 1217-W prototype with 118-cm^2 circular coupling plates.

systems and the model-predicted output powers, as a function of their input voltages. As can be seen, the predictions match well with the measurements, validating the proposed design approach.

2.5. Chapter Summary

A new design approach is introduced that enables large air-gap capacitive WPT systems to achieve high performance in EV charging applications despite the presence of multiple prominent parasitic capacitances. The effect of some of the parasitic capacitances is nullified by employing split-inductor matching networks, which also enable the complex network of the remaining parasitic capacitances to be reduced to a simple four-capacitance model. These parasitic capacitances are directly utilized in realizing the matching network capacitors, eliminating the need for on-board capacitors and enhancing the reliability of the capacitive WPT system. A systematic procedure is developed to accurately measure the equivalent capacitances of the model. The proposed approach is used to design two 6.78-MHz 12-cm air-gap prototype capacitive WPT systems with capacitor-free matching networks. The first system transfers up to 590 W with an efficiency of 88.4%, while the second system transfers up to 1217 W with a power transfer density of 51.6 kW/m^2. The measured output power of the two prototype systems is shown to match well with predictions, validating the proposed design approach.

CHAPTER 3

DESIGN AND OPTIMIZATION OF MATCHING NETWORKS

A significant challenge in designing capacitive WPT systems is the requirement of substantial power transfer across the air-gap while maintaining fringing electric fields in regions surrounding the coupler within safe limits [17]. To limit fringing electric fields, the voltage across the air-gap needs to be limited. This can be achieved by using appropriate circuit stages that provide voltage and current gain to limit the displacement current through the air-gap while maintaining the required power transfer. Additionally, the coupling capacitance in medium-range capacitive WPT systems is usually low, resulting in a large capacitive reactance. This reactance must be compensated to ensure effective power transfer without requiring excessively high voltages, and to minimize reactive power flow and associated losses. Matching networks can be used to provide this required voltage or current gain and reactive compensation simultaneously [63]-[65].

The architecture of a capacitive WPT system incorporating matching networks, presented in Chapter 1, is reproduced here as Fig. 3.1. Wireless power transfer in this system is achieved using two pairs of conductive plates (C_s) separated by an air-gap. The inverter converts the dc input voltage (V_{IN}) into a high-frequency ac voltage (v_{inv}), which is fed into a matching network that steps the voltage up to a significantly higher level (v). This enables high power transfer with a low displacement current through

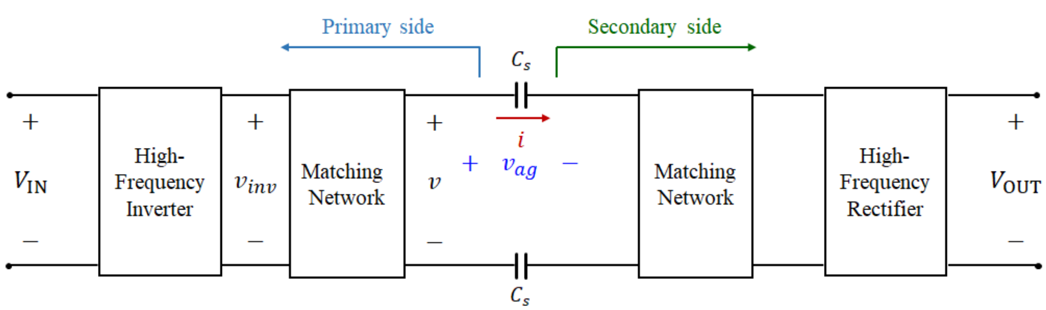


Fig. 3.1: A capacitive wireless power transfer (WPT) system architecture incorporating matching networks that provide voltage/current gain and reactive compensation.

the air-gap (i), which results in a relatively low air-gap voltage (v_{ag}) and low fringing electric fields, helping meet field safety requirements. This matching network also partially compensates the capacitive reactance of the coupling plates. The plates are followed by another matching network that steps the current back up, and the voltage down, to the level required at the output. This network also provides the remaining compensation for the plate reactance. Finally, the high-frequency rectifier interfaces the system to the load, which in many applications is a battery.

Conventionally, the matching networks on the primary and secondary sides of the capacitive WPT system of Fig. 3.1 are each further divided into two functionally distinct networks, as shown in Fig. 3.2(a). The networks adjacent to the coupling plates provide all the reactive compensation, while the networks adjacent to the inverter or the rectifier provide only voltage or current gain and no compensation. Such a distribution is intuitively reasonable, since the coupler-adjacent networks carry

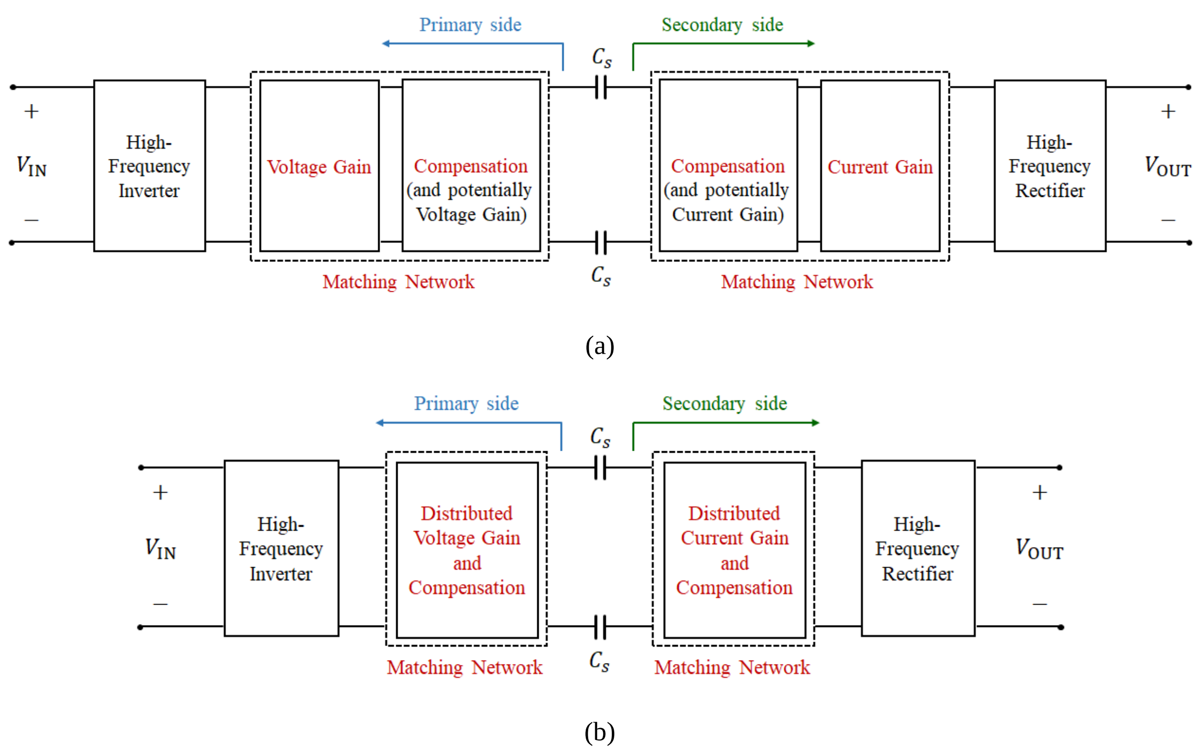


Fig. 3.2: Capacitive WPT systems with two different matching network architectures: (a) conventional matching network architecture in which compensation is only provided by a subset of the network adjacent to the coupling plates, and (b) proposed matching network architecture in which compensation is distributed across all stages of the matching network.

smaller inductor currents, and thus afford to have larger inductors for compensation without excessive losses. Various topological implementations of this approach have been explored. In these implementations, the compensation networks are realized either using inductors [15]-[67], or using L-section networks [60] (in which case the compensation networks also provide some gain). The voltage gain and current gain networks in these implementations are realized either using CLC-T networks [66]-[67], or using LCL-T networks [60].

This chapter presents a new approach to designing matching networks for capacitive WPT systems. In this approach, the required compensation is not restricted to a sub-part of each matching network, as in Fig. 3.2(a), instead both gain and compensation are distributed across the matching networks, as shown in Fig. 3.2(b). This extra degree of freedom opens up the possibility of achieving a higher system efficiency. The proposed approach utilizes multistage L-section matching networks, as shown in Fig. 3.3. In this approach, each L-section stage on the primary side is designed to provide both voltage gain and compensation, while each L-section stage on the secondary side is designed to provide both current gain and compensation. The matching network efficiency is maximized by identifying the optimal number of L-section stages, and the optimal distribution of gain and compensation among these stages. This approach is shown to significantly improve the matching network efficiency compared to an alternate implementation based on the conventional approach, particularly when operating at low air-gap voltages, corresponding to desirably low fringing fields. The proposed approach also enables a better trade-off between efficiency and power transfer density, while meeting field safety requirements.

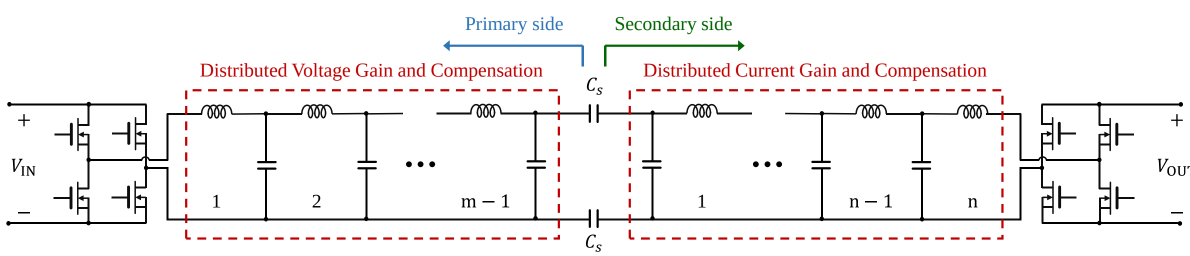


Fig. 3.3: A capacitive WPT system with gain and compensation networks implemented using multistage L-section matching networks.

The efficiency predictions of the proposed design approach are experimentally validated using three 6.78-MHz 100-W prototype capacitive WPT systems. The first prototype system comprises a single-stage matching network, the second system comprises a two-stage matching network, and the third system comprises a three-stage matching network on either side of the capacitive coupler. The matching networks in these prototype systems achieve an overall efficiency (primary and secondary sides combined) of 82.2%, 89.4% and 90.7%, respectively, which closely match the theoretical predictions. The performance of the two-stage prototype system is compared with a conventionally designed 6.78-MHz 100-W capacitive WPT prototype. It is shown that the prototype designed with the proposed approach achieves significantly higher efficiency.

3.1. Design Framework for Matching Networks of Capacitive WPT Systems

The proposed approach optimizes the design of multistage L-section matching networks for capacitive WPT systems. L-section networks are selected because for a given gain, they are typically the most efficient among the common matching network topologies [63]-[64]. Multistage networks are considered because capacitive WPT systems typically require large gain and compensation. Distributing this requirement among multiple stages allows each stage to have substantially lower losses than a single-stage network that provides the full gain and compensation. Therefore, multistage designs can potentially be more efficient than single-stage designs, as further discussed and supported by analytical optimization results in Section 3.3 and validated through experiment in Section 3.6.

Multistage L-section matching networks have been recently analyzed in the context of resonant power converters, where they are designed to provide gain but no reactive compensation [64], [65]. Since the two multistage networks in the capacitive WPT system of Fig. 3.3 together need to compensate for the reactance of the coupling plates, the approaches of [64], [65] are not directly applicable to designing these networks. However, the design framework for L-section stages proposed in [65] allows each stage of a multistage network to have complex input and load impedances, making this framework utilizable for designs that require compensation.

In the design framework of [65], an L-section stage in a multistage matching network is characterized by three quantities: G_i, the current gain provided by the stage; Q_{in}, the input impedance characteristic of the stage, and Q_{load}, the load impedance characteristic of the stage. These quantities are defined in Fig. 3.4 for the two types of L-section stages used in the capacitive WPT system of Fig. 3.3. Given required values of G_i, Q_{in}, Q_{load} and the load resistance R_{load} for each L-section stage of the voltage gain and compensation network in the capacitive WPT system of Fig. 3.3, the inductance and capacitance values of the stage can be determined using the following expressions:

$$L = \frac{\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}+G_i^2 Q_{in}\right)R_{load}}{2\pi f_s}, \tag{3.1a}$$

$$C = \frac{1-G_i^2}{2\pi f_s\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}-G_i^2 Q_{load}\right)R_{load}}. \tag{3.1b}$$

Here, f_s is the operating frequency of the system. Similarly, the expressions for the inductance and capacitance values for each L-section stage of the current gain and compensation network of the capacitive WPT system of Fig. 3.3 are given by:

$$L = \frac{\left(\sqrt{(G_i^2-1)+G_i^2 Q_{in}^2}-Q_{load}\right)R_{load}}{2\pi f_s}, \tag{3.2a}$$

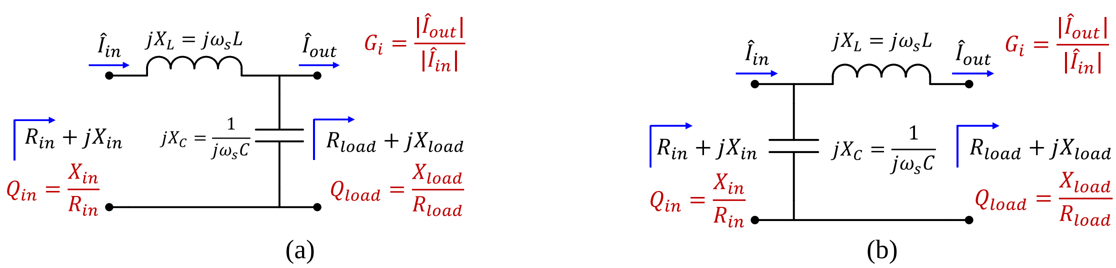


Fig. 3.4: Two types of L-section stages utilized in the multistage matching networks of the capacitive WPT system of Fig. 3.3: (a) voltage gain and compensation stage, and (b) current gain and compensation stage.

$$C = \frac{1-\frac{1}{G_i^2}}{2\pi f_s\left(\sqrt{(G_i^2-1)+G_i^2 Q_{in}^2}+Q_{in}\right)R_{load}}. \tag{3.2b}$$

Derivations of these inductance and capacitance expressions can be found in [65].

This chapter leverages the above framework to design multistage L-section networks in capacitive WPT systems that provide both gain and compensation. The gain provided by each stage is directly quantified by its current gain G_i, while the compensation provided by the stage can be expressed in terms of its impedance characteristics Q_{in} and Q_{load}, and its current gain G_i, as:

$$\Delta X = X_{in} - X_{load} = (G_i^2 Q_{in} - Q_{load})\, R_{load}. \tag{3.3}$$

The next subsection presents an approach built upon this framework to optimally design the matching networks in the capacitive WPT system of Fig. 3.3.

For brevity, the voltage gain and compensation network in Fig. 3.3 is hereafter referred to as the primary-side network, and its stages as primary-side stages; and the current gain and compensation network is referred to as the secondary-side network, and its stages as secondary-side stages. The primary-side network and the secondary-side network together are referred to as the overall matching network.

3.2. Optimization of Multistage Matching Networks for Capacitive WPT Systems

The objective of the proposed optimization approach is to maximize the efficiency of the overall matching network in the capacitive WPT system of Fig. 3.3. This objective is achieved by identifying the optimal number of stages in the primary-side and secondary-side networks, and the optimal distribution of gains (G_i's) and compensations (expressed in terms of the impedance characteristics Q_{in}'s and Q_{load}'s) among these stages. The first step in optimizing the overall matching network efficiency is to express the efficiency of an L-section stage in terms of its current gain and impedance characteristics. The losses in an L-section stage originate from winding and core losses in the inductor, and conduction and dielectric losses in the capacitor. These losses are quantified by the unloaded quality factors, $Q_L = \frac{2\pi f_s L}{R_L}$ for the inductor, and $Q_C = \frac{1}{2\pi f_s C R_C}$ for the capacitor, where R_L and R_C are the equivalent series resistances of the inductor and the capacitor, respectively. In most systems of practical interest, capacitors are much more efficient than inductors (i.e., $Q_C \gg Q_L$). Assuming low losses, and neglecting capacitor losses in comparison to inductor losses, the efficiency of an L-section stage in a multistage matching network can be approximated by:

$$\eta \approx 1 - \frac{Q_{eff}}{Q_L}. \tag{3.4}$$

Here, Q_{eff} is an effective transformation factor associated with the stage. A derivation of this efficiency expression is provided in [65]. Expressions for the effective transformation factor Q_{eff} for the two types of L-section stages (primary-side stage and secondary-side stage) utilized in the capacitive WPT system of Fig. 3.3 are listed in Table 3.1, and also derived in [65]. As can be seen, the effective transformation factor of an L-section stage is a function of the current gain (G_i) and the impedance characteristics (Q_{in} and Q_{load}) of the stage. Therefore, the efficiency of the stage depends on the gain and compensation it provides. Figure 5 shows the efficiency of an example L-section stage of the primary-side network as a function of the current gain (G_i) and the compensation (ΔX, as expressed in (3.1)) it provides, for an inductor quality factor Q_L of 200. As can be seen, the stage is less efficient when it has to provide a lower current gain G_i, i.e., a higher current step-down, or a larger compensation.

TABLE 3.1. EXPRESSIONS FOR THE EFFECTIVE TRANSFORMATION FACTOR Q_{eff} FOR THE L-SECTION STAGES OF FIG. 3.4

L-section Stage Type	Functionality	Expression for $\boldsymbol{Q_{eff}}$
Primary-side stage (Fig. 3.4(a))	Voltage step-up / Current step-down ($\boldsymbol{G_i \leq 1}$)	$\boldsymbol{\frac{1}{G_i}\sqrt{1 - G_i^2 + Q_{load}^2} + Q_{in}}$
Secondary-side stage (Fig. 3.4(b))	Current step-up / Voltage step-down ($\boldsymbol{G_i \geq 1}$)	$\boldsymbol{G_i\sqrt{1 - \frac{1}{G_i^2} + Q_{in}^2} - Q_{load}}$

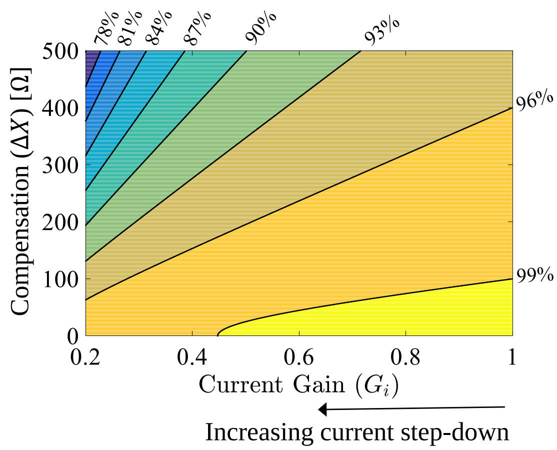


Fig. 3.5: Contour plot showing the efficiency of an L-section stage of the primary-side matching network of a capacitive WPT system, as a function of its current gain G_i and compensation ΔX. Note that a lower current gain value corresponds to a higher current step-down.

Similarly, an L-section stage of the secondary-side network is less efficient when it has to provide a higher current step-up, or a larger compensation.

Assuming that each stage of the matching networks in the capacitive WPT system of Fig. 3.3 is highly efficient, and has the same inductor quality factor, the overall efficiency of its m-stage primary-side network and n-stage secondary-side network can be expressed using (3.4) as:

$$\eta_{mn} = \prod_{p=1}^{m}\left(1 - \frac{Q_{eff,pri,p}}{Q_L}\right)\prod_{q=1}^{n}\left(1 - \frac{Q_{eff,sec,q}}{Q_L}\right)$$

$$\approx \left(1 - \frac{\sum_{p=1}^{m} Q_{eff,pri,p}}{Q_L}\right)\left(1 - \frac{\sum_{q=1}^{n} Q_{eff,sec,q}}{Q_L}\right)$$

$$\approx 1 - \frac{\sum_{p=1}^{m} Q_{eff,pri,p} + \sum_{q=1}^{n} Q_{eff,sec,q}}{Q_L}. \tag{3.5}$$

Here, $Q_{eff,pri,p}$ and $Q_{eff,sec,q}$ are the effective transformation factors of the p-th and q-th stages of the primary-side and secondary-side networks, respectively. It is apparent from the form of (3.5) that maximizing the overall matching network efficiency η_{mn} is equivalent to minimizing the sum of the effective transformation factors of all the stages, $\sum_{p=1}^{m} Q_{eff,pri,p} + \sum_{q=1}^{n} Q_{eff,sec,q}$ (as expressed below in (6a)).

The capacitive WPT system of Fig. 3.3 enforces four constraints on this minimization, as illustrated in Fig. 3.6. First, the input impedance of the first stage of the primary-side network ($Z_{in,pri,1}$ in Fig. 3.6) must be near-resistive for effective power transfer but sufficiently inductive to achieve zero-voltage switching (ZVS) of the inverter transistors. This imposes a constraint on the input impedance characteristic of the first stage of the primary-side network ($Q_{in,pri,1} = X_{in,pri,1}/R_{in,pri,1}$), as expressed in (6b). Second, the load impedance of the last (n-th) stage of the secondary-side network ($Z_{load,sec,n}$ in Fig. 3.6) must be sufficiently capacitive to achieve ZVS of the rectifier transistors. This results in a constraint on the load impedance characteristic of the last stage of the secondary-side network ($Q_{load,sec,n} = X_{load,sec,n}/R_{load,sec,n}$), as expressed in (6c). Third, the load impedance of the last (m-th) stage of the primary-side network, $Z_{load,pri,m}$, and the input impedance of the first stage of the secondary-side network, $Z_{in,sec,1}$, are related to one another by the reactance of the coupling plates of the capacitive WPT system, X_s $(= -\frac{1}{2\pi f_s C_s})$. The resultant constraint on the load impedance characteristic of the last primary-side stage ($Q_{load,pri,m} = X_{load,pri,m}/R_{load,pri,m}$) and the input impedance characteristic of the first secondary-side stage ($Q_{in,sec,1} = X_{in,sec,1}/R_{in,sec,1}$) is expressed in

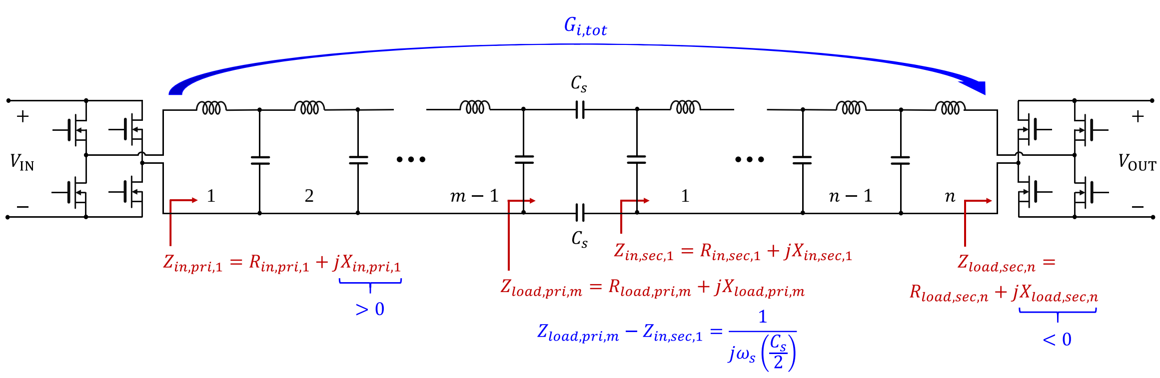


Fig. 3.6: The current gains and input and load impedances of the L-section stages of the primary-side and secondary-side networks of the capacitive WPT system of Fig. 3.3 that have constraints on them.

(6d). Finally, the total current gain required from the overall matching network, denoted by $G_{i,tot}$ in Fig. 3.6, which is the product of the current gains provided by the stages of the primary-side network and the stages of the secondary-side network, is determined by the specified input and output voltages (V_{IN} and V_{OUT}, respectively), and the topology of the inverter and the rectifier. This constraint is mathematically expressed in (6e). With these constraints, the optimization problem can be formally expressed as:

$$\min\left(\sum_{p=1}^{m} Q_{eff,pri,p} + \sum_{q=1}^{n} Q_{eff,sec,q}\right), \tag{3.6a}$$

subject to:

$$Q_{in,pri,1} = \tan\phi_{inv} = \tan\left(\cos^{-1}\frac{1}{1+\frac{2\pi k_{inv} V_{\mathrm{IN}}^2 f_S C_{oss,inv}}{P_{\mathrm{OUT}}}}\right), \tag{3.6b}$$

$$Q_{load,sec,n} = \tan\phi_{rec} = \tan\left(-\cos^{-1}\frac{1}{1+\frac{2\pi\sqrt{2k_{rec}} V_{\mathrm{OUT}}^2 f_S C_{oss,rec}}{P_{\mathrm{OUT}}}}\right), \tag{3.6c}$$

$$Q_{in,sec,1} - Q_{load,pri,m} = \frac{4|X_s|P_{\mathrm{OUT}}}{k_{inv}\sqrt{2k_{rec}}V_{\mathrm{IN}}V_{\mathrm{OUT}}\cos\phi_{inv}\cos\phi_{rec}} \frac{\prod_{p=1}^{m} G_{i,pri,p}}{\prod_{q=1}^{n} G_{i,sec,q}}$$

$$= K_{sys}\frac{\prod_{p=1}^{m} G_{i,pri,p}}{\prod_{q=1}^{n} G_{i,sec,q}}, \tag{3.6d}$$

$$\prod_{p=1}^{m} G_{i,pri,p} \prod_{q=1}^{n} G_{i,sec,q} = G_{i,tot} = \frac{k_{inv}V_{\mathrm{IN}}}{\sqrt{2k_{rec}}V_{\mathrm{OUT}}}\frac{\cos\phi_{inv}}{\cos\phi_{rec}}. \tag{3.6e}$$

Here, ϕ_{inv} (> 0) is the minimum phase difference between the inverter output voltage and output current required to achieve ZVS of the inverter transistors, ϕ_{rec} (< 0) is the minimum phase difference between the rectifier input voltage and input current required to achieve ZVS of the rectifier transistors, $C_{oss,inv}$ and $C_{oss,rec}$ are the linear-equivalent output capacitances of the inverter and rectifier transistors, respectively, k_{inv} is a factor associated with the topology of the inverter ($k_{inv} = \frac{4}{\pi}$ for the full-bridge inverter of Fig. 3.6), k_{rec} is a factor associated with the topology of the rectifier ($k_{rec} = \frac{8}{\pi^2}$ for the full-bridge rectifier of Fig. 3.6), P_{OUT} is the output power of the capacitive WPT system, $G_{i,pri,p}$ is the current gain provided by the p-th stage of the primary-side network, $G_{i,sec,q}$ is the current gain provided by the q-th stage of the secondary-side network, and K_{sys} is a system factor dependent on various design parameters of the capacitive WPT system, and given by:

$$K_{sys} = \frac{4|X_s|P_{\mathrm{OUT}}}{k_{inv}\sqrt{2k_{rec}}V_{\mathrm{IN}}V_{\mathrm{OUT}}\cos\phi_{inv}\cos\phi_{rec}}. \tag{3.7}$$

The expressions given in (3.6b)-(3.6e) and (3.7) are derived in Appendix E. Note that the values of ϕ_{inv} and ϕ_{rec} given by (3.6b) and (3.6c) correspond to the inverter and rectifier transistors achieving zero-voltage switching. In some designs, partial soft-switching may result in higher system efficiency due to lower circulating currents. In such cases, ϕ_{inv} and ϕ_{rec} can simply be given different values depending on the desired extent of soft-switching, and the subsequent analysis remains unchanged.

To solve the optimization problem of (3.6a)-(3.6e), the method of Lagrange multipliers [52] is employed, utilizing the following Lagrangian:

$$\begin{aligned}\mathcal{L} = &\left(\sum_{p=1}^{m} Q_{eff,pri,p} + \sum_{q=1}^{n} Q_{eff,sec,q}\right)\\ &+\lambda_1\left(Q_{in,pri,1} - \tan\phi_{inv}\right) + \lambda_2\left(Q_{load,sec,n} - \tan\phi_{rec}\right)\\ &+\lambda_3\left(Q_{in,sec,1} - Q_{load,pri,m} - K_{sys}\frac{\prod_{p=1}^{m} G_{i,pri,p}}{\prod_{q=1}^{n} G_{i,sec,q}}\right)\\ &+\lambda_4\left(\prod_{p=1}^{m} G_{i,pri,p}\prod_{q=1}^{n} G_{i,sec,q} - G_{i,tot}\right).\end{aligned} \tag{3.8}$$

Here, λ_1, λ_2, λ_3, and λ_4 are Lagrange multipliers. The expression in (3.6a) is minimized subject to the constraints given in (3.6b)-(3.6e) by setting the partial derivatives of the Lagrangian in (3.8) with respect to the gain and impedance characteristics of each L-section stage (G_i, Q_{in} and Q_{load}), and the Lagrange multipliers λ_1, λ_2, λ_3, and λ_4, to zero. This results in a set of simultaneous equations, which are solved to obtain the current gains and impedance characteristics, and consequently the gains and compensations provided by each stage which maximize the overall matching network efficiency. This optimal distribution of gains and compensations is described below.

3.2.1. Optimal Distribution of Gain and Compensation

In the optimized design, the current gains (G_i's) provided by the first $m-1$ stages of the primary-side network come out to be equal (denoted by $G_{i,pri,eq}$), that is:

$$G_{i,pri,1} = G_{i,pri,2} = \cdots = G_{i,pri,m-1} \stackrel{\text{def}}{=} G_{i,pri,eq}. \tag{3.9}$$

This optimal equal current gain $G_{i,pri,eq}$ can be found by solving the following equation:

$$1 + \frac{1}{G_{i,pri,eq}^{2}} = K_{sys} G_{i,pri,eq}^{m+n-2}. \tag{3.10}$$

The optimal current gains of the last $n-1$ stages of the secondary-side network are also found to be equal (denoted by $G_{i,sec,eq}$), that is:

$$G_{i,sec,n} = G_{i,sec,n-1} = \cdots = G_{i,sec,2} \stackrel{\text{def}}{=} G_{i,sec,eq}. \tag{3.11}$$

This optimal equal current gain $G_{i,sec,eq}$ can be obtained by solving the following equation:

$$1 + G_{i,sec,eq}^{2} = K_{sys} G_{i,sec,eq}^{-(m+n-2)}. \tag{3.12}$$

The optimal current gains of the remaining stages, that is, the last (m-th) stage of the primary-side network ($G_{i,pri,m}$) and the first stage of the secondary-side network ($G_{i,sec,1}$) can then be found using:

$$G_{i,pri,m} = \sqrt{\frac{G_{i,tot}}{K_{sys}} \left(\frac{G_{i,pri,eq}^{1-m} G_{i,sec,eq}^{n-1}}{G_{i,tot}} + \frac{G_{i,tot}}{G_{i,pri,eq}^{3(m-1)} G_{i,sec,eq}^{n-1}} \right)}, \tag{3.13}$$

$$G_{i,sec,1} = \sqrt{\frac{K_{sys} G_{i,tot}}{\left(\frac{G_{i,pri,eq}^{m-1} G_{i,sec,eq}^{3(n-1)}}{G_{i,tot}} + \frac{G_{i,tot}}{G_{i,pri,eq}^{m-1} G_{i,sec,eq}^{1-n}} \right)}}. \tag{3.14}$$

The optimal current gains of the primary-side and the secondary-side stages as given by (3.9)-(3.14) are shown for an example capacitive WPT system with a five-stage primary-side network and a five-stage secondary-side network (i.e., $m = n = 5$) in Fig. 3.7. This capacitive WPT system is designed for input and output voltages V_{IN} and V_{OUT} of 60 V, an output power P_{OUT} of 100 W, a coupling capacitance C_p of 10 pF (corresponding to 10 cm × 10 cm coupling plates separated by a 1.2-cm air-gap), an operating frequency of 6.78 MHz (which falls within an Industrial, Scientific, and Medical (ISM) band [68]), and inverter and rectifier transistor output capacitances $C_{oss,inv}$ and $C_{oss,rec}$ of 250 pF (corresponding to GaN Systems GS66506T enhancement-mode GaN transistors). As can be seen from Fig. 3.7, all the primary-side stages except the last (5$^{\mathrm{th}}$) stage provide equal current gain $G_{i,pri,eq}$, and the last stage provides a higher current gain (and hence, a smaller current step-down) than the first four stages. Similarly, all the secondary-side stages except the first stage provide equal current gain $G_{i,sec,eq}$, while the first stage provides a smaller current gain than the other four stages. As expected, the current gains provided by all the primary-side stages are less than 1, indicating that the primary-side network steps down current and steps up voltage, and the current gains provided by all the secondary-side stages are more than 1, indicating that the secondary-side network steps up current, and steps down voltage.

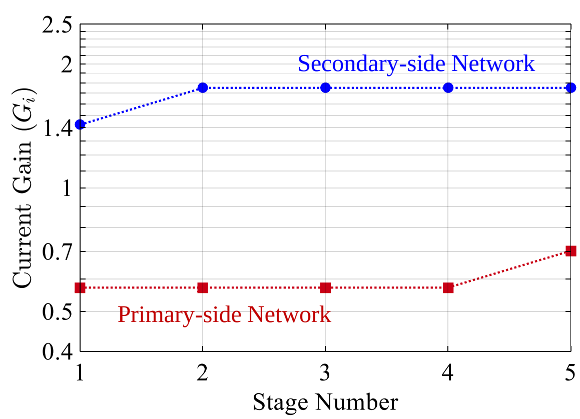


Fig. 3.7: Optimal distribution of current gains provided by the stages of the primary-side and the secondary-side networks of an example 6.78-MHz capacitive WPT system with five primary-side stages and five secondary-side stages, designed to operate with input and output voltages of 60 V, an output power of 100 W, and a coupling capacitance of 10 pF. Note that the current gain along the y-axis is shown on a logarithmic scale.

The optimal load impedance characteristics (Q_{load}'s) of the first $m-1$ primary-side stages also come out to be equal, and are related to the optimal equal current gain of these stages, $G_{i,pri,eq}$, as:

$$Q_{load,pri,1} = Q_{load,pri,2} = \cdots = Q_{load,pri,m-1} = -G_{i,pri.eq}. \quad (3.15)$$

The optimal load impedance characteristic of the last (m-th) primary-side stage is given by:

$$Q_{load,pri,m} = -\frac{G_{i,tot}}{G_{i,pri,eq}^{m-1} G_{i,sec,eq}^{n-1}}. \quad (3.16)$$

Similarly, the optimal input impedance characteristics of the last $n-1$ stages of the secondary-side network are equal, and are related to the optimal equal current gain of these stages, $G_{i,sec,eq}$, as:

$$Q_{in,sec,n} = Q_{in,sec,n-1} = \cdots = Q_{in,sec,2} = \frac{1}{G_{i,sec.eq}}. \quad (3.17)$$

Finally, the optimal input impedance characteristic of the first secondary-side stage is given by:

$$Q_{in,sec,1} = \frac{G_{i,sec,eq}^{m-1} G_{i,sec,eq}^{n-1}}{G_{i,tot}}. \quad (3.18)$$

The remaining impedance characteristics (Q_{in}'s and Q_{load}'s) can be found by noting that for a multistage network, the load impedance characteristic of a stage equals the input impedance

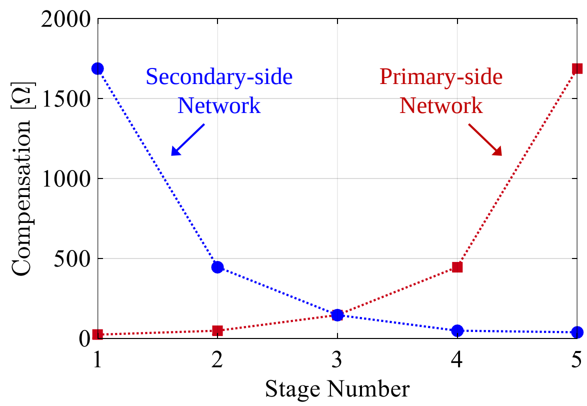


Fig. 3.8: Optimal distribution of compensations provided by the stages of the primary-side and the secondary-side networks of an example 6.78-MHz capacitive WPT system with five primary-side stages and five secondary-side stages, designed to operate with input and output voltages of 60 V, an output power of 100 W, and a coupling capacitance of 10 pF.

characteristic of the following stage, i.e., $Q_{load,p} = Q_{in,p+1}$. Using the optimal current gain and impedance characteristics given by (3.9)-(3.18), the optimal values of the compensations (ΔX's) provided by each stage of the primary-side and secondary-side networks can then be obtained using (3.3).

Figure 8 shows the compensation provided by each primary-side and secondary-side stage of the same example capacitive WPT system as that considered in Fig. 3.7. As can be seen, for both the primary-side network and the secondary-side network in the optimized design, the closer a stage is to the coupling plates, the larger the compensation it provides. This makes intuitive sense from an efficiency optimization perspective since a stage nearer to the coupling plates will have a lower inductor current and therefore affords to have a larger inductor and provide larger compensation without excessive loss.

Additional insights can be drawn from Fig. 3.9(a) and 9(b), which show the optimal gains and compensations provided by the primary-side network and the secondary-side network as a function of the required total current gain $G_{i,tot}$, for the same example capacitive WPT system as considered above. Since the primary-side network provides a current step-down, its gain is represented by the reciprocal of current gain ($1/G_i$), while the gain of the secondary-side network, which steps up current, is represented by current gain (G_i). When the total current gain $G_{i,tot}$ is equal to 1, the secondary-side network steps up the current by the same amount as the primary-side network steps it down, i.e., the two networks provide the same gain, as can be seen from Fig. 3.9(a). In such a case, they also provide the same compensation, as evident from Fig. 3.9(b). When the total current gain is greater than 1, i.e., an overall current step-up is required, the secondary-side network has to step up the current more than the primary-side network steps it down. As the secondary-side network provides a relatively higher gain (see Fig. 3.9(a)), the total matching network losses are minimized by having the secondary-side network provide a relatively smaller fraction of the required compensation (see Fig. 3.9(b)). Since the primary-side network provides a relatively smaller gain, it can afford to provide larger compensation without

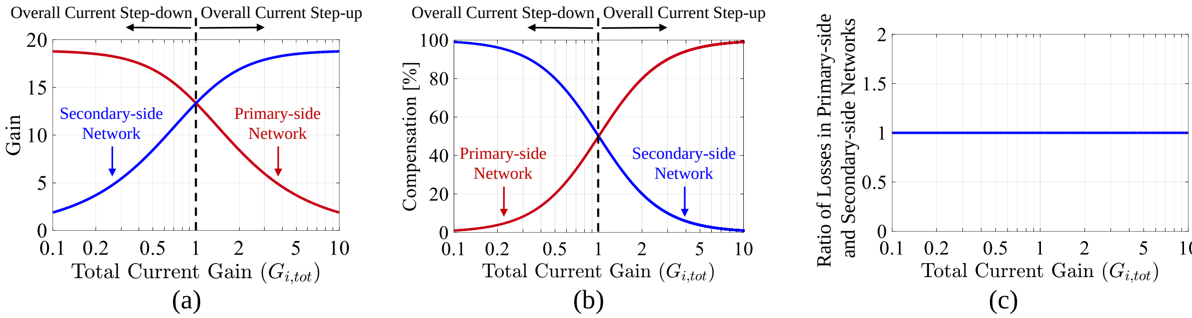


Fig. 3.9: (a) Optimal gain and (b) optimal compensation provided by the primary-side network and the secondary-side network, and (c) ratio of the resulting losses in these networks, for an example 6.78-MHz 100-W capacitive WPT system as functions of its total current gain $G_{i,tot}$. Both primary-side and secondary-side networks in this system comprise five stages, and the coupling capacitance is 10 pF. Note that the total current gain along the x-axis is shown on a logarithmic scale.

incurring excessive losses. On the other hand, for total current gains of less than 1 (overall current step-down), the primary-side network provides a relatively higher gain than the secondary-side network, but provides a smaller fraction of the required compensation. The matching network efficiency in a capacitive WPT system is thus maximized when the network providing the higher gain provides smaller compensation, and vice versa. This optimal trade-off between gains and compensations of the primary-side and the secondary-side networks allows them to share the resulting losses in the overall matching network equally for all values of total current gain $G_{i,tot}$, as can be seen from Fig. 3.9(c).

Depending on the number of stages m and n, (3.9)-(3.18) can also be used to obtain closed-form expressions for the current gains and impedance characteristics of each stage. Such closed-form expressions are provided for capacitive WPT systems with up to two primary-side stages and two secondary-side stages in Appendix F. Given the optimal current gains and impedance characteristics of all the stages, the effective transformation factor Q_{eff} for each stage can be obtained using the expressions provided in Table 3.1, and the optimized overall matching network efficiency can be determined using (3.5). The associated inductance and capacitance values of the stage can then be obtained using (3.1) and (3.2).

3.2.2. Optimal Number of Stages

It can be seen from (3.9)-(3.18) that the optimal gain and impedance characteristics of the matching network stages depend only on the system factor K_{sys}, the total current gain $G_{i,tot}$, and the number of stages in the primary-side and secondary-side networks (m and n, respectively). The effective transformation factor Q_{eff} for these stages, and in turn, the optimized overall matching network efficiency of the capacitive WPT system of Fig. 3.3, is a function of these gains and impedance characteristics. Therefore, the optimized efficiency also depends only on K_{sys}, $G_{i,tot}$, and the number of primary-side and secondary-side stages. For given system specifications (i.e., given values for K_{sys} and $G_{i,tot}$), the overall matching network efficiency can potentially be maximized by optimally selecting the number of stages on each side of the coupling plates.

In order to analyze this, the optimized overall matching network efficiency in the example capacitive WPT system considered in Section 3.2.1 is shown in Fig. 3.10 as a function of the number of primary-side stages (m) for three different values of the number of secondary-side stages (n). The inductor quality factor in this system is assumed to be 200. As can be seen, for each value of the number of

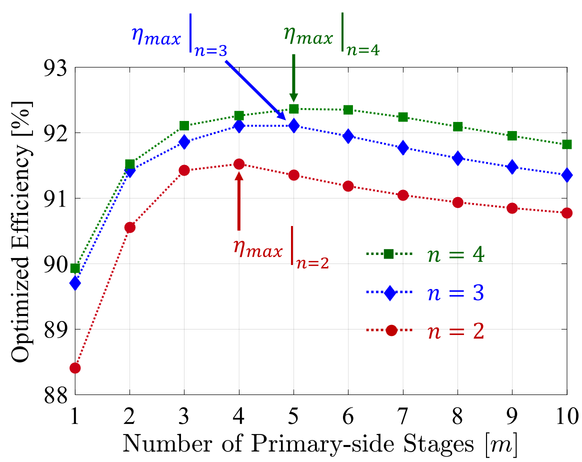


Fig. 3.10: Optimized matching network efficiency as a function of the number of primary-side stages (m) for three different values of the number of secondary-side stages (n), for a 6.78-MHz 100-W capacitive WPT system with coupling capacitance of 10 pF, input and output voltage of 60 V and inductor quality factor of 200. Since the input and output voltages are equal, this chart is also representative of the optimized matching network efficiency as a function of the number of secondary-side stages (n).

secondary-side stages n, the overall matching network efficiency initially increases with the number of primary-side stages m, and then starts to fall. The reason for this is as follows: as a stage is added to the primary-side network, the rest of its stages need to provide less gain and compensation, and hence, the losses in them reduce. Initially, this reduction in loss is more than the loss introduced by the added stage, and the overall matching network efficiency increases. Beyond a critical number of stages, the loss in the added stage exceeds the loss reduction in the remaining stages, and the overall efficiency starts to fall. However, the maximum efficiency, η_{max}, and the number of primary-side stages for which it occurs depends on the number of stages used in the secondary-side network, n. As can be seen from Fig. 3.10, the higher the number of secondary-side stages, the higher is the maximum efficiency η_{max}, and generally the higher the number of primary-side stages for which it occurs. Since the capacitive WPT system considered in this example has equal input and output voltages, Fig. 3.10 is also representative of the optimized matching network efficiency as a function of the number of secondary-side stages n, plotted for different values of the number of primary-side stages m.

Figure 10 indicates that the maximum efficiency η_{max} increases with the number of secondary-side stages n. Similarly, η_{max} would increase with the number of primary-side stages m. The variation in η_{max} is shown as a function of the number of stages (m or n) in Fig. 3.11. As can be seen, although

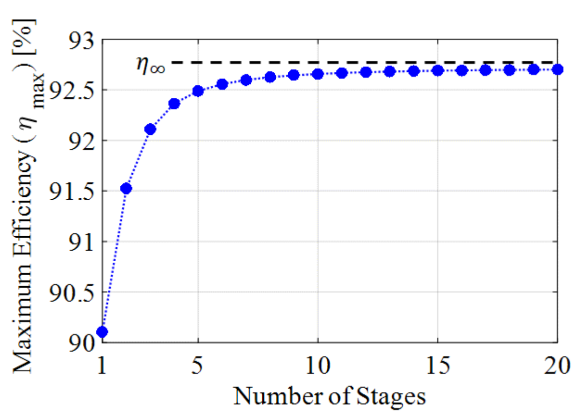


Fig. 3.11: Maximum matching network efficiency η_{max} as a function of the number of stages (primary-side or secondary-side) for a 6.78-MHz 100-W capacitive WPT system with coupling capacitance of 10 pF, input and output voltage of 60 V, and inductor quality factor of 200.

η_{max} does increase monotonically with number of stages, its relative increase reduces with each additional stage and it asymptotically approaches a value η_∞. This asymptotic maximum efficiency η_∞ can be expressed in closed-form as:

$$\eta_\infty \approx 1 - \frac{2\left(1+\ln\left(\frac{K_{sys}}{2}\right)\right)}{Q_L}. \tag{3.19}$$

A derivation of (3.19) is provided in Appendix G. It is interesting to note that given an inductor quality factor Q_L, the asymptotic maximum matching network efficiency η_∞ is solely determined by the system factor K_{sys}, i.e., by the specifications of a capacitive WPT system (see (3.7)).

The asymptotic maximum matching network efficiency η_∞ as given by (3.19) is shown in Fig. 3.12 as a function of the system factor K_{sys} for three different values of the inductor quality factor Q_L. As can be seen, the asymptotic maximum efficiency falls as the value of K_{sys} increases. This relationship between K_{sys} and efficiency can be understood and valuable insights gained by expanding the expression for K_{sys} given in (3.7) into the following form:

$$K_{sys} = \frac{2\sqrt{2}}{\pi\epsilon_0\beta k_{inv}\sqrt{k_{rec}}}\frac{d}{f_s}\frac{P_{\mathrm{OUT}}}{2A}\frac{1}{V_{\mathrm{IN}}V_{\mathrm{OUT}}}\frac{1}{\cos\phi_{inv}\cos\phi_{rec}}. \tag{3.20}$$

This expression is obtained by rearranging the terms in (3.7) after expressing the coupling capacitance C_p as $\beta\frac{\epsilon_0 A}{d}$, where ϵ_0 is the permittivity of free space, A is the area of each coupling plate, d is the length of the air-gap, and β (>1) is a factor that accounts for the additional capacitance resulting from fringing electric fields [69]. As can be seen from (3.20), the value of K_{sys} increases when the air-gap length d is increased or when the operating frequency f_s is decreased. In both cases, the reactance of the coupling plates increases and larger compensating inductances are required, resulting in higher inductor losses. This suggests that in order to maintain efficiency, systems with larger air-gaps can be designed to operate at proportionally higher frequencies, as that would avoid an increase in K_{sys} and a resultant drop in

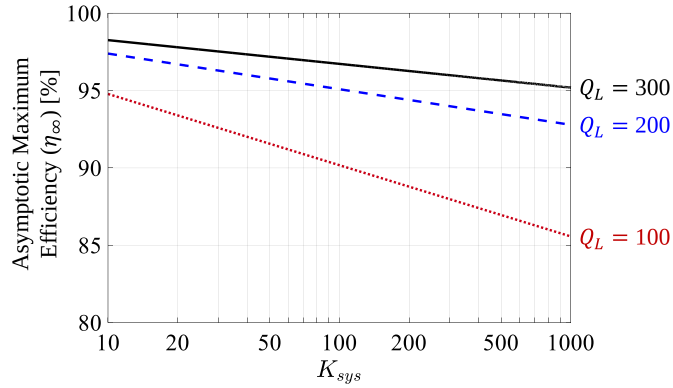


Fig. 3.12: Asymptotic maximum efficiency η_∞ of the overall matching network of the capacitive WPT system of Fig. 3.3 as a function of the system factor K_{sys} for different inductor quality factors.

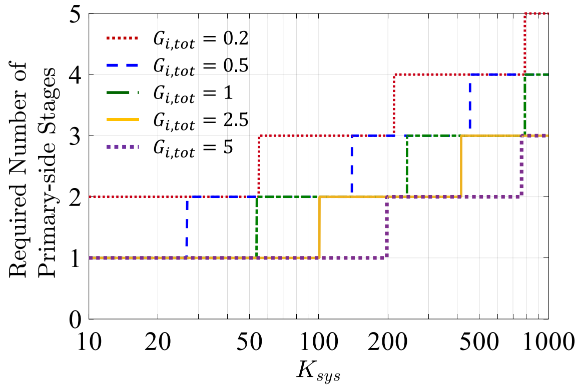
efficiency. Similarly, K_{sys} increases, and efficiency falls, when a higher power transfer density ($P_{\text{OUT}}/2A$) is targeted by increasing the output power P_{OUT} while keeping the plate area (A) unchanged. With an increased output power, the secondary-side network is loaded with a smaller effective resistance (R_{load}). Hence, according to (3.3), the secondary-side network needs to provide a larger current step-up (G_i) to maintain the required compensation (ΔX). Also, the primary-side network has to provide a larger current step-down to meet the overall gain requirement. These higher gain requirements increase the losses in the primary-side and the secondary-side networks, reducing the overall matching network efficiency. This efficiency degradation can be avoided by scaling up the plate area A in proportion to the output power P_{OUT}, as a larger plate area increases the coupling capacitance and reduces the required compensation, counteracting the negative impact of higher gains. The impact of the other parameters comprising K_{sys} on efficiency can be similarly understood.

3.3. Design Guidelines

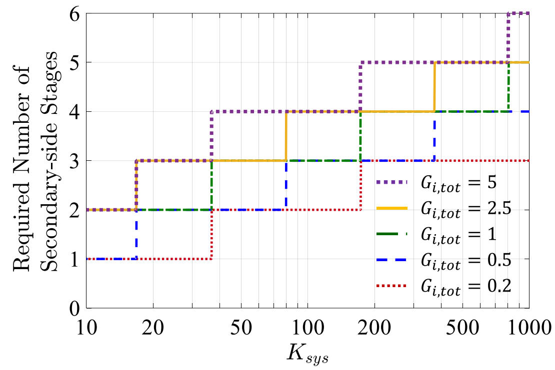
As discussed earlier and evident from Fig. 3.11, although the overall matching network efficiency increases with number of stages, the increment in efficiency becomes smaller with each additional stage. Furthermore, multistage matching networks with a very large number of stages may suffer from additional losses due to interconnects and variation in inductor quality factor, and may have undesirably large size. This section provides guidelines to select a reasonable number of matching network stages in a capacitive WPT system while maintaining high efficiency.

First, given the system specifications, the value of the system factor K_{sys} can be computed using (3.7). For this value of K_{sys} and an expected inductor quality factor Q_L, the asymptotic maximum matching network efficiency η_∞ can be computed using (3.19). Next, a target matching network efficiency suitable for the application can be selected. For many applications, a reasonable choice could be 99% of the asymptotic maximum efficiency. In order to have a reasonable system size and cost, the matching network can be designed with the minimum total number of stages $(m + n)$ which achieve this target efficiency. For such designs, the number of primary-side and secondary-side stages required to achieve 99% of the asymptotic maximum efficiency is shown as a function of the system factor K_{sys} in Figs. 3.13(a) and 3.13(b), respectively, for five different values of the total current gain $G_{i,tot}$. As can be seen, the required number of both primary-side and secondary-side stages increases with the system factor K_{sys}. This is because, as discussed in Section III(B), the higher the value of K_{sys}, the larger are the gains and/or compensations required from the primary-side and secondary-side networks. Hence, a larger number of stages is required to achieve the target efficiency. It can be further noted from Fig. 3.13 that for a high overall current step-up (e.g., $G_{i,tot} = 5$), more stages are needed in the secondary-side network than in the primary-side network. This is expected as in this case the secondary-side network has to step up the current more (five times more when $G_{i,tot} = 5$) than the primary-side network has to step it down. This higher gain burden on the secondary-side network requires it to have a larger number of stages in order to be sufficiently efficient. Similarly, more primary-side stages and fewer secondary-side stages are needed for small values of $G_{i,tot}$ (e.g., $G_{i,tot} = 0.2$).

Using Fig. 3.13 (or similar plots for a target efficiency other than 99% of the asymptotic maximum efficiency), the required number of stages in the primary-side and secondary-side networks in a capacitive WPT system can be determined by calculating only the system factor K_{sys} and total current



(a)



(b)

Fig. 3.13: (a) Number of primary-side stages and (b) number of secondary-side stages required in the capacitive WPT system of Fig. 3.3 to achieve 99% of the asymptotic maximum efficiency of Fig. 3.12 while using the least total number of stages, plotted as a function of the system factor K_{sys} for different values of the total current gain $G_{i,tot}$.

gain $G_{i,tot}$. For example, consider the capacitive WPT system of Fig. 3.3 for the same design specifications as in Section 3.2.1. The value of K_{sys} for this system is 356 (calculated using (3.7)), and the value of $G_{i,tot}$ is 1 (calculated using (6e)). To achieve 99% of the asymptotic maximum efficiency, the matching networks of this system require three stages on the primary side (according to Fig. 3.13(a)), and four stages on the secondary side (according to Fig. 3.13(b)). If the required output voltage is increased by five times to 300 V and other parameters remain unchanged, the value of K_{sys} is reduced by five times to 71.2 (see (3.7)), and the value of $G_{i,tot}$ is also reduced by five times to 0.2 (see (6e)). As can be seen from Fig. 3.13, three stages are still required on the primary side, but only two stages are now required on the secondary side. This is expected since for a smaller overall current step-up, the target efficiency can be achieved with fewer secondary-side stages, as discussed earlier in this section. Figure 14 shows charts similar to Fig. 3.13 when the target efficiency is reduced to 98% of the asymptotic maximum efficiency. With this smaller target efficiency, fewer stages are needed on both the primary and the secondary side.

To summarize the proposed design methodology, given the system specifications, that is, the air-gap, coupling area, operating frequency, output power, input and output voltages, and the phase-shifts

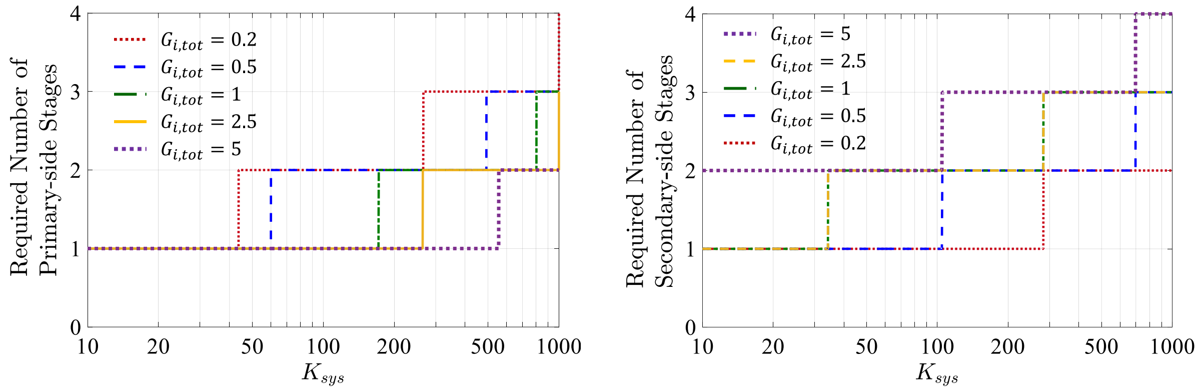


Fig. 3.14: (a) Number of primary-side stages and (b) number of secondary-side stages required in the capacitive WPT system of Fig. 3.3 to achieve 98% of the asymptotic maximum efficiency of Fig. 3.12 while using the least total number of stages, plotted as a function of the system factor K_{sys} for different values of the total current gain $G_{i,tot}$.

associated with soft-switching of the inverter and rectifier transistors, first the value of the system factor K_{sys} and the total current gain $G_{i,tot}$ are determined using (6e) and (3.20), respectively. Next, a target matching network efficiency and the corresponding required number of matching network stages are selected using the guidelines provided in this section. The optimal gains and impedance characteristics required from these stages are then determined using (3.9)-(3.18), and their inductance and capacitance values are found using (3.1) and (3.2).

3.4. Comparison between Proposed and Conventional Approaches

To demonstrate the advantages of the proposed approach to designing matching networks for a capacitive WPT system, its results are compared with those of the conventional approach. As discussed earlier, in the conventional approach compensation is provided by a subset of the matching network adjacent to the coupling plates. An implementations of this approach have been presented in [60]. Unlike the conventional approach, the proposed approach distributes compensation across the entire matching network. To compare the two approaches, a capacitive WPT system with a two-stage L-section matching network on each side of the coupling plates is designed using both approaches.

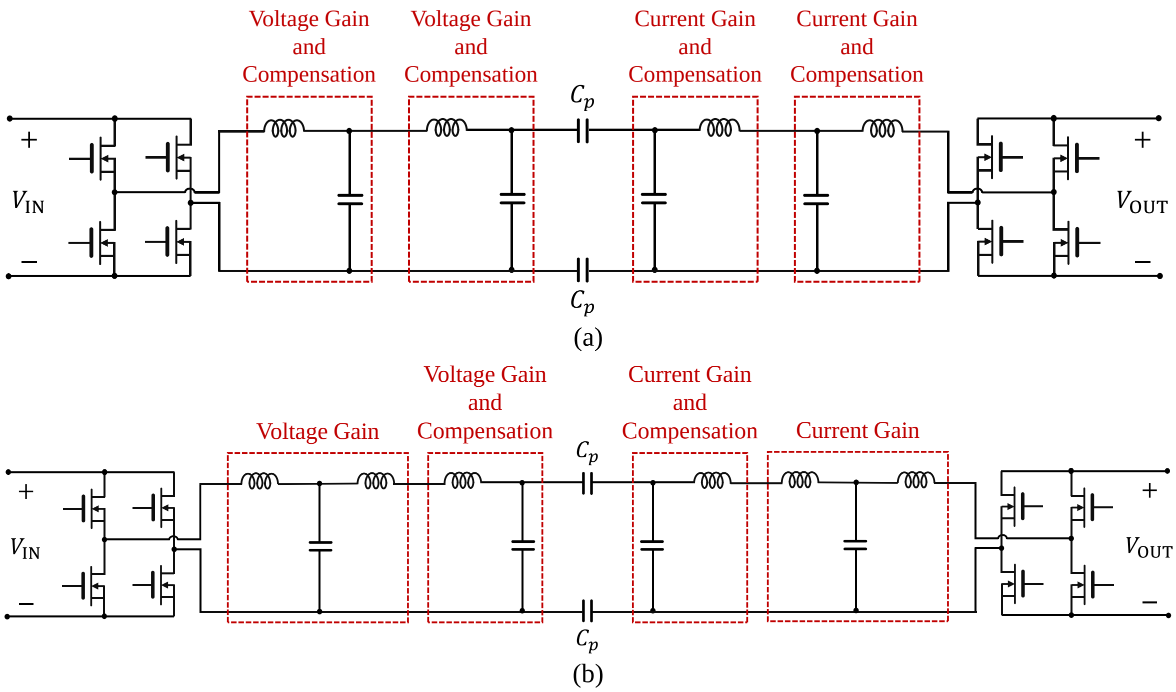


Fig. 3.15: A capacitive WPT system comprising a two-stage matching network on each side of the coupling plates designed using: (a) the proposed approach, and (b) the conventional approach. Although the matching networks in these two systems share the same topology (when the series inductors in (b) are combined), they differ in their functional detail.

In the proposed design, each L-section stage provides a fraction of the overall gain and compensation, as shown in Fig. 3.15(a). The optimal values for the gain and compensation of these stages, and the corresponding inductance and capacitance values, can be determined using the procedure outlined in Section 3.2. For the conventional design, a matching network topology identical to that of the proposed design is selected. Although both designs share the same topology, they differ in their functional detail. In the conventional design the matching network on each side of the coupling plates is functionally split into two parts, as shown in Fig. 3.15(b). One part is an L-section network adjacent to the coupling plates, and the other part is an LCL-T network adjacent to the inverter or the rectifier. The L-section networks provide all the required compensation and a portion of the required gain, while the LCL-T networks provide the remaining gain but no compensation. These networks can be designed using the approach described in Appendix H, which is motivated by the design approach of [60].

In the conventional approach of Appendix H, the capacitive WPT system is designed for a given air-gap voltage. However, the air-gap voltage is not a design constraint in the proposed approach. To enable a fair comparison between the two approaches, the proposed approach is adapted to use the air-gap voltage as a design constraint, as detailed in Appendix I.

The matching network efficiencies predicted by the two approaches over a range of air-gap voltages can now be compared. This analytically-predicted efficiency comparison is shown in Fig. 3.16(a) for a 6.78-MHz 100-W capacitive WPT system with two-stage matching networks, input and output voltages of 60 V, a coupling capacitance of 10 pF (corresponding to 10 cm × 10 cm plates separated by a 1.2-cm air-gap), and an inductor quality factor of 200. As can be seen, the proposed approach achieves a higher efficiency over the entire range of air-gap voltages, with substantial loss reductions as shown in Fig. 3.16(b). For designs with a relatively strict electric field safety constraint, requiring lower air-gap voltages (below approximately 300 V in Fig. 3.16(a)), the efficiencies predicted by both approaches fall as the air-gap voltage is reduced. However, the fall in efficiency with the proposed approach is considerably less than that with the conventional approach. The much flatter efficiency profile of the proposed approach offers a better trade-off between efficiency and safety of a capacitive WPT system.

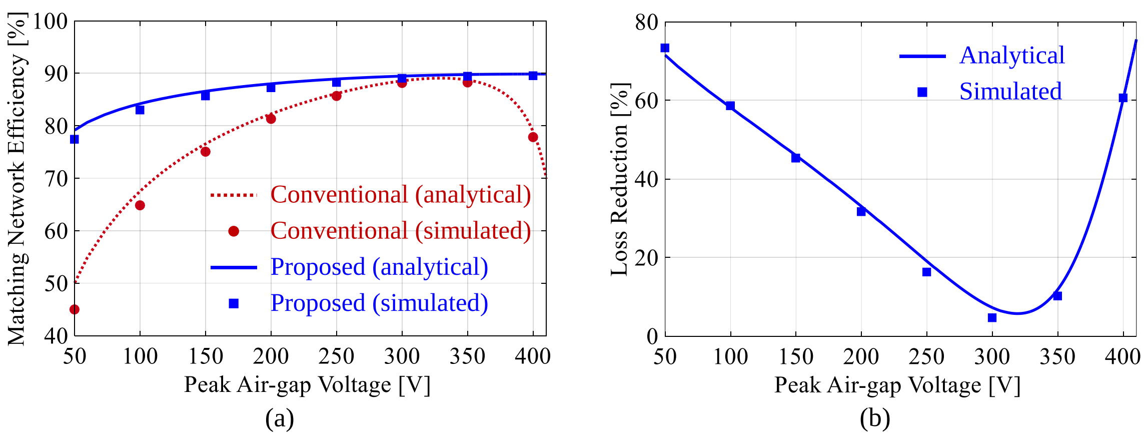


Fig. 3.16: Comparison of the proposed and the conventional design approaches over a range of air-gap voltages for a 100-W, 6.78-MHz capacitive WPT system with two-stage matching networks on each side of the coupling plates, a total current gain $G_{i,tot}$ of 1 and inductor quality factor of 200: (a) matching network efficiency resulting from the two approaches, and (b) loss reduction achieved by the proposed approach relative to the conventional approach. The continuous curves in (a) and (b) indicate analytically predicted results, and the markers indicate LTspice-simulated results.

For example, it can be seen from Fig. 3.16(a) that if an efficiency of 85% is desired, the conventional approach requires an air-gap voltage of 233.5 V, while the proposed approach only requires an air-gap voltage of 131.2 V, which is 43.8% lower. Similarly, if safety considerations restrict the air-gap voltage to 150 V, the conventional approach achieves an efficiency of 76.5%, while the proposed approach achieves an efficiency of 85.8%, corresponding to a loss reduction of nearly 46.2%. This analytical comparison is validated using a series of LTspice-based simulations, whose results are also shown in Fig. 3.16. As can be seen, the simulated results closely match the analytically predicted results.

The proposed approach also enables a better trade-off between efficiency and power transfer density. This is illustrated in Fig. 3.17(a) for a capacitive WPT system with the same input and output voltages and coupling capacitance as described above, and for three different air-gap voltages. The power transfer density in Fig. 3.17 is varied by changing the output power while maintaining the coupling plate dimensions at 10 cm × 10 cm. As can be seen from Fig. 3.17(a), for each air-gap voltage, the efficiencies of the matching networks designed using both approaches decrease as the power transfer density increases. This trade-off between efficiency and power transfer density is in line with the discussion in Section 3.2.2. However, Fig. 3.17(a) shows that as the power transfer density increases, the matching

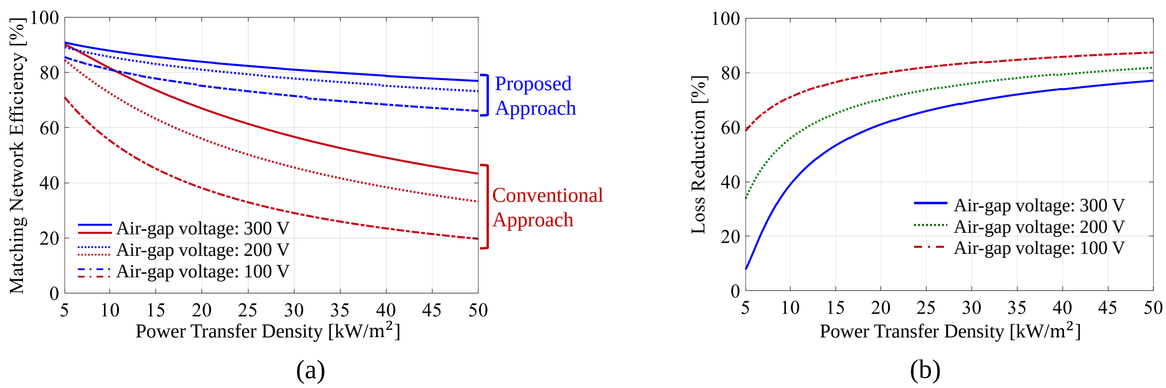


Fig. 3.17: Analytical comparison of the proposed and the conventional approaches to designing matching networks for a 6.78-MHz capacitive WPT system over a range of power transfer densities for three different air-gap voltages. The system comprise two-stage matching networks on each side of the coupling plates and the matching network inductors have an inductor quality factor of 200: (a) matching network efficiency, and (b) loss reduction.

network designed using the proposed approach is able to achieve a much higher and flatter efficiency than the matching network designed using the conventional approach. The corresponding loss reduction achieved by the proposed approach over the conventional approach is shown as a function of power transfer density in Fig. 3.17(b). As can be seen, the higher the power transfer density, the greater the loss reduction. For all air-gap voltages considered in Fig. 3.17(b), loss reductions exceeding 60% are achievable for power transfer densities higher than 20 kW/m^2. The comparison results shown in Figs. 3.16 and 3.17 together indicate that the proposed approach is more suitable for designing high-power-transfer-density capacitive WPT systems with relatively low air-gap voltages.

3.5. Experimental Validation

To validate the efficiency predictions of the proposed design approach, three prototype capacitive WPT systems are designed for the same specifications as those considered in the analysis of Sections III and V: an input and output voltage of 60 V, an output power of 100 W, a coupling capacitance of 10 pF (corresponding to 10 cm × 10 cm coupling plates separated by a 1.2 cm air-gap) and an operating frequency of 6.78 MHz. All three systems have full-bridge inverters and rectifiers, and are symmetric

TABLE 3.2. MATCHING NETWORK INDUCTANCE AND CAPACITANCE VALUES FOR THE THREE CAPACITIVE WPT SYSTEMS DESIGNED USING THE PROPOSED APPROACH

	Single-Stage System ($m = n = 1$)	Two-Stage System ($m = n = 2$)	Three-Stage System ($m = n = 3$)
$L_{pri,1}$	6.2 μH	1.7 μH	1.2 μH
$C_{pri,1}$	89.2 pF	373 pF	508.5 pF
$L_{pri,2}$	–	23 μH	4.64 μH
$C_{pri,2}$	–	16.5 pF	75.2 pF
$L_{pri,3}$	–	–	31.4 μH
$C_{pri,3}$	–	–	8 pF
$L_{sec,1}$	6.2 μH	23 μH	31.4 μH
$C_{sec,1}$	89.2 pF	16.5 pF	8 pF
$L_{sec,2}$	–	1.7 μH	4.64 μH
$C_{sec,2}$	–	373 pF	75.2 pF
$L_{sec,3}$	–	–	1.2 μH
$C_{sec,3}$	–	–	508.5 pF

around the coupling plates, that is, they have the same number of stages in their primary-side networks as in their secondary-side networks. The first system comprises single-stage networks, the second system comprises two-stage networks, and the third system comprises three-stage networks on both the primary and the secondary side. The values of the inductances and capacitances in the matching networks of these three systems are obtained using the approach described in Section III, and are listed in Table 3.2.

The above-designed three capacitive WPT systems are built and tested. The matching network inductance and capacitance values in the three prototype systems are very close to the values listed in Table 3.2. The inductors of the prototype systems are built as single-layer air-core solenoids, and are

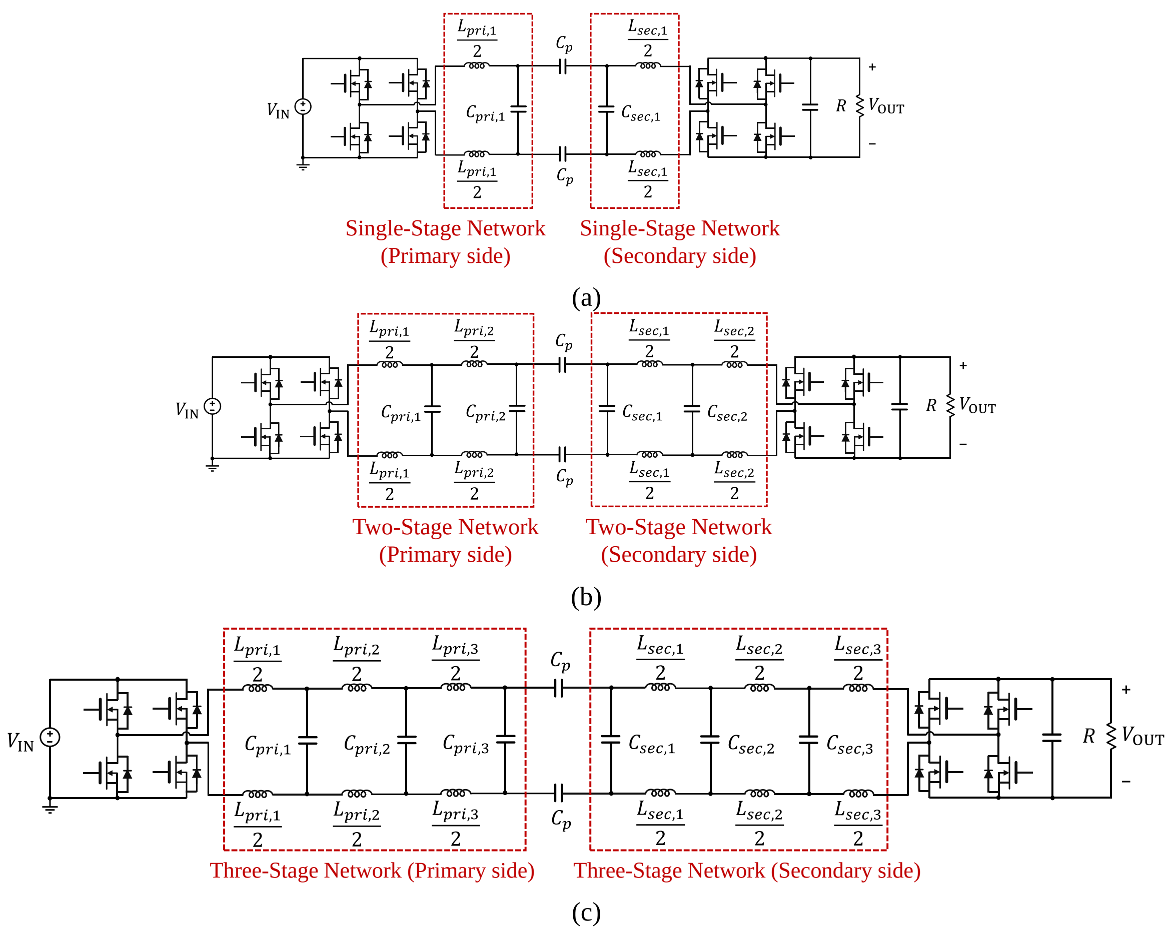


Fig. 3.18: Schematics of the 6.78-MHz 100-W capacitive WPT prototypes comprising a full-bridge inverter, a full-bridge rectifier, and (a) one, (b) two, and (c) three L-section stages on each side of the coupling plates.

split into two equal halves, with one half placed in the forward path and the other half in the return path, as shown in Fig. 3.18. The circuit symmetry imposed by this split-inductor design reduces parasitic ground currents that may otherwise impact power transfer and efficiency of the system, as mentioned in Chapter 2. The average value of the measured quality factor of the inductors is 251.5 for the single-stage system, 219.8 for the two-stage system, and 241.7 for the three- stage system. The matching network capacitors are implemented using NP0 ceramic capacitors. The capacitive coupler for these prototype systems is constructed using 10 cm × 10 cm copper plates separated by a 1.2-cm air-gap, resulting in a measured coupling capacitance of 10 pF. The inverter and rectifier are constructed using GaN Systems'

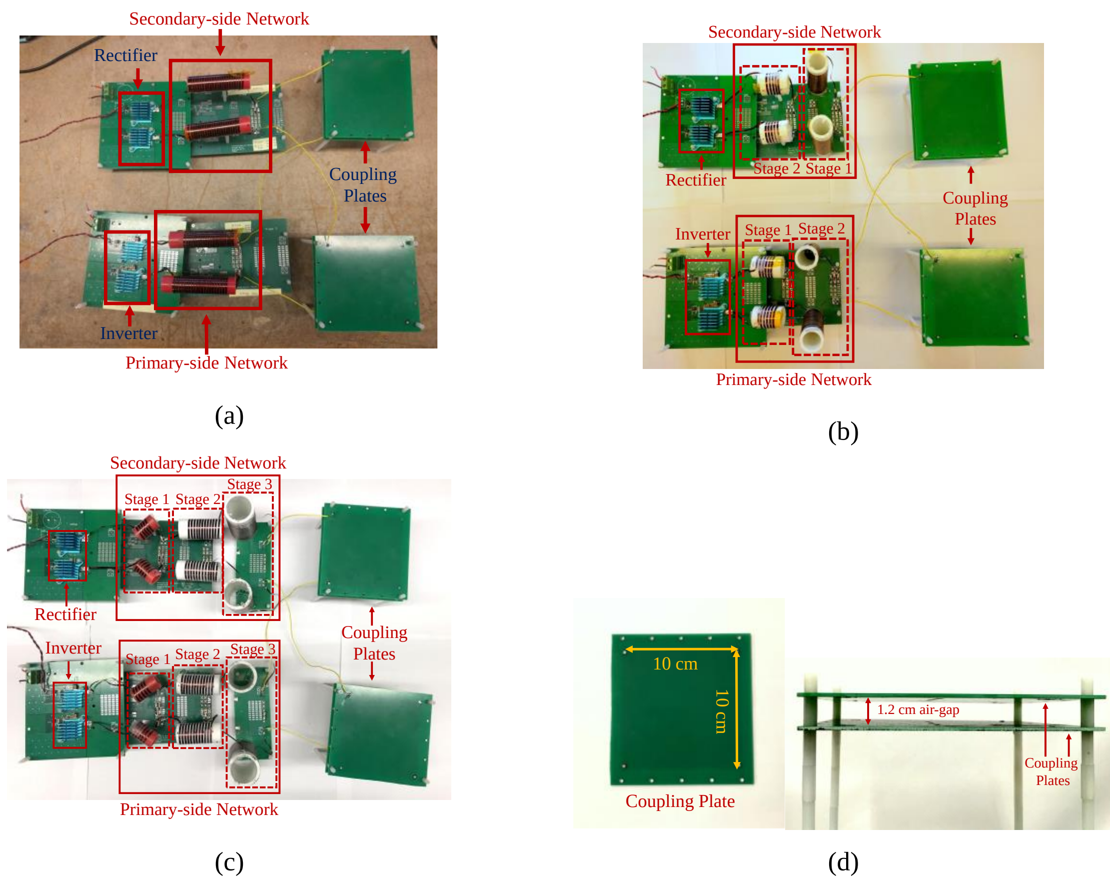


Fig. 3.19: Photographs of the 6.78-MHz 100-W prototype capacitive WPT systems designed using the proposed approach: (a) single-stage system, (b) two-stage system, (c) three-stage system, and (d) top and side views of the coupling plates.

GS66506T transistors. Photographs of the three prototype systems, along with the capacitive coupler, are shown in Fig. 3.19.

The measured inverter output voltages and output currents, and rectifier input voltages and input currents of the prototype systems are shown in Fig. 3.20. As can be seen, for all the three systems, the inverter and rectifier transistors achieve ZVS. The measured output power is 100.2 W for the single-stage system, 100.4 W for the two-stage system, and 102.1 W for three-stage system – all reasonably close to the designed output power of 100 W.

The matching network efficiencies of the prototype systems have also been measured. The matching network efficiency is first directly computed from the measured waveforms of the inverter output voltage and output current, and the rectifier input voltage and input current (shown in Fig. 3.20), by

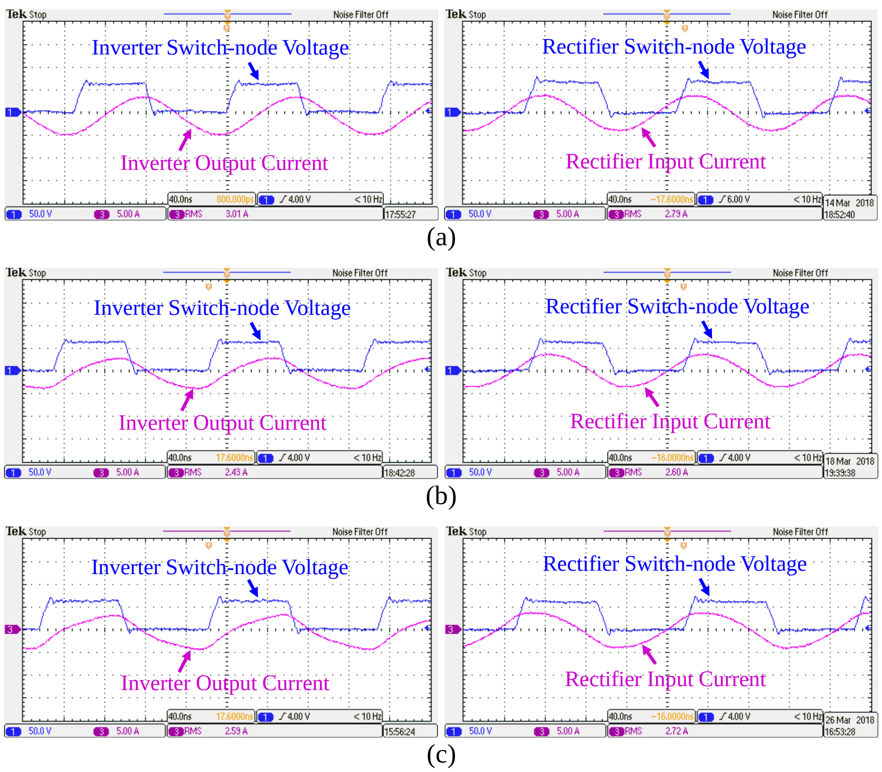


Fig. 3.20: Measured switching waveforms of the three 6.78-MHz 100-W prototype capacitive WPT systems designed using the proposed approach: (a) single-stage system, (b) two-stage system, and (c) three-stage system.

exporting these waveforms to MATLAB. The voltage and current waveforms are correctly aligned during measurement by accounting for the timing mismatch between the voltage and current probes, which is pre-determined using a wideband resistive load. To confirm the accuracy of these high-frequency ac measurements, the matching network efficiency of each of the three prototypes is also estimated from its dc-dc efficiency, measured using the dc input power of the inverter and the dc output power at the load. The conduction losses in the inverter and rectifier GaN transistors are then estimated using their datasheet on-resistance (with appropriate values for junction temperature), multiplied by a factor accounting for dynamic on-resistance [70]. Since the transistors achieve ZVS turn-on and low-current turn-off, conventional switching losses are neglected. However, additional switching losses resulting from hysteretic effects in the charging and discharging of the GaN-transistor output capacitances are considered [71]. The estimated conduction and switching losses are subtracted from the total measured losses to obtain an estimate of the matching network losses, and thus, the matching network efficiency. It is found that the matching network efficiencies from the high-frequency measurements and the dc measurements are within 0.5% of one another for all three prototype systems. The measured matching network efficiency from the dc measurements is 82.2% for the single-stage system, 89.4% for the two-stage system, and 90.7% for the three-stage system. This increasing trend in efficiency with higher number of stages is expected, as discussed earlier in Section 3.2.2. The measured

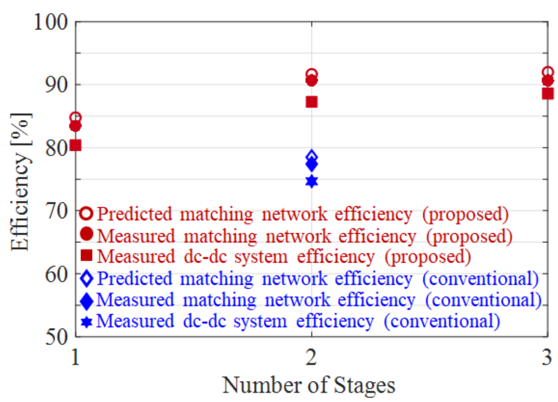


Fig. 3.21: Predicted and measured matching network efficiencies of the prototype systems implemented in this manuscript. Also shown are the measured dc-dc system efficiencies used to determine the measured matching network efficiencies.

dc-dc efficiencies, estimated matching network efficiencies, and analytically predicted matching network efficiencies of the three systems are shown in Fig. 3.21. As can be seen, there is an excellent match between the estimated and predicted matching network efficiency. Note that the predicted efficiencies are computed using (3.4), which neglects capacitor losses. This approximation holds because the capacitors used in the prototypes have more than ten times higher quality factor than the inductors. In designs where the capacitor losses are closer to the inductor losses, the predicted efficiency can instead be computed using the rms currents in the inductors and capacitors together with their quality factors.

The proposed approach to designing matching networks for capacitive WPT systems is also experimentally compared with the conventional approach. For this comparison, a prototype capacitive WPT system with two-stage matching networks on the primary and the secondary side is designed using the conventional approach, and built and tested. This system has the same input and output voltages, output power, coupling capacitance, and the same air-gap voltage as the two-stage system designed using the proposed approach, and also operates at the same frequency of 6.78 MHz. The matching network inductance and capacitance values, the peak energy stored in these inductors, and the designed

TABLE 3.3. MATCHING NETWORK INDUCTANCE AND CAPACITANCE VALUES AND AIR-GAP VOLTAGE OF THE TWO-STAGE CAPACITIVE WPT SYSTEMS DESIGNED USING THE CONVENTIONAL AND PROPOSED APPROACHES

	Conventional Design ($m = n = 2$)	Proposed design ($m = n = 2$)
$L_{pri,1}$	355 nH	1.7 μH
$C_{pri,1}$	1.55 nF	373 pF
$L_{pri,2}$	5.87 μH	23 μH
$C_{pri,2}$	95.3 pF	16.5 pF
$L_{sec,1}$	5.87 μH	23 μH
$C_{sec,1}$	95.3 pF	16.5 pF
$L_{sec,2}$	355 nH	1.7 μH
$C_{sec,2}$	1.55 nF	373 pF
$E_{L_{pri,1}}$	2.7 μJ	12.6 μJ
$E_{L_{pri,2}}$	74.6 μJ	9.5 μJ
$E_{L,sec,1}$	74.6 μJ	9.5 μJ
$E_{L,sec,2}$	2.7 μJ	12.6 μJ
$E_{L,tot}$	154.6 μJ	44.2 μJ
$V_{ag,pk}$	405 V	

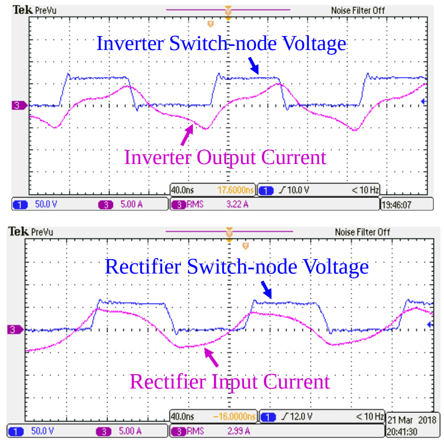


Fig. 3.22: Measured switching waveforms of the 6.78-MHz 100-W prototype capacitive WPT system with two-stage networks on both the primary and the secondary side, designed using the conventional approach.

air-gap voltage for both these systems are shown in Table 3.3. The average value of the measured quality factor of the inductors in the conventionally designed system is 239.6. As can be seen from Table 3.3, the inductors of the proposed design store less total energy ($E_{L,tot}$), and hence, for the same quality factor, are overall less lossy than those of the conventional design (since the inductor quality factor is proportional to the ratio of the stored energy and the loss in the inductor over an operating cycle). The measured waveforms of the inverter output voltage and output current, and the rectifier input voltage and input current of the conventionally designed system are shown in Fig. 3.22. The measured efficiency of this system is also shown in Fig. 3.21. As can be seen, the measured efficiency matches well with the prediction. Since the predicted efficiency is computed using fundamental-frequency analysis, its good match with measurement suggests that the higher-order harmonics visible in the current waveforms of Fig. 3.22 do not significantly impact efficiency. This also suggests that It can also be seen from Fig. 3.21 that the prototype with two-stage matching networks designed using the proposed approach achieves substantially higher efficiency than the conventionally designed prototype (89.4% for the proposed approach versus 76.2% for the conventional approach). This corresponds to a 62.1% reduction in losses, which is in good agreement with the predicted loss reduction of 64.9%.

3.6. Chapter Summary

This chapter introduces an analytical optimization approach to designing multistage L-section matching networks in capacitive WPT systems. The proposed approach maximizes the efficiency of the multistage matching network while ensuring the required overall gain and reactive compensation, by identifying the optimal number of matching network stages, and the optimal distribution of gains and compensations among these stages. A comprehensive design guideline is also provided to achieve a desirable trade-off between the number of stages and the efficiency of the matching network. The proposed approach is compared to the conventional approach to designing multistage matching networks in capacitive WPT systems, and the matching networks designed using the proposed approach are shown to achieve a higher and flatter efficiency across a wide range of air-gap voltages. The proposed approach also offers a better trade-off between efficiency and power transfer density, while maintaining low fringing electric field levels. The efficiency predictions of the proposed design approach are experimentally validated using three 6.78-MHz, 100-W prototype capacitive WPT systems comprising single-stage, two-stage and three-stage matching networks. The measured matching network efficiencies of all these prototypes closely match with the theoretical predictions. Furthermore, the matching networks of the prototype two-stage system designed using the proposed approach is shown to achieve significantly higher efficiency than its conventional counterpart.

CHAPTER 4

DYNAMIC CAPACITIVE WPT WITH ACTIVE VARIABLE REACTANCE (AVR) RECTIFIER

The design approach presented in the previous chapter ensures that the matching networks resonate with the capacitive coupler at the operating frequency of the WPT system and compensate for the coupler reactance. However, when the couplers are misaligned or the air-gap between them is changed (for example, while charging a moving vehicle, or charging vehicles with different ground clearances, respectively), the coupling reactance is altered. Consequently, the system falls out of resonance and the power transfer and efficiency drop drastically [72]. In WPT systems operating at low frequencies, where bandwidths are not restrictive (such as below 150 kHz), the traditional approach to dealing with variations in coupling is to change the operating frequency to track the resonant frequency of the system [73]. However, WPT systems operating above 150 kHz must comply with stringent FCC radio-frequency interference regulations unless they operate in one of the industrial, scientific and medical (ISM) bands (for example, 6.78 MHz, 13.56 MHz and 27.12 MHz), which have very restricted bandwidths [68]. One solution employed in low power (up to a few Watts) inductive WPT systems is to use a bank of capacitors that can be switched in and out of the compensating network, so as to keep the resonant frequency roughly unchanged in the event of coupling variations [74], [75]. However, in high power WPT systems, this approach requires many high-voltage and high-current switches, making it expensive. Furthermore, this approach is less suited to capacitive WPT systems, since it requires multiple switchable compensating inductors which are larger and more lossy than capacitors. Another adaptive impedance matching technique involves the use of variable inductors [76], but this reduces system efficiency and does not scale well with power. Other approaches include the use of auxiliary coils [77], multiple sequentially phased coils [78], or complicated coil geometries [79]. These approaches result in higher complexity in the coupler and the system. Furthermore, such approaches have only been explored for inductive WPT, and their applicability to capacitive WPT systems has not been demonstrated.

A recent approach to reducing the impact of coupling variations involves the use of resonant networks that transform the WPT system's load impedance in a manner such that when the coupling reactance changes, the impedance seen by the inverter changes by a relatively small amount [80]-[84]. These impedance compression approaches are suitable for high-frequency WPT systems because of their fixed-frequency nature. However, the coupling variation is only compressed and not fully compensated. As a result, the misalignment range over which flat power transfer can be maintained is relatively limited, and the circuit has remnant circulating currents, leading to over-sizing of components and sub-optimal efficiencies (especially at high power levels). Also reported in literature is the use of additional dc-dc converters that change the loading condition of a WPT system to partially recover power transfer and efficiency during coupling variations [85]-[87]. As in the impedance compression approaches, these dc-dc converter based approaches also do not fully compensate for the change in coupling reactance, and hence, have a limited misalignment range and relatively high circulating currents. Other approaches based purely on the control of power, such as [88]-[43], suffer from high complexity and are unable to maintain flat power transfer in the event of large coupling variations.

This chapter introduces a new approach to compensate for coupling variations in inductive and capacitive WPT systems using an active variable reactance (AVR) rectifier. The AVR rectifier provides a continuously variable reactance while operating at a fixed frequency and maintaining soft-switching. This enables it to seamlessly compensate for coupling variations while achieving high efficiency in high-frequency WPT systems. Furthermore, the proposed AVR rectifier maintains the output power of the WPT system at a fixed level even for large variations in coupling. A comprehensive design methodology is presented that maximizes the tolerable range of misalignments in AVR-rectifier-enabled capacitive WPT systems while achieving target efficiencies. A 13.56-MHz 12-cm air-gap prototype capacitive

WPT system incorporating the AVR rectifier, which can be scaled up in power for EV charging applications, is designed, built, and tested. This AVR-rectifier-enabled prototype maintains full power transfer for up to 45% lateral misalignment of the couplers and up to 45% increase in the vehicle's road clearance. In a dynamic EV charging scenario, the AVR-rectifier-enabled system transfers 80% more energy during a single pass of the vehicle over the charging pad, as compared to a system without the AVR rectifier. The measured performance of the prototype system is in good agreement with predictions.

4.1. Active Variable Reactance (AVR) Rectifier

The architecture of an AVR rectifier used in a capacitive WPT system is shown in Fig. 4.1. The AVR rectifier incorporates a resonant network that splits the power into two branches, one inductive and another capacitive. These branches comprise equal and opposite impedances ($+jX$ and $-jX$), and each of them is connected to a half-bridge rectifier. Although these two branches are similar to those present in a resistance compression network (RCN) [90], the AVR rectifier differs topologically and functionally from the RCN. Unlike in RCN, the outputs of its two half-bridge rectifiers are not connected in parallel. Instead, they are interfaced with the system output using two dc-dc converters. These dc-dc converters share a common output voltage V_{OUT}, and are designed to regulate their input voltages V_1 and V_2, as

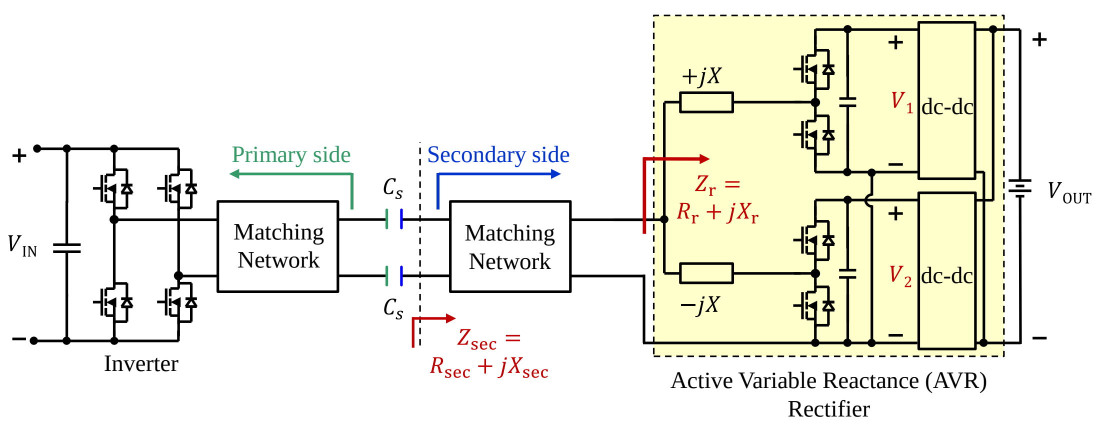


Figure 4.1: A capacitive wireless power transfer (WPT) system with an active variable reactance (AVR) rectifier that can provide continuously variable reactive compensation by controlling the rectifiers' output voltages V_1 and V_2.

shown in Fig. 4.1. To achieve zero-voltage and near-zero-current switching of the rectifier transistors and hence maintain high efficiencies, the impedances looking into the two rectifier switch-nodes must be near-resistive. Applying fundamental frequency analysis under this condition, the input impedance of the AVR rectifier, shown as Z_{r} in Fig. 4.1, is given by:

$$Z_{\mathrm{r}} = R_{\mathrm{r}} + jX_{\mathrm{r}} = \frac{k_{rec}^2 V_1^2 V_2^2 + P_1 P_2 X^2}{k_{rec}(P_1 V_2^2 + P_2 V_1^2)} + jX \frac{(P_1 V_2^2 - P_2 V_1^2)}{(P_1 V_2^2 + P_2 V_1^2)}. \tag{4.1}$$

Here, R_{r} and X_{r} are the real and imaginary parts of Z_{r}, X is the differential reactance of the AVR rectifier, P_1 and P_2 are the powers processed by the top and the bottom rectifiers, respectively, and k_{rec} is the gain associated with the rectifiers, and has a value of $\frac{2}{\pi^2}$ for each of the half-bridge rectifiers of Fig. 4.1. A derivation of (4.1) is provided in Appendix J.

When the coupling plates are fully aligned, and the air-gap is at its nominal value, the matching networks shown in Fig. 4.1 fully compensate for the coupler reactance. Under this condition, the dc-dc converters of the AVR rectifier operate in pass-through mode, and their input voltages V_1 and V_2 are both equal to the system output voltage V_{OUT}, i.e., $V_1 = V_2 = V_{\mathrm{OUT}}$. Therefore, the inductive and capacitive branches (having reactance $+X$ and $-X$, respectively) of the AVR rectifier each processes half of the output power P_{OUT}, i.e., $P_1 = P_2 = \frac{P_{\mathrm{OUT}}}{2}$, and the AVR rectifier does not provide any net reactance ($X_{\mathrm{r}} = 0$, as can be seen from (4.1)). When the plates are misaligned, or the air-gap becomes higher than nominal, the capacitive reactance of the coupler increases (say by $-\Delta X_{\mathrm{s}}$, where $\Delta X_{\mathrm{s}} = \frac{1}{2\pi f_{\mathrm{s}}\left(\frac{C_{\mathrm{s}}}{2}\right)} - \frac{1}{2\pi f_{\mathrm{s}}\left(\frac{C_{\mathrm{s},0}}{2}\right)}$), and $C_{\mathrm{s},0}$ is the nominal coupling capacitance of one plate pair), and the matching networks can no longer provide sufficient compensation. This leads to a substantial fall in power transfer and efficiency. To mitigate this, the voltages V_1 and V_2 of the AVR rectifier are made unequal by varying the duty ratios of the dc-dc converters. This results in an unequal distribution of power in the inductive and capacitive branches, enabling the AVR rectifier to provide a non-zero reactance ($X_{\mathrm{r}} \neq 0$), and compensate for the coupling variation. By appropriately controlling the voltages V_1 and V_2, this AVR rectifier's input reactance is brought to a value such that an inductive reactance $+\Delta X_{\mathrm{s}}$ is added to the secondary-side impedance Z_{sec} (see Fig. 4.1), and hence, the change in coupling reactance ($-\Delta X_{\mathrm{s}}$) is compensated. Furthermore, the chosen values of the two voltages of the AVR rectifier also ensure that the real part of Z_{sec} is kept the same as in the aligned/nominal-air-gap case, hence maintaining the same output power. The required value of the secondary-side impedance, Z_{sec}, to simultaneously achieve reactive compensation and fixed output power is therefore given by:

$$Z_{\mathrm{sec}} = R_{\mathrm{sec}} + jX_{\mathrm{sec}} = R_{\mathrm{sec,0}} + j(X_{\mathrm{sec,0}} + \Delta X_{\mathrm{s}}), \tag{4.2}$$

where $R_{\mathrm{sec,0}}$ and $X_{\mathrm{sec,0}}$ are the real and imaginary parts of Z_{sec} when the couplers are fully aligned with nominal air-gap. The corresponding required value of the AVR rectifier's input impedance, Z_{r}, depends on the design of the secondary-side matching network, and can be determined by transforming Z_{sec} through the secondary-side matching network. This required value of the AVR rectifier's input impedance ($Z_{\mathrm{r}} = R_{\mathrm{r}} + jX_{\mathrm{r}}$) can be achieved by maintaining the following values for its two rectifier output voltages V_1 and V_2:

$$V_1 = \sqrt{\frac{\frac{1}{2k_{\mathrm{rec}}} P_{\mathrm{OUT}} \left(R_{\mathrm{r}}(k+1) - \sqrt{R_{\mathrm{r}}^2 (k+1)^2 - 4kX^2}\right)\left(\left(R_{\mathrm{r}}(k+1) - \sqrt{R_{\mathrm{r}}^2 (k+1)^2 - 4kX^2}\right)^2 + 4X^2\right)}{\left(\left(R_{\mathrm{r}}(k+1) - \sqrt{R_{\mathrm{r}}^2 (k+1)^2 - 4kX^2}\right)^2 + 4kX^2\right)(1+k)}}, \tag{4.3}$$

and

$$V_2 = \sqrt{\frac{\frac{1}{2k_{\mathrm{rec}}} P_{\mathrm{OUT}} \left(R_{\mathrm{r}}(k+1) - \sqrt{R_{\mathrm{r}}^2 (k+1)^2 - 4kX^2}\right)\left(\left(R_{\mathrm{r}}(k+1) - \sqrt{R_{\mathrm{r}}^2 (k+1)^2 - 4kX^2}\right)^2 + 4k^2X^2\right)}{\left(\left(R_{\mathrm{r}}(k+1) - \sqrt{R_{\mathrm{r}}^2 (k+1)^2 - 4kX^2}\right)^2 + 4kX^2\right)(1+k)}}, \tag{4.4}$$

where $k = \frac{X+X_{\mathrm{r}}}{X-X_{\mathrm{r}}}$. A derivation of (5.3) and (5.4) is provided in Appendix J.

The operation and performance of the AVR rectifier is illustrated in Fig. 4.2 for a 13.56-MHz 12-cm air-gap capacitive WPT system. Figure 4.2(a) shows the output voltages of the two rectifiers V_1 and V_2 (normalized to the system output voltage V_{OUT}), and Fig. 4.2(b) shows the power processed by these two rectifiers P_1 and P_2, respectively (normalized to the nominal output power P_{OUT}), as a function of misalignment between the primary-side and secondary-side couplers. As the misalignment increases from zero, the AVR rectifier voltage V_1 is decreased while the AVR rectifier voltage V_2 is increased. As a result, the power processed by the top half-bridge rectifier (P_1) decreases, while the power processed by the bottom half-bridge rectifier (P_2) increases, keeping the total output power constant. The AVR-rectifier-enabled capacitive WPT system thus compensates for large coupling variations while maintaining full power transfer.

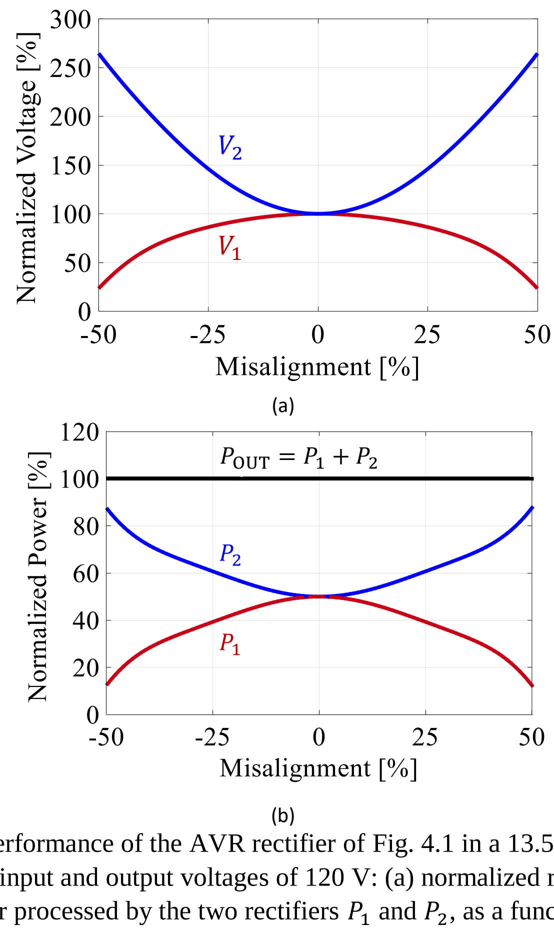


Figure 4.2: Operation and performance of the AVR rectifier of Fig. 4.1 in a 13.56-MHz 300-W 12-cm air-gap capacitive WPT system with input and output voltages of 120 V: (a) normalized rectifier output voltages V_1 and V_2, and (b) normalized power processed by the two rectifiers P_1 and P_2, as a function of coupler misalignment. Misalignment is normalized relative to the lateral dimension of the coupler.

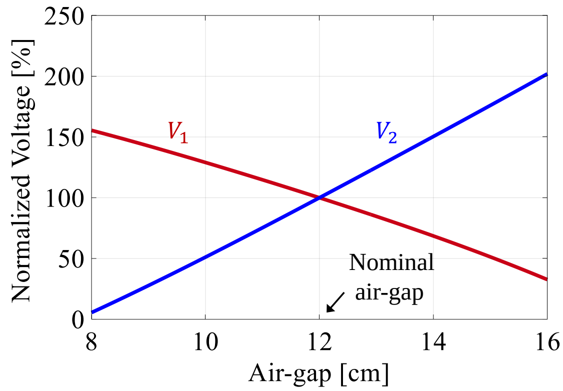


Figure 4.3: AVR rectifier voltages V_1 and V_2, normalized with respect to the system output voltage V_{OUT}, as a function of the air-gap between the roadway-side and the vehicle-side coupling pads in a 13.56-MHz 300-W 12-cm air-gap capacitive WPT system with input and output voltages of 120 V.

The AVR rectifier can also compensate for varying air-gaps. When the air-gap is larger than its nominal value, the AVR rectifier needs to provide inductive compensation. This is achieved by making the AVR rectifier voltage V_2 greater than the system output voltage V_{OUT}, and making the AVR rectifier voltage V_1 smaller than V_{OUT}, as shown in Fig. 4.3. When the air-gap is smaller than its nominal value, the AVR rectifier has to provide capacitive compensation. This is achieved by making V_2 smaller than V_{OUT}, and making V_1 larger than V_{OUT}.

It is also possible to incorporate a time-reverse dual of the AVR rectifier into the high-frequency inverter of the WPT system and utilize it to provide variable reactive compensation [91]. However, the AVR rectifier based WPT system more easily allows different types of vehicles to utilize the same roadway charging infrastructure since the additional system components are added only to the vehicle side. Furthermore, having the variable compensation system on the vehicle side allows its design to be optimized based on the specifics of the vehicle, including its road clearance and the dimensions of its receiving pad.

4.2. Design Methodology

The design methodology presented here for an AVR-rectifier-enabled capacitive WPT system aims to maximize the range of coupling variations over which full power can be transferred, while achieving an acceptable level of efficiency under nominal coupling conditions (i.e., for coupling associated with no misalignment and the nominal air-gap value). Under nominal coupling conditions, when the AVR rectifier is providing no net reactance and its dc-dc converters are in pass-through mode, the efficiency of the AVR-rectifier-enabled capacitive WPT system is dominated by the losses in its matching networks. Therefore, the proposed methodology focuses on the matching network losses, and co-optimizes the AVR rectifier and the matching networks to achieve its design objectives.

Figure 4.4 shows an AVR-rectifier-enabled capacitive WPT system with its matching networks implemented using L-sections, as is typically the case in large air-gap WPT applications, such as EV charging. Under nominal coupling conditions, these matching networks fully compensate for the coupling reactance, while providing an overall current gain G (defined as the ratio of the amplitudes of the AVR rectifier input current i_{avr} and the inverter output current i_{inv}, as shown in Fig. 4.4). The output power of this AVR-rectifier-enabled capacitive WPT system under nominal coupling conditions can be expressed in terms of the matching network's overall current gain G and the AVR rectifier's differential reactance, X, as:

$$P_{\text{OUT}} = \frac{V_{\text{OUT}}}{X}\sqrt{\frac{2k_{\text{inv}}^2 k_{\text{rec}} V_{\text{IN}}^2}{G^2} - 4k_{\text{rec}}^2 V_{\text{OUT}}^2}, \tag{4.5}$$

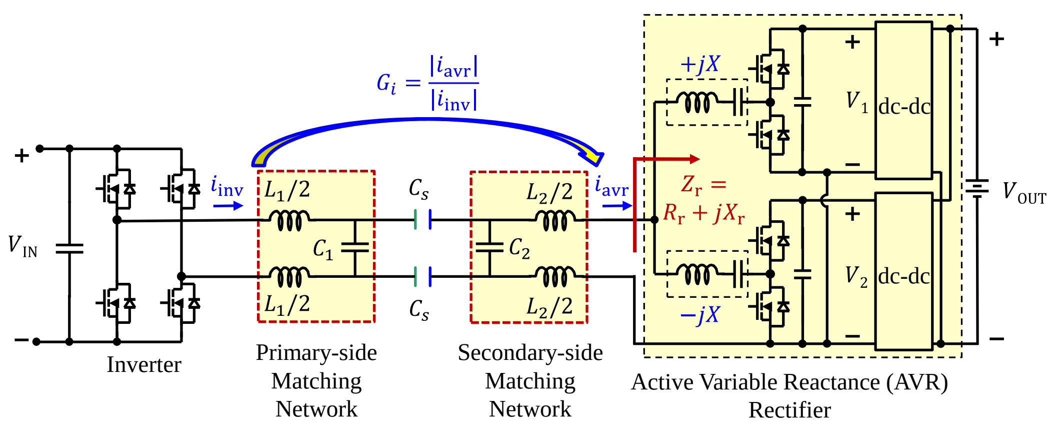


Figure 4.4: An AVR-rectifier-enabled capacitive WPT system with L-section matching networks designed to compensate for the nominal coupling reactance $X_s \left(= \frac{1}{2\pi f_s (C_s/2)}\right)$ and provide an overall current gain $G \left(= \frac{|i_{\text{avr}}|}{|i_{\text{inv}}|}\right)$.

where V_{IN} is the input voltage of the inverter, and k_{inv} is the voltage gain associated with the inverter and equal to $\frac{4}{\pi}$ for the full-bridge inverter of Fig. 4.4. A derivation of (4.5) is provided in Appendix K. As can be seen from (4.5), for given values of input and output voltages and given inverter and rectifier topologies, the desired value of output power under nominal coupling conditions can be achieved by choosing different combinations of the current gain, G, and the reactance, X, as long as G satisfies:

$$G < \frac{1}{\sqrt{2}} \frac{k_{\mathrm{inv}}}{\sqrt{k_{\mathrm{rec}}}} \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}} \equiv G_{\mathrm{max},1}. \tag{4.6}$$

This upper limit on the value of current gain G (derived from (4.5) in Appendix K) ensures a real value for output power. Hence, the capacitive WPT system could potentially be designed by arbitrarily selecting G (in the range $0 < G < G_{\mathrm{max},1}$) and determining X so as to satisfy (4.5). However, different choices for the current gain G enable different ranges of coupling variations that can be fully compensated by the AVR rectifier, and also result in different matching network efficiencies. The goal here is to determine the value of the current gain G that maximizes the range of fully compensable coupling variation, while achieving a desired level of matching network efficiency.

The overall efficiency of the primary and secondary side matching networks of the capacitive WPT system shown in Fig. 4.4 can be expressed in terms of the current gain G as:

$$\eta = 1 - \frac{2\sqrt{\frac{2X_S P_{\mathrm{OUT}}}{k_{\mathrm{inv}}^2 V_{\mathrm{IN}}^2} G - 1}}{Q_{\mathrm{L}}}. \tag{4.7}$$

Here, Q_{L} is the quality factor of the matching network inductors. The expression for the matching network efficiency given in (4.7) can be derived using the methodology outlined in Chapter 3. As can be seen from (4.7), and illustrated in Fig. 4.5, the matching network efficiency falls as the current gain G increases. Therefore, to achieve efficiency above a minimum desired efficiency η_{des}, the matching networks must be designed to have a current gain G limited by:

$$G < \frac{k_{\mathrm{inv}}^2 V_{\mathrm{IN}}^2}{2X_{\mathrm{s}} P_{\mathrm{OUT}}}\left(1 + \frac{Q_{\mathrm{L}}^2}{4}(1-\eta_{\mathrm{des}})^2\right) \equiv G_{\mathrm{max,2}}. \tag{4.8}$$

Hence, the upper bound on the matching network current gain G is determined by the lower of the two limits given by (4.6) and (4.8); and the valid range of G is:

$$0 < G < \min(G_{\mathrm{max,1}}, G_{\mathrm{max,2}}). \tag{4.9}$$

To determine the optimal value of G within this range, the corresponding value of the AVR rectifier's differential reactance X can be calculated using (4.5) and used to determine the range of coupling variations which can be fully compensated. The range of coupling variations that can be fully compensated by the AVR rectifier are determined by the limiting values of its input impedance, and the impedance transformation provided by the secondary side matching network. The limiting values of input impedance depend on the value of the AVR rectifier's differential reactance X. First, the reactance provided by the AVR rectifier X_{r} cannot exceed X:

$$|X_{\mathrm{r}}| \leq X. \tag{4.10}$$

This reactance limit can be understood by considering the limiting cases in terms of the half-bridge rectifier output voltages V_1 and V_2 of the AVR rectifier. The expression for the input reactance of the AVR rectifier, X_{r}, as given by (4.1), can be rearranged as:

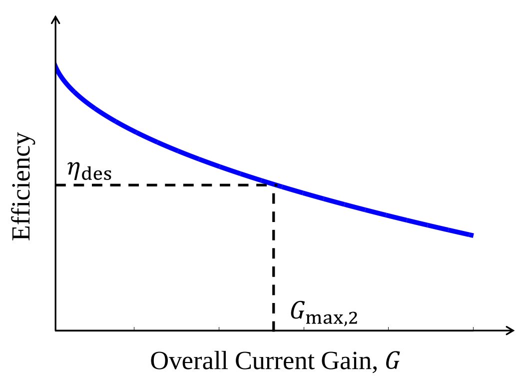


Figure 4.5: Matching network efficiency as a function of its overall current gain G in a capacitive WPT system.

$$X_{\mathrm{r}} = X \frac{\left(\frac{V_2^2}{P_2} - \frac{V_1^2}{P_1}\right)}{\left(\frac{V_2^2}{P_2} + \frac{V_1^2}{P_1}\right)}. \tag{4.11}$$

It can be observed from the form of (4.11) that X_{r} is maximum when the voltage V_1 is equal to zero, and is minimum when the voltage V_2 is equal to zero. When the voltage $V_1 = 0$, the switch-node of the top half-bridge rectifier is effectively shorted to ground. The corresponding input reactance of the AVR rectifier is given, according to (4.11), by: $X_{\mathrm{r}} = X$. Similarly, when the voltage $V_2 = 0$, i.e., the switch-node of the bottom half-bridge rectifier is shorted to ground, the reactance X_{r} is equal to $-X$. By controlling the voltages V_1 and V_2 to have non-zero positive values, the AVR rectifier can provide any amount of reactance between the $\pm X$ limits.

The second input impedance related limit is associated with the magnitude of the AVR input impedance Z_{r} ($\equiv \sqrt{R_{\mathrm{r}}^2 + X_{\mathrm{r}}^2}$), which has a minimum value of X:

$$|Z_{\mathrm{r}}| \geq X. \tag{4.12}$$

This impedance limit can be understood by considering the expression for Z_{r} given by (4.1). Using (4.1), the magnitude of the AVR rectifier's input impedance can be expressed and simplified as:

$$|Z_{\mathrm{r}}|^2 = \left(\frac{k_{\mathrm{rec}}^2 V_1^2 V_2^2 + P_1 P_2 X^2}{k_{\mathrm{rec}}(P_1 V_2^2 + P_2 V_1^2)}\right)^2 + X^2 \frac{(P_1 V_2^2 - P_2 V_1^2)}{(P_1 V_2^2 + P_2 V_1^2)^2}^2$$

$$= X^2 + \left(\frac{k_{\mathrm{rec}} V_1^2 V_2^2 - P_1 P_2 X^2}{k_{\mathrm{rec}}\left(P_1 V_2^2 + P_2 V_1^2\right)}\right)^2. \tag{4.13}$$

Since $\left(\frac{k_{\mathrm{rec}} V_1^2 V_2^2 - P_1 P_2 X^2}{k_{\mathrm{rec}}\left(P_1 V_2^2 + P_2 V_1^2\right)}\right)^2 \geq 0$, the value of $|Z_{\mathrm{r}}|^2$ must be greater than X^2, i.e., the value of $|Z_{\mathrm{r}}|$ must be greater than or equal to X.

Hence, the overall design procedure for the AVR-rectifier-enabled capacitive WPT system of Fig. 4.4 is as follows. The input and output voltages V_{IN} and V_{OUT}, output power P_{OUT}, operating frequency

f_{s}, and the topology of the inverter and the rectifier (which determine the values of k_{inv} and k_{rec}) are assumed to be given. The value of the overall matching network current gain G is swept in small steps from zero to its maximum value imposed by (4.9). For each value of current gain G, the matching networks are optimally designed, i.e., the optimal values of the inductances L_1, L_2 and capacitances C_1, C_2 are determined so as to maximize the overall matching network efficiency, using the guidelines provided in Appendix C. The value of the AVR rectifier's differential reactance is also determined for each value of current gain G using:

$$X = \frac{V_{\mathrm{OUT}}}{P_{\mathrm{OUT}}}\sqrt{\frac{2k_{\mathrm{inv}}^2 k_{\mathrm{rec}} V_{\mathrm{IN}}^2}{G^2} - 4k_{\mathrm{rec}}^2 V_{\mathrm{OUT}}^2}, \tag{4.14}$$

which is derived from (4.5). Next, for each value of current gain G, the magnitude of the change in coupling reactance (ΔX_{s}) that needs to be compensated is increased from zero in small steps. For each value of ΔX_{s}, the input impedance of the AVR rectifier, Z_{r} ($= R_{\mathrm{r}} + jX_{\mathrm{r}}$), required to fully compensate for the change in coupling reactance and maintain constant output power, is obtained by numerically solving the two equations formed by equating the real and imaginary parts of:

$$\left((R_{\mathrm{r}} + jX_{\mathrm{r}}) + j\omega_{\mathrm{s}} L_2\right) \,||\, \left(-\frac{j}{\omega_{\mathrm{s}} C_2}\right) = \left(\frac{4k_{rec}^2 V_{\mathrm{OUT}}^4 + P_{\mathrm{OUT}}^2 X^2}{4k_{rec} V_{\mathrm{OUT}}^2 P_{\mathrm{OUT}}} + j\omega_{\mathrm{s}} L_2\right) \,||\, \left(-\frac{j}{\omega_{\mathrm{s}} C_2}\right) + j\Delta X_{\mathrm{s}}, \tag{4.15}$$

A derivation of (4.15), which is a restatement of (4.2) utilizing Z_{r} transformed through the secondary-side matching network, is provided in Appendix L. If the AVR rectifier's input impedance Z_{r} ($= R_{\mathrm{r}} + jX_{\mathrm{r}}$) satisfies the conditions given by (4.10) and (4.12), the corresponding change in coupling reactance ΔX_{s} can be fully compensated, and larger values of ΔX_{s} are considered until the corresponding required value of Z_{r} violates one of the two conditions. The largest change in coupling reactance that does not result in violation of (4.10) and (4.12) is obtained for all the considered values of current gain G. The value of current gain that results in the highest value for fully compensable change in coupling reactance is selected for the design. This design procedure is presented in the form of a flowchart in Fig. 4.6.

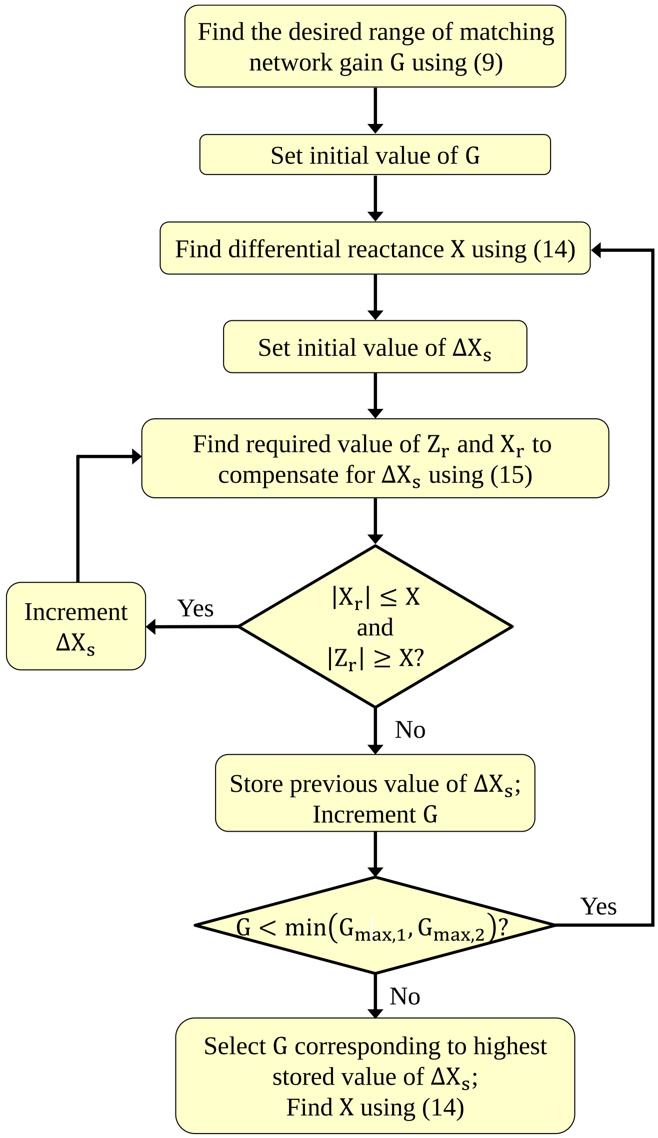


Figure 4.6: Design methodology for the AVR-rectifier-based capacitive WPT system of Fig. 4.1.

4.3. Design Example

To illustrate the design methodology described above, it is utilized to design a 13.56-MHz 12-cm air-gap AVR-rectifier-enabled capacitive WPT system having the same topology as Fig. 4.4, with input and output voltages of 120 V and an output power of 300 W. The matching network efficiency in this system is targeted to be at least 90% under nominal coupling conditions, i.e., $\eta_{\text{des}} = 90\%$. Designing such a system means selecting appropriate values for the matching network overall current gain G and the AVR rectifier's differential reactance X. Following the procedure described in Section 4.2, first the upper limit on the current gain G is determined. One upper limit that ensures real values of output power, $G_{\max,1}$, is equal to 2 according to (4.6). The other upper limit that ensures at least 90% matching network efficiency, $G_{\max,2}$, is equal to 0.57 according to (4.8) (for an inductor quality factor of 150). The value of $G_{\max,2}$ can also be determined graphically from Fig. 4.7. The upper limit on current gain G is the lower of the two limits $G_{\max,1}$ and $G_{\max,2}$, according to (4.9). Hence, the maximum selectable value of the current gain G is below 0.57.

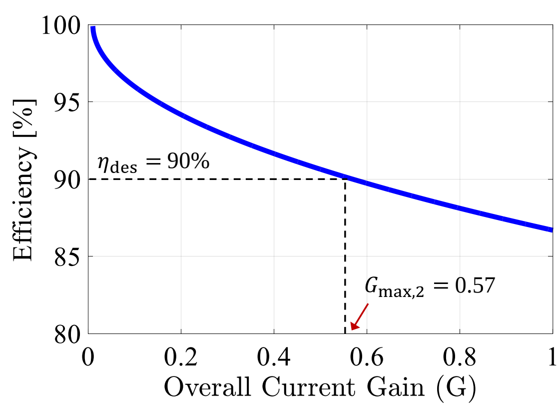


Figure 4.7: Matching network efficiency as a function of the overall current gain G provided by the matching networks in the example 13.56-MHz 12-cm air-gap capacitive WPT system. The operable range of the overall current gain of the matching network is set to be G <0.57 in order to ensure at least 90% matching network efficiency.

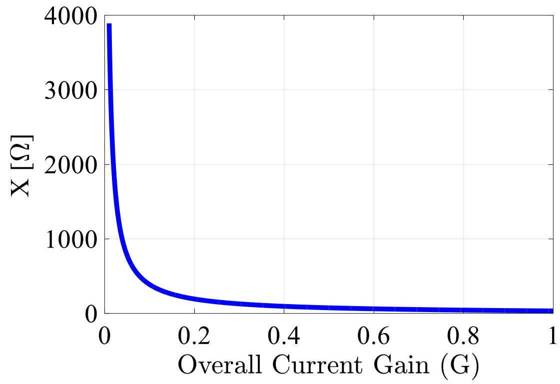


Figure 4.8: AVR rectifier's differential reactance, X, as a function of the overall current gain G provided by the matching networks in the example 13.56-MHz 12-cm air-gap capacitive WPT system.

Next, the matching network current gain is swept within the range $0 < G < 0.57$ in small steps. For each value of the current gain G, the values for the inductances L_1, L_2 and the capacitances C_1, C_2 of the matching networks are obtained using the procedure given in Appendix C, and the value of the AVR rectifier's differential reactance X is obtained using (4.14). The value of the reactance X for this example capacitive WPT system is shown as a function of the matching network current gain G in Fig. 4.8. Next, for each value of current gain G, the magnitude of the change in coupling reactance ΔX_s is increased from zero in small steps. This change in coupling reactance may correspond to different coupler misalignments or different values of air-gap. Figure 4.9 shows the coupling capacitance in this capacitive WPT system as a function of misalignment between the primary-side and secondary-side coupling plates. For different values of misalignments, the values of coupling capacitances are obtained using

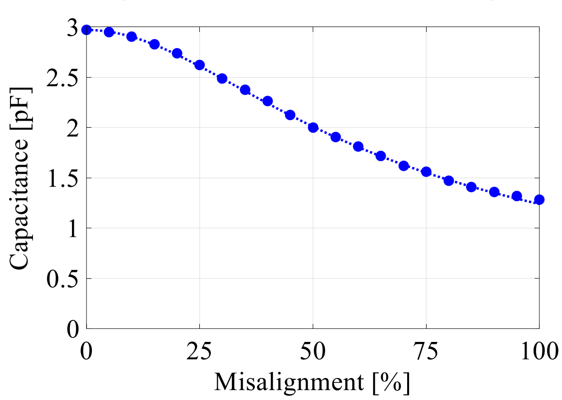


Figure 4.9: Coupling capacitance of the 22-cm diameter 12-cm air-gap capacitive WPT system as a function of misalignment between the couplers. Coupling capacitance values are obtained using Ansys HFSS electromagnetic field simulator.

Ansys HFSS electromagnetic field simulator, and the magnitude of the change in coupling reactance (ΔX_{s}) relative to its nominal value is calculated. For each value of ΔX_{s}, the value of the AVR rectifier's input impedance Z_{r} ($= R_{\mathrm{r}} + jX_{\mathrm{r}}$) required to provide reactive compensation and maintain constant output power is obtained using (4.15).

The magnitudes of the required AVR rectifier input reactance, X_{r}, and the required AVR rectifier input impedance, Z_{r}, normalized with respect to the AVR rectifier's differential reactance X, are shown in Fig. 4.10 as a function of misalignment between the couplers for different values of matching network gain G. The regions shaded in light yellow in Figs. 4.10(a) and 4.10(b) indicate the domains where the conditions (4.10) and (4.12) are satisfied, and hence, fully compensating the change in coupler reactance using the AVR rectifier is feasible. As can be seen from Fig. 4.10(b), the required value of the AVR

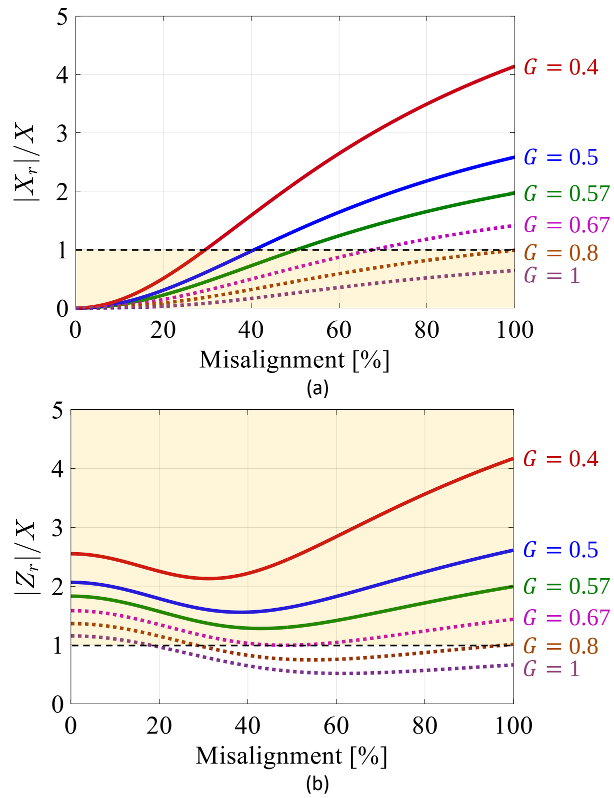


Figure 4.10: Magnitudes of the required AVR rectifier input reactance X_{r}, and the required AVR rectifier input impedance Z_{r}, both normalized with respect to the AVR rectifier's differential reactance X, as a function of the misalignment between the coupling plates for a 13.56-MHz 12 cm air-gap capacitive WPT system with an input and output voltage of 120 V and an output power of 300 W, for different values of the matching network gain G.

rectifier input impedance Z_{r} stays within its feasible range for all values of matching network current gain within $0 < G < 0.57$ across all values of misalignment between 0% and 100%. However, the value of the AVR rectifier input reactance X_{r} stays within its feasible range for a wider range of misalignments when the matching network current gain G is higher, as is evident from Fig. 4.10(a). Therefore, within the valid range for matching network current gain, a value of G just below 0.57 maximizes the range of coupling variations over which full reactive compensation can be provided and full power transfer can be maintained. This value of G enables full compensation for up to 50% misalignment of the couplers, as can be seen from Fig. 4.10(a). Hence, a matching network current gain G of value just below 0.57 is selected for the design. The corresponding values of the matching network inductances and capacitances, obtained using the procedure outlined in Appendix C, and the AVR rectifier's differential reactance X, obtained using (4.14), are listed in Table 4.1.

It is also instructive to note from Fig. 4.10(b) that for all values of matching network current gain G up to 0.67, the magnitude of the AVR rectifier input impedance Z_{r} always stays within its feasible range. Current gains greater than the selected value (just below 0.57) and up to 0.67 enable full compensation for more than 50% misalignment, as can be seen from Fig. 4.10(a). However, given the assumed quality factor of available inductors ($Q_{\mathrm{L}} = 200$), matching networks that provide such high current gains will not be able to meet the targeted matching network efficiency of 90%; hence, these designs are not considered. For matching network current gains above 0.67, the magnitude of Z_{r} falls below its feasible range for relatively smaller values of misalignment (see Fig. 4.10(b)); for example, a current gain G of 0.8 results in a design that can fully compensate for misalignments of only up to 28%. Thus, selecting

TABLE 4.1: DESIGNED VALUES OF THE MATCHING NETWORK INDUCTANCES AND CAPACITANCES AND THE AVR RECTIFIER'S DIFFERENTIAL REACTANCE IN THE EXAMPLE 13.56-MHZ 300-W CAPACITIVE WPT SYSTEM

L_1	C_1	L_2	C_2	X
4.9 μH	26.5 pF	15.0 μH	7.6 pF	65.4 Ω

the matching network current gain to be just under 0.57 maximizes the range of misalignment that can be fully compensated by the AVR-rectifier-enabled capacitive WPT system of Fig. 4.4, while achieving a matching network efficiency above 90%.

Figure 4.11 shows the performance of such an AVR-rectifier-enabled capacitive WPT system designed to compensate for up to $\pm$50% misalignment of the couplers in a dynamic EV charging scenario. As the vehicle passes over the charging pad, the system without the AVR rectifier transfers high power only for a small range of misalignment, while the system with the AVR rectifier transfers full power for up to $\pm$ 50% misalignment, with 78.5% more total energy transfer over a vehicle pass (comparing areas under curves in Fig. 4.11). The proposed design methodology enables such enhanced energy transfer, and hence, requires fewer charging pads to be installed in a dynamic EV charging scenario. On the other hand, in order to maintain the same average power, the system without the AVR rectifier will need to process a higher peak power, potentially increasing the cost of power electronic components. A systematic analysis of the benefits of incorporating the AVR rectifier in a capacitive WPT system is presented in Appendix M.

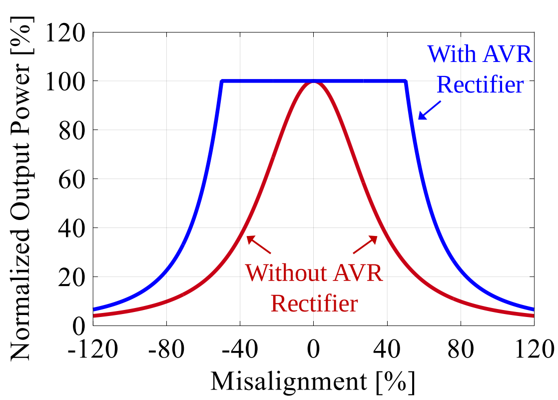


Figure 4.11: Comparison of the power transferred by the capacitive WPT system with and without the AVR rectifier in a dynamic EV charging scenario.

4.4. Experimental Validation

A prototype AVR-rectifier-enabled capacitive WPT system, having the topology shown in Fig. 4.4, and designed using the proposed methodology to compensate for up to ±50% coupler misalignment, is built and tested. This prototype system operates at 13.56 MHz, with dc input and output voltages of 120 V, and delivers up to 300 W through a 12-cm nominal air-gap using 22-cm diameter coupling plates, and can be scaled up in power for dynamic EV charging applications. The operating frequency of 13.56 MHz was chosen because it enables higher power transfer and higher efficiency than 6.78 MHz, due to a 4x reduction in the required matching network inductance (in general, for a given coupling capacitance, the matching network inductance value is proportional to $1/f^2$). A schematic of the prototype system, including the topologies of the dc-dc converters used in the AVR rectifier, is shown in Fig. 4.12. The experimental setup, shown in Fig. 4.13(a), allows variable misalignment between the roadway-side and the vehicle-side coupling plates, as well as a variable air-gap to emulate charging scenarios with different vehicle road clearances. Here, the roadway and vehicle chassis are modeled by 1-m × 1-m aluminum sheets. The matching network inductors and the inductor in the $+jX$ branch of the AVR rectifier are realized using single-layer air-core solenoids. The matching network capacitors are realized by the parasitic capacitance that exists between the coupling plates and the roadway or the

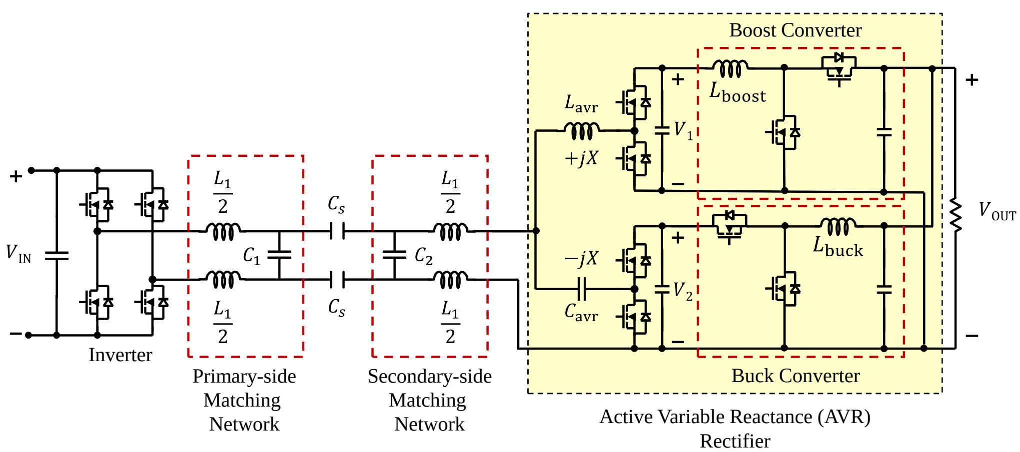


Figure 4.12: Schematic of the prototyped AVR-rectifier-enabled capacitive WPT system, including the topologies of the dc-dc converters utilized as part of the AVR rectifier.

vehicle chassis. The desired values of these capacitances are achieved by appropriately spacing the coupling plates from the roadway and the vehicle chassis. This eliminates the need for discrete high-voltage capacitors in the matching networks, increasing the efficiency and reliability of the system. A photograph of the prototype AVR rectifier is shown in Fig. 4.13(b). It can be noted that since one of the rectifier output voltages (V_2) must increase and the other (V_1) must decrease with misalignment (see Fig. 4.2), the top dc-dc converter is implemented as a boost converter, and the bottom one as a buck converter. Both the dc-dc converters operate at 100 kHz. The full-bridge inverter, the half-bridge rectifiers, and the dc-dc converters all utilize GaN Systems GS66506T 650-V 22-A enhancement-mode GaN transistors. The inductors of the dc-dc converters are designed so as to maintain the current ripple within 20% for the full range of dc-dc conversion ratios required to compensate for up to $\pm$50% coupler misalignment. These inductors are built using 1000-strand Litz wire wound on RM-14 cores. Additional details regarding the components used in this prototype are listed in Table 4.2.

When the roadway-side and the vehicle-side coupling plates are fully aligned and vertically separated by the nominal air-gap of 12 cm, both dc-dc converters of the AVR rectifier operate in pass-through mode, and hence, their input voltages (V_1 and V_2) are equal to the system output voltage of 120 V. Under this condition, the prototype system transfers output power of 300 W with a dc-to-dc efficiency of 84.1%. The corresponding measured switch-node voltages and input currents of the two half-bridge

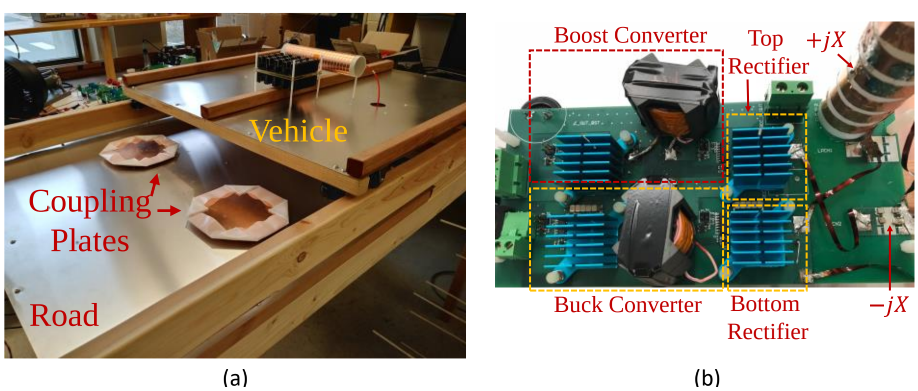
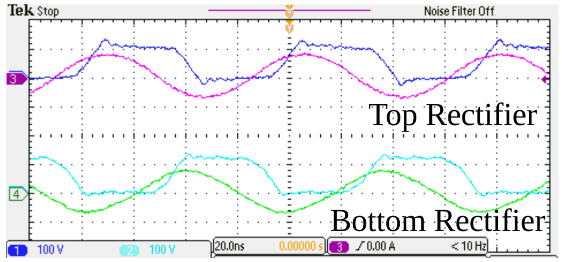


Figure 4.13: Photographs of the 13.56-MHz 300-W prototype AVR-rectifier-enabled capacitive WPT system: (a) test setup for dynamic capacitive wireless EV charging, (b) AVR rectifier used in this system.

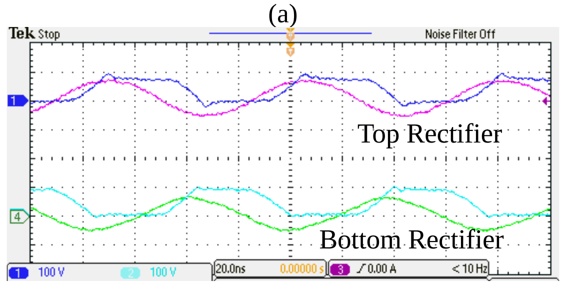
TABLE 4.2: COMPONENTS USED IN THE ACTIVE VARIABLE REACTANCE (AVR) RECTIFIER PROTOTYPE

Component	Value	Description
Inverter, Rectifier, and dc-dc Converter Transistors	-	GS66506T 650-V/22-A eGaN FETs
C_s	3 pF	22-cm diameter plates, 12-cm air-gap
L_1	5.0 μH	Air-core single-layer solenoid
C_1	25.9 pF	Realized by placing the roadway-side plates 10 mm above the roadway
L_2	15.1 μH	Air-core single-layer solenoid
C_2	7.8 pF	Realized by placing the vehicle-side plates 32 mm below the vehicle chassis
L_{avr}	790 nH	Air-core single-layer solenoid
C_{avr}	182 pF	1.5 kV NP0 ceramic capacitor
L_{boost}	133 μH	1000-strand Litz wire, RM-14 core
L_{buck}	112 μH	1000-strand Litz wire, RM-14 core

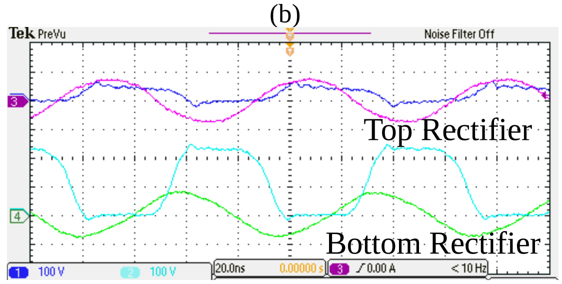
rectifiers are shown in Fig. 4.14(a). The smooth transitions of the switch-node voltages indicate that the rectifier transistors achieve zero-voltage switching (ZVS). When the coupling plates are misaligned, with the vertical separation maintained at 12 cm and the voltages V_1 and V_2 still kept equal (i.e., the AVR rectifier kept inactive), the output power falls rapidly. For example, at 45% misalignment between the coupling plates, the output power falls to 30% of the full output power. The measured rectifier waveforms at 45% misalignment are shown in Fig. 4.14(b). It can be noted that since the EV battery is modeled by a resistor in this prototype, the fall in output power translates to a drop in the load voltage.



(a)



(b)



(c)

Figure 4.14: Measured switch-node voltages and input currents of the half-bridge rectifiers in the 13.56-MHz 12-cm air-gap AVR-rectifier-enabled capacitive WPT prototype when: (a) the coupling pads are fully aligned, (b) the coupling pads are misaligned by 45% with no AVR operation, and (c) the pads are misaligned by 45% and the AVR rectifier is operated to restore the output power to its nominal value.

To maintain full output power, the duty ratios of the buck and boost converters of the AVR rectifier are varied such that V_1 decreases and V_2 increases in accordance with (4.3) and (4.4). As a result, the output power of the prototype system is maintained at its nominal value of 300 W for up to 45% misalignment between the couplers, approaching the 50% misalignment design target. At 45% misalignment, the output voltage of the top rectifier, V_1, is 54 V, and that of the bottom rectifier, V_2, is 234 V. The corresponding rectifier and dc-dc converter waveforms are shown in Fig. 4.4.14(c) and Fig. 4.15, respectively. As can be seen from Fig. 4.14(c), the rectifier transistors continue to achieve ZVS. In this experiment, the voltages V_1 and V_2 are regulated manually for each value of misalignment. However, these voltages can be automatically controlled using a feedback control architecture that does

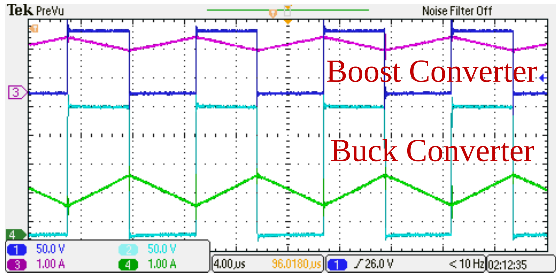


Figure 4.15: Measured switch-node voltages and inductor currents of the buck and the boost converters of the AVR rectifier when the output power is restored to its nominal value at 45% misalignment between the coupling pads.

not need communication between the primary and secondary sides. Such a control architecture, using two feedback loops to ensure reactive compensation and constant output power, is presented in the next chapter.

The measured and predicted output power, with and without AVR rectifier operation, are shown in Fig. 4.16 as a function of misalignment between the couplers. The output power is predicted for each value of misalignment using the corresponding value of coupling capacitance as obtained from Fig. 4.9. As can be seen, the measured power profile, with and without AVR rectifier, matches the theoretical predictions except for large values of misalignments (above 50%). The reason for the mismatch is that at larger misalignments, losses in the matching networks increase due to larger circulating currents, while the predicted output power values assume lossless power conversion. By comparing the areas

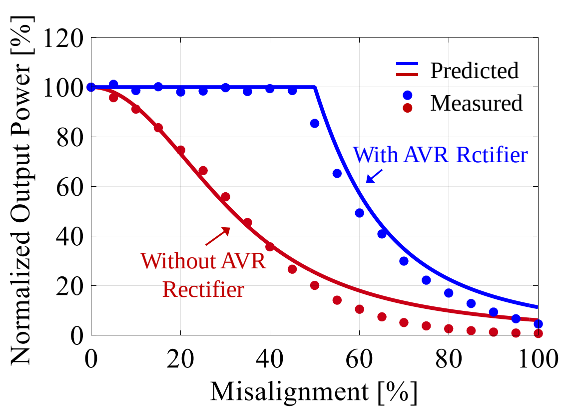


Figure 4.16: Measured and predicted output powers of the 13.56-MHz 12-cm air-gap prototype capacitive WPT system as a function of lateral misalignment in the coupler without (red) and with (blue) the AVR rectifier operation.

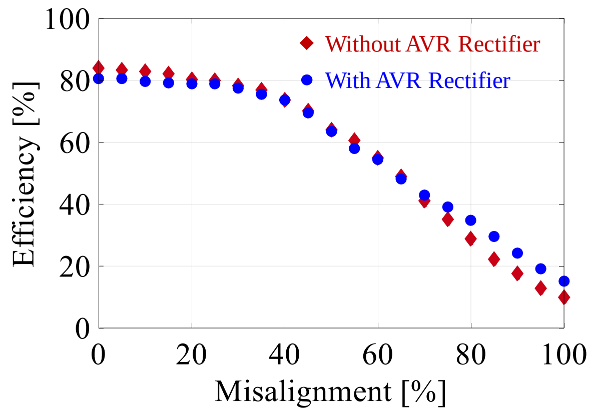


Figure 4.17: Measured efficiencies of the 13.56-MHz 12-cm air-gap prototype capacitive WPT system as a function of lateral misalignments between the roadway-side and vehicle-side coupler without (red) and with (blue) the AVR rectifier operation.

under the measured data points in Fig. 4.16, it can be seen that the prototype capacitive WPT system transfers 80% more energy to the vehicle during a single pass over the charging pad, which is in agreement with the predicted value of 78.5%. Figure 4.17 shows the efficiency of the prototype system with and without the AVR rectifier as a function of misalignment. As can be seen, the efficiency falls in both the cases, however, the rate of fall is lower with the AVR rectifier. It can also be noted that the AVR rectifier enables the prototype system to maintain an almost flat efficiency profile for up to 25% misalignments. The increase in losses in the AVR rectifier with increasing misalignments is due to the higher conversion ratios of its dc-dc converters. A more optimized design of the dc-dc converters can potentially maintain a flatter efficiency profile with misalignment.

The matching network efficiency in the AVR-based capacitive WPT prototype is estimated from experimentally measured data for various values of misalignment, and is shown in Fig. 4.18. To estimate the matching network efficiency, first the measured waveforms of the inverter output voltage and current, and the half-bridge rectifier input voltages and currents are used to determine the combined conduction losses in L_{avr} and C_{avr} are then subtracted from this total loss to determine the matching network losses. As can be seen, the matching network efficiency stays flat for up to 25% misalignments in the coupler. The estimated matching network efficiency in the prototype system without the AVR is

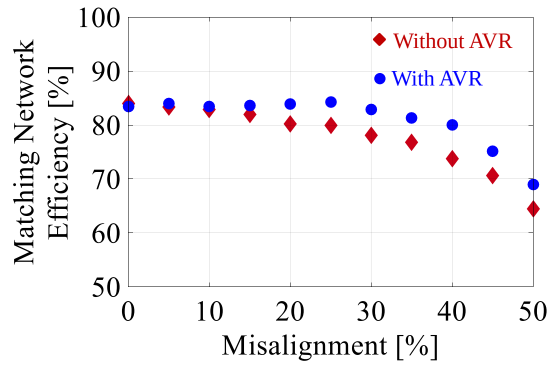


Figure 4.18: Estimated matching network efficiency in the capacitive WPT prototype with and without the AVR rectifier as a function of lateral misalignment between the roadway-side and the vehicle-side coupler.

also shown in Fig. 4.18 over the same range of misalignment. It can be seen that the matching network efficiency is more flat for the system with the AVR rectifier. This is because of increased circulating currents in the system without the AVR rectifier due to uncompensated reactance.

The performance of the prototype capacitive WPT system is also evaluated for various air-gaps between the roadway-side and vehicle-side coupling pads. As the air-gap is increased from its nominal value of 12 cm, the value of the AVR rectifier voltages V_1 and V_2 are changed to compensate for the additional coupling reactance. Figure 4.19 shows the performance of the prototype under such a scenario. As can be seen, the prototype system maintains full output power for air-gaps ranging from 12

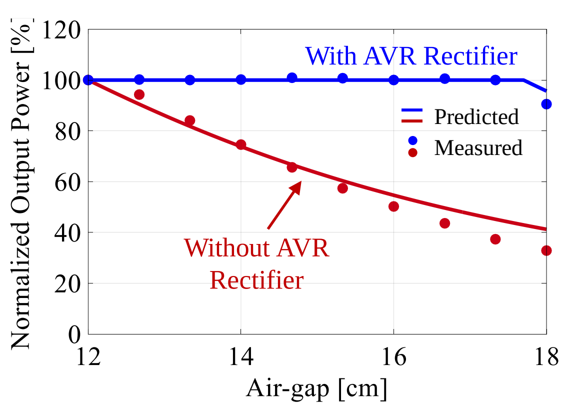


Figure 4.19: Measured and predicted output powers of the prototype capacitive WPT system as a function of air-gap between the roadway-side and vehicle-side coupler without (red) and with (blue) the AVR rectifier operation.

cm to 17.4 cm, corresponding to a 45% increase in air-gap. Thus, when scaled up for EV applications, this system can transfer full charging power to vehicles with different ground clearances. Figure 4.19 also compares the predicted output power of the prototype with and without AVR operation as a function of the air-gap. To generate the predicted power plots, the values of the coupling capacitance are determined as a function of the air-gap using Ansys HFSS electromagnetic field simulator. As can be seen, the measured output power profile matches well with the theoretically predicted values. Figure 4.20 shows the dc-to-dc efficiency of the prototype system with and without AVR rectifier operation as the air-gap is varied. It can be seen once again that the AVR-based system maintains a flatter efficiency profile.

For an actual dynamic EV charging application, the tolerable range of misalignments could potentially be further extended by designing the matching networks to fully compensate for a certain misaligned condition. For example, the matching networks could be designed to fully compensate for the coupling reactance when the charging pads are $\pm 50\%$ misaligned. In such a design, the AVR rectifier would provide no reactance at $\pm 50\%$ misalignment, provide inductive reactance for misalignments beyond $\pm 50\%$, and provide capacitive reactance for misalignments within $\pm 50\%$, as opposed to only providing inductive reactance whenever there is any misalignment. Designing the AVR-rectifier-enabled capacitive WPT system in such a manner could enhance the energy transfer to the vehicle during a single

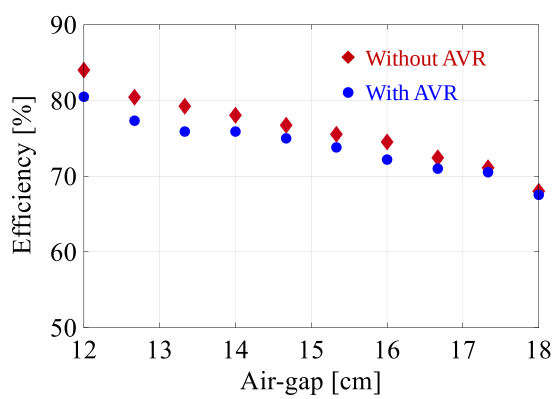


Figure 4.20: Measured efficiencies of the prototype capacitive WPT system with and without the AVR rectifier as a function of air-gap between the roadway-side and vehicle-side coupler.

pass over the charging pad. However, the matching networks of such a system would need to compensate for a larger nominal coupling reactance (corresponding to $\pm$50% misalignment), and the AVR rectifier would require the use of dc-dc converters with both step-up and step-down capability, which may result in a less efficient system.

4.5. Chapter Summary

This chapter introduces the active variable reactance (AVR) rectifier, which can continuously compensate for coupling variations in WPT systems. The AVR rectifier operates at fixed frequency, compensates for coupling variations, and maintains full power transfer by adjusting the output voltages of its two rectifiers. A comprehensive methodology is also proposed for the design of AVR-rectifier-enabled capacitive WPT systems that maximizes the allowable range of coupling variations. A similar approach can be utilized for the design of AVR-rectifier-enabled inductive WPT systems. The proposed approach is validated using a scalable 13.56-MHz, 300-W, 12-cm nominal air-gap prototype capacitive WPT system incorporating an AVR rectifier. This prototype system maintains full power transfer for up to 45% lateral misalignment of the couplers and up to 45% increase in vehicle road clearance. In a dynamic EV charging scenario, the AVR-rectifier-enabled system transfers 80% more energy during a single pass of the vehicle over the charging pad, as compared to a system without the AVR rectifier. The measured performance of the prototype system is in good agreement with the analytical predictions.

CHAPTER 5

CLOSED-LOOP CONTROL OF DYNAMIC CAPACITIVE WPT SYSTEMS

This chapter introduces a closed-loop control strategy for the AVR rectifier in a capacitive WPT system. The proposed approach utilizes a dual-loop control architecture which ensures that the AVR rectifier provides reactive compensation and simultaneously maintains a constant output power. The reference signals for the two control loops are chosen in a way that eliminates the need of high-frequency sensing for measuring coupling variations. An analytical small-signal model of the AVR-rectifier-based capacitive WPT system is developed and design of the controller is discussed. To validate the proposed approach, it is utilized to control the AVR rectifier of a 6.78-MHz capacitive WPT prototype. The prototype is demonstrated to regulate output power for 30% misalignment between charging pads.

5.1. Proposed Control Strategy

In the event of any misalignment, the AVR rectifier in the capacitive WPT system of has to satisfy two control objectives: (i) compensate for the change in coupling reactance, and (ii) maintain a constant output power. An instinctive approach to meeting these objectives would be to maximize output power for any misalignment by utilizing a maximum-power-point tracking (MPPT) algorithm. However, while MPPT ensures that maximum power is restored, it does not guarantee that the change in coupling reactance is compensated, resulting in increased circulating currents and reduced efficiency. This can be understood by noting that output power of the full-bridge inverter of in the capacitive WPT system is given by:

$$P_{\mathrm{OUT}} = \frac{8}{\pi^2} V_{\mathrm{IN}}^2 \frac{R_{\mathrm{inv}}}{R_{\mathrm{inv}}^2 + X_{\mathrm{inv}}^2}, \tag{5.1}$$

where R_{inv} and X_{inv} are the real and imaginary parts, respectively, of the impedance seen by the inverter. Hence, the same output power can be achieved with different combinations of R_{inv} and X_{inv}, while only one of these combinations (corresponding to $X_{\text{inv}} = 0$) ensures that reactive compensation is also achieved. A zero reactance ($X_{\text{inv}} = 0$) can be ensured by sensing the phase difference between the inverter output voltage and current, and controlling this phase to be zero. However, in multi-MHZ capacitive WPT systems, sensing such a phase difference requires very high sampling frequency (~ hundreds of MHz), making the control very sensitive to sensing delays and increasing controller cost. Hence, there is a need for a better control methodology.

This chapter proposes a closed-loop control strategy which restores output power and ensures reactive compensation under misalignment conditions without having to sense high-frequency signals. To understand the proposed control strategy, consider Fig. 5.1, which shows a simplified model of the AVR-rectifier-based capacitive WPT system. Power (P_{OUT}) is transmitted from a constant ac voltage source v to a controllable load resistance R_c through a varying reactance X_v and a controllable reactance X_c. This output power can be expressed as:

$$P_{\text{OUT}} = v^2 \frac{R_v}{R_v^2 + (X_v + X_c)^2}. \tag{5.2}$$

As X_v varies, output power can be maintained in this circuit by controlling the reactance X_c to compensate for the change in X_v (i.e., by ensuring that $X_v + X_c$ remains constant), and keeping the resistance R_c the same. However, as stated before, controlling X_c requires the information of how much change X_v has undergone, and hence, requires high-frequency sensing. The need for high-frequency sensing can be alleviated by noting that when X_v varies, the two quantities that are kept constant are R_v

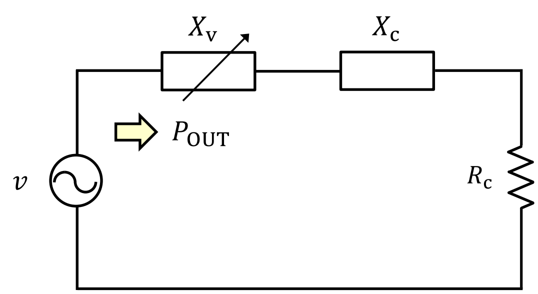


Fig. 5.1: Simplified model of the AVR-rectifier-based capacitive WPT system.

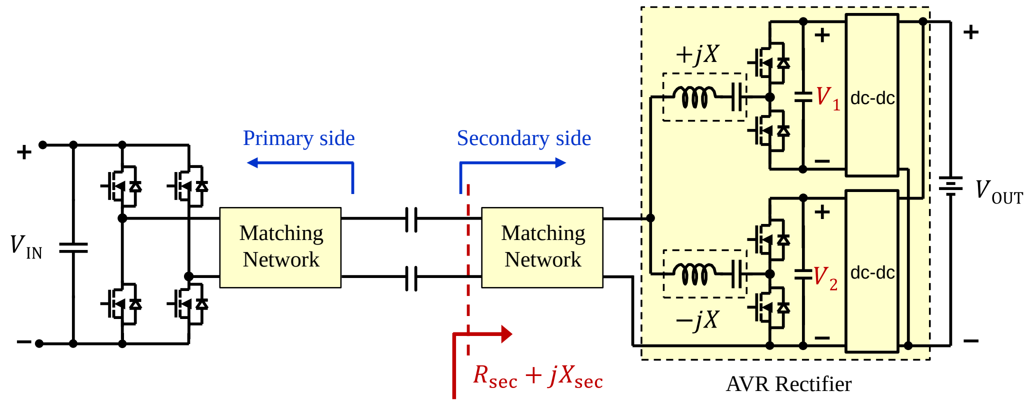


Fig. 5.2: An AVR-rectifier-based capacitive WPT system indicating the impedance looking into the secondary side.

and P_{OUT}. Therefore, simultaneously controlling R_v and P_{OUT} to their required values will automatically ensure that $(X_v + X_c)$ remains constant, i.e., the change in X_v is compensated. In the AVR-based capacitive WPT system (shown in Fig. 5.2), this translates to compensating for coupling variation by maintaining the output power (P_{OUT}) and the resistance looking into the secondary-side (R_{sec}) constant. As will be explained next, both output power and the resistance R_{sec} can be computed by sensing only dc signals, eliminating the need for high-frequency sensing.

The proposed control architecture is shown in Fig. 5.3. It comprises two control loops: the first loop regulates output power, and the second loop regulates value of the secondary-side resistance R_{sec}, thus ensuring reactive compensation. To compute output power and R_{sec}, only the dc voltages V_{OUT}, V_1 and V_2, and the dc currents I_1 and I_2 are sensed. The output power is computed as:

$$P_{\mathrm{OUT}} = V_{\mathrm{OUT}}(I_1 + I_2). \tag{5.3}$$

The secondary side input resistance R_{sec} is determined by first calculating the AVR input impedance as:

$$Z_{\mathrm{r}} = \frac{V_1^2 V_2^2 + V_{\mathrm{OUT}}^2 I_1 I_2 X^2}{V_{\mathrm{OUT}}(V_1^2 I_2 + V_2^2 I_1)} + jX \frac{V_2^2 I_1 - V_1^2 I_2}{V_1^2 I_2 + V_2^2 I_1}, \tag{5.4}$$

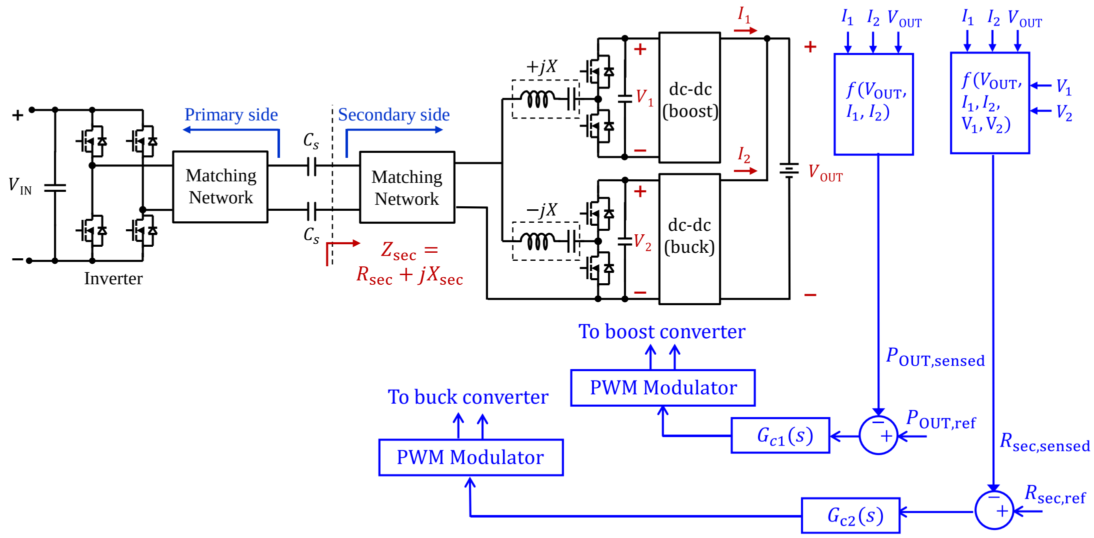


Fig. 5.3: Proposed control strategy for AVR rectifier in a capacitive WPT system.

and then employing impedance transformation of the secondary-side matching network upon Z_r. These measured values of P_{OUT} and R_{sec} are compared to their corresponding reference values $P_{OUT,ref}$ and $R_{sec,ref}$, and the errors are fed through two PI compensators to generate the duty ratios of the two dc-dc converters.

5.2. Small-Signal Modeling and Controller Design

Before designing two controllers in the above control architecture, it is important to identify the small-signal transfer functions from the duty ratios of the dc-dc converters to the output variables of interest, P_{OUT} and R_{sec}. The capacitive WPT system of Fig. 5.3 has two parts operating at very different frequencies: the inverter, matching networks and the rectifiers (termed the 'resonant' part) operate at the ISM-band frequency (6.78MHz, 13.56 MHz etc.), while the dc-dc converters operate at hundreds of kHZ (100 kHz in the prototype system of Chapter 4). Due to nearly two orders of magnitude higher frequency, the resonant part is able to track any voltage or current variations incurred by the dc-dc converters within a very small fraction of the dc-dc converters' switching periods. Therefore, the dynamics of the dc voltages and currents in the system, and hence, those of the output power and R_{sec}, can be assumed to be solely determined by the dynamics of the dc-dc converters. Under the above

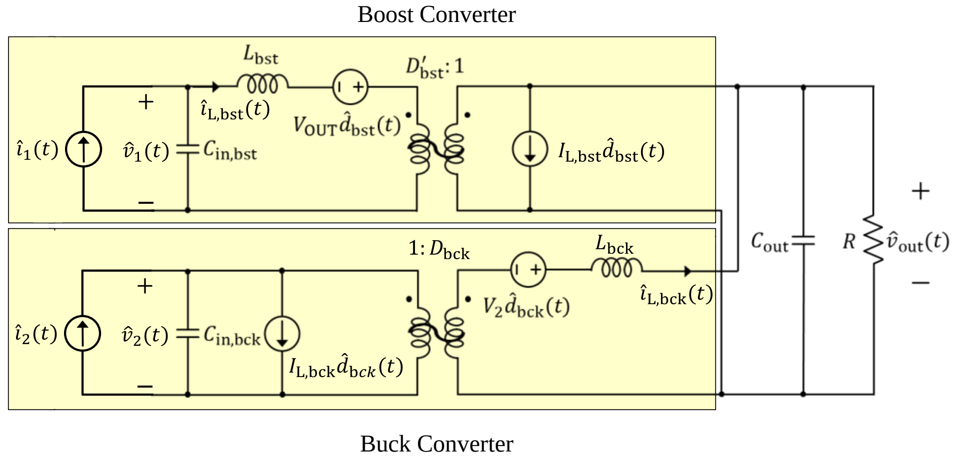


Fig. 5.4: Small-signal model of the dc-dc converter part of the AVR-rectifier-based capacitive WPT system of Fig. 5.2.

assumption, the small-signal model of the capacitive WPT system can essentially be represented by the small-signal model of the dc-dc converters. It can be noted that since one of the AVR voltages must increase and the other must decrease with misalignment (see Fig. 4.2 of the Chapter 4), the top dc-dc converter is implemented as a boost converter, and the bottom one as a buck converter. The combined small-signal model of the boost and buck converters are shown in Fig. 5.4. This model is derived by considering that at a given operating point, the EV battery can be modeled as a capacitor in parallel with a load resistor. In this scenario, controlling the output power delivered to the load resistor translates to controlling the output voltage v_{out}. In this thesis, only the small-signal transfer function from the buck converter duty ratio to the output voltage $\left(\frac{\hat{v}_{\mathrm{out}}}{\hat{d}_{\mathrm{bck}}}\right)$ is derived, and can be repeated to obtain the remaining transfer functions.

The overall transfer function $\left(\frac{\hat{v}_{out}}{\hat{d}_{bck}}\right)$ is derived by first finding it in absence of the boost converter, and then computing the effect of the boost converter using the extra element theorem [92]. In absence of the boost converter, the transfer function can be expressed as:

$$\left(\frac{\hat{v}_{out}}{\hat{d}_{bck}}\right)_{\text{buck}} = \frac{V_{\text{OUT}}}{D_{bck}} \frac{1 + \frac{RC_{\text{in,bck}}}{D_{\text{bck}}^2} s}{1 + R\left(\frac{C_{\text{in,bck}}}{D_{\text{bck}}^2} + C_{\text{out}}\right) s + \frac{L_{\text{bck}} C_{\text{in,bck}}}{D_{\text{bck}}^2} s^2 + \frac{L_{\text{bck}} C_{\text{in,bck}} C_{\text{out}} R}{D_{\text{bck}}^2} s^3}. \tag{5.5}$$

The effect of the boost converter is computed by considering it as an extra element, with the extra element impedance given by the output impedance of the boost converter ($Z_{\text{out,bst}}$), and expressed as:

$$Z_{\text{out,bst}} = \frac{1}{{D'_{\text{bst}}}^2}\left(sL_{\text{bst}} + \frac{1}{sC_{\text{in,bst}}}\right). \tag{5.6}$$

To find the effect of the boost converter using the extra element theorem [92], two port impedances need to be determined: (i) the null impedance Z_{N}, which is the impedance looking from the extra-element port (here, system output port) while nulling the output voltage, and (ii) the impedance Z_{D}, which is equal to the input impedance looking from the extra-element-port with $\hat{d}_{bck}$ set to zero. These two port-impedances are given by:

$$Z_{\text{N}} = 0, \tag{5.7a}$$

and

$$Z_{\text{D}} = R \;||\; \frac{1}{sC_{\text{out}}} \;||\left(sL_{\text{bck}} + \frac{D_{\text{bck}}^2}{sC_{\text{in,bck}}}\right). \tag{5.7b}$$

The small–signal transfer function in presence of both the buck and the boost converter can then be determined using the extra element theorem as:

$$\left(\frac{\hat{v}_{out}}{\hat{d}_{bck}}\right)_{\text{buck+boost}} = \left(\frac{\hat{v}_{out}}{\hat{d}_{bck}}\right)_{\text{buck}} \frac{1+\frac{Z_{\text{N}}}{Z_{\text{out,bst}}}}{1+\frac{Z_{\text{D}}}{Z_{\text{out,bst}}}}. \tag{5.8}$$

The transfer function in absence of the boost converter, given by (5.5), and the transfer function in presence of both the buck and the boost converter, given by (5.8), are shown in Fig. 5.5. If the assumption made previously in this section that the dynamics of the overall system can be solely determined by the

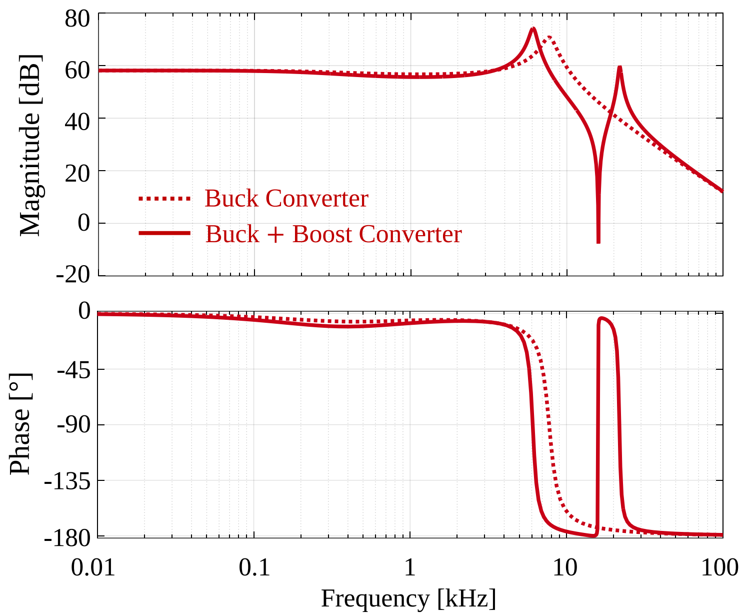


Fig. 5.5: Buck converter duty ratio to output voltage small-signal transfer function $\left(\frac{\hat{v}_{out}}{\hat{d}_{bck}}\right)$.

dynamics of the dc-dc converters is true, the dc-dc converter transfer function given in (5.8) must match the transfer function of the overall system. To validate this, the overall system is simulated in PLECS. A perturbation is given to the buck converter duty ratio at different frequencies and the transfer function of the overall system is determined by observing the magnitude and phase of the resulting perturbation in the output voltage. The modeled transfer function and the simulated transfer functions are overlaid in Fig. 5.6, showing a close match, and hence, validating the previous assumption.

As can be seen from Fig. 5.6, the overall transfer function comprises very high-Q poles and zeros. It is desired to design the dc-dc converters in a way such that these high-Q poles and zeros lie at a much higher frequency than the bandwidth of the dynamic capacitive WPT system. This bandwidth depends on the rate of variation of the voltages V_1 and V_2 of the AVR rectifier. The frequency content of V_1 and V_2 are shown in Fig. 5.7 considering a vehicle speed of 60 mph. As can be seen, most of the frequency content is limited well below 100 Hz, hence, choosing a bandwidth of 100 Hz is sufficient. Since the high-Q poles and zeros seen in Fig. 5.6 are usually at a frequency much higher than 100 Hz, they will

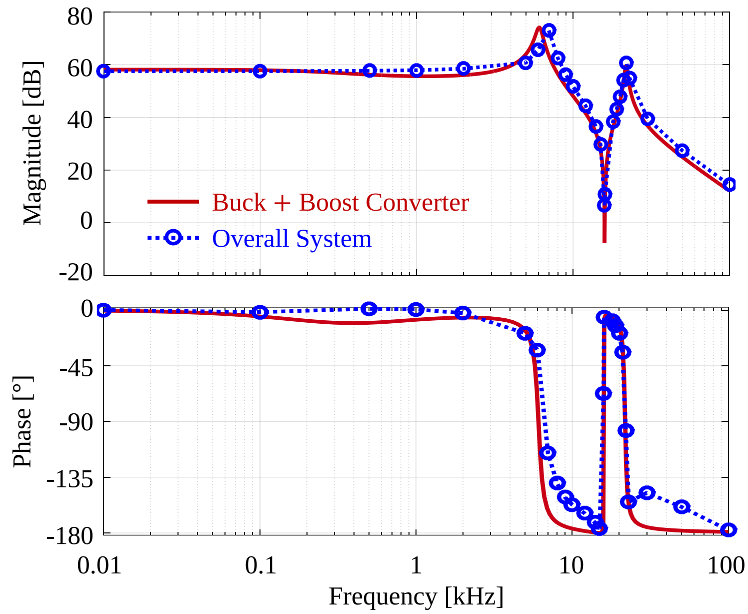


Fig. 5.6: Validation of the modeled small-signal transfer function with simulation of the overall capacitive WPT system.

not significantly affect the controller performance. It can be observed that the transfer function of Fig. 5.6 has a phase close to 0° at the desired bandwidth, hence, using PI controllers to control the loops will suffice. The PI controllers are designed for the worst case dc gain of the uncompensated loops that can occur in the targeted range of tolerable misalignments.

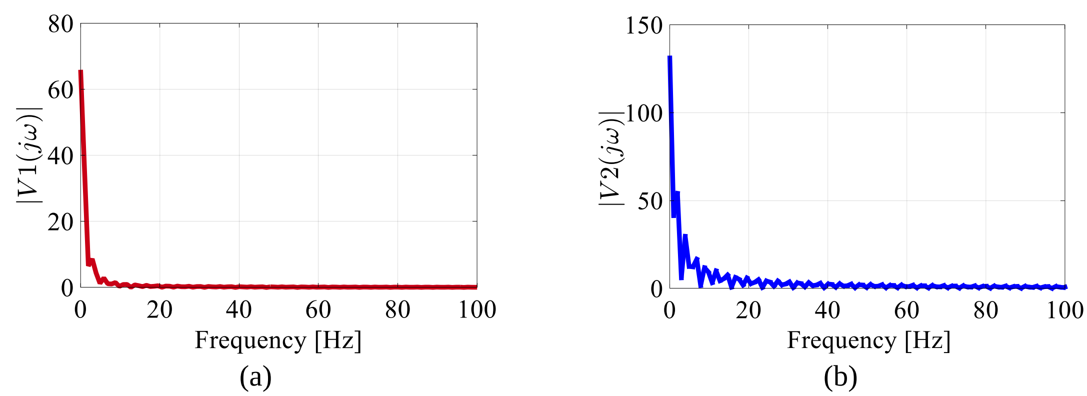


Fig. 5.7: Frequency content of the voltages V_1 and V_2 of the AVR rectifier as they are varied to compensate for misalignments between the charging pad when a vehicle with 12 cm ground clearance is moving at 60 mph.

The AVR-based capacitive WPT system need to simultaneously restore output power and reactive compensation in the event of coupling variation. Therefore, the two feedback loops controlling output power the secondary-side resistance R_{sec} in the control architecture of Fig. 5.3 operate with similar bandwidths. This may lead to significant interaction between the two loops that may adversely affect their operation. Such interactions can be modeled using two cross-connected transfer function blocks as shown in Fig. 5.8 (drawn in red). This interaction can be minimized by introducing two decoupling gains $K_{12}(s)$ and $K_{21}(s)$, as also shown in Fig. 5.8 (drawn in blue). These two gains are designed so that they nullify the effects of the inter-loop transfer functions by maintaining the following relationships:

$$K_{12}(s)G_{\mathrm{p,d_1}}(s) + G_{\mathrm{r,d_1}}(s) = 0, \tag{5.9}$$

$$K_{21}(s)G_{\mathrm{p,d_2}}(s) + G_{\mathrm{p,d_2}}(s) = 0, \tag{5.10}$$

Ideally, the decupling gains $K_{12}(s)$ and $K_{21}(s)$ need to be designed so that (5.9) and (5.10) are satisfied for all frequencies up to the desired crossover frequency of the feedback loops. However, if the magnitude and phase of the open-loop transfer functions at the crossover frequency are nearly the same as in dc (which is likely when the required bandwidth is low), it is sufficient to design these gains so as to satisfy (5.9) and (5.10) only at dc. This renders the decoupling gains to be constant and easier to implement.

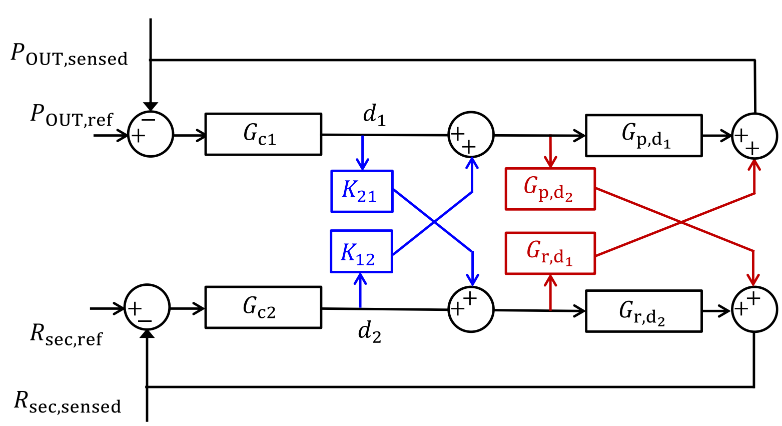


Fig. 5.8: Control loop interactions and decoupling of control loops while regulating the dc-dc converters of the AVR rectifier.

5.3. Experimental Validation

To validate the proposed control strategy, a 6.78-MHz 65-W proof-of-concept scaled prototype capacitive WPT system is designed, built, and tested. A schematic of the prototype is shown in Fig. 5.9, and a photograph of the prototype is shown in Fig. 5.10. Each of the matching networks is implemented using an L section comprising a series inductor and a shunt capacitor. These networks are optimally designed using the guidelines provided in Chapter 3 so as to maximize their efficiency. The capacitive coupler in this system comprise 10 cm × 10 cm plates separated by a 2.5 mm air-gap. The full-bridge inverter, the half-bridge rectifiers, and the dc-dc converters are realized using GaN transistors. The matching network inductors and the inductor in the $+jX$ branch of the AVR rectifier are implemented as single-layer air-core solenoids. The matching network capacitors and the capacitor of the $-jX$ branch of the AVR rectifier are realized with ceramic NP0 capacitors. The inductance and capacitance values used in the matching networks and the AVR rectifier are listed in Table 5.1. The load in this system is emulated using a 5.3 Ω resistor. The closed-loop control is realized using a 200-MHz, 32-bit microcontroller.

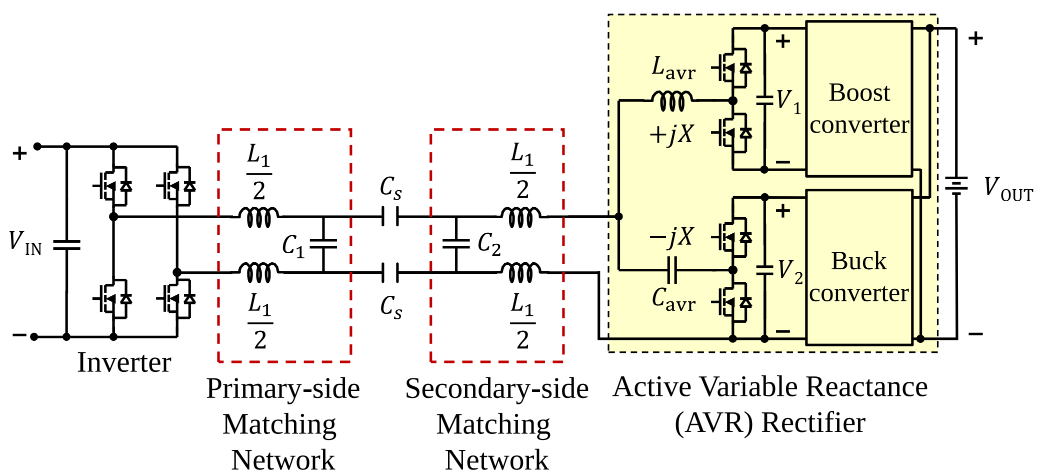


Fig. 5.9: Schematic of the prototype capacitive WPT system with AVR rectifier.

When the primary-side and secondary-side coupling plates are fully aligned to one another, and the dc-dc converter of the AVR rectifier operate in pass-through mode, the prototype

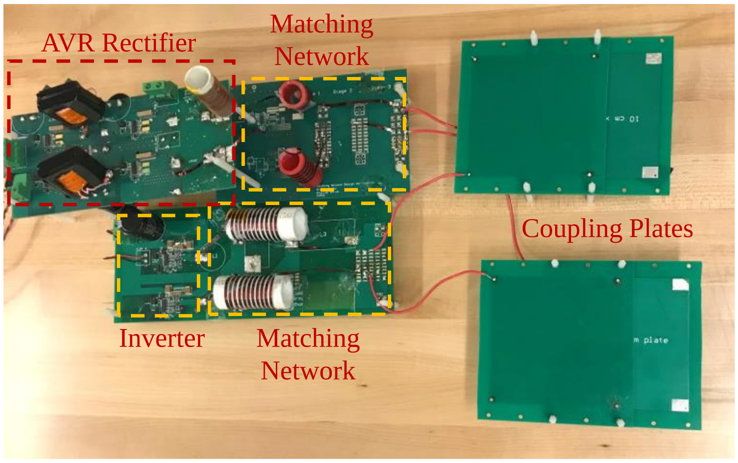


Fig. 5.10: Photograph of the prototype capacitive WPT system with AVR rectifier.

TABLE 5.1: COMPONENTS USED IN THE ACTIVE ARIABLE REACTANCE RECTIFIER PROTOTYPE

Component	Value	Description
Inverter, Rectifier, and dc-dc Converter Transistors	–	GS66506T 650-V/22-A eGaN FETs
C_s	36 pF	10cm × 10 cm plates, 2.5 mm air-gap
L_1	1.4 µH	Air-core single-layer solenoid
C_1	381 pF	NP0 ceramic capacitor
L_2	3.8 µH	Air-core single-layer solenoid
C_2	126 pF	NP0 ceramic capacitor
L_{avr}	163 nH	Air-core single-layer solenoid
C_{avr}	3.3 nF	NP0 ceramic capacitor

system delivers 65 W across the air-gap, resulting in a voltage of 18.5 V across the resistive load. As the coupling plates are misaligned, the output power, and consequently the voltage across the load resistor falls. In order to test the operation of the closed-loop AVR rectifier, the plates are first misaligned by 30% with the dc-dc converters still kept in pass-through mode, and then the controller is turned on. The resulting waveforms of the system output voltage V_{OUT}, and the input voltages of the two dc-dc converters V_1 and V_2, are shown in Fig. 5.11. As can be seen, when the dc-dc converters are in pass-through mode, all three voltages are at 15.1 V, corresponding to an output power of 43 W. When the controller is turned on, the input voltage of the boost converter (V_1) falls to 7.2 V, and the input voltage of the buck converter (V_2) rises to 20 V, causing the output voltage to rise to its nominal value of 18.5 V, and the output power to its nominal value of 65 W $-$ validating the operation of the proposed control strategy.

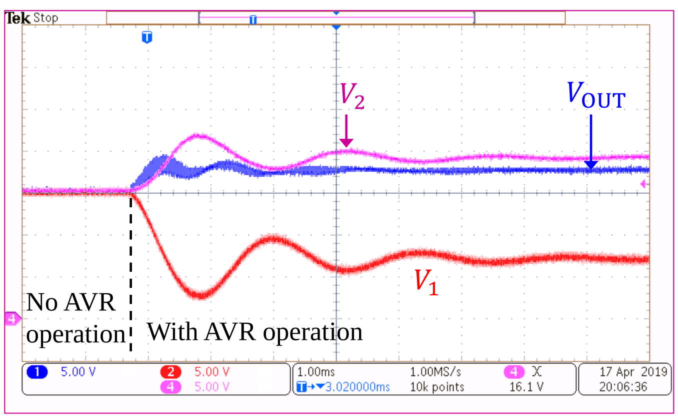


Fig. 5.11: Measured waveforms of the output voltage and the input voltages of the dc-dc converters of the capacitive WPT prototype demonstrating closed-loop operation of the AVR rectifier.

5.4. Chapter Summary

A closed-loop control approach is proposed that enables the AVR rectifier in a capacitive WPT system to provide reactive compensation and maintain constant output power for large coupling variations. The proposed approach employs a dual-loop control strategy to regulate the dc-dc converters of the AVR rectifier. The loop references are chosen in an innovative way so that the coupling variations can be compensated without requiring any high-frequency sensing. An analytical small-signal model of the AVR-based capacitive WPT system is derived and verified with simulation. A 6.78-MHz 65-W capacitive WPT prototype is built and its AVR rectifier is controlled using the proposed approach. The prototype system is demonstrated to maintain full output power for up to 30% misalignments between the couplers.

CHAPTER 6

COMPARISON WITH INDUCTIVE WPT SYSTEMS

The previous chapters have established that capacitive WPT systems can achieve high power transfer density and high efficiency, and when combined with an AVR rectifier, can maintain a constant power transfer even for large variation in coupling conditions. However, capacitive WPT is still an exploratory field, and have merely been used for commercial purposes. On the other hand, inductive WPT systems, having gone through extensive research over the past two decades, have started to be commercially deployed in consumer electronics, robotics, and even dynamic EV charging applications. Both the WPT systems have their benefits, and both have the potential of large scale commercialization. Therefore, to focus future research in the right direction, and to be able to select the right WPT method for an application, it is important to compare the potentials of both inductive and capacitive WPT systems.

This chapter presents a theoretical comparison between inductive and capacitive WPT systems. The maximum power transfer capabilities of the two WPT systems are formulated while adhering to their physical limits, with the limit set by saturation of the magnetic core in inductive WPT systems, and by electric breakdown of air in capacitive WPT systems. The efficiency of inductive and capacitive WPT systems are formulated in terms of the system specifications, and the tradeoff between efficiency and power transfer density are compared. It has been shown that capacitive WPT systems are favored by a higher operating frequency, while inductive WPT systems are favored by a larger gap to area ratio. Introduction of multistage compensation networks increases the efficiency of both systems, but the improvement is significantly higher for capacitive WPT systems, resulting in a better tradeoff between efficiency and power transfer density.

6.1. Architecture and Implementation of Inductive and Capacitive WPT Systems

The general architecture of the inductive and capacitive WPT systems considered for comparison in this chapter is shown in Fig. 6.1. In both inductive and capacitive WPT systems, an inverter converts the dc input voltage (V_{IN}) to a high-frequency ac voltage (v_{inv}), which is then stepped up by the primary-side matching network. In inductive systems, this high voltage (v_{p}) enables high power transfer with relatively small currents through the coils, and hence, smaller fringing magnetic fields, while in capacitive systems, the high voltage enables high power transfer with relatively small displacement current through the coupling plates, resulting in smaller fringing electric fields. Another matching network on the secondary side steps the current back up and the voltage down to a level (V_{OUT}) required to charge the battery. A high-frequency rectifier interfaces the battery to the WPT systems. To ensure effective power transfer, the two matching networks also compensate for the reactance of the coupler (which is inductive for the inductive WPT system and capacitive for the capacitive WPT system) so that the impedance seen by the inverter stays near-resistive.

An example implementation of both the inductive and capacitive WPT systems is shown in Fig. 6.2. The inductive coils form a loosely coupled transformer which is represented in Fig. 6.2(a) by a T-network (L_{p} and L_{s} denote the self-inductance of the primary-side and secondary-side coils, respectively, and M denotes the mutual inductance). The capacitances of the coupling plates in the capacitive WPT systems are denoted by C_{s} in Fig. 6.2(b). The inverter and the rectifier are implemented with a full-bridge topology, and the matching networks with a single-stage L-section topology. Note

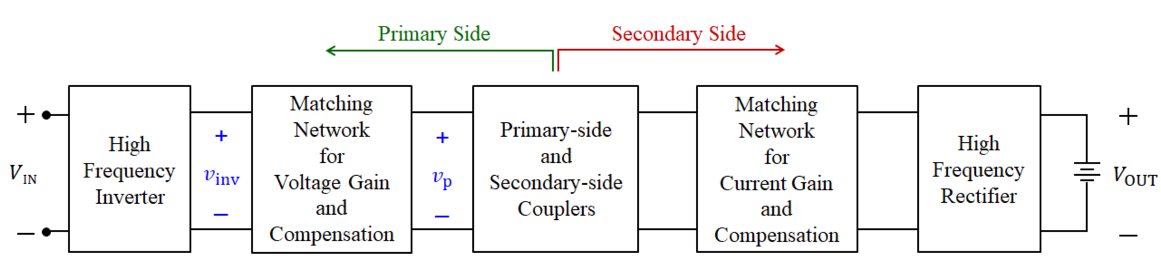


Fig. 6.1: Architecture of a WPT system.

that in the matching networks of the inductive WPT system, the inductance is in the shunt branch and the capacitance is in the series branch, while in the capacitive WPT system their positions are flipped. This allows these networks to provide the right polarity of gain and compensation. To understand this, let us consider a simple case when these networks only provide the required compensation, and do not provide any current step-down/step-up. Since no gain is required, the shunt branches of these networks would be open. Under such a condition, the series capacitors of the inductive WPT matching networks would be able to provide a capacitive compensation, while the series inductors of the capacitive WPT matching networks would be able to provide an inductive compensation.

Inductive WPT systems have previously been realized using other forms of matching networks, including series-series compensation network, series-parallel compensation network, and LCC compensation network. However, for a fair comparison, the matching networks are assumed to be L-section in both cases, and have topologies dual to one another.

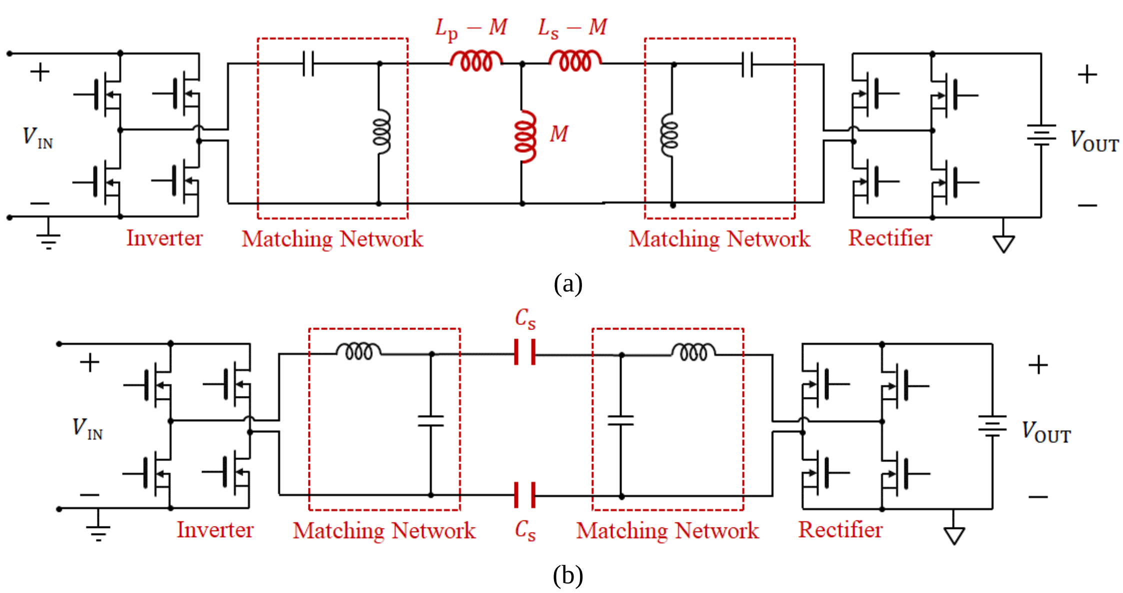


Fig. 6.2: An example implementation of (a) an inductive WPT system and (b) a capacitive WPT system.

6.2. Maximum Power Transfer Capability of Inductive and Capacitive WPT Systems

To compete with conventional gasoline vehicles in terms of refuel time, and to enable dynamic and semi-dynamic charging, it is imperative to charge EVs faster, requiring chargers with large power transfer capability. Furthermore, expansion of WPT to applications such as charging electric buses [93], heavy-duty trucks [94] and even trains [95] comes with a rapidly growing power demand from WPT systems. Therefore, the maximum power transfer capability is a very important parameter for the success of a wireless charging technology. The maximum power transfer capability of a WPT system primarily depends on the physical limits of the system (assuming that the electronic components of the system are thermally capable of delivering this power). In an inductive WPT system, a higher power transfer

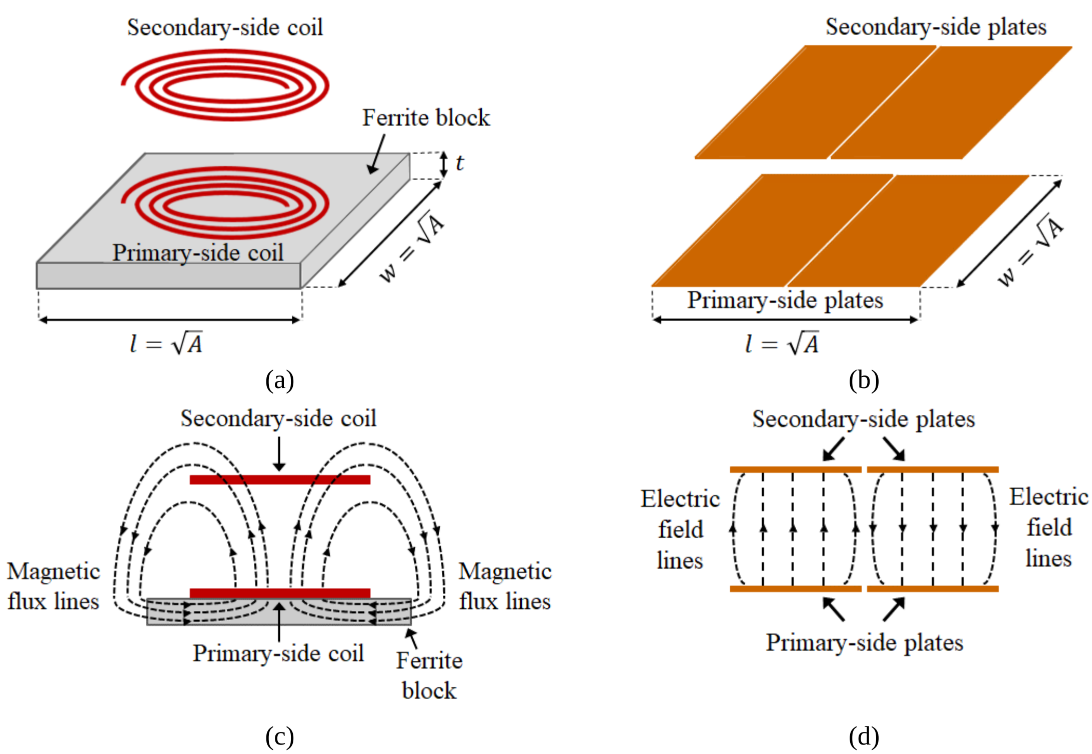


Fig. 6.3: Construction of WPT couplers: (a) inductive WPT coupler with primary-side and secondary-side coils (the ferrite block on the secondary-side is not shown for the purpose of clarity), (b) capacitive WPT system with primary-side plates and secondary-side plates. Both the WPT couplers are square-shaped and occupy an area A on both primary and secondary sides, and the ferrite block in the inductive WPT has a thickness t. Front view of the two WPT systems and their power transfer mechanisms: (c) in inductive WPT, the magnetic flux lines generated by the primary-side coil links to the secondary-side coil and returns through the ferrite blocks, (d) in capacitive WPT, the electric field lines generated from a primary-side plate links to a secondary-side plate and vice versa.

translates to a larger current through the coupling coils, and hence, a larger magnetic flux density in the ferrite core. Therefore, the power transfer capability of an inductive WPT system is limited by the saturation flux density of its ferrite core (B_{max}). Similarly in a capacitive WPT system, a higher power transfer translates to a larger voltage across the air-gap, and in turn, a higher electric field intensity in the air-gap. The power transfer capability in capacitive WPT systems are thus limited by the maximum allowable electric field intensity in the air-gap (E_{max}) that does not cause breakdown of air. Figure 6.3 shows the construction of an inductive and a capacitive WPT system, demonstrating the magnetic flux lines inside the ferrite core of the inductive WPT system, and the electric field lines in the air-gap of the capacitive WPT system. Since an inductive WPT system behaves like a loosely coupled transformer [96], the resultant flux in the primary-side core can be approximated as the magnetizing flux generated by the primary-side coil. If the primary-side coil generates a magnetizing flux ϕ, the flux density in the primary-side core can be expressed as:

$$B = \frac{\phi}{\sqrt{A}t}, \tag{6.1}$$

where A is the area of the square-shaped core, and t is the thickness of the core, as shown in Fig. 6.3(a). In a capacitive WPT system, given an air-gap voltage v_{ag} and an air-gap length d, the electric field intensity in the air-gap can be approximated by neglecting fringing effect as:

$$E = \frac{v_{\text{ag}}}{d}. \tag{6.2}$$

To analyze power transfer in an inductive and a capacitive WPT system, their dc input voltage, inverter and primary-side matching network are modeled as a Thevenin-equivalent ac voltage source v_{th} in series with a Thevenin impedance Z_{th}, and their secondary-side matching network and rectifier and the battery are modeled as another impedance Z_{sec}, as shown in Fig. 6.4. For simplicity of the analysis, let us assume that all the reactive compensation is provided by the primary-side matching network, and hence,

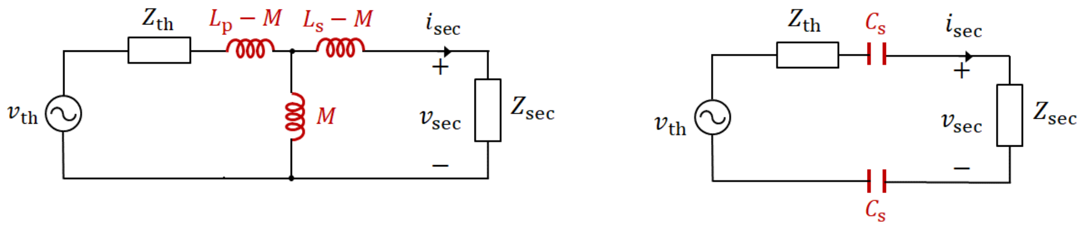


Fig. 6.4: Thevenin equivalent model of (a) an inductive WPT system and (b) a capacitive WPT system.

the impedance looking from the secondary-side of the coupler is resistive (i.e., $Z_{\rm sec} = R_{\rm sec} + j0$). In the inductive WPT system of Fig. 6.4(a), the voltage generated across the secondary-side coil is given by:

$$v_{\rm sec} = N_2 \left|\frac{d\phi_{\rm s}}{dt}\right| = 2\pi f_{\rm ipt} N_2 \phi_{\rm s}, \tag{6.3}$$

where N_2 is the number of turns in the secondary-side coil, $f_{\rm ipt}$ is the operating frequency of the system, and $\phi_{\rm s}$ is the portion of the flux generated by the primary-side coil that is linked to the secondary side. Using (6.1) and (6.3), the maximum power transfer capability of the inductive WPT system can be expressed as:

$$P_{\rm ipt,max} = v_{\rm sec,max} i_{\rm sec} = 2\pi f_{\rm ipt} \sqrt{A} t \kappa B_{\rm max} N_2 i_{\rm sec}, \tag{6.4}$$

with $i_{\rm sec}$ being the current in the secondary-side coil, and κ being the coupling coefficient that represents how much fraction of the primary-side generated flux is linked to the secondary side.

In the capacitive WPT system of Fig. 6.4(b), given an air-gap voltage $v_{\rm ag}$, the displacement current through the air-gap $i_{\rm ag}$ can be expressed as:

$$i_{\rm ag} = 2\pi f_{\rm cpt} C_{\rm s} v_{\rm ag} = 2\pi f_{\rm cpt} \epsilon_0 \frac{A}{2d} v_{\rm ag}, \tag{6.5}$$

where $f_{\rm cpt}$ is the operating frequency of the system, and A is the total area of the coupling plates on either the primary or the secondary side. Using (6.2) and (6.5), the maximum power transfer capability of the capacitive WPT system can be expressed as:

$$P_{\text{cpt,max}} = v_{\text{sec}} i_{\text{sec,max}} = v_{\text{sec}} i_{\text{ag,max}} = \pi f_{\text{cpt}} A \epsilon_0 E_{\max} v_{\text{sec}}, \tag{6.6}$$

Dividing (6.4) by (6.6), the ratio of the power transfer capabilities of the inductive and capacitive WPT systems can be expressed as:

$$\frac{P_{\text{ipt,max}}}{P_{\text{cpt,max}}} = 2\left(\frac{f_{\text{ipt}}}{f_{\text{cpt}}}\right)\left(\frac{B_{\max}}{\epsilon_0 E_{\max}}\right)\frac{t}{\sqrt{A}}\kappa\frac{N_2}{R_{\text{sec}}}. \tag{6.7}$$

For a saturation flux density of 0.5 T and an electric field breakdown limit of 3 MV/m, the factor $\left(\frac{B_{\max}}{\epsilon_0 E_{\max}}\right)$ in (6.7) is of the order of ~10^4, providing a first-glance impression that the inductive WPT system can potentially transfer much larger power than the capacitive WPT system. This is in line with the common intuition that since the value of the permeability of air (μ_0) is several orders of magnitude higher than its permittivity (ϵ_0), the magnetic field has a much higher energy density than the electric field. Therefore for a given coupler area, an inductive WPT system is able to store much higher energy in its air-gap than the capacitive WPT system. However, the transferred power does not only depend on the energy that can be stored in the air-gap, but also on how frequently this energy is delivered to the output, i.e., the operating frequency of the system. Therefore, capacitive WPT systems can potentially achieve power transfer capabilities similar to inductive WPT systems by operating at ~10^4 times higher frequency, which is also understood from (6.7).

However, the power transfer ratio given in (6.7) also depends on other geometrical and electrical parameters of the WPT system. In line with common intuition, using a coil with higher number of turns (enabling more flux generation) and a thicker ferrite block (allowing more flux without core saturation) increases the power transfer capability of an inductive WPT system. On the other hand, a larger coupling area favorably impacts capacitive WPT systems. This is because in capacitive WPT systems, a larger plate area allows proportionally more electric flux in the air-gap, and proportionally more power transfer, while in inductive WPT systems, the magnetic flux can only increase proportional to the core length/width (i.e., the square root of the area), as long as the thickness of the block is kept the same (see

(6.1)). It is interesting to note that a higher magnitude of the secondary-side impedance R_{sec}, which can be obtained by increasing the gain of the secondary-side network, also favorably impacts capacitive WPT systems. This is because in a capacitive WPT system, for the same electric field intensity in the air-gap (and hence the same displacement current through the coupling plates), a higher R_{sec} leads to a larger power transfer. In contrast in an inductive WPT system, for the same flux density in the core (and hence same induced voltage across the secondary-side coil), a higher R_{sec} leads to a smaller power transfer.

To gain a quantitative intuition, let us consider an inductive and a capacitive WPT system each having a coupling area of 30 cm $\times$ 30 cm. Let us assume that the thickness of the ferrite block is 10% of its length/width, i.e., 3 cm, the coils use 5-mm diameter wires, allowing 30 turns, and the inductive WPT system has a coupling factor of 0.3 (which is fairly common for medium-range systems). With these parameters, a 170 Ω of secondary-side resistance R_{sec} will ensure that the capacitive WPT system need to operate at only 100 times higher frequency to achieve the same power transfer capability as the inductive WPT system. With the use of GaN transistors that are able to switch at multi-MHz frequencies, and the fact that high-power inductive WPT systems usually limit their operating frequencies to tens to a couple of hundreds of kHz, it can be deduced that capacitive WPT systems have the potential to achieve similar power transfer capabilities as inductive WPT systems given that the high-switching-speed transistors are thermally well managed.

6.3. Maximum Achievable Efficiency in Inductive and Capacitive WPT Systems

In capacitive WPT systems, the major source of losses are its matching network inductors. The losses in the coupling plates, which may arise due to surface conduction or induced eddy currents, and the switching and conduction losses in the inverter and the rectifier transistors, are usually insignificant in comparison (losses in the matching network inductors constitute up to 95% of the overall losses in the prototype systems presented in the previous chapters). Therefore, the total loss in a capacitive WPT system can be approximated by its matching network losses. On the contrary, in inductive WPT systems, both the matching networks and the coupling coils contribute comparably to the overall losses, and both must be considered in efficiency estimation. In the subsequent analysis, first the matching network losses in inductive and capacitive WPT systems are compared, assuming that the inductive coupler is lossless. Then the losses in the inductive coupler is added and its effect is analyzed. In all the subsequent analysis, it is assumed that the parasitic resistance and capacitance of the transistors used in both inductive and capacitive WPT systems have negligible impact on their overall efficiency at all operating power and frequency levels.

As described in Chapter 3, the losses in the matching network of a WPT system depends on the gain and compensation it provides. Typically, the higher the gain and compensation a network provides, the higher are its losses. Applying the optimized matching network design approach proposed in chapter 3, the overall efficiency of the single-stage L-section networks of the capacitive WPT system Fig. 6.1(b) can be expressed as:

$$\eta_{\mathrm{mn,cpt}} \approx 1 - \frac{2\sqrt{\frac{2P_{\mathrm{cpt}}}{k_{\mathrm{inv}}\sqrt{2k_{\mathrm{rec}}}V_{\mathrm{IN}}V_{\mathrm{OUT}}}\left(\frac{1}{\omega_{\mathrm{cpt}}\left(\frac{C_S}{2}\right)}\right)}}{Q_{\mathrm{L,cpt}}}, \tag{6.8}$$

where P_{cpt} is the transferred power, $\omega_{\mathrm{cpt}} = 2\pi f_{\mathrm{cpt}}$, k_{inv} is a gain associated with the inverter, and is equal to $4/\pi$ for the full-bridge inverter of Fig. 6.2(b), k_{rec} is a gain associated with the rectifier, and is equal to $8/\pi^2$ for the full-bridge rectifier of Fig. 6.2(b), and $Q_{\mathrm{L,cpt}}$ is the unloaded quality factor of the matching network inductors. Applying similar design approach to the inductive WPT system, its matching network efficiency can be expressed as:

$$\eta_{\mathrm{mn,ipt}} \approx 1 - \frac{2\sqrt{\frac{2P_{\mathrm{OUT}}}{k_{\mathrm{inv}}\sqrt{2k_{\mathrm{rec}}}V_{\mathrm{IN}}V_{\mathrm{OUT}}}(\omega_{\mathrm{ipt}}M)}}{Q_{\mathrm{L,ipt}}}, \tag{6.9}$$

Where $\omega_{\text{ipt}} = 2\pi f_{\text{ipt}}$, and $Q_{\text{L,ipt}}$ is the unloaded quality factor of its matching network inductors. It can be seen from (6.8) and (6.9) that the efficiencies of both the WPT systems falls with output power, and increases with input and output voltages. Furthermore, the higher the reactance that needs to be compensated ($\omega_{\text{ipt}}M$ for the inductive WPT system and $\frac{1}{\omega_{\text{cpt}}\left(\frac{C_S}{2}\right)}$ for the capacitive WPT system), the lower is the matching network efficiency. However, since an inductive reactance increases with frequency and a capacitive reactance decreases with frequency, the matching network efficiency of the inductive WPT system falls with frequency while that of the capacitive WPT system rises with frequency. Assuming that both the WPT systems are operated at the same frequency f, and their matching network inductors have the same quality factor, the ratio of losses in the two WPT systems can be expressed using (6.8) and (6.9) as:

$$\frac{P_{\text{loss,ipt}}}{P_{\text{loss,cpt}}} \approx 2\pi f \sqrt{M\left(\frac{C_S}{2}\right)}. \tag{6.10}$$

As expected, a higher operating frequency results in relatively lower losses in the matching networks of the capacitive WPT system. On the other hand, a smaller mutual inductance favorably impacts the efficiency of the inductive WPT system, while a smaller coupling capacitance negatively impacts the efficiency of the capacitive WPT system. This is expected since a smaller mutual inductance will reduce the compensation requirement in the inductive WPT system, but a smaller coupling capacitance will increase the compensation requirement in the capacitive WPT system. It is interesting to note that a smaller mutual inductance or a smaller coupling capacitance both correspond to a larger air-gap or a smaller coupling area. Therefore, the relative losses in the inductive WPT system will be smaller for a smaller area to gap ratio.

The above comparison only concerns losses in the matching networks of both the systems. As stated previously, the losses in the coupler of the inductive WPT system also contribute significantly to its overall losses. The losses in the coupler of the inductive WPT systems has been expressed in previous literature [97] as:

$$P_{\mathrm{loss,coil}} = \frac{2}{Q_{\mathrm{c}}}\sqrt{\frac{L_{\mathrm{p}}L_{\mathrm{s}}}{M}}P_{\mathrm{OUT}}, \tag{6.11}$$

Q_{c} being the unloaded quality factor of the coil. The coil quality factor in inductive systems are usually comparable or sometimes much smaller than the quality factor of the matching network inductors, and can add significant losses to the system.

To compare the above losses quantitatively, an inductive and a capacitive WPT system with the same coupling area, air-gap and input and output voltages are considered. The detailed specifications of these systems are provided in Table 6.1. The coils of the inductive WPT system are constructed in a way that utilizes all the available coupling area. The mutual inductance of the inductive WPT coupler is computed by using the empirical expression given in [98]. Figure 6.5 shows the efficiencies of both the systems as a function of their power transfer density for three different operating frequencies: (a) 200 kHz, (b) 2 MHZ, and (c) 20 MHz. Power transfer density in Fig. 6.5 is increased by keeping the coupling area same and increasing the output power of the systems. The matching network inductors of both the systems and the coupling coil of the inductive WPT system are assumed have a quality factor of 500. As the

TABLE 6.1: SPECIFICATIONS OF THE COMPARED INDUCTIVE AND CAPACITIVE WPT SYSTEMS

Total coupling area	30 cm × 30 cm
Air-gap	12 cm
Input voltage	400 V
Output voltage	400 V
Coil wire diameter	8.25 mm (AWG0)
Number of turns	18

frequency increases, the efficiency of a capacitive WPT system rises closer to that of the inductive WPT system, and in this example is even higher than the inductive WPT system's efficiency at a frequency of 20 MHz. As stated previously, the recent development of high-switching-speed GaN transistors enables efficient operation at multi-MHz frequency level, which opens the door for pushing the efficiency limits of capacitive WPT systems.

One way to improve the efficiency of both the WPT systems is to use multistage matching networks, the advantages of which are demonstrated in Chapter 3. In a multistage network, each stage provides a part of the required overall gain and compensation, and hence, are more efficient than a single-stage

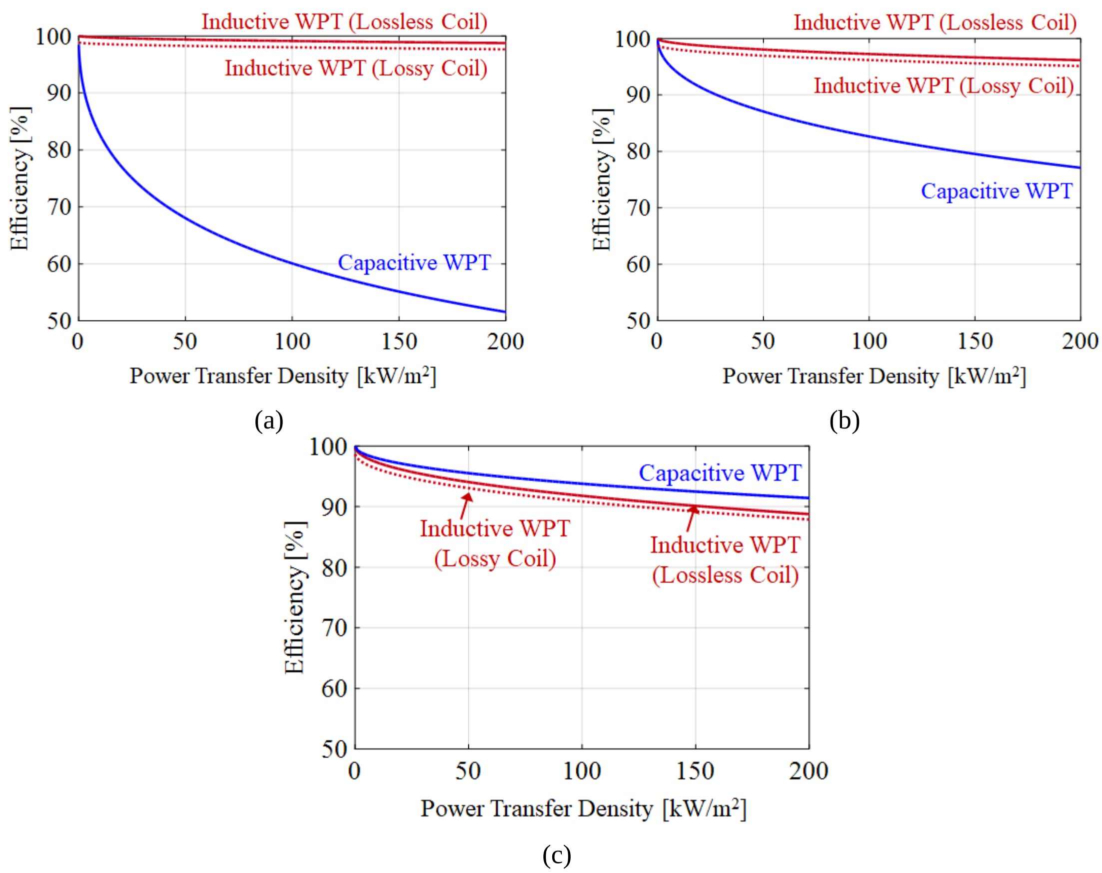


Fig. 6.5: Comparison of the efficiency of an inductive and a capacitive WPT system having the specifications of Table 6.1 as a function of their power transfer density for three different operating frequencies: (a) 200 kHz, (b) 2 MHz, and (c) 20 MHz.

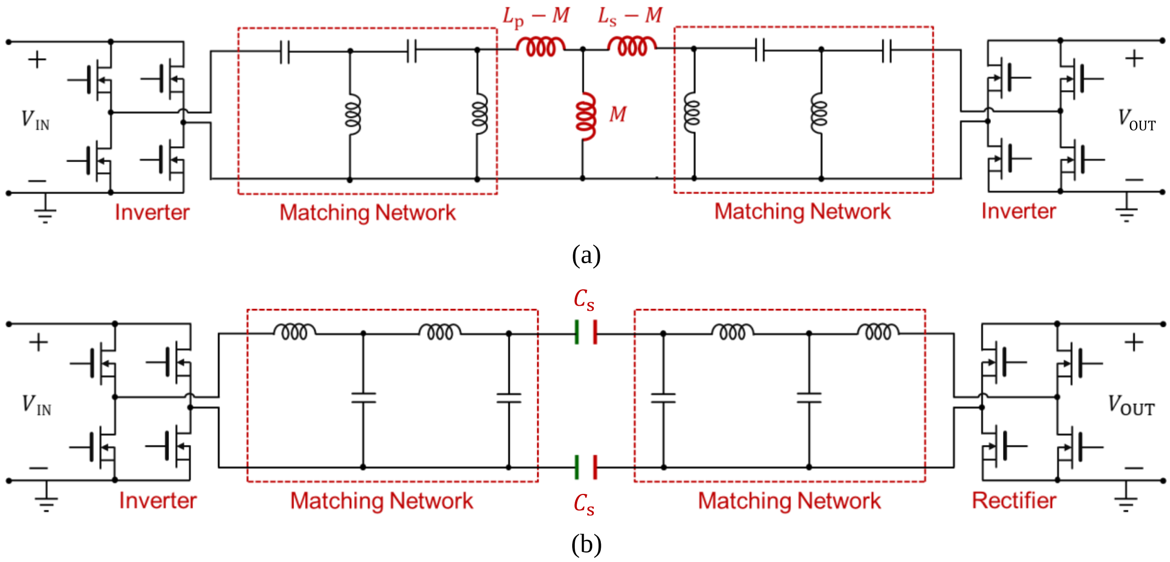


Fig. 6.6: (a) An inductive WPT system and (b) a capacitive WPT system with two-stage matching networks.

network. This opens up the possibility that the multistage network, a collection of multiple less lossy stages, can have a higher overall efficiency than its single-stage counterpart. To evaluate the advantages of multistage networks, the example inductive and capacitive WPT systems considered above are designed with two-stage matching networks, as shown in Fig. 6.6. The efficiencies of the single-stage and two-stage versions of the systems are compared in Fig. 6.7, and the corresponding loss reduction in the two systems are shown in Fig. 6.8. As can be seen, the loss reduction of the capacitive WPT system

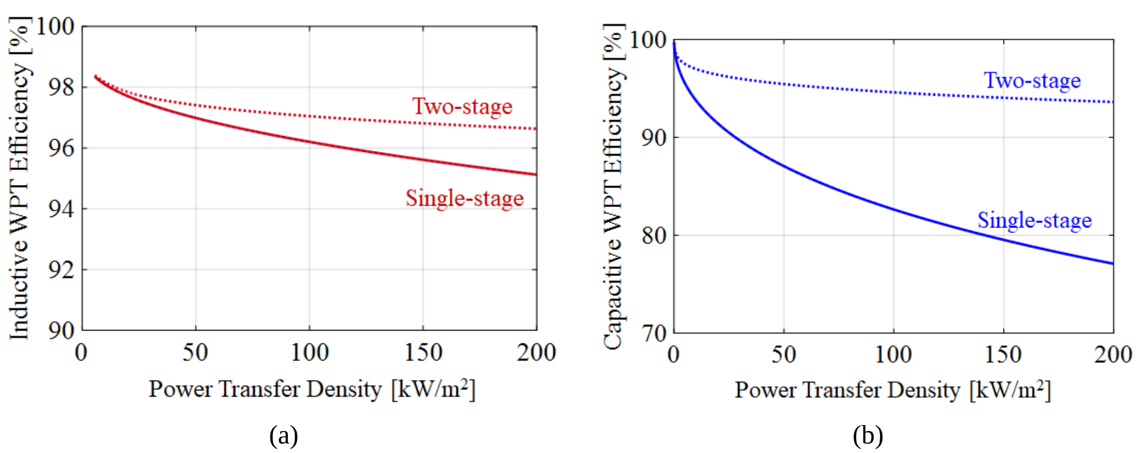


Fig. 6.7: Efficiency comparison between a single-stage and a two-stage matching network based WPT system: (a) inductive WPT system, (b) capacitive WPT system.

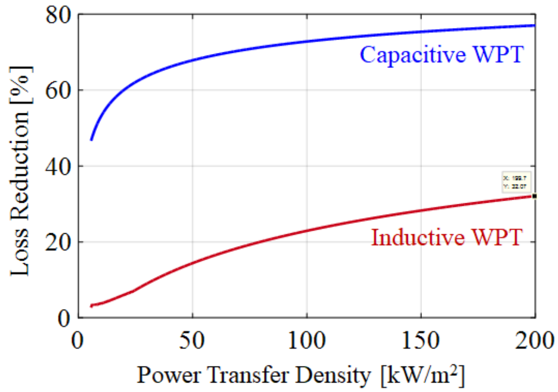


Fig. 6.8: Loss reduction enabled by the use of two-stage matching networks in an inductive and a capacitive WPT system.

is more than twice that of the inductive WPT system. The reason is that using multiple stages only improves the efficiency of the matching networks, whereas a significant portion of the losses in the inductive WPT system is in its coils. This relative advantage would enable a capacitive WPT system with two-stage matching networks to achieve efficiencies comparable to inductive systems at a lower frequency.

6.4. Chapter Summary

A theoretical comparison of the power transfer capabilities and achievable efficiencies of inductive and capacitive WPT systems is presented. The power transfer capability of the WPT systems are formulated while adhering to their physical limits. It is observed that the capacitive WPT system can potentially achieve similar power transfer as inductive WPT systems at ~100 times the operating frequency, which is possible since capacitive WPT systems do not use ferrites and does not suffer from associated high-frequency losses. The power transfer capability of the capacitive WPT systems is found to be more favorably impacted by a lager coupling area then the inductive WPT systems. In terms of efficiency, capacitive WPT systems are favored by a higher operating frequency, whereas inductive WPT systems are favored by a smaller area to gap ratio. The use of multistage matching network is shown to increase the efficiency of both the systems, however, the improvement is much less for inductive WPT systems since the coupler in these systems also contribute to a significant portion of the overall losses.

CHAPTER 7

SUMMARY AND CONCLUSIONS

7.1. Thesis Summary and Conclusions

Wireless power transfer (WPT) can enhance consumer convenience and safety by enabling autonomous charging in applications ranging from biomedical implants, portable and consumer electronics and electric vehicles (EVs). WPT can especially transform EV charging technology by transferring power to the EV battery from the roadway through air while the vehicle is in motion. This drastically brings down the size and cost of the batteries and enable zero charging time and potentially unlimited range, accelerating EV adoption and propelling us to a greener future.

Wireless power transfer is conventionally achieved using inductive techniques where energy is transferred from a transmitting coil to a receiving coil through magnetic fields. Inductive WPT systems need ferrite blocks for magnetic flux guidance and shielding, making these systems heavy, bulky, expensive and difficult to embed in roadway. Furthermore, losses in ferrites increase exponentially with operating frequency, limiting the potential for the WPT system's size reduction. On the other hand, capacitive WPT systems, which utilize relatively directed electric fields for power transfer, do not need dielectric material for flux guidance. Therefore, they can be operated at high frequencies, reducing their size, weight and cost. Furthermore, compared to their inductive counterparts, capacitive WPT systems generate substantially lower eddy-current-induced heating and losses in surrounding metallic structures, and have higher tolerance to coupling variations. This thesis introduces the topology and associated design and control techniques for MHz-frequency high-power-transfer-density capacitive WPT systems that can efficiently transfer kW-level power across large air-gap, and can also maintain its power transfer over a wide range of misalignments and air-gap variations.

Chapter 2 of this thesis develops a new design approach to mitigate the effect of parasitic capacitances in the charging environment of large air-gap capacitive WPT systems (now also published in [99] and [100]). These parasitic capacitances can be comparable to the coupling capacitance and can severely degrade power transfer and efficiency. The proposed approach addresses the challenge by employing split-inductor matching networks, which allow the complex network of parasitic capacitances to be simplified into an equivalent four-capacitance model. The shunt capacitances of this model are directly utilized as the matching network capacitors, hence, absorbing the parasitic capacitances and utilizing them in the power transfer mechanism. This also eliminates the need for discrete high-voltage capacitors, enhancing the efficiency and reliability of the system. A systematic procedure is developed to accurately measure the equivalent capacitances of the model, enabling the system's performance to be reliably predicted. The proposed approach is used to design two 6.78-MHz 12-cm air-gap prototype capacitive WPT systems with capacitor-free matching networks. The first system transfers up to 590 W using 150 cm^2 square coupling plates, and achieves an efficiency of 88.4%. The second prototype system transfers up to 1217 W using 118 cm^2 circular coupling plates, achieving a power transfer density of 51.6 kW/m^2. The measured output power profiles of the two systems match well with their predicted counterparts, validating the proposed design approach.

Chapter 3 of this thesis an analytical optimization approach for the design of multistage L-section matching networks in capacitive WPT systems, which maximizes the network efficiency while achieving the required overall gain and compensation (now also published in [101], and under review in [102]). The proposed approach identifies the optimal number of matching network stages, and the optimal distribution of gains and compensations among these stages. Compared to the conventional approach to designing matching networks for capacitive WPT systems, the proposed approach results in a higher and flatter efficiency for a wide range of air-gap voltages. The proposed approach also offers a better trade-off between efficiency and power transfer density, while meeting electric field safety requirements. The efficiency predictions of the proposed design approach are experimentally validated using three 6.78-MHz, 100-W prototype capacitive WPT systems, one with single-stage matching networks, one with two-stage matching networks, and another with three-stage matching networks. The measured matching network efficiencies of the prototype systems are in close agreement with the theoretical predictions. The prototype system with two-stage matching networks is also compared with a prototype system designed using the conventional approach, and is shown to achieve significantly higher efficiency.

Chapter 4 of this thesis addresses the challenges related to misalignments and air-gap variation in a dynamic charging scenario by introducing the active variable reactance (AVR) rectifier – a new approach to continuously compensate for coupling variations in WPT systems (now also published in [103] and [104]). The AVR rectifier operates at a fixed frequency and incorporates a power-splitting resonant network. By controlling the ratio of the split powers in its branches, the AVR rectifier continuously compensates for large misalignments and distance variations between couplers, while maintaining full power transfer. A comprehensive methodology is presented that maximizes the tolerable range of misalignments in an AVR-rectifier-enabled capacitive WPT system while meeting efficiency targets. The proposed approach is validated using a 13.56-MHz, 300-W, 12-cm nominal air-gap prototype capacitive WPT system, which incorporates an AVR rectifier and can be scaled up in power for dynamic electric vehicle (EV) charging applications. The prototype system maintains full power transfer for up to 45% lateral misalignment in the coupler and up to 45% increase in the vehicle's road clearance. In a dynamic EV charging scenario, the AVR-rectifier-enabled system transfers 80% more energy during a single pass of the vehicle over the charging pad, as compared to a system without the AVR rectifier. The measured performance of the prototype system is in good agreement with the predictions.

Chapter 5 of this thesis develops a closed-loop control strategy to dynamically compensate for coupling variations in capacitive WPT systems utilizing the AVR rectifier (now also published in [105]). The proposed control approach utilizes a decoupled-dual-loop strategy to regulate the power in the two branches of the AVR rectifier. This approach enables dynamic reactive compensation and output power recovery under varying coupling conditions without having to sense any high-frequency voltage or current. A comprehensive small-signal model of the AVR-rectifier-based capacitive WPT system is developed and the controller design method is discussed. A 6.78-MHz scaled capacitive WPT prototype, incorporating an AVR rectifier controlled using the proposed approach, is designed, built and tested. The proposed closed-loop control strategy enables the prototype system to maintain constant output power for large misalignments between the coupling pads.

Finally, Chapter 6 of this thesis presents a theoretical comparison between inductive and capacitive WPT systems and discusses their projected performances. The maximum power transfer capabilities of the two WPT systems are formulated while adhering to their physical limits, with the limit set by saturation of the magnetic core in inductive WPT systems, and by electric breakdown of air in capacitive WPT systems. The efficiency of inductive and capacitive WPT systems are formulated in terms of the system specifications, and the tradeoff between efficiency and power transfer density are compared. It has been shown that capacitive WPT systems are favored by a higher operating frequency, while inductive WPT systems are favored by a larger gap to area ratio. Introduction of multistage compensation networks are shown to increase the efficiency of both systems, with the improvement being significantly higher for capacitive WPT systems, resulting in a better tradeoff between efficiency and power transfer density.

7.2. Recommendations for Future Work

There are numerous opportunities to build on the work presented in this thesis, three of which are identified below.

First, the capacitive couplers used in the prototype systems presented in this thesis are constructed simply using two pairs of copper plates. However, in a real dynamic charging scenario, these plates must be packaged in a way that enables them to be embedded in the roadway for EV charging systems, or in the floor of a warehouse/factory for material handling applications. This packaging is desired to have a low profile while also being structurally rigid, so that they can easily be embedded but do not flex under the weight of vehicles. To avoid using discrete high-voltage capacitors in the system and thus enhance reliability, this packaging must also ensure that the resulting capacitance between the pair of plates is equal to the required matching network capacitance. A particular challenge will be to optimally design the coupler to achieve a favorable trade-off between its size, the system efficiency, and cost.

Second, this thesis proposes a way to maintain a constant power transfer when the charging pads are misaligned, which is an enabling technology for dynamic EV charging. Future work may involve detecting a moving vehicle, intelligently decide when to turn on the charging system, and at which rate the power transfer should be increased so as to spend maximum possible time at the nominal power level. Another potential research area is the detailed estimation of infrastructural and maintenance cost of an AVR-rectifier-based dynamic EV charging system.

Third, the predictions made in this thesis regarding the relative performances of inductive and capacitive WPT systems, as well as recommended ways to improve their performances, need to be experimentally validated. A potential approach to perform such experiments will be to build inductive and capacitive WPT systems for a specific coupling area and air-gap, and observe how power transfer and efficiency changes with varying operating frequency and number of matching network stages.

It is hoped that this thesis will motivate the exploration of these exciting research opportunities.

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APPENDIX A

EXPRESSIONS FOR EQUIVALENT CAPACITANCES IN THE FOUR-CAPACITANCE MODEL

This appendix derives the transformation of the six-capacitance model of the EV charging environment given by Fig. 2.11(d) into the four-capacitance model shown in Fig. 2.11(e), and henceforth, the expressions for the equivalent series and shunt capacitances of the four-capacitance model given by (2.1)-(2.3). The equivalent model of the EV charging environment of Fig. 2.11(d) is reproduced in Fig. A.1, with the four circuit terminals marked as A, B, C, and D, and their voltages with respect to the inverter ground as v_A, v_B, v_C, and v_D, respectively. The currents flowing into terminal A, terminal B, terminal C, and terminal D are denoted as i_A, i_B, i_C, and i_D, respectively. Using KCL at node A′, the current i_A can be expressed as:

$$i_A = (v_A - v_B) j\omega_s \left(C_{pp,r} + \frac{C_{pr}}{2} + \frac{C_{pv'}}{2}\right) + (v_A - v_C) j\omega_s C_s + (v_A - v_D) j\omega_s C_d. \tag{A.1}$$

Similarly, using KCL at node B′, the current i_B can also be expressed as:

$$i_B = (v_B - v_A) j\omega_s \left(C_{pp,r} + \frac{C_{pr}}{2} + \frac{C_{pv'}}{2}\right) + (v_B - v_D) j\omega_s C_s + (v_B - v_C) j\omega_s C_d. \tag{A.2}$$

Since terminal A and terminal B form the input port of this two-port network, the current entering terminal A must be equal to that leaving terminal B, i.e.,

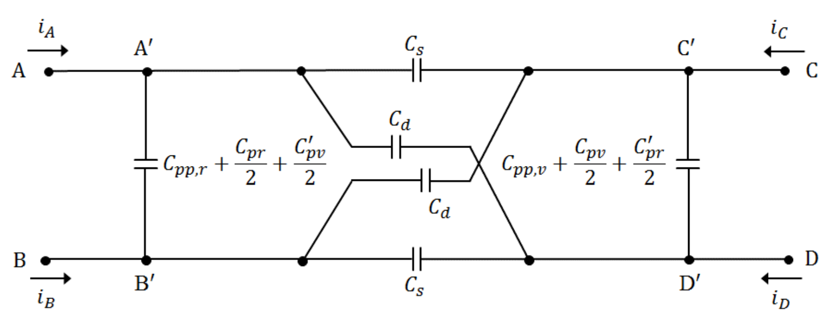

Fig. A.1: Two-port six-capacitance model of the EV charging environment as represented in Fig. 2.11(d).

$$i_A = -i_B. \tag{A.3}$$

Substitution of the expressions for i_A and i_B given in (A.1) and (A.2) into (A.3) yields:

$$(v_A + v_B - v_C - v_D)j\omega_s(C_s - C_d) = 0. \tag{A.4}$$

Since the angular switching frequency ω_s is non-zero, and in any capacitive WPT system the diagonal capacitance C_d is smaller than the series capacitance C_s, it can be concluded from (A.4) that,

$$v_A + v_B = v_C + v_D. \tag{A.5}$$

Using (A.1) and (A.5), the current i_A flowing into terminal A can be expressed as:

$$i_A = (v_A - v_B)j\omega_S\left(C_{pp,r} + \frac{C_{pr}}{2} + \frac{C_{pv}{}'}{2} + C_d\right) + (v_A - v_C)j\omega_s(C_s - C_d)$$

$$= (v_A - v_B)j\omega_S C_{p1,eqv} + (v_A - v_C)j\omega_s C_{s,eqv}. \tag{A.6}$$

Here, $C_{p1,eqv}$ is equal to $\left(C_{pp,r} + \frac{C_{pr}}{2} + \frac{C_{pv}{}'}{2} + C_d\right)$, and $C_{s,eqv}$ is equal to $(C_s - C_d)$. It can be seen from (A.6) that the current i_A flowing into terminal A is the sum of the current flowing from node A$'$ to node B$'$ through an equivalent capacitance $C_{p1,eqv}$ and another current flowing from node A$'$ to node C$'$ through an equivalent capacitance $C_{s,eqv}$. Similarly, using (A.2) and (A.5), the current i_B flowing into terminal B can be expressed as:

$$i_B = (v_B - v_A)j\omega_S C_{p1,eqv} + (v_B - v_D)j\omega_s C_{s,eqv}. \tag{A.7}$$

Therefore, the current i_B flowing into terminal B is the sum of the current flowing from node B$'$ to node A$'$ through an equivalent capacitance $C_{p1,eqv}$ and another current flowing from node B$'$ to node D$'$ through an equivalent capacitance $C_{s,eqv}$. The currents i_C and i_D flowing into terminals C and D, respectively, can similarly be expressed as:

$$i_C = (v_C - v_D)j\omega_S\left(C_{pp,v} + \frac{C_{pv}}{2} + \frac{C_{pr}{}'}{2} + C_d\right) + (v_C - v_A)j\omega_s(C_s - C_d)$$

$$= (v_C - v_D)j\omega_S C_{p2,eqv} + (v_C - v_A)j\omega_s C_{s,eqv}, \tag{A.8}$$

and

$$i_D = (v_D - v_C)j\omega_s C_{p2,eqv} + (v_D - v_B)j\omega_s C_{s,eqv}. \tag{A.9}$$

Following similar logic as that for i_A and i_B, i_C and i_D can be thought of as the sum of two currents: one flowing through the capacitance $C_{p2,eqv}$, and another flowing through a capacitance $C_{s,eqv}$. Using (A.6)-(A.9), the two-port network can be represented as shown in Fig. A.2, with a shunt capacitance $C_{p1,eqv}$ across the input port A-B, a shunt capacitance $C_{p2,eqv}$ across the output port C-D, and two series capacitances, each of value $C_{s,eqv}$ connected between each of the terminals of the input and the output port. This is the same four-capacitance model of the EV charging environment as presented in Fig.

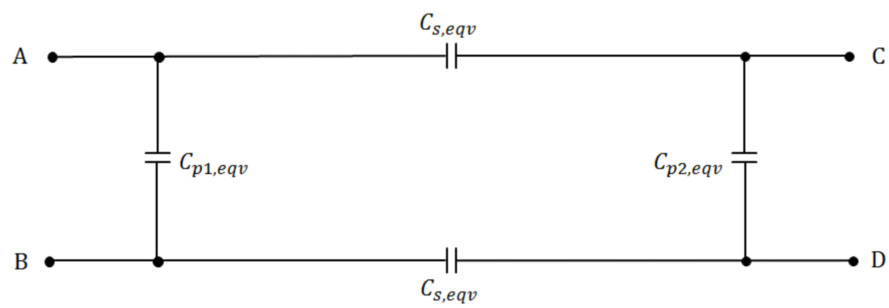

Fig. A.2: Two-port four-capacitance model of the EV charging environment as represented in Fig. 2.11(e).

2.11(e), with the expressions for the equivalent shunt and series capacitances of the model as given by (2.1)-(2.3).

APPENDIX B

VALIDITY OF COUPLER MODEL UNDER MISALIGNED CONDITION

This appendix discusses the validity of the modeling methodology shown in Fig. 2.11 when the vehicle-side plates are misaligned from the roadway-side plates. Figure B.1 shows the circuit schematic of a capacitive WPT system incorporating all the existing parasitic capacitances. The modeling methodology illustrated in Fig. 2.11 remains valid as long as the system is symmetrical with respect to the line passing through the roadway and the vehicle chassis (node R and node V), as shown in Fig. B.1. In the fully aligned condition, this symmetry is maintained provided the two roadway-side plates are equal in area and equidistant from the roadway, and the two vehicle-side plates are equal in area and equidistant from the vehicle chassis. These requirements are reasonable easy to achieve.

The vehicle-side plates can be misaligned with respect to the roadway-side plates along two directions, as shown in Fig. B.2. In both these cases, the shunt capacitances of the matching networks remain practically unchanged, since these are dominated by the capacitances between the roadway-side plates and the roadway (C_{pr}), or the vehicle-side plates and the vehicle chassis (C_{pv}), which are much larger than the other parasitic capacitances in Fig. 2.11. However, both the series capacitance C_s and the diagonal capacitance C_d in Fig. 2.11 can change substantially with misalignment.

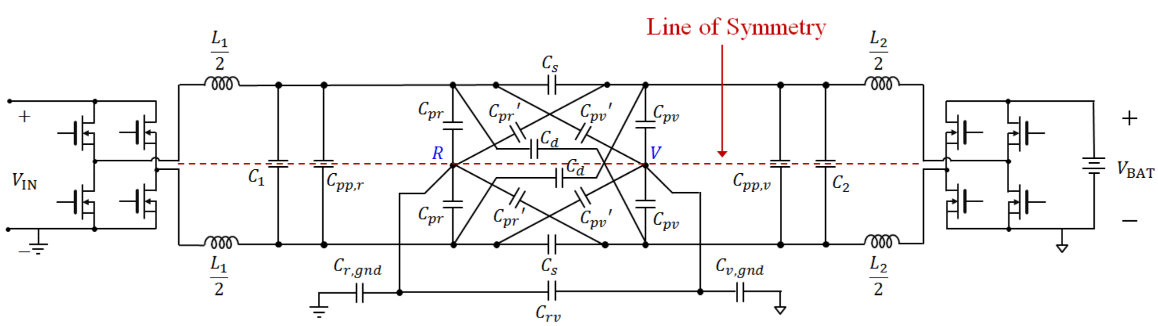

Fig. B.1: Circuit schematic of a capacitive WPT system for EV charging incorporating split-inductor matching networks and the parasitics present in the EV charging environment.

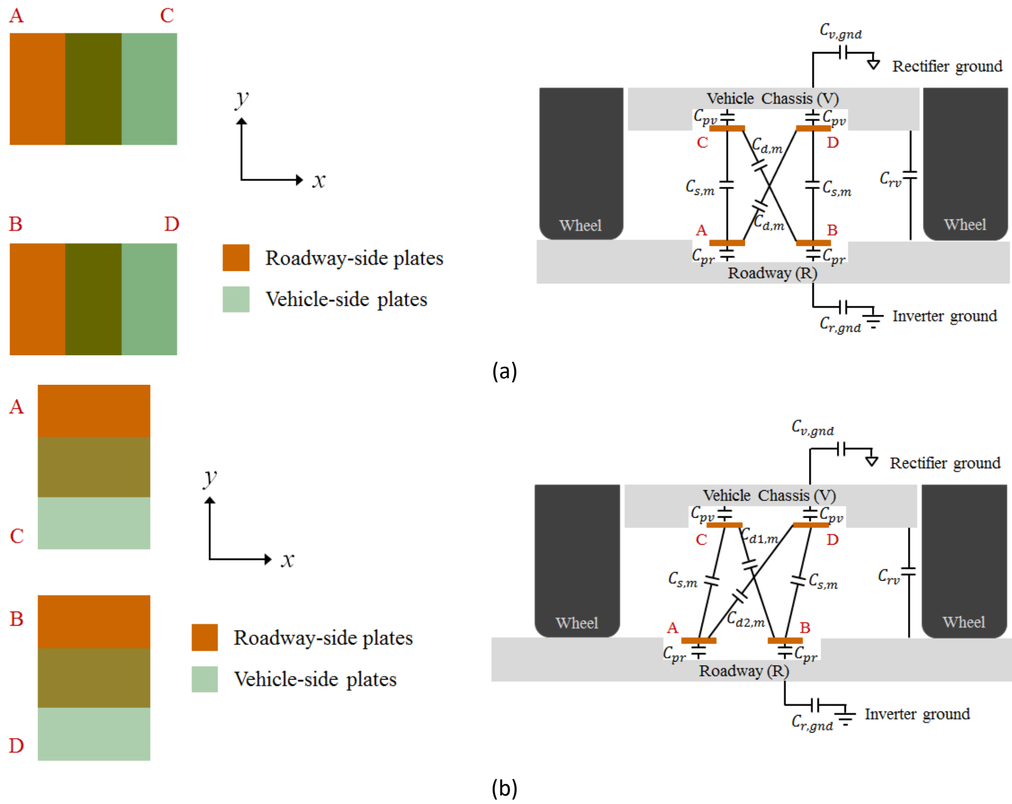

Fig. B.2: Misalignments between the roadway-side and vehicle-side coupling plates in a capacitive WPT system for EV charging and the corresponding effects on the series capacitances (C_s) and the diagonal capacitances (C_d): (a) misalignment along x-axis, (b) misalignment along y-axis.

When the misalignment is along the x-axis (see Fig. B.2(a)), the modified value of the two series capacitances (shown as $C_{s,m}$) are still equal to each other, and so are the modified values of the diagonal capacitances $C_{d,m}$. Therefore, the symmetry in the system is maintained, and the modeling methodology of Fig. 2.11 remains valid. When the misalignment is along the y-axis, as shown in Fig. B.2(b), the modified values of C_s remain equal, but the modified values of the diagonal capacitances are different (shown as $C_{d1,m}$ and $C_{d2,m}$). As the symmetry is not fully maintained, the currents through the parasitic ground capacitances $C_{r,gnd}$ and $C_{v,gnd}$ in Fig. B.1 no longer remain zero, and the modeling methodology of Fig. 2.11 is not strictly valid. However, an "approximate" model can still be applied while maintaining reasonable accuracy. To do so, we first ignore the parasitic ground currents and model the circuit as before using Fig. 2.11(d), but with unequal diagonal capacitances. The corresponding series equivalent capacitance of Fig. 2.11(e) can be expressed by following the method shown in Appendix A as:

$$C_{s,eqv,m} = 2\frac{C_{s,m}^2 - C_{d1,m}C_{d2,m}}{2C_{s,m} + C_{d1,m} + C_{d2,m}}. \quad \text{(B.1)}$$

Note that the expression of $C_{s,eqv,m}$ in (B.1) reduces to that of $C_{s,eqv}$ in (3) when the diagonal capacitances are equal (i.e., $C_{d1} = C_{d2} = C_d$). Next, the output power of the full system (Fig. B.1) is compared to the approximate model. Such a comparison is shown in Fig. B.3 for an example 6.78-MHz 1-kW capacitive WPT system under misalignments along the y-axis using LTspice simulations. As can be seen, the output power of the full system deviates from the approximate model's output power by less than 12% for up to 50% misalignment. In a practical scenario, y-axis misalignments during stationary or dynamic charging are likely to remain within 50%, particularly with sufficiently large roadway-side pads. Hence, the proposed modeling methodology can still be applied with fairly accurate results.

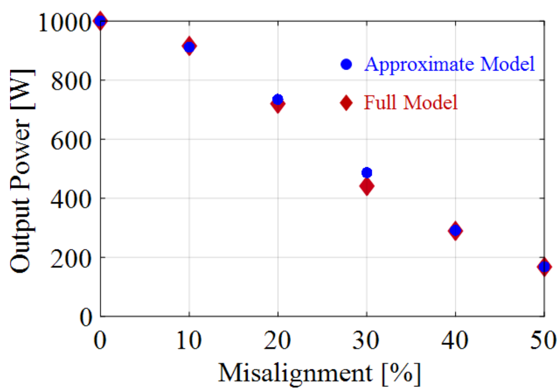

Fig. B.3: Comparison of simulated output powers of the capacitive WPT system under misalignment along y-axis using the full model and the approximate model.

APPENDIX C

EXPRESSIONS FOR DEVIATION IN OUTPUT POWER DUE TO ERROR IN CAPACITANCE MEASUREMENT

This appendix derives the expression for the deviation in output power due to errors in the equivalent shunt capacitance $C_{p1,eqv}$, as given by (2.4). At the nominal condition (with no error in capacitance values), the matching networks fully compensate for the coupling reactance, and hence, the impedance seen by the inverter is purely resistive, shown as R_{inv} in Fig. C.1. Under the assumption that the capacitive WPT system is highly efficient (i.e., input power is equal to output power), the nominal output power can therefore be expressed as:

$$P_{\mathrm{OUT}} = \frac{8}{\pi^2}\frac{V_{\mathrm{IN}}^2}{R_{inv}}. \tag{C.1}$$

Under this nominal condition, the roadway-side matching network is loaded by a capacitive impedance, shown as $R - jX$ in Fig. C.1. When the matching networks are optimally designed using the methodology presented in Chapter 3, this impedance can be expressed as:

$$R - jX = \frac{2}{\omega_s C_{s,eqv}}\left(\frac{V_{\mathrm{IN}}V_{\mathrm{OUT}}}{V_{\mathrm{IN}}^2+V_{\mathrm{OUT}}^2} - j\frac{V_{\mathrm{IN}}^2}{V_{\mathrm{IN}}^2+V_{\mathrm{OUT}}^2}\right). \tag{C.2}$$

The resistance seen by the inverter can now be expressed as:

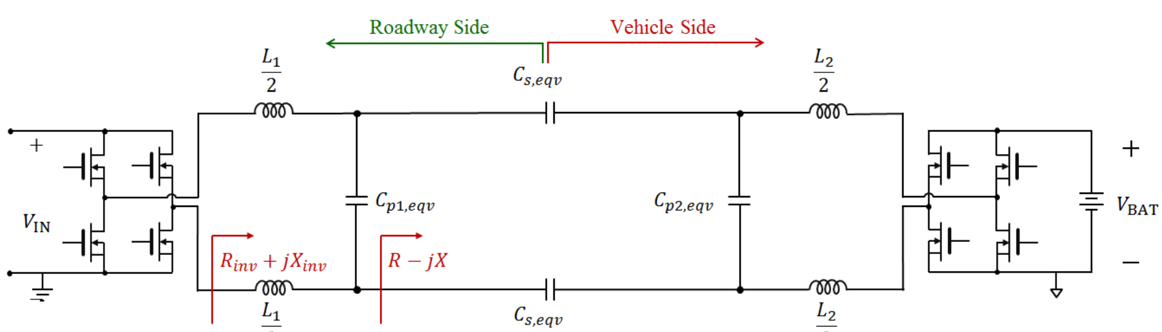

Fig. C.1: The capacitive WPT system of Fig. 13 with the impedance seen by the inverter indicated as ($R_{inv} + jX_{inv}$), and the load impedance of the roadway-side matching network indicated as ($R - jX$).

$$R_{inv} = Real\left((R - jX)\,||\left(\frac{1}{j\omega_s C_{p1,eqv}}\right) + j\omega_s L_1\right)$$

$$= Real\left((R - jX)\,||\left(\frac{1}{j\omega_s C_{p1,eqv}}\right)\right). \tag{C.3}$$

In a capacitive WPT system for EV charging, the air-gap is much larger than the distance between the roadway-side plates and the roadway. Therefore, the value of the equivalent series capacitance $C_{s,eqv}$ is much smaller than that of the shunt capacitances $C_{p1,eqv}$. Neglecting the value of $C_{s,eqv}$ compared to the value of $C_{p1,eqv}$ in (C.3), the resistance seen by the inverter can be approximated by:

$$R_{inv} \approx \frac{R}{\omega_s^2 C_{p1,eqv}^2}\left(\frac{1}{R^2+X^2}\right). \tag{C.4}$$

When there is an error in the value of this capacitance ($\Delta C_{p1,eqv}$), the impedance seen by the inverter no longer remains purely resistive. Utilizing (C.4), the resistive and reactive parts of this new impedance seen by the inverter, $R_{inv,new} + jX_{inv,new}$, can be expressed as:

$$R_{inv,new} = \frac{R}{\omega_s^2\left(C_{p1,eqv}+\Delta C_{p1,eqv}\right)^2}\left(\frac{1}{R^2+X^2}\right) = \frac{R_{inv}}{1+\left(\frac{\Delta C_{p1,eqv}}{C_{p1,eqv}}\right)^2}. \tag{C.5}$$

and,

$$X_{inv,new} = \omega_s L_1 - \frac{\left(X+\omega_s\left(C_{p1,eqv}+\Delta C_{p1,eqv}\right)\left(R^2+X^2\right)\right)}{\omega_s^2\left(C_{p1,eqv}+\Delta C_{p1,eqv}\right)^2}\left(\frac{1}{R^2+X^2}\right). \tag{C.6}$$

The inductance L_1 of the roadway-side matching network can be obtained by using the fact that the reactance seen by the inverter is zero under nominal condition, and can be expressed as:

$$L_1 = \frac{\left(X+\omega_s C_{p1,eqv}\left(R^2+X^2\right)\right)}{\omega_s^3 C_{p1,eqv}^2}\left(\frac{1}{R^2+X^2}\right). \tag{C.7}$$

Substituting the expressions for R and X from (C.2) and the expression for L_1 from (C.7) into (C.6), and using the assumption that $C_{s,eqv}$ is much smaller than $C_{p1,eqv}$, $X_{inv,new}$ can be approximated as:

$$X_{inv,new} \approx \frac{1}{\omega_s C_{p1,eqv}} \left(\frac{\Delta C_{p1,eqv}}{C_{p1,eqv}} \right). \tag{C.8}$$

The new output power can now be expressed using this new inverter impedance as:

$$P_{\mathrm{OUT,new}} = P_{\mathrm{OUT}} + \Delta P_{\mathrm{OUT}} = \frac{8}{\pi^2} V_{\mathrm{IN}}^2 \left(\frac{R_{inv,new}}{R_{inv,new}^2 + X_{inv,new}^2} \right), \tag{C.9}$$

where ΔP_{OUT} is the resultant deviation in output power. First substituting the expression for R_{inv} derived from (C.1) into (C.5), and then further substituting the resultant expression for $R_{inv,new}$ from (C.5) and the expression for $X_{inv,new}$ from (C.8) into (C.9), the new output power can be expressed as:

$$P_{\mathrm{OUT,new}} = P_{\mathrm{OUT}} + \Delta P_{\mathrm{OUT}} = P_{\mathrm{OUT}} \left(1 - \frac{1}{\left(1 + \frac{V_{\mathrm{IN}} V_{\mathrm{OUT}} \omega_s C_{s,eqv}}{2 P_{\mathrm{OUT}} \left(\frac{\Delta C_{p1,eqv}}{C_{p1,eqv}} \right)^2} \right)} \right). \tag{C.10}$$

Rearranging (C.10), the relative change in output power can be expressed as:

$$\frac{\Delta P_{\mathrm{OUT}}}{P_{\mathrm{OUT}}} = - \frac{1}{\left(1 + \frac{V_{\mathrm{IN}} V_{\mathrm{OUT}} \omega_s C_{s,eqv}}{2 P_{\mathrm{OUT}} \left(\frac{\Delta C_{p1,eqv}}{C_{p1,eqv}} \right)^2} \right)}, \tag{C.11}$$

which is the same as (2.4).

APPENDIX D

EXPRESSIONS FOR ERRORS IN CALCULATED VALUES OF EQUIVALENT CAPACITANCES

This appendix derives the expressions for the errors in the calculated values of the equivalent capacitances $C_{p1,eqv}$, $C_{p2,eqv}$, and $C_{s,eqv}$ resulting from errors in measuring the input capacitances (C_{in}), for the twenty test combinations mentioned in Section 2.3 of Chapter 2. As an example, consider the test combination (D, E, F). By solving the three equations resulting from the expressions for $C_{in,D}$, $C_{in,E}$, and $C_{in,F}$ (see Fig. 2.14), the equivalent capacitances $C_{s,eqv}$, $C_{p1,eqv}$, and $C_{p2,eqv}$ can be expressed in terms of these input capacitances as:

$$C_{s,eqv} = \frac{1}{2}\left(-C_{in,E} + C_{in,F}\right), \tag{D.1a}$$

$$C_{p1,eqv} = \frac{1}{4}\left(-4C_{in,D} + 3C_{in,E} + C_{in,F}\right), \tag{D.1b}$$

and

$$C_{p2,eqv} = \frac{1}{4}\left(4C_{in,D} + C_{in,E} - C_{in,F}\right). \tag{D.1c}$$

Using (D.1a), the error in $C_{s,eqv}$ can be expressed as:

$$\Delta C_{s,eqv} = \frac{1}{2}(-\Delta C_{in,E} + \Delta C_{in,F}). \tag{D.2}$$

It can be seen from (D.2) that $\Delta C_{s,eqv}$ will be maximum when $\Delta C_{in,E}$ is positive and $\Delta C_{in,F}$ is negative, or vice versa. The magnitude of the maximum possible error in $C_{s,eqv}$ is thus given by:

$$|\Delta C_{s,eqv}| = \frac{1}{2}(\left|\Delta C_{in,E}\right| + |\Delta C_{in,F}|). \tag{D.3}$$

Dividing both sides of (D.3) by $C_{s,eqv}$,

$$\left|\frac{\Delta C_{s,eqv}}{C_{s,eqv}}\right| = \frac{1}{2}\left(\left|\frac{\Delta C_{in,E}}{C_{s,eqv}}\right| + \left|\frac{\Delta C_{in,F}}{C_{s,eqv}}\right|\right)$$

$$= \frac{1}{2}\left(\left|\frac{\Delta C_{in,E}}{C_{in,E}}\right|\left(\frac{C_{in,E}}{C_{s,eqv}}\right) + \left|\frac{\Delta C_{in,F}}{C_{in,F}}\right|\left(\frac{C_{in,F}}{C_{s,eqv}}\right)\right). \quad \text{(D.4)}$$

Using the expressions for $C_{in,E}$, and $C_{in,F}$ given in Fig. 2.15, and assuming that the value of the series capacitance $C_{s,eqv}$ is much smaller than those of the shunt capacitances $C_{p1,eqv}$ and $C_{p2,eqv}$ (as is typically the case for large air-gap capacitive WPT systems), the relative error in $C_{s,,eqv}$ given by (D.4) can be approximated as:

$$\left|\frac{\Delta C_{s,eqv}}{C_{s,eqv}}\right| = \frac{1}{2}\left(\left|\frac{\Delta C_{in,E}}{C_{in,E}}\right|\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right) + \left|\frac{\Delta C_{in,F}}{C_{in,F}}\right|\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\right). \quad \text{(D.5)}$$

The relationship among the errors in measuring the input capacitances $C_{in,D}$, $C_{in,E}$, and $C_{in,F}$ can be understood by analyzing their measurement method described in Section IV, where the capacitance is resonated with a known inductance L, and the resonant frequency f_0 is identified by exciting the setup with a variable frequency source. The expression for C_{in} is given in (2.11), and is reproduced here as:

$$C_{in,i} = \frac{1}{4\pi^2 f_0^2 L}, \quad \text{(D.6)}$$

The accuracy in measuring the resonant frequency Δf_0 depends on the frequency resolution of the variable frequency source. The error in the input capacitance (ΔC_{in}) due to the error in the resonant frequency (Δf_0) can be expressed as:

$$\frac{\Delta C_{in}}{\Delta f_0} \approx \frac{d(C_{in})}{d(f_0)} = -\frac{2}{4\pi^2 f_0^3 L} = -2\,\frac{C_{in}}{f_0}, \quad \text{(D.7)}$$

Rearranging (D.7) yields:

$$\left|\frac{\Delta C_{in}}{C_{in}}\right| = 2\left|\frac{\Delta f_0}{f_0}\right|. \quad \text{(D.8)}$$

Therefore, the relative error in C_{in} is twice the relative error in the resonant frequency of the setup. The measured input capacitances in the tests shown in Fig. 2.14 have magnitudes comparable to one another. Hence, with the same inductance L, the resonant frequency f_0 will be of similar magnitude for all these tests. The error Δf_0 due to the frequency resolution of the source is also likely to be very similar for such close values of frequencies. Therefore, to simplify the analysis, it can be assumed that the relative error in the resonant frequency, and hence, the relative error in the measured input capacitance are the same for all the tests of Fig. 2.14, i.e.,

$$\left|\frac{\Delta C_{in,A}}{C_{in,A}}\right| = \left|\frac{\Delta C_{in,B}}{C_{in,B}}\right| = \left|\frac{\Delta C_{in,C}}{C_{in,C}}\right| = \left|\frac{\Delta C_{in,D}}{C_{in,D}}\right| = \left|\frac{\Delta C_{in,E}}{C_{in,E}}\right| = \left|\frac{\Delta C_{in,F}}{C_{in,F}}\right| = \left|\frac{\Delta C_{in}}{C_{in}}\right|. \tag{D.9}$$

Substituting the expressions for $\left|\frac{\Delta C_{in,E}}{C_{in,E}}\right|$ and $\left|\frac{\Delta C_{in,F}}{C_{in,F}}\right|$ from (D.9) into (D.4), the relative error in $C_{s,eqv}$ can be expressed as:

$$\left|\frac{\Delta C_{s,eqv}}{C_{s,eqv}}\right| = \left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left|\frac{\Delta C_{in}}{C_{in}}\right|. \tag{D.10}$$

The relative errors in the other equivalent capacitances $C_{p1,eqv}$ and $C_{p2,eqv}$ can be determined in a similar manner. Table D.1 shows the expressions for the relative errors in the three equivalent capacitances $C_{p1,eqv}$, $C_{p2,eqv}$ and $C_{s,eqv}$ for the twenty possible test combinations discussed in Section 2.3.

TABLE D.1: RELATIVE ERRORS IN THE CALCULATED VALUES OF THE EQUIVALENT CAPACITANCES OF THE FOUR-CAPACITANCE MODEL OF FIG. 13 FOR ALL POSSIBLE TWENTY TEST COMBINATIONS MENTIONED IN SECTION IV

Test Combination	$\left\lvert\frac{\Delta C_{p1,eqv}}{C_{p1,eqv}}\right\rvert$	$\left\lvert\frac{\Delta C_{p2,eqv}}{C_{p2,eqv}}\right\rvert$	$\left\lvert\frac{\Delta C_{s,eqv}}{C_{s,eqv}}\right\rvert$
A B C	$2\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p1,eqv}}{C_{s,eqv}}\right)\sqrt{2\frac{C_{p2,eqv}}{C_{s,eqv}}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A B D	$2\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p2,eqv}}{C_{s,eqv}}\right)\sqrt{2\frac{C_{p1,eqv}}{C_{s,eqv}}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A B E	$\left(1+\frac{C_{p2,eqv}}{C_{p1,eqv}}+\frac{1}{2}\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(1+\frac{5}{2}\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A B F	$\left(2+\frac{3}{2}\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$3\left(1+\frac{1}{2}\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A C D	$2\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p1,eqv}}{C_{s,eqv}}\right)\sqrt{2\frac{C_{p2,eqv}}{C_{s,eqv}}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A C E	$2\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$4\frac{C_{p1,eqv}C_{p2,eqv}}{C_{s,eqv}^2}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A C F	$2\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$6\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$4\frac{C_{p1,eqv}C_{p2,eqv}}{C_{s,eqv}^2}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A D E	$2\left(1+\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(1+\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{\left(C_{p1,eqv}+2C_{p2,eqv}\right)}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A D F	$2\left(2+3\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$4\left(2+\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{\left(C_{p1,eqv}+2C_{p2,eqv}\right)}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
A E F	$\left(2+\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(1+2\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
B C D	$2\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p2,eqv}}{C_{s,eqv}}\right)\sqrt{2\frac{C_{p1,eqv}}{C_{s,eqv}}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
B C E	$\left(1+\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(1+\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{\left(2C_{p1,eqv}+C_{p2,eqv}\right)}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
B C F	$\left(3+\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(2+3\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{\left(2C_{p1,eqv}+C_{p2,eqv}\right)}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
B D E	$2\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$4\frac{C_{p1,eqv}C_{p2,eqv}}{C_{s,eqv}^2}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
B D F	$6\frac{C_{p2,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\frac{C_{p1,eqv}}{C_{s,eqv}}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$4\frac{C_{p1,eqv}C_{p2,eqv}}{C_{s,eqv}^2}\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
B E F	$\left(1+2\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(2+\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
C D E	$\left(1+\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(1+\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
C D F	$\left(2+\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(2+\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$2\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
C E F	$\frac{1}{2}\left(3+\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(1+2\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$
D E F	$\left(1+2\frac{C_{p2,eqv}}{C_{p1,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\frac{1}{2}\left(3+\frac{C_{p1,eqv}}{C_{p2,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$	$\left(\frac{C_{p1,eqv}+C_{p2,eqv}}{C_{s,eqv}}\right)\left\lvert\frac{\Delta C_{in}}{C_{in}}\right\rvert$

APPENDIX E

EXPRESSIONS FOR CONSTRAINTS ON THE DESIGN OF CAPACITIVE WPT SYSTEM AND THE SYSTEM FACTOR

This appendix derives the expressions for the constraints on the design of the capacitive WPT system of Fig. 3.6 as given by (3.6b)-(3.6e), as well as the expression for the system factor K_{sys} as given by (3.7). Figure E.1 shows the schematic of the full-bridge inverter of the capacitive WPT system of Fig. 3.6, operating during the state when the transistors Q_1 and Q_4 are on and the transistors Q_2 and Q_3 are off. The total charge stored in the output capacitance $C_{oss,inv}$ of Q_2 and Q_3 is given by:

$$q_s = 2C_{oss,inv}V_{\mathrm{IN}}. \tag{E.1}$$

This charge needs to be removed by the inverter output current in order to achieve ZVS of transistors Q_2 and Q_3. Figure E.2 shows typical waveforms for the inverter output voltage and output current. The inverter output current ($i_{out,inv}$) lags the inverter output voltage ($v_{out,inv}$) by an angle ϕ_{inv}. After the transistors Q_1 and Q_4 are turned off at time $\frac{T_s}{2}$, the inverter output current can discharge the output capacitances of Q_2 and Q_3 until time t_1 when the current reaches zero. Therefore, the charge removed by the inverter output current from the output capacitances of the transistors Q_2 and Q_3 is equal to the

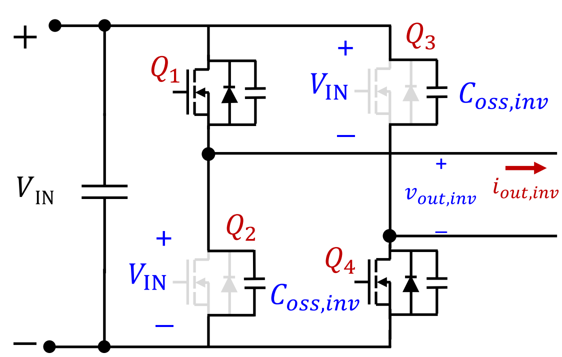

Fig. E.1: Schematic of the full-bridge inverter in the capacitive WPT system of Fig. 3 during the positive half of the switching cycle.

area under the waveform $i_{out,inv}$ from time $\frac{T_s}{2}$ to time $t_1(=\frac{T_s}{2}+\frac{\phi_{inv}}{2\pi f_s})$. This removed charge can therefore be expressed as:

$$q_r = \int_{\frac{T_s}{2}}^{t_1} I_{pk}\sin(2\pi f_s t - \phi_{inv})dt = \frac{I_{pk}}{2\pi f_s}(1-\cos\phi_{inv}), \tag{E.2}$$

where I_{pk} is the peak of the inverter output current. This peak current can be related to the input voltage V_{IN}, the output power P_{OUT} and the phase-lag ϕ_{inv} as:

$$I_{pk} = \frac{2P_{\mathrm{OUT}}}{k_{inv}V_{\mathrm{IN}}\cos\phi_{inv}}. \tag{E.3}$$

Substituting this expression for I_{pk} in (E.3) gives the following expression for the charge removed by the inverter output current:

$$q_r = \frac{P_{\mathrm{OUT}}}{\pi f_s k_{inv} V_{\mathrm{IN}}}\frac{(1-\cos\phi_{inv})}{\cos\phi_{inv}}. \tag{E.4}$$

To achieve ZVS with minimum circulating current, the removed charge given by (E.4) must equal the charge stored in the output capacitances of Q_2 and Q_3, q_s, as given by (E.1). Equating these two expressions, the required inverter phase-lag can be obtained as:

$$\phi_{inv} = \cos^{-1}\frac{1}{1+\frac{2\pi k_{inv}V_{\mathrm{IN}}^2 f_s C_{oss,inv}}{P_{\mathrm{OUT}}}}. \tag{E.5}$$

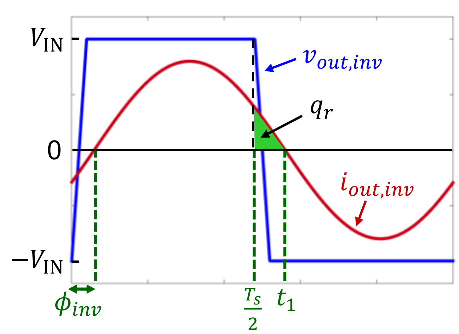

Fig. E.2: Waveforms of the inverter switch-node voltage and the inverter output current indicating the charge available from the inverter output current to enable ZVS of the inverter transistors.

By symmetry, the same inverter phase-lag will achieve ZVS for transistors Q_1 and Q_4. Using (25), and noting that the inverter output voltage and output current are same as the input voltage and input current of the first primary-side stage, the input impedance characteristic of the first primary-side stage can be expressed as:

$$Q_{in,pri,1} = \frac{X_{in,pri,1}}{R_{in,pri,1}} = \frac{|Z_{in,pri,1}| \sin \phi_{inv}}{|Z_{in,pri,1}| \cos \phi_{inv}} = \tan \phi_{inv} = \tan\left(\cos^{-1} \frac{1}{1+\frac{2\pi k_{inv} V_{\text{IN}}^2 f_S C_{oss,inv}}{P_{\text{OUT}}}}\right), \qquad \text{(E.6)}$$

which is the same as given in (3.6b). The expression in (3.6c) can be obtained in an identical manner by applying the condition for ZVS with minimal circulating current to the rectifier transistors.

The input current of the first stage of the primary-side network, i.e., the inverter output current, and the output current of the last stage of the secondary-side network, i.e., the rectifier input current, can be expressed, respectively, as:

$$\left|I_{in,pri,1}\right| = \frac{2P_{\text{OUT}}}{k_{inv} V_{\text{IN}} \cos \phi_{inv}}, \qquad \text{(E.7)}$$

and

$$\left|I_{out,sec,n}\right| = \frac{2P_{\text{OUT}}}{\sqrt{2k_{rec}} V_{\text{OUT}} \cos \phi_{rec}}. \qquad \text{(E.8)}$$

Using (E.7) and (E.8), the total current gain $G_{i,tot}$ can be expressed as:

$$G_{i,tot} = \frac{|I_{out,sec,n}|}{|I_{in,pri,1}|} = \frac{k_{inv} V_{\text{IN}}}{\sqrt{2k_{rec}} V_{\text{OUT}}} \frac{\cos \phi_{inv}}{\cos \phi_{rec}}. \qquad \text{(E.9)}$$

This expression for the total current gain $G_{i,tot}$ is the same as given by (3.6e).

The input impedance characteristic of the first secondary-side stage and the load impedance characteristic of the last (m-th) primary-side stage can be related as:

$$Q_{in,sec,1} - Q_{load,pri,m} = \frac{X_{in,sec,1}}{R_{in,sec,1}} - \frac{X_{load,pri,m}}{R_{load,pri,m}}.$$

$$= \frac{X_{in,sec,1} - X_{load,pri,m}}{R_{in,sec,1}} = \frac{2|X_p|}{R_{in,sec,1}}. \quad \text{(E.10)}$$

In deriving (E.10), we have used the fact that the load resistance of the last (m-th) primary-side stage is the same as the input resistance of the first secondary-side stage ($R_{load,pri,m} = R_{in,sec,1}$), and the input reactance of the first secondary-stage plus the total coupling reactance is equal to the load reactance of the last primary-side stage ($X_{in,sec,1} - 2|X_p| = X_{load,pri,m}$). Since the L-section stage highly efficient, the input power of the stage is approximately equal to its output power, and the input resistance of the stage, R_{in}, can be related to its current gain G_i as:

$$R_{in} = \frac{\mathrm{P_{OUT}}}{|\hat{I}_{in}|^2} = \frac{|\hat{I}_{out}|^2 R_{load}}{|\hat{I}_{in}|^2} = \left(\frac{|\hat{I}_{out}|}{|\hat{I}_{in}|}\right)^2 R_{load} = G_i^2 R_{load}. \quad \text{(E.11)}$$

Applying (E.11) to all the stages of the secondary-side network, $R_{in,sec,1}$ can be expressed as:

$$R_{in,sec,1} = \prod_{q=1}^{n} G_{i,sec,q}^2 R_{load,sec,n}$$

$$= \frac{\prod_{q=1}^{n} G_{i,sec,q} k_{rec} V_{\mathrm{OUT}}^2 \cos^2 \phi_{rec}}{P_{\mathrm{OUT}}} \left(\frac{G_{i,tot}}{\prod_{p=1}^{m} G_{i,pri,p}}\right). \quad \text{(E.12)}$$

Substituting this expression for $R_{in,sec,1}$ into (E.10) yields:

$$Q_{in,sec,1} - Q_{load,pri,m} = \left(\frac{4|X_p|P_{\mathrm{OUT}}}{k_{inv}\sqrt{2k_{rec}}V_{\mathrm{IN}}V_{\mathrm{OUT}} \cos \phi_{inv} \cos \phi_{rec}}\right) \frac{\prod_{p=1}^{m} G_{i,pri,p}}{\prod_{q=1}^{n} G_{i,sec,q}}, \quad \text{(E.13)}$$

which is the same as (3.6d). Note that the term within the parenthesis on the right-hand side of (E.13) is the expression for the system factor K_{sys} as given in (3.7).

APPENDIX F

EXPRESSIONS FOR OPTIMAL CURRENT GAINS AND IMPEDANCE CHARACTERISTICS FOR UP TO TWO-STAGE MATCHING NETWORKS

TABLE F.1. EXPRESSIONS FOR OPTIMAL CURRENT GAINS AND COMPENSATION CHARACTERISTICS OF THE STAGES IN A CAPACITIVE WPT SYSTEM WITH UP TO TWO STAGES IN EACH OF THE PRIMARY-SIDE AND SECONDARY-SIDE NETWORKS

	$m = 1, n = 1$	$m = 1, n = 2$	$m = 2, n = 1$	$m = 2, n = 2$
$G_{i,pri,1}$	$\sqrt{\frac{1 + G_{i,tot}^2}{K_{sys}}}$	$\sqrt{\frac{1}{K_{sys}} \frac{\left(G_{i,sec,2}^2 + G_{i,tot}^2\right)}{G_{i,sec,2}}}$	$\frac{1}{2}\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)$	$\sqrt{\frac{1 + \sqrt{4K_{sys} + 1}}{2K_{sys}}}$
$G_{i,pri,2}$	–	–	$\sqrt{\frac{1}{K_{sys}} \frac{\left(G_{i,pri,1}^2 + G_{i,tot}^2\right)}{G_{i,pri,1}^3}}$	$\sqrt{\frac{2\left(1 + G_{i,tot}^2\right)}{1 + \sqrt{1 + 4K_{sys}}}}$
$G_{i,sec,1}$	$G_{i,tot}\sqrt{\frac{K_{sys}}{1 + G_{i,tot}^2}}$	$\sqrt{\frac{K_{sys} G_{i,tot}^2}{G_{i,sec,2}\left(G_{i,sec,2}^2 + G_{i,tot}^2\right)}}$	$\sqrt{K_{sys}\left(\frac{G_{i,tot}^2 G_{i,pri,1}}{G_{i,tot}^2 + G_{i,VG,1}^2}\right)}$	$\sqrt{\frac{2K_{sys} G_{i,tot}^2}{\left(1 + G_{i,tot}^2\right)\left(\sqrt{1 + 4K_{sys}} - 1\right)}}$
$G_{i,sec,2}$	–	$\frac{2}{\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)}$	–	$\sqrt{\frac{\sqrt{1 + 4K_{sys}} - 1}{2}}$
$Q_{in,pri,1}$	$\tan\phi_{inv}$	$\tan\phi_{inv}$	$\tan\phi_{inv}$	$\tan\phi_{inv}$
$Q_{load,pri,1}$	$-G_{i,tot}$	$-\frac{G_{i,tot}}{2}\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)$	$-\frac{1}{2}\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)$	$-\sqrt{\frac{1 + \sqrt{4K_{sys} + 1}}{2K_{sys}}}$
$Q_{in,pri,2}$	–	–	$Q_{load,pri,1}$	$Q_{load,pri,1}$
$Q_{load,pri,2}$	–	–	$-\frac{2G_{i,tot}}{\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)}$	$-G_{i,tot}$
$Q_{in,sec,1}$	$\frac{1}{G_{i,tot}}$	$\frac{2}{G_{i,tot}\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)}$	$\frac{1}{2G_{i,tot}}\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)$	$\frac{1}{G_{i,tot}}$
$Q_{load,sec,1}$	$\tan\phi_{rec}$	$\frac{1}{2}\left(K_{sys} - \sqrt{K_{sys}^2 - 4}\right)$	$\tan\phi_{rec}$	$\sqrt{\frac{2}{\left(\sqrt{1 + 4K_{sys}} - 1\right)}}$
$Q_{in,sec,2}$	–	$Q_{load,sec,1}$	–	$Q_{load,sec,1}$
$Q_{load,sec,2}$	–	$\tan\phi_{rec}$	–	$\tan\phi_{rec}$

This appendix provides closed-form expressions for the optimal current gains and compensation characteristics of the L-section stages of capacitive WPT systems having up to two stages in their primary-side and up to two stages in their secondary-side networks (that is, for $m = 1$ or 2, and $n = 1$ or 2). These closed-form expressions are given above in Table F.1 in terms of the system factor K_{sys} (which can be computed using (3.7)), the total current gain $G_{i,tot}$ (which can be computed using (3.6e)), the minimum phase between the inverter output voltage and output current (ϕ_{inv}) required for ZVS of the inverter transistors (which can be computed using (3.6b)), and the minimum phase between the rectifier input voltage and input current (ϕ_{rec}) required for ZVS of the rectifier transistors (which can be computed using (3.6c)).

APPENDIX G

EXPRESSION FOR ASYMPTOTIC MAXIMUM MATCHING NETWORK EFFICIENCY

This appendix derives the expression for the asymptotic maximum matching network efficiency η_∞ of the capacitive WPT system of Fig. 3.3, as given by (3.19). Rearranging (3.10) gives the following relationship for $(m + n - 2)$:

$$m + n - 2 = \frac{\ln\left(\frac{1+G_{i.pri,eq}^2}{K_{sys}G_{i,pri,eq}^2}\right)}{\ln G_{i.pri,eq}}. \tag{G.1}$$

Using (3.7) and (3.9)-(3.18), the overall matching network efficiency can be expressed as:

$$\eta_{mn} \approx 1 - \frac{\sum_{p=1}^{m} Q_{eff,pri,p} + \sum_{q=1}^{n} Q_{eff,sec,q}}{Q_L}$$

$$= 1 - \frac{(m+n-2)\left(\frac{1}{G_{i,pri,eq}} - G_{i,pri,eq}\right) + 2\sqrt{K_{sys}G_{i,pri,eq}^{m+n-2} - 1}}{Q_L} - \frac{\tan\phi_{inv}}{Q_L} + \frac{\tan\phi_{rec}}{Q_L}. \tag{G.2}$$

Substituting the expression for $(m + n - 2)$ from (G.1) into (G.2) yields:

$$\eta_{mn} = 1 - \frac{\ln\left(\frac{1+G_{i.pri,eq}^2}{K_{sys}G_{i,pri,eq}^2}\right)\frac{\left(\frac{1}{G_{i,pri,eq}} - G_{i,pri,eq}\right)}{\ln(G_{i,pri,eq})} + \frac{2}{G_{i,pri,eq}}}{Q_L} - \frac{\tan\phi_{inv}}{Q_L} + \frac{\tan\phi_{rec}}{Q_L}. \tag{G.3}$$

As the number of stages in the primary-side and secondary-side networks (m and n, respectively) increase, each stage provides a smaller gain, i.e., a gain closer to unity. In the limiting case, as the number of stages approaches infinity, the optimal equal current gain $G_{i,pri,eq}$ provided by the first $(m - 1)$ primary-side stages and the optimal equal current gain $G_{i,sec,eq}$ provided by the last $(n - 1)$ secondary-side stages both approach 1. Applying this limiting condition to (G.3) gives:

$$\eta_\infty = \lim_{m,n\to\infty} \eta_{mn} = \lim_{G_{i,pri,eq}\to 1} \eta_{mn}$$

$$= \lim_{G_{i,pri,eq}\to 1} 1 - \frac{\ln\left(\frac{1+G_{i,pri,eq}^2}{K_{sys}G_{i,pri,eq}^2}\right)\frac{\left(\frac{1}{G_{i,pri,eq}}-G_{i,pri,eq}\right)}{\ln(G_{i,pri,eq})}+\frac{2}{G_{i,pri,eq}}}{Q_L} - \frac{\tan\phi_{inv}}{Q_L} + \frac{\tan\phi_{rec}}{Q_L}. \qquad \text{(G.4)}$$

Applying L'Hospital's rule, the asymptotic maximum efficiency expression of (G.4) reduces to:

$$\eta_\infty = 1 - \frac{2\left(1+\ln\left(\frac{K_{sys}}{2}\right)\right)}{Q_L} - \frac{\tan\phi_{inv}}{Q_L} + \frac{\tan\phi_{rec}}{Q_L}. \qquad \text{(G.5)}$$

The term $\tan\phi_{inv}$ in (G.5) arises due to the phase-difference between the inverter output voltage and output current required to achieve ZVS of the inverter transistors. Similarly, the term $\tan\phi_{rec}$ in (G.5) arises due to the phase-difference between the rectifier input voltage and input current required to achieve ZVS of the rectifier transistors. For a well-designed system, these phase angles, and hence their tangents, are small, and can be neglected in comparison to the value of the first two terms in (G.5). Therefore, the asymptotic maximum efficiency can be approximated as:

$$\eta_\infty \approx 1 - \frac{2\left(1+\ln\left(\frac{K_{sys}}{2}\right)\right)}{Q_L}, \qquad \text{(G.6)}$$

which is the same as (3.19).

APPENDIX H

CONVENTIONAL APPROACH TO DEIGNING MATCHING NETWORKS IN CAPACITIVE WPT SYSTEMS

This appendix describes the conventional approach to designing matching networks in a capacitive WPT system, based on the approach presented in [60]. In this approach, the parts of the networks adjacent to the coupling plates provide all the required compensation and a portion of the required gain, while the parts adjacent to the inverter and the rectifier provide the remaining gain and no compensation. The capacitive WPT system of [60] comprise a two-stage network on the primary side of the coupler and another two-stage network on the secondary side. The topology of such a capacitive WPT system

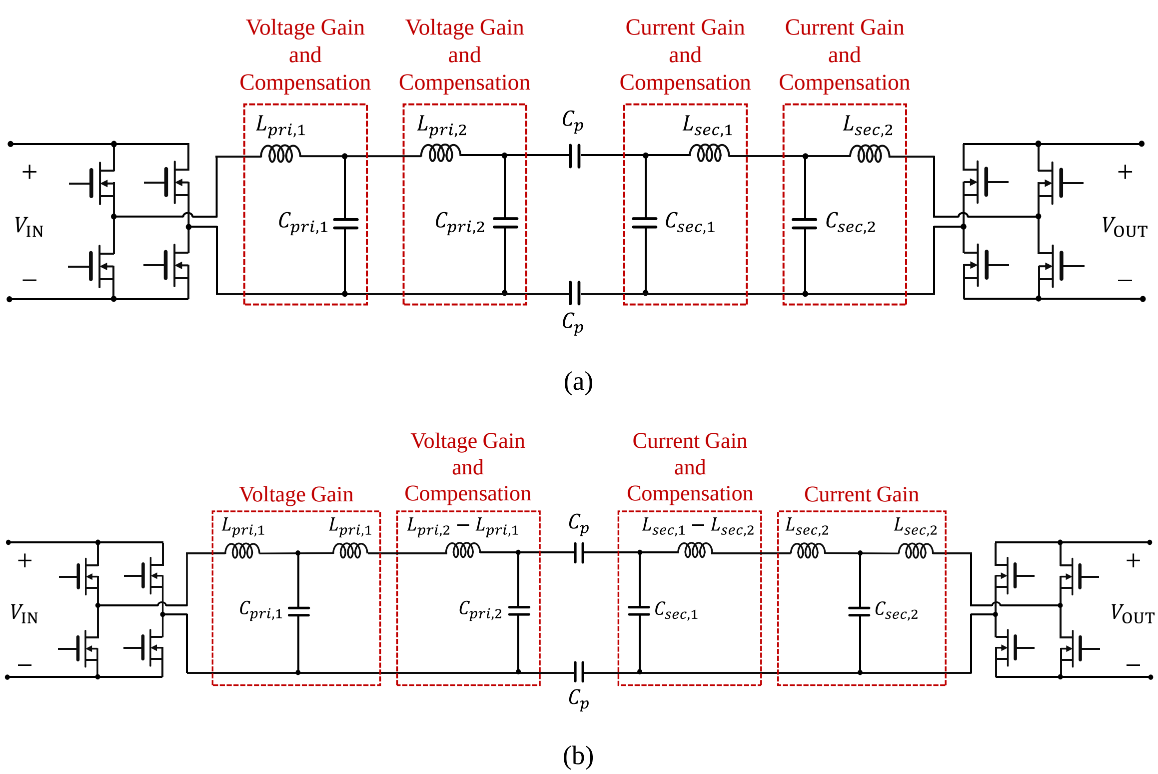

Fig. H.1: Conventional design approach for a capacitive WPT system with two-stage matching networks on either side of the coupler: (a) system topology, and (b) breakdown of matching networks into their functional components.

is shown in Fig. H.1(a). In this design approach, the inductances of the second stage of the primary-side network and the first stage of the secondary-side network ($L_{pri,2}$ and $L_{sec,1}$ in Fig. H.1(a), respectively) are split into two functional parts, as shown in Fig. H.1(b). In the the primary-side network, the first functional part of this inductance equals the inductance of the first stage ($L_{pri,1}$ in Fig. H.1(b)). The capacitance of the first stage ($C_{pri,1}$) is then designed to have a reactance equal to that of $L_{pri,1}$ at the operating frequency f_s, that is:

$$\frac{1}{2\pi f_s C_{pri,1}} = 2\pi f_s L_{pri,1}. \tag{H.1}$$

With this design, the LCL-T network formed by the two inductances $L_{pri,1}$ and the capacitance $C_{pri,1}$ forms an immittance network [54] that provides a voltage step-up but does not provide any reactive compensation. In a similar manner, in the secondary-side network, the second functional part of the inductance equals the inductance of the second stage ($L_{sec,2}$ in Fig. H.1(b)). The capacitance of the second stage ($C_{sec,2}$) is designed to have a reactance equal to that of $L_{sec,2}$ at the operating frequency f_s, and is given by:

$$\frac{1}{2\pi f_s C_{sec,2}} = 2\pi f_s L_{sec,2}. \tag{H.2}$$

The LCL-T network comprising the inductances $L_{sec,2}$ and the capacitance $C_{sec,2}$ is also an immittance network. This network provides a current step-up and no compensation. All the compensation in the system shown in Fig. H.1(b) is provided by the remaining part of the inductance of the second stage on the primary side ($L_{pri,2} - L_{pri,1}$ in Fig. H.1(b)), the capacitance of this stage ($C_{pri,2}$), the remaining part of the inductance of the first stage on the secondary side ($L_{sec,1} - L_{sec,2}$), and the capacitance of this stage ($C_{sec,1}$). To achieve this, the inductance $L_{pri,2} - L_{pri,1}$ is designed to resonate with an effective capacitance that equals the parallel combination of the capacitance $C_{pri,2}$ with a series combination of the two coupling capacitances C_p and the capacitance $C_{sec,1}$, as shown in Fig. H.2(a). This can be mathematically expressed as:

$$L_{pri,2} - L_{pri,1} = \frac{1}{(2\pi f_s)^2} \frac{1}{\left(C_{pri,2} + \left(\frac{C_p}{2} \parallel C_{sec,1}\right)\right)}. \tag{H.3}$$

Similarly, the inductance $L_{sec,1} - L_{sec,2}$ is designed to resonate with an effective capacitance that equals the parallel combination of the capacitance $C_{sec,1}$ with a series combination of the two coupling capacitances C_p and the capacitance $C_{pri,2}$, as shown in Fig. H.2(b), and mathematically expressed as:

$$L_{sec,1} - L_{sec,2} = \frac{1}{(2\pi f_s)^2} \frac{1}{\left(C_{sec,1} + \left(\frac{C_p}{2} \parallel C_{pri,2}\right)\right)}. \tag{H.4}$$

Using the design relationships of (H.1)-(H.4), and applying superposition and Kirchhoff's voltage law (KVL) under the assumption of lossless power conversion, the following additional design relationship is obtained:

$$\frac{C_{pri,1}C_{sec,2}}{2C_{pri,2}C_{sec,1} + C_{pri,2}C_p + C_{sec,1}C_p} = \frac{1}{\pi k_{inv}\sqrt{2k_{rec}}} \frac{P_{\mathrm{OUT}}}{f_s C_p V_{\mathrm{IN}} V_{\mathrm{OUT}} \cos\phi_{rec}}. \tag{H.5}$$

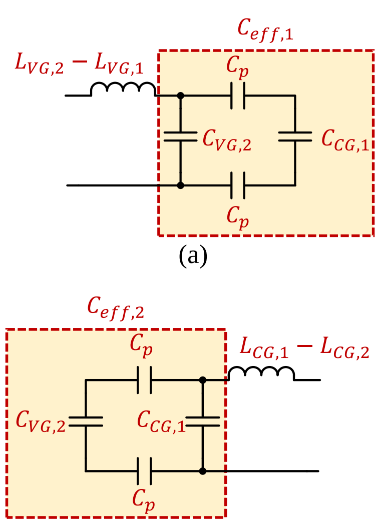

Fig. H.2: Resonances used to provide compensation in the capacitive WPT system of Fig. H.1(b): (a) $L_{pri,2} - L_{pri,1}$ resonates with the effective capacitance $C_{eff,1}$ (b) $L_{sec,1} - L_{sec,2}$ resonates with the effective capacitance $C_{eff,2}$.

Since the two-stage networks on the primary and secondary sides in the system of Fig. H.1(a) have a total of eight components, three more design relationships are required in addition to those provided in (H.1)-(H.5). Two of these design relationships are obtained by observing that the capacitive WPT system designed using the conventional approach is symmetric about the coupling plates, that is, the inductance and capacitance values of the primary-side and secondary-side stages that are symmetrically located relative to the coupling plates are equal [60]. This symmetry results in the following relationships:

$$C_{pri,1} = C_{sec,2}, \tag{H.6}$$

$$C_{pri,2} = C_{sec,1}. \tag{H.7}$$

The final relationship is obtained by designing the matching networks to achieve a desired air-gap voltage. Using (H.1)-(H.7), and applying KVL to the circuit of Fig. H.1(a), the circuit component values can be related to the RMS value of the air-gap voltage, $v_{ag,rms}$, as:

$$\frac{C_{pri,2}+C_p}{C_{pri,1}} = \frac{\sqrt{k_{inv}^2 V_{\mathrm{IN}}^2 + 2k_{rec}{V_{\mathrm{OUT}}}^2 + 2k_{inv}\sqrt{2k_{rec}}V_{\mathrm{IN}}V_{\mathrm{OUT}}\cos\left(\frac{\pi}{2}-\phi_{rec}\right)}}{2V_{ag,pk}}. \tag{H.8}$$

Given a desired air-gap voltage $v_{ag,rms}$, (H.1)-(H.8) can be used to obtain the values of the eight inductances and capacitances of the two stages of the primary side network and the two stages of the secondary-side network of the capacitive WPT system of Fig. H.1(a).

APPENDIX I

EXPRESSIONS FOR OPTIMAL CURRENT GAINS AND IMPEDANCE CHARACTERISTICS IN AIR-GAP VOLTAGE CONSTRAINED DESIGN

This appendix derives expressions for the optimal current gains (G_i's) and impedance characteristics (Q_{in}'s and Q_{load}'s) of the primary-side and secondary-side stages of the capacitive WPT system of Fig. 3.6, when the voltage across the air-gap v_{ag} is specified. Given the air-gap voltage v_{ag}, the displacement current through the coupling plates can be expressed as:

$$I_p = \frac{v_{ag}}{X_p}. \tag{I.1}$$

Given the input and output voltages and the output power of the capacitive WPT system, the plate current directly determines the total current gains required from the primary-side network and the secondary-side network (denoted by $G_{i,pri,tot}$ and $G_{i,sec,tot}$, respectively), which are given by:

$$G_{i,pri,tot} = \frac{I_p}{I_{in,pri,1}} = \frac{k_{inv} V_{\mathrm{IN}} \cos\phi_{inv} I_p}{\sqrt{2} P_{\mathrm{OUT}}}, \tag{I.2}$$

$$G_{i,sec,tot} = \frac{I_{out,sec,n}}{I_p} = \frac{\sqrt{2k_{rec}} V_{\mathrm{OUT}} \cos\phi_{rec}}{\sqrt{2} P_{\mathrm{OUT}} I_p}. \tag{I.3}$$

With these additional constraints, the Lagrangian in (3.8) can be re-written as:

$$\begin{aligned}
\mathcal{L} = &\left(\sum_{p=1}^{m} Q_{eff,pri,p} + \sum_{q=1}^{n} Q_{eff,sec,q}\right) \\
&+\lambda_1 \left(\prod_{p=1}^{m} G_{i,pri,p} - \frac{k_{inv} V_{\mathrm{IN}} \cos\phi_{inv} I_p}{\sqrt{2} P_{\mathrm{OUT}}}\right) \\
&+\lambda_2 \left(\prod_{q=1}^{n} G_{i,sec,q} - \frac{\sqrt{2k_{rec}} V_{\mathrm{OUT}} \cos\phi_{rec}}{\sqrt{2} P_{\mathrm{OUT}} I_p}\right) \\
&+\lambda_3 (Q_{in,pri,1} - \tan\phi_{inv}) + \lambda_4 (Q_{load,sec,n} - \tan\phi_{rec})
\end{aligned}$$

$$+\lambda_5\left(Q_{in,sec,1}-Q_{load,pri,m}-\frac{|X_p|I_p^2}{P_{\mathrm{OUT}}}\right). \tag{I.4}$$

The optimal current gains and compensation characteristics can be determined using the procedure outlined in Section 3.2. Similar to the case when the air-gap voltage is not specified (as in Section 3.2), the current gains of the first $(m-1)$ stages of the primary-side network come out to be equal, i.e.,

$$G_{i,pri,1}=G_{i,pri,2}=\cdots=G_{i,pri,m-1}\stackrel{\mathrm{def}}{=}G_{i,pri,eq}. \tag{I.5}$$

Similarly, the current gains of the last $(n-1)$ stages of the secondary-side network also come out to be equal, i.e.,

$$G_{i,sec,n}=G_{i,sec,n-1}=\cdots=G_{i,sec,2}\stackrel{\mathrm{def}}{=}G_{i,sec,eq}. \tag{I.6}$$

The optimal load impedance characteristics of the first $(m-1)$ primary-side stages are also equal, and related to the optimal equal current gain $G_{i,VG,eq}$ as:

$$Q_{load,pri,1}=Q_{load,pri,2}=\cdots=Q_{load,pri,m-1}=-G_{i,pri.eq}. \tag{I.7}$$

Similarly, the optimal input impedance characteristics of the last $(n-1)$ secondary-side stages also come out to be equal, and related to the optimal equal current gain $G_{i,sec,eq}$ as:

$$Q_{in,sec,1}=Q_{in,sec,2}=\cdots=Q_{in,sec,n-1}=\frac{1}{G_{i,sec,eq}}. \tag{I.8}$$

The optimal equal current gains $G_{i,pri,eq}$ and $G_{i,sec,eq}$, the optimal load impedance characteristic of the last (m-th) primary-side stage, $Q_{load,pri,m}$, and the optimal input impedance characteristic of the first secondary-side stage, $Q_{in,sec,1}$, can be determined by simultaneously solving the following equations:

$$G_{i,pri,eq}=\frac{G_{i,pri,tot}}{\sqrt{G_{i,pri,eq}^{2(m-1)}\left(1+Q_{load,pri,m}^2\right)-G_{i,pri,tot}^2}}, \tag{I.9}$$

$$G_{i,sec,eq}=\frac{\sqrt{G_{i,sec,tot}^2\left(1+Q_{in,sec,1}^2\right)-G_{i,sec,eq}^{2(n-1)}}}{G_{i,sec,eq}^{n-1}}, \tag{I.10}$$

$$Q_{in,sec,1} - Q_{load,pri,m} = \frac{|X_p| I_p^2}{P_{\text{OUT}}}, \tag{I.11}$$

$$\frac{G_{i,pri,eq}^{2(m-1)} Q_{load,pri,m}}{G_{i,pri,tot}\sqrt{G_{i,pri,eq}^{2(m-1)}\left(1+Q_{load,pri,m}^2\right)-G_{i,pri,tot}^2}} + \frac{G_{i,sec,tot}^2 Q_{in,sec,1}}{G_{i,sec,eq}^{n-1}\sqrt{G_{i,sec,tot}^2\left(1+Q_{in,sec,1}^2\right)-G_{i,sec,eq}^{2(n-1)}}} = 0. \tag{I.12}$$

The current gains of the last primary-side stage and the first secondary-side stage can then be determined using the following expressions:

$$G_{i,pri,m} = \frac{G_{i,pri,tot}}{G_{i,pri,eq}^{m-1}}, \tag{I.13}$$

$$G_{i,sec,1} = \frac{G_{i,sec,tot}}{G_{i,sec,eq}^{n-1}}. \tag{I.14}$$

Finally, given these optimal current gains and compensation characteristics, the inductance and capacitance values of the L-section stages of the primary-side and the secondary-side networks can be obtained using (3.1) and (3.2).

APPENDIX J

EXPRESSION FOR INPUT IMPEDANCE OF AN AVR RECTIFIER

This appendix derives the expression for the input impedance Z_r of the AVR rectifier as given by (4.1), and the relationships between the voltages V_1 and V_2 of the AVR rectifier as given by (4.3) and (4.4). The AVR-rectifier-enabled capacitive WPT system of Fig. 4.1 is redrawn in Fig. J.1, with the resistances looking into the top and bottom rectifiers indicated as R_1 and R_2, respectively. Under fundamental frequency analysis, these resistances can be expressed as:

$$R_1 = k_\mathrm{rec}\frac{V_1^2}{P_1}, \tag{J.1}$$

and

$$R_2 = k_\mathrm{rec}\frac{V_2^2}{P_2}. \tag{J.2}$$

The input impedance of the AVR rectifier can now be expressed as:

$$Z_\mathrm{r} = R_\mathrm{r} + jX_\mathrm{r} = (R_1 + jX)||(R_2 - jX)$$

$$= \frac{R_1R_2 + X^2}{R_1 + R_2} + jX\frac{(R_2 - R_1)}{R_2 + R_1}. \tag{J.3}$$

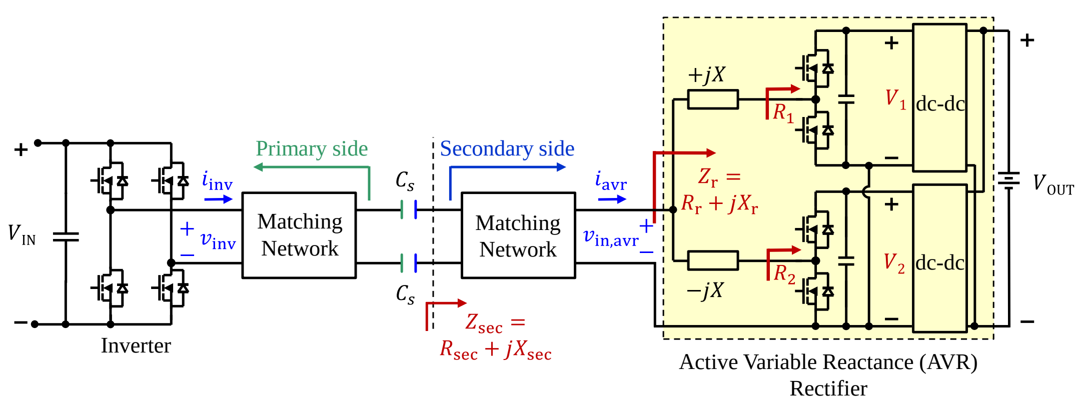

Fig. J.1: A capacitive wireless power transfer (WPT) system with an active variable reactance (AVR) rectifier showing the resistances looking into the two half-bridge rectifiers R_1 and R_2.

Substituting expressions for R_1 and R_2 given by (J.1) and (J.2) into (J.3) yields:

$$Z_{\mathrm{r}} = R_{\mathrm{r}} + jX_{\mathrm{r}} = \frac{k_{rec}^2 V_1^2 V_2^2 + P_1 P_2 X^2}{k_{rec}(P_1 V_2^2 + P_2 V_1^2)} + jX\frac{(P_1 V_2^2 - P_2 V_1^2)}{(P_1 V_2^2 + P_2 V_1^2)}, \tag{J.4}$$

which is the same as (4.1). Splitting (J.4) into two equations by equating its real and imaginary parts, and solving for R_1 and R_2 yields:

$$R_1 = \frac{(k+1)R_{\mathrm{r}} - \sqrt{(k+1)^2 R_{\mathrm{r}}^2 - 4kX^2}}{2k}, \tag{J.5}$$

and

$$R_2 = \frac{(k+1)R_{\mathrm{r}} - \sqrt{(k+1)^2 R_{\mathrm{r}}^2 - 4kX^2}}{2}, \tag{J.6}$$

where $k \equiv \frac{X+X_{\mathrm{r}}}{X-X_{\mathrm{r}}}$. When the coupling reactance changes, the AVR rectifier's input impedance is varied by changing the voltages V_1 and V_2 to provide reactive compensation and maintain output power at a fixed level. To maintain a constant output power, the powers processed by the two rectifiers must be related as:

$$P_1 + P_2 = P_{\mathrm{OUT}}. \tag{J.7}$$

Substituting expressions for P_1 and P_2 derived from (J.1) and (J.2) into (J.7) yields:

$$k_{\mathrm{rec}}\left(\frac{V_1^2}{R_1} + \frac{V_2^2}{R_2}\right) = P_{\mathrm{OUT}}. \tag{J.8}$$

By applying Kirchhoff's voltage law (KVL) around the two loops formed by each of the differential reactance ($+jX$ and $-jX$) and the following half-bridge rectifier, the magnitude of the voltages V_1 and V_2 can be expressed under fundamental frequency approximation as:

$$V_1 = \frac{\pi}{\sqrt{2}} v_{\mathrm{in,avr}} \frac{R_1}{\sqrt{R_1^2 + X^2}}, \tag{J.9}$$

and

$$V_2 = \frac{\pi}{\sqrt{2}} v_{\text{in,avr}} \frac{R_2}{\sqrt{R_2^2+X^2}}, \tag{J.10}$$

where $v_{\text{in,avr}}$ is the input voltage of the AVR rectifier. Dividing (J.10) by (J.9) yields:

$$\frac{V_2}{V_1} = \frac{R_2}{R_1}\sqrt{\frac{R_1^2+X^2}{R_2^2+X^2}}. \tag{J.11}$$

Substitution of expressions for R_1 and R_2 given by (J.5) and (J.6) into (J.8) and (J.11) and subsequent simplification results in the following two relationships for V_1 and V_2:

$$V_1 = \sqrt{\frac{\frac{1}{2k_{\text{rec}}}P_{\text{OUT}}\left(R_{\text{r}}(k+1)-\sqrt{R_{\text{r}}^2(k+1)^2-4kX^2}\right)\left(\left(R_{\text{r}}(k+1)-\sqrt{R_{\text{r}}^2(k+1)^2-4kX^2}\right)^2+4X^2\right)}{\left(\left(R_{\text{r}}(k+1)-\sqrt{R_{\text{r}}^2(k+1)^2-4kX^2}\right)^2+4kX^2\right)(1+k)}}, \tag{J.12}$$

and

$$V_2 = \sqrt{\frac{\frac{1}{2k_{\text{rec}}}P_{\text{OUT}}\left(R_{\text{r}}(k+1)-\sqrt{R_{\text{r}}^2(k+1)^2-4kX^2}\right)\left(\left(R_{\text{r}}(k+1)-\sqrt{R_{\text{r}}^2(k+1)^2-4kX^2}\right)^2+4k^2X^2\right)}{\left(\left(R_{\text{r}}(k+1)-\sqrt{R_{\text{r}}^2(k+1)^2-4kX^2}\right)^2+4kX^2\right)(1+k)}}. \tag{J.13}$$

which are the same as (4.3) and (4.4).

APPENDIX K

EXPRESSION FOR OUTPUT POWER IN AVR-RECTIFIER-BASED CAPACITIVE WPT SYSTEMS

This appendix derives the expression for the output power in the AVR-rectifier-enabled capacitive WPT system of Fig. 4.4, as given by (4.5), and the expression for the first upper limit on the overall current gain of the matching network, $G_{\max,1}$, as given by (4.6). The rms value of the voltage at the output port of the inverter can be expressed as:

$$v_{\mathrm{inv}} = \frac{1}{\sqrt{2}} k_{\mathrm{inv}} V_{\mathrm{IN}}. \tag{K.1}$$

Under the nominal coupling condition, the impedance seen by the inverter, and the input impedance of the AVR rectifier are both purely resistive. Under this condition, assuming lossless power conversion, the rms voltage at the input port of the AVR rectifier can be expressed as:

$$v_{\mathrm{in,avr}} = \frac{P_{\mathrm{OUT}}}{|i_{\mathrm{avr}}|} = \frac{v_{\mathrm{inv}}|i_{\mathrm{inv}}|}{|i_{\mathrm{avr}}|} = \frac{\frac{1}{\sqrt{2}} k_{\mathrm{inv}} V_{\mathrm{IN}} |i_{\mathrm{inv}}|}{|i_{\mathrm{avr}}|} = \frac{1}{\sqrt{2}} \frac{k_{\mathrm{inv}} V_{\mathrm{IN}}}{G}, \tag{K.2}$$

where G is the overall current gain provided by the matching networks, defined as $G \equiv |i_{\mathrm{avr}}|/|i_{\mathrm{inv}}|$. Under nominal coupling conditions, the dc-dc converters of the AVR rectifier are in pass-through mode, i.e., $V_1 = V_2 = V_{\mathrm{OUT}}$, and each half-bridge rectifier processes half the output power, i.e., $P_1 = P_2 = \frac{P_{\mathrm{OUT}}}{2}$. Therefore, under this nominal coupling condition, the input resistances of the two rectifiers, R_1 and R_2, can be expressed as:

$$R_1 = R_2 = k_{\mathrm{rec}} \frac{V_1^2}{P_1} = k_{\mathrm{rec}} \frac{V_2^2}{P_2} = k_{\mathrm{rec}} \frac{V_{\mathrm{OUT}}^2}{\left(\frac{P_{\mathrm{OUT}}}{2}\right)}. \tag{K.3}$$

Furthermore, the input impedance of the AVR rectifier can be expressed as:

$$Z_{\mathrm{r}} = R_{\mathrm{r}} + jX_{\mathrm{r}} = (R_1 + jX)||(R_2 - jX) = \frac{R_1 R_2 + X^2}{R_1 + R_2} + jX \frac{(R_2 - R_1)}{R_2 + R_1}. \tag{K.4}$$

Substituting expressions for R_1 and R_2 given by (K.3) into (K.4) results in the expression for the AVR rectifier's input impedance under nominal coupling condition, and is given by:

$$Z_{\mathrm{r}} = R_{\mathrm{r}} + jX_{\mathrm{r}} = \frac{4k_{rec}^2 V_{\mathrm{OUT}}^4 + P_{\mathrm{OUT}}^2 X^2}{4k_{rec} V_{\mathrm{OUT}}^2 P_{\mathrm{OUT}}} + j0. \tag{K.5}$$

Since, under the nominal coupling condition, the AVR rectifier does not provide any reactance ($X_{\mathrm{r}} = 0$), the output power can be expressed as:

$$P_{\mathrm{OUT}} = \frac{v_{\mathrm{in,avr}}^2}{R_{\mathrm{r}}}. \tag{K.6}$$

Substitution of expressions for $v_{\mathrm{in,avr}}$ and R_{r} given by (K.2) and (K.5), respectively, into (K.6) and subsequent simplification yields:

$$P_{\mathrm{OUT}} = \frac{V_{\mathrm{OUT}}}{X}\sqrt{\frac{2k_{\mathrm{inv}}^2 k_{\mathrm{rec}} V_{\mathrm{IN}}^2}{G^2} - 4k_{\mathrm{rec}}^2 V_{\mathrm{OUT}}^2}, \tag{K.7}$$

which is the same as (4.5). It can be seen from (K.7) that for P_{OUT} to be real and non-zero, the overall current gain of the matching network must satisfy the following relationship:

$$\frac{2k_{\mathrm{inv}}^2 k_{\mathrm{rec}} V_{\mathrm{IN}}^2}{G^2} - 4k_{\mathrm{rec}}^2 V_{\mathrm{OUT}}^2 > 0. \tag{K.8}$$

Simplification of (K.8) yields:

$$G < \frac{1}{\sqrt{2}} \frac{k_{\mathrm{inv}}}{\sqrt{k_{\mathrm{rec}}}} \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}} \equiv G_{\mathrm{max,1}}, \tag{K.9}$$

which is the same as (4.6).

APPENDIX L

AVR RECTIFIER INPUT IMPEDANCE RELATIONSHIP FOR PROVIDING REACTIVE COMPENSATION AND MAINTAING FULL POWER TRANSFER

This appendix derives the relationship that must be satisfied by the input impedance of the AVR rectifier, Z_{r}, to ensure reactive compensation and full power transfer under varying coupling conditions, as given by (4.15). The change in coupling reactance ($-\Delta X_{\mathrm{s}}$) is compensated by controlling the voltages V_1 and V_2 of the AVR rectifier such that the secondary-side impedance, Z_{sec}, is more inductive than its nominal value by an amount $+\Delta X_{\mathrm{s}}$, as expressed mathematically in (4.2) and reproduced here:

$$Z_{\mathrm{sec}} = Z_{\mathrm{sec,0}} + j\Delta X_{\mathrm{s}}, \tag{L.1}$$

where $Z_{\mathrm{sec,0}} = R_{\mathrm{sec,0}} + jX_{\mathrm{sec,0}}$. The value of the secondary-side impedance can be obtained by transforming the AVR input impedance Z_{r} through the secondary-side matching network, and can be expressed as:

$$Z_{\mathrm{sec}} = (Z_{\mathrm{r}} + j\omega_{\mathrm{s}}L_2) \,||\, \left(-\frac{j}{\omega_{\mathrm{s}}C_2}\right) = (R_{\mathrm{r}} + jX_{\mathrm{r}} + j\omega_{\mathrm{s}}L_2) \,||\, \left(-\frac{j}{\omega_{\mathrm{s}}C_2}\right). \tag{L.2}$$

The value of this secondary-side impedance under nominal coupling conditions can be expressed as:

$$Z_{\mathrm{sec,0}} = \left(Z_{\mathrm{r,0}} + j\omega_{\mathrm{s}}L_2\right) \,||\, \left(-\frac{j}{\omega_{\mathrm{s}}C_2}\right). \tag{L.3}$$

The input impedance of the AVR rectifier under nominal coupling conditions, $Z_{\mathrm{r,0}}$, can be obtained by substituting $V_1 = V_2 = V_{\mathrm{OUT}}$, and $P_1 = P_2 = \frac{P_{\mathrm{OUT}}}{2}$ into (4.1), and is given by:

$$Z_{\mathrm{r,0}} = \frac{4k_{rec}^2V_{\mathrm{OUT}}^4 + P_{\mathrm{OUT}}^2X^2}{4k_{rec}V_{\mathrm{OUT}}^2P_{\mathrm{OUT}}} + j0. \tag{L.4}$$

Substituting the expression for $Z_{\mathrm{r,0}}$ given by (L.4) into (L.3) yields:

$$Z_{\text{sec},0} = \left(\frac{4k_{rec}^2 V_{\text{OUT}}^4 + P_{\text{OUT}}^2 X^2}{4k_{rec} V_{\text{OUT}}^2 P_{\text{OUT}}} + j\omega_{\text{s}} L_2\right) \mid\mid \left(-\frac{j}{\omega_{\text{s}} C_2}\right). \tag{L.5}$$

Substituting expressions for Z_{sec} and $Z_{\text{sec},0}$ given by (L.2) and (L.5) into (L.1) yields:

$$\left((R_{\text{r}} + jX_{\text{r}}) + j\omega_{\text{s}} L_2\right) \mid\mid \left(-\frac{j}{\omega_{\text{s}} C_2}\right) = \left(\frac{4k_{rec}^2 V_{\text{OUT}}^4 + P_{\text{OUT}}^2 X^2}{4k_{rec} V_{\text{OUT}}^2 P_{\text{OUT}}} + j\omega_{\text{s}} L_2\right) \mid\mid \left(-\frac{j}{\omega_{\text{s}} C_2}\right) + j\Delta X_{\text{s}}, \tag{L.6}$$

which is the same as (4.15).

APPENDIX M

SYSTEM COST METRIC FOR COMPARING AVR-BASED AND NON-AVR-BASED DYNAMIC CAPACITIVE WPT SYSTEMS

This appendix introduces a system cost metric to compare AVR-based and non-AVR-based dynamic wireless power transfer systems. This system cost metric includes the cost of both roadway and vehicle side components, as well as the cost of energy consumed in charging the vehicle, and is formulated as:

$$c_{\mathrm{tot}} = c_{\mathrm{r}} n_{\mathrm{r}} + (c_{\mathrm{v}} + c_{\mathrm{bat}} + c_{\mathrm{e}}) n_{\mathrm{v}}. \tag{M.1}$$

Here, c_{r} is the cost of one roadway-side wireless charging module, n_{r} is the number of roadway-side modules on a given length of roadway, c_{v} is the cost of each vehicle-side charging module, c_{bat} is the cost of battery in each vehicle, c_{e} is the cost of electrical energy needed to propel a vehicle over the given length of roadway, and n_{v} is the number of vehicles using this electrified roadway in a given period of time.

To evaluate the potential benefits of the AVR rectifier using (M.1), consider the electrified roadway shown in Fig. M.1. This roadway comprises a series of charging pads placed at intervals such that when designed for vehicles equipped with the AVR rectifier, the vehicles receive constant power, as shown by the solid blue line. On the other hand, when designed for vehicles without the AVR rectifier, the vehicles receive pulsating power, as shown by the dotted red line, since power transfer in a non-AVR-based system falls rapidly with misalignment. To deliver the same average power to a vehicle, the non-AVR-based system needs to transfer substantially higher peak power than the AVR-based system.

Both the AVR and non-AVR-based systems have the same number of roadway-side components. However, the AVR-based system is rated for lower peak power, so in terms of the cost of the roadway-side charging pads, c_{r}, the AVR-based system is less expensive than the non-AVR-based system. The vehicle side of the AVR-based system has a larger number of components. This higher component count

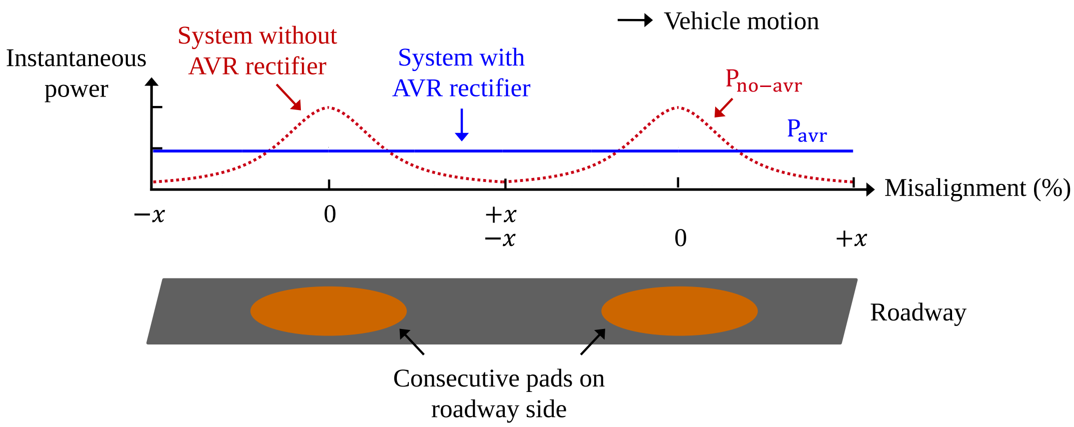

Fig. M.1: Wireless power delivered to an electric vehicle by an electrified roadway in an AVR-based (solid blue line) and a non-AVR-based (dotted red line) system. The AVR-based system delivers constant power, while the non-AVR-based system delivers pulsating power with a substantially higher peak value.

can be outweighed by the lower power rating of the AVR-based system. For example, the vehicle side of the AVR-based system described in Section V has 2.2-times larger number of components than the non-AVR-based system. However, due to its non-uniform power delivery profile, the non-AVR based system needs to deliver 2.4-times higher peak power to an EV. Therefore, in terms of cost of the vehicle-side charging components, c_{v}, the AVR-based system is also less expensive than the non-AVR-based system. To account for the pulsating power of the non-AVR-based system, the vehicle battery needs to store more energy, and also accept higher charging currents compared to the AVR-based system. Therefore, the cost of the vehicle battery, c_{bat}, is also lower for an AVR-based system.

Finally, the AVR and non-AVR-based systems have to deliver the same average power to the vehicle. The AVR-based system has slightly lower full-power efficiency than the non-AVR-based system. However, since the AVR-based system is always operating close to its full power, its weighted average efficiency can potentially be higher than the weighted average efficiency of the non-AVR-based system, which is operating across its wide power range. To evaluate this, the energy drawn from the input source for one pass of a vehicle over a roadway-side pad is calculated for the AVR-based and the non-AVR-based systems as follows:

$$E_{\mathrm{in,pass,avr}} = \int_{-T/2}^{T/2} \frac{P_{\mathrm{avr}}}{\eta_{\mathrm{avr}}} dt. \tag{M.2}$$

$$E_{\mathrm{in,pass,no-avr}} = \int_{-T/2}^{T/2} \frac{P_{\mathrm{no-avr}}}{\eta_{\mathrm{no-avr}}} dt, \tag{M.3}$$

Here, P_{avr} and $P_{\mathrm{no-avr}}$ represent the instantaneous power delivered to the battery by the AVR-based and the non-AVR-based systems, respectively; η_{avr} and $\eta_{\mathrm{no-avr}}$ are the efficiencies of the two systems; and T is the time required for one pass of the vehicle. The efficiency of the AVR-based and the non-AVR-based systems are estimated using loss models for the inverter, matching networks, rectifier, and dc-dc converters. Based on these loss models, the AVR-based system draws 14% less energy than the non-AVR-based system to propel a vehicle over a given length of roadway, translating to a lower energy cost c_{e}.

In summary, despite its higher component count, the AVR-based dynamic wireless charging system results in a lower system cost, as given by (54), than the non-AVR-based system due to its ability to maintain constant power transfer.