TANTALUM OXIDE AND GE-INCORPORATED TANTALUM OXIDE PREPARED BY PULSED LASER DEPOSITION FOR HIGH-K DIELECTRIC APPLICATIONS

A Thesis

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by

Po-Ya Hsu

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Abstract

The electrical properties of tantalum oxides and Ge-incorporated tantalum oxides prepared by Pulsed Laser Deposition (PLD) in various oxygen environments (oxygen partial pressure from 8 mTorr to 100 mTorr) and deposition temperatures (room temperature to 400 °C) have been investigated in this study. The short-circuited capacitors and high dissipation factors of tantalum oxides deposited at high oxygen partial pressures (> 60 mTorr) suggest the porous structure of the film caused by low surface mobility of the atoms in high oxygen partial pressure environment. The overall high dissipation factors (>0.3) of tantalum oxide prepared at low oxygen partial pressure (8 mTorr) suggest the tantalum oxide is not fully oxidized even at 250 °C deposition temperature. X-ray Photoelectron Spectroscopy (XPS) analysis, and the fact of low dissipation factors (<0.04) without frequency dependence confirms the tantalum oxides deposited above 17.5 mTorr oxygen partial pressure are fully oxidized. Tantalum oxides deposited at an oxygen partial pressure of 30 mTorr at 250°C and 400°C show overall low dissipation factors (<0.01) without self-shadowing effect at thick region of the film, confirming the deposition condition for high-quality tantalum oxides. By fitting the XPS data, it is suggested that there are about 10% sub-oxides in the tantalum oxide prepared in low oxygen partial pressure (8 mTorr) causing the high dissipation factors. By alternately depositing Ta and Ge monolayer in PLD with selected shot ratio, Ge-incorporated tantalum oxide with composition spread of Ta concentration from 75% to 95% (Ge concentration from 25% to 5%) is generated. The Ge-incorporated tantalum oxide shows dielectric enhancement behavior from the range of 25% Ge substitution to 5% Ge substitution. With only 5% Ge substitution for Ta, a k value of 35 is obtained. The k value is increased by about 60% compared to the value of pure Ta_2O_5 (k=22)

in literature. The k values of tantalum oxide and Ge-incorporated tantalum oxide using PLD is higher than the literature value where sputtering is used to prepare the films. However, the trend of the dielectric enhancement behavior shows good correspondence in these two systems. It is possible that Ta oxide films and Ge-incorporated tantalum oxide films prepared by PLD can have higher dielectric constants. As a result, tantalum oxide system is still a promising candidate in PLD for high-k dielectric application

Biographical Sketch

Po-Ya Hsu was born in Taipei, Taiwan. He received his Bachelor's and Master's degrees in Engineering and System Science at National Tsing Hua University in Taiwan in 2010 and 2011. During the graduate study at National Tsing Hua University, he completed his Mater's thesis with the topic of "Fabrication of Highly Efficient Flexible Dye-sensitized Solar Cells Based on Quasi-solid-state electrolytes". In his thesis work, several attempts were made to successfully fabricate highly efficient flexible dye-sensitized solar cells based on quasi-solid-state electrolytes and ITO/PEN substrates, including compression treatment on photoelectrodes, binder-free low temperature TiO_2 paste, light-confined effects, thermal deposited Pt-counter electrodes and quasi-solid state electrolyte with TiO_2 nanoparticles. He was hired by Center for Energy and Environmental Research in National Tsing Hua University as a research assistant for developing advanced technology for dye-sensitized solar cells after graduating in 2011. He came to Cornell in 2012, and joined Prof. van Dover's group. He focused on the project "Tantalum oxide and Ge-incorporated tantalum oxide prepared by pulsed laser deposition for high-k dielectric applications" as the topic of his Master's thesis.

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1. Introduction

1.1 Background of high-k dielectric

The dielectric constant k reflects the ability that a material polarizes under electrical fields. For a dielectric oxide material, the relationship between capacitance per unit area, oxide thickness and dielectric constant k can be written as following:

$k=C_{ox}\ t_{ox}$,where k is the dielectric constant, C_{ox} is the capacitanc per unit area, and t_{ox} is the thickness of the oxide. High-k dielectric refers to a material with high dielectric constant k compared to silicon dioxide (k=3.9). Investigation of high-k dielectric materials has drawn much attention because of its widely usage in semiconductor industry such as gate dielectric in Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), and capacitors in Dynamic Random-Access Memory (DRAM).

1.2 Gate dielectric in Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

"MOSFET" stands for Metal Oxide Field Effect Transistor. It is a transistor used for amplifying or switching electronic signals. MOSFETs are widely used in the communication and computer industries. A MOSFET consists of a drain, a source, and a metal (or poly-Si) gate on top of a conductive substrate. As shown in Fig.1, the n-type MOSFET has two n-type source and drain, and a p-type substrate (opposite for p-type MOSFET). The two n-type regions are isolated from the p-type substrate, which prevents the current flow between the source and drain. However, by applying a voltage at the gate electrode (V_{GS}), an n-type conductive inversion channel layer will appear between the source and drain, and make it possible for the current flow. The distance

between the source and the drain is defined as channel length (L), which is one of the key parameters for the behavior of a MOSFET. An insulating gate dielectric is used to separate the gate from the substrate, and it has been one of the most important parts in MOSFETs. The drain current (I_D) of a MOSFET is proportional to the capacitance of gate dielectric, and can be expressed as follows:

$I_D \propto C_{ox} \propto k /(t_{ox} L)$, where C_{ox} represents the capacitance of the oxide, k represents the dielectric constant of the oxide, t_{ox} represents the thickness of the oxide, and L is the gate length. As a result, increasing the k value, and decreasing the oxide thickness and gate length can increase the drain current (I_D). However, short-channel effect (as the channel length shrinks, the gate gradually loses the ability to control the channel current, causing the variation of threshold voltage) limits the continuous shrinkage of gate length. As shown in Fig 2, reducing the gate dielectric thickness will increase gate current density, which is desirable for maximizing circuit speed. However, as the thickness of traditional gate dielectric material SiO_2 scales below 2 nm, the tunneling leakage current increases drastically. In order to reduce the tunneling leakage current while remaining a high capacitance of gate dielectric, replacing the traditional SiO_2 with thicker high-k dielectric materials is therefore a promising way to increase gate current density, and maximizing device speed.

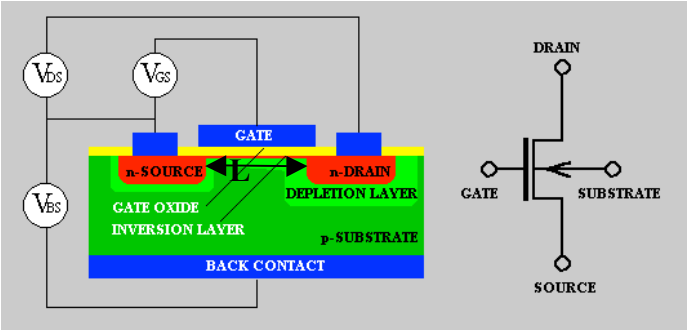


Fig. 1 The basic structure of an n-type MOSFET [1]

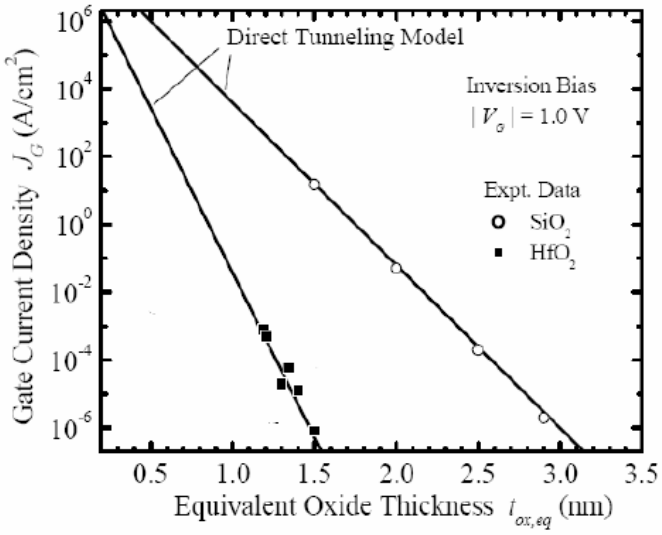


Fig. 2 Relationship between equivalent oxide thickness and gate current density [2]

1.3 Capacitors in Dynamic Random-Access Memory (DRAM)

Another application of high-k dielectric in semiconductor industry is the capacitors in Dynamic Random-Access Memory (DRAM). DRAM is a type of memories that stores every bit in separated charged or discharged capacitors (as "0" or "1") (Fig. 3). In order to increase the capacity of DRAM, memory cells must be scaled down while remaining certain charge level for reliable read out. To keep the high capacitance, one of the approaches is to scale down the

thickness of dielectric. However, tunneling leakage current limits this approach. Alternatively, the integration of high-k dielectric can increase the capacitance while limiting the leakage current by making a thicker dielectric. As a result, the key parameters to be optimized for the dielectric in DRAM are high dielectric constant and low leakage current, and high-k materials seem to be the perfect solution to it. It is worth noticing that in order to minimize the leakage current while maximizing the dielectric constant, a trade-off between crystalline structure and amorphous structure has to be carefully considered. Although it is possible to have a higher dielectric constant with a crystalline film, the grain boundaries can act as extra leakage paths.

1.4 Requirements of gate dielectric in MOSFET

Gate dielectric in MOSFET is one of the most important applications of high-k dielectric. A viable high-k material for gate dielectric application in MOSFETs must have a dielectric constant around 10~30, must have a bandgap above 5 eV to provide a large enough barrier height to avoid excessive leakage current, must be thermally stable within the thermal budget (e.g. 1000°C for 0.1-10 s) in processing, and must be amorphous materials after device integration rather than crystalline materials to avoid non-uniform electrical field on the channel layer [3]. In order to continue Moore's Law (a prediction of the number of transistor per unit area will double every 18 months or so by Gordon Moore), MOSFET must be scaled down. The gate dielectric thickness is therefore scaled down to be comparable with the device dimension, and reduce short-channel effect. A high-dielectric-constant material could achieve the same capacitance with a larger thickness, which prevents tunneling leakage current. The contact property between gate dielectric and Si substrate is also essential in MOSFET. The local bonding at Si/gate dielectric interface will influence the band offset, and affect leakage current

consequently. Charge trapping/detrapping process at the interface will also cause instability of electrical performance.

1.5 Need for high-k dielectric in MOSFET

One of the major limitations in reducing oxide thickness is based on the following tunneling current density equation:

$$j = \frac{\rho_m(E_t)}{V}\{ f_m(E_t)\,[1 - f_i(E_t)] - f_i(E_t)\,[1 - f_m(E_t)]\}\frac{8\pi\hbar l}{E_t}\left(\int dS \cdot j_{if}\right)^2 \ \mathrm{A/cm^2}$$

where j is the tunneling current density, $\rho_m(E_t)$ is the number of allowed quantum states on the equal-energy surface in the reciprocal space of the electrode. V, ħ, l, $f_m(E_t)$, and $f_i(E_t)$ are the volume of the electrode, the reduced Planck's constant, the thickness of the electrode, and the Fermi-Dirac distribution of electrons designating the occupancy of an energy state of E_t in the electrode and insulator, respectively [3]. In order to limit the tunneling current level with the required thickness for low-power applications, tremendous efforts have been made to improve the quality of traditional SiO_2 dielectric. However, the fundamental thickness limitation of SiO_2 (~1.2 nm) has been reached several years ago based on the tunneling current density equation. Fortunately, a thicker oxide thickness can be made to achieve the same gate current density with a high-k dielectric, and therefore the tunneling current issue can be reduced.

Because of the widely usage of high-k dielectric in semiconductor industry, investigation of a promising candidate of high-k dielectric materials has been a major filed in materials science.

For the applications of gate dielectric in MOSFET and capacitors in DRAM, tantalum oxide is one of the strongest candidates because of its high dielectric constant, low leakage current, high

breakdown field, and excellent step coverage characteristics. However, several factors still affect the performance of Ta_2O_5 as a dielectric in MOSFET and DRAM. These include film microstructure, stoichiometry, band offset, Ta_2O_5/Si interface, bulk defects, and crystallization effect [4].

1.6 Background of tantalum oxide

Tantalum oxide or tantalum pentoxide Ta_2O_5 is an inert material with large band gap about 4.5 eV, a dielectric constant from 20 to 40 depending on the deposition methods and post annealing conditions, a crystallization temperature around 600-700 °C, a high refractive index of 2.2 at 633 nm. It almost doesn't absorb light ranging from 300nm up to 2.0μm wavelengths, so it can be used in antireflective coatings for solar cells [5]. The k values of Ta oxides vary with synthesis methods. For amorphous Ta oxides, a k value of 22 of Ta oxide prepared by reactive sputtering was reported by S.C. Barron in 2009 [20]. R. A. B. Devine et. al. reported a k value of 24-25 of Ta oxide prepared by CVD [21]. G. S. Oehrlein et. al. reported a k value of 22-30 of Ta oxide by thermal oxidation [22]. A k value of 25 of Ta oxide by Atomic Layer Epitaxy (ALE) was reported by K. Kukli et. al. in 1996 [23]. Generally the k values of crystalline Ta oxides are higher than amorphous Ta oxides. For example, a k value of 52 of crystalline Ta oxide was achieved by sputtering followed with rapid thermal annealing [24]. The as-deposited tantalum oxide is usually amorphous at room temperature. At elevated temperatures, crystalline β-Ta_2O_5 and α-Ta_2O_5 phases were obtained around 600-700 °C, and 1000-1360 °C. The overall crystal structure is orthorhombic in both cases. It is chemically stable, and it is only soluble in concentrated hydrogen fluoride solutions. It is also a useful corrosion-resistant coating material due to its chemical stability [4, 5]

Among various applications of tantalum oxide, one of the greatest potential of tantalum oxide is to replace the traditional SiO_2 in DRAM and MOSFET. SiO_2 has been known to be the nearly perfect dielectric due to its superior interface properties with Si substrate. The only drawback of SiO_2 that restrains its application is the low dielectric constant (k~3.9). And it has become a major issue as the dimension of electronic devices becomes smaller and smaller. The reason that SiO_2 has a lower dielectric constant compared to high-k dielectrics (e.g. Ta_2O_5) is that SiO_2 has a lower polarizability. Lower polarizability implies stronger bonding, and a stronger bonding implies a larger separation between bonding and antibonding energies. Since the bandgap of SiO_2 (~9 eV) is larger than most of the high-k dielectrics (e.g. the bandgap of Ta_2O_5 is about 4.5 eV), SiO_2 has a relatively low dielectric constant. Although tantalum oxide has many attractive advantages as described above, it still has some weak spots.

The Si/Ta_2O_5 interface is not as perfect as Si/SiO_2 interface, and low-k interfacial layers are usually obtained between Ta_2O_5 and silicon substrate as shown in Fig. 4. The local bonding and defects at the interface will modify barrier height and trap carriers. These interfacial layers may deteriorate the equivalent dielectric constant, leakage current, and carrier mobility. Another drawback of tantalum oxide is its relatively low bandgap (about 4.5 eV). Generally it is a trade-off between dielectric constant and energy bandgap since higher polarizability (higher dielectric constant) implies weaker bonding (smaller bandgap) as shown in Fig. 5. A large bandgap can ensure enough barrier height to reduce leakage current. Fortunately, Ta_2O_5 capacitors still exhibit up to several orders of magnitude lower leakage current than SiO_2. High temperature processing is sometimes unavoidable in semiconductor industry, and this leads to another challenge of tantalum oxide: amorphous stability. Tantalum oxide usually crystallizes above 600 °C [5,10], and this restrains some of the thermal processes. Typically crystallization is an undesirable

feature because the grain boundaries can provide extra current leakage paths, and introduce non-uniform potential for moving carriers. Although crystalline tantalum oxide usually has a higher dielectric constant, a larger leakage current and carrier scattering issue also come with it. It is essential to have a stable amorphous structure of gate dielectric in MOSFET.

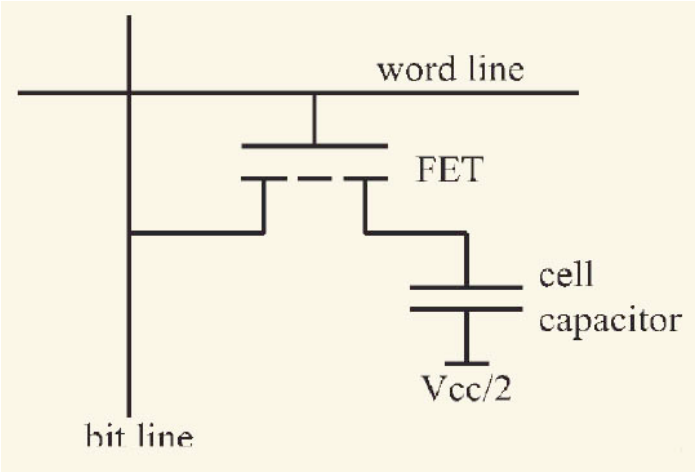


Fig. 3 Basic cell structure of a DRAM [19]

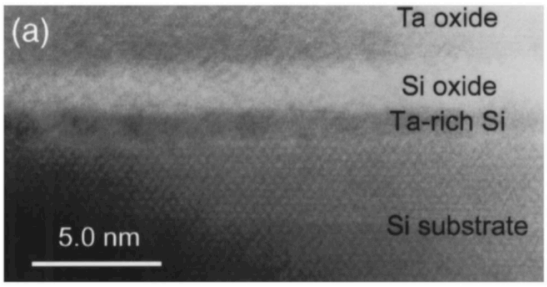


Fig. 4 Cross-sectional TEM of tantalum oxide/silicon interface [5]

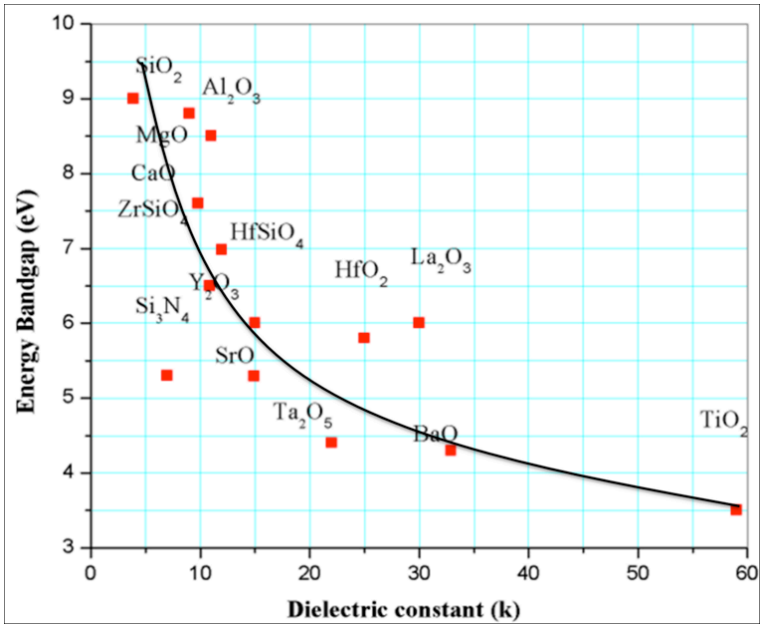


Fig. 5 Bandgap v.s. dielectric constant (k) of several high-k materials [18]

1.7 Synthesis of tantalum oxide films

Tantalum oxide can be synthesized by various methods including Chemical Vapor Deposition (CVD), Evaporation, Sputtering, and Pulsed Laser Deposition (PLD).

CVD usually is widely used in semiconductor industry. It favors large area growth, good composition control, good film uniformity, and excellent step coverage with very high aspect ratio trench. However, restricted deposition temperature, and impurity control are the main drawbacks. Evaporation is a simple and common technique in thin film deposition where the target material is evaporated in vacuum, and condensed on the substrate. The thickness control and step coverage are its main challenges. Sputtering is a physical deposition method where target atoms are bombarded by plasma. It has controllable growth, low temperature process, and

good compositional consistency. However, plasma induced damage can be an important issue in high-quality thin film deposition.

1.8 Pulsed Laser Deposition (PLD)

PLD is a physical vapor deposition technique, and it well known in producing high-quality films in low temperature where a high-power laser strikes a target material that is to be deposited. As shown in Fig. 6, the vaporized target material expands to the surrounding vacuum in a form of plasma (plume) containing atoms, molecules, ions, electrons, particulates, and clusters. Then the plasma (plume) deposits the vaporized material as a thin film on a substrate. In order to avoid trench formation during deposition, the target is rotated, and the laser beam is rastered. Substrate temperature and gas environment can also be controlled. Although PLD has the advantage of process simplicity, flexibility, and high quality, the deposition of uniform and large-area thin films, and particulates in the films are its major issue [6].

In spite of the simple set up of PLD, the process of laser-target interaction and thin film growth can be complicated. The process of PLD can be divided into four steps: Ablation of target materials and plasma (plume) creation, plasma (plume) dynamic, deposition of vaporized materials on the substrate, and nucleation and growth of target materials on the substrate [7].

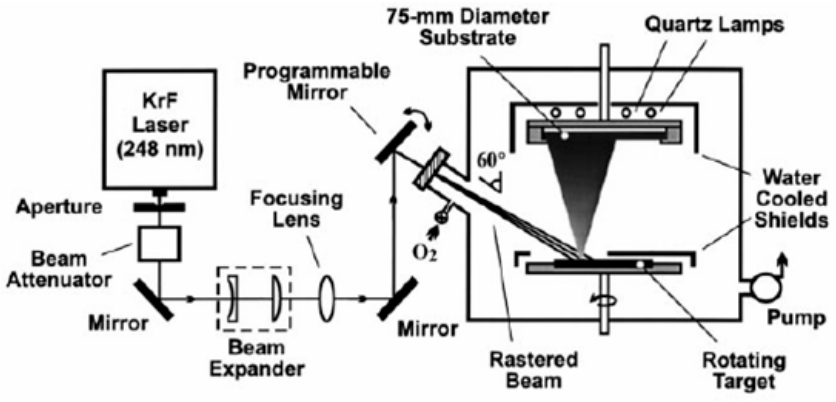


Fig. 6 Schematic of PLD instrument set-up [6]

Ablation of target materials

The process of ablation of target materials and plasma creation during laser-target material interaction is complicated. The removal of atoms from the target material is confined in the surface region of the target during non-equilibrium state. The incident laser penetrates the target in a depth depending on the laser power and the refraction index of the target material. Typically the penetration depth is in the region of 10 nm in most cases. The strong electrical field produced by the laser will remove electrons from the bulk material of the penetrated region in picosecond or nanosecond. Surface defects such as cracks, nodules, and voids will increase the electrical field, and enhance this process. The ejected free electrons oscillate with the electrical field, and collide with the atoms in target materials. The surface of the target material is heated up and the material is vaporized by the energy transfer from the energetic electrons to the lattice of the target material.

Plasma (plume) dynamic

The vaporized material expands in a form of plasma in a direction normal to the target surface toward the substrate. The distribution of the plasma density is similar to Gaussian distribution, and the distribution is affected by environment pressure in the chamber. The energetic species in the plasma will slow down due to the increase of the environment pressure.

Deposition of vaporized materials on the substrate

The deposition of vaporized materials on the substrate is critical in determining the quality of the thin film. The energetic ablated species bombard on the substrate, and may cause damage on the surface, and induce defects on the film. When the condensation rate of the target material is high enough, a thermal equilibrium between the film growth and the expense of the flow of the energetic species can be reached.

Nucleation and growth of target materials on the substrate

The nucleation and growth processes are affected by several factors, including laser energy, substrate temperature, substrate surface, and background pressure. The laser energy will affect the ionization degree of the target material, film quality, stoichiometry, and the deposition flux. Generally, the nucleation density increases with increasing deposition flux. The substrate temperature is an important factor in nucleation density. Generally the nucleation density decreases with increasing substrate temperature. Substrate cleanness and roughness will affect the film quality a lot. Dust on substrate can cause pinholes in the film, and deteriorate the property of the thin film. In oxide deposition, oxygen background is essential to ensure stoichiometry of the thin film. The background pressure will also directly affect the kinetic energy of the ablated target material.

1.9 Mixed-oxide dielectric

Mixed-oxide dielectric has been a plausible strategy to modify the bandgap, increase the dielectric constant and stabilize the amorphous structure [8, 9]. By adding a third element in the metal oxide film, the amorphous phase can be stabilized, which breaks the thermodynamic limit in thermal processing, and a higher dielectric constant may be obtained. There are several limitations of conventional high-k dielectrics in MOSFETs. For instance, Ta_2O_5 has been widely used as a high-k dielectric in capacitors of memory chips. However, it has a major drawback for gate oxide application in MOSFETs because of its low crystalline temperature (600 -700 °C), low-k and low-quality interface with Si, small band gap (4.5 eV) and small electron band offset (0.3 eV) with respect to Si [9]. The addition of a third element will also change the property of the interfacial layer, and change the electrical properties as a result. Some of these drawbacks can be reduced by process techniques. For instance, the low-k and low-quality interface between high-k dielectric and silicon can be thinned by dynamic annealing process, such as short time exposure to high temperature in low oxygen pressure background [9]. However, the process the relatively hard to control, and it is complicated. As a result, the thermodynamic limit has to be broken in high-k dielectrics such as Ta_2O_5 in order to further increase its potential for high-k dielectric application in MOSFET or DRAM.

Some successful results have been obtained in tantalum-based mixed-oxides. For example, the addition of a third element will disrupt the long-range order formation, and thus stabilize the amorphous structure. Fig. 7 shows the XRD patterns of several tantalum-based mixed-oxides, including Ta-Al-O, Ta-Si-O, and Ta-Ti-O after 700 °C annealing. The pure Ta_2O_5 shows β-Ta_2O_5 peaks after annealing. Ta-Al-O and Ta-Si-O stay amorphous after annealing. The Ta-Ti-O shows only TiO_2 peaks, and it does not contain any crystalline Ta_2O_5. Another example of Ta-

Zr-O also shows over 800 °C crystallization temperature, which is 200 °C higher than the crystallization temperature of pure Ta_2O_5 in Fig. 8.

The additional element can also have effect on the bond structure. Fig. 9 shows the XPS spectra of Ta-Hf-O thin films with various Hf concentrations. The binding energy of Ta $4f_{7/2}$ decreases with increasing Hf concentration. And the binding energy of Hf $4f_{7/2}$ increases with increasing Ta concentration. These shifts are due to charge transfer. Because the average bond ionicity of HfO_2 is higher than that of Ta_2O_5 (0.68 vs. 0.61), Hf will be more ionic and Ta will be less ionic in Ta-Hf-O thin film. Plus, O and Ta have higher electron negativity than that of Hf. As a result, the negative partial charge of O increases, and the positive partial charge of Ta and Hf decrease with increasing Hf concentration.

The interfacial layer between the oxide and Si substrate is also affected by the addition of third element. Fig. 10 shows the TEM cross-section images of the Ta-Hf-O thin films with various Hf concentrations. It is found that all the interfacial layers are amorphous, and the interfacial layer is thinner with higher Hf concentration. It is suggested that the addition of Hf slows the O_2 diffusion, and reduces the oxidation of Si.

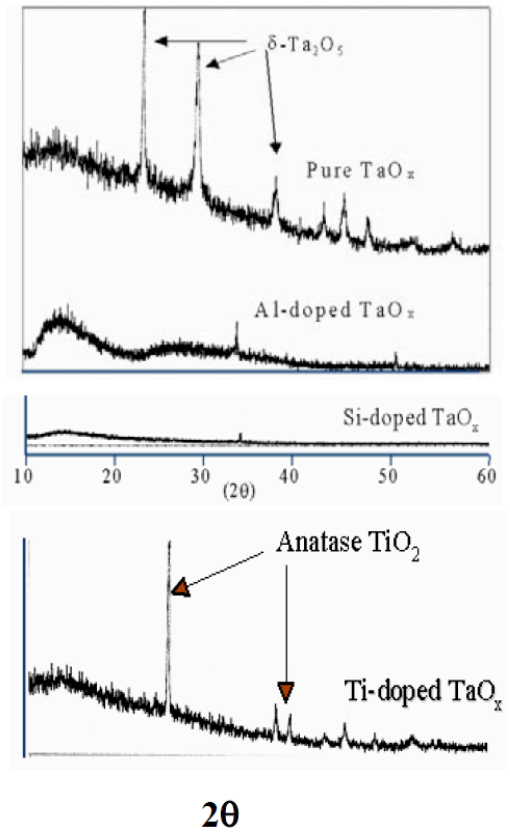


Fig. 7 XRD patterns of various tantalum-based mixed-oxide [9]

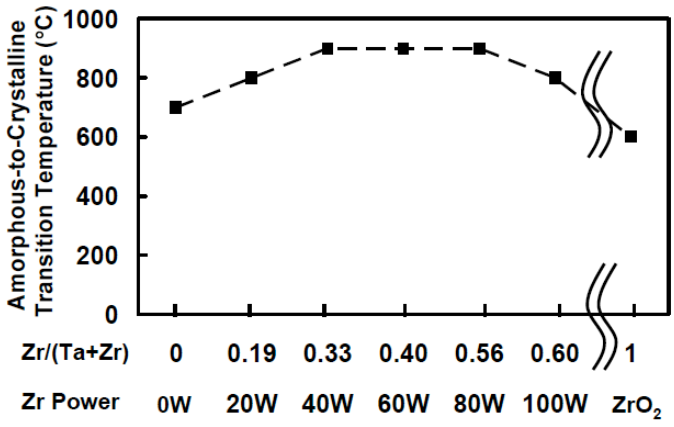


Fig. 8 The crystallization temperature of Ta-Zr-O as a function of Zr concentration [9]

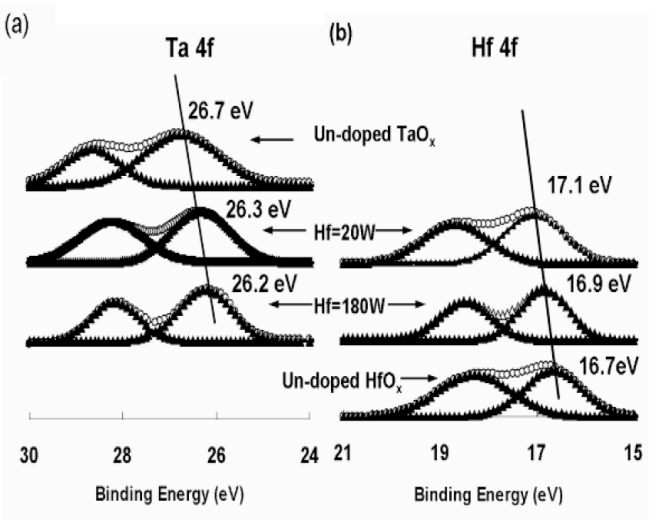


Fig. 9 The XPS spectra of Ta 4f and Hf 4f in Ta-Hf-O thin film with various Hf concentration [9]

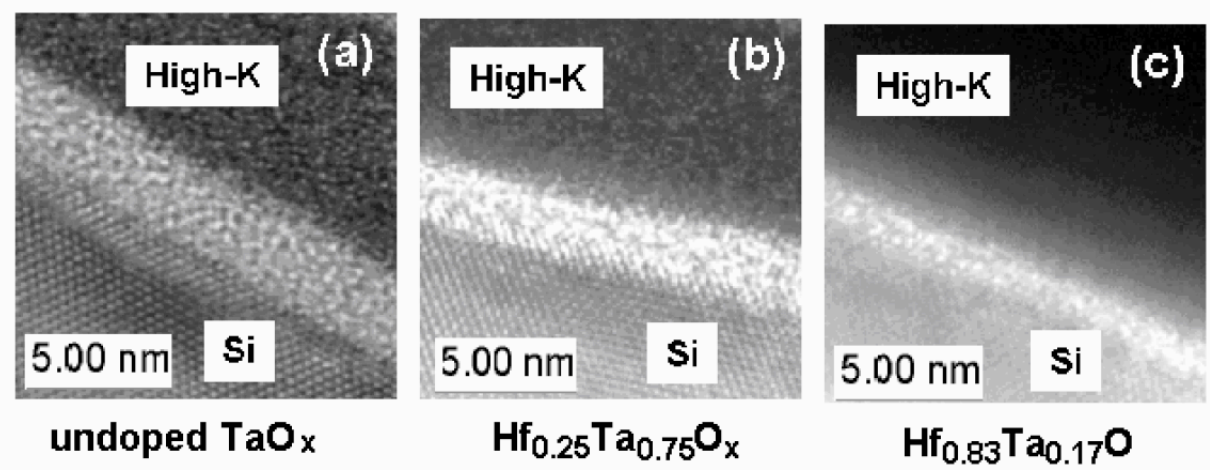


Fig. 10 TEM cross-section images of Ta-Hf-O thin films with various Hf concentrations [9]

Another advantage of mixed-oxide is the possibility of dielectric enhancement behavior. Dielectric enhancement is described as the increase in the dielectric constant above the expected value from the linear interpolation of the values of the endmembers [8]. Taro Naoi et al. has shown the dielectric enhancement in amorphous Ta-Ge-O system in 2012 with co-sputtering

technique [8]. However, the dielectric property of this system hasn't been studied with PLD technique.

1.10 Ge-incorporated tantalum oxide

In this study, Ge is chosen to substitute for Ta to prepare Ta-Ge-O thin film. The reason that Ge is used in tantalum-based mixed-oxide is the opportunity of Ge to replace Si because of its higher carrier mobility [11]. Tantalum oxide is now a promising capacitor material in production, and tantalum oxide, unlike the unstable interface formation between Ta_2O_5 and Si, is stable in contact with unoxidized Ge. In 2012, it is reported that the relative dielectric constant of $Ta_xGe_{1-x}O_y$ mix oxide thin film can be increased by 40 % over the value obtained for pure amorphous Ta_2O_5 films with only 3% substitution of Ge for Ta [8]. As shown in Fig. 11, the dielectric enhancement occurred in the Ta-Ge-O system when the Ta cation fraction is above 75%. And the dielectric constant rises to 30.5, a 40 % improvement compared to bare amorphous Ta_2O_5 (k=22) when 3% Ta cation is replaced by Ge cation. From the refractive index analysis over different Ta cation fractions, the increase of dielectric constant is mainly due to the enhancement in the ionic polarizability instead of the electronic polarizability (Fig. 12). Even though there are some promising properties of gate dielectric application in mix oxide systems, the underlying mechanisms for these properties are still not clear. Therefore, it is necessary to keep conducting research in this highly potential system for the next generation MOSFETs.

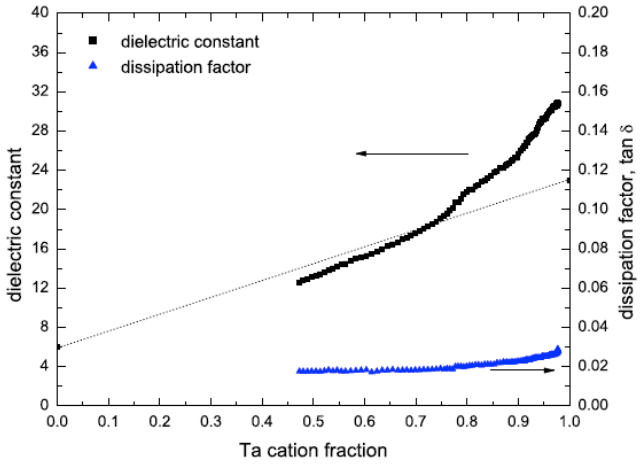


Fig. 11 Dielectric constant variation in Ta-Ge-O mix oxide with various Ta cation fractions [8]

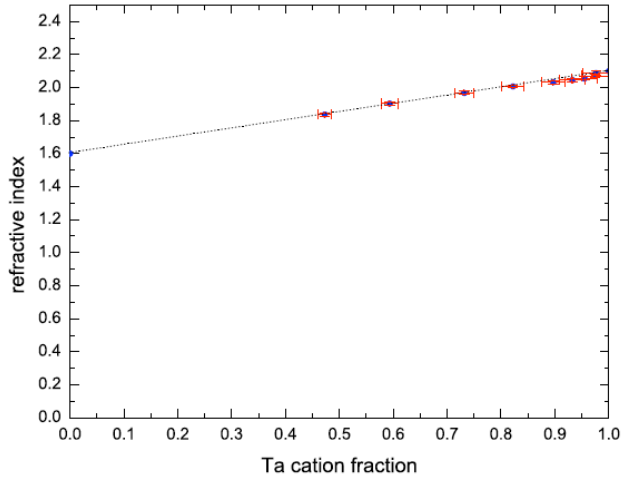


Fig. 12 Refractive index of Ta-Ge-O mix oxide with various Ta cation fractions [8]

2. Experimental

2.1 Sample preparation

In order to test the dielectric property of the thin films, samples are prepared in Metal-Insulator-Metal (MIM) structure on Si substrate. As shown in Fig. 13, a 30 nm Cr layer is first evaporated on the Si substrate as an adhesion layer for the following Pt layer as a bottom electrode. A 35 nm Pt layer is then evaporated on the Cr layer. The Cr/Pt under-layer is a vital component in the electrical characterization. The tantalum oxide and Ge-incorporated tantalum oxide are deposited with PLD on Cr/Pt under-layer. Additionally, certain samples have a line of Apiezon-W (referred to as black wax hereafter) on the center of the silicon substrates before oxide deposition (Fig. 14). The black wax will be dissolved later after the deposition in order to reveal the cross-section for the thickness measurement with profilometer (Fig. 15). Pt dots with diameter of 200 μm, and thickness of 35 nm are evaporated through a shadow mask on the tantalum-based oxide as top electrodes (Fig. 13).

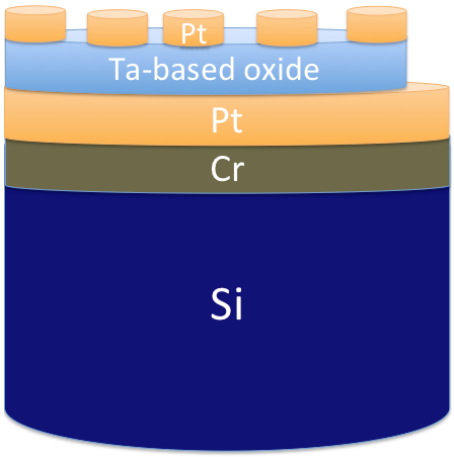


Fig. 13 Schematic of the MIM structure of the sample

Fig. 14 Black wax on Si substrate before oxide deposition [12]

Fig. 15 Oxide sample after removing the underneath black wax in the center line [13]

2.2 Pulsed laser deposition of tantalum oxide films and Ge-incorporated tantalum oxide films

Oxides are deposited by Neocera Ex200 PLD system with KrF 248 nm excimer laser source operated at 23 V (150 J/cm^2) and 10 Hz shot rate. 1-inch Ta target (0.250 inches thick, 99.99%), and 2-inch Ge sputtering target are used in the system. Before deposition, 2,000 laser shots are applied as pre-ablation shots to clean the impurities on the surface of the target. For pure tantalum oxide, 23,000 laser shots are applied under various oxygen partial pressure

environments from 8 mTorr to 100 mTorr, and various deposition temperatures from room temperature to 400 °C (as shown in Table 1). The base pressure of the chamber is controlled at 3 μTorr, and the oxygen partial pressure is controlled by altering the oxygen flow rate or the pumping rate. Si substrate is placed upside down into the holder, and the oxide film is deposited from the direction perpendicular to the substrate as shown in Fig. 5. The targets are rotated about the center of the target in 10-11 ° /s, and rastered in 9° for 1-inch Ta target, and 17° for 2-inch Ge target about the center of the target holding carousel. The raster angle is to ensure an even removal of materials through the surface of the target. Before deposition, the glass window attached on the chamber where laser goes through is polished by μm diamond paste, and cleaned with acetone and isopropyl alcohol.

100 mTorr	✦	—	—
60 mTorr	✦	—	—
30 mTorr	✦	✦	✦
17.5 mTorr	✦	—	—
8 mTorr	✦	✦	—
Oxygen Pressure / Deposition Temp.	Room temperature	250 °C	400 °C

Table 1 Matrix of pure tantalum oxide sample depositions (the star symbol means the sample is prepared at that condition)

Ge-incorporated tantalum oxide is prepared by alternative deposition of Ta and Ge monolayer with certain shot ratio. Fig. 16 illustrates the concept of depositing Ge-incorporated tantalum oxide. Based on the film thickness profiles of pure Ta oxide and pure Ge oxide (Fig. 17) with profilometer measurement, the low Ta concentration sample (90% of Ta, and 10% of Ge at the center of the wafer; hereafter referred to as low Ta concentration sample), and the high Ta concentration sample (95% of Ta, and 5% of Ge at the center of the wafer; hereafter referred to as high Ta concentration sample) are prepared with Ge to Ta shot ratio of 2:144 and 1:152 to achieve a peak thickness estimation to 100 nm. It should be noticed that since the Ge-incorporated tantalum oxide is prepared by rotation of the sample by 180 ° during deposition to achieve an alternatively deposition (as shown in Fig. 16), the Ge oxide peak concentration will be at the other side of the wafer compared to Ta oxide peak in Fig. 17. The deposition rate

profile is also fit with the Lorentzian distribution [13]. The concentration profiles of these two Ge-incorporated tantalum oxide samples are then calculated as shown in Fig. 18. The error bounds are established based on the average fraction error of the data points [13]. The deposition is under oxygen partial pressure of 17.5 mTorr at room temperature based on the report in [12].

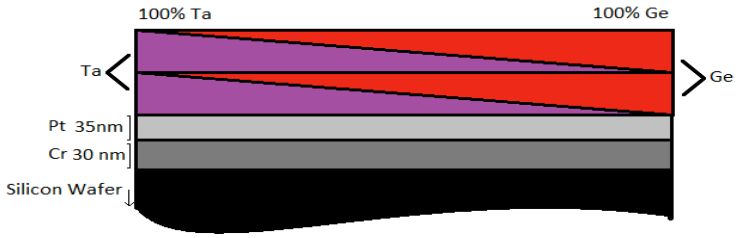


Fig. 16 Schematic of Ge-incorporated tantalum oxide (figure is created by Deborah DeLuca, Alexander Montelione, and Robert Newcomb in Cornell MSE senior lab)

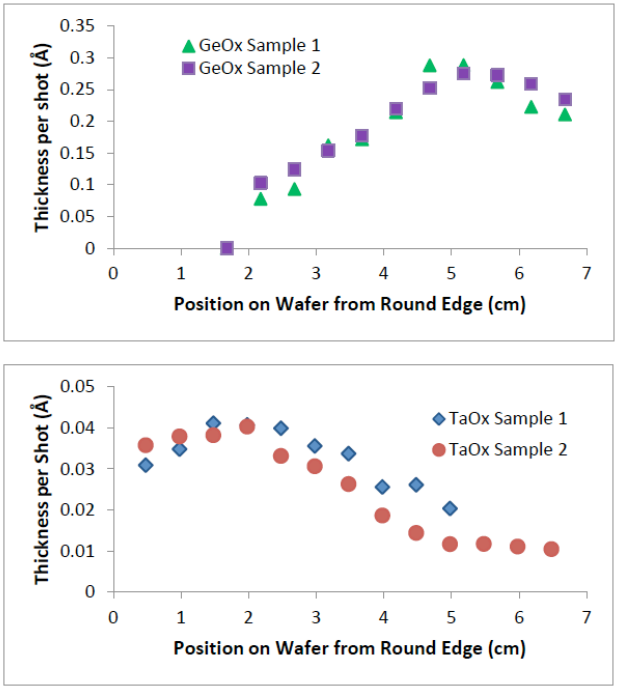


Fig. 17 The deposition profiles of pure Ta oxide and Ge oxide [13]

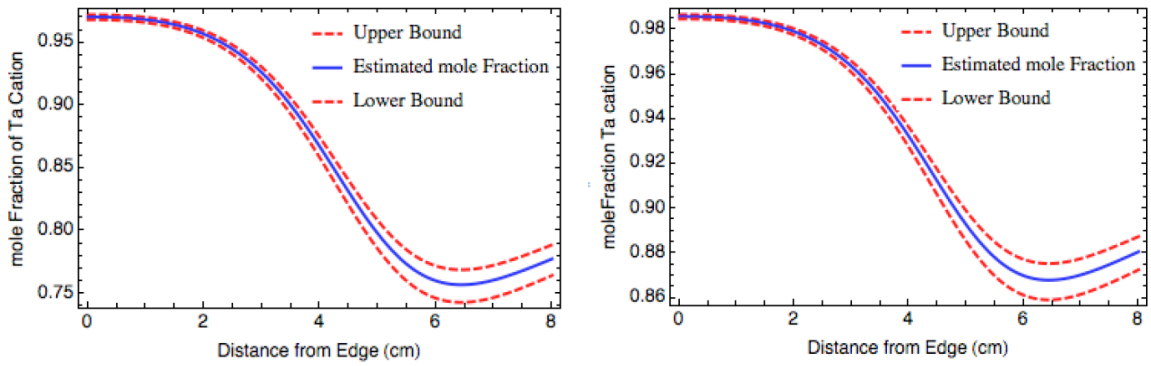


Fig. 18 Mole fraction profiles of Ge-incorporated tantalum oxides of low Ta concentration sample (left), and high Ta concentration sample (right) [13]

2.3 Electrical measurement-capacitance and dissipation factor

The capacitance and dissipation factor are measured at 10kHz (additional 1kHz, and 100kHz measurements for certain samples) by an LCR meter (HP 4284) and commercial probe station at 0.5Vac. Capacitance is a measure of the ability of a material to store electrical charges. A capacitor is usually made in the Metal-Insulator-Metal (MIM) structure, where the insulator serves as dielectric materials. It can be calculated if the geometry of the conductor and the property of the dielectric are known. For a parallel-plate capacitor with the area of electrode A, a thickness d of the dielectric material, and the dielectric constant k of the dielectric material, the capacitance C of the dielectric can be expressed as: $C = \varepsilon_0 k A / d$, where ε_0 is the vacuum permittivity $8.85*10^{-12}$ F/m. Dissipation is a measure of the energy loss rate in dielectric. The electrical energy dissipates in dielectric material usually in the form of heat. To quantify the energy loss in a dielectric, the dissipation factor is defined as the lost tangent ($\tan \delta$) of the dielectric constant: $\tan \delta = \mathrm{Im}(\varepsilon)/\mathrm{Re}(\varepsilon)$. For a high-quality capacitor, the dissipation factor and

capacitance doesn't show much frequency dependence, and the dissipation factor is about 1% to 2% for high-k materials [14].

2.4 Scanning Electron Microscope (SEM) morphology

Tescan-Mira3-FESEM is used for Scanning Electron Microscope (SEM) morphology analysis in this study. A 10 nm Au-Pd coating is deposited on the sample for enhancing the conductivity. Scanning Electron Microscope (SEM) is a type of electron microscope where a focused electron beam scans on the surface of the sample to create images. The electrons from the electron beam interact with the atoms in the sample, producing secondary electrons from the surface of the sample. The number of secondary electrons is a function of the angle between the electron beam and the surface. By scanning the electron beam, the surface morphology of the sample can be obtained. To avoid electron charging on the sample surface, an insulating material is usually coated with gold to enhance the conductivity. SEM can achieve a resolution of 1 nm, and the specimen can be observed in high vacuum, low vacuum or even in wet condition.

2.5 X-ray Photoelectron Spectroscopy (XPS) analysis

Surface Science Instrument SSX-100 is used for X-ray Photoelectron Spectroscopy (XPS) analysis in this study. X-ray Photoelectron Spectroscopy (XPS) is a surface analysis technique that measures the elemental composition, chemical state, and empirical formula. The spectra are obtained by irradiating X-ray on the material while measuring the kinetic energy and numbers of the electrons escape from the material surface from 0 to 10 nm from the top of the surface. The binding energy of the emitted electron is then calculated by the following relationship:

$E_{binding}=E_{photon}-(E_{kinetic}+\varphi)$, where $E_{binding}$ is the binding energy of the electron, E_{photon} is the energy of the photon of the X-ray, $E_{kinetic}$ is the kinetic energy of the emitted electron, and φ is the work function of the spectrometer. A schematic of the XPS physic is shown in Fig. 19. XPS requires very high vacuum conditions, typically 10^{-8} to 10^{-9} millibar. XPS generally detects all elements with atomic number greater than 3, and the analysis is very sensitive to the condition of material surface which strongly affect the number of escaped electrons.

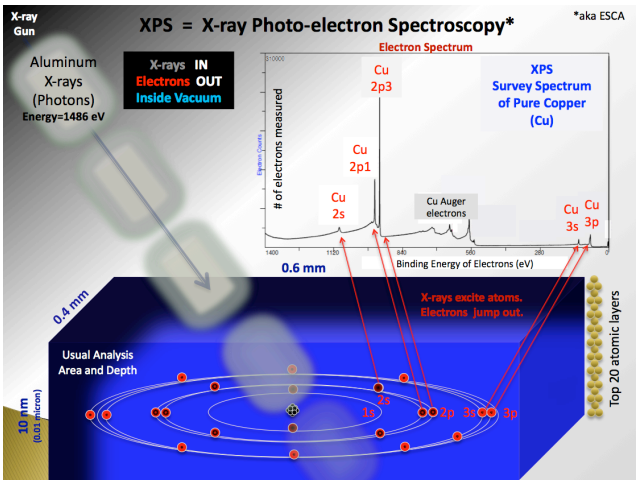


Fig. 19 A schematic of XPS physics (figure from Wikimedia Commons)

3. Results and Discussion

3.1 Pulsed Laser Deposition

Tantalum oxide, germanium oxide, and Ge-incorporated tantalum oxide thin films prepared by PLD show fringe patterns as seen in Fig. 20. The fringe patterns are characteristic of thin film interference, showing the distribution of oxide thin film. It should be noticed that the fringe patterns are not affected only by the materials, but also by deposition conditions which change the distribution profile of the thin film. Fig. 21 illustrates the fringe patterns of tantalum oxide thin films deposited at various oxygen partial pressures. It is obvious that the oxygen background during deposition changes the distribution of the oxide.

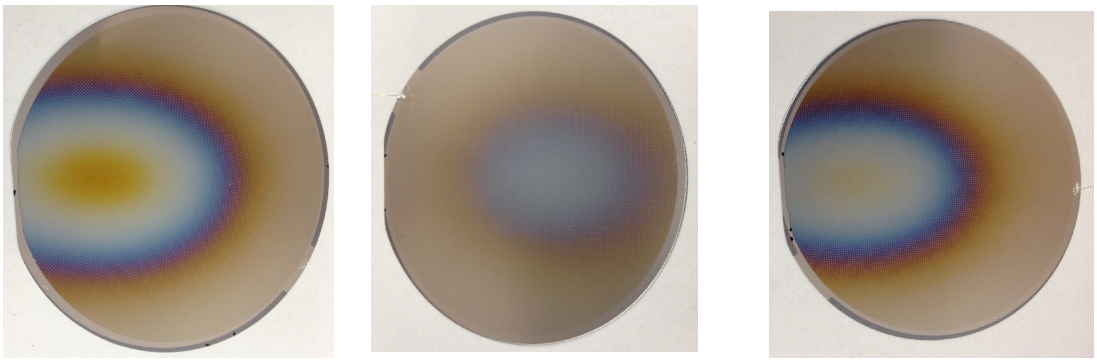


Fig. 20 Ta oxide, Ge oxide, and Ge-incorporated Ta oxide (from left to right) deposited at an oxygen partial pressure of 17.5 mTorr at room temperature showing fringe patterns

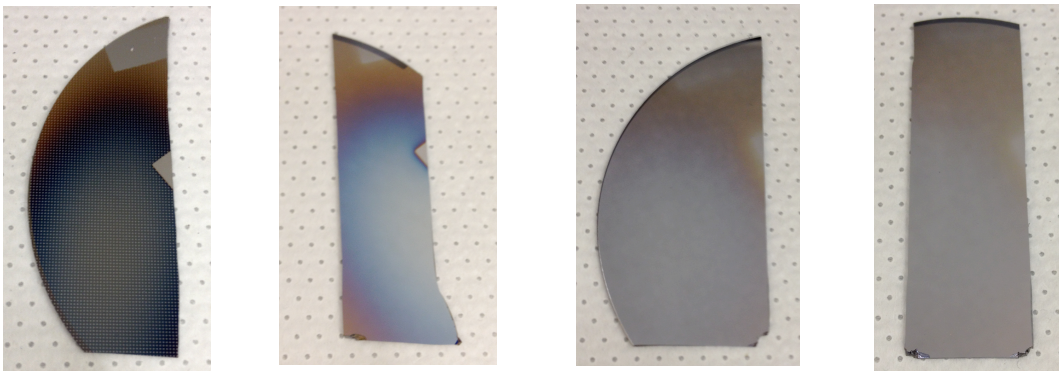
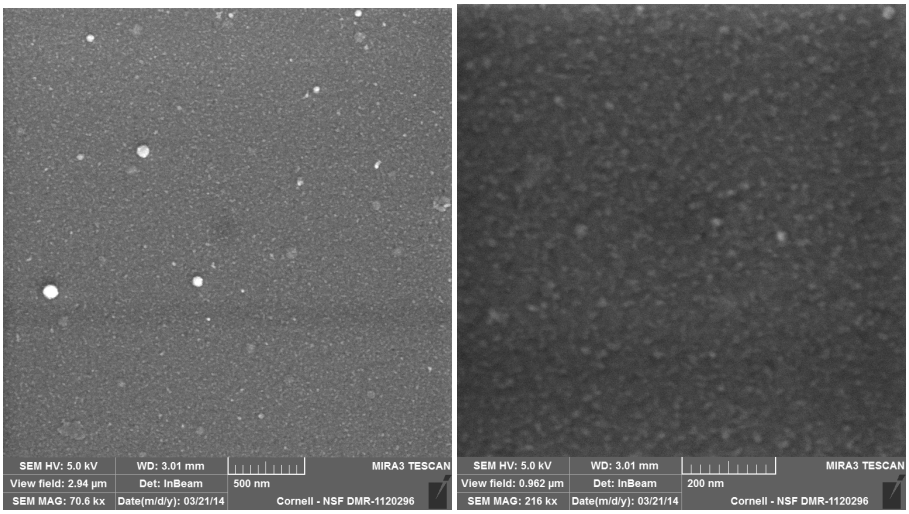


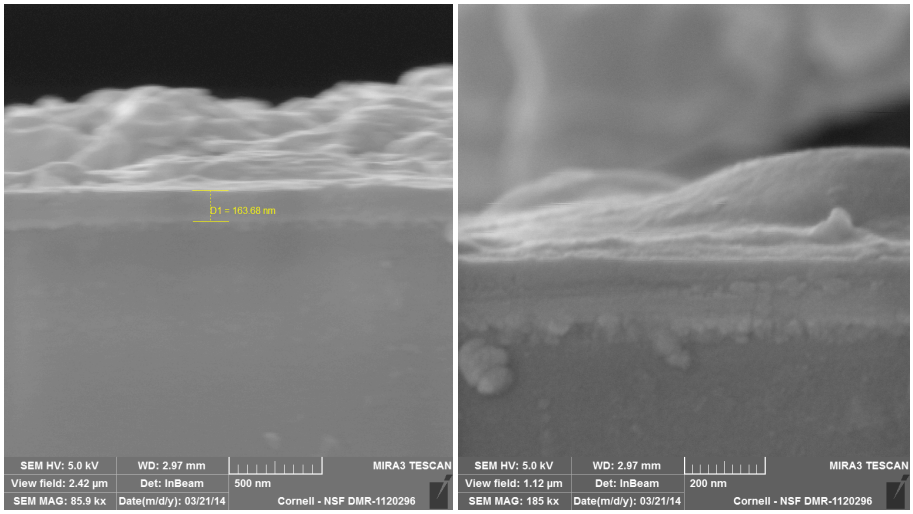
Fig. 21 Ta oxide deposited at oxygen partial pressures of 8mTorr, 30 mTorr, 60mTorr, and 100mTorr (from left to right) at room temperature showing fringe patterns

3.2 SEM morphology of tantalum oxide prepared by PLD

Fig. 22 shows the cross-section and top-view SEM images of the thickest region of tantalum oxide thin film deposited at an oxygen partial pressure of 17.5 mTorr at room temperature. In Fig. 22 (a), the clusters on the surface of the film are droplets splashed from laser spots on the target, which is known to be one of the characteristics in PLD [10]. The clusters can also be formed by low surface-mobility Ta atoms, which loss their kinetic energy during the flight from the target to the substrate. The cross-section image of thin film is shown in Fig. 22 (b). The tantalum oxide film thickness at the thickest region is confirmed to be around 150 nm (total thickness of 160 nm in the image minus 10 nm Au-Pd coating). The image also shows a good adhesion between tantalum oxide and Si substrate by PLD technique. Due to the limited resolution of SEM, the detail structure of the thin film such as porosity is not shown in the images.



(a)



(b)

Fig. 22 SEM top view images (a), and cross-section images (b) of the thickest region of tantalum oxide thin film deposited at an oxygen partial pressure of 17.5 mTorr at room temperature

Capacitance (F)
Dissipation Factor

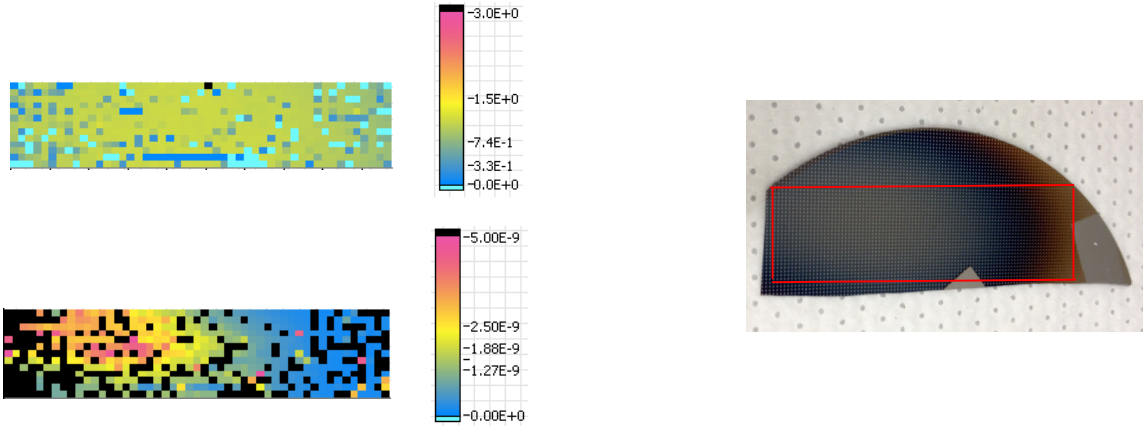
3.3 Electrical properties-deposition condition correlation of tantalum oxide

3.3.1 Effect of oxygen partial pressure

In order to investigate the effect of oxygen partial pressure during deposition on the electrical property of tantalum oxide, the capacitance and dissipation factor are measured at 10 kHz for samples deposited at oxygen partial pressures of 8 mTorr, 17.5 mTorr, 30 mTorr, 60 mTorr, and 100 mTorr at room temperature.

8 mTorr sample

Fig. 23 shows the heat map of capacitance and dissipation factor, and the corresponding measured region of the sample deposited at an oxygen partial pressure of 8 mTorr at room temperature. The overall capacitance is about $1.5*10^{-9}$ F among the entire measured region. The dissipation factor is measured to be about 1.5 ~2.0 at thick region, and 0.1~0.3 at thin region.



(a) (b)

Fig. 23 (a) Heat map of capacitance (F) (top) and dissipation factor (bottom), and (b) the corresponding measured region (red box) of Ta oxide deposited at an oxygen partial pressure of 8 mTorr at room temperature

17.5 mTorr sample

For the sample deposited at 17.5 mTorr oxygen partial pressure at room temperature, the heat map of capacitance and dissipation factor is shown in Fig. 24. The capacitance ranges from $5*10^{-10}$ F to $2*10^{-10}$ F through thick to thin region, and the dissipation factor is measured to be about 0.9~1.0 at thick region, and 0.02~0.03 at thin region.

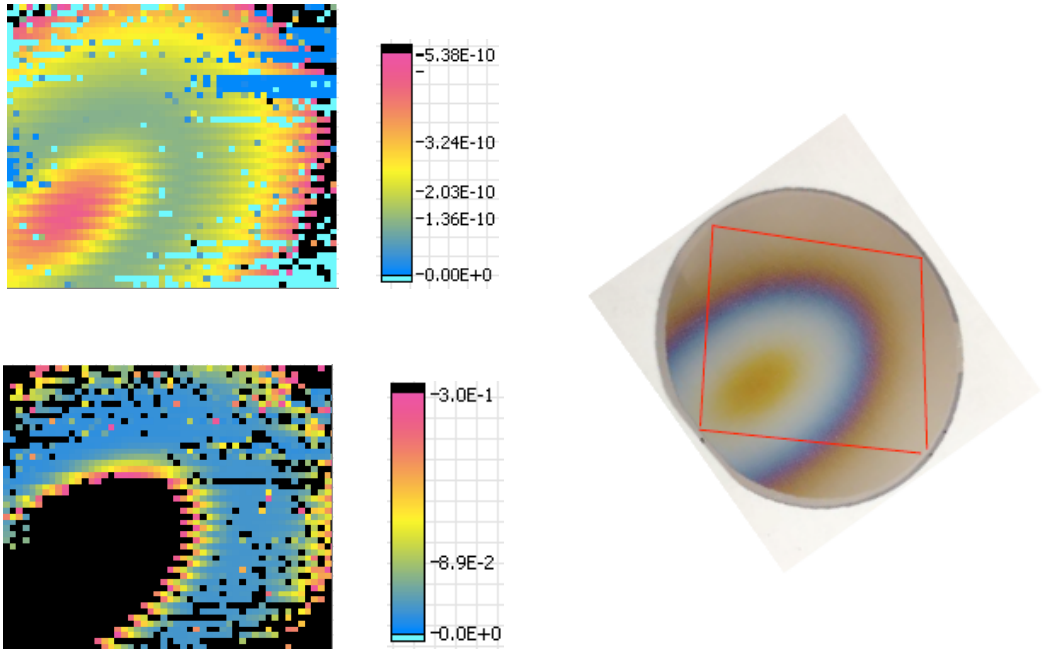
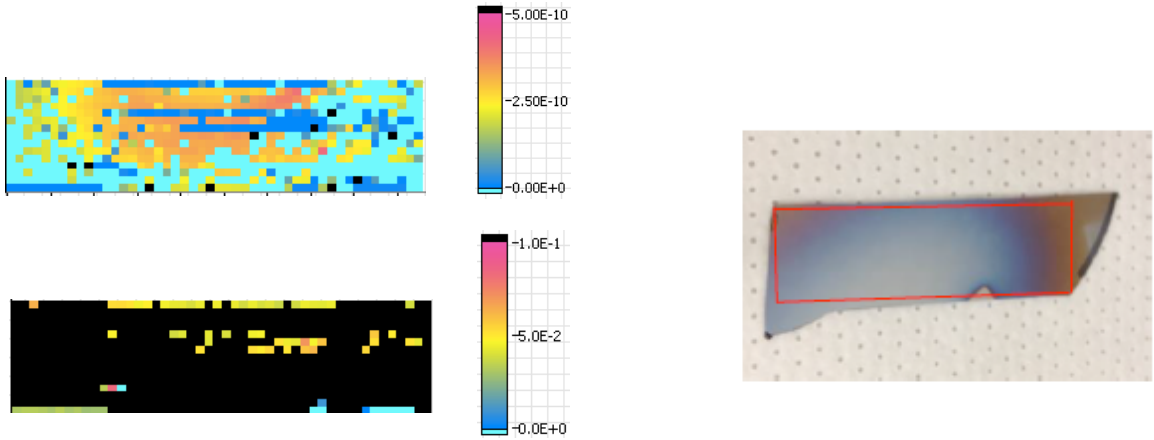


Fig. 24 (a) Heat map of capacitance (F) (top) and dissipation factor (bottom), and (b) the corresponding measured region (red box) of Ta oxide deposited at an oxygen partial pressure of 17.5 mTorr at room temperature

Capacitance (F)
Dissipation Factor

30 mTorr sample

Similarly, for the sample deposited at 30 mTorr oxygen partial pressure at room temperature, the heat map of capacitance and dissipation factor is shown in Fig. 25. The capacitance is about $3*10^{-10}$ F at thick region, and the dissipation factor is measured to be about 0.6~0.7 at thick region. It is worth noticing that the capacitors at thin region are all short-circuited for this sample. The short-circuited capacitors are caused by pinholes in the film. Pinholes are defects in the film caused by unclean substrate surface. With the extension through the thickness of the film, pinholes can lead to a conducting path through the dielectric, causing the short-circuited capacitors.

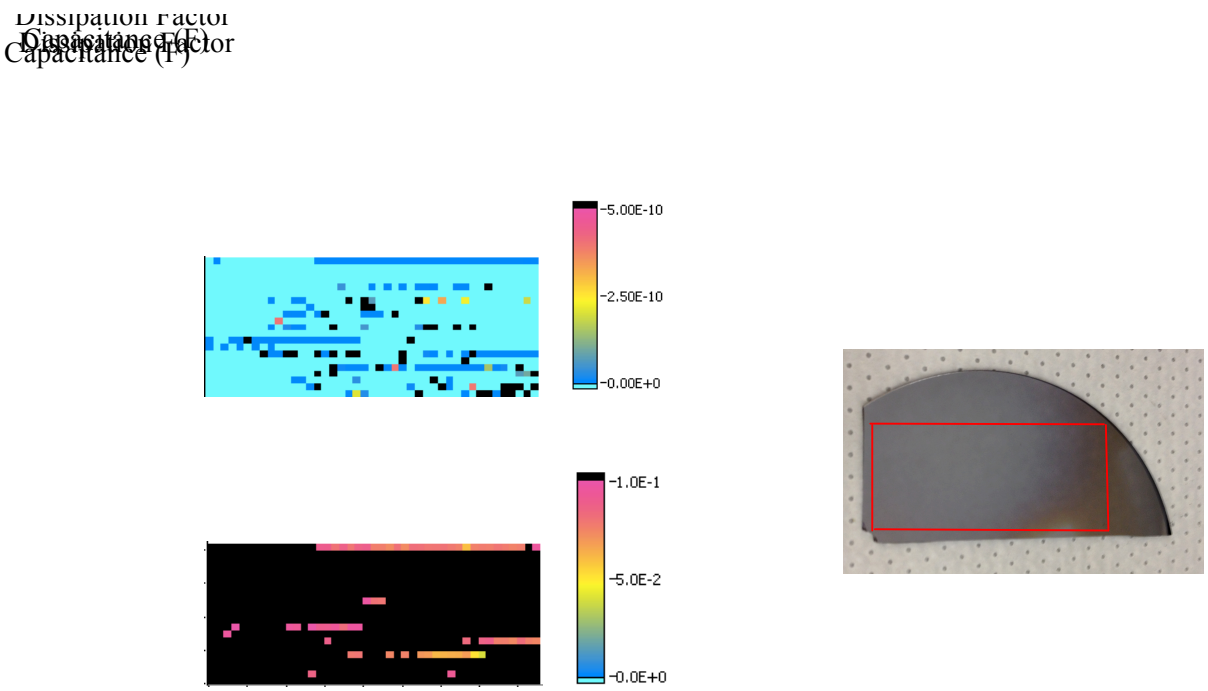


(a) (b)

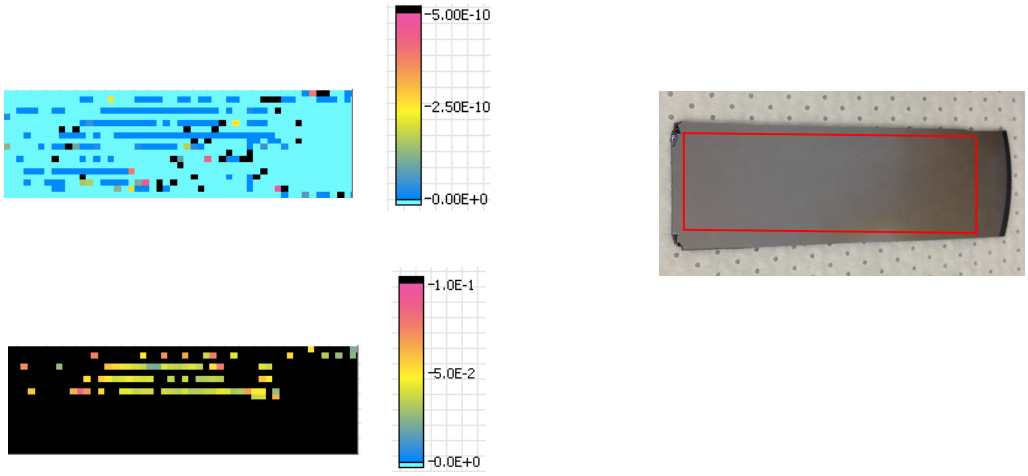
Fig. 25 (a) Heat map of capacitance (F) (top) and dissipation factor (bottom), and (b) the corresponding measured region (red box) of Ta oxide deposited at an oxygen partial pressure of 30 mTorr at room temperature

60 mTorr and 100 mTorr samples

Fig. 26 shows the heat map of capacitance and dissipation factor, and the corresponding measured region of the sample deposited at oxygen partial pressures of 60 mTorr (Fig. 26 a) and 100 mTorr (Fig. 26 b) at room temperature. It is clear to see that almost every capacitor on these two samples are short-circuited even at thick regions. The reason for the overall short-circuited capacitors is suggested to be the porous structure of Ta oxide deposited at high oxygen partial pressure background. The high oxygen partial pressure environment contains a lot of oxygen atoms. During the deposition, the ablated tantalum atoms collide with oxygen atoms in the background during the flight from the target to the substrate, and thus loss kinetic energy. The low energy tantalum atoms have a low surface mobility on the substrate, causing the porous structure of tantalum oxide during deposition. Water molecule or hydroxyl ions are absorbed into the film, creating a hopping conduction path. As a result, the capacitors are short-circuited in the tantalum oxide films deposited at high oxygen partial pressures of 60 mTorr and 100 mTorr.



(a)



(b)

Fig. 26 Heat map of capacitance (F) (top) and dissipation factor (bottom), and the corresponding measured region (red box) of Ta oxide deposited at an oxygen partial pressure of (a) 60 mTorr, and (b) 100 mTorr at room temperature

Tantalum oxide is formed by oxidation of the surface of the deposited film, and by the collision with oxygen atoms during the flight from the target to the substrate [10]. Therefore, more oxygen atoms in the background will provide more opportunities for oxidation. Table 2 summarizes the capacitance, dissipation factor, and estimated k values of tantalum oxides deposited at oxygen partial pressures from 8 mTorr to 30 mTorr (the capacitors in the 60 mTorr and 100 mTorr samples are short-circuited, so they are excluded from discussion). The estimated k values are based on the thickness profile of tantalum oxide deposited at an oxygen partial pressure of 17.5 mTorr at room temperature (Fig. 17). As shown in Table 2, the dissipation factors are lower at thin regions of tantalum oxides deposited at 8 mTorr and 17.5 mTorr compared to thick regions. The reason for higher dissipation factors at thick region is suggested to be the "self-shadowing effect" at high deposition rate region during deposition where atoms easily pile up. Self-shadowing effect is an effect during deposition that arriving atoms cannot settle on top of each other, but rather settle on sideways into the nearest positions where they can have relaxed bond length. As shown in Fig. 27, the atoms on sideways will block the upcoming atoms, and shadow the low areas from deposition [15]. The result of self-shadowing effect is porous structure with voids. These pores will absorb water or hydroxyl ions, causing larger heat dissipation under electrical field. Therefore, dissipation factors are higher at thick regions. The high dissipation factors (>0.1) even at thin regio in the 8 mTorr sample imply the oxide is not fully oxidized at this level of oxygen environment. Both the capacitance and dissipation factor decrease when the oxygen partial pressure increases from 8 mTorr to 17.5 mTorr. High estimated k values and high dissipation factor imply higher polarizability in the 8 mTorr sample, which is considered to be not fully oxidized. The high dissipation factor and high estimated k values in the 30 mTorr

sample is suggested to be the reason of porous structure as the same in the 60 mTorr and 100 mTorr samples.

Oxygen partial pressure	Region of the oxide	Capacitance	Estimated k value	Dissipation factor
8 mTorr	Thick	$1.5*10^{-9}$	~330	1.5~2.0
	Thin	$1.5*10^{-9}$		0.1~0.3
17.5 mTorr	Thick	$5.0*10^{-10}$	---	0.9~1.0
	Thin	$2*10^{-10}$	~44	0.02~0.03
30 mTorr	Thick	$3.0*10^{-10}$	~99	0.6~0.7
	Thin	Short-circuited	---	----

Table 2 Capacitance, dissipation factor, and estimated k values of Ta oxide thin films deposited at various oxygen partial pressures

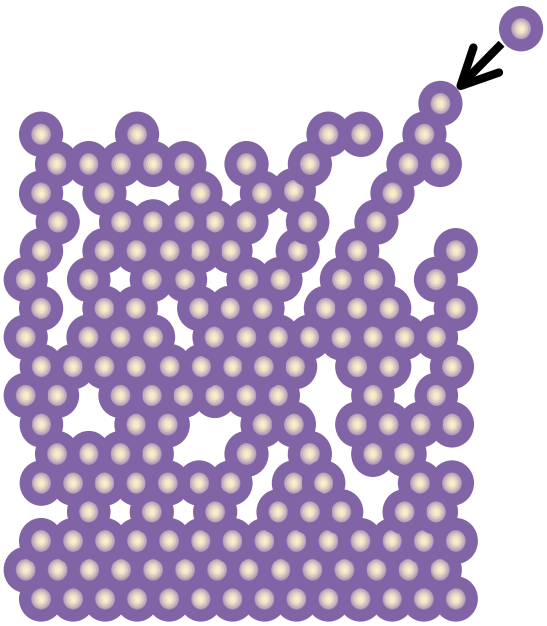


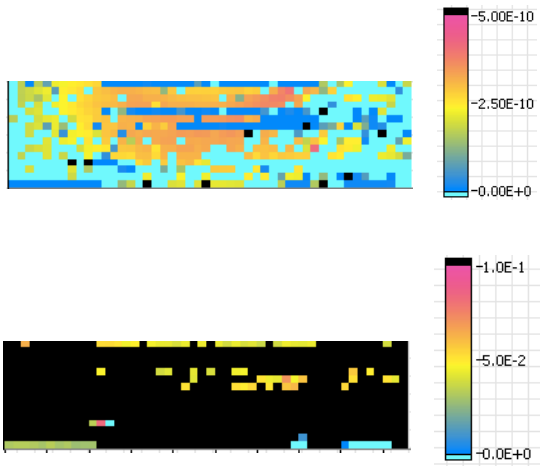
Fig. 27 Schematic of self-shadowing effect

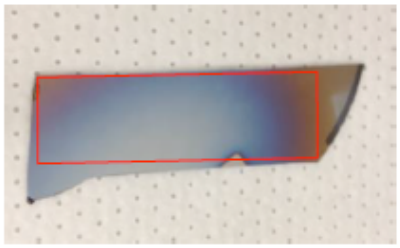
3.3.2 Effect of deposition temperature (25 °C-400 °C) on capacitance and dissipation factor

Substrate temperature during deposition has a large impact on thin film structures. Elevated temperature will provide the arriving atoms with more surface mobility to reduce the roughness and porous structure of the film. High temperature will also enhance oxidation in oxygen environment, and favor crystallization of the thin film. With the fact that high-quality capacitors of low dissipation factors (<0.04) are only observed at thin regions of tantalum oxide deposited at an oxygen partial pressure of 17.5 mTorr, whereas low-quality capacitors of high dissipation factors (>0.1) are among the entire region of the film deposited at a higher oxygen partial pressure of 30mTorr, it is suggested that the porous structure of the film rather than the oxidation level causes the high dissipation factors. Since the porous structure is caused by the atoms with low surface mobility on the substrate, the effect of deposition temperature on the electrical property of tantalum oxide thin film deposited at an oxygen partial pressure of 30 mTorr is investigated. Fig. 28 shows the heat map of capacitance and dissipation factor, and corresponding measured region of the samples deposited at room temperature, 250 °C, and 400 °C at an oxygen partial pressure of 30 mTorr. As shown in Fig. 28, except the thin regions of the oxides where capacitors are short-circuited, the dissipation factor decreases with the increase of deposition temperature. The dissipation factors of the sample deposited at room temperature are all greater than 0.1, but the dissipation factors drop dramatically to less than 0.01 for samples deposited at elevated temperatures of 250 °C and 400 °C. Capacitors with such low dissipation factors are considered to be high-quality. And this implies that the porous structure of tantalum oxide deposited at room temperature is reduced by the increase of deposition temperature. Furthermore, compared to the sample deposited at an oxygen partial pressure of 17.5 mTorr at room temperature, the self-shadowing effect at thick region of the film is reduced. Overall low

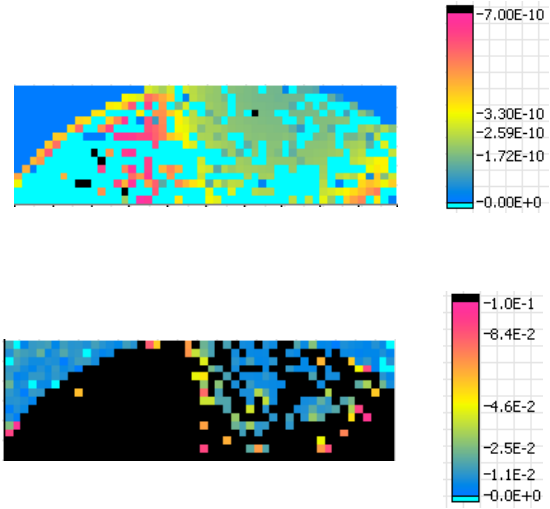
dissipation factors are observed except the regions that are short-circuited. However, increasing the substrate temperature from room temperature to 250 °C for tantalum oxide deposited at an oxygen partial pressure of 8mTorr does not improve the electrical property. As shown in Fig. 29, the capacitance of tantalum oxide deposited at an oxygen partial pressure of 8mTorr at 250 °C is around $2*10^{-9}$F, and the dissipation factor ranges from 2 to 10 through thin to thick region. This suggests the tantalum oxide is still not fully oxidized at an oxygen partial pressure of 8 mTorr at 250 °C.

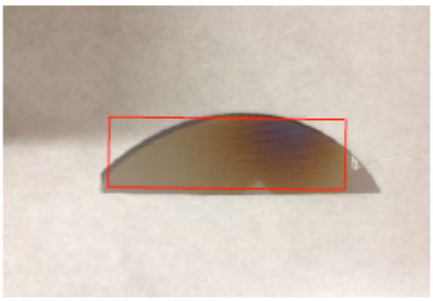
Dissipation Factor
Capacitance (F)
Dissipation Factor





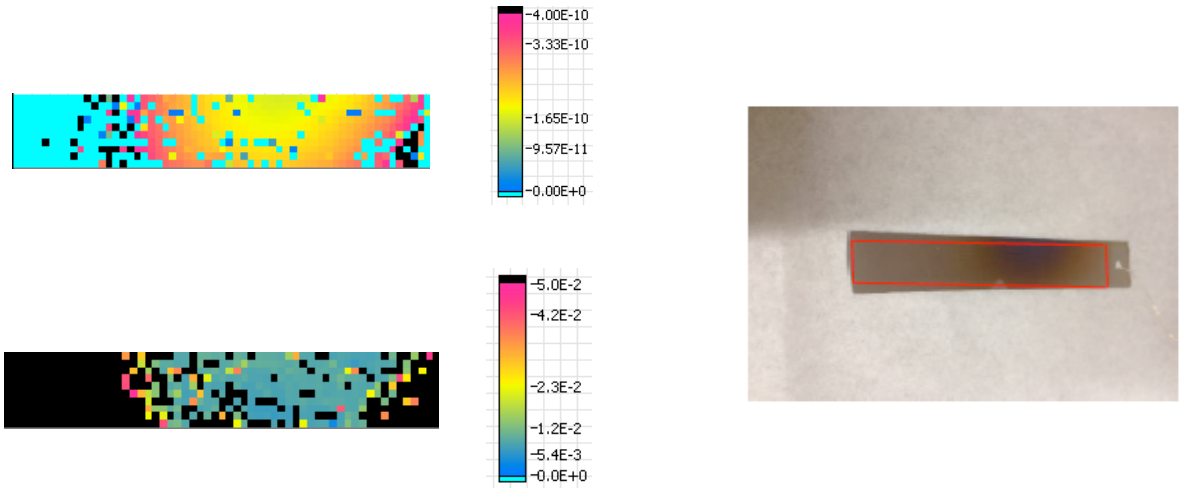
(a)





(b)

Dissipation Factor



(c)

Fig. 28 Heat map of capacitance (F) (top) and dissipation factor (bottom), and the corresponding measured region (red box) of Ta oxide deposited at (a) room temperature, (b) 250 °C, and (c) 400 °C at an oxygen partial pressure of 30 mTorr

Capacitance (F)

Dissipation Factor

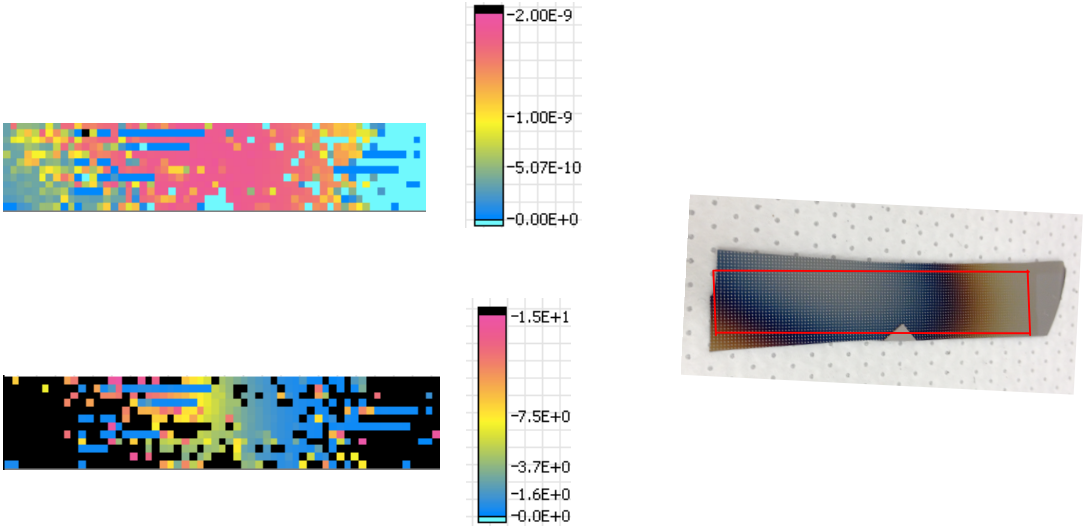


Fig. 29 Heat map of capacitance (F) (top) and dissipation factor (bottom), and the corresponding measured region (red box) of Ta oxide deposited at an oxygen partial pressure of 8 mTorr at 250 °C

3.4 Frequency dependence of capacitance and dissipation factor measurement

Frequency dependence of capacitance and dissipation factor is related to the quality of the capacitor as well as the polarizability characteristics. A high-quality capacitor doesn't show much frequency dependence of its capacitance and dissipation factor [14]. Fig. 30 presents the heat maps of capacitance and dissipation factor of tantalum oxide deposited at an oxygen pressure of 8 mTorr at room temperature with 1kHz, 10kHz, and 100kHz measuring frequency. Although the capacitance does not show much frequency dependence, the dissipation factor drops an order of magnitude at 100kHz. Similarly, the tantalum oxide deposited at an oxygen partial pressure of 8 mTorr at 250°C also shows frequency dependence of the dissipation factor as shown in Fig. 31. The dissipation factor also drops an order of magnitude at 100kHz. However, the tantalum oxide deposited at an oxygen partial pressure of 30 mTorr at 400°C does

not show any frequency dependence of capacitance and dissipation factor (<0.01) as presented in Fig. 32. The low dissipation factor (<0.01) with no frequency dependence confirms the film deposited at an oxygen partial pressure of 30 mTorr at 400 °C is fully oxidized.

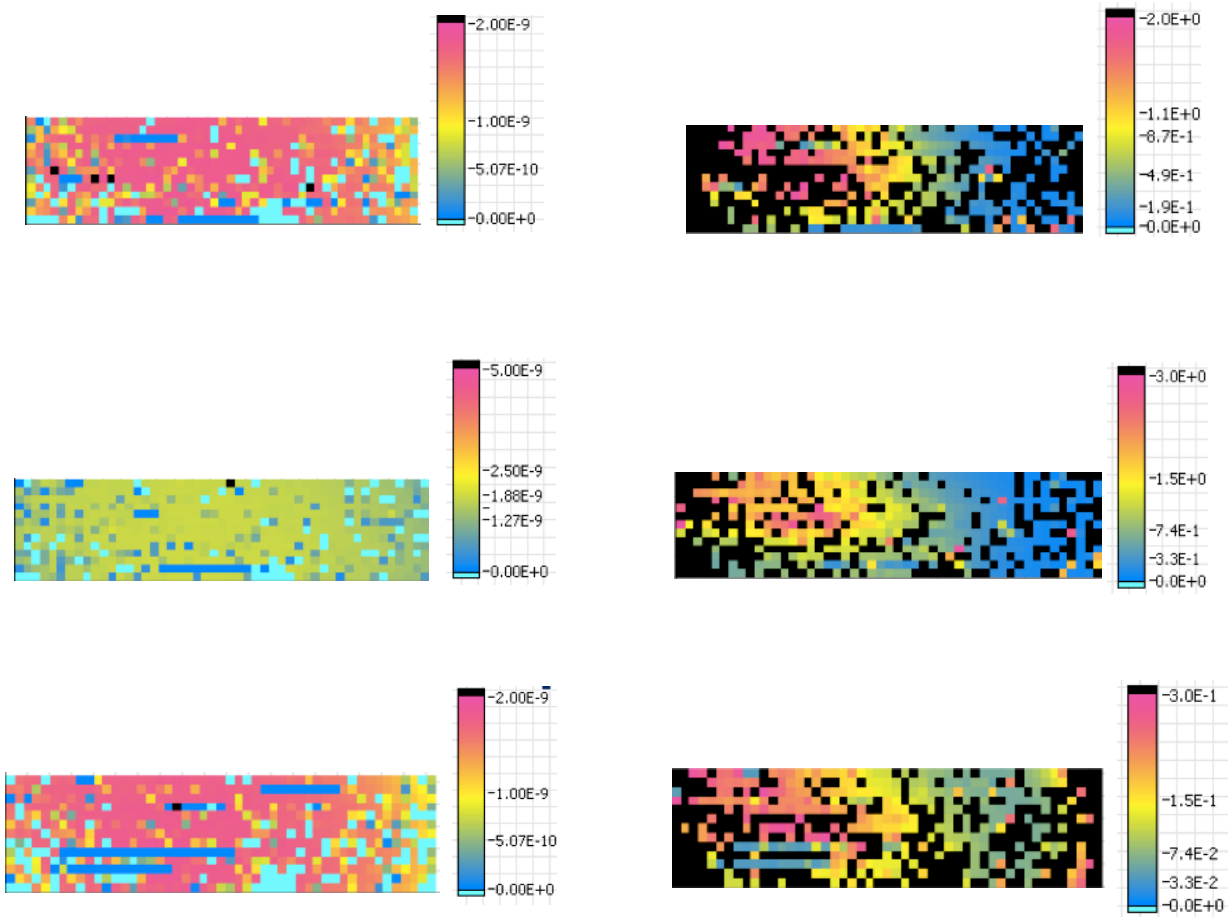


Fig. 30 Heat map of capacitance (F) (left) and dissipation factor (right) of Ta oxide deposited at an oxygen partial pressure of 8 mTorr at room temperature with measuring frequency of (a) 1kHz, (b) 10kHz, and (c) 100kHz

100kHz
10kHz
1kHz

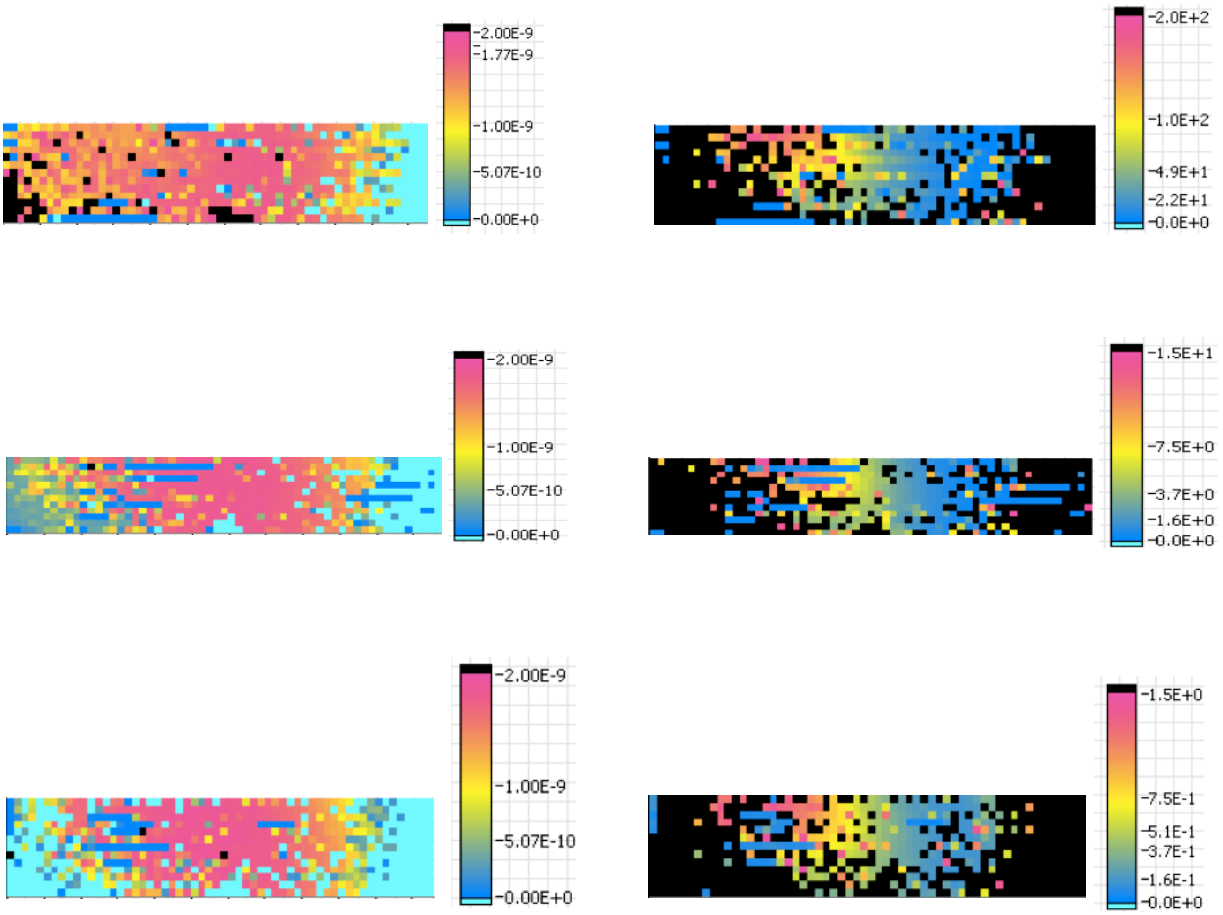


Fig. 31 Heat map of capacitance (F) (left) and dissipation factor (right) of Ta oxide deposited at an oxygen partial pressure of 8 mTorr 250 °C with measuring frequency of (a) 1kHz, (b) 10kHz, and (c) 100kHz

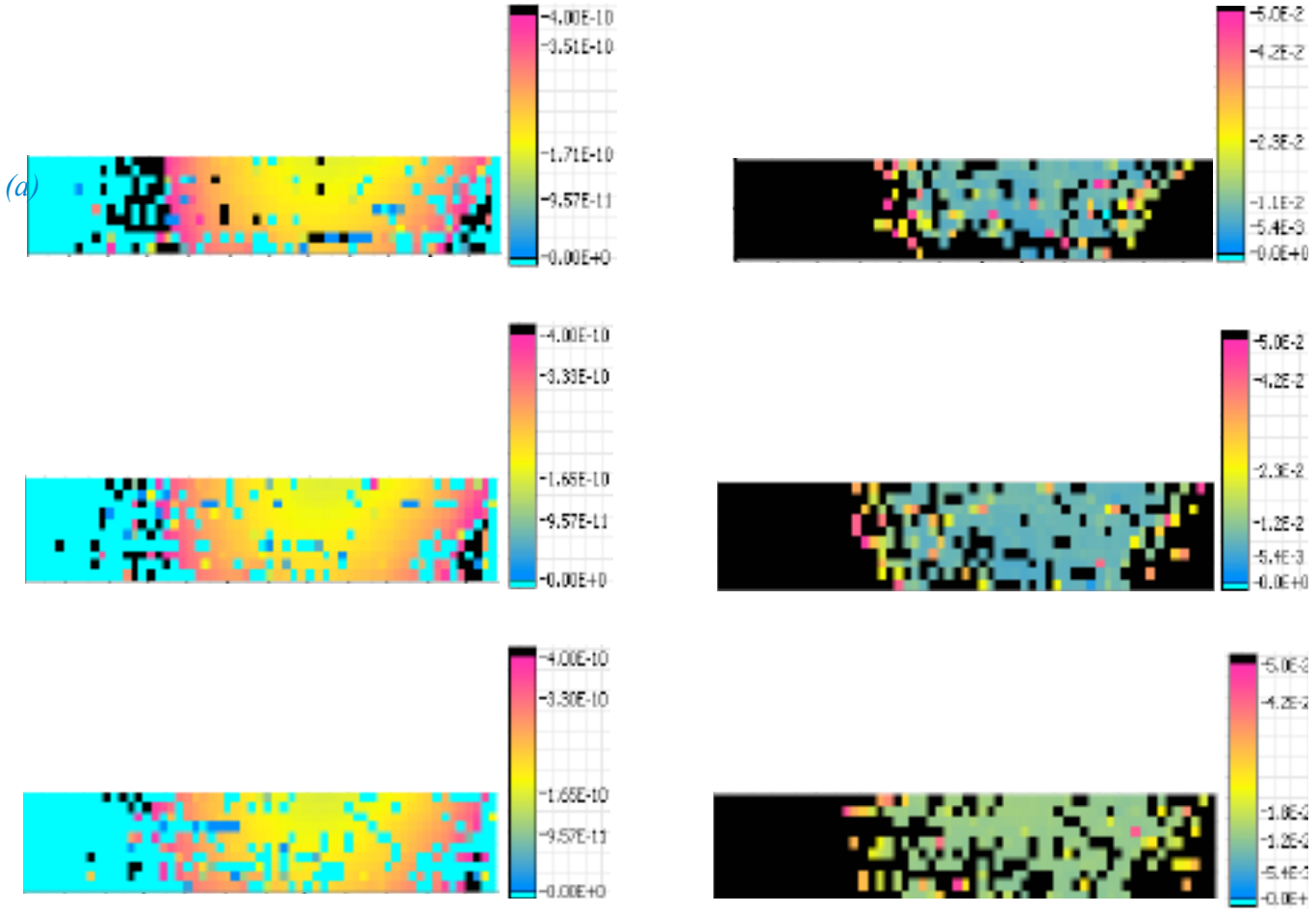
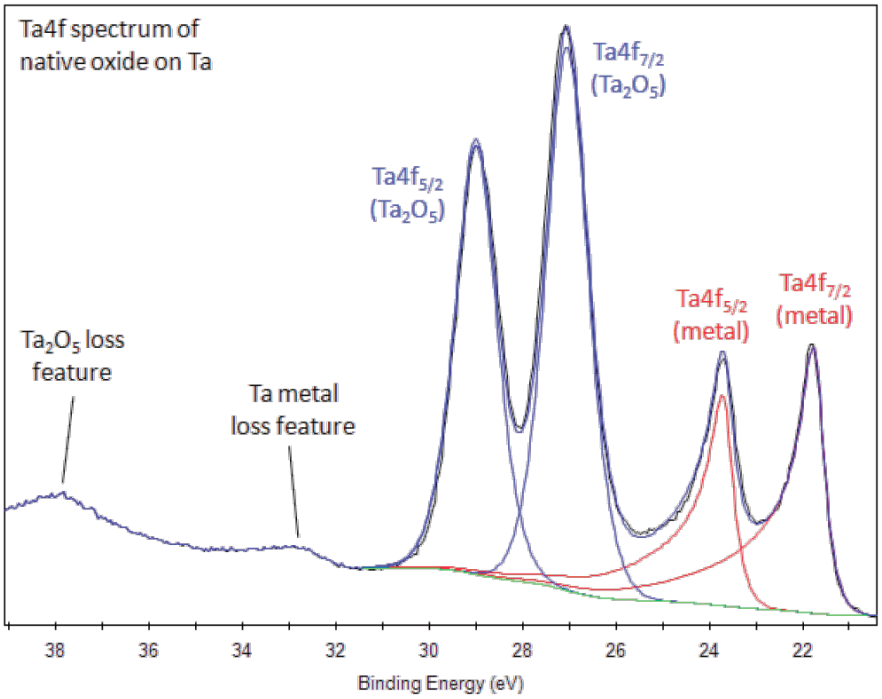


Fig. 32 Heat map of capacitance (F) (left) and dissipation factor (right) of Ta oxide deposited at an oxygen partial pressure of 30 mTorr 400 °C with measuring frequency of (a) 1kHz, (b) 10kHz, and (c) 100kHz

3.5 X-ray Photoelectron Spectroscopy (XPS) analysis

XPS is used to examine the oxidation state of tantalum oxide thin films deposited at various conditions. The typical Ta 4f XPS spectra and the corresponding binding energies are presented in Fig. 33. As shown in the figure, Ta $4f_{7/2}$ binding energy for tantalum metal (Ta^{0+}) is around 21.76 eV, and 26.56 eV for fully oxidized Ta_2O_5 (Ta^{5+}). The binding energies of tantalum sub-oxides (Ta^{4+}, Ta^{3+}, Ta^{2+}, Ta^{1+}) are therefore between 21.76 eV and 26.56 eV. The doublet of Ta 4f peaks is a result of spin orbit splitting, where two possible states have different binding energies [16]. The specific area ratio of Ta $4f_{7/2}$ to Ta $4f_{5/2}$ is 4:3 [16].



Species	Ta 4f7/2 Binding Energy (eV)	Std. Dev.
Metal (Literature Average)	21.76	0.16
Ta2O5 (Literature Average)	26.56	0.42
Metal (A(0.38,0.7,10)GL(10) Lineshape)	21.55	0.03
Metal (LA(1.1,7,25) Lineshape)	21.46	0.02
Sub-Oxide	24.66	0.16
Ta2O5	26.71	0.23

Fig. 33 Ta 4f XPS spectra and corresponding binding energies (data from Thermo Scientific XPS knowledge base)

The XPS analysis is taken at the thickest region of the film. Fig. 34 shows the Ta 4f XPS spectra of tantalum oxides deposited at an oxygen partial pressure of 30 mTorr at 400°C and 250°C. As shown in the figure, there are no obvious Ta metal peaks shown in the spectra in both samples. The peak fitting with area ratio constraint of Ta 4f $_{7/2}$ and Ta 4f $_{5/2}$ confirms that the tantalum oxides deposited at an oxygen partial pressure of 30 mTorr at 400°C and 250°C are full oxidized. This result well corresponds to their electrical properties, where their dissipation factors are

below 0.01, and no frequency dependence shown in the 30mTorr/400°C sample. The XPS spectra for tantalum oxides deposited at oxygen partial pressures of 17.5 mTorr and 30 mTorr at room temperature are presented in Fig. 35. Similarly, the XPS spectra confirm that the tantalum oxides deposited at oxygen partial pressures of 17.5 mTorr and 30 mTorr at room temperature are full oxidized. This also confirms that the high dissipation factors (>0.1) of tantalum oxide deposited at an oxygen partial pressure of 30 mTorr at room temperature, and the high dissipation factors at the thick region of the film deposited at 17.5 mTorr oxygen partial pressure at room temperature come from porous structure film, not the oxidation state. The film deposited at an oxygen partial pressure of 8 mTorr is suggested to be not fully-oxidized from its electrical properties. As illustrated in Fig. 36, its XPS spectrum shows a clear "tail" at lower binding energy region compared to the fully-oxidized sample. Fig. 37 shows the fitting of peaks of Ta 4f XPS spectrum of tantalum oxide deposited at 8 mTorr oxygen partial pressure at 250°C. As shown in the figure, the Ta 4f peaks are composed of fully-oxidized Ta 4f peaks and a subset of Ta 4f peaks that shift to lower binding energies. By calculating the peak area percentage, the percentage of shifted Ta 4f peaks is about 10%, which indicates that there are about 10% of Ta sub-oxides in the 8mTorr/250°C sample. These 10% sub-oxides are therefore responsible for the high dissipation factor of the film.

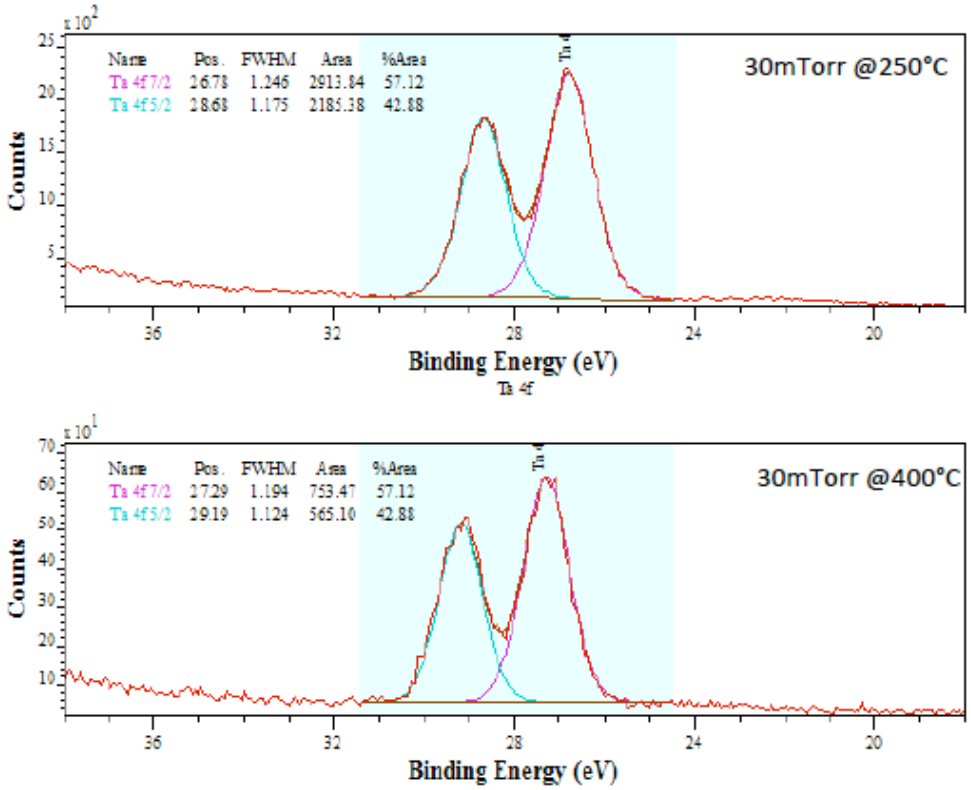


Fig. 34 Ta 4f XPS spectra of tantalum oxides deposited at an oxygen partial pressure of 30 mTorr at 400°C (bottom) and 250°C (top)

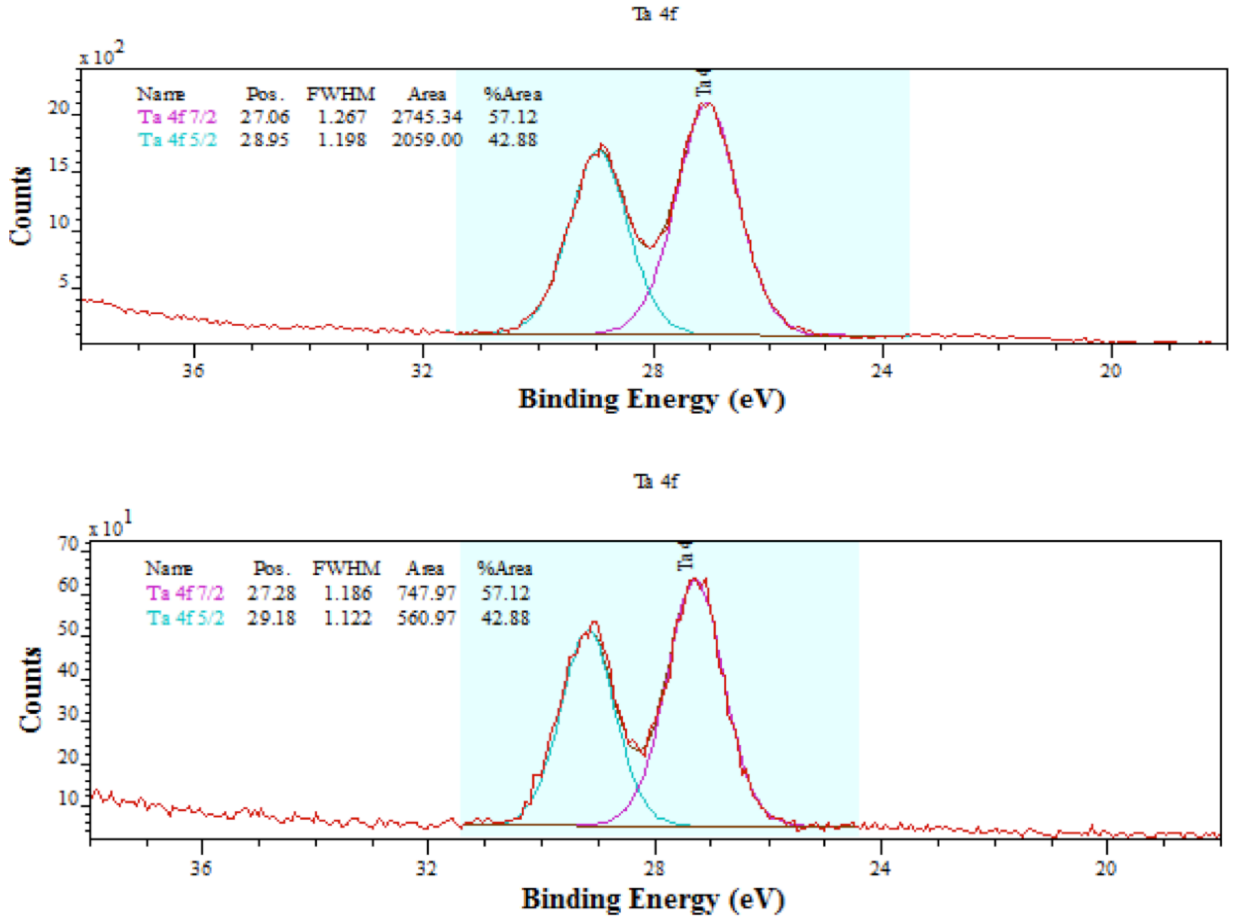


Fig. 35 Ta 4f XPS spectra of tantalum oxides deposited at room temperature at oxygen partial pressures of 30 mTorr (bottom) and 17.5 mTorr (top)

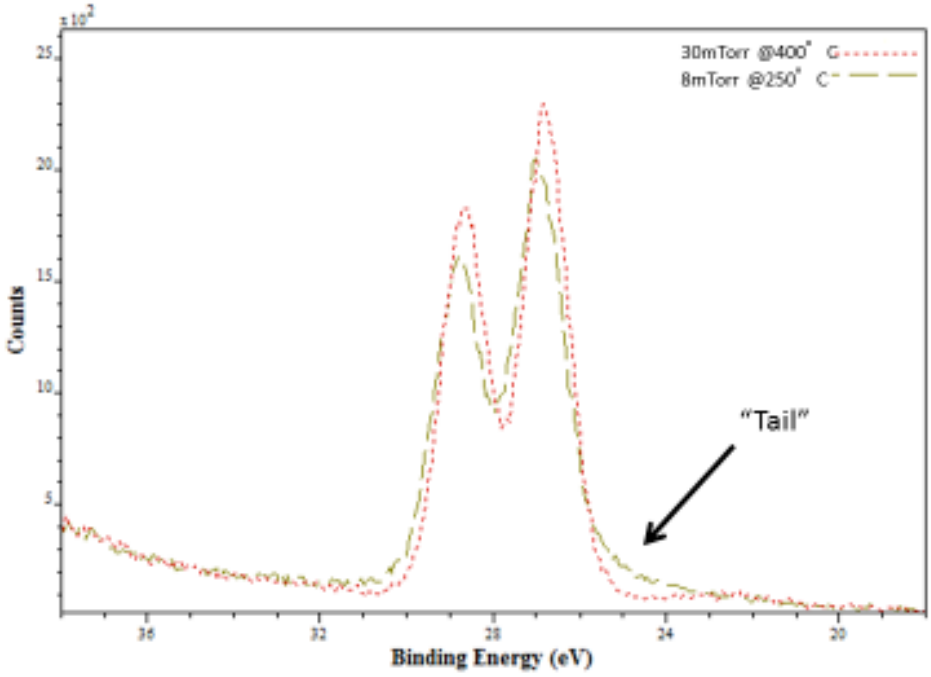


Fig. 36 The Ta 4f XPS spectra of Ta oxides deposited at 8mTorr oxygen partial pressure/250°C and 30 mTorr oxygen partial pressure/400°C

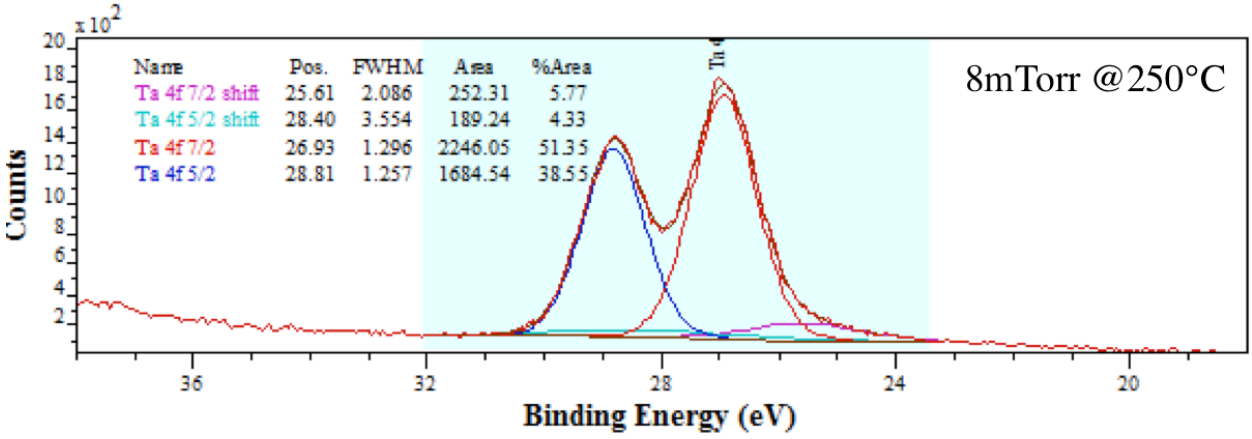


Fig. 37 Ta 4f XPS spectra of tantalum oxides deposited at an oxygen partial pressures of 8 mTorr at 250°C

3.6 Calculation of the k value based on the thickness profile and capacitance measurement

In order to calculate reliable k values of tantalum oxide prepared by PLD. Two threshold levels of capacitance and dissipation factor are set to ensure reliable capacitors for the calculation of k values. Capacitors with capacitance lower than 10^{-11}F, and dissipation factors larger than 0.04 are not included in the calculation. The capacitance and dissipation factor values of tantalum oxide deposited at an oxygen partial pressure of 17.5 mTorr at room temperature along the center line of the sample are shown in Fig. 38, where data are collected at capacitors along the center line of the wafer, and two other capacitors on either side of it (5 capacitors at each position along the center line on the wafer). According to the tantalum oxide thickness profile in Fig. 17, the capacitance profile in Fig. 38, and the constant electrode area of $3.14*10^{-8}$ m^2, the calculated k values of tantalum oxide are then presented in Fig. 39. The k values of pure tantalum oxide prepared by PLD range from 40 to 44, which is much higher than the literature value of 24 using

sputtering technique [8]. The discrepancy of k values of tantalum oxide may come from the error in measured thickness or the possible dielectric enhancement in PLD process.

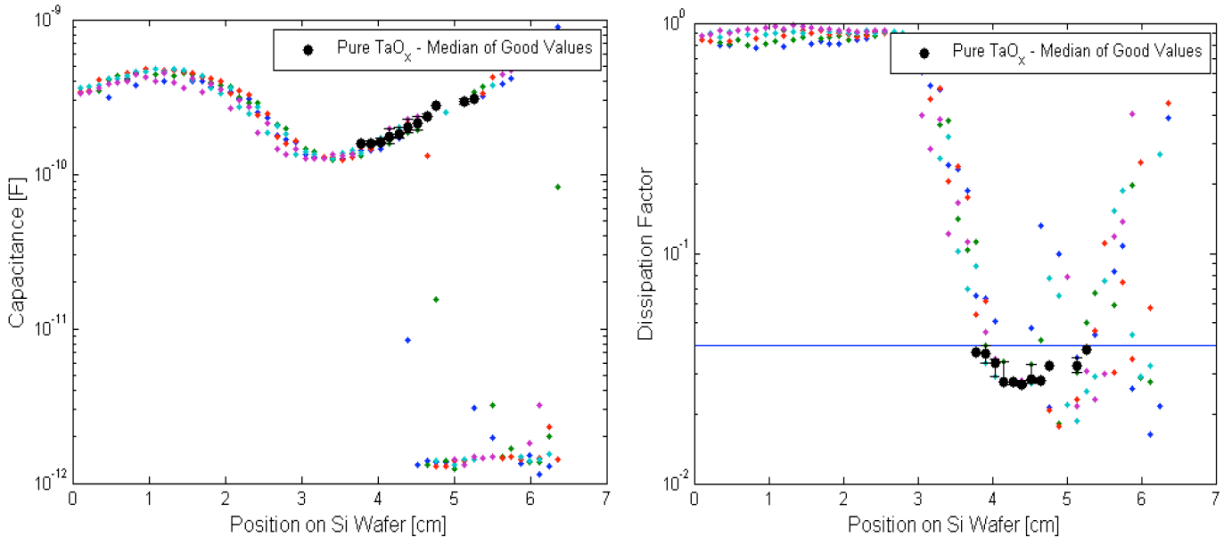


Fig. 38 Capacitance (left) and dissipation factor values of tantalum oxide prepared by PLD. Small dots represent individual capacitors at each position, and large dots represents median of "qualified" values used in calculating k values [13].

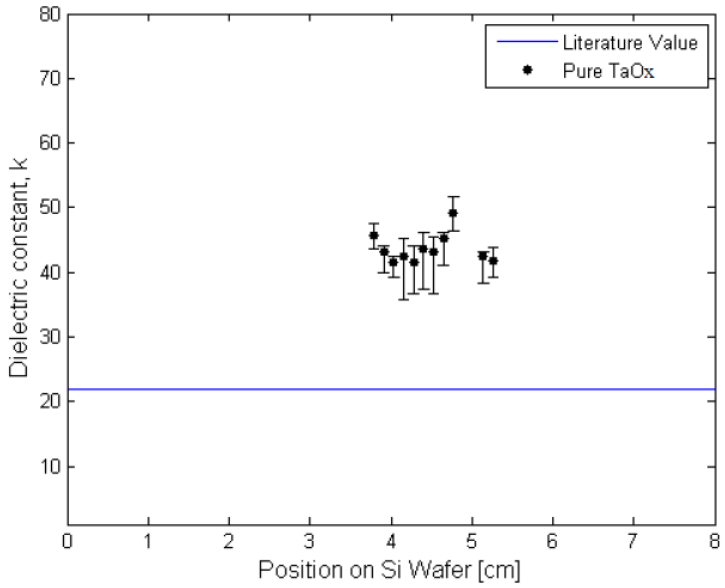


Fig. 39 Calculated k values of tantalum oxide prepared by PLD as a function of position along the center line on Si substrate, and the literature k value of 22 by sputtering [13] [20].

3.7 Ge-incorporated tantalum oxide

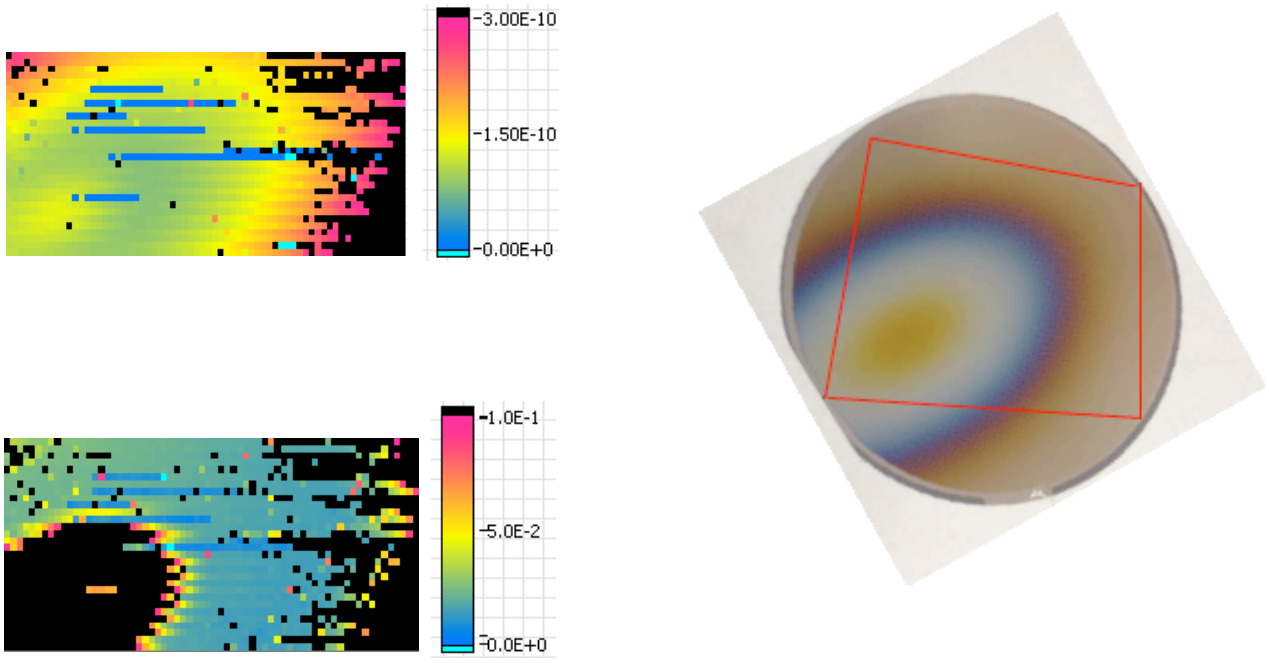
Ge-incorporated tantalum oxide is prepared by alternative deposition of Ta and Ge monolayer with certain shot ratio. It should be noticed that tantalum is deposited from the left hand side (marked as position 0) of the substrate, while germanium is deposited from the other side of the substrate. As a result, tantalum concentration decreases with the increase of positions on the substrate.

Low Ta concentration sample

Fig. 40 shows the as-deposited films and the heat map of capacitance and dissipation factors of low Ta concentration sample (90% of Ta, and 10% of Ge at the center of the wafer; hereafter referred to as low Ta concentration sample). The capacitance are about $1.0*10^{-10}$ to $1.5*10^{-10}$ at thin region of the film. Except the thick region where self-shadowing effect causes high

Capacitance (F)
Dissipation Factor

dissipation factors, the dissipation factors at thin region are below 0.04. Similarly, in order to further calculate the k values, 5 data points at each position along the center line on the wafer are collected for capacitance and dissipation factor values as presented in Fig. 41. Similarly, as shown in Fig. 42, the k values of low Ta concentration sample are calculated by selected reliable capacitors. The k values remain close to 30 at the positions along the center line.



(a) (b)

Fig. 40 (a) Heat map of capacitance (top) and dissipation factor (bottom) of low Ta concentration sample (90% of Ta, and 10% of Ge at the center of the wafer), and (b) the corresponding measured region (red box).

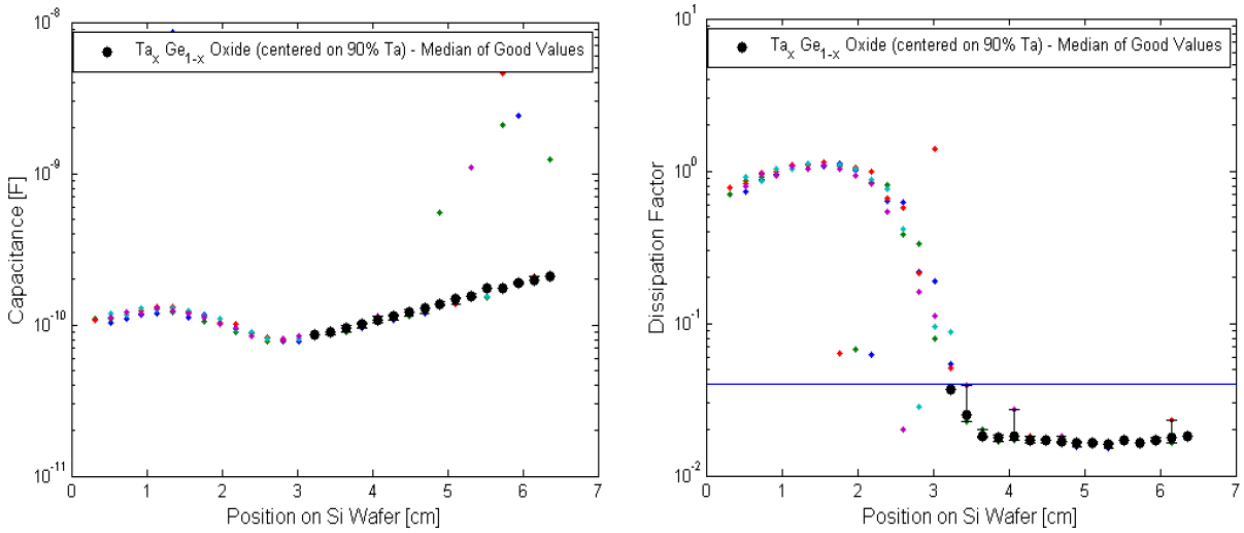


Fig. 41 Capacitance (left) and dissipation factor values of Ge-incorporated Ta oxide (90% of Ta, and 10% of Ge at the center of the wafer). Small dots represent individual capacitors at each position, and large dots represents median of "qualified" values used in calculating k values [13].

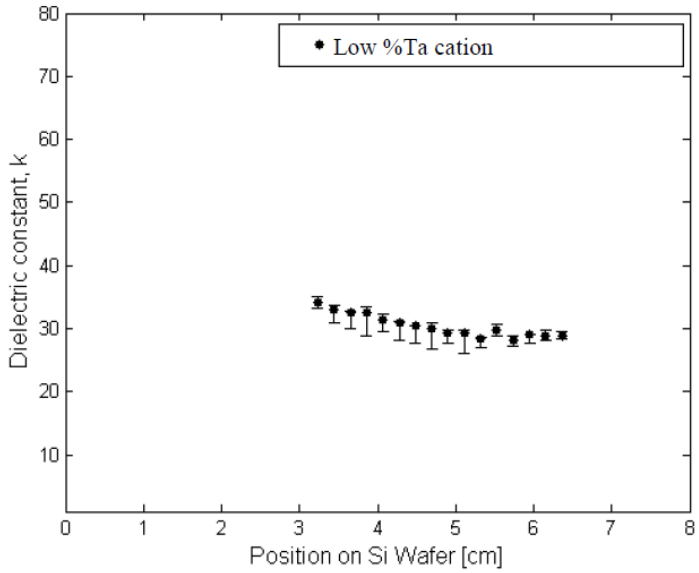
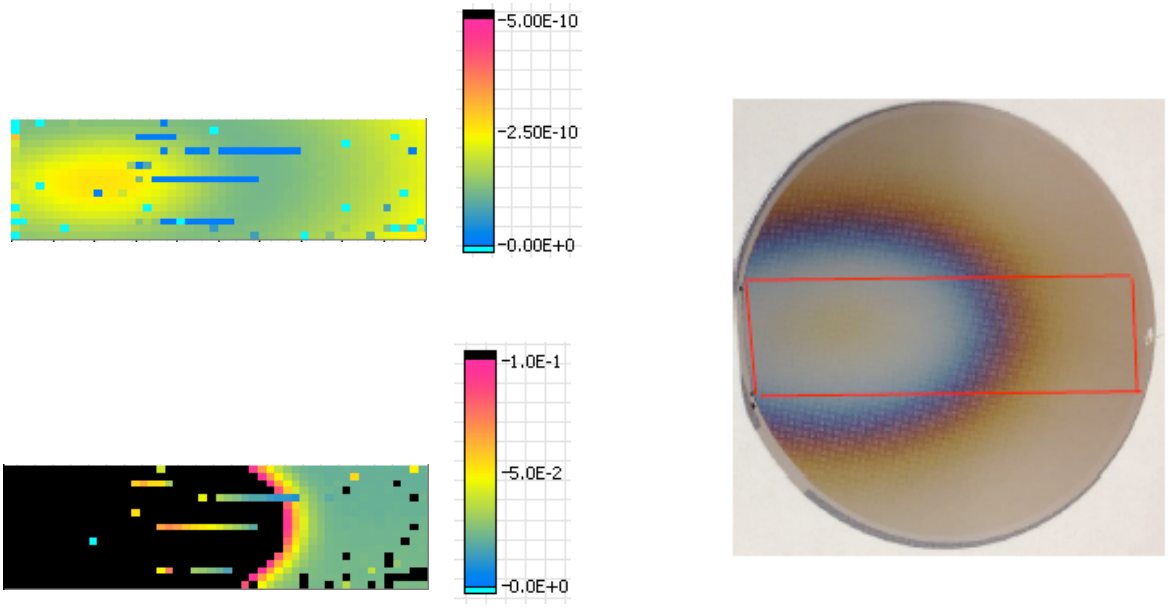


Fig. 42 Calculated k values of Ge-incorporated Ta oxide (90% of Ta, and 10% of Ge at the center of the wafer) as a function of position along the center line on Si substrate [13].

High Ta concentration sample

Fig. 43 shows the as-deposited films and the heat map of capacitance and dissipation factors of high Ta concentration sample (95% of Ta, and 5% of Ge at the center of the wafer; hereafter referred to as high Ta concentration sample). The capacitances are higher than the capacitances of the low Ta concentration sample, and the dissipation factors are still low (<0.04) at thin region of the film. Fig. 44 shows the capacitance and dissipation factor values at positions along the center line on the wafer. With the selected values of capacitance, the k values of high Ta concentration sample as a function of position are shown in Fig. 45. The k values range from 28 to 35 with the increase of Ta concentration (decrease of positions on the substrate).



(a) (b)

Fig. 43 (a) Heat map of capacitance (top) and dissipation factor (bottom) of low Ta concentration sample (90% of Ta, and 10% of Ge at the center of the wafer), and (b) the corresponding measured region (red box).

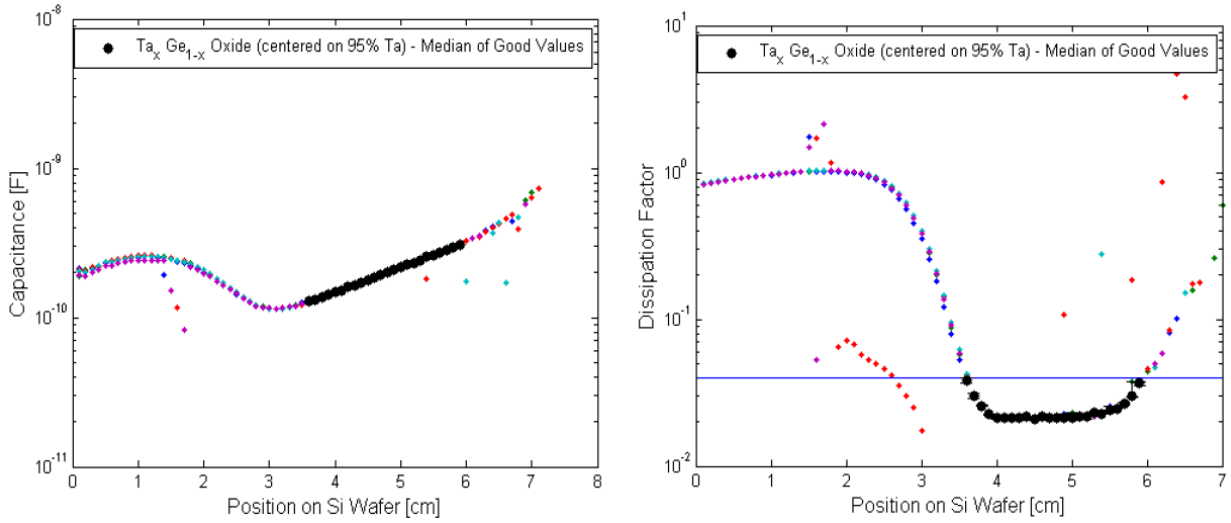


Fig. 44 Capacitance (left) and dissipation factor values of Ge-incorporated Ta oxide (95% of Ta, and 5% of Ge at the center of the wafer). Small dots represent individual capacitors at each position, and large dots represents median of "qualified" values used in calculating k values [13].

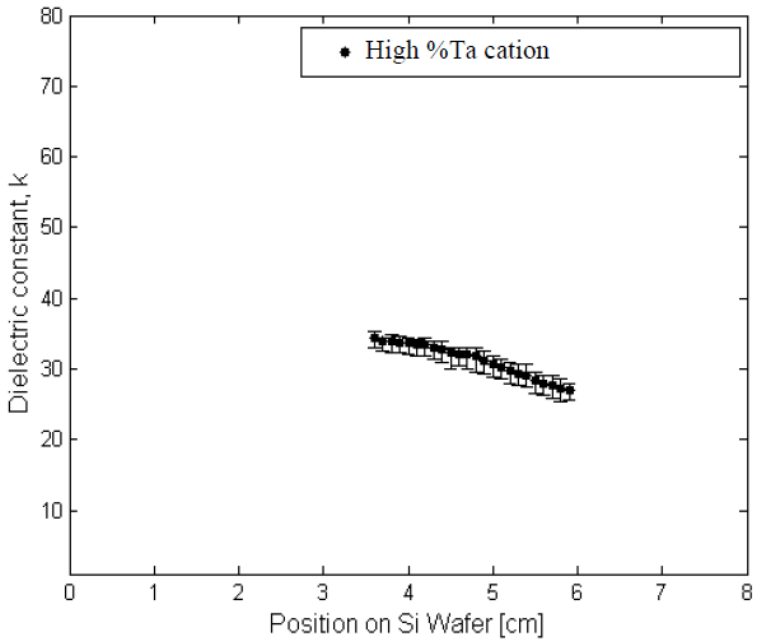


Fig. 45 Calculated k values of Ge-incorporated Ta oxide (95% of Ta, and 5% of Ge at the center of the wafer) as a function of position along the center line on Si substrate [13].

3.8 k values of Ge-incorporated tantalum oxide as a function of Ta concentration compared to literature results

Based on the mole fraction profile of Ge-incorporated tantalum oxide in Fig. 18, and the calculated k values as a function of position on the wafer, the k values of Ge-incorporated tantalum oxide are plotted as a function of Ta concentration in Fig. 46. Generally, the k values of Ge-incorporated tantalum oxide in this study follow the similar trend of literature values from Ta concentration of 75% to Ta concentration of 95%. The absolute k values well correspond to literature values with PLD technique [17], and the k values are higher than the values with sputtering technique [8] through all compositions. The discrepancy may arise from the thickness measurement, and the possible dielectric enhancement in PLD process.

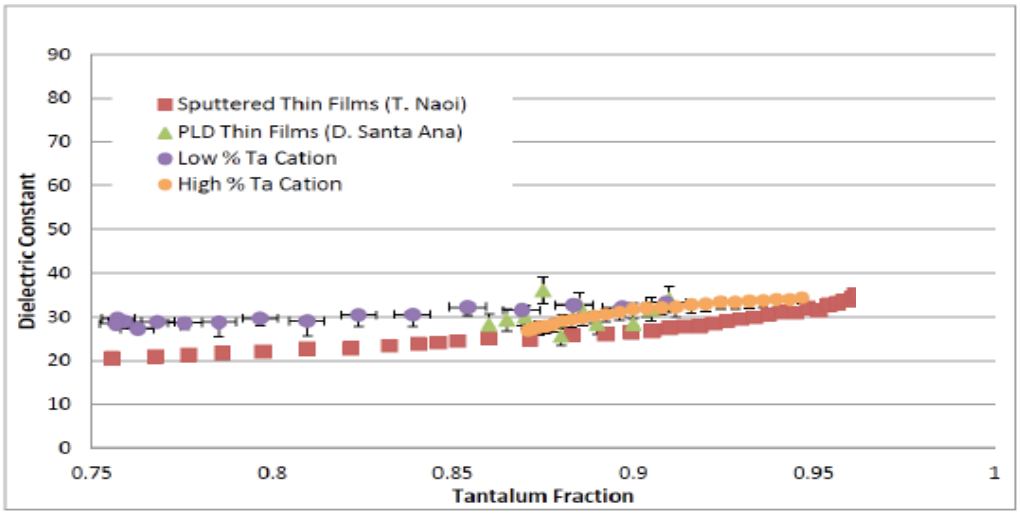


Fig. 46 Dielectric constant (k value) of Ge-incorporated tantalum oxide as a function of Ta concentration compared to literature values [13]

4. Conclusions

The electrical property and chemical state of tantalum oxide thin films prepared by PLD technique are affected by the oxygen partial pressure and substrate temperature during deposition. In order to have tantalum oxides with high quality, both parameters have to be carefully considered. Tantalum oxides deposited above an oxygen partial pressure of 17.5 mTorr are fully oxidized by the confirmation of XPS analysis. However, the capacitors of tantalum oxides deposited at high oxygen partial pressures of 60 mTorr and 100 mTorr at room temperature are short-circuited through the entire film region. It is suggested the porous structure caused by low surface mobility Ta atoms in high oxygen partial pressure background results in the poor electrical property. Ta oxide films deposited at low oxygen partial pressure of 8 mTorr at room temperature and 250°C show high dissipation factors (>0.1) through the entire regions of the films. XPS analysis confirms the film is not fully oxidized, and there are about 10% Ta sub-oxides causing the high dissipation factors. The sample deposited at an oxygen partial pressure of 17.5 mTorr at room temperature shows low dissipation factors (<0.04) at thin region of the film, whereas high dissipation factors (>0.3) caused by self-shadowing effect are obtained at thick region of the film. Tantalum oxide deposited at 30 mTorr oxygen partial pressure at room temperature shows high dissipation factors (>0.1) among the entire region, and it is suggested the porous structure rather than the oxidation state caused the poor electrical property. At elevated deposition temperatures, tantalum oxide deposited at 30 mTorr oxygen partial pressure at 250°C and 400°C shows overall low dissipation factors (<0.01) except the region with short-circuited capacitors. The self-shadowing effect at thick region of the film is also reduced at the deposition conditions of 30 mTorr oxygen partial pressure at 250°C and 400°C. The film deposited at 30 mTorr oxygen partial pressure at 400°C also shows frequency independence (1kHz to 100kHz)

on capacitance and dissipation factors, implying fully oxidized high-quality tantalum oxide. The k values of the tantalum oxide film by PLD technique are calculated to be 40 to 44, which are higher than the literature value of 22 with sputtering technique.

Ge-incorporated tantalum oxides with Ta concentration from 75% to 95% are prepared by alternative deposition of Ta and Ge with certain shot ratios. The k values of Ge-incorporated tantalum oxide follow the similar trend of literature values from Ta concentration of 75% to Ta concentration of 95% with dielectric enhancement behavior. And the k values are higher than the values with sputtering technique through all compositions. The absolute k values ranges from 28 to 35 at all compositions. With only 5% Ge substitution (95% Ta), a k value of 35 is obtained. A 60% increase of k value compared to the k value of pure tantalum oxide in literature (k=22).

The overall k values of tantalum oxide and Ge-incorporated tantalum oxide prepared by PLD are higher than the values prepared by sputtering technique. Despite the discrepancy of the k values, the data was consistent in this study. It is possible that PLD is a promising technique to produce high dielectric constant tantalum based oxides. As a result, PLD is a viable option to prepare tantalum oxide and Ge-incorporated tantalum oxide for high-k dielectric application.

Future Work

Future areas of research following this study include TEM cross-section image analysis on the tantalum oxides prepared at high oxygen partial pressures (<60 mTorr) to confirm the suggested porous structure. Using tantalum oxide target instead of tantalum metal target is another possibility to explore the properties of tantalum oxide in PLD system. In order to further understand the mechanism of dielectric enhancement behavior in Ge-incorporated tantalum oxide in PLD system, XPS analysis may also be taken on the Ge-incorporated tantalum oxide sample to characterize the oxidation states of Ge and Ta. Optical properties such as refractive index can also be measured to investigate the origin of dielectric enhancement behavior in Ge-incorporated tantalum oxide. XRD or electron beam diffraction analysis can also confirm the amorphous structure of both tantalum oxide and Ge-incorporated tantalum oxide. The interface properties of Ta_2O_5 and Si substrate are also potential future area of research since the interface properties are essential in high-k dielectric applications. To study the higher k values in tantalum based oxide prepared by PLD compared to sputtering technique, electron diffraction is one of the possibility to study the short range order of crystallinity of the films.

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