# BULK TITANIUM WAVEGUIDE – A NEW PLATFORM FOR UNIPLANAR MICROWAVE CIRCUITS AND RFMEMS

A Dissertation

Presented to the Faculty of the Graduate School

Of Cornell University

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

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January 2008

# BULK TITANIUM WAVEGUIDE – A NEW PLATFORM FOR UNIPLANAR MICROWAVE CIRCUITS AND RFMEMS

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Cornell University 2008

The majority of uniplanar circuits are based on transmission lines of two basic topologies: Microstrip and Coplanar Waveguide (CPW). Microstrip offers low loss, while suffering from large circuit size, high dispersion, poor design flexibility, and the necessity of large via holes. CPW improves upon microstrip by bringing the ground to the same level as the signal, therefore providing low dispersion, smaller circuit size, high design flexibility and no via holes. However, the fields in CPW concentrate on the thin edges and are therefore less confined. This translates into higher conductor loss, cross-talk and poor power handling capability.

We present a new topology for uniplanar microwave circuitry: bulk titanium waveguide. The waveguide is formed by coplanar titanium segments separated by low-loss dielectric that is planarized to the same level as the titanium. Due to the high aspect ratio of the dielectric cross section, the electric field is confined primarily within the dielectric, therefore reducing losses due to radiation and parasitic coupling. This geometry distributes the surface current across the entire height of the structure, reducing conductor losses while enhancing power handling capabilities. The high aspect ratio in-plane electrical isolation also provides through-wafer interconnects with a high packing density. When integrated with a bulk titanium package, this waveguide provides a robust, compact, packaging solution for microwave subsystems as well as other microcomponents such as MEMS. We have successfully designed, fabricated and characterized packaged waveguides which measured, at 40GHz, ~0.7dB/mm insertion loss and the impact due to package < 0.1dB. Additionally, we

developed a quasi-static model based on conformal mapping that accurately describes the characteristics of the waveguide.

Titanium has one of the highest strength to weight ratio among metals. It is naturally resistant to corrosive environments and is a widely used as implants due to its bio-compatibility. Titanium is also one of the few materials with an endurance limit, which means that it can be deformed repeatedly without breaking. However, the current manufacturing processes for titanium sheets are not tailored for microfabrication. We developed a suite of technologies that overcome issues such as residual stress, thickness variation, embedded defects and surface roughness.

## BIOGRAPHICAL SKETCH

Xiaojun Trent Huang grew up in Luoyang, China, where he lived until the age of 15 when he moved to Hefei, China to attend the University of Science of Technology of China. After college, he entered the University of Virginia for graduate studies. Upon receiving a M.A. in physics, he entered Cornell University for his PhD. He paused his study at Cornell and joined the high-tech industry and worked for several years in areas of optics and RFMEMS, before joining UCSB as a post-graduate researcher, when he started his research on bulk-titanium RFMEMS. He received his PhD in 2008 and is currently working on RFMEMS and Micro-fluidics.

To my family

# ACKNOWLEDGMENTS

The road leading to my Ph.D. has not been a straight and easy one. A number of people have helped tremendously. First and foremost, I would like to thank Prof. MacDonald for his consistent support and guidance over the years, without which this work would not have been possible. I especially appreciate the freedom he gave me in pursuing innovations in my research. I am extremely grateful for the understanding and consideration from Prof. Pollock, Kan, and Spencer, who agreed to serve on my committee on short notices. I would also like to thank Prof. Bhave, who generously acted as proxy due to Prof. Spencer's absence at my defense.

Seven years' of departure from Cornell is a long time and that alone could have been an impassible hurdle, if not for the kind help from Barb at the Graduate School and Scott at the School of Electrical Engineering. I truly appreciate their consideration and professionalism.

I would like to thank Shane and Changsong for their significant contributions to the research. Special thanks to Masa and Dave for their continuous support and numerous insightful discussions.

Working with such an intelligent and dynamic group at UCSB has been a wonderful experience in my life. Payam, Marco, Emily, Yanting, Adam(s), Seth, Marcus, have all been very helpful and pleasurable researchers to work with. Last, I would also like to thank Prof. Kim Turner's group for their help and support.

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# CHAPTER 1

# INTRODUCTION

For low frequency signals, a wire, or metal trace, on a planar circuit - such as a printed circuit board - can be approximated as a lumped component with a single complex value representing its resistive and reactive properties. At higher frequencies, e.g., microwave frequencies, this approximation breaks down as the physical dimensions of these metal traces become significant relative to the wavelength of the signal [1, 2]. The metal traces now serve as transmission lines with distributed properties that can be utilized to form a myriad of devices with easily implemented changes in their geometries [3, 4].

The vast majority of high frequency, planar circuits are realized with two simple transmission line topologies: microstrip [5, 6] and coplanar waveguide (CPW) [7, 8]. Both topologies consist of thin metal traces fabricated on top of low-loss dielectric substrates.

We present a new 3D topology to microwave circuits, based on a bulk metal substrate with geometries containing dielectric-filled, high aspect ratio trenches for signal carrying. Based on newly developed microfabrication techniques in bulk titanium, the backbone of our new planar circuit platform – bulk titanium waveguide – offers the advantages of compact geometry, superior field confinement, and the capability of forming a small-footprint, high-performance RFMEMS package.

The topological comparison of the bulk titanium and conventional planar waveguides is illustrated in Figure 1-1. Instead of having a large block of dielectric as the universal carrier/substrate, the bulk titanium waveguide limits the dielectric to within the high aspect ratio trenches between segments of bulk titanium that are coplanar, therefore carrying over similar advantages to CPW over microstrip, such as

flexibility in design and ease of integration, low ground inductance, and compact size [9, 10]. Meanwhile, the deep electromagnetic wave-carrying trenches expand the wave-carrying areas from the thin metal edges, as in the case of CPW, to the entire thickness of the substrate, therefore reducing loss. Another key difference in the field distribution lies in the high aspect ratio of trenches, which confines the electric field, therefore significantly reduces losses due to radiation, cross-talk, as well as other parasitic coupling effects. With a much larger surface area to volume for signal transmission, the power handling capability is also improved compared to the conventional waveguide designs.

### 1.1 Bulk metal waveguide - concept and performance highlights

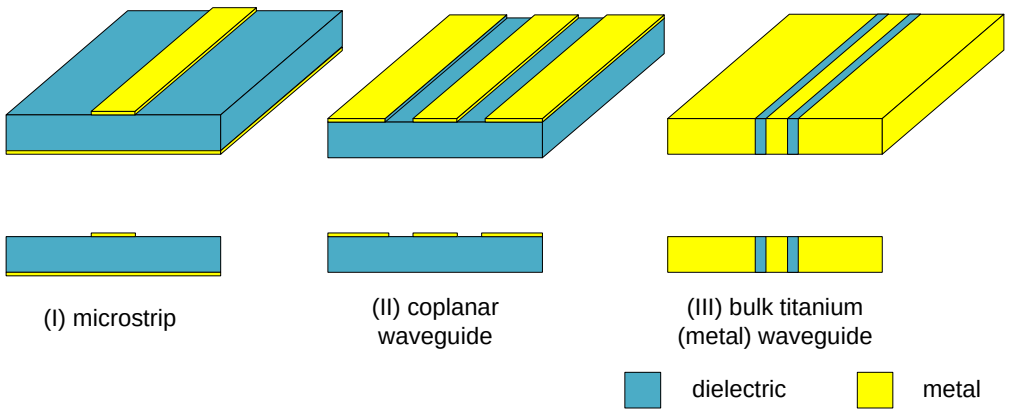


**Figure 1-1 Bulk titanium waveguide compared to conventional planar circuits**

In order to expand the utility of planar circuits, and to minimize cross-talk and undesirable coupling, a package is required, forming a cavity above the waveguide, which allows for integration of other micro-components such as an IC or MEMS. Traditional approaches either feed the signal through the sides of the package,

underneath the areas where the package is integrated on the substrate, therefore generating undesirable parasitic effects, or based on drilled via holes within the insulating substrates and subsequently filling the holes with electroplated metals, thereby reducing the performance dependency on the presence of the package. For ceramic substrates, these vias are formed either by laser drilling [11, 12] or molding in the green state of the ceramic material [13]. Both approaches are restricted by the maximum aspect ratio of the vias, hence prohibiting the inclusion of a large number of interconnects within a compact package. In addition, laser drilling induces a large amount of stress; green state fabrication is limited by the lateral precision; both approaches introduce planarity issues.

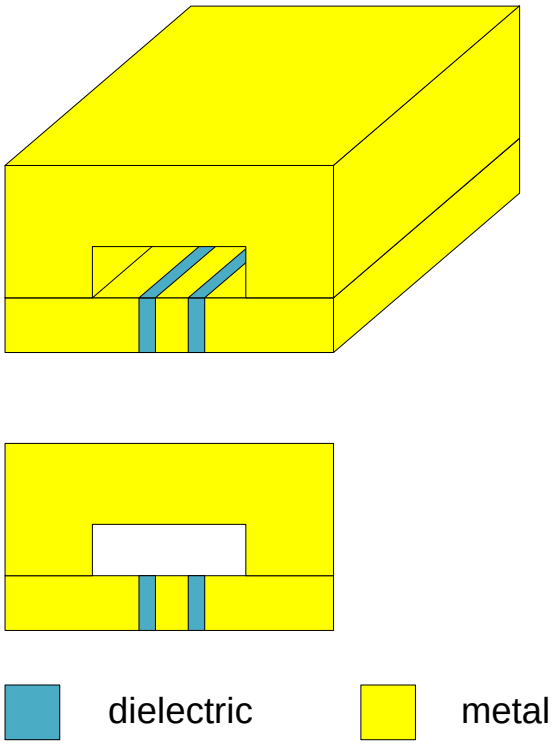


**Figure 1-2 Packaging for bulk titanium waveguide**

We propose a method that uses etching deep, high aspect ratio trenches, filling the trenches with low-loss dielectrics and planarizing the resulting structures which provide a viable solution to the above issues. In our process the trench filling dielectric material electrically isolates adjacent segments of titanium, therefore forming through-wafer/through-package electrical interconnects. Due to the high aspect ratio of the titanium etch, a high packing density of interconnects can be formed. The structures can be made symmetrical, therefore minimizing the overall stress. This is demonstrated by a 1"x1" sample that remains flat after being thinned to 30 μm. Up to 1000 V was applied across a 15 μm thick trench isolation without breakdown. The schematic of a system package is shown in Figure 1-2. Here, a bulk-titanium cavity is formed by etching and coating of a bonding agent, and the etched substrate is bonded to the RF circuit on the bulk titanium waveguide. The package further acts as the mechanical support for the RF system. Other micro-components, such as MEMS, can be integrated into the circuit prior to packaging. An important note is that the RF concept can be realized with other bulk metals as well, provided that a similar suite of fabrication techniques can be developed.

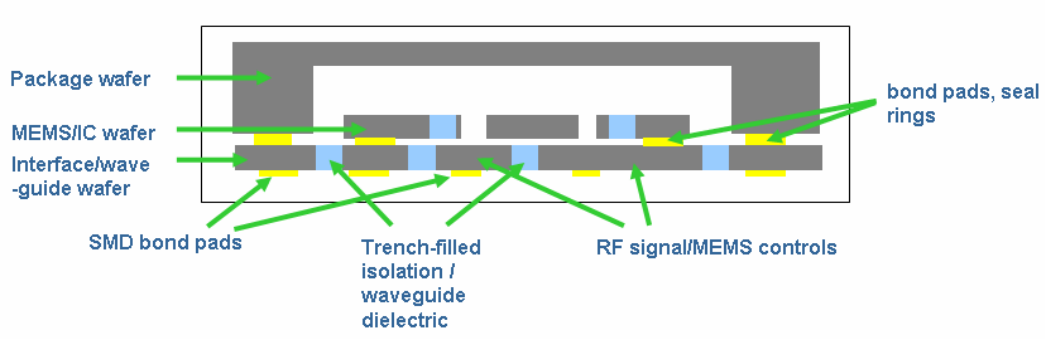


**Figure 1-3.Schematic of a RFMEM system based on packaged bulk titanium waveguide**

An example of a packaged RFMEMS system is demonstrated in Figure 1-3. Here, a MEMS device based on the same trench-filling/isolation concept is integrated inside the package through bonding.

## 1.2 Fabrication and associated issues

A simplified fabrication process flow is illustrated in Figure 1-4. Starting with a deep etch into the bulk titanium substrate [14-16], the etched trenches are filled with a low-loss dielectric material [14]. The excess dielectric is removed through a lapping process, which is also performed on the reverse side of the wafer until the bottom of the trenches is exposed. The planarization step achieves thickness uniformity across the wafer, while creating and finalizing the geometry for the waveguide electrical isolation and electrical interconnects. The package cavity is formed by etching another titanium substrate; then the two substrates are bonded together.

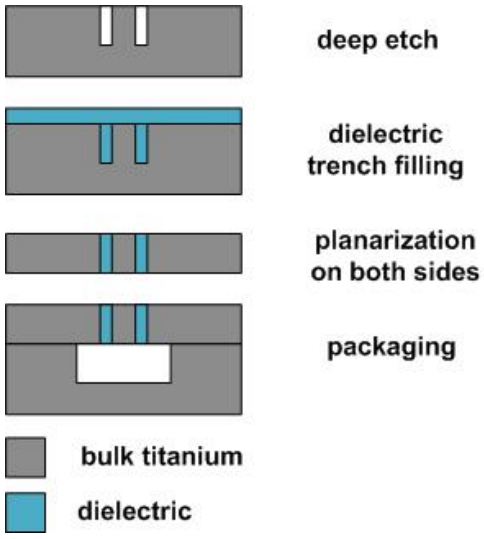


**Figure 1-4 Simplified fabrication sequence of packaged bulk titanium waveguide**

While the use of metal eliminates many RF performance issues associated with silicon, the metal substrate also introduces many fabrication issues that require attention. The manufacturing processes for bulk titanium substrates are insufficient for the required microfabrication. Routine handling, such as device singulation, generates deformations prohibitively large for subsequent processing. We have successfully developed a suite of fabrication technologies which planarizes the samples, removes the surface defects from the manufacturing processes, and ensures consistent, high aspect ratio etch results.

## 1.3 Achievement highlights

### 1.3.1 Novel planar circuit/RF platform concept

The bulk titanium waveguide provides a novel platform for planar circuitry. Based on high aspect ratio trench-filling and planarization, the resulting waveguide structure offers superior field confinement, therefore reducing parasitic coupling and loss due to radiation. The flat surface facilitates subsequent microfabrication processes, such as layer-stacking/bonding. We developed a quasi-static model that predicts the fundamental behavior of the waveguide system and verifies the model with simulation and characterization.

### 1.3.2 Suite of processing techniques which enable/enhance bulk titanium based microfabrication

Bulk titanium fabrication issues include surface defects, residual stress, substrate deformation, surface roughness and thickness variation. These challenges come from manufacturing processes which are not designed for microfabrication, and the metallic nature of titanium. Inspired by the available macroscopic processes for titanium in

traditional manufacturing, we have studied and characterized a complete planarization procedure that will minimize the residual stress, reduces gross deformations, and planarizes the substrate; the procedure also removes surface defects and provides a smooth surface finish. The result: <~2 μm thickness variation across a 1"x1" sample surface, and grass-free deep (~200 μm) etches, and with <~3 nm surface roughness.

### 1.3.3 Novel micro-component packaging solution with low parasitic coupling to package and high density, through-wafer interconnects

One of the most important features enabled by the procedures for making bulk titanium waveguides is the through-wafer electrical interconnects. The trench-filling and planarization process provide high-density, in-plane electrical isolation that offers superior performance over traditional through-via interconnects. The field confinement also significantly reduces parasitic coupling to the all-titanium packaging. A 15 μm dielectric-filled isolation is shown to withstand up to 1000V of bias without breaking down. This packaging solution offers compact construction and provides high performance for RF, MEMS, as well as other micro-components.

### 1.3.4 Experimental proof: low loss waveguides with minimal impact from packaging

With a carefully designed calibration and measurement procedure in place, the titanium waveguides measured ~2 dB/mm transmission loss. Sidewall Au coating further reduces the loss to ~<1 dB/mm. The impact of insertion loss from packaging is measured to be <0.1 dB for a 2 mm x 2 mm x 70 μm package. We also expect these results to improve over time as well as the design and fabrication procedures are further optimized.

## 1.4 Bulk titanium as MEMS material

### 1.4.1 Background

Titanium is 30% stronger than steel, but is nearly 50% lighter. Titanium is 60% heavier than aluminum, but twice as strong. In fact, titanium has the highest strength-to-weight ratio of any pure metal [15-17]. Titanium has excellent strength retention to 1,000 degrees Fahrenheit. Titanium is often alloyed with aluminum, manganese, iron, molybdenum and other metals to increase strength, to withstand high temperatures, and to lighten the resultant alloy. Another valuable characteristic is titanium's high corrosion resistance: when exposed to the atmosphere, titanium forms a tenacious oxide film that resists many corrosive environments, such as salty water. In fact, the titanium metal industry was first established in the 1950s primarily in response to the emerging aerospace industry requirements, where titanium finds applications for the manufacture of airframe structural components and skin, aircraft hydraulic systems, air engine components, rockets, missiles, and space craft, where these above-mentioned properties are highly valued.

Before the 1970s, titanium had been mainly used in aerospace applications. As the cost of titanium products dropped, it gradually made its way into other practical uses such as shipbuilding: primarily in submarines, in ship's propellers, shafts, rigging, and other highly corrosive parts.

Another remarkable characteristic of titanium is its suitability in medical applications [18, 19]. Due to its light weight, its strength, and its immunity to corrosion and biocompatibility, titanium is widely used in applications such as bone and dental implants, cardiovascular devices, external prostheses and surgical instruments. Titanium products are also becoming increasingly utilized in other industries as well, from petrochemical applications to sporting goods.

### 1.4.2 Bulk titanium MEMS

Micro-electro-mechanical Systems (MEMS) emerged from technological advances in semiconductor technologies and extended existing material processing techniques to achieve new, sometimes 3-dimensional, structures with unique functions. Since their first debut as a capacitive actuator made with deposited polysilicon chemically released, MEMS have taken on many different shapes, materials and structures. Applications that have been realized by taking advantage of MEMS' unique characteristics include mechanical, chemical, optical [20, 21] and wireless/RF [22, 23]. A wide range of novel structures have been implemented to better serve the applications for which these systems were employed. These structures can be categorized into two main types: surface and bulk MEMS. Surface MEMS rely on the layers of materials deposited and subsequently released to realize movable or 3-dimensional structures – a good example being the standardized multi-user MEMS processes (MUMPS) process [24, 25]. The substrate primarily functions as a mechanical support. Bulk MEMS involve etching of the substrate – often with high aspect ratios -- and the resulting structures are often embedded within the substrate. Bulk MEMS utilize the entire depth of the substrate; therefore significantly enhance the volume efficiency of the system, as well enabling more functional surface areas per unit chip area. For RF applications of most currently employed frequency ranges, due to the diversified nature of electromagnetic waves, the substrate has a large impact on system performance. In fact, silicon, due to its high loss tangent at most usable RF frequencies, often leads to significant performance losses [26]. Titanium offers superior conductivity and magnetic transparency, therefore is a material more suited as the substrate for RF applications.

As one of a few materials showing an endurance limit, or fatigue limit [17, 27, 28], below a threshold stress level, titanium will not fail given a near infinite number of

cycles; whereas materials with no endurance limit fail at a small fraction of the tensile strength. This critical aspect was one of the main reasons why titanium was chosen as an alternative to silicon in the fabrication of MEMS. We chose commercially pure, grade 1 (CP1), titanium as our substrate material to avoid the potential complications of using alloys in chemical-sensitive MEMS processes such as plasma etching.

Another important characteristic of titanium-based materials is the reversible transformation of the crystal structure from alpha ($\alpha$, hexagonal close-packed) structure to beta ($\beta$, body-centered cubic) structure at moderate threshold temperatures. This allotropic behavior, which depends on the type and amount of alloy contents, allows complex variations in microstructure and more diverse strengthening opportunities than those of other nonferrous alloys such as copper or aluminum.

Table 1-1 compares titanium, as well common titanium compounds, with common semiconductor/MEMS materials. Titanium has a fracture toughness of 50 $MPam^{1/2}$, close to 2 orders of magnitude higher than that of Single Crystel Silicon (SCS) (7 $MPam^{1/2}$), which makes titanium a more robust material candidate for packaging. Like SCS, titanium can be planarized and polished to provide sufficient smoothness and planarity for sub-micron semiconductor processes. The Mohs hardness of titanium, 6.0, -- although not as high as SCS (7.0) or some harden steels – is much greater than that of most pure metals, thus earning titanium the scientifically inaccurate name “sharpest metal”.

### 1.5 Current development in TiMEMS

One of the most important requirements for bulk substrate material in MEMS, is the ability to support high aspect ratio trench etching. The discovery of anisotropic plasma etching of bulk titanium [14-16] has opened new doors to bulk titanium

MEMS. M. Aimi et. al. demonstrated the first bulk titanium MEMS device [29] – titanium mirror arrays.

**Table 1-6 Titanium compounds vs. common MEMS materials**

| | SC Si | Poly Si | SiO2 | Si3N4 | SiC | TEOS |
|---|---|---|---|---|---|---|
| Elastic Modulus (Gpa) | 63-170 | 134 | 90 | 300 | 410 | 74 |
| Density (kg/m3) | 2329 | 2330 | 2200 | 3440 | 3160 | 2150 |
| Resistivity (ohm m) | | | 1.00E+16 | | 1.00E+02 | 1.00E+16 |
| Specific modulus (E/p) | 7.30E+07 | 5.75E+07 | 4.09E+07 | 8.72E+07 | 1.30E+08 | 3.44E+07 |
| Acoustic Velocity (m/sec) | 8.54E+03 | 7.58E+03 | 6.40E+03 | 9.34E+03 | 1.14E+04 | 5.87E+03 |
| Thermal Expansion (K-1) | 2.60E-06 | | 5.00E-07 | 8.00E-07 | 3.30E-06 | 5.00E-07 |
| Thermal Cond. (W/m K) | 124 | 29 | 1.4 | 29 | 120 | 0.9 |
| Dielectric Constant | 11.9 | 11.8 | 3.9 | 8 | 9.7 | 4.3 |
| Melting Temperature ( C ) | 1414 | 1414 | 1722 | 1900 | 2830 | 1722 |
| Hardness Mohs (knoop) | 7 | | 6.5 | | 9.3 (2500) | |
| Fracture Toughness (Mpa) | 0.8 | | 0.95 | 6 | 3.5 | |
| Structure | Diamond | Amorphous | Quartz | Amorphous | Wurtzite | Amorphous |
| | Ti | TiO2 | TiB2 | TiC | TiN | AlN |
| Elastic Modulus (Gpa) | 108 | 282 | 400 | 100-500 | 600 | 394 |
| Density (kg/m3) | 4506 | 4230 | 4380 | 4900 | 5210 | 3200 |
| Resistivity (ohm m) | 3.90E-07 | 0.1 | 9.00E+04 | 0.005 | 2.05E-07 | |
| Specific modulus (E/p) | 2.40E+07 | 6.67E+07 | 9.13E+07 | 6.12E+07 | 1.15E+08 | 1.23E+08 |
| Acoustic Velocity (E/p)1/2 | 4.90E+03 | 8.16E+03 | 9.56E+03 | 7.82E+03 | 1.07E+04 | 1.11E+04 |
| Thermal Expansion (K-1) | 8.60E-06 | 7.50E-06 | 5.60E-06 | 6.40E-06 | 6.30E-06 | 4.15E-06 |
| Thermal Cond. (W/m K) | 21.9 | 6.7 | 25 | 25 | 29 | 280 |
| Dielectric Constant | | 86-170 | | | | 4.7 |
| Melting Temperature ( C ) | 1668 | 1830 | 3225 | 3140 | 2950 | 3000 |
| Hardness Mohs (knoop) | 6.0 | 6.2 | (2850) | (2470) | 9 (1770) | (1225) |
| Fracture Toughness (Mpa) | 50 | 5 | 4 | 3 | 5 | 3 |
| Structure | Hexagonal | Rutile | Hexagonal | Cubic | Cubic | Wurtzite |

E. Parker et. al. [30, 31] extended the plasma etch process and explored the use of bulk titanium in multi-layer needles for potential use in drug delivery into human bodies. I. Tuval et. al. [16] took advantage of the 3-dimensional nature of deep etched titanium substrates and obtained dielectrophoretic(DEP)-based micron-sized particle separation within liquid-filled channels.

Under a DARPA funded project, we developed the first packaged bulk titanium waveguide (BTW) structure that is of low loss and is capable of serving as the backbone for a bulk titanium package solution with high interconnect density for MEMS and other micro-components. As a demonstration, C. Ding et al. [32] fabricated a bulk titanium switch capable of 15 billion stiction-free contact cycles and is compatible with BTW integration.

## 1.6 Dissertation organization

The basic concept of the bulk titanium waveguide is covered in Chapter 2. The key distinctions from the conventional planar waveguides are analyzed in detail. To help visualize the behavior of the waveguide, an analytical model is derived based on conformal mapping, which also provides a qualitative understanding of how the waveguide behaves and how key characteristics, such as impedance and losses, depend on the waveguide parameters. Some of the negative byproducts of introducing titanium, a non-single-crystal, and non-semiconductor grade substrate, include manufacturing limitations, such as residual stress, embedded defects and thickness variations; and deformations from routine handling such as chip singulation. These byproducts pose severe challenges for the successful realization of a bulk titanium waveguide as well as many other RFMEMS. Chapter 3 discusses the suite of technologies we developed to overcome these issues. The result is substrates with < 2 m thickness variation and ~2.8 nm average roughness. Once the substrate is planarized and free of embedded defects from manufacturing processes, deep trenches are etched and filled with a low-loss dielectric material. The details and results are illustrated in Chapter 4.

One of the biggest challenges of high frequency circuits is the difficulty involved in predicting the measured behavior, especially for low-loss passive components. Minute variations in measurement procedures can affect the measurement results significantly. We established a complete set of measurement procedures, including on-chip TRL calibration standards. Chapter 5 describes the experimental setup and discusses the measurement results. Finally, we look into the future extensions of the technology by studying some examples such as band-pass filters, which take advantage of the unique properties of the bulk titanium waveguide concept.

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# CHAPTER 2

# CONCEPT AND THEORETICAL ANALYSIS FOR PACKAGED BULK-TITANIUM WAVEGUIDE

## 2.1 Concept and key features

The key objective of our research is the construction of a robust micro-packaged solution for a low-loss RF waveguide platform. The physical, as well as chemical, robustness lies in the unique material advantages of titanium. In addition, the metallic nature of titanium, can be utilized to achieve unique advancements in RF performance when compared to conventional choices of RF circuit substrates. Conventional construction of planar circuits, i.e., microstrip [6, 25] and coplanar waveguides (CPW) [6, 1], is based on substrates such as silicon, gallium arsenide, and ceramics. These substrates share one common property: all of them are considered insulators in the most simplistic models. Current is mostly carried by metal traces deposited on the horizontal, planar surfaces of the substrate. Packages for such circuits are typically formed by bonding metal caps on top. Electrical interconnects are achieved either by running signal traces underneath the metal caps with a thick insulating layer in between to reduce parasitic loss, or by forming through-wafer conductive paths with electroplating. Either approach poses challenges on system performances.

With a metallic substrate, we are granted the option to revolutionize the fundamental topology of those conventional RF platforms. Instead of using the substrate as the dielectric, our waveguides are formed by creating deep, narrow trenches in the conductive substrate, filling them with low-loss dielectrics and then planarizing the resulting structure to form bulk titanium “islands” separated by high aspect ratio dielectrics. The electromagnetic signal being transmitted is mostly

confined within the gaps between the conductors, due to the high aspect ratio of the trenches. This superior field confinement, as well as the in-situ through-wafer construction, facilitates the implementation of low-parasitic packaging. In addition, the same process used for the waveguides also forms through-wafer electrical interconnects. The recent developments in bulk titanium etching as well as trench filling and planarization allow for high interconnect packing density.

### 2.1.1 Background: Planar circuitry- microstrip and CPW

As two of the most common forms of uni-planar RF circuits, CPW and microstrip are not only the foundation of many commercial RF systems, but also used to fabricate most RFMEMS [6] devices. As shown in Figure 2-1, a microstrip waveguide is composed of a patterned thin metal line -which carries the RF signal- on top of an insulating substrate with a large (often approximated as infinite) metal ground plane deposited on the opposite side.

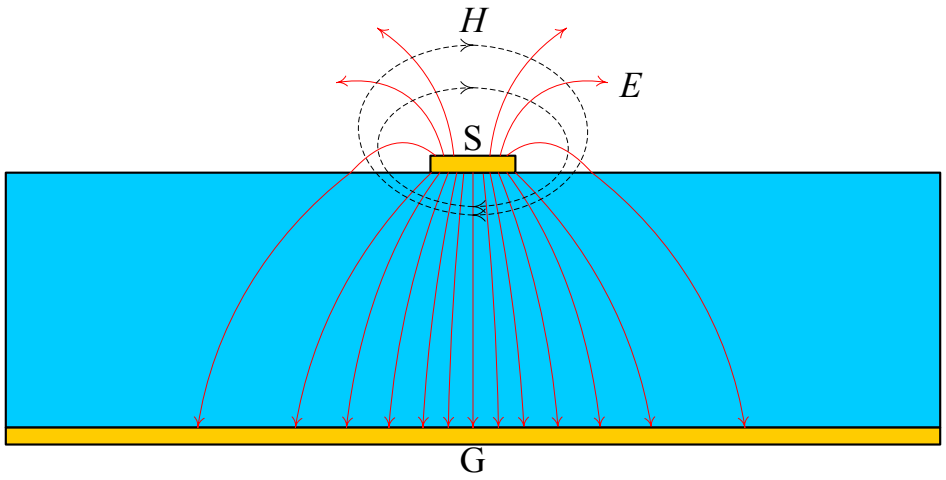


**Figure 2-1 Schematic of a microstrip waveguide**

The simplicity of the signal line makes it easy to implement many RF/microwave functions, such as filters, splitters and combiners, couplers etc. However, heterogeneous integration of other devices can pose significant challenges due to the complexity of grounding, which typically involves drilling holes through the insulating substrates and filling them with metals, an expensive process that takes up much area and creates issues such as planarity and stress. The lack of grounding on the signal plane also causes the microstrip waveguide to be more susceptible to undesirable coupling to nearby devices.

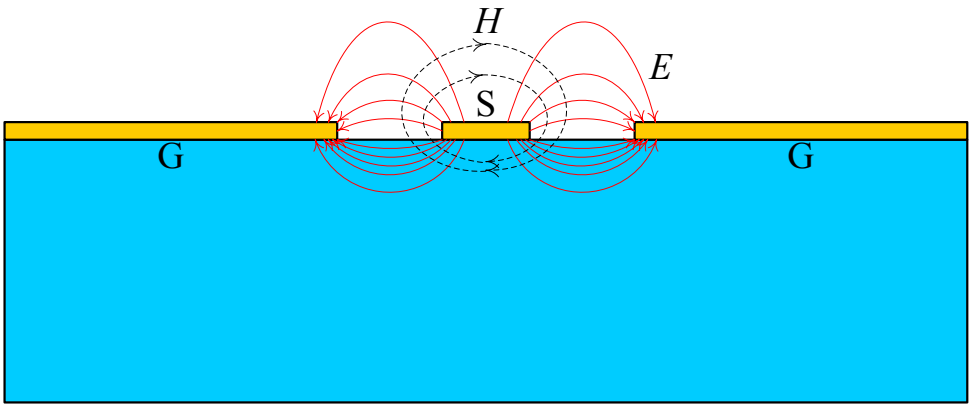


**Figure 2-2 Schematic of a CPW**

First proposed in 1969 [6, 1], a CPW consists of a signal-carrying metal line sandwiched between metal ground lines/large areas that are fabricated on the same plane (Figure 2-2). Raising the ground to the same plane as the signal line creates in-situ shielding and results in less parasitic coupling and radiation loss. The inclusion of grounds also helps facilitate the heterogeneous integration of devices and systems. These advantages over microstrip, however, also come with tradeoffs. The

propagation currents concentrate on the thin edges of the metal traces as opposed to the bottom of the microstrip lines, which is much broader. This results in greater loss due to the finite conductivity of the metal. In addition, the absence of the unified ground plane makes the ground areas more likely to suffer from potential drifts, especially at discontinuities such as bends and tapers. The additional conductor also lends itself to the creation of more propagation modes. As a result, especially for higher frequency applications, CPW design often involves tight tolerances and additional fabricated features such as air bridges.

### 2.1.2 High aspect ratio metal CPW

Conventional uniplanar RF circuits are fabricated on insulating substrates and the thickness of the metal lines are usually 2-5 μm, i.e., within an order of magnitude of the skin depth at the frequency for the application. The gap between the signal and ground is typically much greater than the thickness of the metal. For example, for a 50 Ω waveguide fabricated with 5 μm thick gold on a 1 mm thick alumina substrate with 100 μm center conductor width, the gap between signal and ground is ~100 μm, which means an aspect ratio between the thickness of metal and the gap of 1:20. As a signal propagates along the waveguide, such a low aspect ratio means poor field confinement and coupling to devices within a few hundred microns. Kudrle et. al. [21] fabricated high aspect ratio parallel plate waveguides by releasing bulk silicon structures from the substrate. The silicon substrate in close vicinity of the electromagnetic field is removed by dry etching. The first published high aspect ratio metal CPW [7; 8] used the LIGA process - a combination of deep X-ray lithography and electroplating techniques - and fabricated CPWs with metal thickness up to a few hundred microns with a gap as small as 10-15 μm. Couplers and filters were made to take advantage of the tight coupling achieved by the high aspect ratio fabrication

capability. Both types of high aspect-ratio transmission lines are suited for stand-alone devices that need to be integrated to a conventional planar circuit.

### 2.1.3 Bulk titanium/metal waveguide

The principle of the bulk titanium waveguide is illustrated in Figure 2-3 and Figure 2-4, where the key idea for the waveguide construction is a micron-sized parallel plate structure realized vertically. Parallel plate offers superior field confinement compared to CPW and microstrip waveguide. This helps to reduce parasitic coupling, which in turn reduces the minimum package size. High aspect ratio etching of bulk titanium, along with trench-filling with insulating dielectrics and planarization, create through-wafer (and through-package), electrically isolated conductors that serve as interconnection paths for signal feed-thrus. The flat surface obtained by the planarization process enables easy integration of additional processes, such as surface MEMS or wafer/chip bonding.

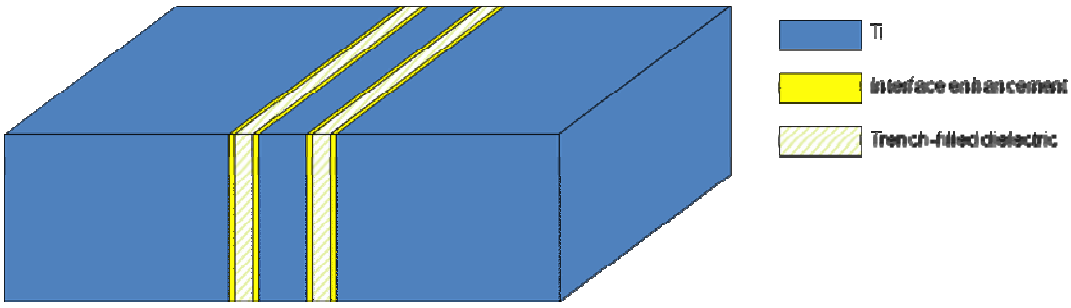


**Figure 2-3 3-dimensional schematic of bulk titanium waveguide**

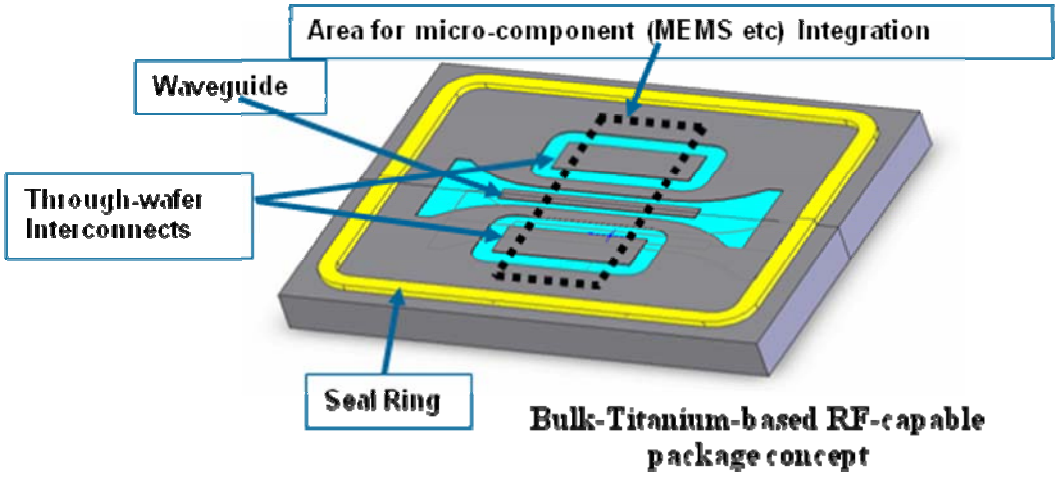


**Figure 2-4 Bulk-titanium packaged waveguide with interconnects and seal ring for packaging**

A simplified fabrication process is illustrated in Figure 2-5, in which only one waveguide structure is included. A surface enhancement layer is used to denote adhesion promoter, diffusion barrier, conductivity enhancement as well as bonding agent. As depicted in the schematic, the waveguide consists of three conductors of the same height with straight sidewalls. The center conductor is symmetrically placed in the middle, separated from the other two conductors by identical gaps that are much narrower than the waveguide height, therefore creating an electromagnetic configuration of a parallel plate waveguide. The signal is carried by the center conductor whereas the other two conductors serve as grounds – a configuration shared by conventional CPW. The system is completed by bonding a cap wafer/chip as the package. The majority of the package material is bulk titanium, and the cavity formed is sealed completely from the outside.

Compared with LIGA fabricated high aspect ratio CPW, the trench-filled bulk titanium waveguide offers the following advantages:

- Integrated bulk-metal-packaged solution

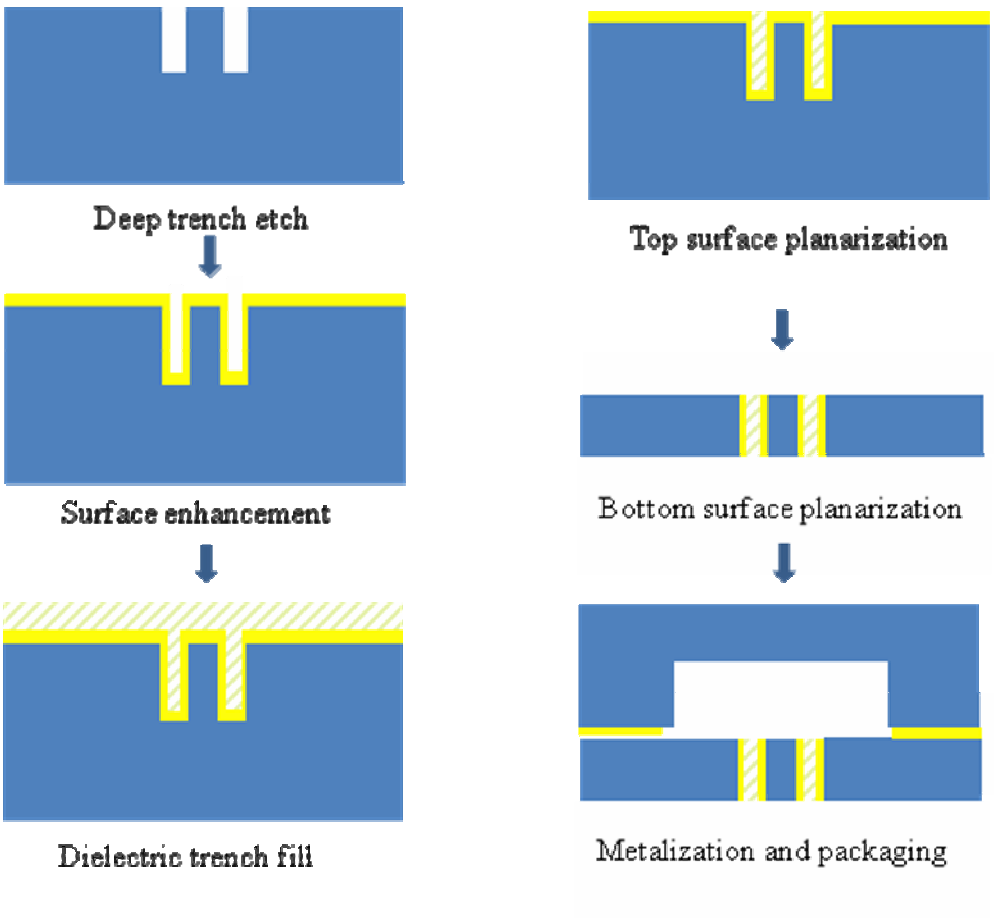


**Figure 2-5 Fabrication process for bulk titanium waveguide**

- No need of another RF substrate
- Planar surface for subsequent processing
- Integrated high density electrical interconnect

Topologically, our high aspect ratio, bulk titanium/metal waveguide can be seen as a new way to make high aspect ratio metal structures. Functionally, it also provides a flat, mechanically contiguous surface for subsequent processing and embedded high density, through-wafer electrical interconnects for electronic/RF packaging. The high electromagnetic field confinement helps minimize crosstalk and parasitic coupling to the package.

Starting with a bulk titanium material, our planarization technique provides a finely polished surface flat enough for subsequent process steps. Our unique dry etching process enables the etching of deep, straight trenches that can be placed microns apart. Trenches are then filled with a low-loss dielectric material and back lapped/polished to reach the dielectric from the reverse side, we achieve a uniplanar structure composed of high aspect ratio bulk titanium structures with dielectric material between providing electrical isolation and mechanical linkage, as shown in Figure 2-5. The resulting planar surfaces facilitate subsequent process steps to integrate devices such as MEMS. In particular, a package can be formed by bonding a bulk titanium cavity. While the sealed cavity protects the enclosed devices against moisture, the embedded, electrically isolated, high aspect ratio titanium islands provide high density interconnects that can be shielded and minimally coupled to the package.

## 2.2 Microwave modeling

### 2.2.1 Waveguide fundamentals

The characteristic of waves propagating in a waveguide can be derived from Maxwell's equations. The derivation of the wave characteristics in a generalized waveguide with a uniform cross section is shown in Appendix A and can be found in many sources . The propagation constant, $\gamma_{TEM}$, for transverse electromagnetic (TEM) waves, where $E_z=0$ and $H_z=0$, is as follows:

$$\gamma_{TEM} = jk = j\omega\sqrt{\mu\varepsilon}\,. \tag{2.1}$$

The corresponding phase velocity is therefore

$$u_{p(TEM)} = \frac{\omega}{k} = \frac{1}{\sqrt{\mu\varepsilon}}\,. \tag{2.2}$$

The wave impedance, defined as the ratio between the transverse components of E and H following a right hand rule, i.e., the ratio between $E_x^0$ and $H_y^0$, can be derived:

$$Z_{TEM} = \frac{E_x^0}{H_y^0} = \frac{j\omega\mu}{\gamma_{TEM}} = \frac{\gamma_{TEM}}{j\omega\varepsilon} = \sqrt{\frac{\mu}{\varepsilon}} \equiv \eta . \tag{2.3}$$

The characteristic impedance $Z_0$, defined by the ratio between the magnitudes of the harmonically varying voltage and current signals propagating down the waveguide, can be derived from the correlation between these signals and their corresponding wave characteristics.

The characteristic impedance $Z_0$, defined by the ratio between the magnitudes of the harmonically varying voltage and current signals propagating down the waveguide, can be derived from the correlation between these signals and their corresponding wave characteristics.

The impedance of a uniform waveguide is given by the general transmission line theory [9]:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}, \tag{2.4}$$

where R, L, G, C are the distributed values of the conductor series resistance, the conductor series inductance, the dielectric conductance and the dielectric capacitance per unit length, respectively. For a low loss waveguide, i.e.,

$$\begin{aligned} \omega L &>> R \\ \omega C &>> G, \end{aligned} \tag{2.5}$$

Eq. (2.4) simplifies into

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{2.6}$$

The corresponding propagation constant defined in Eq. (2.6) is

$$\gamma = \alpha + i\beta = \sqrt{(j\omega L + R)(j\omega C + G)}, \tag{2.7}$$

and simplifies into $\gamma = j\omega\sqrt{LC}$, for a low loss waveguide.

Our analyses will be focused on a quasi-TEM assumption. The fundamental mode of propagation in a two-conductor transmission line such as a coaxial line is essentially a Transverse Electromagnetic Mode (TEM) when the conductors are considered to have infinite conductivity and the dielectric medium is homogeneous, lossless, and isotropic [10]. In practice such requirements are seldom satisfied; they usually have inhomogeneous dielectric or multi-layered structures, which cannot support pure TEM mode propagation. However, at low microwave frequencies (below X- band) the non-TEM nature can be ignored because waveguide dimensions are much smaller than the guided wavelength, the propagation mode closely resembles the TEM mode, and the longitudinal component of the electromagnetic field is small compared to those in the transverse directions. Then the 3-dimensional electromagnetic problem can be reduced to a solution of 2-dimensional Laplace's equation subject to the boundary conditions that lead to a quasi-static transmission line analysis based on TEM mode assumption.

### 2.2.2 1st order RF characteristics of bulk titanium waveguide

The cross section of a bulk titanium waveguide is shown in Figure 2-6. The lateral dimension of the grounds is extended to infinity.

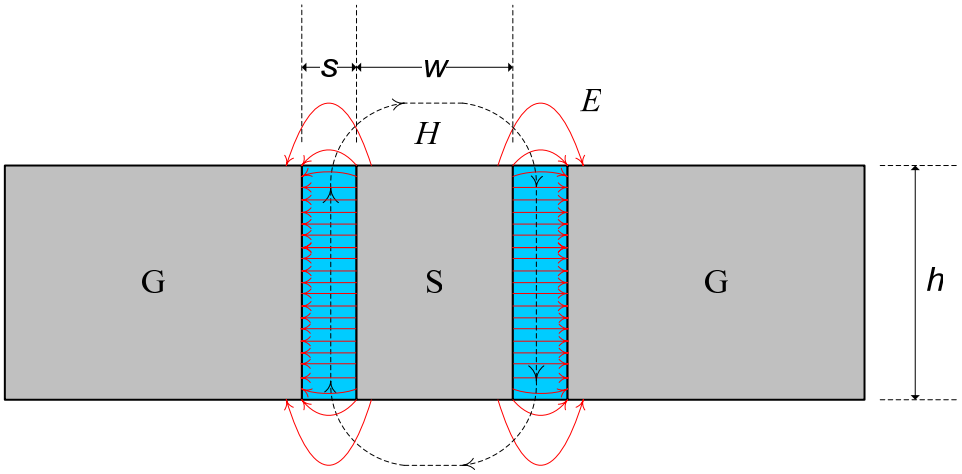


**Figure 2-6 Cross section of bulk titanium waveguide**

Due to the high aspect ratio construction, the geometry of a bulk titanium waveguide resembles that of two parallel plate capacitors in parallel. Considering a TEM mode of wave propagation, the distributed parameters of the waveguide can be derived from a linear model:

$$\begin{aligned} L &= \frac{2\mu_d \mu_0 s}{h} \\ C &= \frac{2\varepsilon_d \varepsilon_0 h}{s} \\ R &= \frac{4R_s}{h} \\ G &= \frac{2\sigma_d h}{s}, \end{aligned} \tag{2.8}$$

where $\mu_c$ and $\mu_d$ are the permeability of the conductor and dielectric, respectively; $\varepsilon_d$ is the permittivity of the dielectric material; $\sigma_d$ is the conductivity of the dielectric material; $R_s$ is the surface resistivity related to the skin depth of the conductor defined as:

$$R_s = \sqrt{\frac{\pi f \mu_c \mu_0}{\sigma_c}} = \sqrt{\frac{\omega \mu_c \mu_0}{2\sigma_c}}, \tag{2.9}$$

where $\sigma_c$ is the conductivity of the conductor. Using Eqs. (2.8) and (2.9) in Eq. (2.4), the characteristic impedance of bulk titanium waveguide is given by

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{\frac{\frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}} + j\omega\frac{\mu_d\mu_0 s}{h}}{\frac{\sigma_d h}{s} + j\omega\frac{\varepsilon_d\varepsilon_0 h}{s}}}. \tag{2.10}$$

Note that it is customary to describe the loss of a dielectric by introducing an imaginary term into its permittivity:

$$\varepsilon_{complex} \equiv \varepsilon' - j\varepsilon'' = \varepsilon_d\varepsilon_0 + \frac{\sigma_d}{j\omega}, \tag{2.11}$$

where $\varepsilon'$ and $\varepsilon''$ are the real and imaginary parts, respectively. Conventionally, loss tangent, $\tan\delta_d$, is often used to gauge the loss of a dielectric:

$$\tan\delta_d \equiv \frac{\varepsilon''}{\varepsilon'} = \frac{\sigma_d}{\omega\varepsilon_d\varepsilon_0}. \tag{2.12}$$

For a low loss waveguide, the characteristic impedance is linked directly to the aspect ratio:

$$Z_0 = \frac{s}{h}\sqrt{\frac{\mu_d\mu_0}{\varepsilon_d\varepsilon_0}}. \tag{2.13}$$

### 2.2.3 Conformal mapping analysis

The first order calculation, as shown in Eqs. (2.8), ignores the fringing field. More accurate modeling of the deviation typically involves conformal mapping, which transforms the more complex geometry into one which has an accurate first order

solution [12; 11] . Problems with similar geometries have been solved in the past for parallel plates surrounded by homogeneous dielectric media, microstrips, slot lines and CPWs [9; 14; 13]. Due to the presence of the dielectric-air interface, a direct mapping of the entire geometry will not result in a solvable problem. To address this specific geometry, we start out by assuming that the interface between trench-filling dielectric and air coincides with a magnetic wall, similar to the treatment used in the derivation for slot lines and CPWs [14] (an alternative approximation is to assume a homogeneous dielectric distribution and use a mapping analysis for the parallel plate waveguide, as shown in Appendix B). Thus, the problem is divided into two regions:

$$\text{Region I } (x \geq 0; y \geq h/2): \begin{array}{l} V = V_0; x = 0 \rightarrow w/2 \\ V = 0; x = w/2 \rightarrow \infty \end{array} \tag{2.14}$$

$$\text{Region II } (x \geq 0; h/2 \geq y \geq 0): \begin{array}{l} V = V_0; x = w/2 \\ V = 0; x = w/2 + S \\ \dfrac{\partial V}{\partial y} = 0; x = w/2 \rightarrow w/2 + S, y = 0 \rightarrow h/2 \end{array} \tag{2.15}$$

This is illustrated in Figure 2-7. Here the contribution of the fringing field is entirely represented in region I.

For Region II, the problem reduces to that of a first-order parallel plate solution and the capacitance per unit length is given by

$$C_{II} = 4 * \varepsilon_0 \varepsilon_d \frac{h/2}{S} = 2\varepsilon_0 \varepsilon_d h / S \tag{2.16}$$

where the factor of 4 comes from symmetry.

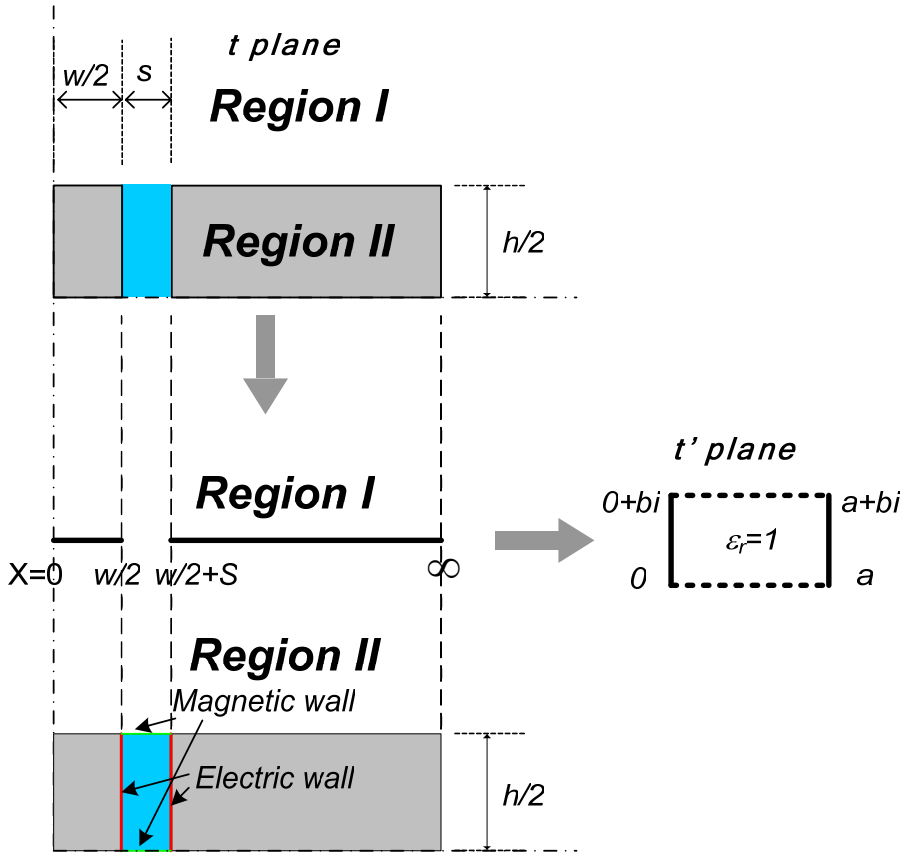


**Figure 2-7 Conformal map for bulk titanium waveguide analysis**

For Region I, the problem is identical to the upper plane of a CPW. This region may be transformed into the interior of a rectangle in t' plane by the following Schwartz-Christoffel transformation [15]:

$$\frac{dt'}{dt} = \frac{A}{\sqrt{[t^2 - (w/2)^2][t^2 - (w/2+S)^2]}}, \tag{2.17}$$

where A is a constant. The values a and b in the t' plane are therefore:

$$a + jb = \int_0^{w/2+S} \frac{Adt}{\sqrt{[t^2 - (w/2)^2][t^2 - (w/2+S)^2]}}. \tag{2.18}$$

The ratio a/b is simply

$$\frac{a}{b} = \varepsilon_0 \frac{K(k)}{K'(k)} = \varepsilon_0 \frac{K(k)}{K(k' = \sqrt{1-k^2})}, \tag{2.19}$$

where $\varepsilon_r$ is the permittivity of the dielectric, $k \equiv w/(w+2S)$ and K(k) is the complete elliptical integral of the first kind [16]. Therefore, the capacitance per unit length is

$$C_I = 4 * \varepsilon_0 \frac{a}{b} = 4\varepsilon_0 \frac{K(k)}{K'(k)} \tag{2.20}$$

Combining (2.16) with (2.20) gives the total capacitance per unit length:

$$C = C_I + C_{II} = \varepsilon_0 [\frac{4K(k)}{K'(k)} + \frac{2\varepsilon_d h}{S}] \tag{2.21}$$

The inductance per unit length, however, is calculated differently. The current distribution needs to be taken into account when considering the different contributions from the parallel plate and the CPW structures. A more accurate model would be to start from the uniform current distribution in the mapped geometry [9]. However, considering the fact that the current concentrates on the sidewalls of the parallel plate structures, the inductance per unit length can be approximated to be a parallel plate structure:

$$L \approx \frac{\mu_0 \mu_d s}{2h} \tag{2.22}$$

where $\mu_d$ is the permeability of the dielectric material in the parallel plate structure; the factor of 2 comes from the fact that two sides of the waveguide compete for current. The impedance of the lossless waveguide is therefore

$$Z_0 = \sqrt{\frac{L}{C}} \approx \frac{1}{2} \sqrt{\frac{\frac{\mu_0 \mu_d s}{h}}{\varepsilon_0 [\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{S}]}} \tag{2.23}$$

Note that Eq. (2.23) ignores the effect of field penetration into metals of finite conductance, or skin effect [2], which leads to additional contribution to the inductance from added magnetic flux. Using the incremental inductance rule on the parallel plate waveguide, the additional inductance (per unit waveguide length), ΔL, can be expressed as:

$$\Delta L = 2 \cdot \mu_c \cdot \frac{1}{2}\sqrt{\frac{2}{\omega\mu_0\mu_c\sigma_c}} \cdot \frac{\partial L_{ext}}{\partial s} \approx \frac{\mu_d}{2h}\sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}}, \tag{2.24}$$

where $L_{ext}$ is the external inductance from Eq. (2.22).

Combing Eq.s (2.23) and (2.24), the characteristic impedance of the bulk titanium waveguide is

$$Z_0 = \frac{1}{2}\sqrt{\frac{\frac{\mu_0\mu_d s}{h} + \frac{\mu_d}{h}\sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}}}{\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}} = \frac{1}{2}\sqrt{\frac{\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})}{\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}}. \tag{2.25}$$

To obtain the loss (the resistive terms) - due to the finite conductivity of the conductors as well as the non-zero conductivity of the dielectric - need to be inserted into Eq. (2.25):

$$\begin{aligned} Z_0 &= \sqrt{\frac{\frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}} + j\omega\frac{\mu_d}{2h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})}{\frac{2\sigma_d h}{s} + j\omega\varepsilon_0[\frac{4K(k)}{K'(k)} + \frac{2\varepsilon_d h}{s}]}} \\ &= \frac{1}{2}\sqrt{\frac{\frac{4}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}} + j\omega\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})}{\frac{\tan\delta_d\omega\varepsilon_d\varepsilon_0 h}{s} + j\omega\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}} \end{aligned} \tag{2.26}$$

where the conductivity of the dielectric has been replaced by the more commonly used loss tangent, as defined in Eq. (2.12).

The propagation constant can be obtained similarly, from Eq. (2.7):

$$\gamma = \alpha + j \cdot \beta = \sqrt{Z \cdot Y} = \sqrt{(R + j\omega L)(G + j\omega C)}$$
$$= \sqrt{\{\frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}} + j\omega\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})\} \cdot \{\frac{\tan\delta_d \omega\varepsilon_d\varepsilon_0 h}{s} + j\omega\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]\}} \quad (2.27)$$

Consequently, the total loss can be expressed in terms of the waveguide characteristics:

$$\alpha = \mathrm{Re}(\gamma)$$
$$= \mathrm{Re}\{\sqrt{\{\frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}} + j\omega\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})\} \cdot \{\frac{\tan\delta_d \omega\varepsilon_d\varepsilon_0 h}{s} + j\omega\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]\}}\} \quad (2.28)$$

Note that the above loss includes contributions from both the conductor and the dielectric. In cases where the conductor loss dominates, i.e., $\tan\delta_d \sim 0$, Eq. (2.28) becomes:

$$\alpha = \mathrm{Re}\{\sqrt{\{\frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}} + j\omega\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})\} \cdot \{j\omega\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]\}}\}$$
$$\approx \mathrm{Re}\{\sqrt{\{-\omega^2\frac{\varepsilon_0\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]\} + j\frac{2\omega\varepsilon_0}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}\} \quad (2.29)$$

Rewriting Eq. (2.7) in triangular function, the loss can be expressed in a more convenient form:

$$\alpha = \mathrm{Re}(\gamma) = \mathrm{Re}\{\sqrt{(j\omega L + R)(j\omega C + G)}\}$$
$$= \sqrt{A}\cos\frac{\theta}{2} \tag{2.30}$$

where

$$A = \sqrt{(RG - \omega^2 LC)^2 + \omega^2 (LG + RC)^2}$$
$$\theta = \arctan[\frac{\omega(LG + RC)}{(RG - \omega^2 LC)}] \tag{2.31}$$

For loss-loss waveguides, where Eq.s (2.5) apply, θ ~ π and Eq. (2.30) can be approximated using the Taylor expansions of triangular functions:

$$\alpha = \sqrt{A}\cos\frac{\theta}{2} \approx \sqrt{A}\frac{1}{2}[\frac{\omega(LG + RC)}{(RG - \omega^2 LC)}] \approx \frac{LG + RC}{2\sqrt{LC}} \tag{2.32}$$

Plugging the expressions for the distributed impedance values, Eq. (2.32) is then

$$\alpha \approx \frac{LG + RC}{2\sqrt{LC}} = \frac{\frac{\mu_d \tan\delta_d \omega\varepsilon_d\varepsilon_0}{s}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}}) + \frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}{2\sqrt{\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}} \tag{2.33}$$

For very high frequencies, when the internal inductance can be neglected, Eq. (2.33) can be simplified:

$$\alpha \approx \frac{\mu_0\mu_d \tan\delta_d \omega\varepsilon_d\varepsilon_0 + \frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}{2\sqrt{\frac{\mu_0\mu_d\varepsilon_0 s}{h}[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}} \tag{2.34}$$

The loss can be divided into two parts, conductor loss: $\alpha_c$, and dielectric loss: $\alpha_d$:

$$\alpha_c \approx \frac{\frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}\varepsilon_0[\frac{2K(k)}{K'(k)}+\frac{\varepsilon_d h}{s}]}{2\sqrt{\frac{\mu_0\mu_d\varepsilon_0 s}{h}[\frac{2K(k)}{K'(k)}+\frac{\varepsilon_d h}{s}]}} \approx \sqrt{\frac{\omega\mu_c\varepsilon_0}{2\mu_d\sigma_c hs}[\frac{2K(k)}{K'(k)}+\frac{\varepsilon_d h}{s}]} \sim \sqrt{\omega}\,, \tag{2.35}$$

$$\alpha_d \approx \frac{\tan\delta_d\omega\varepsilon_d\varepsilon_0}{2\sqrt{\frac{\varepsilon_0 s}{\mu_0\mu_d h}[\frac{2K(k)}{K'(k)}+\frac{\varepsilon_d h}{s}]}} \sim \omega \tag{2.36}$$

Neglecting radiation, the total loss can be estimated by Eq. (2.34), as the sum of conductor and dielectric losses. The loss vs. waveguide lengths of 100-600 μm and a loss tangent of 0.008, are plotted in Figure 2-8. Conductor loss clearly dominates since dielectric loss only represents ~5% of the total loss even at the highest frequency.

Eq. (2.34) also gives the dependency of the total loss as a function of the aspect ratio of the trench, as shown in Figure 2-9. As expected, higher aspect ratio reduces the impedance, therefore results in higher loss.

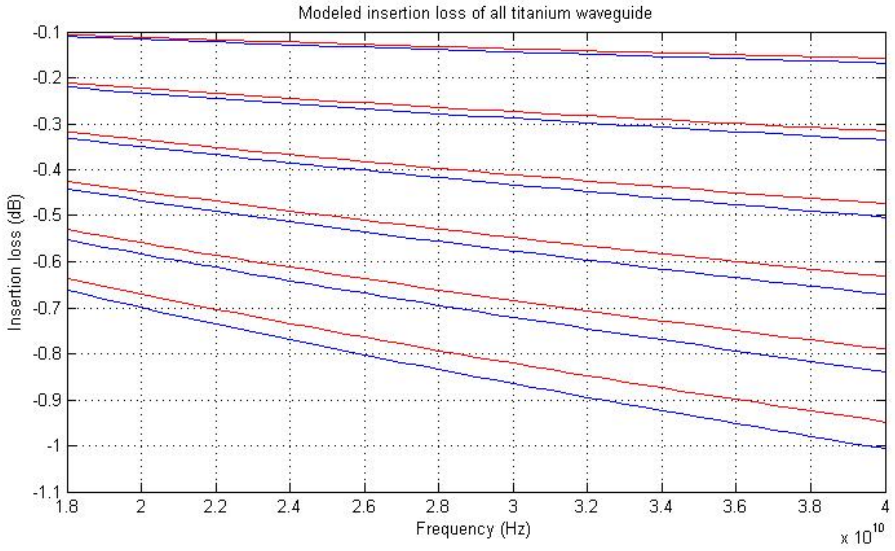


**Figure 2-8 Modeled insertion loss of titanium waveguides of different lengths. Note: all waveguides are of the following common parameters: h=50μm, S=15μm, W=30μm. Red curves: conductor loss; blue curves: conductor and dielectric losses. From top to bottom: 100 μm to 600 μm with 100μm increments**

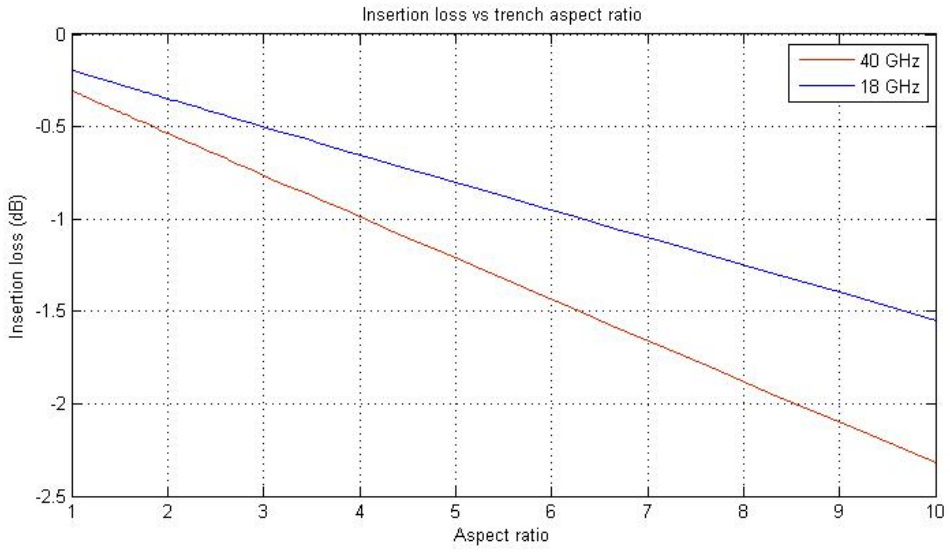


**Figure 2-9 Insertion loss vs. trench aspect ratio**

### 2.2.4 Effect of packaging

The above model can be extended to include the impact of a conductive package, which induces parasitic coupling to the waveguide, hence influencing the overall RF characteristics of the waveguide. The schematic of the analytical model is illustrated in Figure 2-10.

With the assumption of a magnetic wall at the dielectric-air interface, the effect of a conductor package can also be modeled by conformal mapping.

To simplify the model, we assume infinite lateral dimensions and focus on the parasitic effect of a conducting object in the vicinity of the waveguide.

Here we introduce another mapping function:

$$t' = \cosh^2\left(\pi t/2h_p\right), \tag{2.37}$$

where $h_p$ is the gap between the bottom of the conductive package and the top surface of the waveguide.

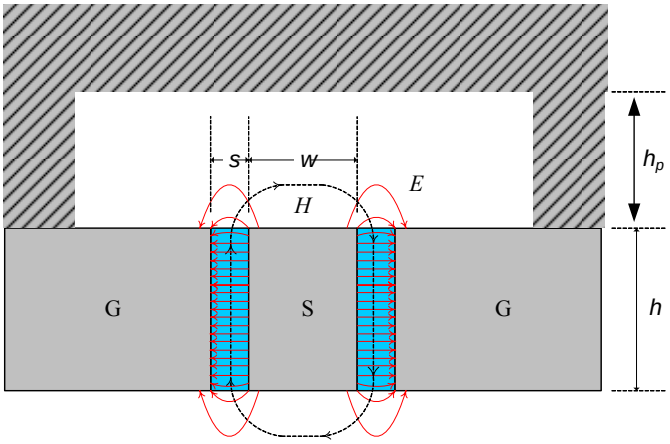


**Figure 2-10 Schematic of bulk titanium waveguide packaged with a conductive cap**

This function maps the package onto the real axis and prepares the region for the following Schwarz-Christophel mapping that converts the configuration into the interior of the rectangle:

$$\frac{dt''}{dt'} = \frac{1}{t'(t'-1)(t'-t_2')(t'-t_3')} \tag{2.38}$$

where $t'_2$ and $t'_3$ are the locations of the edge of the center conductor and the inner edge of the ground, respectively, mapped onto the t' plane, as shown in Figure 2-11. The solution to this equation follows the complete elliptical integral of the first kind:

$$\frac{a}{b} = \varepsilon_0 \frac{K(k)}{K'(k)} + \varepsilon_0 \frac{K(k_1)}{K'(k_1)} \tag{2.39}$$

where

$$k_1 = \tanh(\pi w / 2h_p) / \tanh[\pi(w+2s)/2h_p] \tag{2.40}$$

By taking into account the reverse side of the waveguide, where no package is present, the total capacitance is therefore:

$$C = 4\varepsilon_0 \frac{K(k)}{K'(k)} + 2\varepsilon_0 \frac{K(k_1)}{K'(k_1)} + \frac{2\varepsilon_0 \varepsilon_d h}{s} \tag{2.41}$$

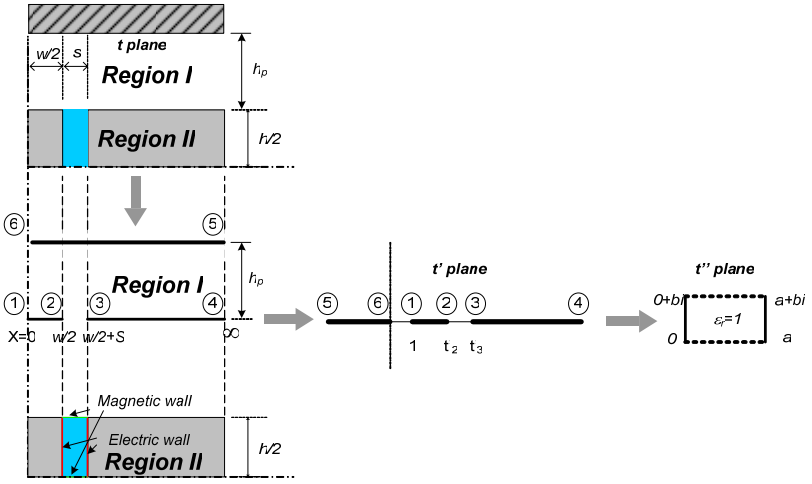


**Figure 2-11 Conformal map for packaged bulk titanium waveguide**

By following the same analysis shown in section 2.2.3, the impedance is obtained:

$$Z_0 = \sqrt{\frac{\frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}} + j\omega\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})}{\frac{\tan\delta_d\omega\varepsilon_d\varepsilon_0 h}{s} + j\omega\varepsilon_0[\frac{4K(k)}{K'(k)} + \frac{2K(k_1)}{K'(k_1)} + \frac{2\varepsilon_d h}{s}]}} \tag{2.42}$$

The loss, similarly:

$$\alpha \approx \frac{LG+RC}{2\sqrt{LC}} = \frac{\frac{\mu_d \tan\delta_d\omega\varepsilon_d\varepsilon_0}{s}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}}) + \frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{K(k_1)}{K'(k_1)} + \frac{\varepsilon_d h}{s}]}{2\sqrt{\frac{\mu_d}{h}(\mu_0 s + \sqrt{\frac{2\mu_c\mu_0}{\omega\sigma_c}})\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{K(k_1)}{K'(k_1)} + \frac{\varepsilon_d h}{s}]}} \tag{2.43}$$

For high frequencies:

$$\alpha \approx \frac{\mu_0\mu_d \tan\delta_d \omega\varepsilon_d\varepsilon_0 + \frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{K(k_1)}{K'(k_1)} + \frac{\varepsilon_d h}{s}]}{2\sqrt{\frac{\mu_0\mu_d\varepsilon_0 s}{h}[\frac{2K(k)}{K'(k)} + \frac{K(k_1)}{K'(k_1)} + \frac{\varepsilon_d h}{s}]}} \tag{2.44}$$

Evidentially, the loss follows the same frequency dependency for conductor loss, and dielectric loss dominant regimes as when without the package.

Note that, due to the assumption and corresponding model used, the performance impact from the presence of a conductive package shows up as a parasitic capacitance.

The net impact on loss from the package is therefore obtained from Eq.s (2.44) and (2.34):

$$\begin{aligned}\Delta\alpha_{pac} \approx & \frac{\mu_0\mu_d \tan\delta_d \omega\varepsilon_d\varepsilon_0 + \frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{K(k_1)}{K'(k_1)} + \frac{\varepsilon_d h}{s}]}{2\sqrt{\frac{\mu_0\mu_d\varepsilon_0 s}{h}[\frac{2K(k)}{K'(k)} + \frac{K(k_1)}{K'(k_1)} + \frac{\varepsilon_d h}{s}]}} \\ & - \frac{\mu_0\mu_d \tan\delta_d \omega\varepsilon_d\varepsilon_0 + \frac{2}{h}\sqrt{\frac{\omega\mu_c\mu_0}{2\sigma_c}}\varepsilon_0[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}{2\sqrt{\frac{\mu_0\mu_d\varepsilon_0 s}{h}[\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}]}}\end{aligned} \tag{2.45}$$

When conductor loss overrides other sources of loss:

$$\Delta\alpha_{pac} \approx \sqrt{\frac{\omega\mu_c\varepsilon_0}{2\mu_d\sigma_c hs}}(\sqrt{\frac{2K(k)}{K'(k)} + \frac{K(k_1)}{K'(k_1)} + \frac{\varepsilon_d h}{s}} - \sqrt{\frac{2K(k)}{K'(k)} + \frac{\varepsilon_d h}{s}}) > 0 \tag{2.46}$$

which indicates an increase in loss, due to the larger contribution from the fringing fields.

For cases where dielectric loss becomes dominant:

$$\Delta\alpha_{pac} \approx \mu_0\mu_d \tan\delta_d \omega\varepsilon_d\varepsilon_0\left(\frac{1}{2\sqrt{\frac{\mu_0\mu_d\varepsilon_0 s}{h}\left[\frac{2K(k)}{K'(k)}+\frac{K(k_1)}{K'(k_1)}+\frac{\varepsilon_d h}{s}\right]}}-\frac{1}{2\sqrt{\frac{\mu_0\mu_d\varepsilon_0 s}{h}\left[\frac{2K(k)}{K'(k)}+\frac{\varepsilon_d h}{s}\right]}}\right)<0 \quad (2.47)$$

The reduction in loss in caused, again, by the increase in fringing fields, which occurs in spaces where the lossy dielectric is absent.

### 2.2.5 Other modes of propagation

As with conventional CPW, the three-conductor construction of the bulk titanium waveguide supports two primary modes of RF wave propagation: odd mode, also called the "CPW mode", in which the field directions in reference to the center conductor are opposite to one another; and the even mode, also referred to as the "coupled stripline mode", or CSL mode, in which the fields from the center conductor to ground on each side of are aligned. The CPW mode is usually the targeted mode responsible for the propagation of signals. The TEM-like field distribution means no cut-off frequency. CSL mode, which occurs especially at locations of asymmetries and discontinuities, results in a potential difference between the grounds on each side and consequently may lead to excessive radiation at discontinuities such as bends and tapers. To suppress the coupled stripline mode, techniques such as air bridges are often used to help equalize the potentials of the grounds on each side.

As demonstrated in Figure 2-12, the much greater depth and therefore larger cross section of the grounds in the bulk titanium waveguides helps reduce the potential difference by significantly reducing the series resistance, therefore reducing the potential imbalance between grounds and suppressing the creation of the CSL mode. Also, the large current-carrying surface area helps eliminate current crowding and improves the ability to accommodate high powers.

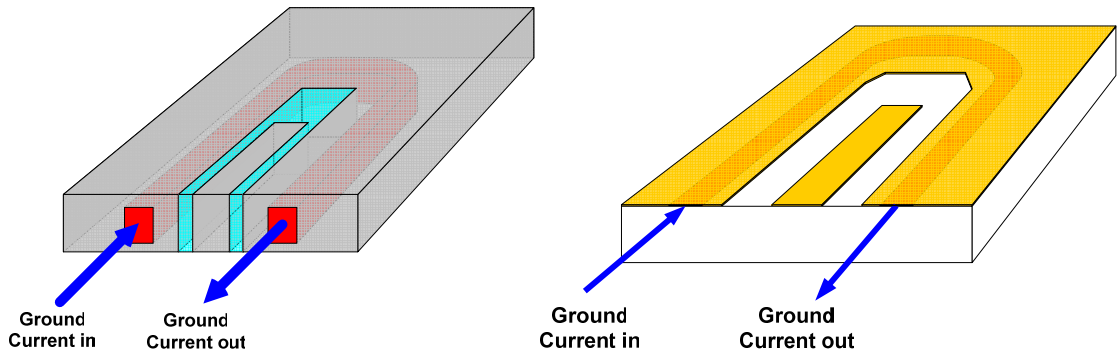


**Figure 2-12 Comparison of current distributions in bulk titanium waveguide (top) and conventional CPW (bottom)**

For applications involving coupling between signals, such as couplers and coupled-line filters, however, the CSL mode can prove useful. The much greater depth of the conductors gives rise to another dimension, as opposed to conventional CPW based configuration, and helps with controlling the performance of the device.

Another possible mode is the TM mode propagating in the dielectric slabs sandwiched between the conductors. Due to the small dimensions of the dielectric material in the gaps, the first allowable mode far exceeds the operating range in frequency – $K_a$ band - of the system.

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# CHAPTER 3

# TITANIUM PLANARIZATION PROCESS DEVELOPMENT

## 3.1 Background

Despite the promises and advantages of titanium versus traditional, single crystal substrates, the metallic nature of bulk titanium substrate also creates obstacles for many semiconductor processes requiring uniformity and planarity. For example, cleaving a single crystal substrate can be easily performed by using a diamond scribe to break the edge, thus creating dislocations which can propagate along preferred directions in the crystal, resulting sharp, clean cleaved edges along the crystalline planes; whereas cutting a titanium substrate typically involves tools such as water-jet cutters, dicing saw and hydraulic presses.

These cuts result in various types of burrs, or severe edge deformations (see Figure 3), which can pose challenges in subsequent processes requiring sample planarity, such as lithography and bonding. The characteristics of the burr vary for different cutting methods. Shearing tools are the most convenient and cost-effective and typically generate a burr in the direction of the outer blade in the shearing tool. The amount of edge burr also depends on the thickness of the sample. For samples thinner than 200 μm, the issue associated with the metallic nature of titanium substrates becomes more severe: semiconductor/MEMS processes, such as thin film deposition, can introduce stresses [1, 2] large enough to plastically deform the substrate; simple procedures such as handling or drying with a nitrogen jet can also result in plastic deformations.

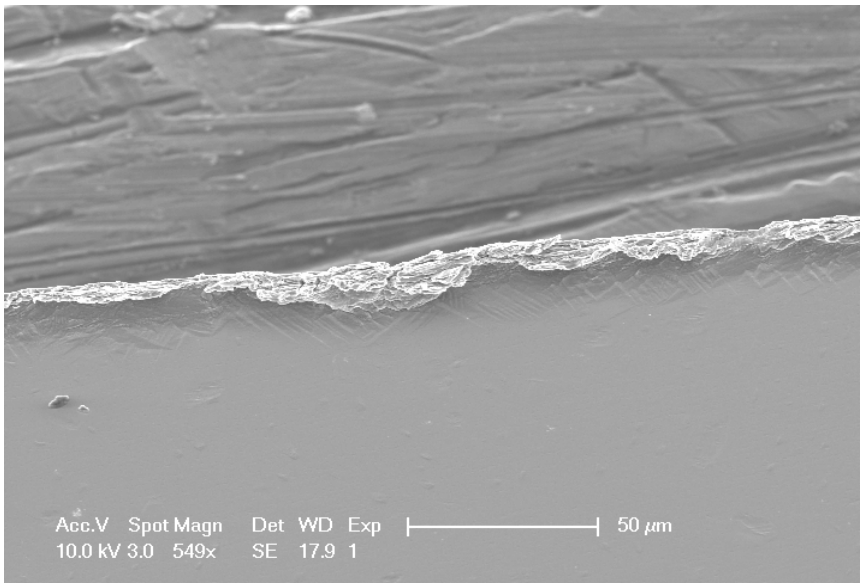


**Figure 3-1 Diced CP titanium sample edge burr**

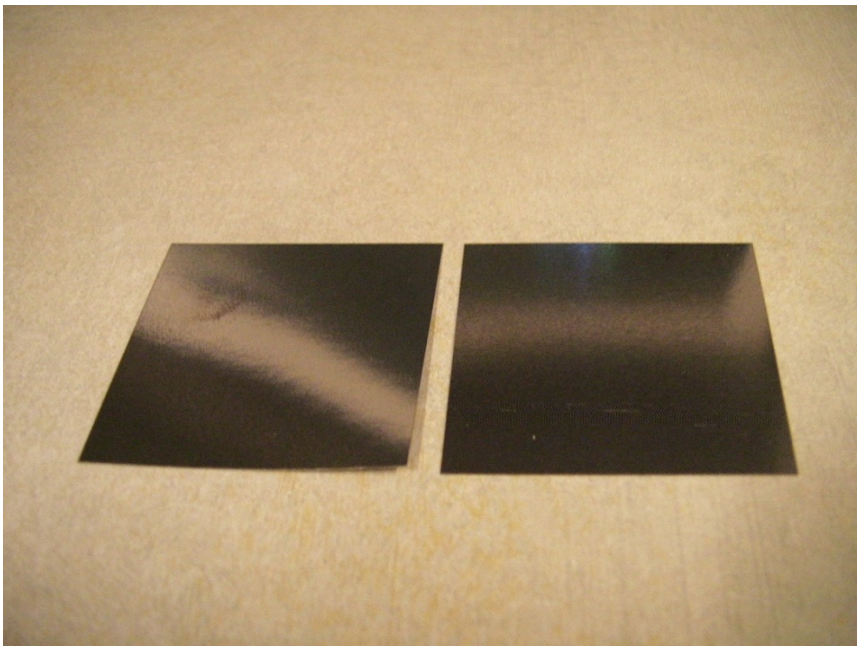

**Figure 3-2a Edge burr created by hydraulic press. Left: 1”x1”x50 µm CP titanium sample as cut from a flattened sheet. Right: 1”x1” sample after flattening anneal**

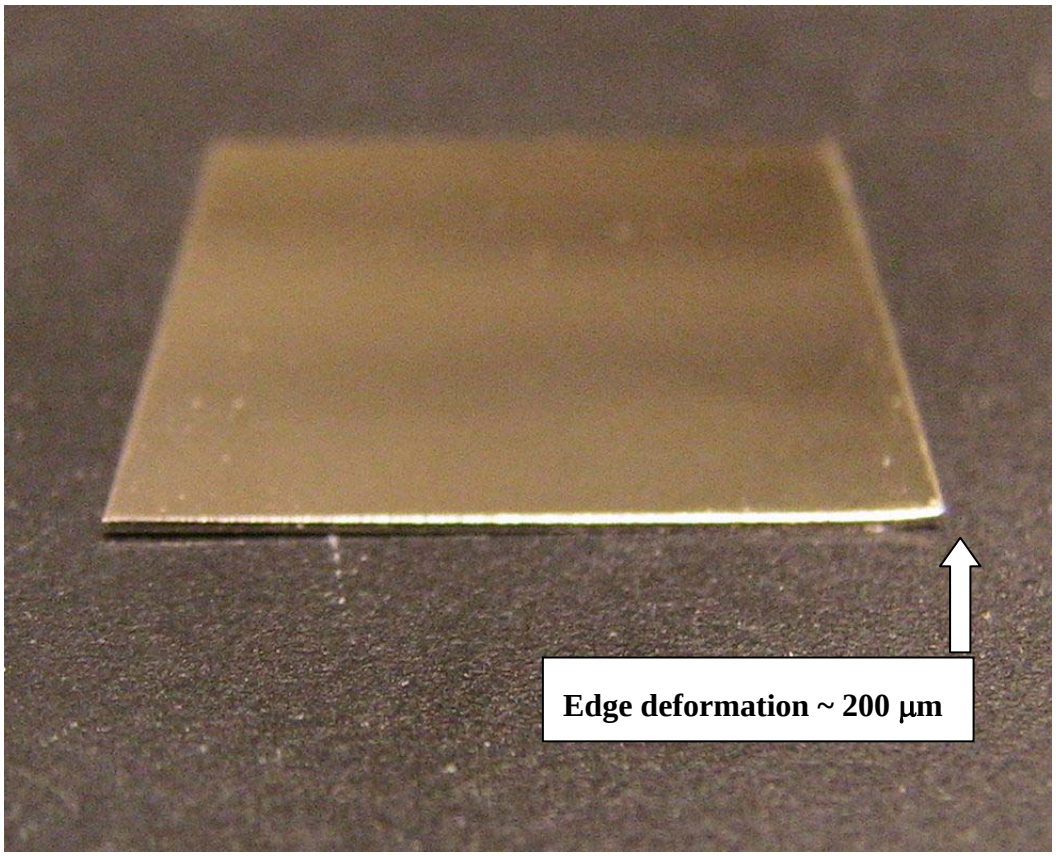


**Figure 3-2b Edge burr on 1"x1"x200 μm CP titanium sample as cut by hydraulic press**

In addition, the manufacturing process of titanium sheets often results in defects such as “rolling hills” and surface flaws [3]. Figure 3-3 shows the 5-point thickness measurement of 10 1”x1” bulk titanium samples cut from the same batch of titanium sheets with the specified thickness of 200 μm. An average thickness of 175.62 μm and standard deviation of 9.51 μm are measured, representing a 5.41% thickness variation within a 1”x1” area. As shown in Chapter 2, small thickness variations are essential to the performance of trench-filled bulk RF waveguide.

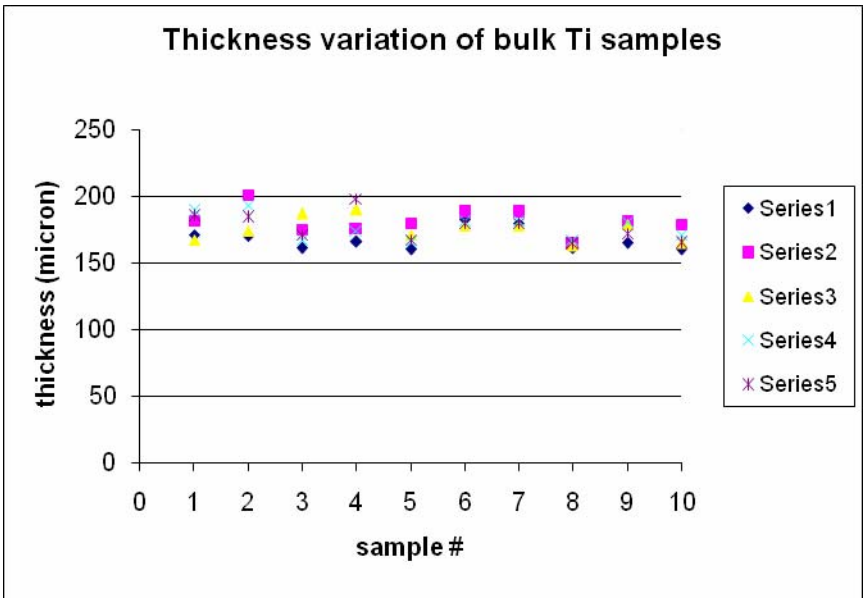


**Figure 3-3 Thickness variation of 10 bulk titanium samples. Different series numbers represent measurements taken at 5 locations on each sample: center and 4 corners**

Moreover, a typical surface of a titanium substrate obtained from suppliers, has a roughness, $R_a$, ~ 100 nm. Surface defects manifest themselves in pits, which are often grain boundary associated, scratches (see Figure 3-4) and invisible flaws such as embedded impurities, which can cause significant defects such as grassing (see Figure 3-5) during subsequent etches. Non-planarity alone can be intolerable for fabrication processes such as lithography and bonding [1, 2]. Traditional techniques, such as silicon carbide abrasive polishing and electropolishing, exist for planarizing and polishing titanium sheet macroscopically [3]. However, the thickness uniformity required for RF performances and the surface quality necessary for dry etching demand the development of processing techniques that are beyond the current state of the art.

In this paper, we present a suite of processes developed to address these issues. The result: flat from edge-to-edge, stress-relieved bulk titanium substrates with roughness as low as 2.8 nm. Our approach is composed of three steps: stress-anneal straightening, for removing gross deformations while releasing the remaining stress; lapping, for evening out the thickness variation across a sample and for removing defects embedded below the substrate surfaces during the manufacturing process, and chemical and mechanical polishing (CMP), for removing the damages caused by the lapping process and minimizing the surface roughness.

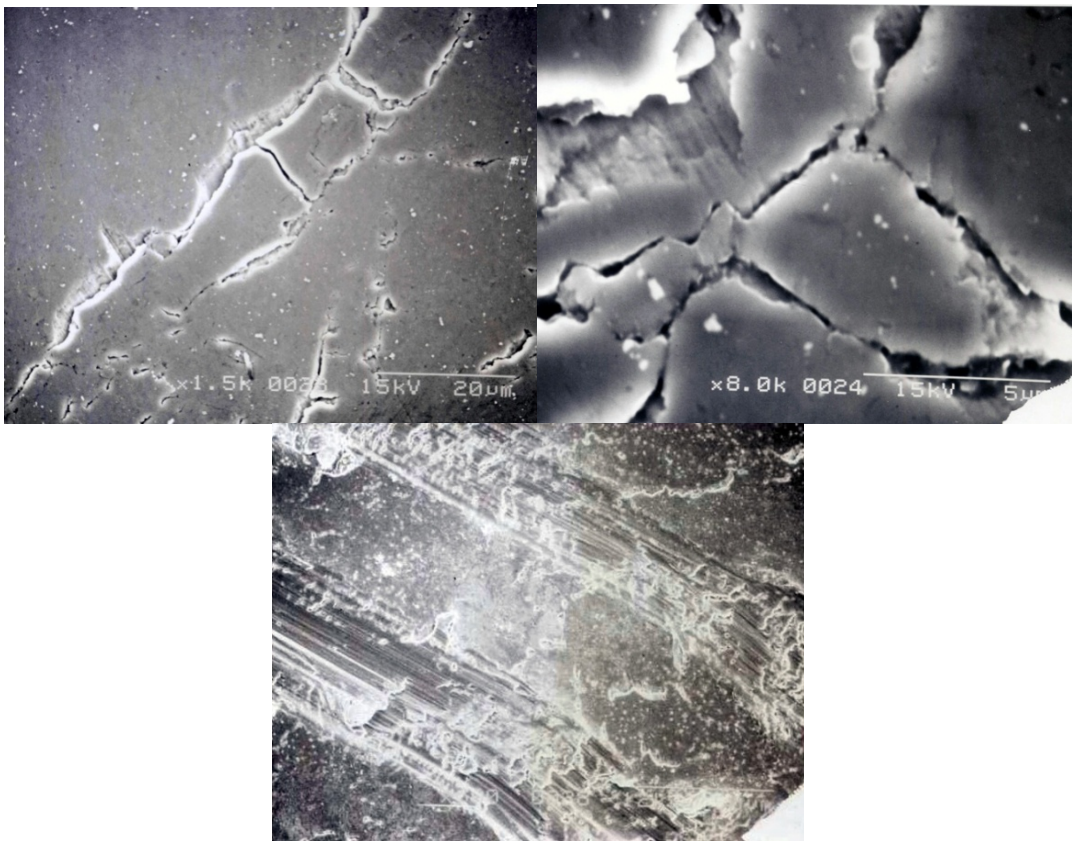


**Figure 3-4 Surface defects of bulk titanium substrates**

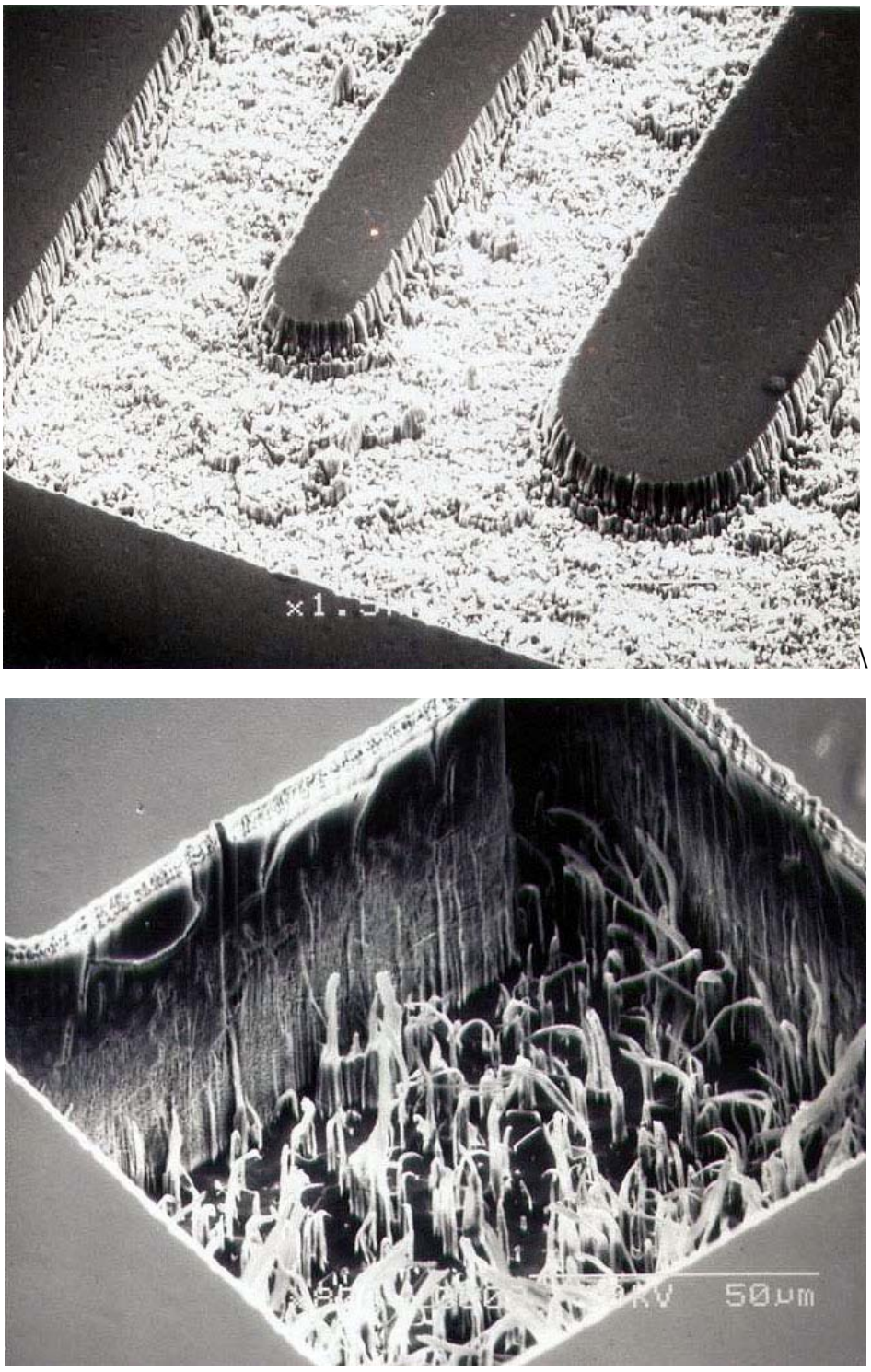


**Figure 3-5 Micromasking (grassing) from dry etch of bulk titanium**

### 3.2 Titanium stress-anneal flattening process

Unlike single crystal substrates, titanium sheets, as obtained from manufacturers, often contain macroscopic deformations (a 6”x6” sheet is shown in Figure 3-6), that increases with handling and subsequent wafer/chip singulation (see Figure 3-2). These deformations often occurs on a scale of hundreds of microns to millimeters and create considerable challenges to most semiconductor/MEMS processes. For the 1”x1” samples used for all our experiments, substrates 25 μm and thinner present a lesser problem since the substrates can easily deform to align with another, flat substrate. For the 100 μm to 200 μm thick substrates used for waveguide fabrication, however, such deformations can be prohibitively large.

**Figure 3-6 Gross deformation of as-obtained bulk titanium substrate**

**Table 3-1 Process sequence for stress-anneal straightening of bulk titanium**

| Process steps | Notes |
|---|---|
| Sample preparation | Clean sample and sandwich wafers with acetone, IPA and DI, 1 minute soak + 1 minute with ultrasound. Dry in 110$^{o}$C convention oven for 5 minutes. |
| Initial pumpdown | 3 pump-vent-pump cycles between 1E-4 torr and 1000 torr at 50$^{o}$C. (helps subsequent pumping to higher vacuum) 1 pump-vent-pump cycles between 1E-5 torr and 1000 torr at 50$^{o}$C. |
| Pumpdown at intermediate temperature | Raise temperature to 200$^{o}$C at 5$^{o}$C/second. Stay for 10 minutes. (elevated temperature expedites outgassing); Tool down |
| Ramp to annealing temperature | Ramp to anneal temperature of 600$^{o}$C (550$^{o}$C minimum) at $^{o}$1C/minute. |
| Pressured anneal | 50 – 200 KPa (sample dependent) for 60 minutes |
| Cool to intermediate temperatures | Cool to 400$^{o}$C at 1$^{o}$C/minute; Cool to 150$^{o}$C at 2$^{o}$C/minute |
| Final cool | Vent chamber to 1000 torr; Cool to50$^{o}$C |

While the non-single-crystalline nature of bulk titanium poses challenges, the metallic properties of titanium can be utilized for removing these deformations while reducing the intrinsic stress embedded in the substrate from its manufacturing and previous handling: titanium and titanium alloys can be stress relieved without adversely affecting strength or ductility.

Stress-relieving treatment decreases the undesirable residual stresses that result from previous manufacturing processes such as forging, forming, straightening, rolling and machining. By applying an external force to deform the substrate into a desired shape while performing the stress-relieving process we can re-shape the sample, which is not provided for single crystal substrates. Specifically, the sample can be sandwiched between flat, sturdy, and stable surfaces. Upon reaching the desired temperature, an external pressure will straighten the sample while the annealing procedure removes the stress buildup prior to this step as well as from the straightening process. The $N_2$ purging and vacuum environment helps minimize the amount of oxidation on the titanium surface. Stress-relieving also helps maintain shape stability and eliminates unfavorable conditions, such as the loss of compressive yield strength commonly known as the Bauschinger effect.

The initial planarization process eliminates many deformations caused by manufacturing and handling. The basic concept is to utilize the high flatness, modulus and chemical stability of sapphire wafers and the enhanced ductility of bulk titanium at elevated temperatures. Stresses, both intrinsic and those caused by the process of planarization, are relieved by a high temperature anneal followed by a controlled slow cooling step, which prevents new stresses from building up.

At lower temperatures, under a large bending moment, CP titanium undergoes partially plastic deformation, and “springs back” once the external moment is released. The resulting residual stresses in a substrate cause damages that can affect subsequent

processes. Stress relief anneal of CP titanium takes place between 485°C and 595°C for 15 minutes to 4 hours, depending on specific material. To maintain the chemical composition of the substrate, it is critical that the ambient is free of reactive gases such as hydrogen, oxygen and nitrogen. At this temperature, no significant grain size growth occurs (Figure 3-7 from [1]), thus maintaining substrate's mechanical properties such as modulus and yield strength. However, the grain boundaries are able to move therefore enhancing material ductility, which reduces the stress. This treatment eliminates burring, as well as reduces curvature in the samples.

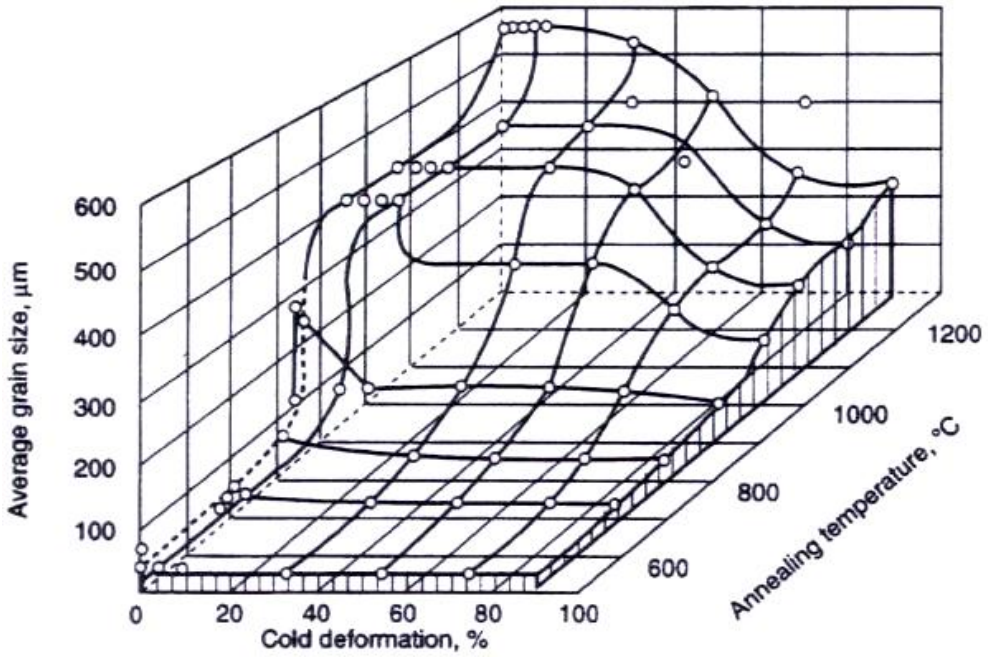


**Figure 3-7 CP titanium grain size vs. annealing temperature [1]**

The procedure of our stress-relief straightening process is listed in Table 3-1. Our experimental setup consists of heating titanium samples between two clean, 500 µm thick silicon wafers 4" in diameter in a Karl Suss SB6 wafer bonder capable of

reaching 600°C while maintaining vacuum. The plate is placed on a large, flat ceramic bed that has integrated electric heating elements. Insulation is placed on top of the plate, and a plastic sheet is sealed to the frame.

Bulk titanium substrates as rolled typically go through a rough grinding process before final delivery. Roughness ranges from 50 nm to several hundred nm, depending on the supplier. Curvatures < 1m and thickness variation > 20 μm in a 1"x1", 200 μm thick sample are common, due to residual stresses and limitations of the manufacturing processes. Using one such sample with ~42 μm maximum bend measured from a 10 mm span with a Wyko NT1110 profilometer, the stress-relief straightening process reduced the maximum deformation to ~6 μm (Figure 3-8)

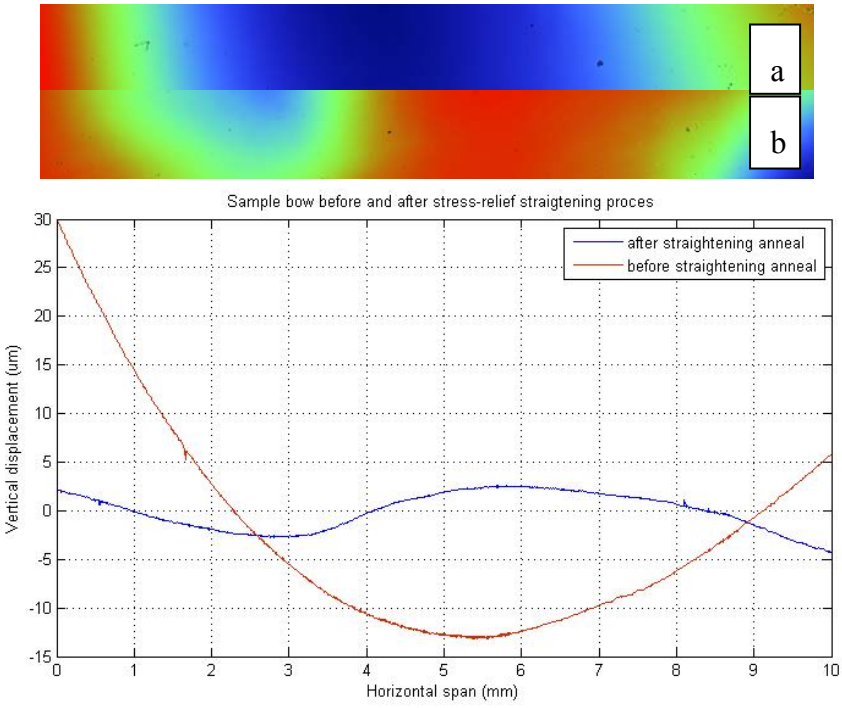


**Figure 3-8 Bulk titanium sample profile measurement in a 10 mm x 1 mm area: a) before stress-relief anneal: maximum bow ~42 μm; b) after stress-relief anneal: maximum bow~6μm**

The temperature dependence of the straightening is illustrated in Figure 3-8 and Figure 3-9. Five samples, all with 200 μm nominal thickness, are monitored through annealing processes at 4 different temperatures: 450°C, 500°C, 550°C and 600°C. The statistical distribution of the deformation measurements come from measurements, each with a 10mm span, taken at different locations of the samples. A temperature of 450°C was insufficient to prevent spring back once the samples were cooled and pressure released. At 500°C, the samples start to show signs of straightening. At 550°C and above, the samples exhibit significant straightening and the standard deviation of the deformation is also drastically reduced, indicating a global flattening effect.

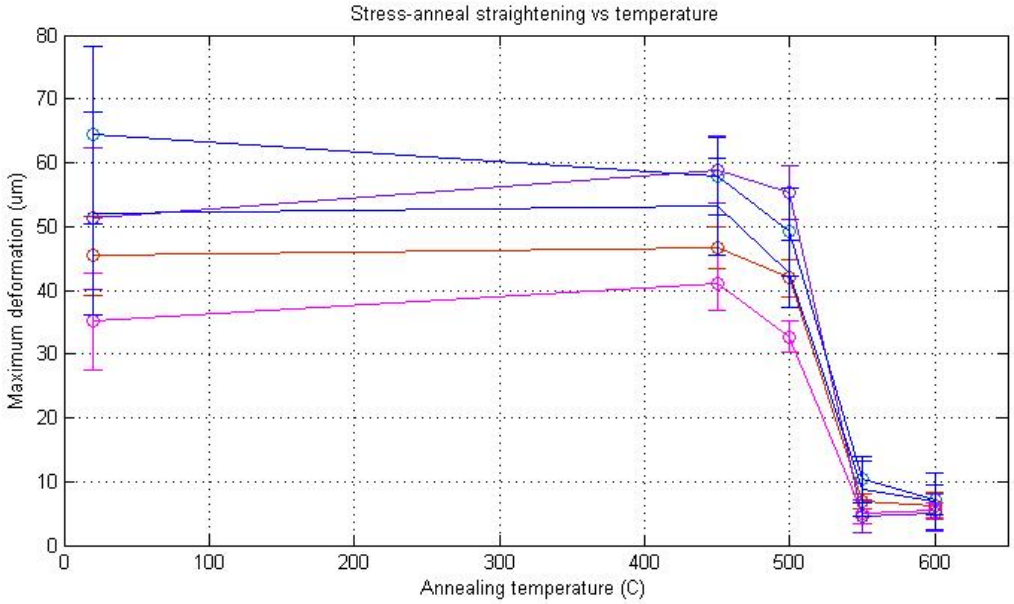


**Figure 3-9 Stress-anneal straightening of 5 1"x1", 200 μm Ti samples**

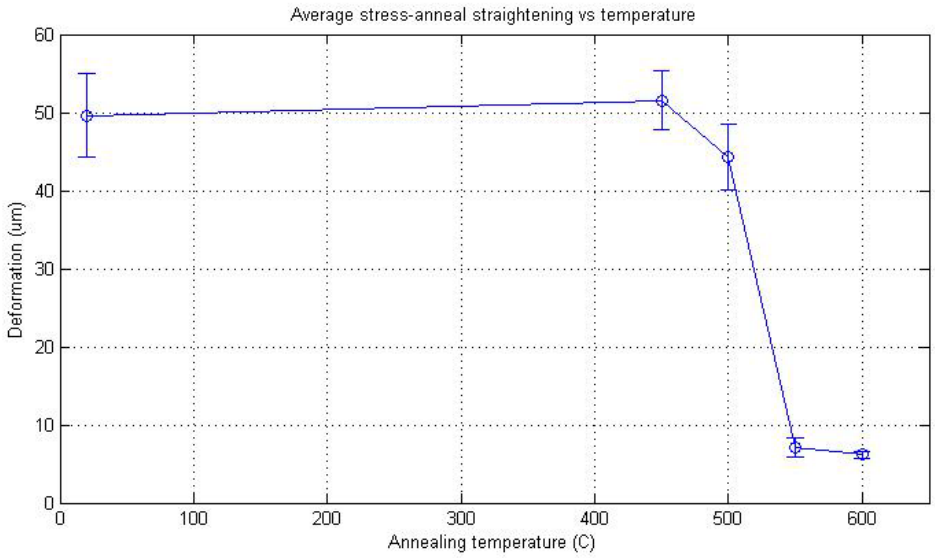


**Figure 3-10 Average deformation after stress-anneal straightening**

While the improvement in planarity of the sample is pronounced, no significant change in roughness was measured (after curvature correction) after the stress-relief anneal (Figure 3-11).

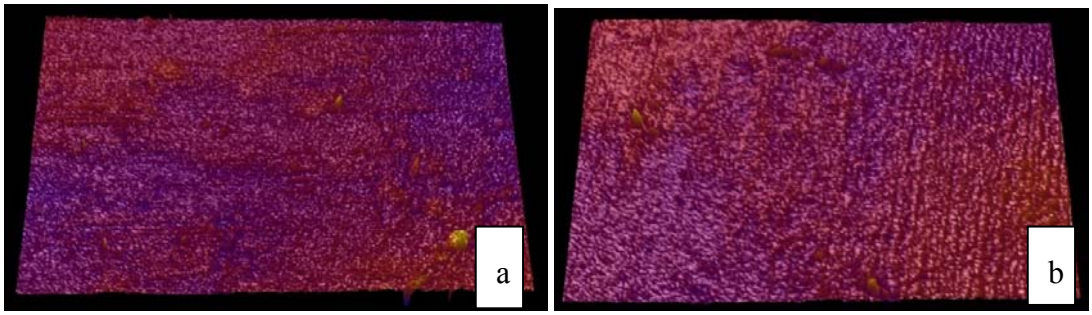


**Figure 3-11 Roughness measurement of bulk titanium samples before lapping/polishing: a) before anneal: $R_a$ =52.82 nm; $R_t$=1.39 μm; b) after anneal: $R_a$ =55.96 nm; $R_t$=1.31 μm**

## 3.3 Titanium lapping and polishing process

### 3.3.1 Lapping and polishing mechanism

Titanium polishing is done traditionally with SiC and of grit sizes ~60-140, which results in a roughness of > 100 nm. Finer polish of <10 nm needed by many semiconductor processes is a challenge compared to SCS. Titanium is ductile, therefore is much more prone to polishing defects such as scratches, embedded particles and high residual stresses. Lapping and polishing are among the oldest manufacturing processes, but they are also among the ones least well supplied with predictive process models. Lapping/polishing plate, slurry use, tool pressure, as well as polishing direction are all important parameters affecting the result. Particle-scale models that calculate the mechanical removal by abrasive particles or mechanical erosion due to shearing stress buildup, provide an overall guideline in varying process parameters for target (MRR) material removal rate and roughness. Preston's empirical equation[4], shows a linear relation between MRR and the product of tool pressure, P, and relative velocity, V, between sample and polishing/lapping pad:

$$MRR = K_e PV \tag{3.1}$$

where $K_e$ is the material dependent Preston coefficient. To address the absence of consumables and sample parameters, Cook et al. [5] developed a model which proposes a Hertzian elastic penetration of a spherical particle under uniform pressure P into the sample surface, sliding along the surface with relative velocity V and removing material volume proportional to the penetration:

$$MRR = \frac{PV}{2E} \tag{3.2}$$

where E is the sample's young's modulus. The resulting sample surface roughness Rs, with a pad charged with such slurry particles is also related to the tool pressure P:

$$R_s = \frac{3}{4} x (\frac{P}{2kE})^{\frac{2}{3}} \tag{3.3}$$

where k is the particle concentration and unity for a fully charged hexagonal packing and x the diameter of the slurry particles.

The effect of the pad, as well as the finite modulus of the slurry particles are addressed in a similar model proposed by Liu et al.:

$$MRR = C(\frac{H_W}{H_W + H_P})(\frac{E_S + E_W}{E_S E_W})PV \tag{3.4}$$

where $H_w$ and $E_w$ are the hardness and modulus of the sample, Hp the hardness of the pad, Es the modulus of the slurry particle, C a coefficient that accounts for the effects of other consumable parameters such as slurry chemicals.

The diamond lapping process is especially suited for metal due to its exceptional cutting ability on different materials, and superior surface finish compared to alumina and SiC (**Error! Reference source not found.**-12 from [6]). Opposite to boron carbide, aluminum oxide, silicon carbide and other abrasives, diamonds do not fracture or become smaller during the process of lapping, thus providing better process repeatability. For softer materials such as metals, a non-rigid pad is used to help reduce the damage. Slurry spray interval is usually less difficult to control. However, too little slurry reduces the lapping rate and increase roughness; too much slurry causes "hydroplaning", i.e., the work piece becomes suspended by the liquid in the slurry, resulting in rapid reduction in the lapping speed. Abrasive particle size is also directly related to the removal rate. There is typically a tradeoff between lapping speed and resulting surface damage, which can be indirectly evaluated by roughness

measurement. Finally, pressure is also important in the determination of throughput and final roughness. Excessive pressure increases roughness significantly while gaining little in speed.

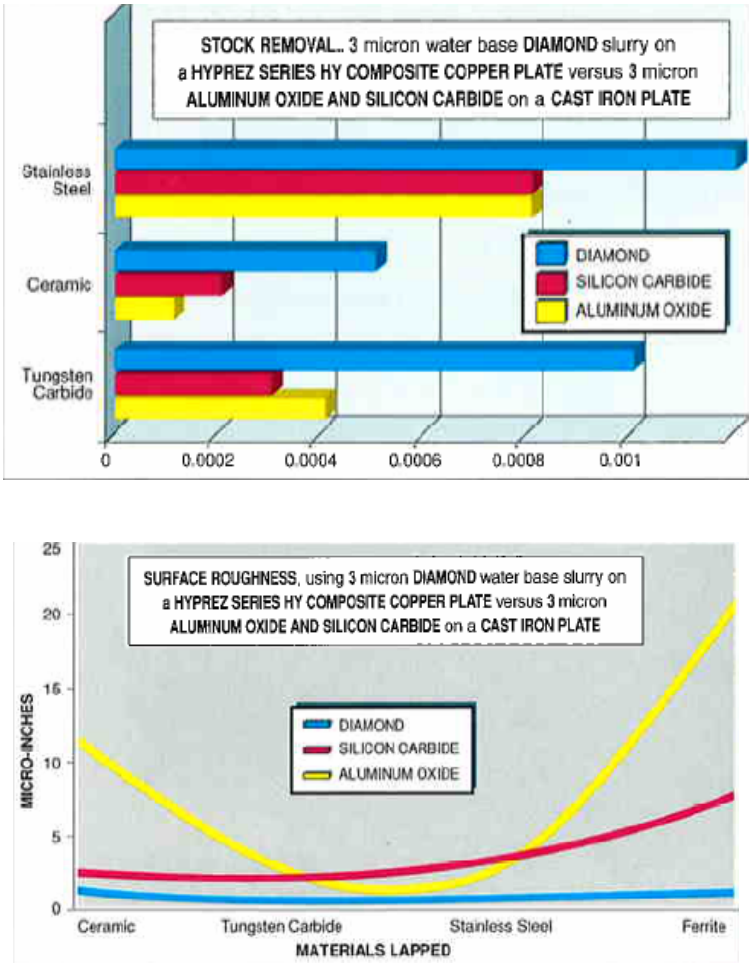


**Figure 3-12 Comparison of commonly used lapping slurries [6]**

The polishing step not only achieves the smooth finish, but is essential in reducing the surface damage caused by the lapping process. The harsh interruption of the surface by the diamond abrasive particles leads to significant amount of compressive stress in the substrate.

### 3.3.2 Experimental procedure

In our experiment, 4 25 μmx25 μm, 200 μm thick titanium samples are sandwiched between 2 single-side polished 4" silicon wafers before pressure is exerted by a SUSS SB6 wafer bonder with UHP helium purging gas. Multiple purging and pumping steps help remove trapped gases and particles, and expedite subsequent pumping. At the bonding temperature, a vacuum of 5e-6 mbar or higher is used to maintain chemical composition of the titanium surface. The maximum tool pressure is determined by the stress level at edges and corners of the samples where they make contact with the sandwich wafers. Over pressure is unnecessary for straightening and can cause stresses exceeding the fracture threshold, which induces fracture in the silicon wafers (Figure 3-13). The resulting change in surface profile is evaluated using a Wyko surface profilometer (Figure 3-14). A field size of ~ 500 μm x 500 μm is used for measuring roughness. Long range deformation is measured with a stitched field of 12 mm x 1 mm.

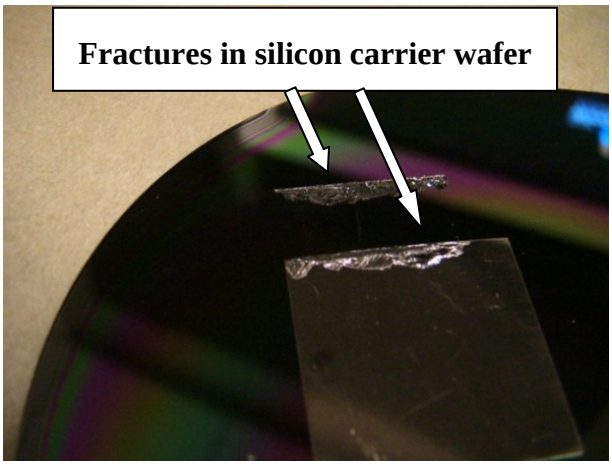


**Figure 3-13 Fractures in carrier SCS wafer due to excessive stresses in stress-anneal straightening process**


**Figure 3-14 Wyko NT1100 interferometer for roughness and deformation measurement**

Lapping and polishing were performed on an Engis Hyprez computer-controlled system (Figure 3-15a). The plates are 15" cast iron/ceramic composite which are compatible with both lapping and polishing processes. Mounting procedure for thinner samples is essential to ensure a thin, uniform adhesive prior to lapping and polishing. A combination of vacuum oven and water-cooled hydraulic press (Figure 3-15b) was used to ensure a thin, uniform, bubble-free bonding adhesive between the samples and the ceramic sample holder (Figure 3-15c). Adhesive depth is evaluated by a dial indicator with resolution down to 1 μm. Diamond slurries were used for lapping and colloidal silica slurry for polishing. Again, the Wyko profilometer was used to evaluate the results with a resolution ~1 nm. A fixed rotation speed of 60 rpm was used for both the plate and the pressure tool.

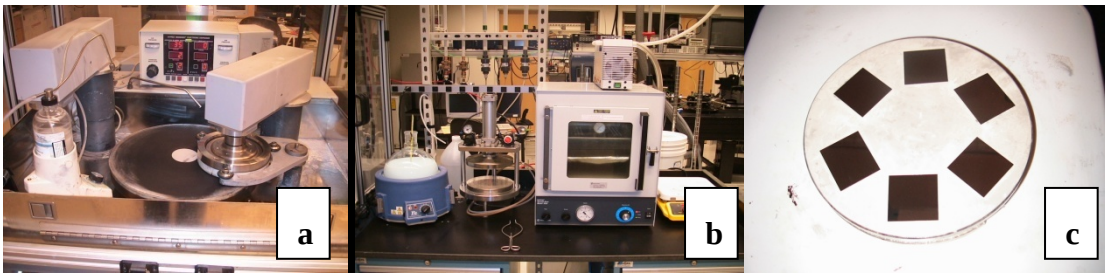


**Figure 3-15 a) Engis Hyprez computer controlled lapping/polishing machine; b) hydraulic press and vacuum oven for bubble-free sample mounting; c) polished bulk titanium samples before dismount**

To evaluate the lapping and polishing results, two key metrics are examined: Ra, the average roughness; $R_t$, the peak-to-valley roughness. $R_a$ gives the short-range roughness, or smoothness, of the surface. $R_t$ shows the maximum height variation, which, when combined with $R_a$, reveals the amount of long-range height variation. $R_t$ is also an indicator of the depth of the deepest scratches created by lapping/polishing process. $R_t$ is customarily used to gauge the amount of damage to the underlying substrate.

The lapping process removes the embedded manufacturing defect, provides global planarization and removes a large amount of material to reach the desired thickness. For the lapping process, the most important results are therefore the material removal rate (MRR) and the $R_t$, since that determines how much additional material needs to be removed by the subsequent damage-removal polishing process. Of course, the sample needs to be lapped sufficiently to ensure long-range planarization.

The polishing process serves two purposes: removing the damage left behind by the lapping process, and obtaining a final target surface finish. Removing the lapping damage includes polishing away the surface layer containing the scratches, as well as a layer beneath which contains defects/dislocations that lead to residual stresses. All

three parameters, i.e., MRR, $R_t$, and $R_a$, are therefore important in determining the performance of the process.

The experimental procedure for the lapping and polishing process is listed in Table 3-2.

**Table 3-2 Process sequence of bulk titanium lapping and polishing**

| Processing steps | Notes |
|---|---|
| Sample measurement | 5 point measurement |
| Sample mounting | 30 minutes @ 175°C on hotplate; Vacuum oven ~100 torr @ 190 °C for 60 minutes |
| Sample measurement | 5 point measurement; <~10 μm variation required |
| Slurry preparation | 3μm oil-based slurry; 15 minute stir |
| Plate charging | 5 minutes |
| Lapping process | 25-30 lb/37.5cm$^2$ |
| Sample cleaning | Ultrasound in DI, 1 minute |
| Sample measurement | 5 point measurement |
| Slurry preparation | 55 °C; 375ml slurry/625ml DI mix |
| Plate conditioning | 120 grit conditioning ring, 2 minutes |
| Plate charging | 5 minutes |
| Polishing process | 10-15 lb/37.5 cm$^2$ |
| Sample cleaning | Ultrasound in DI, 1 minute |
| Sample measurement | 5 point measurement |
| Sample dismount | 200°C, 30 minutes |

### 3.3.3 Results and discussion

**1) Lapping**

The mounting of samples was done with Crystalbond#509 as the adhesive; < 10 μm adhesive thickness variation based on a 5-point measurement on a 1"x1" sample was obtained prior to lapping and polishing processes. At the beginning of each lapping process, 5 μm-25 μm thick, depending on the sample planarity and mounting uniformity, of material needs to be removed before reaching a state long-range planarity, i.e., where the entire sample surface has been lapped. Samples during this intermediate step show patches of non-uniform haze (Figure 3-16). This is essential to ensure controllable results. The initial stress-anneal-straightening step helps minimize mounting non-uniformity, and reduces the amount of material needed to be removed.

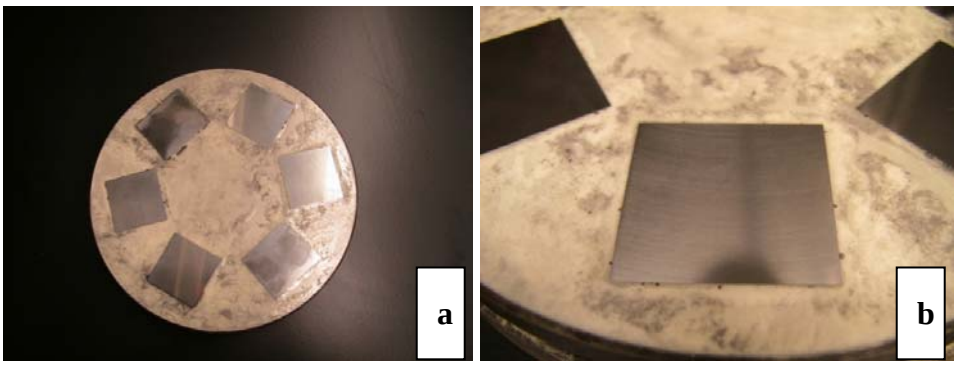


**Figure 3-16 Lapping started: a) before; b) after reaching long-range planarization**

The starting process for lapping uses oil-based 3 μm diamond slurry on a nylon woven pad with a slurry spray interval of 2 seconds every 35 seconds and a plate speed of 60 rpm, and a 20 lb tool pressure for 6 samples mounted on the ceramic sample holder. The spray interval was found to be a less critical parameter affecting the end result. Three particle sizes (1 μm, 3 μm and 60 μm) were evaluated at two

different tool pressures: 15 lb, 30 lb. Larger abrasive particle results in faster removal rates, but also produces greater roughness (see Figure 3-18, Figure 3-19 and Figure 3-20). Although almost twice as fast, using 60 μm slurry particles results in an $R_t$, ~10 times higher. The remaining experiments are based on 3 μm slurry, which offers a good balance between MRR and roughness. MRR, follows an approximately linear dependence on tool pressure (Figure 3-21), as predicted by Eq. (3.1). This can be attributed to the relatively large size (compared to the liquid layer thickness) and hardness (compared to titanium) of the slurry particles, which makes the rigid particle model closer to reality. $R_t$, an indicator for the amount of damage caused by lapping, shows a large jump at the highest pressure (Figure 3-22), which may be due to fluid pad interactions. The resulting surface finish after such a lapping process using 3 μm diamond slurry and 25 lb tool pressure is shown in Figure 3-25: ~1 μm sized scratches across the surface and the grain boundary associated defects are completely removed. The long-range planarization effect is demonstrated in Figure 3-17. The thickness of the samples as obtained from the manufacturer is measured with an average standard deviation of 9.51 μm. After lapping, the average standard deviation is reduced to 1.18 μm.

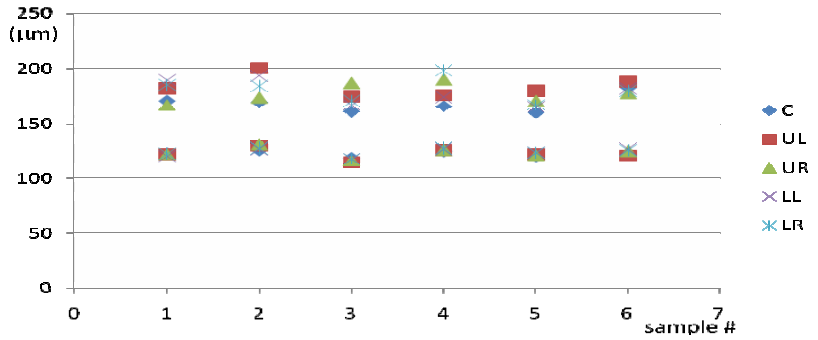


**Figure 3-17 Sample thickness variation before and after lapping on both sides**

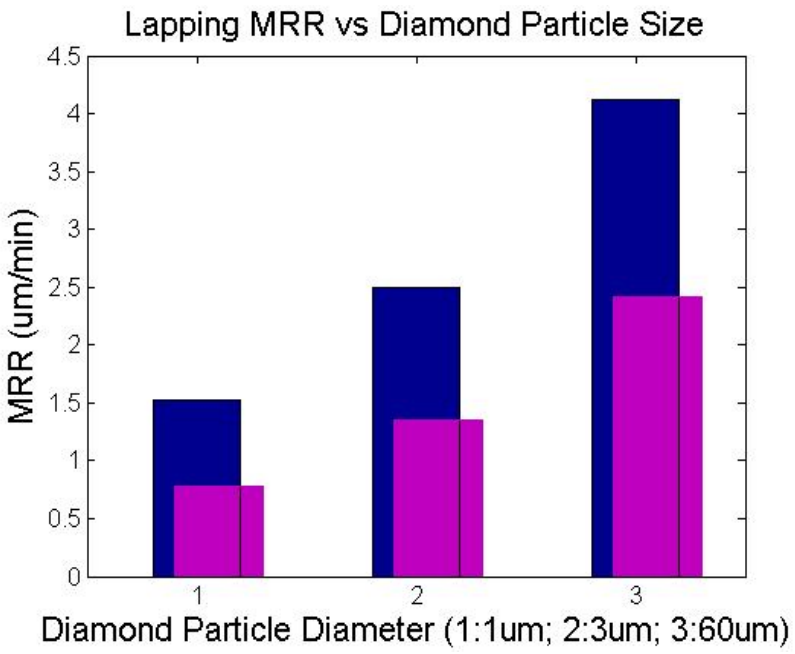


**Figure 3-18 Lapping MRR vs. diamond particle size (blue: 30lb; purple: 15lb)**

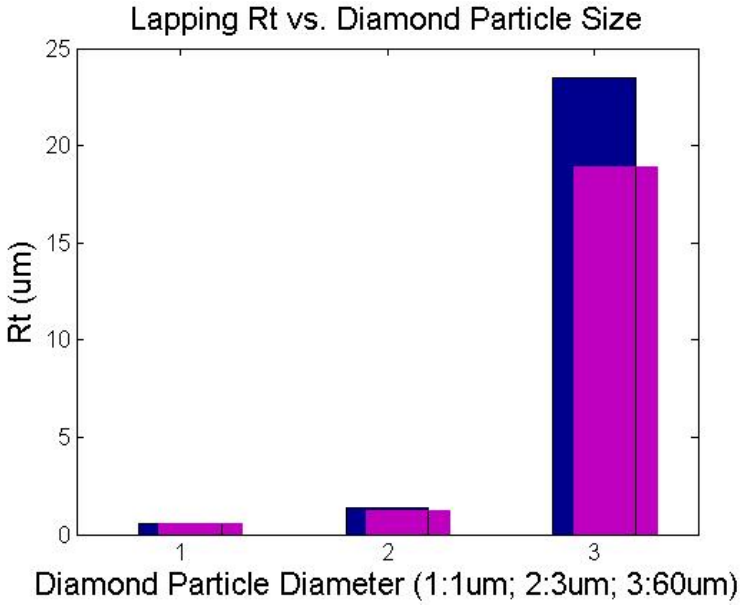


**Figure 3-19 Lapping peak to valley roughness vs diamond particle diameter (blue: 30lb; purple: 15lb)**

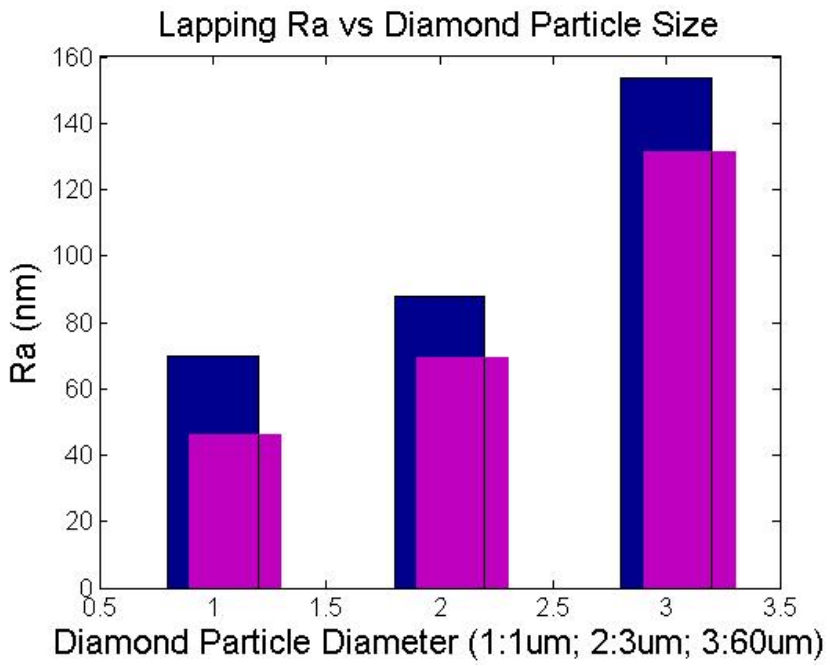


**Figure 3-20 Lapping average roughness vs. diamond particle size (blue: 30lb; purple: 15lb)**

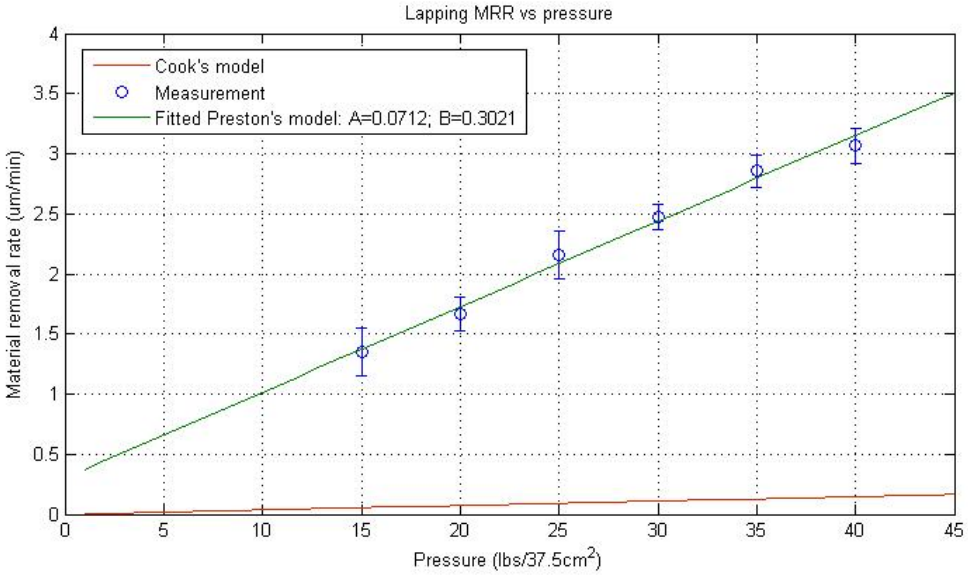


**Figure 3-21 Lapping MRR vs pressure**

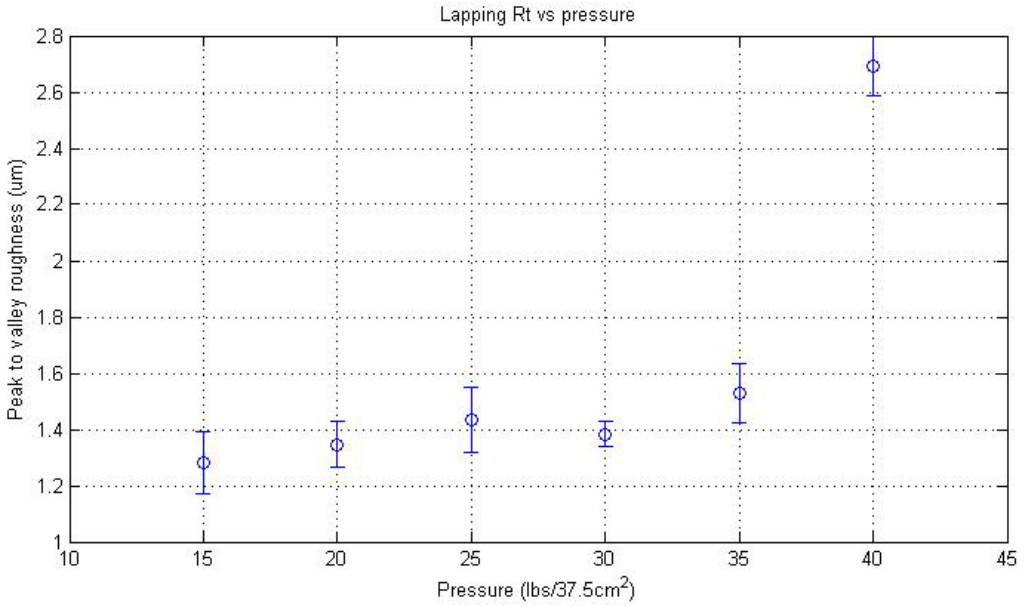


**Figure 3-22 Lapping peak to valley roughness ($R_t$) vs pressure**

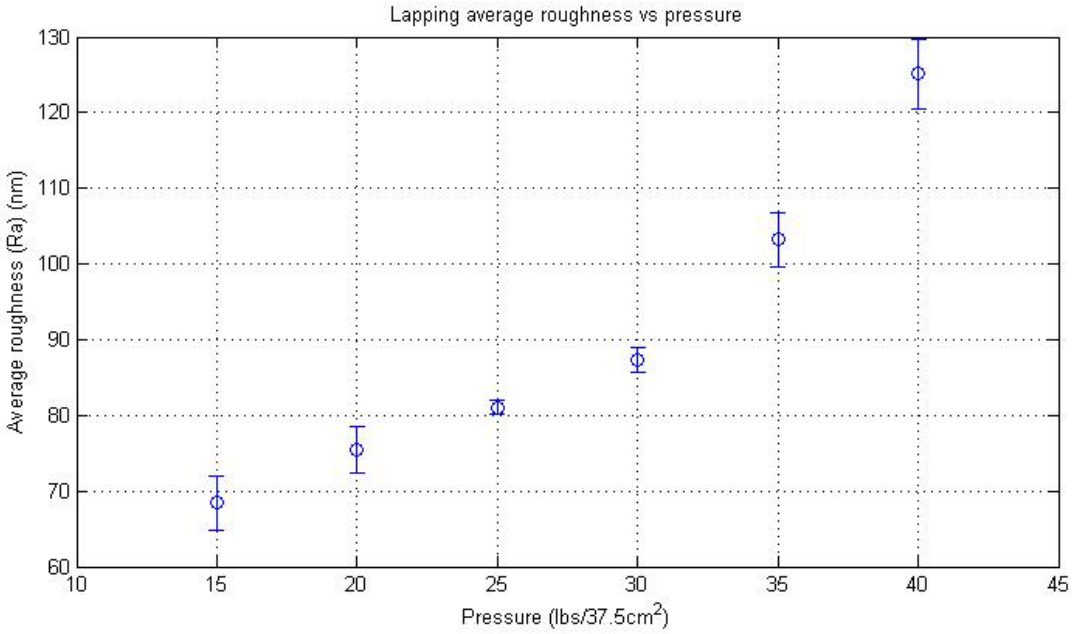


**Figure 3-23 Lapping average roughness ($R_a$) vs pressure**

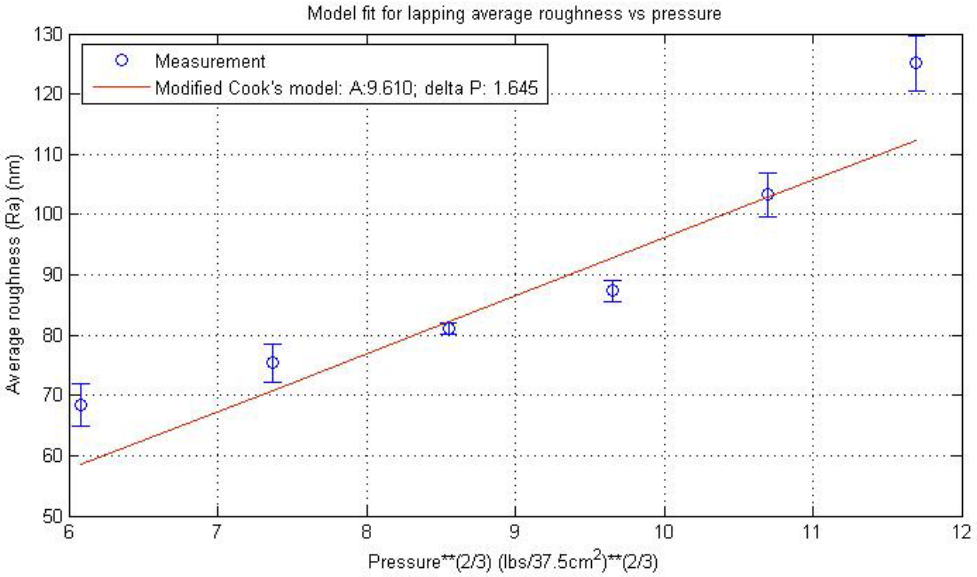


**Figure 3-24 Model fit for lapping average roughness vs pressure**

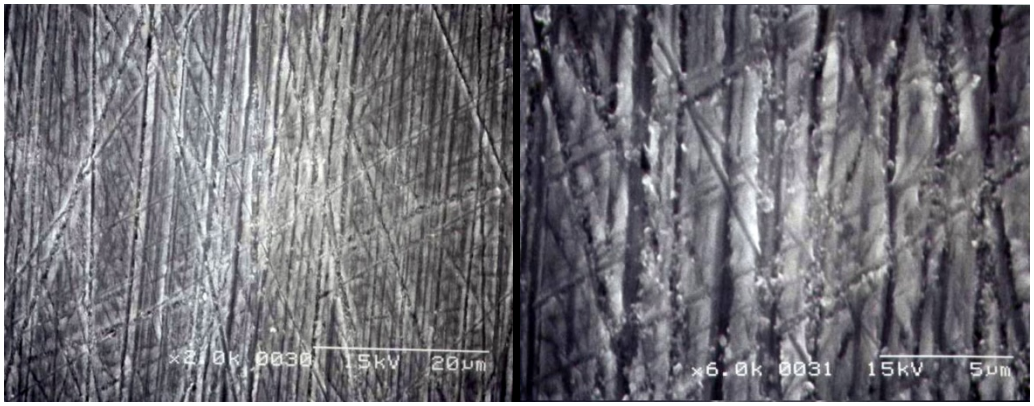


**Figure 3-25 Titanium surface after lapping process**

Another observation is the dependence of the results on condition of the pad. When a new pad is used, the *MRR* drops gradually until it levels off at a stable value, similar to the observation by Le et al. [6]. This phenomenon can be attributed to the

variable charging condition and adjusting the slurry application interval helps achieve consistent results.

The MRR rates of the lapping process using diamond slurries follow the Preston model (see Figure 3-21) with an initial offset, which can be attributed to tooling factors. The lapping/polishing machine is driven pneumatically and the load controlled through a series of valves. Although a lengthy calibration is performed on a weekly basis, it is inevitable that the actual pressure exerted on the samples contains an offset. The modified Preston's model can be written as

$$MRR = A * P + B = K_e * (P + \Delta_p) \tag{3.5}$$

where $\Delta_p$ represents the residual pressure due from the tool and $K_e$ the Preston coefficient. For the data shown in Figure 3-21, these parameters can be obtained with the linear model fit:

$$\begin{aligned} &\Delta_p = 4.2430\ lb/37.5\text{cm}^2 = 0.5032e04\ Pa \\ &K_e = 0.0712\mu m \cdot 37.5\text{cm}^2 / lb \cdot \min = 2.67 \cdot 10^8 \mu m^3 / lb \cdot \min \\ &= 6.0011e-05 \mu m / \min \cdot Pa \end{aligned} \tag{3.6}$$

while the MRR follows a linear dependency with the pressure, the rate at which it varies with pressure differs significantly (Figure 3-21) from Cook's model (Eq.(3.2)) derived from a first principle.

The roughness – both $R_t$ and $R_a$ - measurements also illustrate a monolithic trend (see Figure 3-22 and Figure 3-23) with increasing pressure. $R_a$ agrees well (Figure 3-24) with the 2/3 power dependence suggested by Cook's model (Eq.(3.3)). An unreasonably low equivalent plate charging factor, k ~1.85e-05, however, is needed to match the data with the model.

As lapped, the sample exhibited a compressive stress, as shown in Figure 3-26.

**Figure 3-26 Compressive stress due to lapping damage**

**2) Polishing**

The polishing process is based on 2 nm colloidal silica slurry suspended in distilled water. Three times the peak-to-valley roughness after lapping, or 3* $R_t$ ~5 μm, is used as the minimum polishing distance before taking the characterization data below. Insufficient material removal by polishing may still generate smooth surfaces but the residual stress caused by the damage from the lapping process can result in warping in thin samples (Figure 3-32). As illustrated in Figure 3-27, similar to the case of lapping, the MRR follows a near-linear dependence on tool pressure, consistent with Eq. (3.1). By following the same argument used for describing the pressure offset, the modified Preston's model is written as:

$$MRR = A*P + B = K_e*(P + \Delta_p)$$

$$\Delta_p = 4.5927\ lb/37.5\text{cm}^2 = 0.5449e04\ Pa \tag{3.7}$$
$$K_e = 0.2394\mu m \cdot 37.5\text{cm}^2 / lb \cdot hr = 8.9775 \cdot 10^8 \mu m^3 / lb \cdot hr$$
$$= 2.0178e-04 \mu m / hr \cdot Pa$$

Note that the residual pressure $\Delta_p$ obtained from the CMP results is close to (greater by ~7.61%) that from the lapping results, showing a consistency with the conjecture.

$R_a$ decreases monotonically as the pressure decreases. Fitting to the 2/3 power dependence to pressure gives an equivalent charging factor of k~5.92e-04.

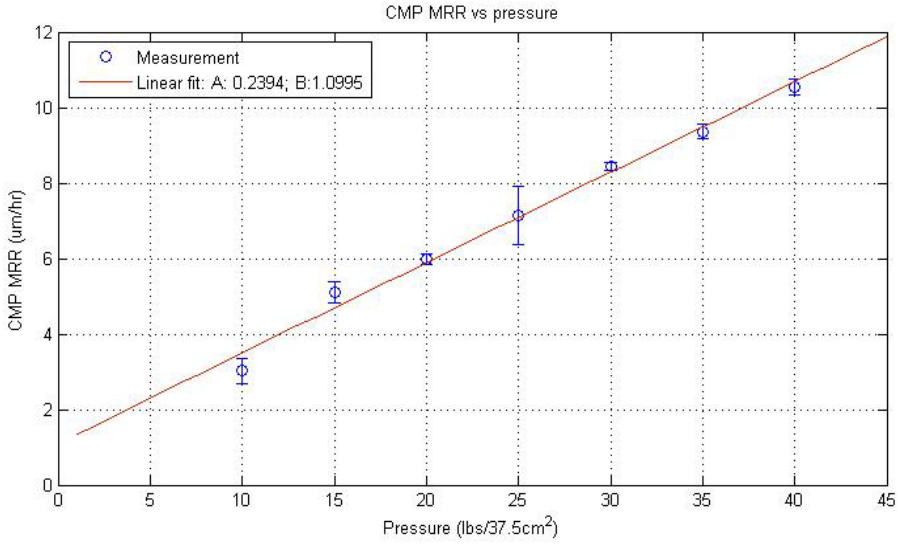


**Figure 3-27 CMP MRR vs. pressure**

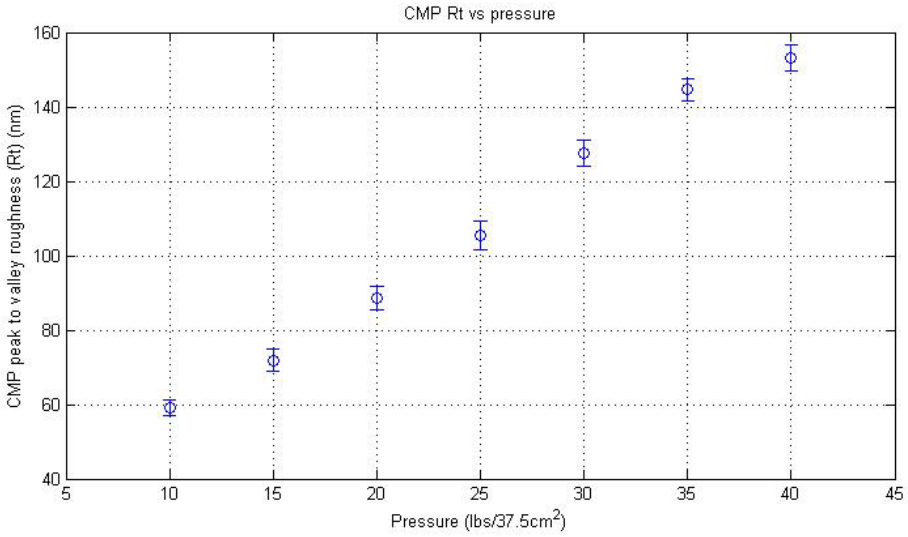


**Figure 3-28 CMP peak to valley roughness vs. pressure**

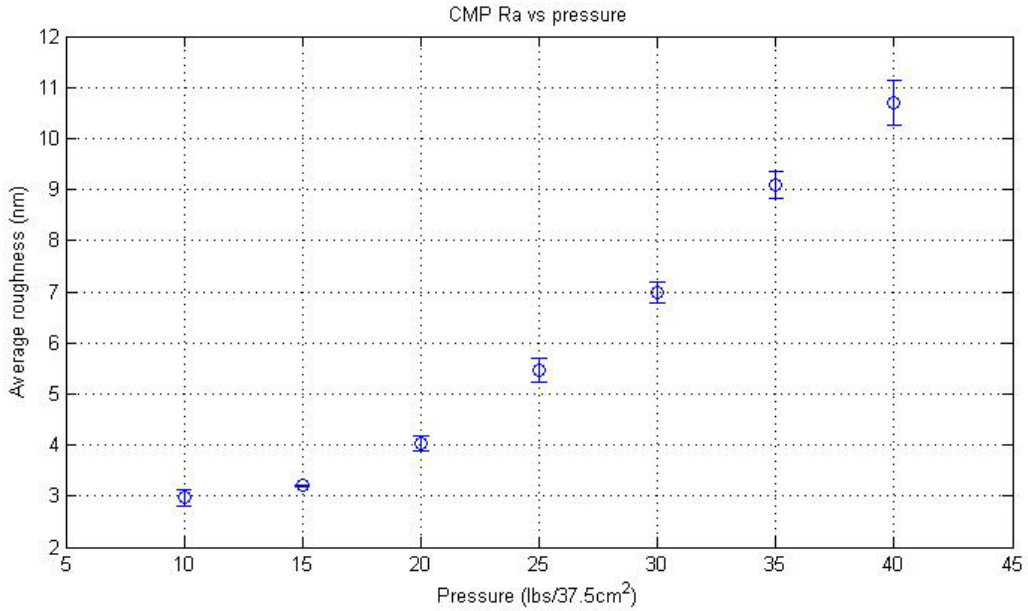


**Figure 3-29 CMP average roughness (Ra) vs. pressure**

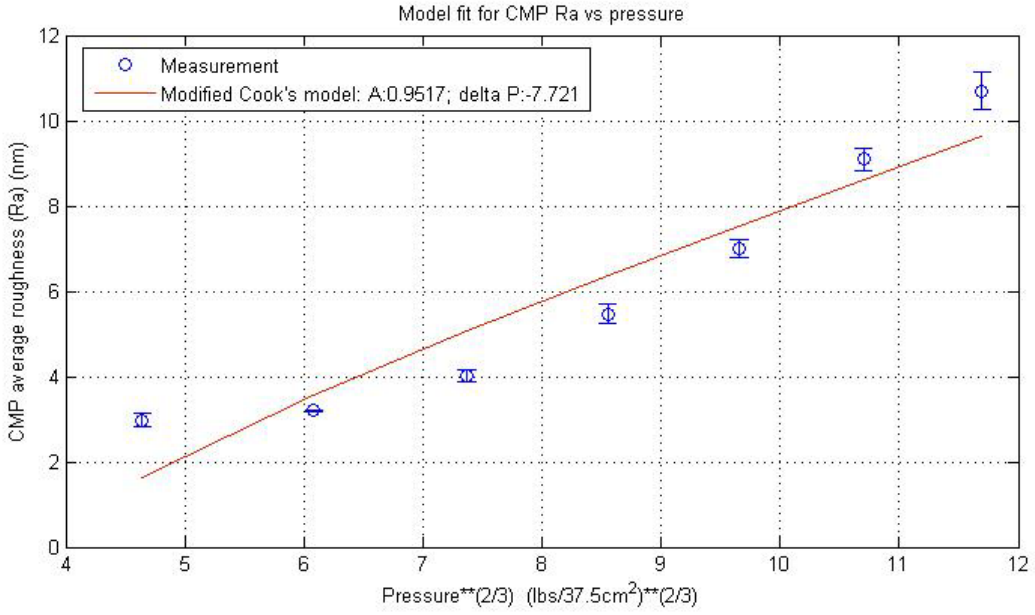


**Figure 3-30 Model fit for CMP average roughness vs. pressure**

The optimal pressure for polishing is determined to be ~15 lbs. The surface finish after the polishing is shown in Figure 3-31. Here, ~5 μm particles were used as a reference to demonstrate the smooth finish.

All data are based on measurements near the center of 1"x1" samples. Variations from sample to sample vary by 10-30%, depending on sample mounting and initial variations in samples as cut.


**Figure 3-31 Titanium surface finish after CMP**

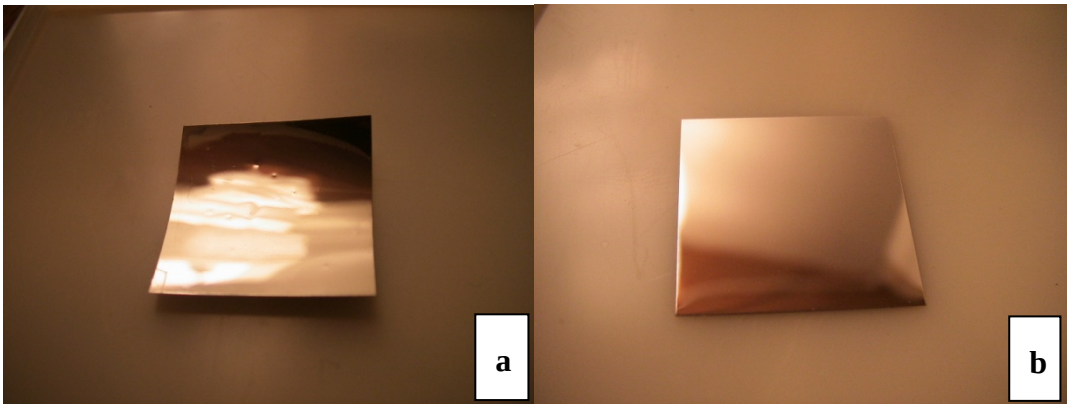


**Figure 3-32 Residual stress due to insufficient polishing. a: concave shape showing remaining damage; b: minimum curvature showing polish completion**

While reducing pressure, in general, helps reduce the roughness, the benefit levels off when pressure reaches a threshold, as indicated in Figure 3-30. The surface finish can not be used as the sole judge for a successful planarization process. The damage created by the lapping process can extend farther and insufficient polishing time manifests itself in the form of residual stresses (see Figure 3-32).

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# CHAPTER 4

# BULK TITANIUM WAVEGUIDE PROCESS DEVELOPMENT

## 4.1 Process overview

The fabrication process for the bulk titanium waveguide can be divided into 5 major steps: initial planarization, which prepares the samples for subsequent steps; deep trench formation, which defines the locations as well as lateral dimensions of the waveguides; trench-filling, which forms the dielectric material for the waveguide; final planarization, which trims the excess dielectric material on top, exposes the trenches from the bottom and creates electrical isolation; packaging, which bonds the waveguide structure to a recessed bulk titanium substrate, forming a protective cavity for the waveguide. Initial planarization has been covered in Chapter 3; this chapter will focus on the remaining four steps.

The deep trench formation, sidewall enhancement and dielectric trench-filling are shown in Figure 4-1. Starting from a sample that has been planarized (Chapter 3), a thick PECVD $SiO_2$ mask layer is deposited and subsequently patterned with photolithography and then etched in a $CHF_3$ plasma. Once the mask oxide is cleared, an anisotropic etch is performed to etch deep into the titanium substrate until the desired depth is reached. The resulting structure then undergoes oxide etching to remove the remaining mask oxide. At this step, the trenches are formed and inspected under an optical microscope for defects. Before the next step, the sample is ultrasonically rinsed in DI water to help remove the sidewall re-deposited films during the long titanium etch. Prior to depositing the high conductivity Au sidewall, an $O_2$ plasma is used, followed by an Ar sputtering process, to help further clean the sample sidewall. Next, without breaking vacuum, a thin titanium adhesion layer is sputtered,

followed by Au sputter deposition which enhances waveguide conductivity. A thin (~1 μm) layer of PECVD $SiO_2$ is subsequently deposited to prime the sidewall. Then, the trenches are filled with BCB and subsequently cured.

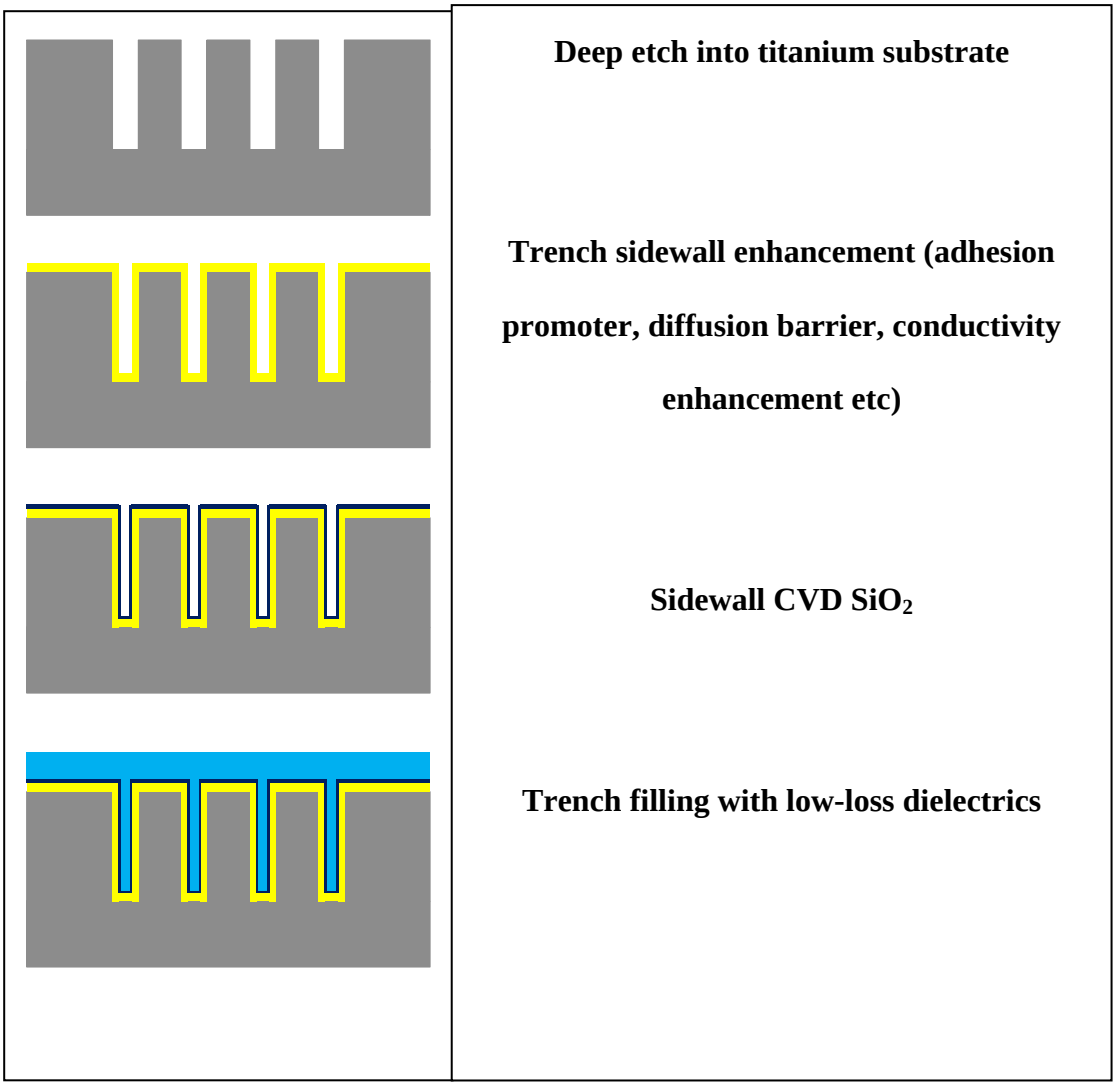


**Figure 4-1 Step I&II: Deep etch and trench-filling with low-loss dielectrics**

The top surface of the sample is now covered with a thick layer of BCB, which must be removed, in order to minimize the stress buildup. Next, the planarization step,

as shown in Figure 4-2, forms the waveguides and the electrical interconnections. This step removes the excess dielectric on the top surface and exposes the dielectric in the trenches from the bottom, therefore forming electrical isolation between blocks of titanium.

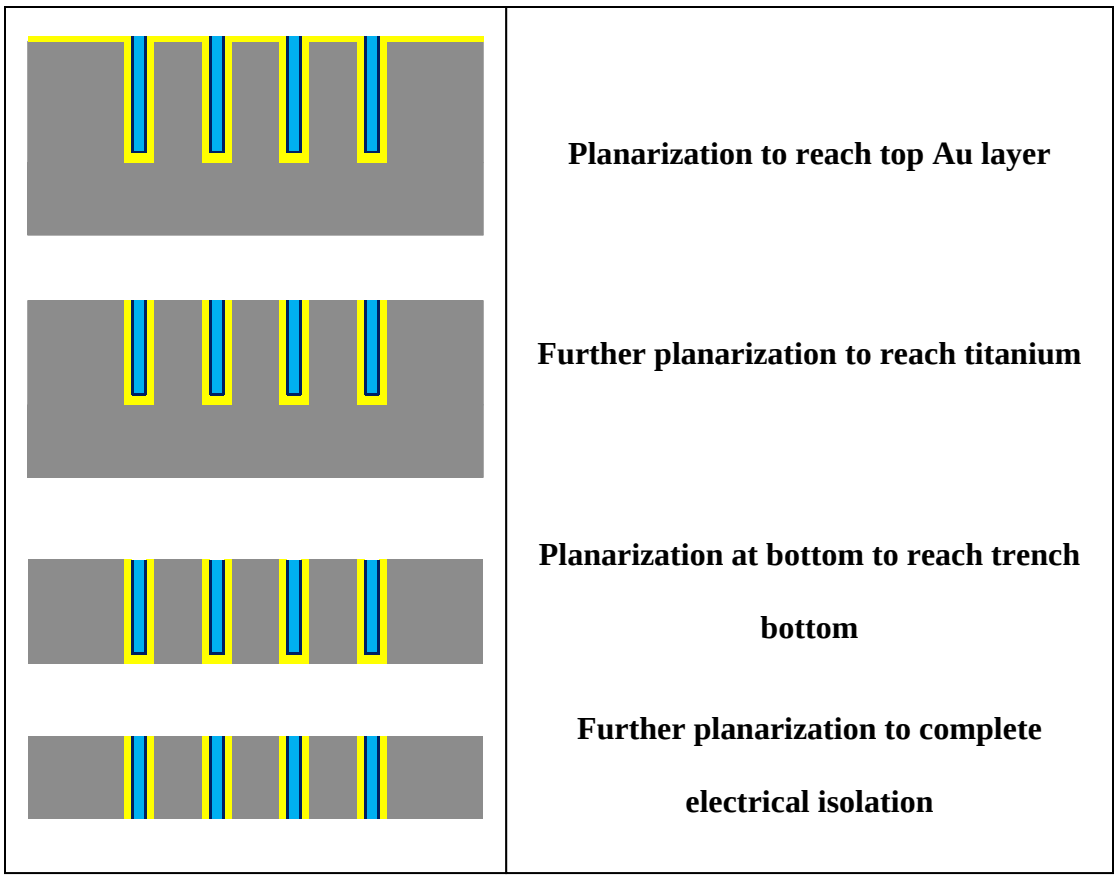


**Figure 4-2 Step III: waveguide and electrode formation through planarization**

Flat surfaces are achieved on both sides of the sample, which facilitate subsequent processing steps. Additional layers can then be added to form structures such as surface MEMS. With an additional deposited Au layer, heterogeneous components, such as IC chips, can also be integrated through surface mount.

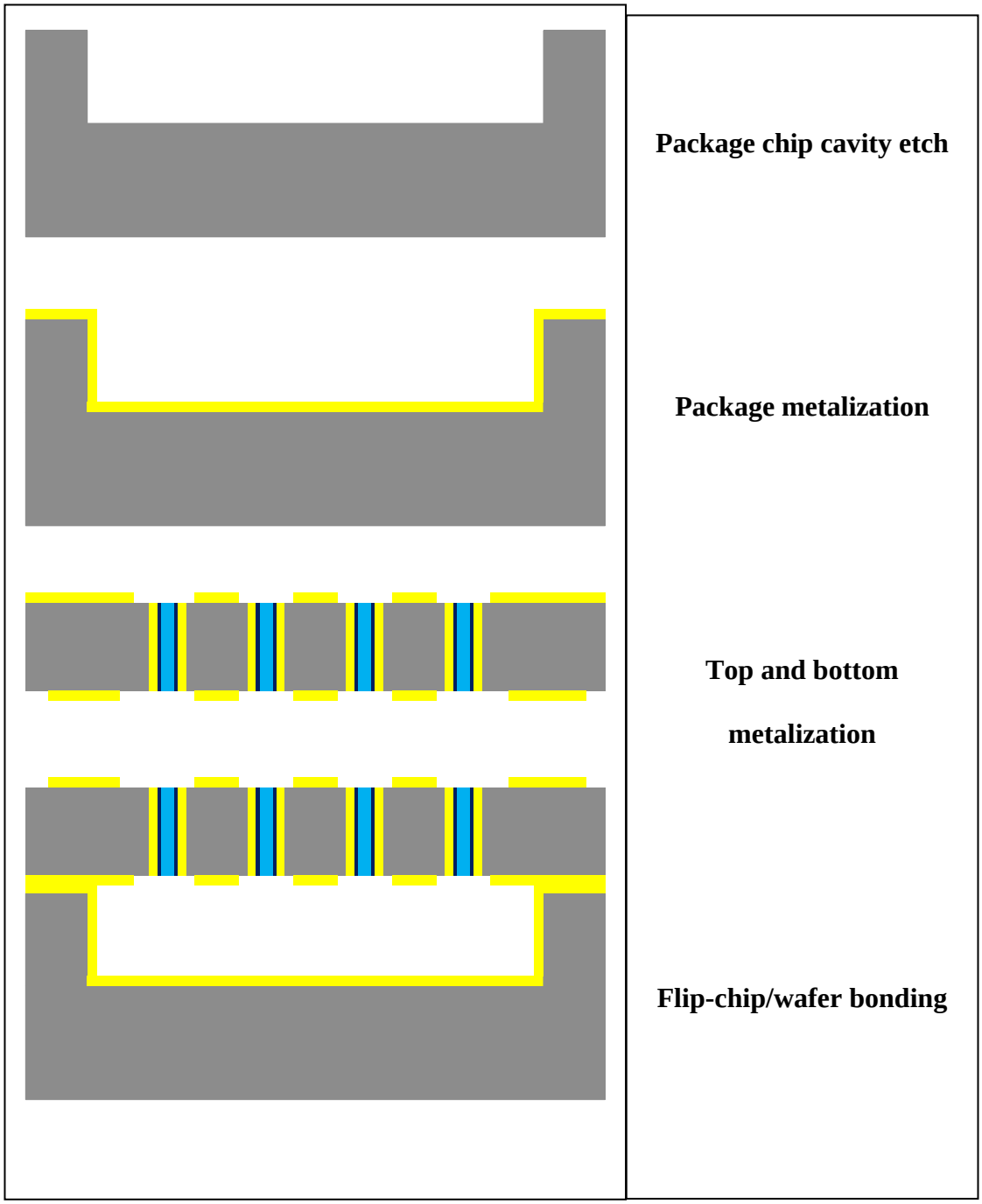


**Figure 4-3 Step IV: packaging and electrical interconnects**

This layer-stacking technique is also used to form the bulk-titanium package, which helps isolate the system from electromagnetic noise, as well as provides an enclosure to prevent the exposure to dust of moisture. Figure 4-3 shows the process step that is used to bond the package using Au-Au thermal compression. Metallization is also used to facilitate probing and integration with other devices/systems.

## 4.2 Titanium deep etch

### 4.2.1 Background

One of the enabling techniques in bulk titanium processing is deep etching. Similar to the case for silicon substrates , deep etching helps create high aspect ratio structures carved out of a bulk substrate, and generates a large surface area. Earlier research on titanium dry etching was performed on deposited thin films by implementing fluorine- and/or chlorine- based chemistries. Bulk titanium etching, however, is incompatible with these methods . The impurities and defects-filled grain boundaries are not sufficiently attacked by the etchants and act as micromasks. To overcome these issues, Aimi et al. introduced a cyclic procedure (MARIO process) similar to that in the Bosch silicon etch process. The isotropic etching is achieved by high-powered plasma based on a $Cl_2$/Ar chemistry, and sidewall passivation is obtained using an $O_2$ RIE. This method produced ~10:1 aspect ratio, structured with ~1 μm scalloping on the sidewall. Such features in trenches can generate undesirable scattering for RF waveguide applications. Parker et. al. introduced a new process, (TIDE process [10]) which extended the maximum etch depth, as well as the aspect ratio (see Figure 4-4), through the use of an Inductively Coupled Plasma (ICP) system. A single anisotropic step was used, which removes the sidewall scalloping intrinsic to the MARIO process.

While these developments set the basis for the etching needed by the waveguide fabrication process, additional research is necessary to extend the etch depth and ensure etch uniformity over a large area.

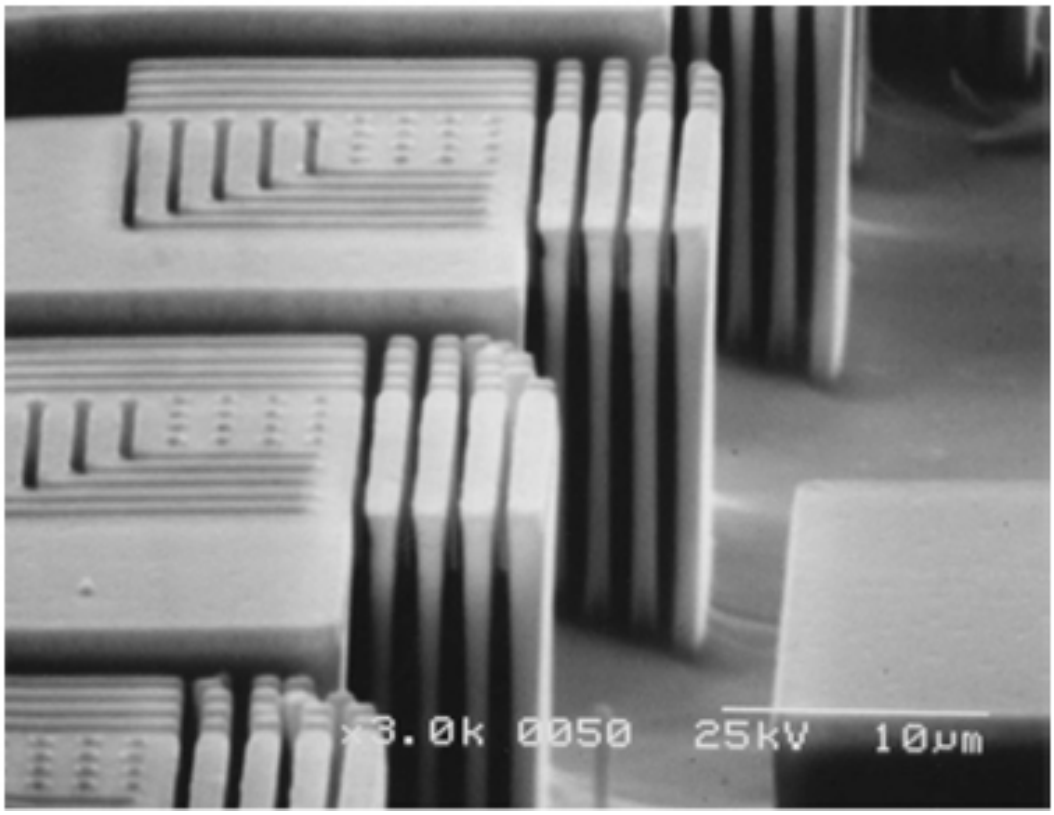


**Figure 4-4 High aspect ratio, bulk titanium structures created by the TIDE process [10].**

### 4.2.1 Detailed etch procedure

Both the MARIO and TIDE processes use a sputtered $TiO_x$ film as the etch mask, which we found to have insufficient uniformity over an area of 1”x1”. Such

uniformity is required for the success fabrication of long waveguide. Our experiments show that high-density plasma-deposited PECVD $SiO_2$ provides superior uniformity over large areas. With a low stress recipe and an improved sample mounting procedure, we have successfully extended the etch to beyond 200 μm in open areas and over 100 μm in 15 μm trenches (Figure 4-5).

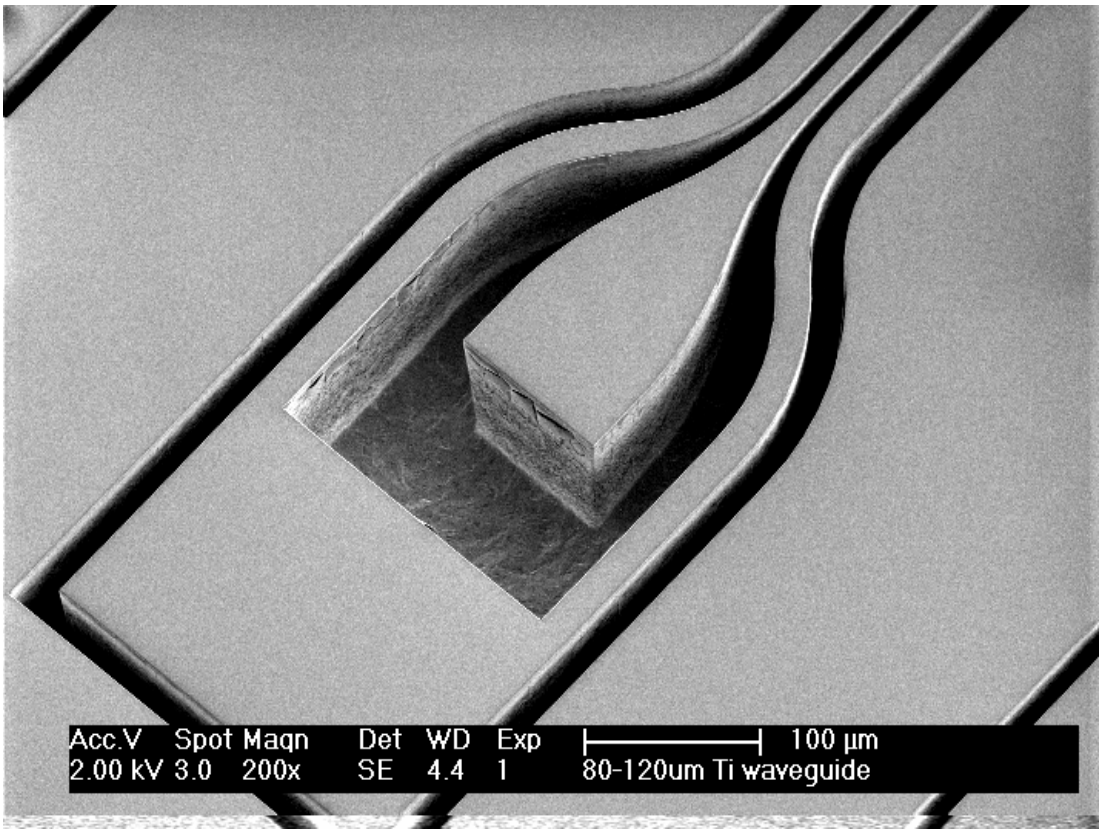


**Figure 4-5 Deep etch into bulk titanium substrate using a PECVD $SiO_2$ etch mark**

Mounting of the samples onto the 6" silicon carrier wafer requires the use of an interface layer to help conduct the heat generated by the high-power ICP used during the deep etch. Previous mounting methods used a hydrocarbon-based diffusion pump

oil, which was insufficient for titanium substrates with thickness in the range of 100-250 μm. The stress in the mask layer induces curvature in the substrate which causes the thin oil layer to be removed from the areas with a larger gap between the sample and the carrier wafer. In addition, the oil loses viscosity at higher temperatures and fails to act as an adhesive layer and result in oxide etch failures. We solved this problem by using a low-temperature (50°C), low-stress (~156MPa compressive) recipe for the deposition of PECVD $SiO_2$ etch mask, as well as the use of a high viscosity, thermal grease as the adhesive layer. The detailed parameters are listed in Table 4-1.

The mask oxide is then patterned and etched in an ICP-based $CHF_3$ etcher. The success of this process is highly dependent on the thermal conduction between the sample and the helium-cooled carrier wafer. Insufficient coverage of a thermally conductive adhesion layer burns the photoresist. The etch rate is ~ 210 nm/min. The total etch time for a 4 μm mask oxide, with 10% overetch, is therefore ~ 21 minutes. Before starting the titanium etch, a short $O_2$ plasma etch is used to remove the polymer formed during the $CHF_3$ etch; then an Ar plasma etch is used to remove the titanium oxide formed during the $O_2$ plasma.

Both the oxide and the titanium etches are performed in a Panasonic E640 ICP etch tool which is capable of very high density ICP with good uniformity over a 6" diameter. The depth of the titanium etch is determined by the etch recipe, the mask oxide thickness, and the trench width. We discovered that the maximum etch depth is predominately determined by the trench width. In other words, loading effects cause the etch to slow down significantly and eventually stops. We have achieved a maximum depth of 140 μm for 15 μm trenches in 120 minutes.

**Table 4-1 Process parameters for deep trench etch in bulk titanium**

| Step name | Parameters | Notes |
|---|---|---|
| Sample preparation | Acetone/IPA/DI, 1 minute each with ultrasound; dry | Dry in 110$^{o}$C convection oven for 5 minutes |
| Mask layer deposition | 3-5 μm, depending on desired etch depth | Low stress recipe @ 50 $^{o}$C; ~156 MPa compressive stress. |
| Lithography | HD8820 polyimide;6K rpm 30 seconds ~2.8μm; softback @ 120$^{o}$C for 60 seconds; Karl Sus MA6 contact aligner 25 seconds exposure; Develop in MF701 for 60 seconds | Polyimide provides vastly superior thermal stability and scratch resistance compared to conventional photoresist. |
| Etching mask oxide | 40 sccm $CHF_3$ ; 500W source; 400W forward bias; 1Pa pressure | Chamber clean with $CF_4/O_2$ and $O_2$ RIE for 15 minutes each; End point detected through observation under optical microscope |
| Etching bulk titanium | 100 sccm $Cl_2$, 5 sccm Ar; 400W source; 100W forward bias; 2Pa pressure | Chamber clean with $CF_4/O_2$ and $O_2$ RIE for 15 minutes each; ~2 μm/min initially, ~140 μm maximum etch depth for 15 μm trenches |

## 4.3 Conductivity enhancement with sidewall Au deposition

As demonstrated in Chapter 2, the overall transmission loss depends largely on the conductivity of the waveguide conductors. A sidewall Au film exceeding ~2 times the skin depth can reduce the conductor loss by ~ 4 times. Table 4-3 outlines the process used for this sidewall enhancement.

**Table 4-2 Process parameters for sidewall enhancement with Au**

| Step name | Parameters | Notes |
|---|---|---|
| Sample preparation | 5 minutes in DI with ultrasound | Re-deposition from etching can lead to excess roughness on sidewall roughness. |
| Ti adhesion layer sputtering | ~ 30 nm | 2 minute Ar sputter clean of sample prior to start. 30 minutes target pre-sputter |
| Au sputtering | ~ 4 μm | ~ 1 μm sidewall coverage, less toward bottom of trenches. |

Figure 4-6 shows a waveguide structure after the sputtered Au sidewall enhancement. A closer inspection of Figure 4- shows some defects in the Au layer, which can be attributed to the remaining sidewall passivation layer from the deep etch (see Figure 4-7)

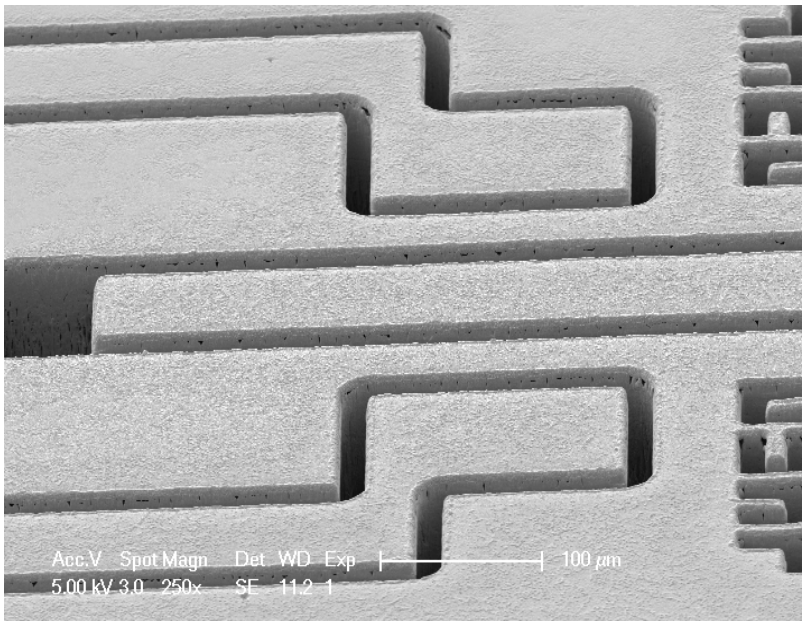


**Figure 4-6 Waveguide structure after sputtered Au sidewall enhancement**

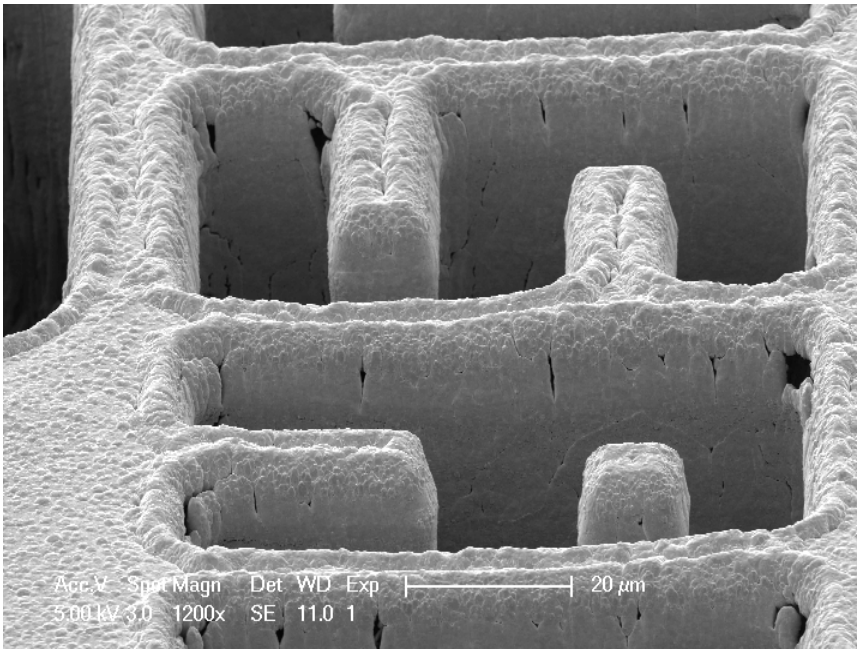


**Figure 4-7 Zoomed in view of sputtered Au sidewall enhancement**

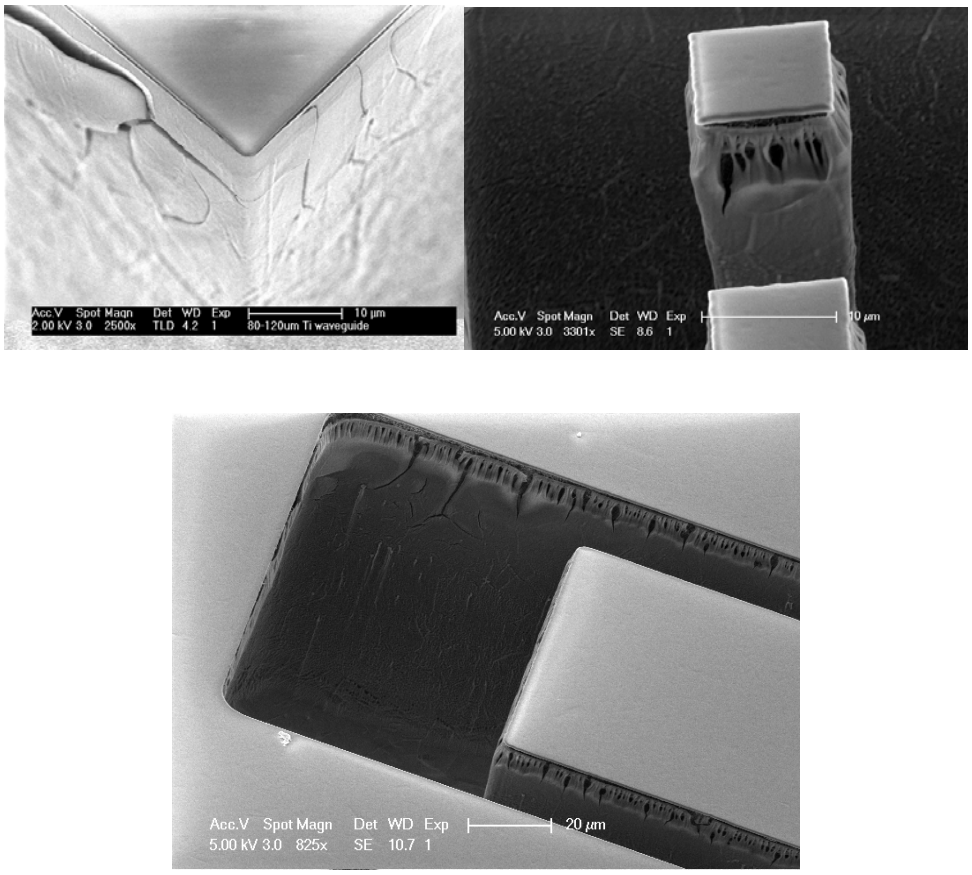


**Figure 4-8 Re-deposited film on trench sidewall after deep etch**

## 4.4 Deep trench-filling process

### 4.4.1 Background

Trench-filling has long been a subject of interest for both VLSI and MEMS fabrication. Widely implemented techniques such as thermal oxidation, LPCVD, and polymers have been applied to fill trenches of various dimensions. For the fabrication of integrated circuits, narrow trenches filled with an oxide sealing layer and a polysilicon plug, also known as "deep trench isolation"[11, 4] provides a compact, and higher

performance alternative to the more traditional LOCal Oxidation of Silicon (LOCOS) isolation method . There trenches are usually <1 μm in width, and <20 μm deep. As one of the bottlenecks in the growing trend of miniaturizing transistor dimensions, the surface topology from the multiple layers of metallization poses issues such as stress and reliability. Trench-filling techniques based on spin-on methods, along with planarization techniques such as CMP, proved to be sufficient to reduce the surface topology.

The characteristics of commonly used trench-filling methods are listed in Table 4-4. Among the methods that create stoichiometrically correct $SiO_2$ films, thermal oxidation offers the best dielectric quality, but takes place at a prohibitively high temperature for titanium processing. PECVD is capable of very low processing temperature, but the intrinsically poor step coverage makes it undesirable for filling deeper trenches.

LPCVD offers improved conformality and yet the processing temperature is, especially for recipes that give better conformality, still higher than the temperature allowed for titanium in an oxidizing ambient. Reflow processes based on phosphorus- and/or boron- doped $SiO_2$ show promise for filling deep trenches without reaching the temperature needed for thermal oxidation. Spin-on polymers, such as Spin-On-Glass (SOG) are designed to fill shallow trenches as wide as ~1 μm and as narrow as a few tens of nanometers . BCB is widely used as a planarization agent , and a RF dielectric, due to its low resistive loss.

For trench-filling applications, the high quality of CVD-deposited $SiO_2$ can be negated by the formation of voids, or, “key hole”, due to insufficient conformality. Therefore, the mechanism of CVD trench-filling needs to be investigated.

**Table 4-3 Parameters for common uses of low-loss trench-filling dielectrics**

| | Maximum depth (μm) | Width (μm) | Maximum aspect Ratio | Resistivity (Ωcm) | Process Temper-ature ($^oC$) | Notes |
|---|---|---|---|---|---|---|
| PECVD $SiO_2$ | Shallow (~5 μm) | Medium (~1-5μm) | Low (~3:1) | Very high (>$10^{18}$) | 100-400 | Low density |
| LPCVD $SiO_2$ | Medium (~20μm) | Medium | Medium (~10:1) | Very high | 400-600 | Medium density |
| Thermal oxidation | Medium | Narrow (~1-3μm) | Medium | Very high | 900-1200 | Highest quality oxide |
| SOG | Shallow | Narrow to very narrow (~0.1μm) | very high (>20:1) | High (>$10^{14}$) | 250-425 | Organics in film |
| BPSG/PSG reflow | Medium | Medium | High (~20:1) | Very high | 450-800 | |
| BCB | High (~50μm) | Medium to high (>10μm) | (~10:1) | Very high | 210-300 | |

Figure 4-9 illustrates a simplified mechanism for "key-hole" formation during a CVD process.

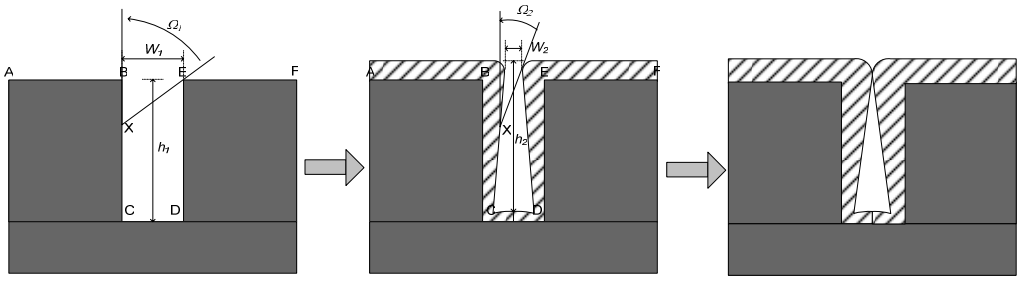


**Figure 4-9 Mechanism for CVD trench filling**

The majority of CVD $SiO_2$ processes use silane as a precursor . Silane molecules react with other oxidizing precursors to form $SiO_2$ molecules, which then get deposited onto the trench surfaces. Assuming low mobility of both silane and $SiO_2$ molecules on the surface, the thickness of the resulting film at any given location is therefore proportional to the deposition rate of $SiO_2$ molecules at this location. At lower pressures, the mean free path far exceeds the trench dimensions, which means that the probability of a $SiO_2$ molecule above the trench landing on any location inside the trench is approximately proportional to the solid angle from the perspective of that location. As the location moves further down toward the bottom of the trench, the solid angle decreases and reaches a minimum at the corners.

The deposition rate, therefore, reaches maximum at the top corner of the trenches and minimum at the bottom corners. A re-entrant profile of the $SiO_2$ film results on the sidewall. As the deposition continues, the solid angle at the bottom of the trench is reduced due to the shadowing effect of the added material near the top of the trench. Eventually, the top of the trench is closed, producing an unfilled gap underneath.

### 4.4.2 TEOS trench filling

One way to overcome the limited conformality is to increase the surface mobility of the precursor. We experimented with a process based on Tetra-Ethyl-Ortho-Silicate (TEOS), a material with a molecular composition shown in Figure 4-10.

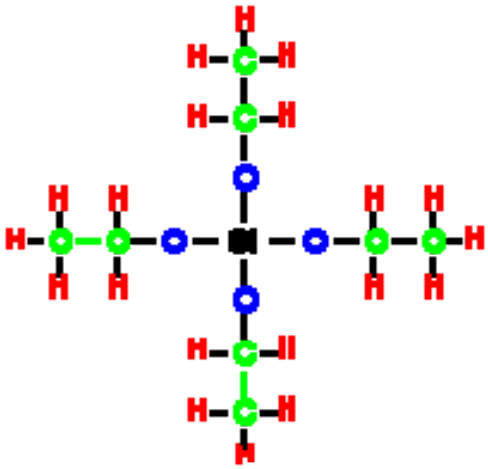

**Figure 4-10 Molecular composition of TEOS**

Having a much larger molecular weight compared to silane, TEOS is liquid at room temperature with a vapor pressure about 1.5 torr. The conversion of TEOS to $SiO_2$ can be achieved either thermally, or with a plasma. As seen from Figure 4-10, the silicon atom is already oxidized, compared to the case of silane and, therefore, the reaction can be simplified as the disassociation of the organic, alkyl groups. The surface mobility of TEOS is far superior compared to silane, therefore improving conformality. To lower the process temperature required for the disassociation of TEOS molecules, either ozone or plasma excitation can be introduced. While the addition of ozone preserves the excellent conformality at lower temperatures, it also results in significant problems with stress buildup, moisture uptake, and stability . The film quality is also strongly influenced by the nature of the substrate. Plasma excitation also lowers the deposition temperature and helps achieve faster deposition rates suited for deep trenches. The added flexibility allows the process to achieve more stable, less moisture-absorbing films . Increasing the RF power and pressure,

while descreasing the gap between plasma electrodes and adjusting the O2/TEOS ratio can help increase the film density. However, the nature of the plasma also reduces the conformality. To overcome this issue, we tried an approach that combines the PETEOS with low pressure Ar sputtering, which trims the deposited oxide more at corners than inside the trenches. The equipment used is an Applied Materials P5000, a cluster tool with multiple champers for deposition and sputter etching without breaking vacuum during the automated chamber-to-chamber transport, as shown in Figure 4-11.


**Figure 4-11 Applied Materials PT5000 clustered deposition/etching tool**

The optimized PETEOS process has the following parameters for the deposition step: Pressure: 10.0 torr; RF power: 450 W; Temperature: 390$^{o}$C; Electrode gap: 200 mils; Gas flows: TEOS:950 mgm, $O_2$: 440 sccm, He(cooling): 500sccm.

The deposition rate is ~ 660 nm/min. The sidewall conformality is evaluated on a silicon sample with trenches of variable widths (see Figure 4-12). A 100 nm titanium

film was sputtered onto the surface of silicon trenches to simulate the effect on a titanium substrate.

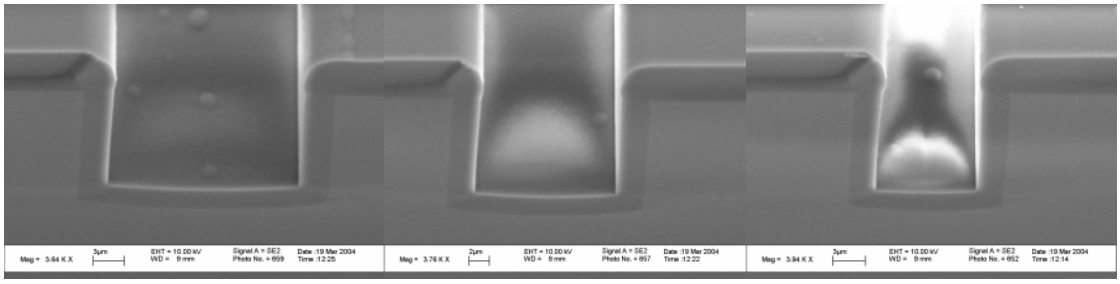

**Figure 4-12 Step coverage of PETEOS film on silicon samples**

As the trenches become narrower, however, the conformality is insufficient in avoiding void formation (see Figure 4-13).

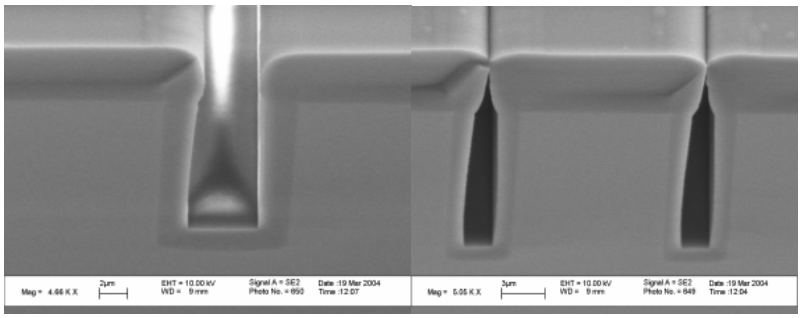

**Figure 4-13 Key-hole formation in trenches with PETEOS**

To overcome the lack of conformality intrinsic to the CVD process, we tried a process which breaks up the deposition into short steps and inserts Ar sputtering steps in between to reduce the film thickness at the corners. This method reduced the void successfully (see Figure 4-14). However, the overall deposition rate is also significantly reduced and the procedure requires a great deal of control and very fine steps. The recipe used to produce the results shown in Figure 4-14 has 20 deposition steps and a 90% deposition/etch ratio.

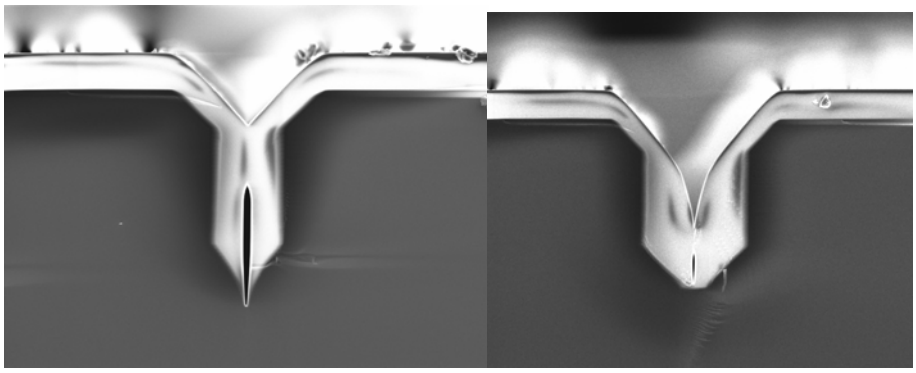

**Figure 4-14 Trench fill of PETEOS with alternating Ar sputtering**

While this process shows some promise, the difficulties in step control, the prolonged machine time (each process for samples in Figure 4-14 required more than 15 hours of combined deposition/sputtering/transport time) and associated cost, make it inappropriate for filling wider and deeper trenches.

### 4.4.3 BCB trench fill

For trenches deeper than 50 μm and wider than 10 μm, oxidation and CVD face challenges such as stress buildup, and void formation. While polymer fill may still leave residual stresses, it can fill trenches completely, given the right surface properties. The selection criteria are loss (resistivity), viscosity (thickness), and adhesion to titanium, gold and $SiO_2$ surfaces. We choose BCB for the following reasons :

- Dielectric constant (2.5) nearly independent of temperature and frequency (for Ka band)
- Low leakage current: $4.4 \pm 0.5 \times 10^{-10}$ A/cm2 (0.5 MV/cm) and $6.8 \pm 0.8 \times 10^{-10}$ A/cm2 (1.0 MV/cm); high resistivity: $1 \times 10^{19}$ Ω-cm; and low loss tangent: $\tan\delta <\sim 0.008$ for Ka band
- High breakdown voltage: 5.3 ± 0.2 x 106 V/cm

- Good thermal stability: $T_g > 350^oC$;
- Low stress (on silicon): < 28 MPa
- Excellent planarization properties
- Wide range of different thicknesses

The chemical structure of BCB (benzocyclobutene) is composed of a benzene ring attached to a cyclobutene ring. Due to its antiaromatic nature, the monomer is easily polymerized and the cross-linked structure is very stable. Originally developed as a thin-film dielectric, the BCB family has been expanded into a wide range of thicknesses and is used extensively for packaging and interconnect, due to its excellent planarization properties [12]. We selected the most viscous BCB polymers, the photo-definable 4026-46 and the dry-etchable 3022-63 , both offered by Dow Chemical, due to the wide variation in the trench dimension to be filled. The Dow polymers are divinylsiloxane (DVS)-based with a molecular composition of its monomer illustrated in Figure 4-15.

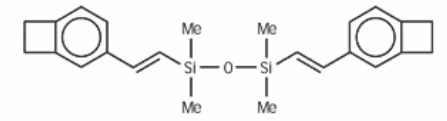


**Figure 4-15 (DVS)-based monomer for BCB**

Our experiments indicated that 3022-63 produces the best trench-filling results with the cleanest surface finish.

Table 4-4 lists the process parameters used in the trench filling process. Surface preparation plays an important role in trench-filling. A hydrophilic surface helps ensure void-free filling.

**Table 4-4 Process parameters for trench-filling with BCB**

| Step name | Parameters | Notes |
|---|---|---|
| Surface preparation | Acetone/IPA/DI for 1 minute each with ultrasound; Bake in 110C convection oven for 5 minutes; $O_2$ RIE clean (300mT, 100W, 1minute) | Surface needs to be dry and flake-free from previous processes. |
| $SiO_2$ lining layer | 1 μm high density PECVD | Low-stress recipe with good conformality |
| Adhesion promoter | AP3000, 3Krpm for 30 sec with 500rpm/sec ramp; bake @ 115$^o$C hotplate for 30 sec | Baking promotes adhesion |
| BCB deposition | Static dispense; 3Krpm for 45 sec with 500rpm/sec ramp; | ~12.9 μm thick BCB after cure |
| Edge bead removal | ~1mm on all edges with razor blades | Use T1100 to clean and prevent BCB overflow |
| Prebake | 90$^o$C for 60 sec on hotplate (solvent removal) | Overbaking can reduce BCB planarization properties; prebaking in vacuum oven can help trench-filling uniformity by reducing air bubbles trapped in BCB |
| Curing | Multi-stepped cure: Step1: 90$^o$C 1min (stabilization); step2: ramp to 150$^o$C @ 10$^o$C/min, stay for 15 min (facilitates planarization before cross-linking); ramp to 210$^o$C @ 3$^o$C/min, stay for 10 min (slows curing, furthers planarization, and helps prevent temperature overshooting); ramp to 250$^o$C @ 10$^o$C/min, stay for 2 hr. | In sealed programmable oven purged and filled with high purity $N_2$ at 1 atmospheric pressure; slow ramping helps promote film uniformity and minimizing cracking after cure |

As we experimented with various surfaces for BCB trench-fill, we discovered that it is critical to minimize the amount of moisture on the surface prior to the application of BCB. A 100 nm sputtered titanium layer on the sidewall of etched bulk titanium trenches helps stabilize Au adhesion to bulk titanium. AP3000, the Dow-developed adhesion promoter, needs baking for consistent bonding of BCB on gold surfaces.

Another critical control parameter is curing. BCB starts to cure at temperatures as low as 150°C. However, the degree of cross-linking increases dramatically as the temperature exceeds 180°C. Figure 4-16 shows the curing behavior of BCB as a function of temperature and time.

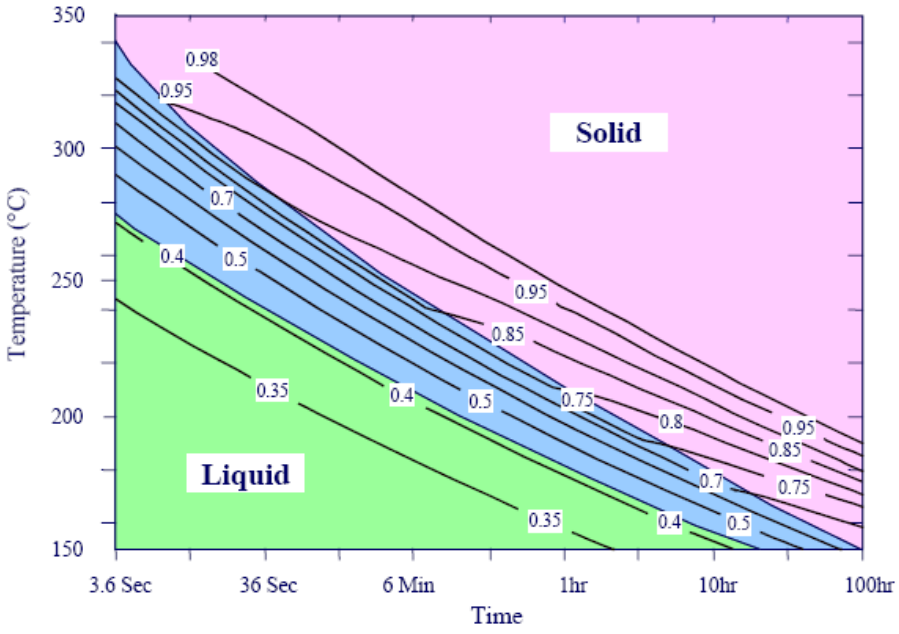


**Figure 4-16 Extend of BCB curing versus temperature and time**

Since the trenches to be filled with BCB vary significantly in widths and, therefore, aspect ratio, it is imperative to ensure planarization with a reflow process before the final curing step.

It has been shown repeatedly in the literature the importance of a slow, "soft", cure for the effectiveness of BCB planarization. We found that 150$^{o}$C is effective in enhancing the planarization of BCB without significant cross-linking. Figure 4-17 shows the resulting fill of BCB on a 5 μm wide trench covered with 100 nm thickness sputtered titanium. Extensive tests were also conducted on bulk titanium surfaces but, due to the difficulties in cross-sectioning deep titanium trenches, we use titanium covered silicon trenches for cross-section examination.

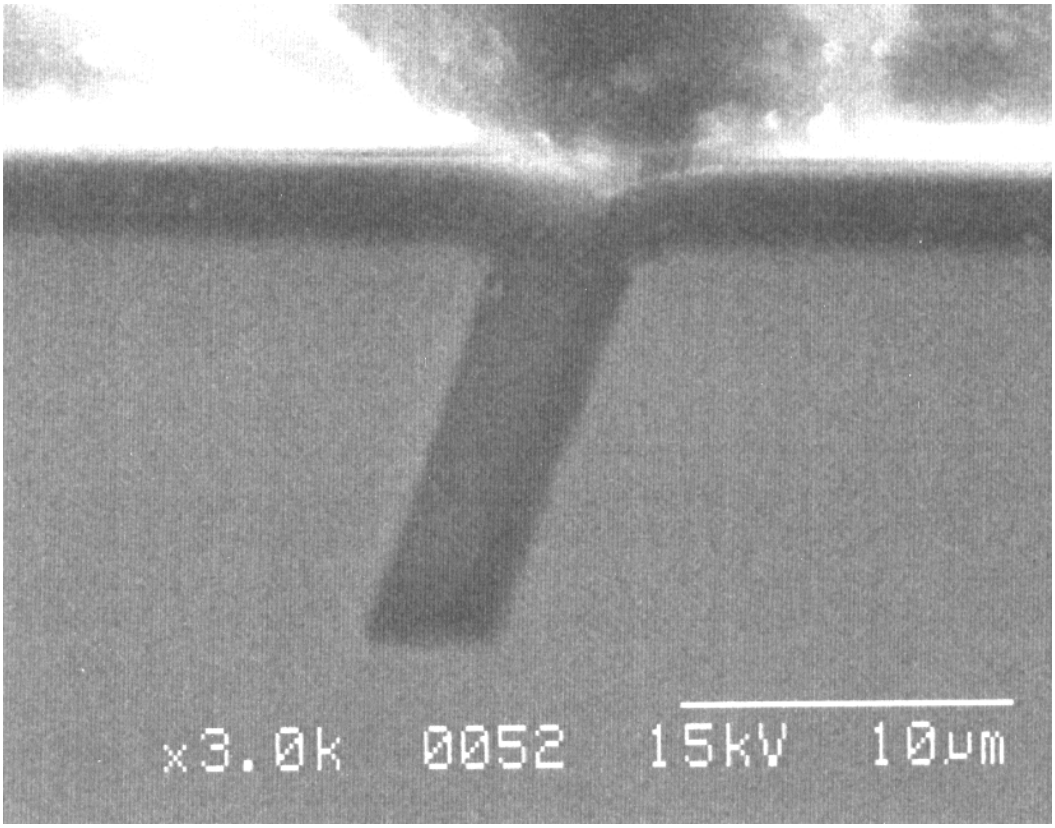


**Figure 4-17 5 μm silicon trench (coated with 100nm sputtered Ti) filled with BCB**

## 4.5 Planarization and electrical interconnection formation

### 4.5.1 Front side planarization

Trench-filling with BCB leaves behind a thick layer of BCB in areas without trenches. This layer, often greater than 10 μm, depending on the specific processing procedure, can create stress that leads to global deformation in thin samples. Removing the excess BCB can be done either by dry etching or lapping/CMP; the techniques are discussed in detail in Chapter 3.

The advantage of lapping and CMP is such that BCB is a much softer material than titanium and can therefore be readily removed. The difference in removal rate as well as appearance of the materials makes it easy to stop the lapping process without removing too much titanium. The process we use is the same as described in Chapter 3.

Figure 4-18 shows the top surface of the titanium waveguide after planarization. Note that the titanium regions are not charged during SEM imaging, indicating that all titanium segments are still electrically connected.

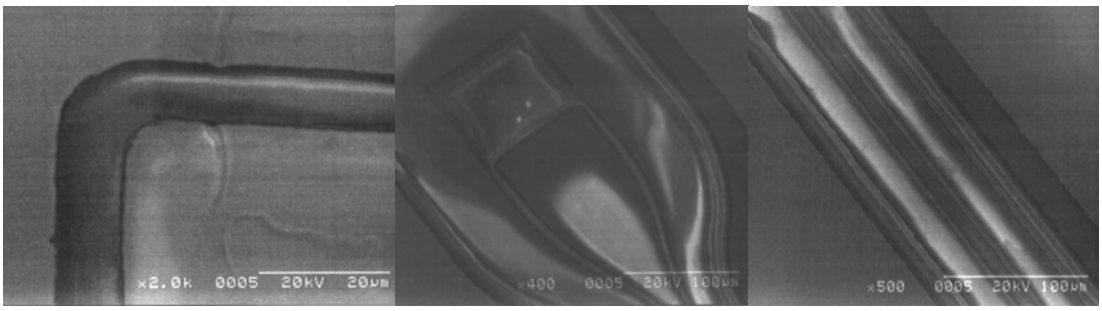


**Figure 4-18 Waveguide structures after top planarization**

The surface of BCB is smooth but protrudes slightly beyond the surface of the titanium, due to the pressure exerted on the surface during the planarization procedure and the BCB's ability to be compressed. The highest point in the BCB was measured ~ 0.5 μm at the center of a 10 μm trench.

### 4.5.2 Backside planarization and electrical interconnects

Once the front surface is planarized, the samples are flipped and mounted upside down. The removal of the backside titanium serves two purposes: completing the waveguide structure and creating through-substrate electrical interconnects. The bottom of the trenches serves as a visual aid for judging the required planarization. Once the trenches become visible after a sufficient amount of titanium has been removed, the lapping process is stopped and the polishing starts, until a desirable surface finish is obtained.

Once the sample passes visual inspection under optical microscope, two methods are used to examine the end point for the process: resistance measurement and inspection under SEM. The resistance measurement is used to test the electrical isolation between different regions of the titanium substrate. The BCB-filled trench isolation produced no measurable current when tested with a HP precision parameter analyzer. For test structures with 15 μm trenches, voltages up to 1000V were applied across the trenches with no measurable sign of breakdown, consistent with the measurement results listed in .

Inspection under SEM not only shows more details of the surface, but allows for a global inspection on the quality of the electrical isolation. In other words, due to the small protrusion of the BCB inside the trenches after the planarization, if electrical isolation is achieved, the titanium region isolated from the ground by the BCB-filled trenches will charge up.

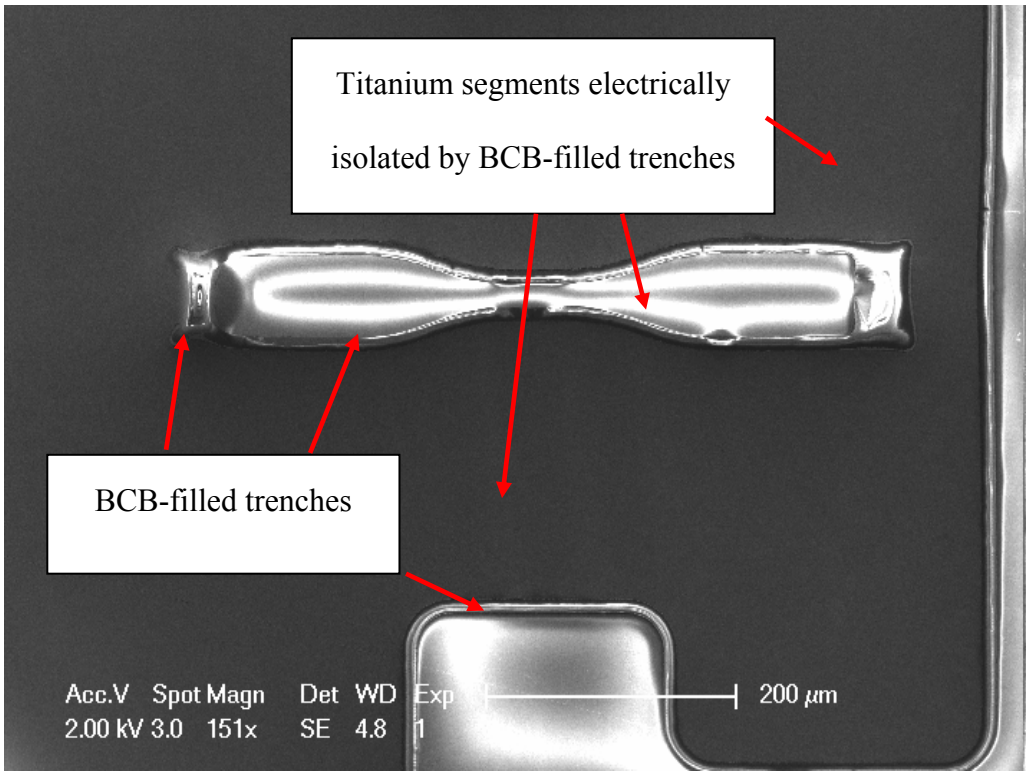


**Figure 4-19 Completed bulk titanium waveguide; Bright areas indicate charging inside SEM**

Figure 4-19 shows a completed bulk titanium waveguide. The titanium regions isolated by the BCB-filled trenches produced charging in the SEM. A close-up view is shown in Figure 4-20. Note the smooth surface finish on both titanium and BCB surface. Some artifacts are due to charging. Figure 4-21 illustrates more waveguide structures with through-wafer electrical interconnect. More close-up views are shown in Figure 4-22.

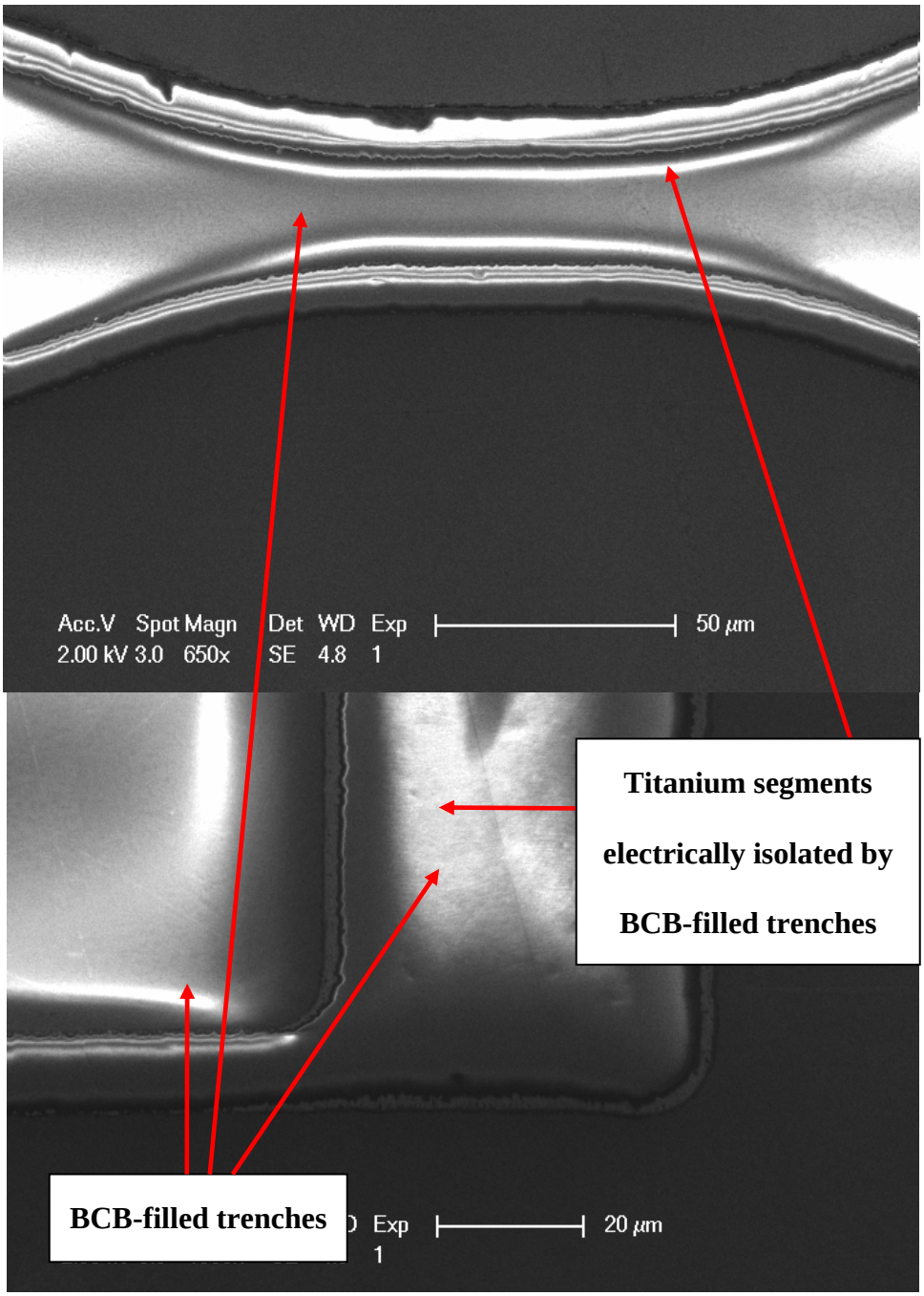


**Figure 4-20 Close-up views of completed bulk titanium waveguides**

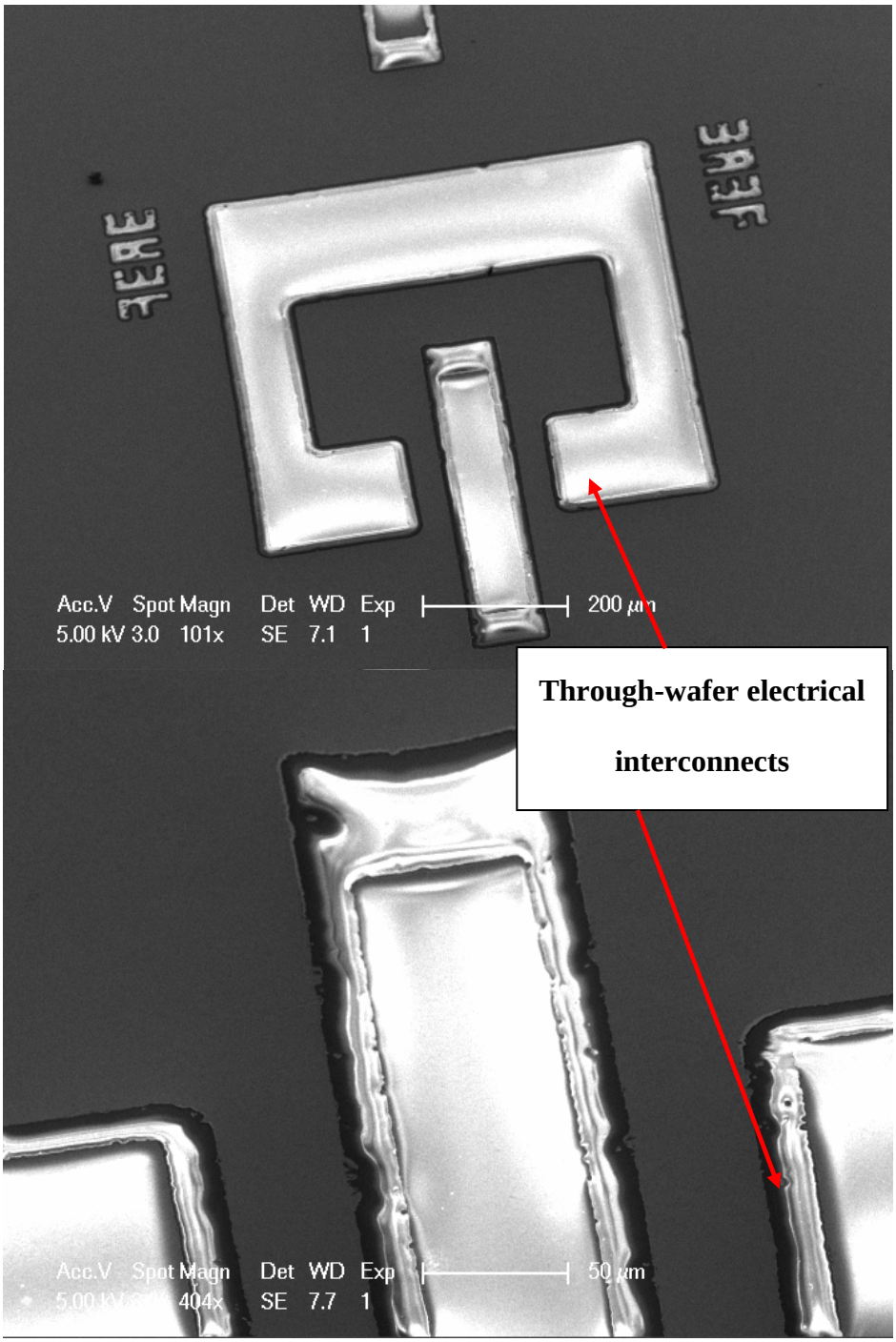


**Figure 4-21 Completed bulk titanium waveguides with through-substrate electrical interconnects**

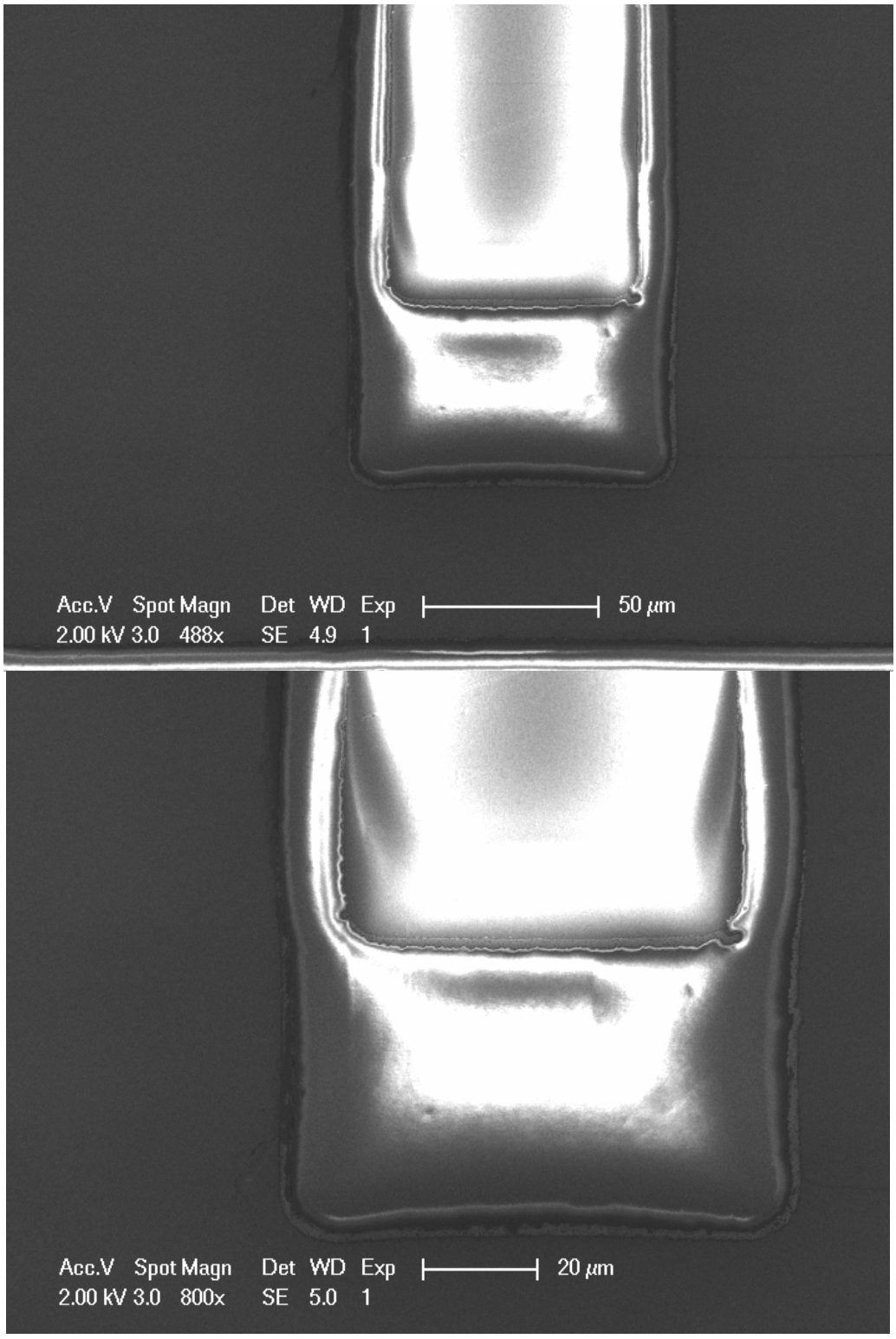


**Figure 4-22 Close-up views of trench-isolation**

Incomplete isolation shows up clearly under SEM (see Figure 4-23). Although an effective way to quickly screen devices for possible electrical isolation failure, this method can sometimes produce inaccurate results due to the limitation of the sample mounting method for the SEM. Devices with questionable isolation need to be further tested electrically. Figure 4-24 shows a set of calibration devices that have been electrically tested to work and yet a few of the devices did not produce charging under SEM.

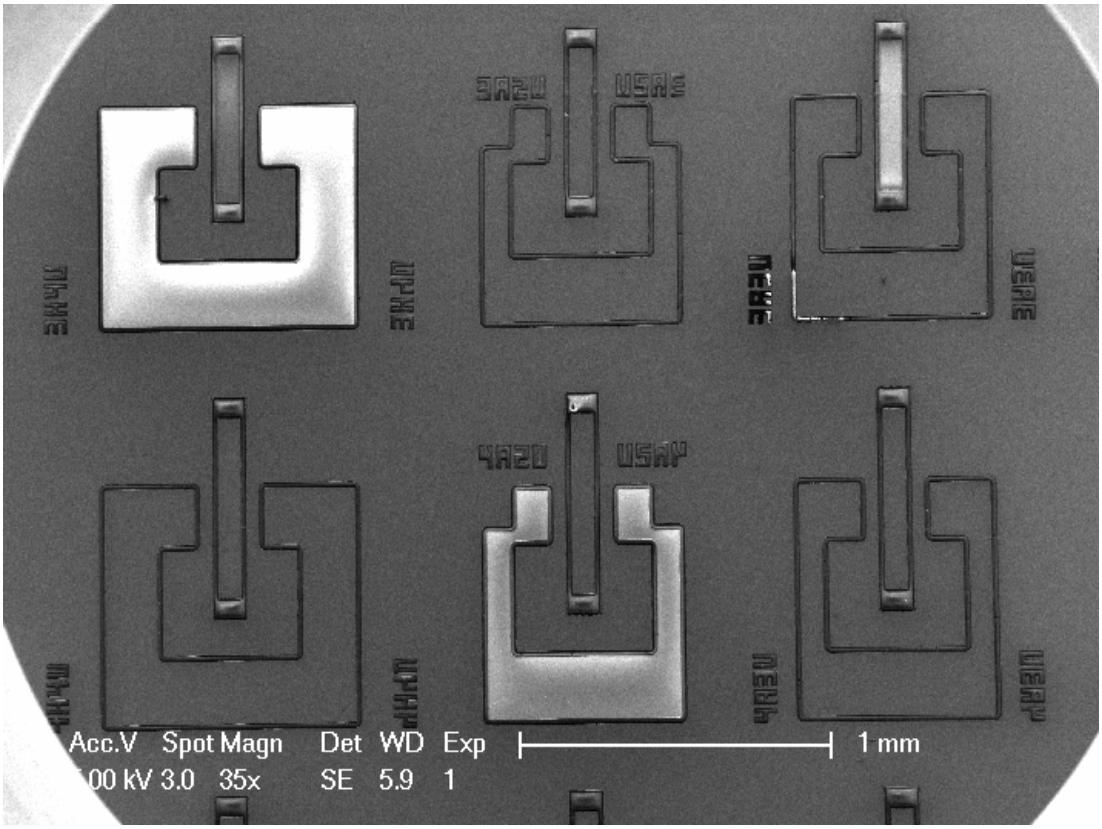


**Figure 4-23 Failed electrical isolation due to insufficient reverse-side planarization**

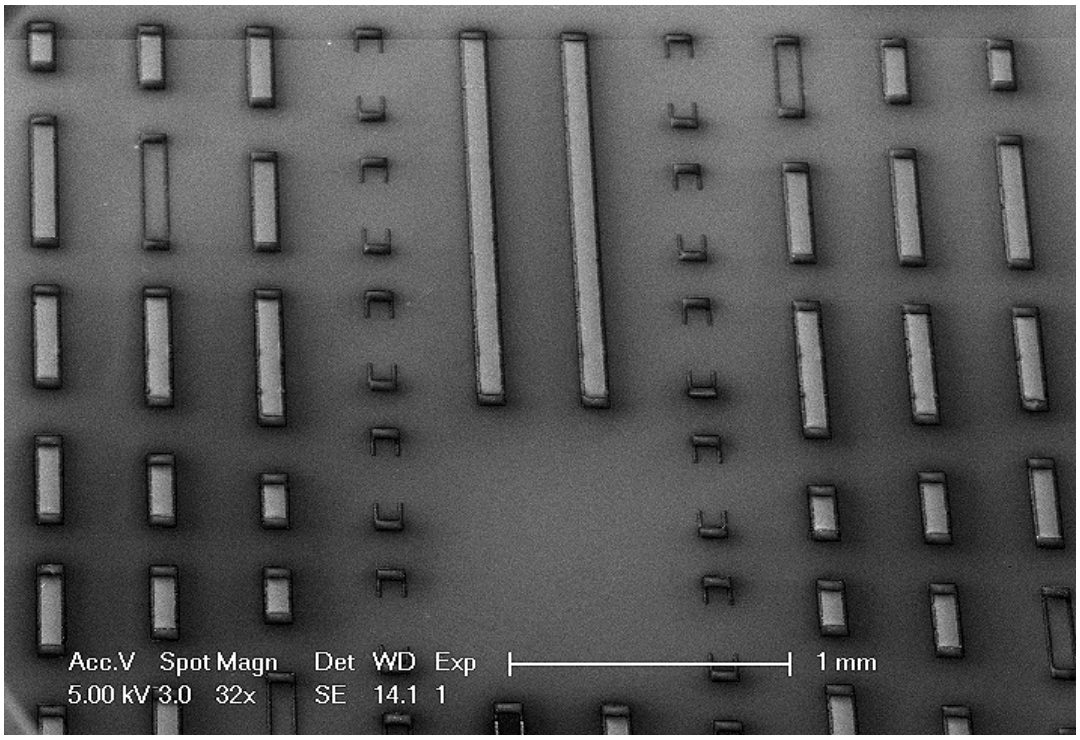


**Figure 4-24 Completed TRL calibration devices; Isolation verified electrically on all devices, although some devices do not charge up under SEM.**

### 4.6 Packaging

The unique construction of the bulk titanium waveguide allows for very compact packages. The superior field confinement and the through-substrate electrical interconnects provide a high packing density, therefore achieving a significantly reduced package size.

The RFMEM package is formed by bonding an etched bulk titanium cavity. Figure 4-26 illustrates cavities that measure 2.2 mm x 1.5 mm x 70 μm in dimensions. We are working on a new generation of devices with package size ~ 800 μm x 600 μm x 70 μm, as shown in the layouts in Figure 4-25.

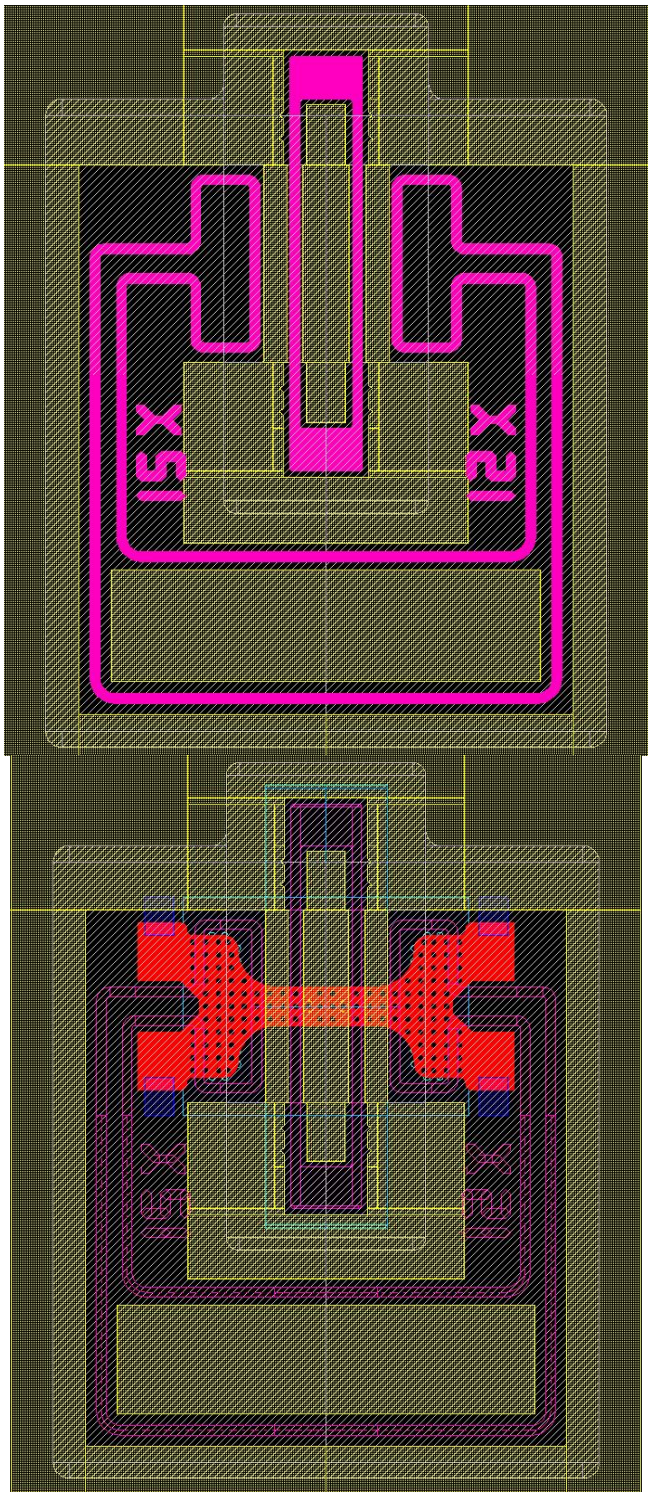


**Figure 4-25 New waveguide design with 800μm x 600μm lateral package dimensions**

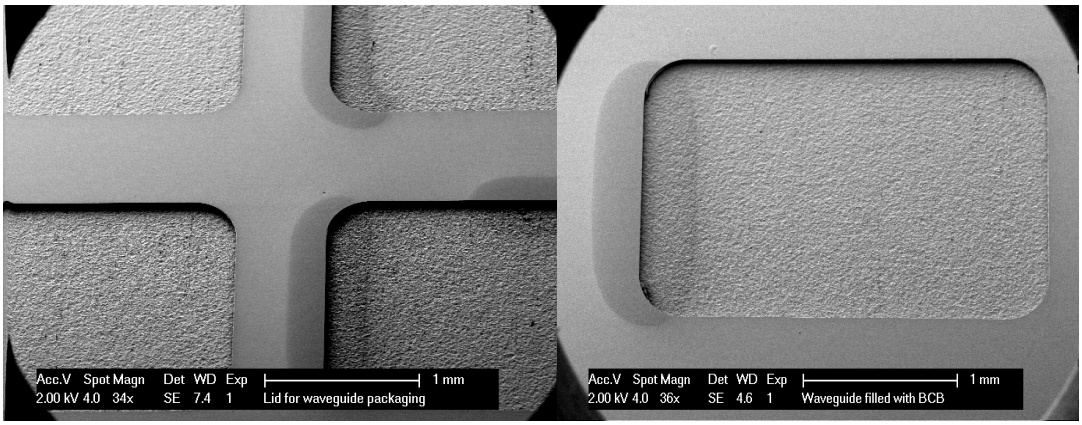


**Figure 4-26 Deep etched bulk titanium cavity for packaging**

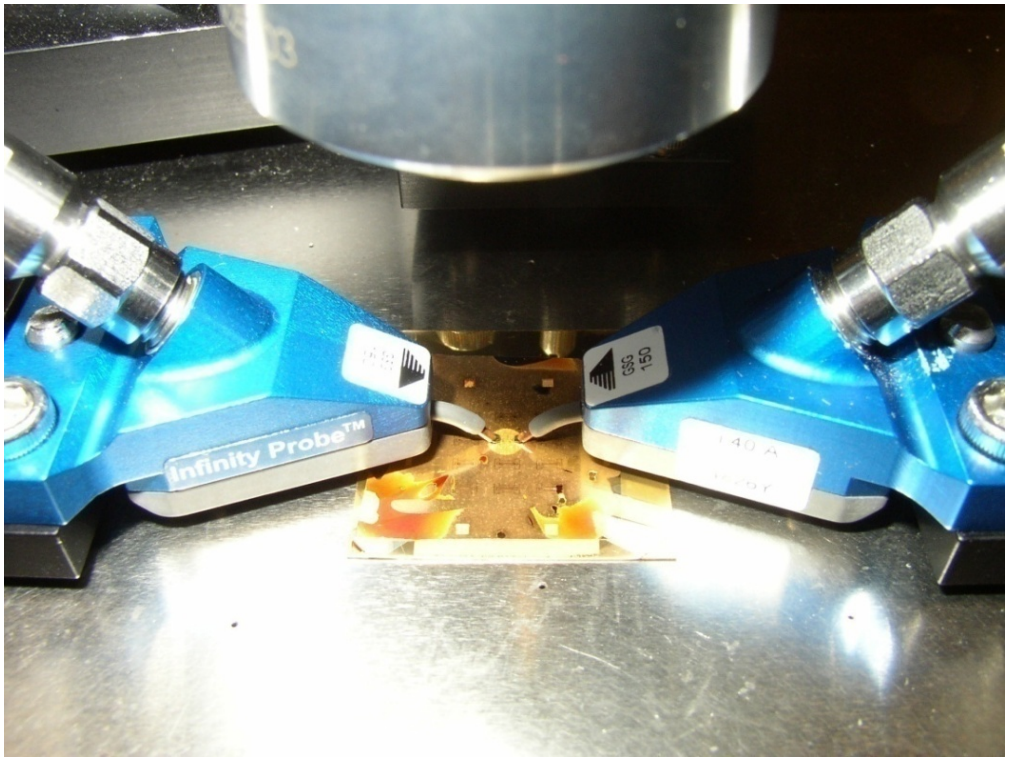


**Figure 4-27 Packaged bulk titanium sample under RF test**

Figure 4-27 shows a packaged waveguide sample under test. The bulk titanium package also provides the substrate for the waveguide.

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# CHAPTER 5

# RF PERFORMANCE OF BULK TITANIUM WAVEGUIDES

## 5.1 RF measurement setup

RF/microwave characterization of waveguides can be done a variety of ways. We choose to use a network analyzer for its accurate internal frequency sweeping signal source and a highly sensitive receiver. Our measurement arrangement, as shown in Figure 5-1, is done with a 2-port setup which monitors the S-parameters of the DUT with a frequency span covering the Ka band (18 GHz to 40 GHz). The approach address the potential applications in satellite communications, radars etc. A low-loss passive in nature, our devices require a great deal of attention in the measurement setup.

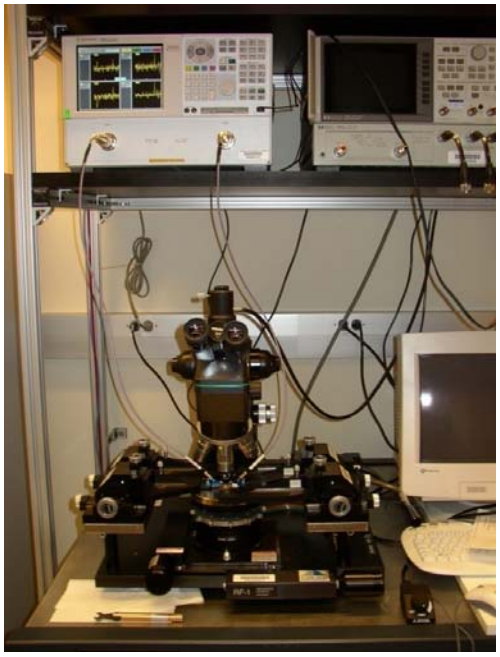

**Figure 5-1 Measurement setup for waveguide characterization**

The network analyzer we use is a Vector Network Analyzer (VNA), model E8363B, by Agilent (Figure 5-2 ). The frequency range is 10 MHz to 40 GHz with a dynamic range of 110 dB and < 0.006 dB trace noise. The nominal power is specified at -12 dBm with a range of -23 to -4 dBm. At 1KHz IF bandwidth, the noise floor is specified <-94 dBm.

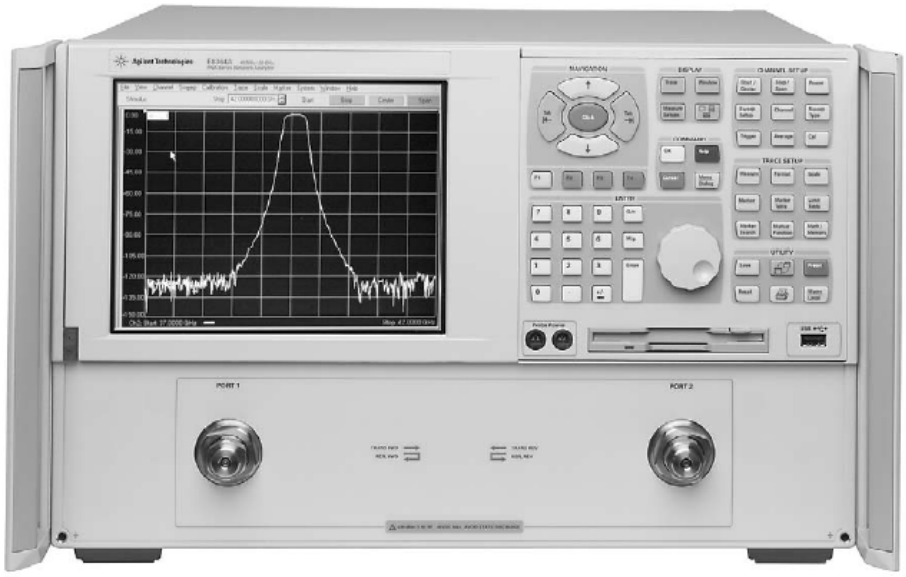

**Figure 5-2 Agilent E8363B network analyzer**

Compared to conventional CPWs, our waveguides have tighter pitches and, sometimes, titanium contact surfaces instead of gold. The more commonly used beryllium copper (BeCu) probe tips do not penetrate the native oxide consistently enough to provide a stable readout to even complete a calibration process. For more consistent contact resistance, we choose "Infinity Probes" (see Figure 5-4) manufactured by Cascade Microtech. The lithographic thin film construction of these

probes reduces crosstalk (specified ~ 30 dB @ 40 GHz) and, most importantly, provides low and stable contact resistance. Originally developed to consistently penetrate the native oxide layer on aluminum and provide and contact resistance as low as 0.05 Ω, and < 0.1 Ω over 100,000 cycles [1]. We discovered that the non-oxidizing nickel alloy tipped probes perform consistently on bare titanium surface. The ~12 μm x 12 μm probe tips are well suited for the fine pitches of our waveguides (see Figure 5-3). The probes are installed onto a Cascade RF-1 probe station (see Figure 5-4).

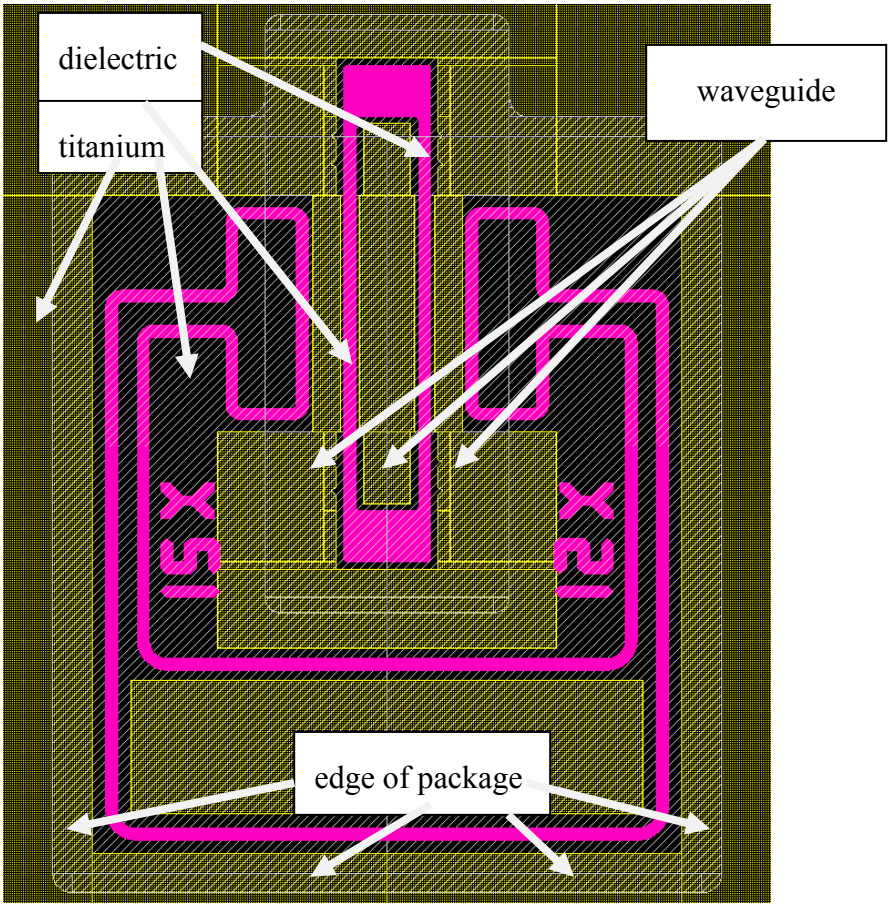


**Figure 5-3 Packaged waveguide layout**

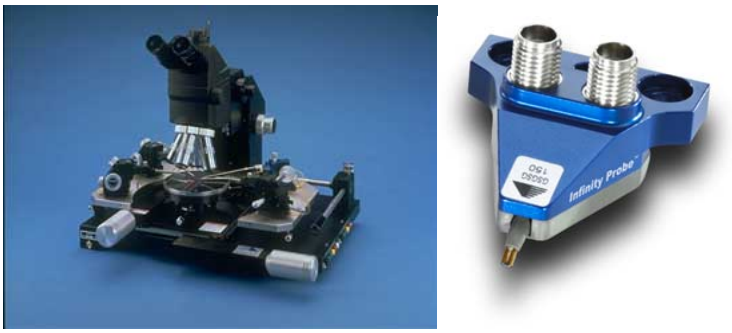


**Figure 5-4 Cascade RF-I probe station (left) and Infinity probe (right)**

Another potential issue that surfaces due to the unique construction of our RF system is the transition loss due to the large variation of electromagnetic field at the interface between the probes and the waveguide. Compared to conventional CPW, where the fields takes on a shape similar to those carried by the CPW tips with similar geometric shapes, the transition in fields is more abrupt and therefore more prune to errors in calibration.

Many calibration procedures exist for microwave frequencies. Short-Open-Load-Thru (SOLT), one of the most commonly used calibration procedures, is not feasible due to the difficulties involved in fabricating broadband 50 Ω on-wafer resistors using our process. Instead, we choose a Thru-Reflect-Line (TRL) calibration procedure. With working frequencies ranging from 10 GHz to 40 GHz, the line standards we use range from 100 μm to 2 mm. Details in the calibration procedure are described in the section 5.3.

The different electromagnetic field distribution in our waveguides means that commercial calibration kits can only be used for calibration to before the probes. Setting the reference planes to beyond the probe contact points is essential in understanding and characterizing the loss behavior due to the waveguide itself and any RF component on top. Commercial calibration substrates are fabricated on ceramic

substrates and the conductor (gold) traces are typically 1-3 μm thick and 100 μm-1000 μm apart, depending impedance and substrate parameters. The aspect ratio (height vs. width) of the gap between conductors for our waveguide much greater, therefore the fields in our waveguides are much more confined and closer to a parallel plate waveguide. The vast difference in field distribution leads inevitably to greater transition loss between the probes and the waveguides. To put the reference planes beyond the contact pads, a custom calibration kit made with the same process, preferably on the same chip, are required. We designed and fabricated a suite of devices following the guideline of TRL calibration (see section 5.3)

The reference plane is set to be around 100 μm from the points of probe contact. Alignment marks (notches, see Figure 5-5) are defined in a gold layer to help keep the sliding distance of the probes consistent and around 25 μm, thereby minimizing errors due to distance variations from the probe to the reference plane.

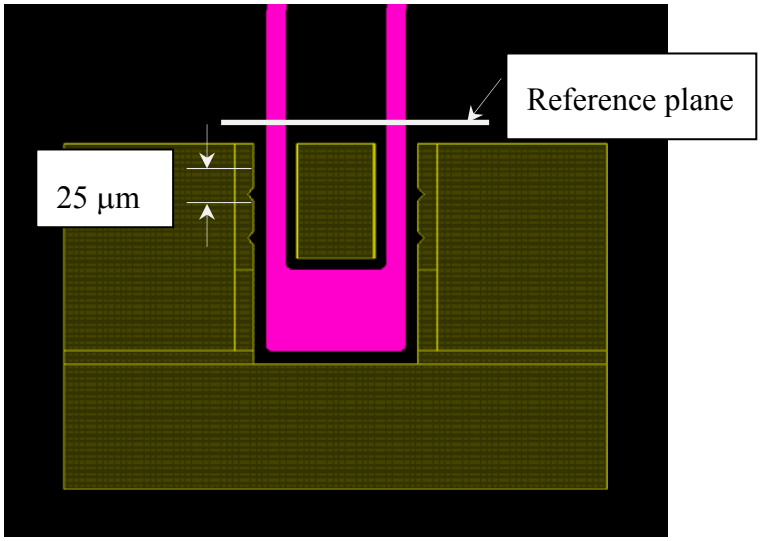


**Figure 5-5 Design of probing area of waveguide**

## 5.2 Waveguide design

One of the most important aspects of constructing a RF system is the understanding of its basic transmission line/waveguide structures. The electromagnetic waves propagating along the waveguides can exhibit undesirable behaviors if the waveguides are not designed properly. Some of the most common issues include scattering, return loss, unwanted radiation, and undesirable parasitic. With conventional planar waveguides such as microstrip and CPW, a large gap between adjacent devices/structures is often required, to reduce unwanted coupling at the cost of chip area. The unique construction of bulk titanium waveguide offers superior field confinement, therefore reducing loss due to parasitic coupling. The key parameters determining the characteristics of the waveguide include trench dimensions (both width and height), trench separation, or the width of the middle conductor, choice of dielectrics, and sidewall enhancement.

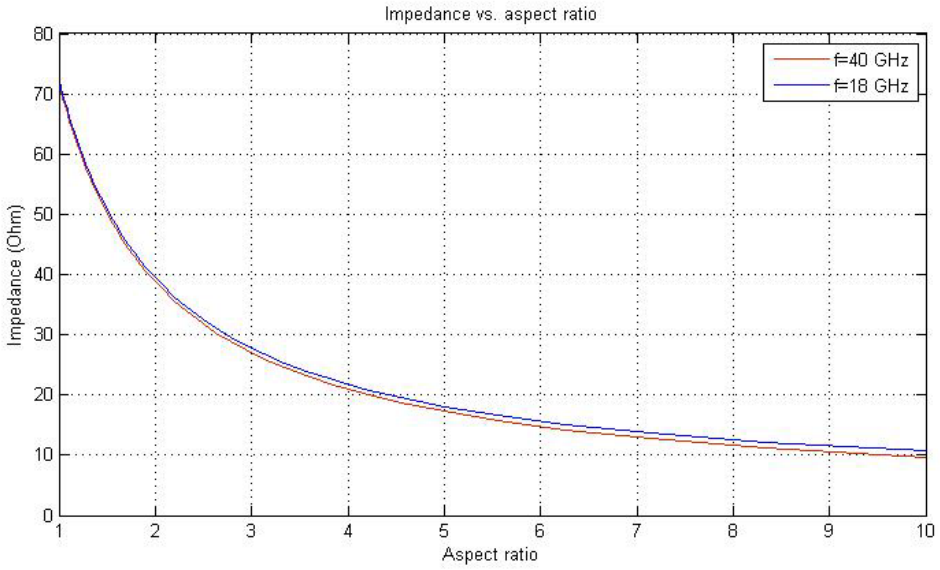


**Figure 5-6 Impedance vs. aspect ratio (h=50 μm, W=30 μm)**

The impedance of the waveguide is primarily determined by the aspect ratio of the trench (see Figure 5-6, calculated from Equation (2.37)), due to the parallel-plate-like field distributions. The finite fringe field, however, does impact the impedance, therefore W, the width of the middle conductor plays a slight role in impedance also (see Equation (2.37)). As shown in Figure 5-7, the impedance varies from ~25.0 Ω for W=15 μm to ~23.8 Ω for W=100 μm, or a ~4.8% change. This shows that, unlike traditional CPW, the impedance of the bulk titanium waveguide is nearly independent of the center conductor width.

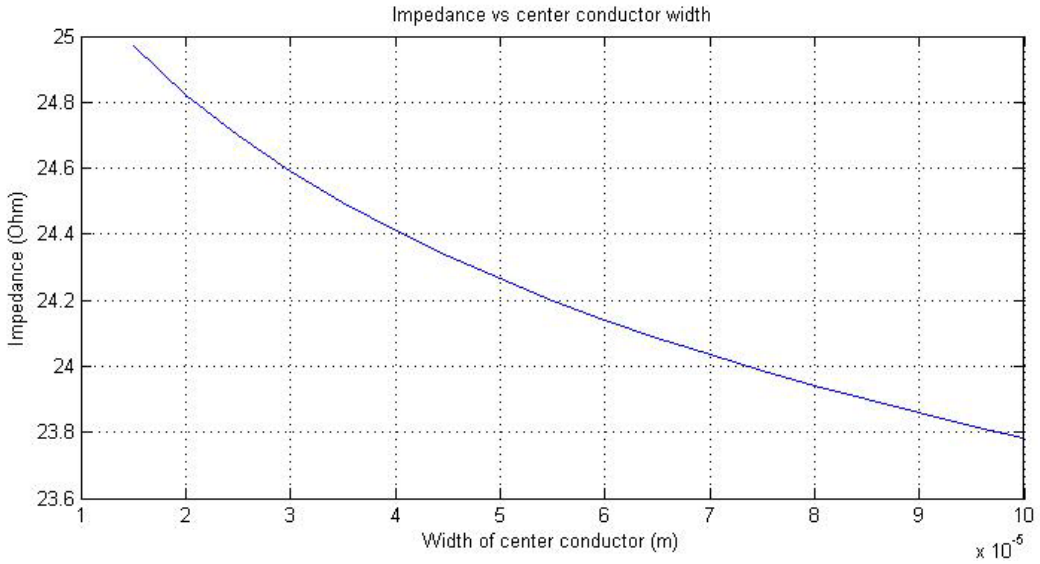


**Figure 5-7 Impedance @ 40GHz vs. center conductor width**

Figure 5-8 shows the frequency dependency of the impedance calculated by Equation (2.37) for waveguide dimensions W=30 μm, S=15 μm, and h=50 μm at the frequency range of the measurements. The monotonic drop in impedance with increasing frequency results from the drop in internal inductance. At 40 GHz, the impedance is projected to be ~24.6 Ω̃.

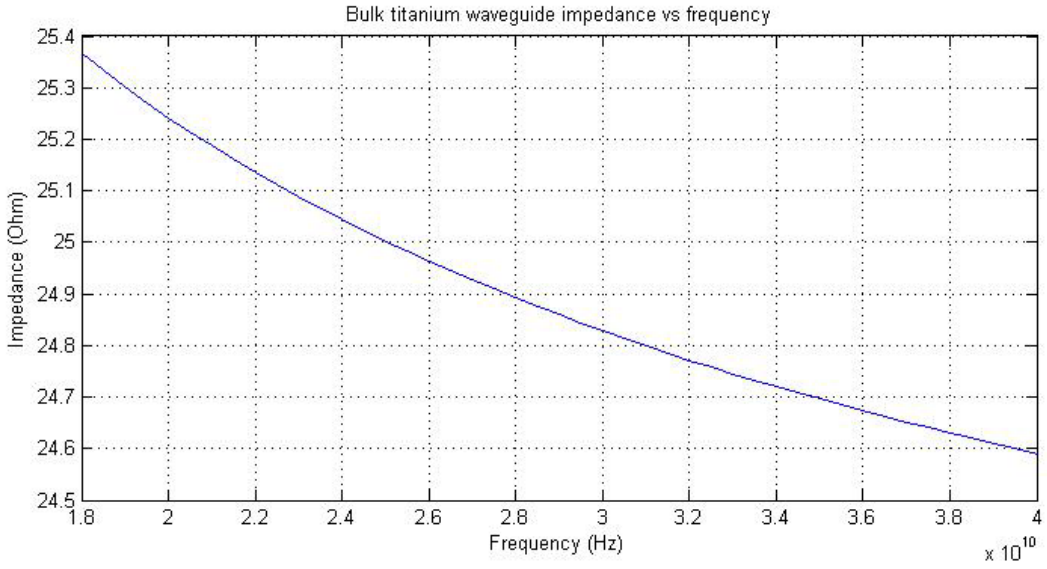


**Figure 5-8 Modeled bulk titanium waveguide impedance**

Have gold on sidewall of trenches reduces conductor loss, as well as field penetration, therefore reduces internal inductance, and total impedance, as shown in Figure 5-9.

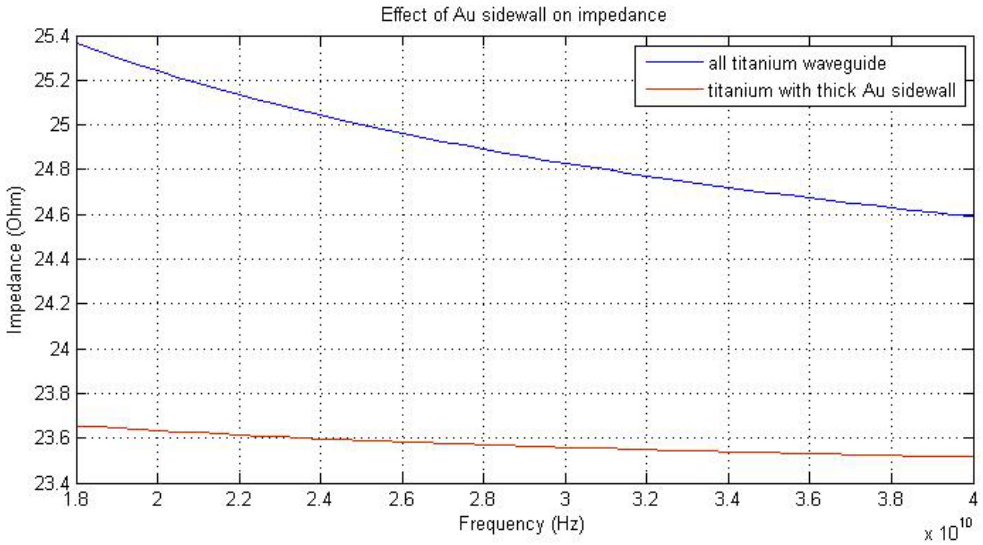


**Figure 5-9 Effect of Au sidewall on impedance**

As a topologically new waveguide/transmission line, it is important to outline a set of design rules. Table 5-1 outlines the key design rules with brief explanations.

**Table 5-1 Design rules for bulk titanium waveguides**

| Design features | Design rules | Notes |
|---|---|---|
| Trench width | 10-20 μm; consistent width for entire chip/wafer | Limited by etching characteristics such as loading effects, sidewall verticality and roughness. |
| Trench depth | 30-100 μm; identical to waveguide height; variation measured < 2 μm for 2.5 cm x 2.5 cm chip area | Limited by maximum etch depth and loading effect; greater depth strengthens sample chip but lowers waveguide impedance. |
| Middle conductor width | >2x trench width; typical range: 30-100 μm; size determines choice of probes | Too small a width causes field leakage between trenches and lowers impedance due to coupling |
| Waveguide separation | >4x trench width | Too small a separation causes parasitic coupling between waveguides |
| Waveguide length | Limited by chip/wafer dimensions | Scattering in very long waveguides is likely, due to etch/sidewall film defects and chip/wafer height variations |
| Distance between adjacent trenches | >trench width | Limited by etch anisotropy and loading effect |
| Package cavity dimensions | laterally, >2x trench width from the outmost edge of field concentrated features; vertically, >3x trench width | Sufficient separation from field concentrated feature helps minimize parasitic coupling to package |

## 5.3 RF calibration

The physical quantities a VNA measures directly are the vector ratios of the reflected or transmitted energy to the energy incident upon the DUT. However, any measurement setup involves components such as cables and connectors between the VNA and the DUT. Signal scattering due to mismatched impedances can alter the measured results. Even with perfectly matched impedances, the variations in the mode shapes of the electromagnetic fields, caused by the topological differences in different parts of the RF circuit, produce transition losses in the form of reflections and radiations. As a result, the measured signals are convoluted by numerous contributions of unknown amounts. This problem can be solved by calibration, which takes advantage of the knowledge that the unknown contributions can be made highly consistent and that the waveguides used by the DUTs are usually of known – and well behaving -- characteristics. Through a series of standardized steps, the information about the DUTs can be de-embedded from the convoluted signals.

Figure 5-10 shows the schematic of the calibration setup for the bulk titanium waveguides. We choose a TRL calibration procedure, due to its suitability to measuring low-loss passive DUTs, as well as the complexity involved in making on-wafer resistors. The detail derivation of the de-embedding procedure is listed in Appendix C.

The effects of the various RF/microwave reflections/discontinuities can be represented by hypothetical virtual networks that interface the network analyzer to the DUT. The measurements of the known standards determine the scattering parameters of these virtual networks. The true scattering parameters of the DUT can then be calculated by stripping the error networks from the measured responses of the DUT.

Calibration techniques differ primarily in the choices of standards and their corresponding error models.

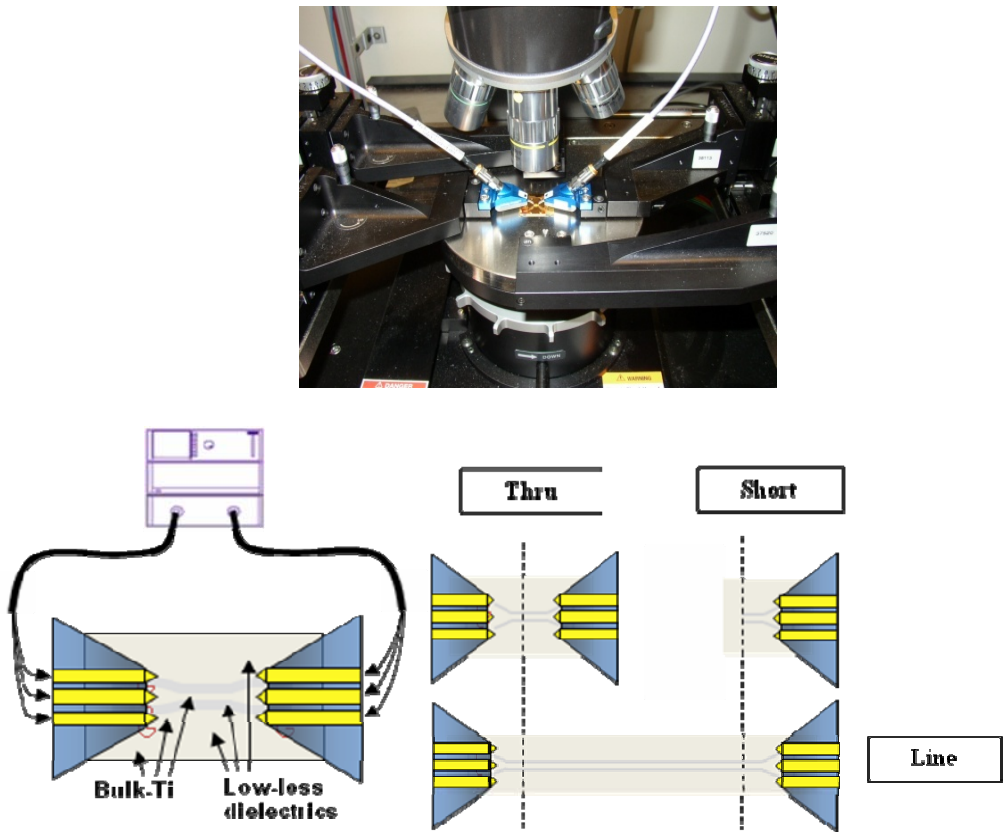


**Figure 5-10 measurement schematic**

TRL is an accurate calibration technique suited for low loss passives at elevated frequencies [2]. TRL standards include Thru, Reflection and Line. Thru represents a standard with zero length beyond the reference planes, in other words, the two reference planes for the two port measurement overlap. Reflection can be either a short or open, where all the signal energy gets reflected. Line contains standards of various lengths, determined by the frequency range for the application.

TRL calibration is extremely accurate, in most cases more accurate than an SOLT calibration [3]. Another advantage of TRL calibration is that the TRL standards need not be defined as completely and accurately as the SOLT standards. While SOLT standards are completely characterized and stored as the standard definition, TRL standards are modeled, and not completely characterized. However, TRL cal accuracy is directly proportional to the quality and repeatability of the TRL standards. Physical discontinuities, such as bends in the transmission lines and beads in coaxial structures, will degrade the TRL calibration. The connectors must be clean and allow repeatable connections.

Figure 5-11 shows the design of the calibration standards. The reference plane is set at ~25 μm from the contact points of the probes (see Figure 5-5). The design of the standards is illustrated in Figure 5-12: the reflect standard is realized with the waveguide trench ending at the reference plane and shorted to the substrate; the line standards are waveguides of difference lengths, measured from the reference planes; the thru standard is a line with the length of the waveguides set to zero, or, when the reference planes at both ends of the waveguide meet.

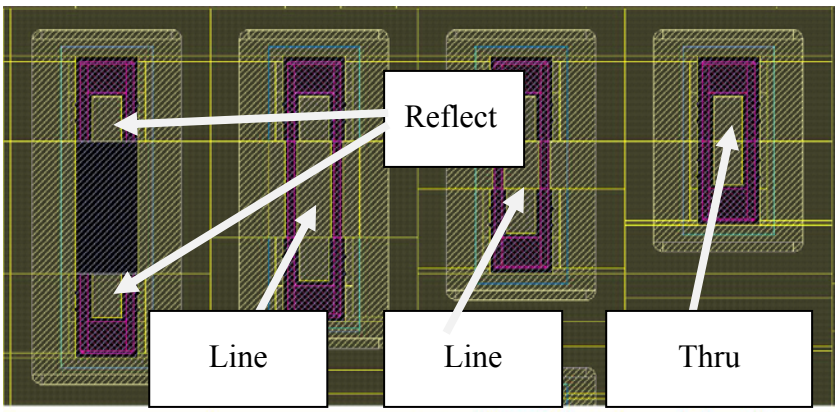


**Figure 5-11 Zoomed-in view of calibration standards**

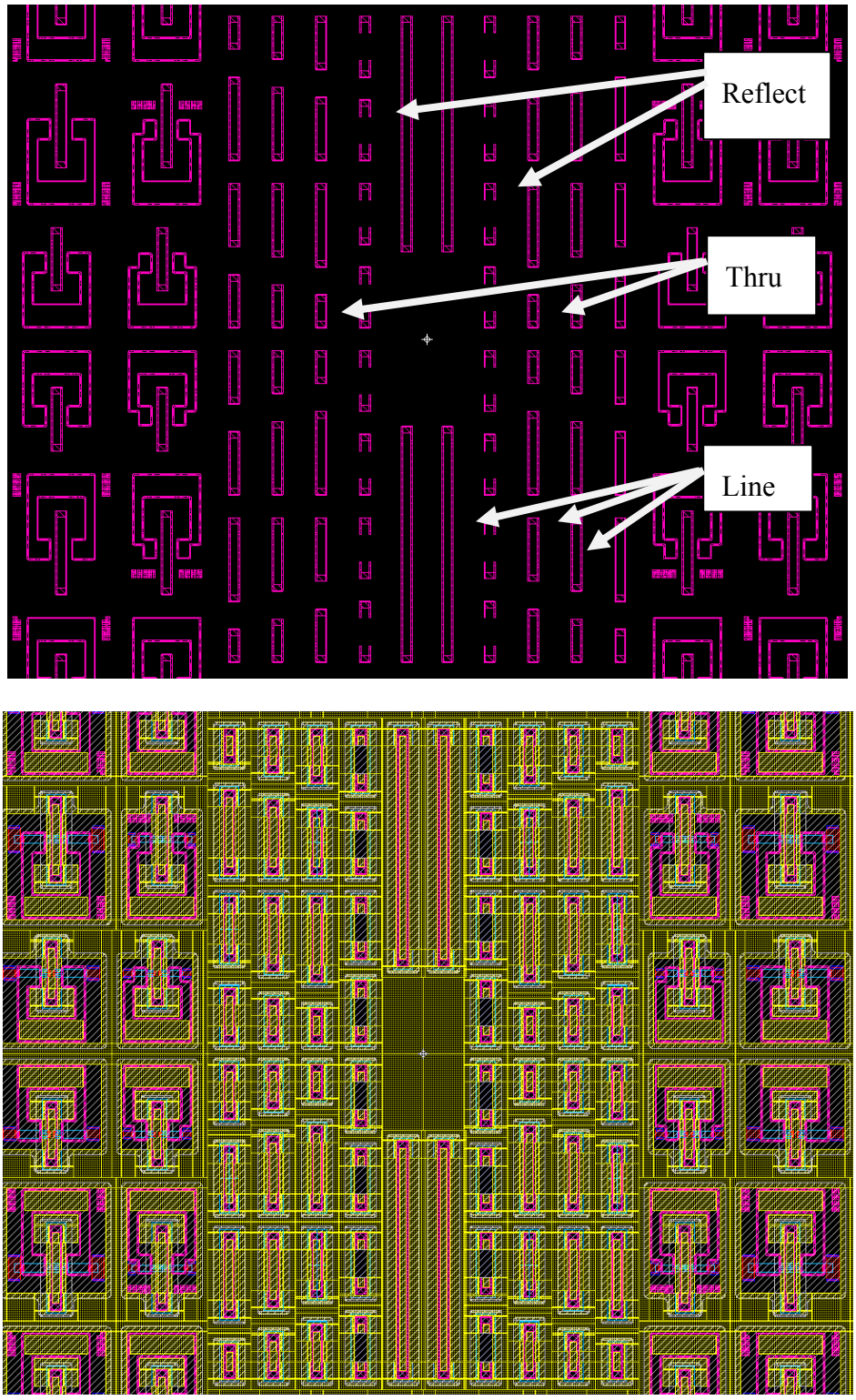


**Figure 5-12 On-chip TRL calibration standards design. Top: trench layer; bottom: all layers**

### 5.4 Measurement/calibration errors:

For low-loss passive components at higher frequencies such as the Ka band, the measured data often contains noise and errors that can be of similar amplitudes compared to the signals. The errors come from many sources. Random errors are often associated with equipment and processing variations. For instance, the contact resistance and the exact location of the probe contacts vary from run to run and the variations become escalated when sample inconsistencies from processing. Human errors also play a role, due to the large number of process steps that are newly developed. Systematic errors can be mostly attributed to equipment inaccuracies from sources such as the network analyzers, the cable and connector setup and, very importantly, calibration errors, especially since the bulk titanium waveguide has a 3-D geometry different from conventional CPW and microstrip.

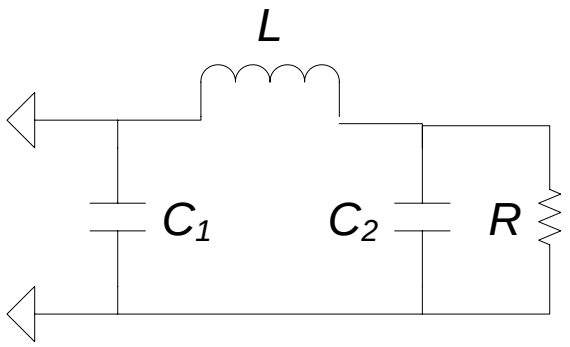


**Figure 5-13 Lumped model for calibration standards**

The algorism used in PNAs used for TRL calibrations [4], simplifies the de-embedding process by using a lumped element model such as shown in Figure 5-13, which uses a series inductance to simulate the effects of current transition from the

probes onto the calibration standards. The simplification of simulating the effect due to discontinuities with a 2, 3-parameter polynomial can lead to more discrepancies in our measurements due to the different topology of the bulk titanium waveguide. More accurate analyses may be obtained based on raw measurement data and a more sophisticated circuit model [5].

Calibration errors can come from many sources: inconsistent probing, both in contact resistance and probing locations; fabrication imperfections, including imprecise dimensions, asymmetries and unexpected scattering centers, such as etch grass and roughness; errors in polynomial model for standards [6]. These errors can lead to measurement inaccuracies. As a pioneering work, our effort has been focused on proof of concept and within-an-order-of-a-magnitude demonstration and verification of theoretical modeling, simulation and the performance advantages brought forth by the novel 3-D construction of the RF system.

For low-loss passive measurements at high frequencies, the inaccuracies from the calibration can be of the same order of magnitude as or exceed the loss.

### 5.5 RF simulation

For relatively complicated or most real world applications, quasi-static analyses as performed in Chapter 2 can only provide theoretical guidance. More quantitative performance estimations require full-wave analyses with 3-D electromagnetic field simulations, such as HFSS by Ansoft Inc. As the industrial standard for RF/microwave EM field solver, HFSS utilizes a Finite Element Method (FEM) to compute the electrical behavior of high speed components and is the tool we use for system design and verification. Understanding the parameter settings for HFSS is

essential to obtaining accurate simulation results. A typical set of simulation parameters is listed in Table 5-2.

**Table 5-2 Typical analysis parameters for HFSS simulation**

| | | |
|---|---|---|
| Convergence factor (delta S) | 0.002 | Program default: 0.02 |
| Boundary | Radiation at surfaces not overlapping with excitation ports | 10X beyond device (cross-sectional) dimensions |
| Excitation ports | Wave ports | Lump ports also used with similar results |
| Pass requirement | 10 passes minimum; 30 passes maximum; 3 passes after convergence | |

The convergence factor determines the accuracy of the simulation. HFSS uses a self-adaptive mesh which adjusts itself according to the convergence error. To ensure consistency with experiment, the total volume is chosen to be at least 10X of the largest dimensions of the device cross-section with a radiation boundary assigned to the outer edge. Two types of excitations were used: “wave ports” and “lump ports”. Wave ports, or, external ports, which assume an infinite extension of the cross-section, are used to determine the transmission characteristics of the waveguide. Lump ports,

which are embedded within the volume being simulated, enable simulations of more complex inputs and are also used to analyze the parasitic effects of the waveguide ends. The transmission characteristics of the waveguide obtained from lump port simulations are comparable to those obtained by wave port simulations. To minimize random errors, the simulations are set to complete at least 10 passes and 3 after convergence factor is reached.

### 5.5.1 HFSS model

Figure 5-14 shows a model used for the characterization of an unpackaged, straight titanium waveguide. Figure 5-15 shows the mesh after adaptive refinement on one of the excitation ports. The material properties are listed as follows:

**Table 5-3 Material properties used in HFSS simulations**

| Material name | Relative permittivity | Relative permeability | Bulk conductivity (siemens) | Loss tangent |
|---|---|---|---|---|
| BCB | 2.5 | 1 | 1.0e-17 | 0.002 |
| Titanium | 1 | 1.00018 | 2.34e06 | N/A |
| Gold | 1 | 0.99996 | 4.71e07 | N/A |

Note that both the loss tangent and relative permittivity are frequency dependent but they are nearly invariant [7] for the frequency range of our measurement.

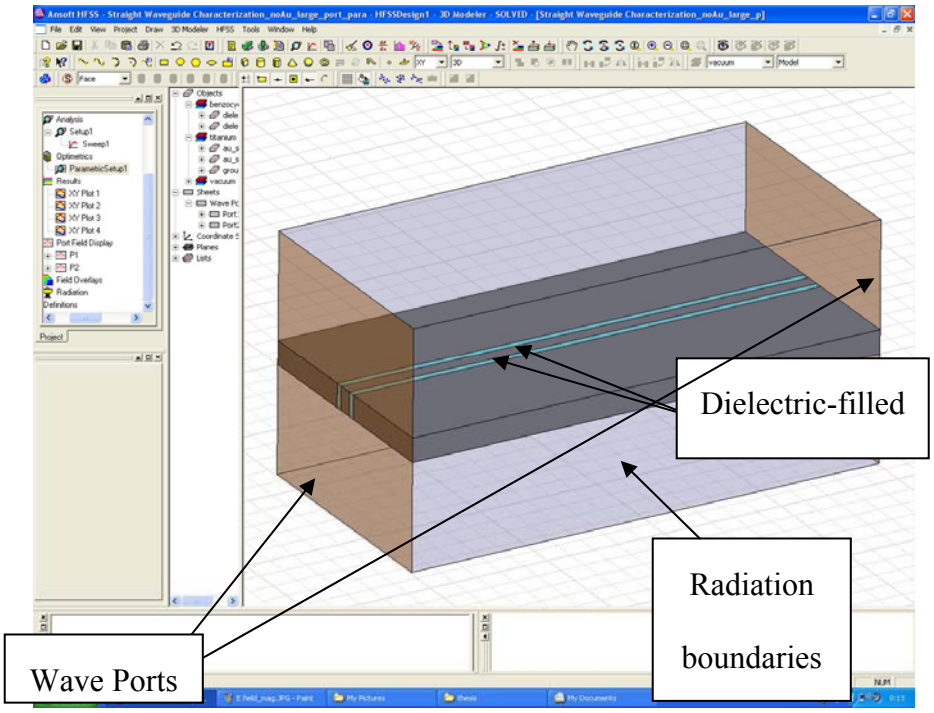


**Figure 5-14 3D model for waveguide simulations**

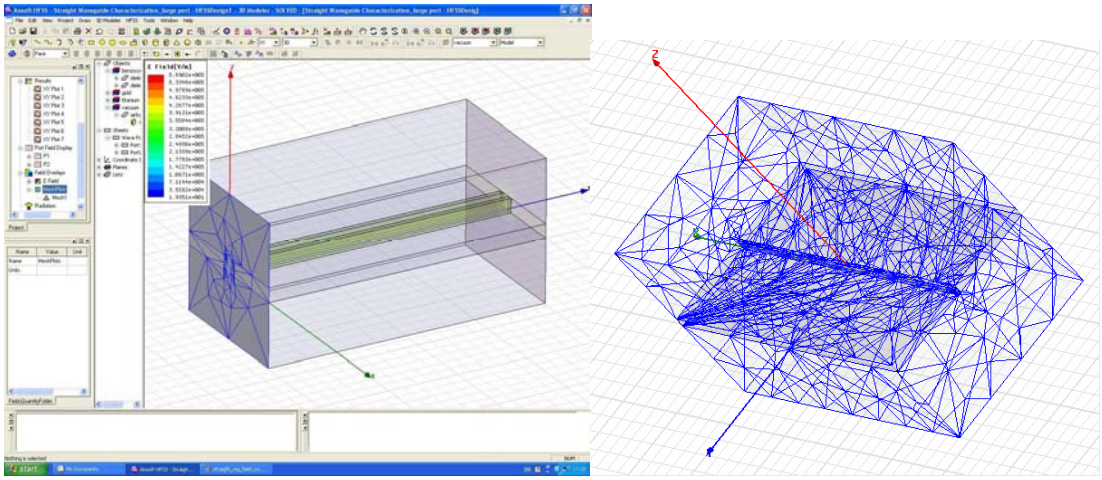

**Figure 5-15 Mesh model for bulk titanium waveguide simulation**

Field confinement is demonstrated in Figure 5-16 and Figure 5-17. Note that, although not shown in the plot, due to a known display artifact, fields are solved inside

the conductors as well. As indicated by the simulated results at the port, the field intensity drops by an order of a magnitude beyond a distance ~ 2 x gap, in all directions away from the signal carrying dielectric-filled trenches.

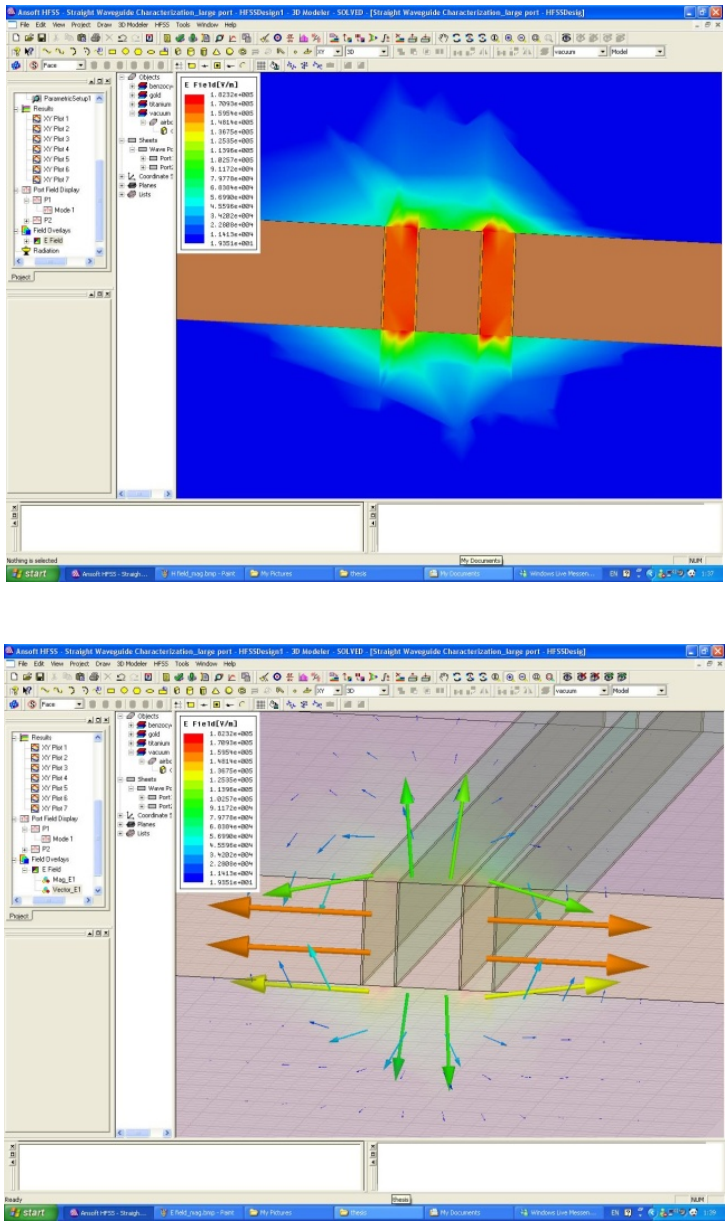

**Figure 5-16 Magnitude and direction of electric field at cross section**

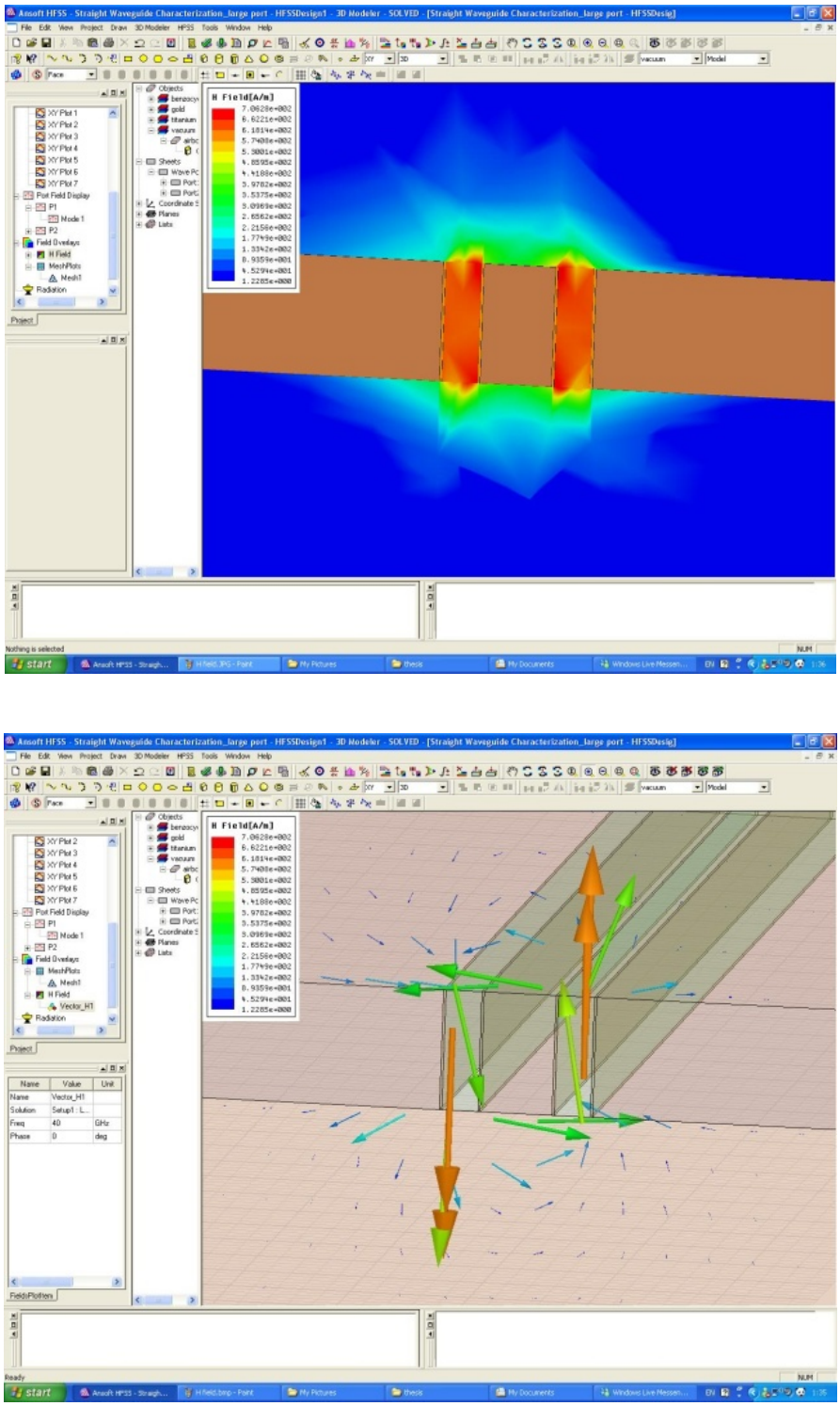


**Figure 5-17 Magnitude and direction of magnetic field at cross section**

### 5.5.2 Impedance characterization

Having an accurate impedance value is vital for setting up TRL calibrations. At high frequencies, to the first order, the impedance of the waveguide is determined by the aspect ratio, as well as the permittivity of the trench-filling dielectric, and is independent of the frequency (Equation (2.25)). At low frequencies, the skin depth increases and the distributed series resistance decreases. However, the overall magnitude of the impedance increases with a lower frequency, due to the larger contribution from the internal inductance Eq. (2.37). This behavior is verified with HFSS and compared to the theoretical models in Figure 5-18.

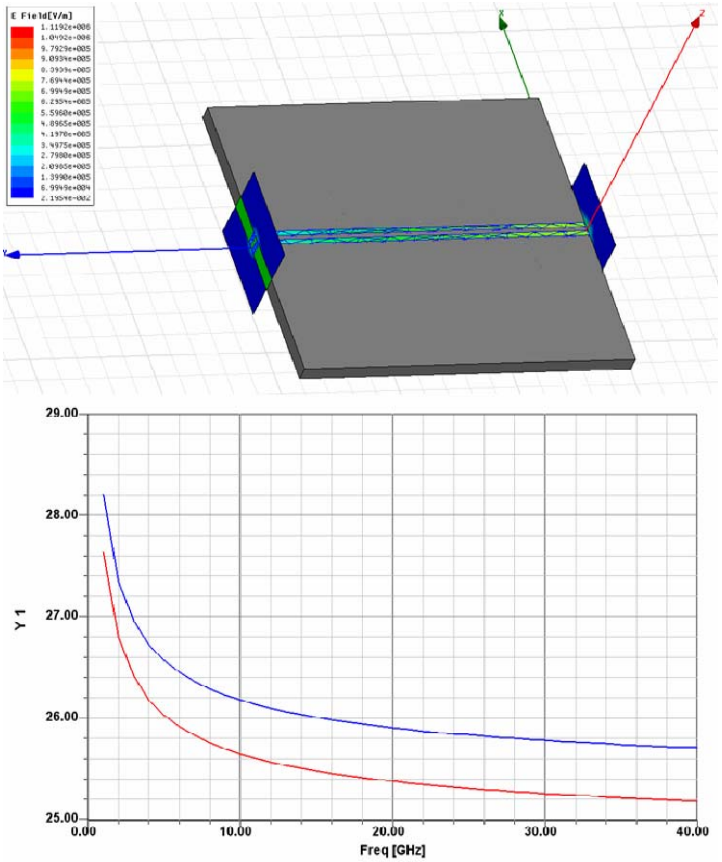


**Figure 5-18 Impedance characterization**

## 5.6 Loss characterization

The most common term for evaluating the lossiness of 2-port waveguides is Insertion Loss (IL), $S_{21}$, which is defined as the ratio between the output and input powers:

$$S_{21} \equiv \frac{P_{out}}{P_{in}} = \left|\frac{V_{out}}{V_{in}}\right|^2 = \frac{e^{-2\alpha l}}{1+e^{-2\alpha l}} \approx e^{-2\alpha l}, \tag{5.1}$$

where $P_{out}$ and $P_{in}$ are the input and out put powers, respectively; $\alpha$ is the loss factor, or the real part of the propagation constant; l is the length of the waveguide. Insertion loss is customarily evaluated in log scale:

$$IL(dB) = 10*\log(S_{21}) \approx -20\alpha l \tag{5.2}$$

The loss can be attributed to multiple sources: reflection, radiation, and resistive losses.

Return Loss (RL) represents the energy that gets reflected back to the source. Assuming

$$RL \equiv 10*\log(S_{11}) = 10*\log(\frac{P_{refl}}{P_{in}}) = 20*\log(\left|\frac{V_{refl}}{V_{in}}\right|) \tag{5.3}$$

RL is a direct measure on the success of the calibration, as a perfect calibration procedure eliminates the reflections to the test ports. Figure 5-19 shows a typical measured return loss for a well-calibrated system, where the RL reaches a maximum of ~38 dB at 40 GHz.

Neglecting the reflection loss, the total insertion loss, $\alpha_{tot}$, of a waveguide can be written as:

$$\alpha_{tot} = \alpha_{cond} + \alpha_{diel} + \alpha_{rad}, \tag{5.4}$$

where $\alpha_{cond}$ , $\alpha_{diel}$, $\alpha_{rad}$ represent the losses due to the finite conductivity of the conductors, the resistive loss of the dielectric media, and radiation, respectively.

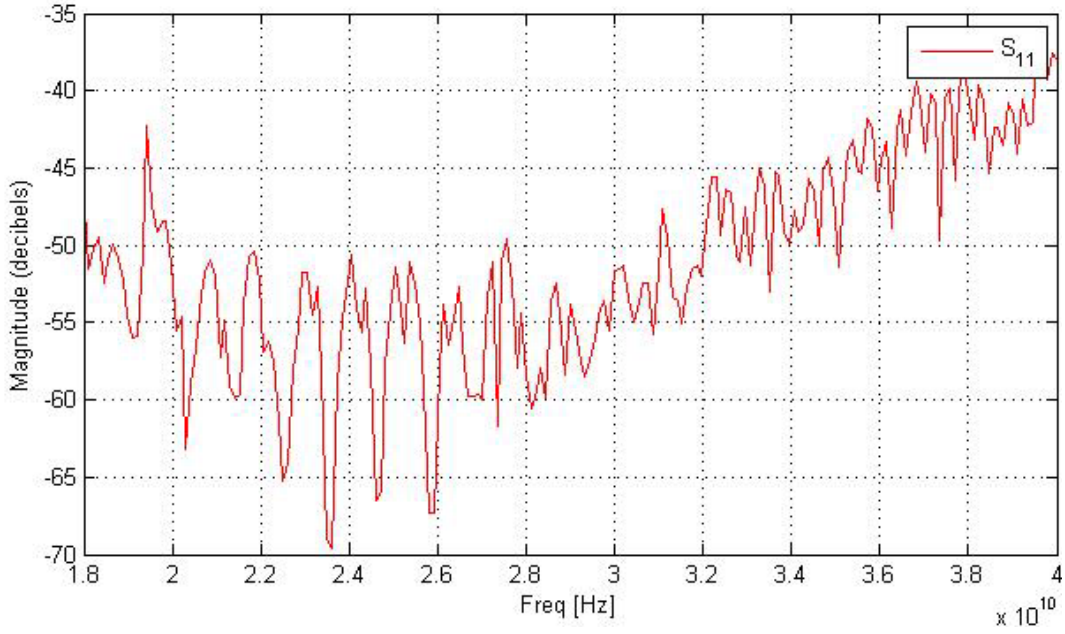


**Figure5-19 Return loss of a packaged 400 μm waveguide**

Radiation loss is primarily determined by mode coupling. When the primary transmitted mode has similar frequencies as a parasitic mode, the mode shapes are similar, and their fields overlap, significant loss due to radiation occurs. For traditional CPWs, the parasitic mode primarily responsible for radiation loss is the TM mode of the dielectric slab beneath the conductors, as well as the resonant modes of the cavity created by metal packages.

In the case of bulk titanium waveguide, Due to the absence of a large bulk of dielectric, the dominant parasitic mode is the package cavity mode. Since the fields are mostly confined within the gaps, as shown in Figures 5-16 and Figure 5-17, the overlap with cavity modes is less and the metal package can be of narrower dimensions, therefore increasing the frequency of the 1st cut-off frequency. (see Equation (5.7))

The insertion loss of the bulk titanium waveguides are measured and compared to Eq. (2.46) in Figure 5-20. The lowest percentage difference between experiment and theory, at 18 GHz, is ~ 18.8%; the highest difference, measured ~ 22.3%, occurs at 40 GHz.

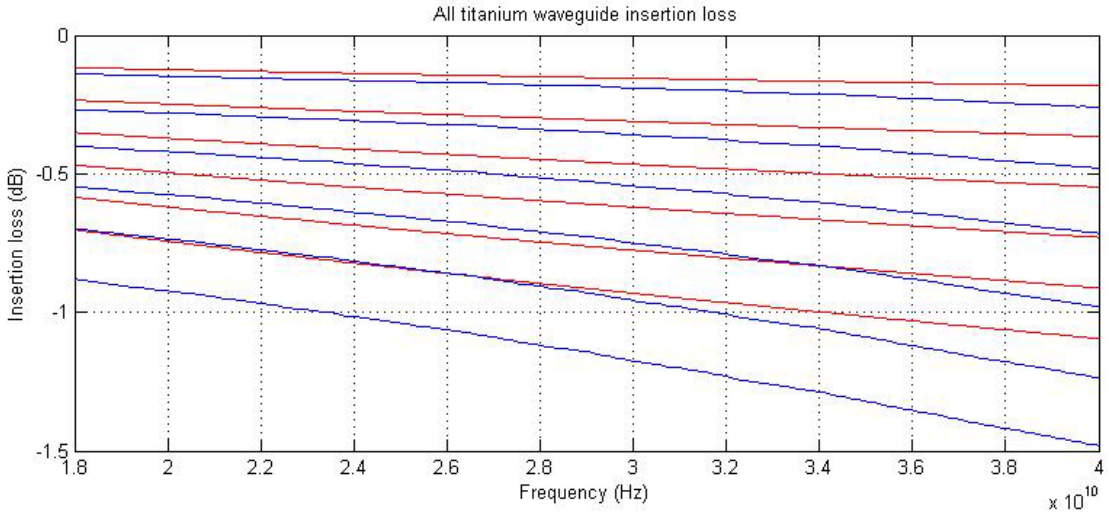


**Figure 5-20 Insertion loss of all-titanium waveguides. Red curves: theory; blue curves: experiment. Top to bottom: 100 m to 600 m with 100 m increments**

The total loss at the target frequency range, as shown in Chapter 2, is dominated by the conductor loss. A layer of gold coated on the sidewall, therefore, offers a direct solution to loss reduction. To obtain a sufficient thickness, so that the fields do not penetrate into the underlying titanium, a thickness of ~1 to 2 x skin depth is needed. As shown in Figure 5-21, the skin depth in gold is ~0.5 μm at 18 GHz and ~ 0.4 μm at 40 GHz.

A 1 μm of gold is deposited and it generates a considerable drop in insertion loss (Figure 5-22). The insertion loss at 40 GHz for a 100 μm waveguide drops from ~ 0.22 dB to ~ 0.077 dB.

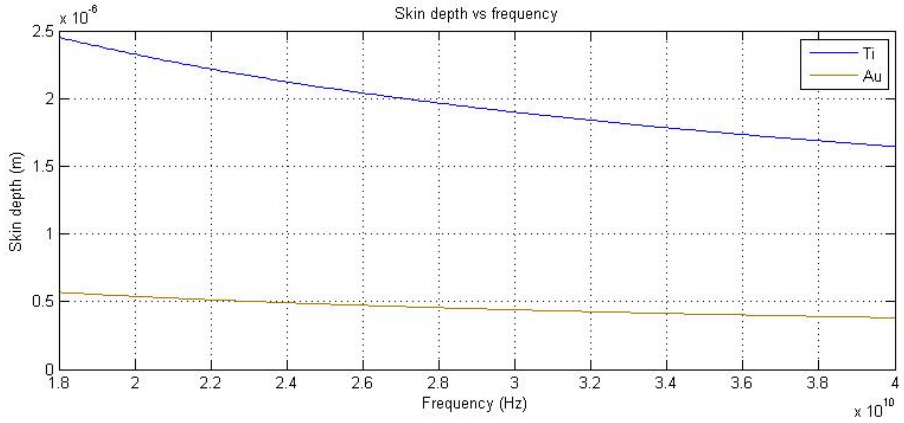


**Figure 5-21 Skin depth vs frequency**

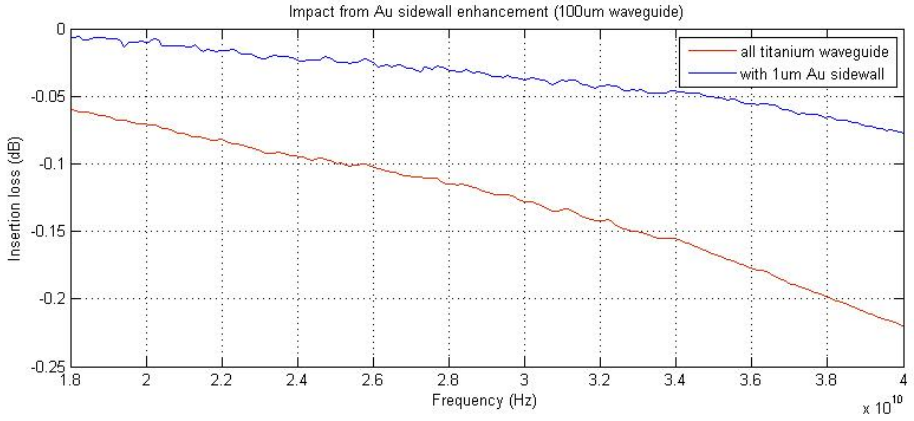


**Figure 5-22 Impact of Au sidewall enhancement on 100 μm long waveguide**

As seen in Chapter 2, the propagation loss for a BCB filed gold waveguide with the same dimensions, according to Eq. (2.46), assuming a conductor loss-dominating regime, should be ~ $\sqrt{1/\sigma_c}$ and therefore the sidewall enhancement should reduce the loss to ~ 0.049 dB, or a loss reduction of ~ 4.49 X. The discrepancy can be accounted for by the limited conformality of the sputtered gold film, i.e., the sidewall is only covered partially due to process limitations.

The insertion loss of the sidewall enhanced waveguides for different lengths, as plotted in Figure 5-23. The loss at 40 GHz shows a nearly linear dependence (Figure 5-24) versus length, which is consistent with Eq. (5.2).

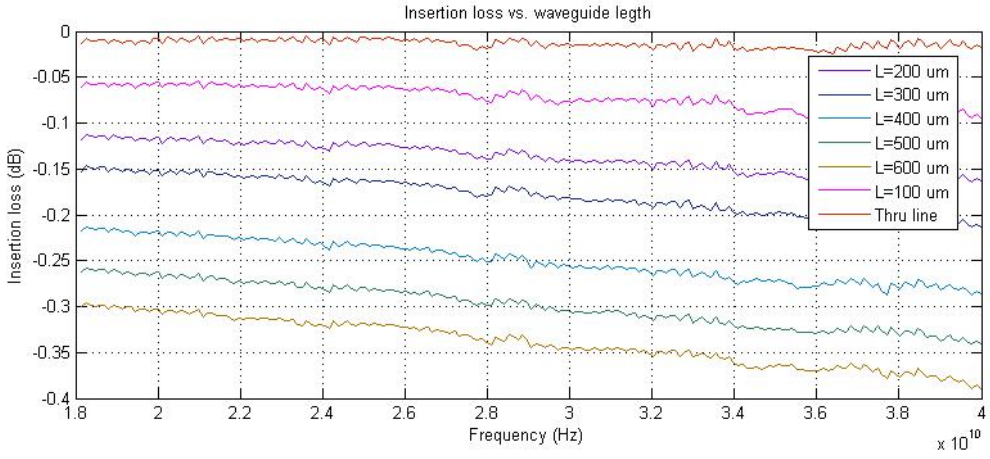


**Figure 5-23 Insertion loss vs. length for Au enhanced waveguides**

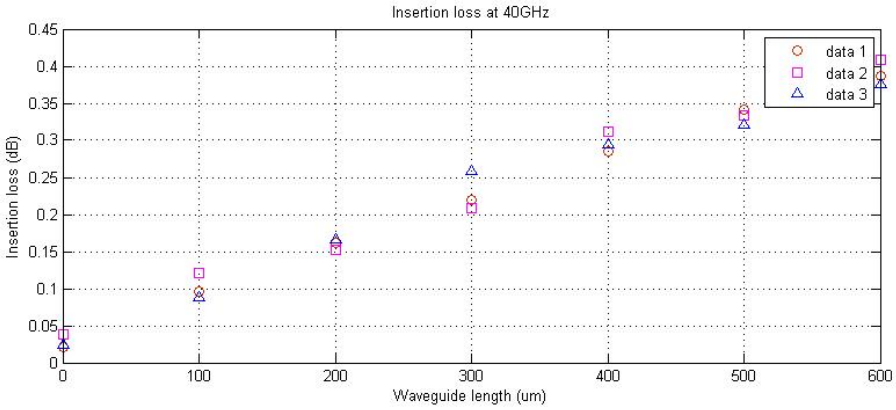


**Figure 5-24 Insertion loss at 40 GHz**

The waveguide performance can be significantly impacted by the presence of the package. However, the good field confinement provided by the bulk titanium waveguide ensure inconsiderable impact due to package, as shown in the measurement

results (Figure 5-25). With a package on top, the insertion loss of a 200 μm waveguide increased by ~0.08 dB at 40 GHz.

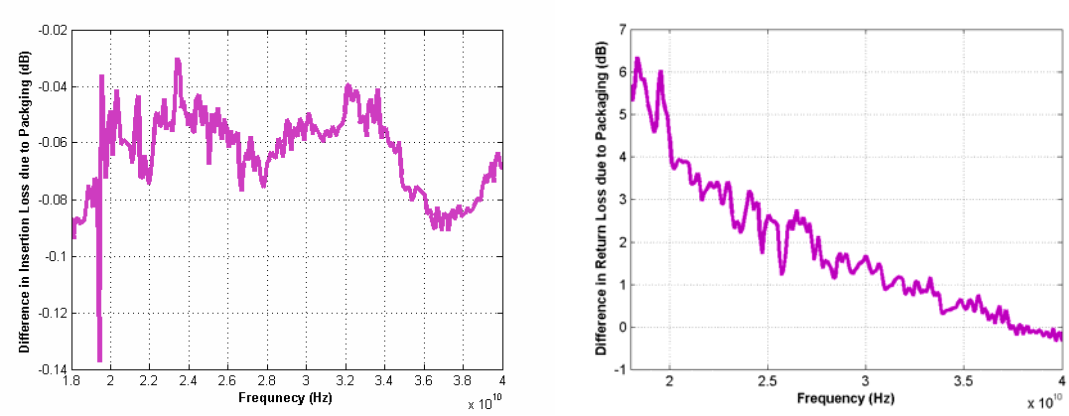


**Figure 5-25 Impact of package on loss characteristics. Left: Insertion loss; Right: Return loss**

The corresponding return loss of the waveguide, as shown in Figure 5-26, peaked at 40 GHz and is consistently below 28 dB, indicating a successful calibration.

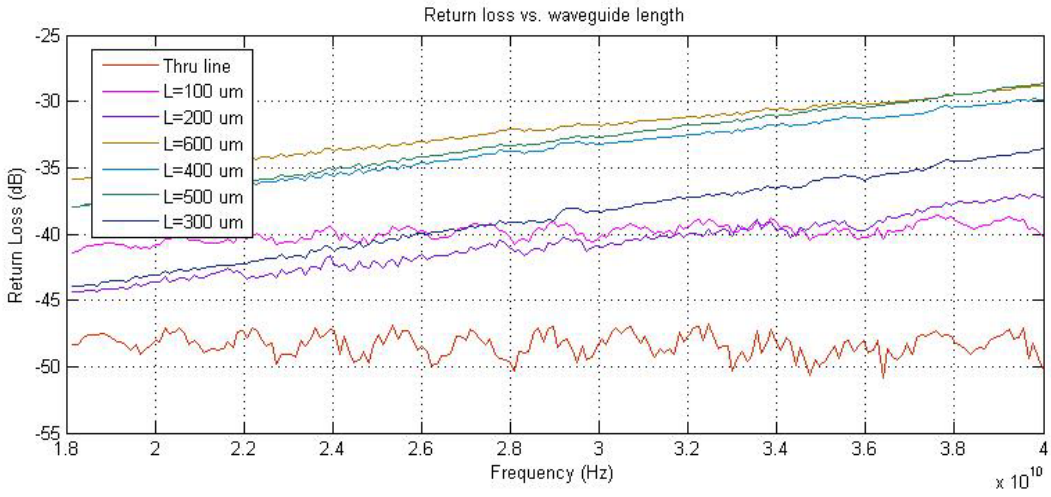


**Figure 5-26 Return loss vs. waveguide length**

## 5.7 Effects due to processing imperfections

Besides the parasitics, the behaviors of RF components can be also negatively impacted by the non-ideal procedures involved in their fabrication processes. The most influential imperfections include sidewall roughness, etching grass/particles, angled sidewalls, and polishing defects. Sidewall roughness results from the combination of etching and sidewall film deposition. The effect of small (compared to skin depth) sidewall roughness can be modeled as an addition to the effective series resistance [8]:

$$\alpha_c^{'} = \alpha_c \left[ 1 + 2/\pi \tan^{-1}\{1.4(\Delta/\delta_s)^2\} \right], \tag{5.5}$$

where $\Delta$ is the characteristic dimension of the roughness, and $\delta_s$ the skin depth. At 40 GHz, for $\Delta$~500 nm (striation on sidewall), the percentage increase in the conductor loss due to roughness on titanium waveguide is therefore, approximately, 8.65%. In the case of thick sidewall Au coverage, the increase becomes 75.1%. Note that, since Equation (5.5) is obtained based on a perturbation theory, it is no longer accurate for $\Delta \sim \delta_s$.

Although the titanium etching process is much more robust since its invention [9-11], it is still going through constant refinements. Etching defects can still appear and serve as scattering centers inside the waveguides and the probability of such occurrences increases with waveguide length. In addition, the success of the calibration procedure also depends on the successful and accurate fabrication of the standards, which, since occupying more area, as seen in Figure 5-27, are more susceptible to processing imperfections.

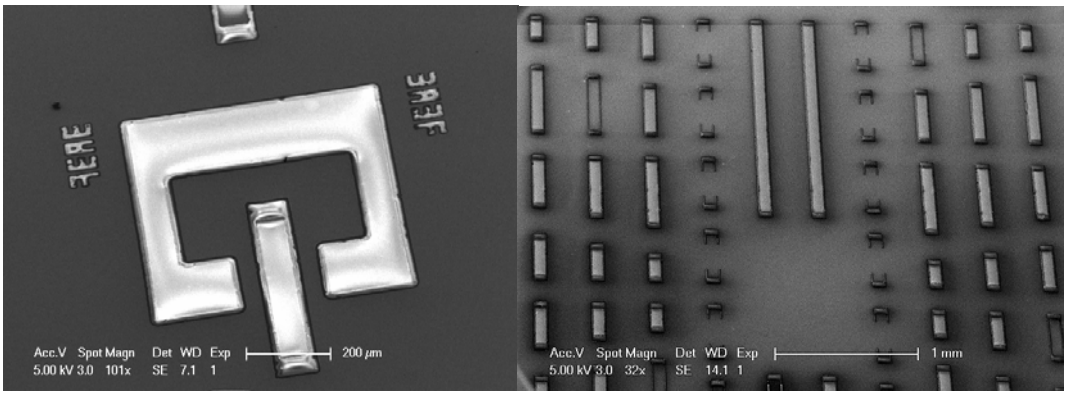


**Figure 5-27 Fabricated Bulk titanium waveguides. Left: a single waveguide with electrode; Right: A set of TRL calibration devices**

Non- (but near-) straight sidewalls, as long as the cross-section remains consistent throughout the length of the waveguides, will only change the impedance and field distribution slightly and will not cause significant loss and change in RF performance. However, variations in cross-section can serve as scattering centers.

Polishing can also lead to device inconsistencies with uneven surface finishes and residue particles.

## 5.8 Impact from packaging

The presence of a metal cap atop an RF system helps isolate electromagnetic noises from reaching the system and disturbing the electromagnetic fields of the signal being transmitted. The most common form of an RF package is a metal cap, as well as associated electrical interconnections, and it is commonly implemented in nearly all RF circuits. However, the introduction of metal cap and electrical interconnections also lead to issues that can negatively impact system performance and reliability. In the case of RFMEMS, the package also serves the purpose of sealing the MEMS,

protecting it from environmental influences such as pressure change, particles and moisture.

The most prevalent packaging solution involves a metal cap and signal traces which enter and exit the package from beneath the seal ring. An insulating layer is implemented to electrically isolate the signals from the package without disturbing the package seal. While this approach is topologically compatible with most planar circuits, the main issues involved are the added parasitic capacitance to the package due to the proximity of the package as the signal traces enter and exit the package, which can also vary with the presence of external forces; the reliability of the package seal, due to the inclusion of an insulating layer underneath the seal ring; and the limited interconnect density.

Another effect of the package is the modal coupling between the transmission modes of the RF system and the metal cavity created by the package. The amount of coupling is a function of mode overlap, as well as the frequency of operation. In other words, to ensure minimum radiation loss, modal overlap needs to be minimized and the frequency of operation sufficiently apart from the lowest parasitic mode.

The parasitic modes of a metal package can be analyzed by approximating the boundaries to those of a rectangular metal cavity. The resonance modes, $\Psi_{nmq}$, of an air-filled rectangular cavity, by approximating metal surfaces with perfect conductors, correspond to frequencies:

$$f_{cavity} = \frac{c}{2}\sqrt{\left(\frac{q}{l}\right)^2 + \left(\frac{n}{a}\right)^2 + \left(\frac{m}{b}\right)^2}, \tag{5.6}$$

where c is the speed of light; dimensions a, b and l are illustrated as in Figure 5-28; n, m, q are the mode indices. For example, the mode shapes indicated by the dotted lines in Figure 5-29 correspond to n=4, m=2, q=8.

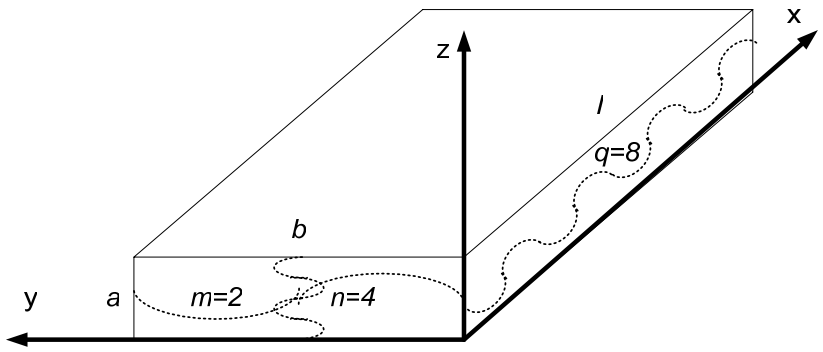


**Figure 5-28 Cavity modes created by metal package**

The frequency of the fundamental mode, $f_0$, is obtained by setting n=1, m=1, q=1:

$$f_0 = \frac{c}{2}\sqrt{\left(\frac{1}{l}\right)^2 + \left(\frac{1}{a}\right)^2 + \left(\frac{1}{b}\right)^2} \tag{5.7}$$

For a package with dimensions typical for conventional planar circuit: a=b=l=5 mm, $f_0$~51.96 GHz, which becomes comparable to the top of the K band frequencies.

The field confinement of the bulk titanium waveguide, however, enables much tighter packages. For example, the surface RF switches have a package as small as 800 μm x 800 μm x 50 μm, which translates into a fundamental mode frequency, from Equation (5.7), of ~3.012 THz, or 2 orders of magnitude higher than the top of the Ka band.

## 5.9 Summary and technology comparison

Table 5-4 outlines how the bulk titanium waveguide compares with other forms of planar waveguides in terms of RF performances.

**Table 5-4 Comparison between planar waveguides**

| | Impedance (Ω) | Dielectric loss | Conductor loss | Radiation Loss |
|---|---|---|---|---|
| Bulk-Ti | Low to medium (limited by trench-filling) | low | medium to low (low when sidewall enhanced with Au) | low |
| Microstrip | Low to high | low | low | moderate |
| CPW | Medium to high | low | Moderate (current crowding) | moderate |
| LIGA CPW | Low to high | low | medium to low | low |

| | Ease of integration with other components | RFMEMS processing and packaging | Additional notes |
|---|---|---|---|
| Bulk-Ti | Moderate | Planar surface compatible with layer stacking; Compact, low loss with high density, integrated through-wafer interconnects | New platform; Small footprint; Low cross-talk; High packing density; High coupling between in-plane adjacent conductors |
| Microstrip | Moderate to difficult | Layer stacking possible; Medium sized metal cap with interconnects from side or laser-drilled through vias | Well established platform |
| CPW | Easy | Layer stacking possible; Medium sized metal cap with interconnects from side or laser-drilled through vias | Well established platform; Flexible design |
| LIGA CPW | moderate | Single layer only; Medium sized (rely on CPW for interconnects and packaging); | New components; High coupling between in-plane adjacent conductors |

To compare the propagation loss of the bulk titanium waveguide with conventional CPW, we use measured results from waveguides reported in [9-12] because of the similar lateral waveguide dimensions and frequency ranges used in experimental measurements. The CPWs reported in [10, 11] were fabricated on insulating

substrates with Ag or Au traces. The conductor dimensions are as follows: thickness: 0.8 μm; center conductor width: 10 μm; gap: 7 μm. For the CPW fabricated on a GaAs substrate with evaporated Ag ($\sigma$=6.0e05 $S \cdot cm^{-1}$) traces, the propagation loss was measured to be ~0.60 dB/mm (40 GHz). On a pyrex substrate with electroplated Au traces ($\sigma$=2.55e05 $S \cdot cm^{-1}$), the loss was ~ 0.72 dB/mm (40 GHz). With similar geometries but thinner Au traces on GaAs substrates, the CPWs used in [9, 12] produced slightly higher losses. For center conductor width of 4 m and a gap of 13 μm, CPWs with 0.25 μm thick Au traces generated a loss of ~2.3 dB/mm (40 GHz). A 0.5 μm thick Au reduced the loss to ~1.2 dB/mm (40 GHz). When the conductor traces are wider (6 μm) and with a larger gap of 43 μm, the losses were reduced to ~0.8 dB/mm and 0.4 dB/mm for Au thickness of 0.25 μm and 0.5 μm, respectively. The propagation loss increased rapidly with a reduced gap, indicating the current crowding effect in CPW.

As shown in Figure 5-23, the Au-coated bulk titanium waveguide was measured to have a loss of ~0.68 dB/mm. The measured difference in propagation loss compared to CPW is not enough to show the advantage of the bulk titanium waveguide. This can be attributed to process imperfections such as the insufficient Au sidewall coverage near the bottom of the trenches, as also indicated in Figure 5-22.

The key differences of the titanium waveguide when compared to traditional waveguides such as microstrip and CPW lie in it unique topology. The high aspect ratio construction ensures superior field confinement within the gap, therefore reducing the radiation loss and cross-talks with components in its vicinity. The conductor loss, however, has to do with the conductor used. Titanium's conductivity is ~ 20 times less compared to gold and a waveguide constructed by all titanium as its conductor generates more loss. A sidewall enhancement with gold reduces that loss significantly. Due to the coplanar nature of the grounds, similar to traditional CPW,

bulk titanium waveguide can be easily integrated with other components through direct bonding. The high aspect ratio, through-wafer construction of the titanium waveguide doubles as electrical interconnects, which along with the superior field confinement, provide a compact, high performance alternative to micro-component packaging.

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# CHAPTER 6

# FUTURE DIRECTIONS: APPLICATIONS BASED ON BULK-TITANIUM RF PLATFORM

In this thesis, the fundamental properties of a novel, bulk titanium waveguide design have been investigated in depth. A quasi-static model delineates the dependence of its operational characteristics on key design parameters. A comprehensive suite of fabrication techniques has also been developed and characterized. Furthermore, a compact package has been successfully integrated on the waveguide, and experiments carried out confirmed the predicted performance using models and simulations. The next major step in this project is to extend the basic functionality of the waveguide for the establishment of a comprehensive RF platform integrating higher level functionalities.

The bulk titanium waveguide has distinct advantages over previous traditional forms of waveguides. These advantages can be extended by making better, more efficient RF component/systems with functionalities beyond simple waveguides. For instance, the superior field confinement of the bulk titanium waveguide helps reducing the overall chip size by reducing parasitic coupling effects; the integrated, high-density, through-wafer interconnects further reduce chip size while improving performance due to shorter signal paths; the flat surface of the waveguide facilitates the integration of additional layers and processing sequences. For applications, the high aspect ratio waveguide reduces parasitic coupling, thereby allowing compact, titanium packaging well suited for corrosive environments such as sea water. The bio-compatibility of titanium lends itself to potential implantable biomedical applications.

In order to further explore the opportunities of potential applications based on the bulk titanium RF platform, it is necessary to investigate the fundamental properties of the waveguide in implementations beyond its original ideal waveguide form. The most notable implementation in this case involves discontinuities. As with the traditional planar waveguides, such as microstrip [1-7] and CPW [8-12], fully understanding these discontinuities is essential for device applications beyond waveguides. As an initial attempt, HFSS will be used to explore these fundamental issues.

## 6.1 Discontinuities in bulk titanium waveguide

In planar circuitry, waveguides not only serve as the signal carrying medium, but also perform other functions such as signal splitting and impedance matching. Planar waveguides are often curved with a tight radius for saving chip space. These geometric changes, however, introduce discontinuities seen by the signal, which lead to significant losses and device performance penalties if not designed properly. For simplicity, all waveguides used in the analyses below have a uniform cross-section with a 15 μm trench width, a 30 μm center conductor width and a 50 μm height.

### 6.1.1 Bends

As with traditional CPW, a bend in the waveguide causes a change in the conductive length between the inner and outer radii, and can result in substantial radiation loss [10, 11]. Air bridges or mitred corners are often implemented to help reduce the radiation. While these approaches are successful in some applications, they are typically limited to operation within a finite bandwidth and can add processing complexity, or become

a reliability concern. Better field confinement in the bulk titanium waveguide may help reducing the radiation loss.

Figure 6-1 shows the HFSS model used for simulating a 180 degree bend with a 100 μm radius and within a 1mm long waveguide. Multiple modes are assigned to the input and output ports to analyze the effect of modal coupling. The additional loss in the fundamental mode, when compared to a straight 1 mm long waveguide, is computed to be 0.21 dB at 40 GHz.

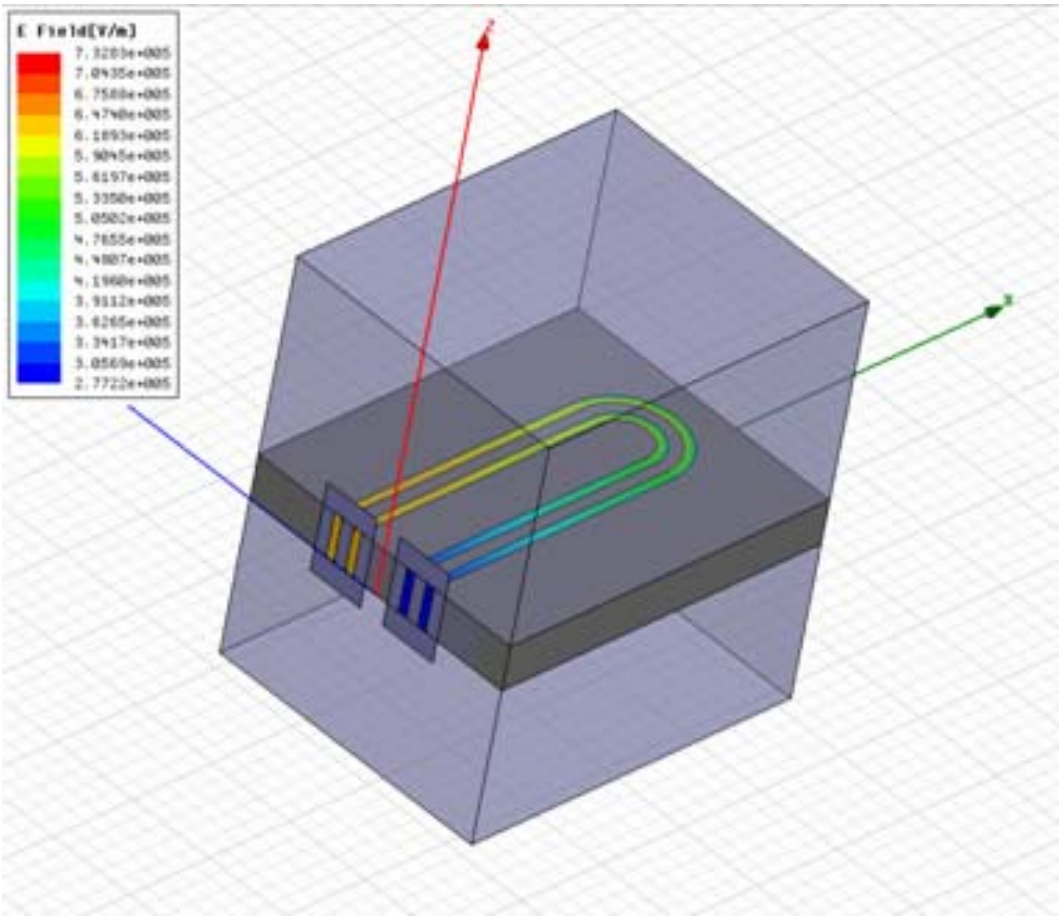


**Figure 6-1 HFSS model for bend analysis**

### 6.1.2 Tapers

One of the key advantages of planar circuits is the possibility of tailoring device characteristics by simply varying lateral dimensions. Tapers, as opposed to abrupt steps, are often used to transfer signals between ports with different dimensions without introducing excessive losses. Figure 6-2 shows the model used to study a taper transitioning from a 30 μm waveguide width to 10 μm. This taper transforms the impedance from ~71.5 Ω to 23.8 Ω, a tapering length of 200 μm introduce an additional ~0.17 dB to the computed insertion loss.

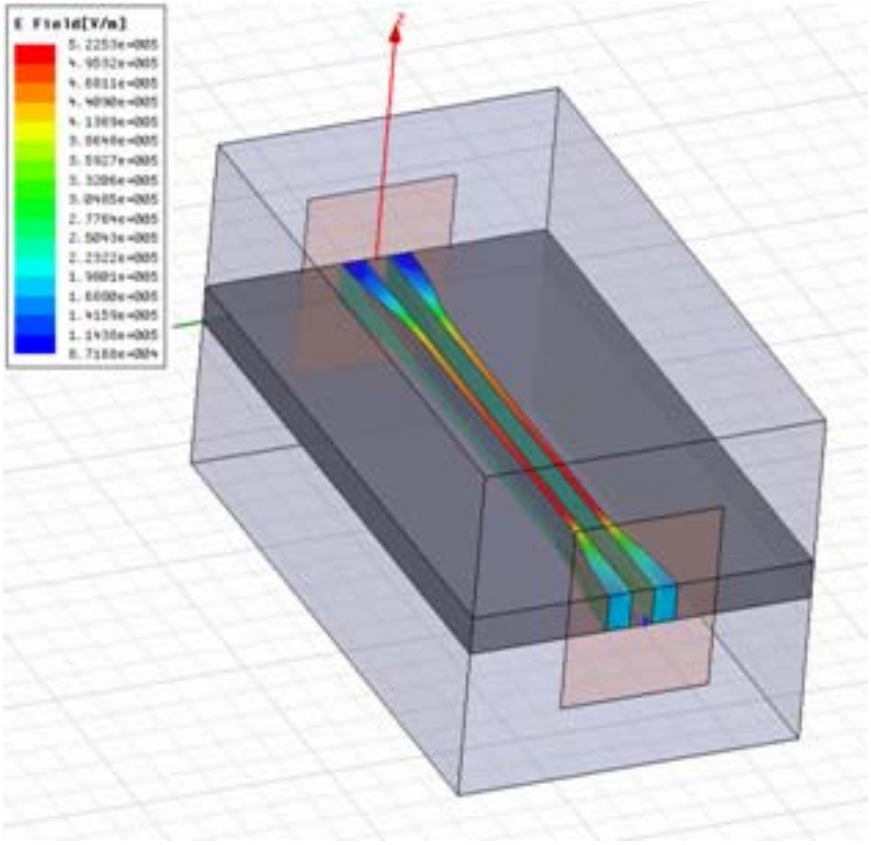

**Figure 6-2 HFSS model for study on tapers**

### 6.1.3 Interface with traditional CPW

To better integrate with other devices and systems that are not implemented on the bulk titanium waveguide, it is essential to study the behavior of the interface between a bulk titanium waveguide to traditional planar circuits. CPW is chosen here, due to its relative topological similarities to the bulk titanium waveguide. However the topology dissimilarity is large enough such that significant power loss can be expected at the transition interface. The construction of one attempted such interface is illustrated in Figure 6-3. 50 μm x 50 μm x 50 μm gold cubes are used to simulate electroplated solder joints between the bulk titanium waveguide and the CPW. Note that the center conductor is widened to 100 m. The interface loss is obtained by comparing the waveguide/switch structures with and without the interface to CPW. At 40GHz, the loss from each taper transition is ~ 1.52 dB (~half of the total insertion loss)

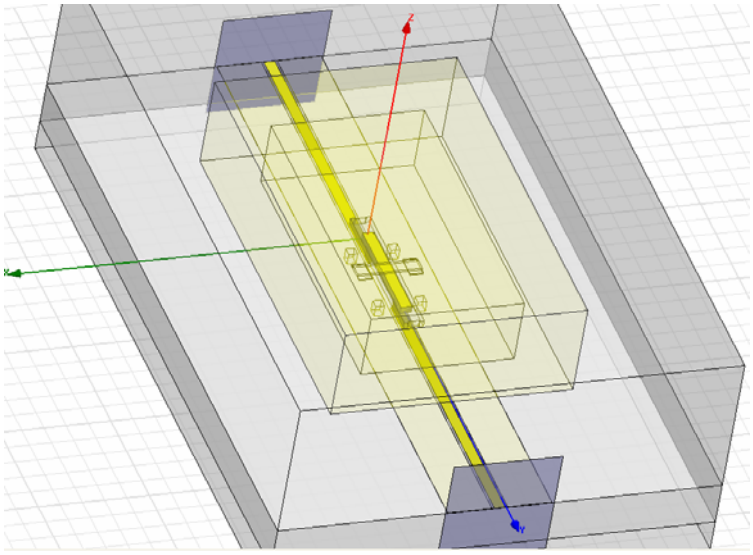

**Figure 6-3 HFSS model for integration of bulk titanium waveguide with traditional CPW**

## 6.2 Applications based on BTW RF platform

The above simulations show that the bulk titanium waveguide provides acceptable RF performance without extensive optimization. Applications based on the extension of the waveguide concept can be developed. As a demonstration for the bulk titanium waveguide, we study three specific device applications: a band pass filter, a RF switch and a shielded waveguide, which can be implemented based on the understanding of the waveguide characteristics.

### 6.2.1 Band-pass filter

The distributed behavior of waveguides makes them natural candidates for constructing filters. Discontinuities can act as controlled reactive components used to adjust filter parameters.

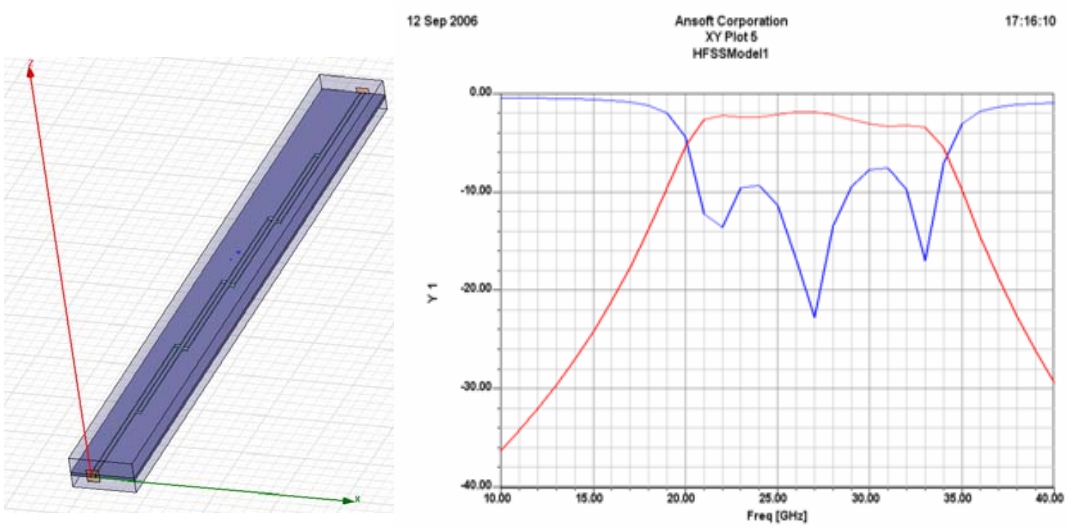


**Figure 6-4 HFSS model and results for band pass filter design I. Red curve: S21; blue curve: S11**

While both CPW and microstrip band-pass filters have been constructed and studied extensively in literature [2, 3, 8, 11, 13], the bandwidth of the filters is reduced by the limited capacitive coupling. The high aspect ratio of the bulk titanium waveguide provides large coupling, and enables increased bandwidth range and low insertion loss.

Plotted in Figure 6-4 is the HFSS simulation results on the initial design of a band-pass filter. For the 30 GHz filter, a center frequency of ~27.5 GHz, a 3-dB bandwidth of ~14 GHz, or ~51% of the center frequency, and a minimum insertion loss of ~1.95 dB at ~26.5 GHz are obtained.

An end-coupled filter design is also simulated. As shown in Figure 6-5, the center frequency is ~29 GHz; the 3-dB bandwidth is ~28.5 GHz, or ~98% of the center frequency; the minimum insertion loss is ~1.4 dB, occurring at ~28 GHz.

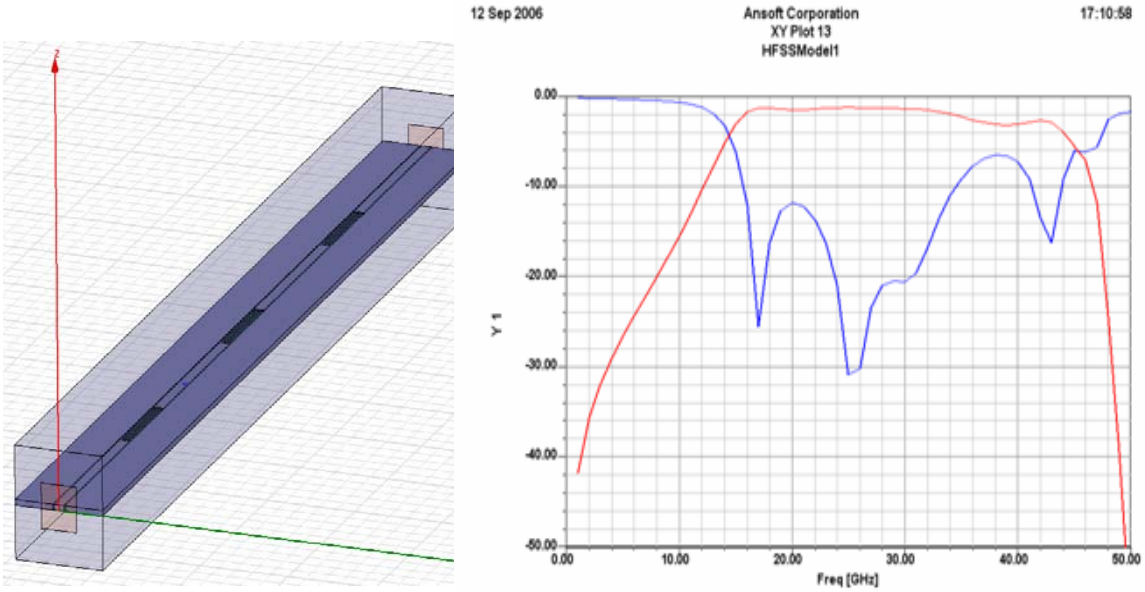


**Figure 6-5 HFSS model and results for band pass filter design II. Red curve: S21; blue curve: S11**

### 6.2.2 RF switch

**1) Simulation**

To further illustrate the capability of the bulk titanium waveguide as the building block for an RF system, we choose a shunt RF switch as the demonstration vehicle.

The shunt switch is a more natural implementation for the bulk titanium waveguide, due to the reduction in transition loss. A simplified Ohmic contact switch design is shown in Figure 6-6. At 40 GHz, the insertion loss is ~ 0.22 dB and isolation for a perfect Ohmic contact ~38 dB.

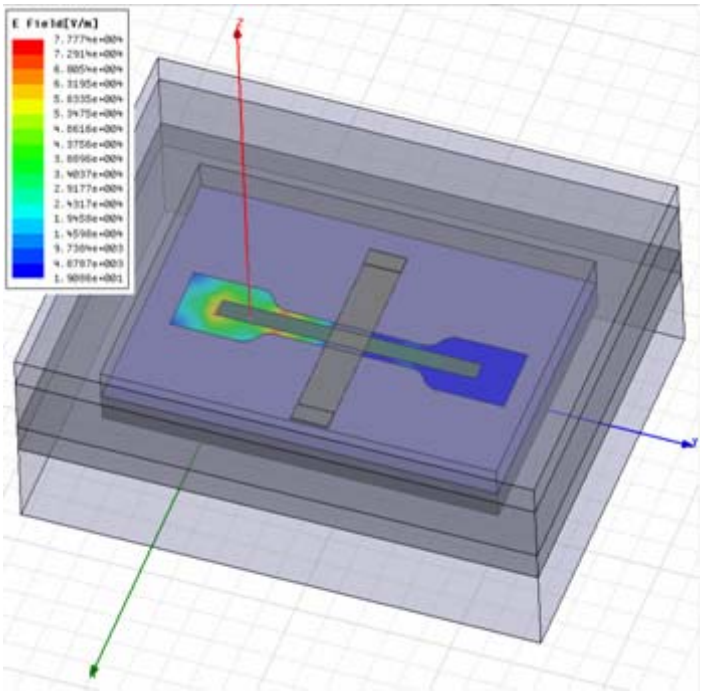


**Figure 6-6 HFSS model for shunt RF contact switch**

The effect of non-zero contact resistance is analyzed by inserting a resistive surface layer at the contact, which induces field leakage, or reduced isolation performance as shown in Figure 6-7.

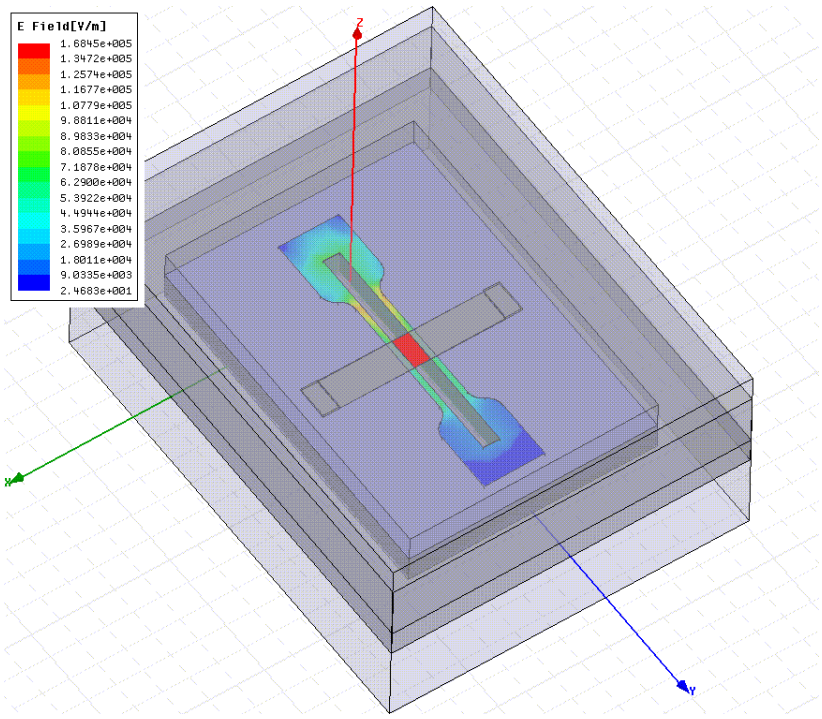


**Figure 6-7 Field leakage (reduced isolation) due to non-zero contact resistance**

### 2) Initial experimental results

As an ongoing effort, we fabricated switches with a surface micromachining process. Figure 6-8 shows the process flow. Although we have successfully stress-engineered the surface switch through the use of a composite beam construction and achieved a relatively flat structure over flat titanium substrates (see Figure 6-10 and Figure 6-12), the current generation devices are still experiencing issues with release residue, which prevented the complete contact of the switch. As a result, no direct measurement of isolation was obtained. However, they still serve as a parasitic capacitor and therefore validate the true insertion loss of the bulk titanium waveguide-based RF system. In addition, our design includes an additional proof-of-concept device. The surface switch structure is deposited without sacrificial layer, thus shorting the center conductor to ground and demonstrating the isolation performance of a nearly ideal contact. Figure  shows the insertion loss of the partially released switch, which is

~0.31dB at 40GHz. The isolation of the stuck-on device is shown in Figure 6-15. The measured isolation of this ideal contact is ~ 32 dB at 40GHz.

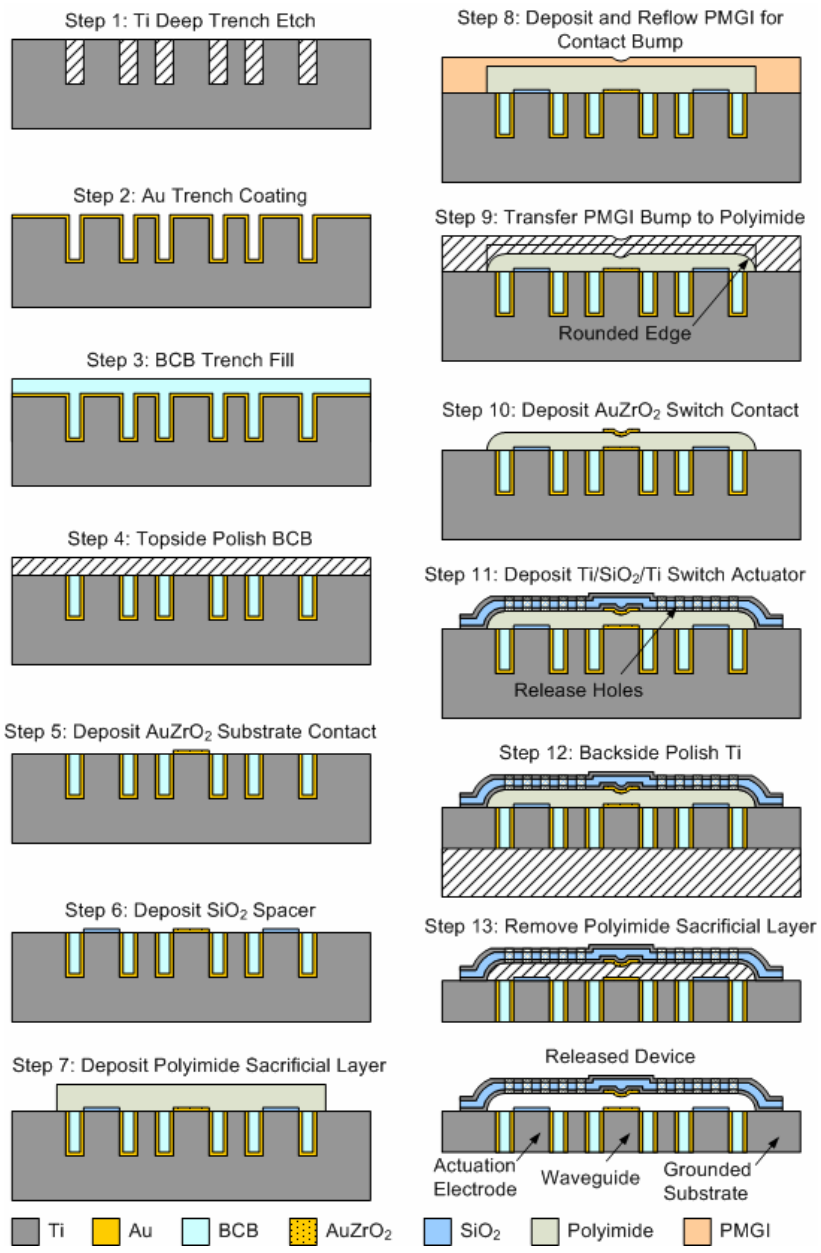


**Figure 6-8 Process sequence for surface RF switch on bulk titanium waveguide**

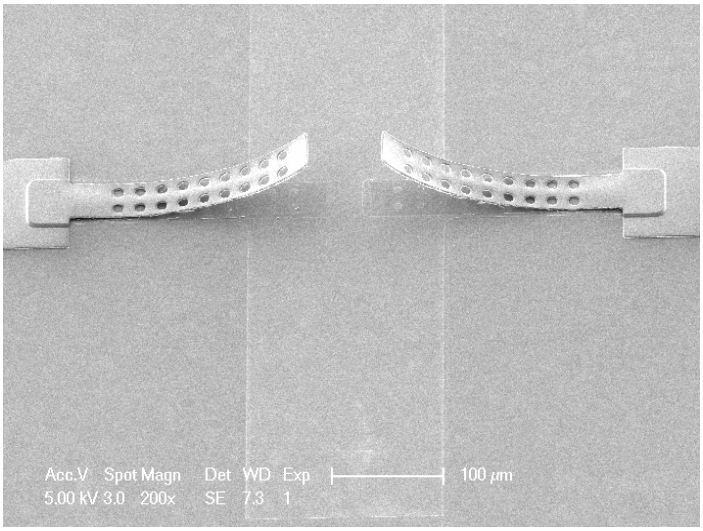


**Figure 6-9 Surface RF switch before stress-engineering**

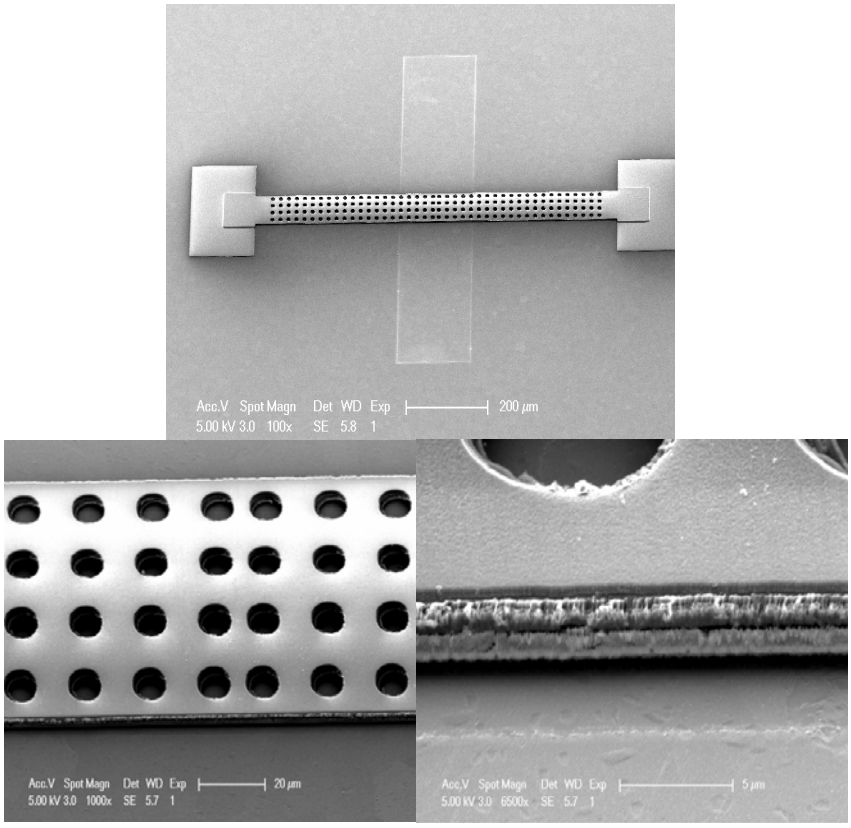


**Figure 6-10 Stress-engineered surface RF switch structure**

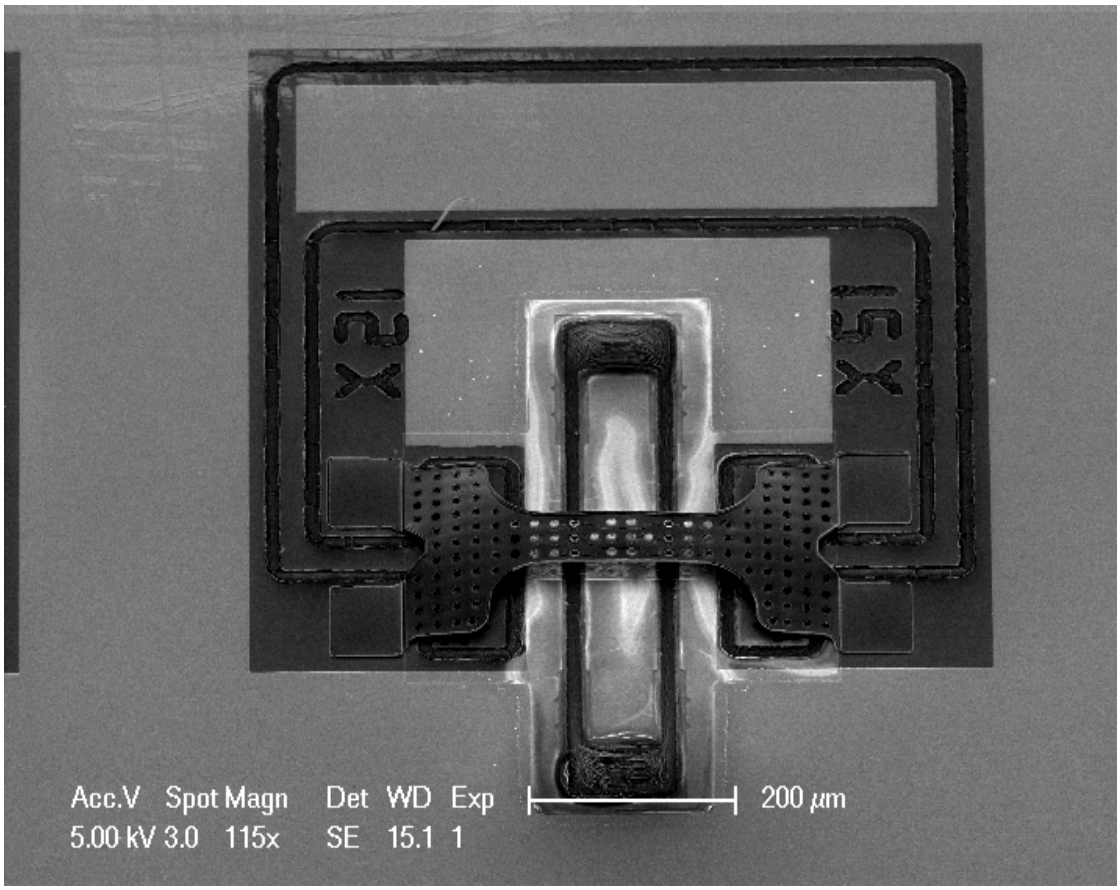


**Figure 6-11 Completed RF shunt switch on bulk titanium waveguide**

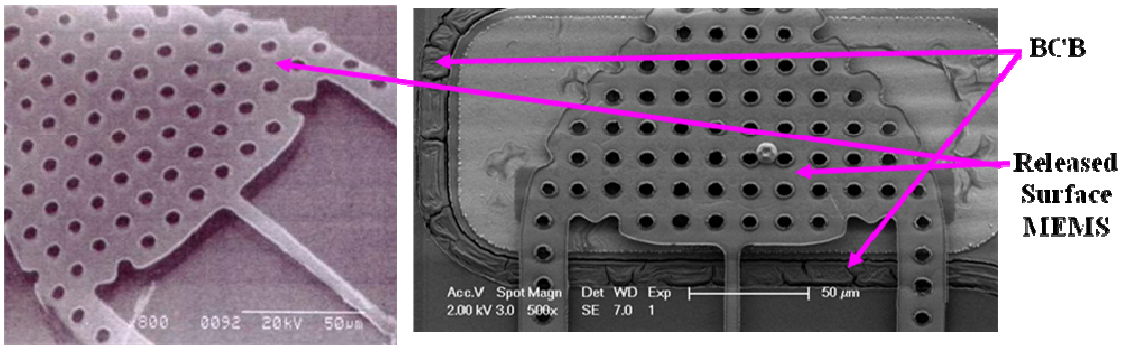


**Figure 6-12 Completed RF shunt switch**

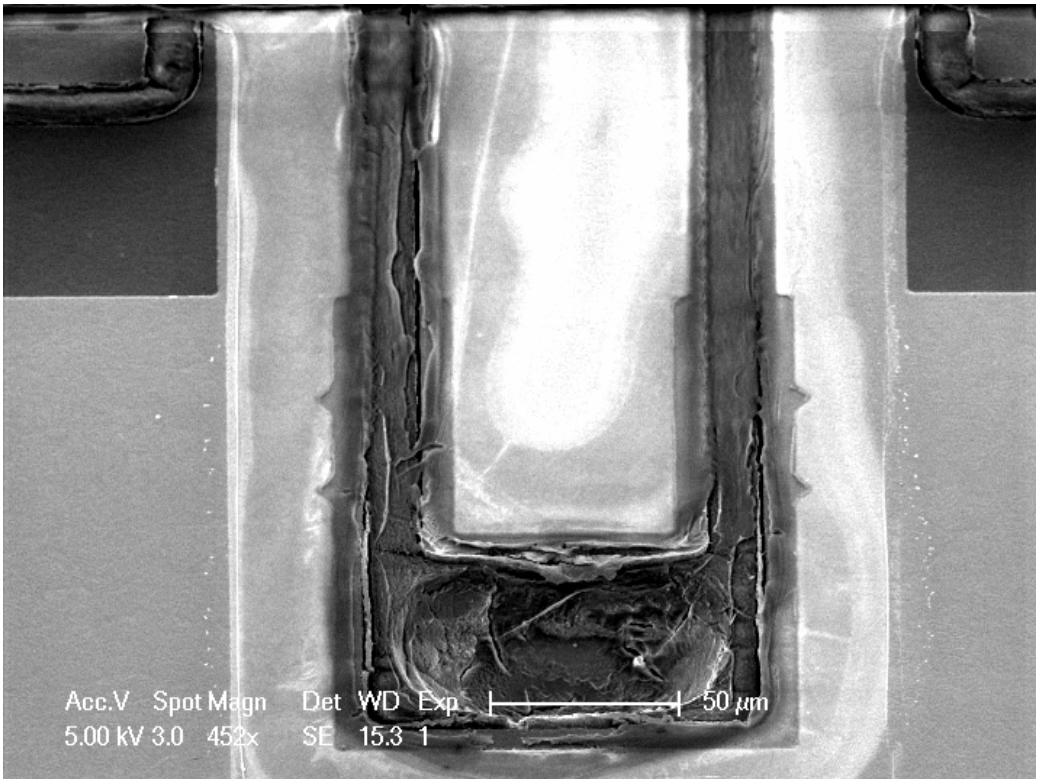


**Figure 6-13 Residue after release etch**

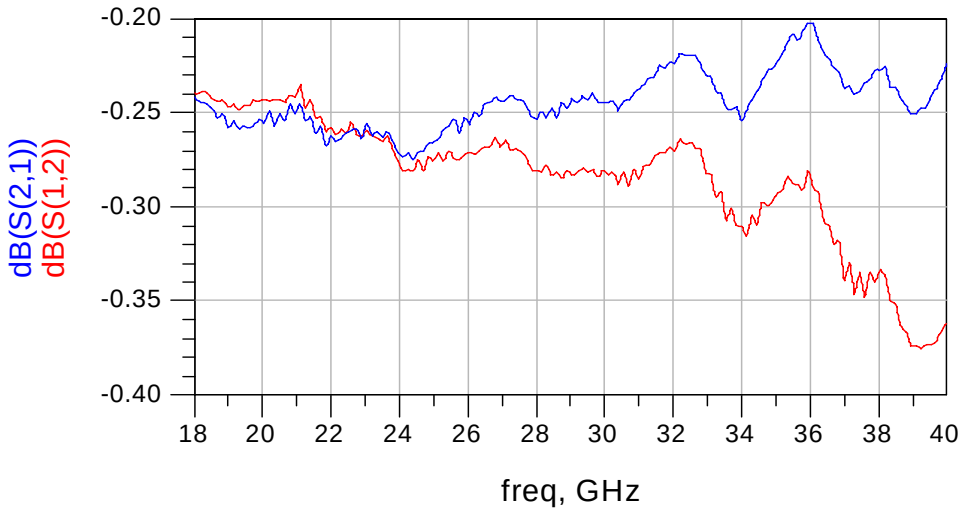


**Figure 6-14 Measured insertion loss of a partially released device**

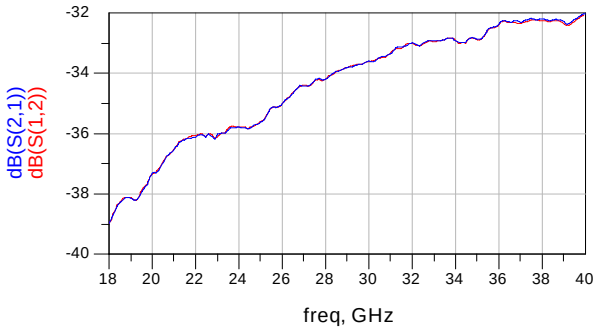


**Figure 6-15 Measured isolation of a stuck-on device**

### 6.2.3 Shielded waveguide

Completely shielded waveguides [14] are desirable in applications where minimum cross-talk is allowed. Macroscopic waveguides, such as coaxial lines, support a wide range of applications by ensuring low-loss with minimum cross-talk. Due to field confinement and the layer-stacking process capability of the bulk titanium waveguide, a completely shielded waveguide structure can be constructed without introducing significant design or process changes. The performance of these structures is simulated with HFSS (see Figure 6-16). At 40 GHz, the propagation loss is simulated at ~0.28 dB/mm.

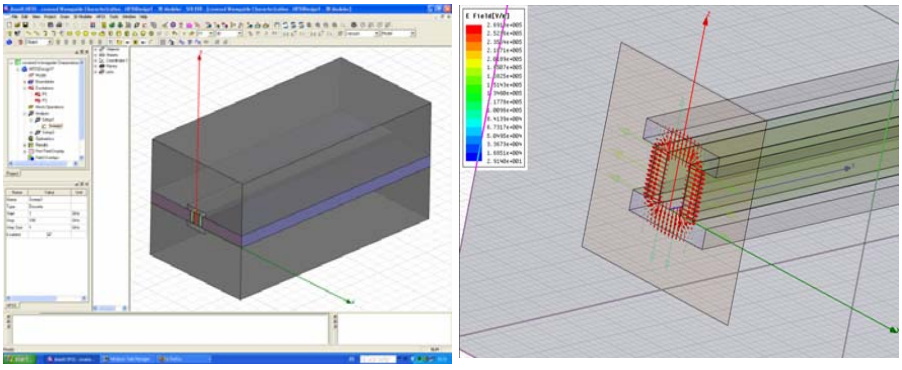

**Figure 6-16 HFSS model for completely shielded waveguide**

## 6.3 Summary

With HFSS as the main tool, common discontinuities occurring in the bulk titanium waveguide are investigated. The characterization of these discontinuities provides the critical knowledge for extending the functionality of the novel microwave transmission line beyond the basic functionalities of the waveguide.

Key results at 40GHz are as follows: a $180^0$ bend within a 1mm long waveguide with a 100 μm radius causes an additional loss of, when compared to a straight waveguide, ~0.21 dB; a 200 μm long taper which gradually completes the width transition from 30 μm to 10 μm leads to an additional loss ~0.17 dB; an interface with 50 μm x 50 μm x 50 μm electroplated gold solder joints on a conventional CPW generates ~1.52 dB transition loss.

Several applications based on the bulk titanium waveguide have also been studied. Initial designs of band-pass filters which take advantage of the high coupling between adjacent conductors have been shown to have high pass-band widths and low insertion losses. For a broad-side coupled filter, a center frequency of ~27.5 GHz, a 3-dB bandwidth of ~14 GHz (~51% of the center frequency), and a minimum insertion loss of ~1.95 dB at ~26.5 GHz are obtained. End-coupled filter design is also attempted. The center frequency is ~29 GHz; the 3-dB bandwidth is ~28.5 GHz (~98% of the center frequency); the minimum insertion loss is ~1.4 dB, occurring at ~28 GHz.

Another important technology extension is RF switch. Surface shunt switches are investigated with simulations and experiments. While simulations demonstrated the feasibility of the switches with good performance results in both insertion loss and isolation, early experiments based on a plasma-released composite surface MEMS process verified the switch concept with low measured insertion loss and high isolation. The composite surface structure has a CVD $SiO_2$ core layer sandwiched

between evaporated titanium layers. Thicknesses of these layers are used to fine tune the overall stress. While a more robust release process is still being studied, preliminary results provide a proof of concept: at 40 GHz, the insertion loss is measured to be ~0.31 dB; the isolation of a stuck-on device with ideal contacts is measured to be ~32 dB.

Finally, as a natural extension from the bulk titanium waveguide, completely shielded waveguides are simulated. The computed transmission loss based on first-generation design is ~0.28 dB/mm at 40GHz.

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## APPENDIX

### A. Derivation for field equations for waveguides with an arbitrary cross-section

A generalized waveguide with a uniform cross section is used and waves are assumed to propagate in the +z direction, as shown in Figure A-1:

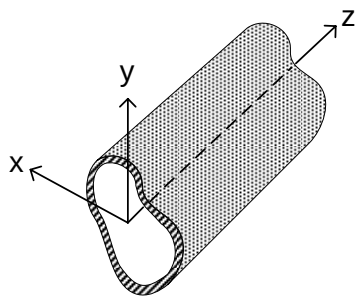


**Figure A-1 A uniform waveguide with an arbitrary cross section**

Here the wave carrying media has permeability $\mu$ and permittivity $\varepsilon$. Using the source-free form, i.e., current density $J$=0 and charge density =0, of Maxwell's equations, the electric field $E$ and magnetic field $H$ follow a relation described by a second-order differential equation:

$$\nabla \times \nabla \times E = -\mu \frac{\partial}{\partial t}(\nabla \times H) = -\mu\varepsilon \frac{\partial^2 E}{\partial t^2} \tag{2.1}$$

Re-writing the expression and substituting $u = 1/\sqrt{\mu\varepsilon}$, equation (2.1) becomes

$$\nabla^2 E - \frac{1}{u^2}\frac{\partial^2 E}{\partial t^2} = 0\,. \tag{2.2}$$

Assuming that the waves propagates in the +z direction with a propagation constant

$$\gamma = \alpha + i\beta \,, \tag{2.3}$$

and a harmonic time dependence with an angular frequency $\omega$, eq.(2.2) becomes

$$\nabla^2 E + k^2 E = 0 \,, \tag{2.4}$$

where $k \equiv \omega\sqrt{\mu\varepsilon}$ . The magnetic field distribution follows a similar relation:

$$\nabla^2 H + k^2 H = 0 \,. \tag{2.5}$$

Eq.s (2.4) and (2.5) are known as Helmholtz equations. Separating the Laplacian operator into cross-sectional and longitudinal coordinates, we have

$$\begin{aligned} \nabla_{xy}{}^2 E + h^2 E &= 0 \\ \nabla_{xy}{}^2 H + h^2 H &= 0, \end{aligned} \tag{2.6}$$

where

$$h^2 = \gamma^2 + k^2 . \tag{2.7}$$

The various components of E and H are not all independent and are related through Maxwell equations:

$$\begin{aligned} \nabla \times E &= -j\omega\mu H \\ \nabla \times H &= -j\omega\varepsilon E. \end{aligned} \tag{2.8}$$

The transverse field components $E_x^0$, $E_y^0$, $H_x^0$ and $H_y^0$ can therefore be expressed in terms of the two longitudinal components $E_z^0$ and $H_z^0$:

$$H_x^0 = -\frac{1}{h^2}\left(\gamma \frac{\partial H_z^0}{\partial x} - j\omega\varepsilon \frac{\partial E_z^0}{\partial y}\right) \tag{2.9}$$

$$H_y^0 = -\frac{1}{h^2}\left(\gamma \frac{\partial H_z^0}{\partial y} + j\omega\varepsilon \frac{\partial E_z^0}{\partial x}\right) \tag{2.10}$$

$$E_x^0 = -\frac{1}{h^2}\left(\gamma \frac{\partial E_z^0}{\partial x} + j\omega\mu \frac{\partial H_z^0}{\partial y}\right) \tag{2.11}$$

$$E_y^0 = -\frac{1}{h^2}\left(\gamma \frac{\partial E_z^0}{\partial y} - j\omega\mu \frac{\partial H_z^0}{\partial x}\right) . \tag{2.12}$$

## B. Conformal mapping analysis of a finite parallel plate waveguide

The mapping procedure of a finite parallel plate structure is illustrated in Figure B-1:

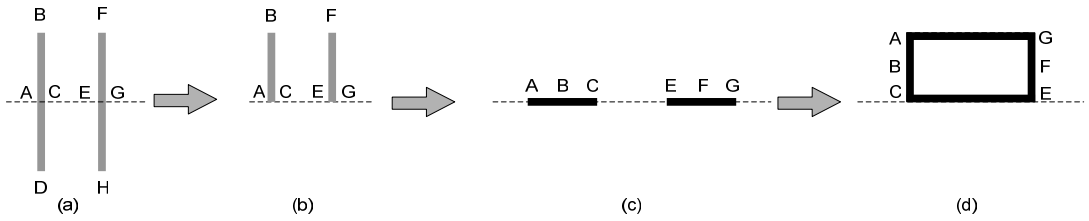


**Figure B-1 Conformal mapping of a finite parallel plate structure**

Starting from a parallel plate capacitor as shown in Figure A-1(a), from symmetry, only a half is taken into the transformation Figure A-1(b); then a Schwarz-Christoffel equation is used to map the boundaries in real space, or the $z = x + iy$ plane, into the another plane, the $t = u + iv$ plane, with the configuration is now a pair of coplanar strips, a mathematically simpler configuration:

$$\frac{dz}{dt} = \frac{A(t^2 - c'^2)}{[(t+\frac{1}{k})(t-\frac{1}{k})(t+1)(t-1)]^{\frac{1}{2}}}, \tag{2.1}$$

where A is a constant, k is the modulus of the elliptic function and c' is a constant that corresponds to the midpoint of the strips in the t plane:

$$c' = \frac{1}{k}\sqrt{\frac{E'(k')}{K'(k')}} \tag{2.2}$$

where $k' \equiv \sqrt{1-k^2}$ , $E'(k')$ is the complete elliptic integral of the second kind and $K'(k')$ is the complete elliptic integral of the first kind. Combining Eqs. (2.1) and (2.2) gives the transformation from the z plane to the w plane:

$$\frac{dz}{dw} = -Ak[sn^2(w,k) - c'^2], \tag{2.3}$$

where $sn(w,k)$ is the Jacobian elliptic function of w.

Since the configuration in the w plane is that of an infinitely large parallel plate, the capacitance between the plates, $C_{tot}$, is given by $\varepsilon_0 * \varepsilon_r * AG/AC$ (in w plane).

Although these analytical equations provide accurate solutions, it is difficult to obtain physical insights on the dependence of key parameters. Approximations can be made to help simplify the problem. For parallel plates with a large aspect ratio, a different transformation can be used which assumes a semi-infinite geometry as shown in Figure B-2.

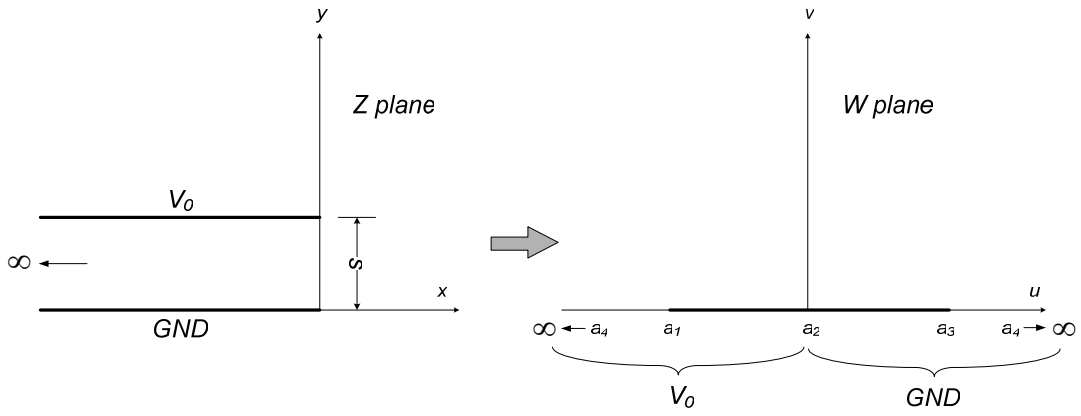


**Figure B-2 Approximated mapping for finite parallel plate structure**

This simplified geometry allows for a simpler conformal mapping based on the following Schwartz transformation:

$$\frac{dz}{dw} = c\frac{(w-a_1)(w-a_3)(w-a_4)}{(w-a_2)} \tag{2.4}$$

where $c$ is a constant, and $a_i$ (i=1 to 4) correspond to the locations on the real axis in the w plane that the vertices in the z plane are mapped to. Rewriting (2.4) and setting

$$a_1 = -1; a_2 = 0; a_3 = +1; a_4 = \infty, \tag{2.5}$$

we have

$$\frac{dz}{dw} = ca_4 \frac{(w-a_1)(w-a_3)(1-w/a_4)}{(w-a_2)} = c' \frac{(w-1)(w+1)}{w}, \tag{2.6}$$

where $c'$ is another constant and to be determined by the specific locations of the vertices in the z plane. Integrating Eq. (2.6) gives

$$z = c'(\frac{w^2}{2} - \ln w) + c'', \tag{2.7}$$

where the constants are determined by the geometry in the z plane: $z = 0 + js$ when $w = a_1 = -1$ and $z = 0 + j0$ when $w = a_3 = +1$ =>

$$c' = -\frac{l}{\pi}; c'' = \frac{l}{2\pi}. \tag{2.8}$$

Plugging Eq. (2.8) into Eq. (2.7) gives the final form of the transformation:

$$z = \frac{l}{\pi}(\frac{1-w^2}{2} + \ln w). \tag{2.9}$$

Eq. (2.9) shows the potential distribution in the resulting w plane is simply, due to symmetry:

$$\Phi = V_0 \frac{\varphi}{\pi}, \tag{2.10}$$

in which $\varphi$ is the angle measured counterclockwise from the positive u axis.

## C. De-embedding procedures for TRL calibration

RF/microwave devices are typically characterized by scattering parameters which relate the incoming and outgoing voltage signals of the various ports. The scattering parameters for a two-port device are defined as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.1}$$

where $a_n$ and $b_n$ are the forward and backward voltages at each port, normalized to the port impedance, $Z_0$. When discussing calibration techniques, where components with different characteristics are cascaded, it is often more convenient to talk in terms of cascadable T-matrices which are defined by

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \tag{3.2}$$

A direct conversion exists between the terms of the S and T matrices:

From S to T:

$$\begin{aligned} T_{11} &= -\frac{\det(S)}{S_{21}} \\ T_{12} &= \frac{S_{11}}{S_{21}} \\ T_{21} &= \frac{-S_{22}}{S_{21}} \\ T_{22} &= \frac{1}{S_{21}} \end{aligned} \tag{3.3}$$

From T to S:

$$
\begin{aligned}
S_{11} &= -\frac{T_{12}}{T_{22}} \\
S_{12} &= \frac{\det(T)}{T_{22}} \\
S_{21} &= \frac{1}{T_{22}} \\
S_{22} &= \frac{-T_{21}}{T_{22}}
\end{aligned}
\tag{3.4}
$$

where det(S) and det(T) indicate the determinants of the matrices S and T, respectively. A two-port measurement setup can be illustrated in Figure C-1:

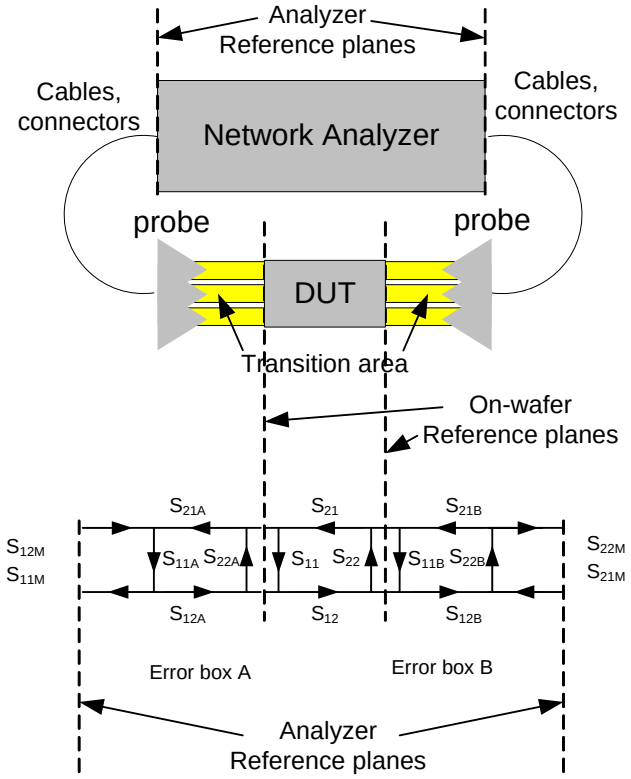


**Figure C-1 Basic model used for TRL de-embedding**

A network analyzer is typically equipped with accurate self-calibration capabilities. The choice of cable, connectors, especially the stability and parasitic characteristics,

plays an important role on the overall accuracy of the measurement. Depending on the specific target of the measurement, the areas where the probes make contacts, as well as areas in close vicinity, can be used as transition areas before the reference planes. The transitions between different areas that the RF/microwave signal goes through are seen as discontinuities and can significantly offset the measured signal. The impact due to these discontinuities can be described with a 10-term error model, where the significant, nonetheless consistent, effects of all the components between the on-wafer reference planes and before the connectors on the network analyzer, on each side of the DUT, are represented by 4 error terms in a scattering matrix:

$$\begin{pmatrix} S_{11i} & S_{12i} \\ S_{21i} & S_{22i} \end{pmatrix} \tag{3.5}$$

The left side of the error matrix is represented by i = A, and the right side i=B. Additional terms, $S_{21L}$ and $S_{12L}$, can also be added to describe the "leakage", or crosstalk between the components across the DUT, as shown in Figure C-2:

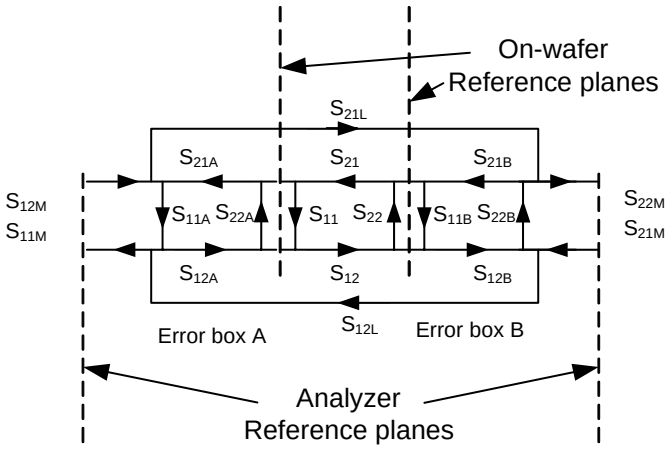


**Figure C-2 Model with leakage across DUT**

The TRL standards are modeled as Figure C-3:

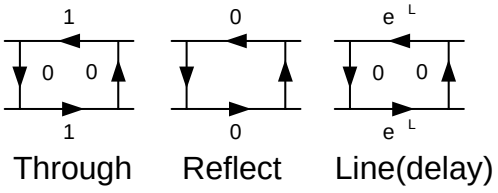


**Figure C-3 Models for TRL standards**

The overall measured system performance can then be written in the form of a cascaded formula:

$$T_M = T_A T_{DUT} T_B \tag{3.6}$$

where the cascadability of T parameters has been utilized. The above equation can be rewritten as

$$T_{DUT} = T_A^{-1} T_M T_B^{-1} \tag{3.7}$$

The fundamental idea of calibration is to use the calibration standards to derive the error matrices and de-embed them from the measured network results of the DUT. With that in mind, the T parameters of the TRL standards can be written as:

$$\begin{aligned} &\text{Through:} && S_{thru} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \\ &\text{Reflect(short):} && S_{11short} = S_{22short} = \Gamma = -1 \\ &\text{Line:} && S_{short} = \begin{pmatrix} 0 & e^{-\gamma l} \\ e^{-\gamma l} & 0 \end{pmatrix} \end{aligned} \tag{3.8}$$

The above equations show that 8 error terms are needed to determine the value of $T_{DUT}$. From the observation that the product of the norms of matrices $T_A$ and $T_B$ is preserved from Eq. (16) to Eq. (17), only 7 out of the 8 error terms are necessary. The through and line standards each gives 4 equations, out of which only 7 are independent, therefore yielding a definitive solution.