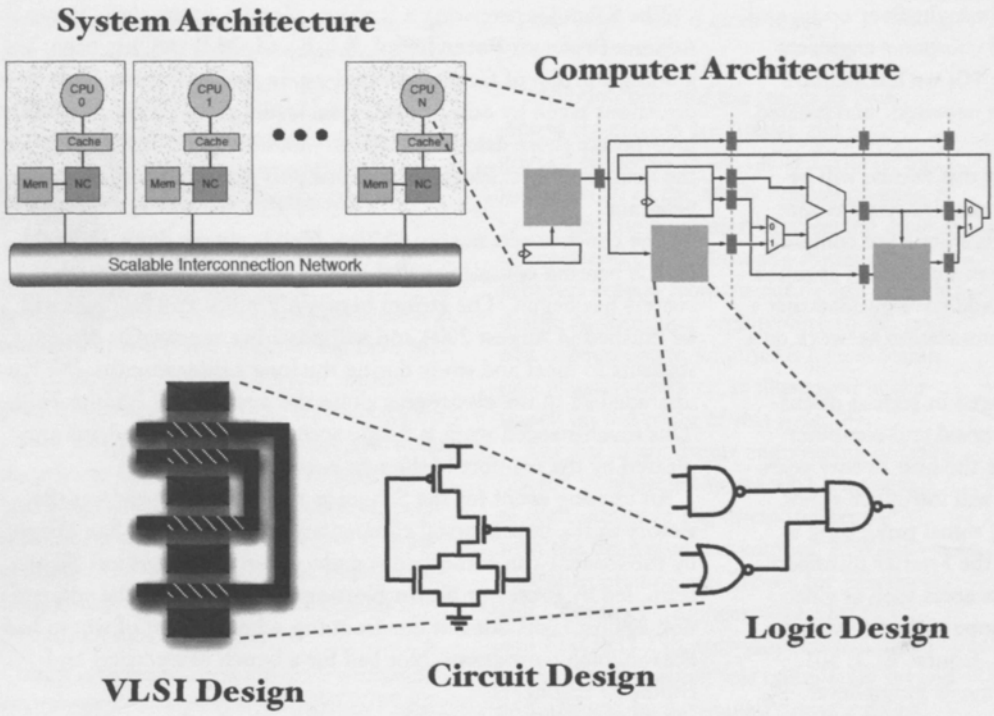
CONNECTIONS

A Report from the School of Electrical and Computer Engineering • Cornell University

Computer Engineering Research

in the School of Electrical and Computer Engineering



Different levels of detail in the design of modern computer systems are shown in the figure, from the physical implementation of computation to the overall system architecture. This logical approach is the core of major revisions now in place in computer engineering instruction and research in the ECE School. Emphasis is placed on the various aspects of computer engineering as experiences that allow the students to progress readily from circuit design, to logic design, to computer architecture, to the eventual desired entity, whether it be solving a problem, performing a laboratory exercise, executing a design project that may lead to a physical product, or conducting thesis research.

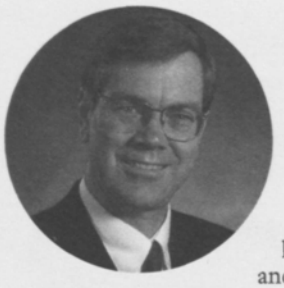
Sketch courtesy of Rajit Manohar.

This 13th edition of *Connections* features the challenging research of our computer engineering research group, updates the history of computer engineering in the EE/ECE School, and considers the impact on the ECE School of revisions in the computer engineering curriculum and of new analytical and experimental techniques in the discipline. The "Positive Feedback" section contains news of recent alumni activities. Other items of interest to alumni are listed below in the table of contents. This year we have again added the "Focus for Excellence" insert for your consideration. When you return the pledge card in the insert please be sure to fill out the activities line. We want to hear what you are up to.

Simpson (Sam) Linke, editor

Spring 2004
In This Issue

Report from the Director



Our faculty takes great pride in the courses that have defined our degree for many years. But in a field that is as dynamic as electrical and computer engineering, the topics need to be adjusted occasionally. In the '60s we saw vacuum-tube physics dropped from the curriculum and replaced by solid-state physics. I would argue that as a result of the transistor, solid-state physics has been defined by electrical engineering for the last 40 years. In the '70s we saw rotating machines dropped from most curricula and replaced by computers. The '80s brought fiber optics and digital technology. We became electrical and computer engineers instead of simply electrical engineers. In the '90s we learned how to connect all these computers together with networks, and created wireless phones, and the web.

Now we are in the "aughties," or whatever this decade will be labeled. We are exploring the new issues of complex systems that are no longer linear time-invariant transfer functions but complex networks that depend on economic and human interaction as much as they depend on Kirchhoff's laws. Who would have guessed that a software "virus" could bring down our communication network or a large part of our power system?

In the past year, the ECE faculty has engaged in serious discussions concerning what it means to be an electrical and computer engineer today. Preparation of a graduate for the next twenty years of his career is a daunting task. Next fall we will introduce a new sophomore course that uses the viewpoint of signal processing to teach the fundamentals of signals, including the Fourier transform. By motivating the course with examples from areas such as video compression or digital communication, we hope to give students early exposure to the excitement of our field. Course ECE 301, Signals and Systems I, will be replaced with a new junior-level course that introduces analytical and computational tools for state-space systems representations, finite-state machines, graph-theoretic approaches to network design and analysis, and examination of concepts of complexity and scalability. Next year I hope we can report on the success of this new sequence in the curriculum.

There have been many notable events within the School during this academic year. We have learned that Professor **Tom Parks,** B.E.E. '61, M.S. '64, Ph.D. '67, along with Professor James H. McClellan of Georgia Tech, will be awarded the 2004 IEEE Jack S. Kilby Signal Processing Medal this summer. This award is a well-deserved tribute to Tom for his major contributions to an important field. The "Recent Faculty Accomplishments" feature in this issue of *Connections* identifies a total of 18 members of our faculty who have received various awards. I am also pleased to announce the promotion of **Lang Tong** to full professor, and the tenure and promotion of **Amit Lal** and **Rajit Manohar** to associate professor. Our enrollments continue to stay healthy. We have over 360 majors between the junior and senior class, plus over 100 M.Eng. students and 188 graduate students working with our faculty. Projections for future enrollments look steady.

The School is preparing a strategic plan for future development. Adjunct Professor **Peter Jessel,** B.E.E. '65, M.S. '66, has been guiding a group of faculty and students in data collection on the directions taken by other schools and leading companies. We will incorporate those data in the design of a hiring and facility plan for the next five years. Please look at our web page for updates on this program.

The construction next to Phillips Hall is almost done. Duffield Hall is nearing completion and occupation by certain research centers has begun. The atrium between Phillips and Duffield will be finished in August 2004 and will provide a spectacular place for students to meet and study during the long winter months. We have upgraded all of the classrooms along the west wall of Phillips Hall. This much-needed work is finally accomplished and students are pleased by the comfort of the new rooms.

An exciting event for the School in this academic year was the victory in the international competition last summer in San Diego by the student-run autonomous underwater vehicle project. The team, led by Professor **Kevin Kornegay,** handily won the competition against eight other teams from top schools, most of whom had oceanographic programs. Not bad for a bunch of electrical and computer engineers!

I thank you for your continued interest in the School. We are entering a time of significant change in the field, and as always would be very happy to hear from you on the state of the field and your reaction to events in the School. With very best wishes,

Clifford R. Pollock
Ilda and Charles Lee Professor of Engineering
Director, School of Electrical and Computer Engineering

Computer Engineering Education Update

by Sam Linke

The growth and impact of computer engineering and technology on the School of Electrical Engineering is well documented in the spring 1992 and spring 1994 issues of *Connections*, and a detailed history of the discipline from its establishment in the School in 1950 to recent times is outlined in the summer 2001 issue of *Connections*. A direct quote from the concluding statements of the latter article states:

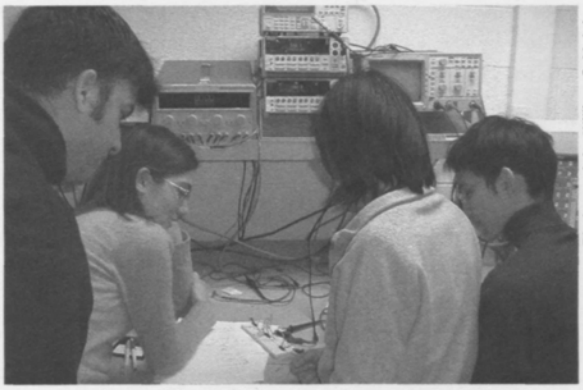
An examination of the advanced courses now offered in the ECE School reflects the profound influence of computer technology on the curriculum. Graduate and undergraduate students who wish to concentrate on computer engineering may choose their electives from a wide variety of available subjects and can augment their studies with appropriate courses offered by the Department of Computer Science.

At about the time that this statement was written, several newly appointed young faculty members with teaching and research interests in computer engineering examined the contents of the then current undergraduate computer engineering courses with a view toward raising the level of instruction in order to become competitive with the best programs offered at competitive institutions. As an example, the *Cornell Courses of Study 1998–99* described the four-credit-hour course ELE E 439 VLSI Digital System Design as follows:

Custom complementary metal-oxide semiconductor/very-large-scale-integrated (CMOS/VLSI) circuit design as seen by a circuit designer. Emphasis on structured design methodologies for digital VLSI systems. Topics include MOS transistors, design rules for MOS integrated circuits, implementation of common digital components, clocking disciplines for VLSI tools for computer-aided design, system design for performance, and novel architectures for VLSI systems.

In contrast, *Courses of Study 2003–04* describes the equivalent five-credit-hour course ECE 474 Digital VLSI Design (revised by Associate Professor **Rajit Manohar**) as follows:

Introduction to digital VLSI design. Topics include basic transistor physics, switching networks and transistors, combinational and sequential logic, latches, clocking strategies, domino logic, programmable logic arrays (PLAs), memories, physical design, floor planning, CMOS scaling, and performance and power considerations. Lecture and homework topics emphasize disciplined design, and include: CMOS logic, layout and timing; computer-aided design and analysis tools; and electrical and performance considerations. Students tape out a small project that is tested in the following semester.



Photograph by William C. Mutch

Figure 1. An experiment in progress in the "Super Lab"

Although many of the topics in both course statements are similar, the pedagogical emphasis in the revised course, and indeed in all of the newly revised courses, is to present the computer engineering courses as experiences that allow the students to progress readily from circuit design to logic design to computer architecture to the eventual desired entity, whether it be a solution or a physical product, as illustrated in the sketch on the cover of this issue.

The list of computer engineering courses offered to undergraduates who may wish to concentrate in the discipline begins with the field-required courses, ENGRD 210, Introduction to Circuits for Electrical and Computer Engineers (see Figure 1), and ENGRD 230, Introduction to Digital Logic Design, which was completely revised and updated by Assistant Professor **Evan Speight,** who has since left Cornell. It was taught this year by Senior Research Associate **Wesley E. Swartz.** Another field-required course, ECE/COM S 314, Computer Organization, was revised by Associate Professor Rajit Manohar and taught this year by Associate Professor **Tony Reeves** and Assistant Professor **Sally McKee**. A two-semester elective course, ECE 474, Digital VLSI Design, was revised by Rajit, who also taught the course during this academic year. The elective course ECE 475, Computer Architecture, was revised by Assistant Professor **Martin Burtscher** and former Assistant Professor **Mark Heinrich** and was taught in the fall 2003 semester by Assistant Professor **José Martínez**. A completely new elective course, ECE 473, Optimizing Compilers (formerly designated as ECE 495), was offered by Martin in the fall 2003 semester. The computer engineering group also offers senior and graduate-level courses that include, among others, ECE 572, Parallel Computer Architecture, taught by José Martínez, ECE 574, Advanced Digital VLSI Design, taught by Rajit Manohar, and a new course, ECE 575, High-Performance Processor Architecture, developed by Assistant Professor Martin Burtscher and taught by him in the spring 2004 semester. A seminar course, ECE 697, Topics in Computer Systems, is conducted by Assistant Professor Sally McKee and staff. Influential papers from the past as well as papers that describe current research and development are discussed.

The conclusion that can be drawn from this brief survey is that computer engineering is now well established in the ECE School as a major entity that is clearly separate from computer science but continues to maintain mutual interactions with that discipline. The courses now contain much more emphasis on the hardware aspects of the technology than in the past, studies stress hardware as well as software issues and devote more attention to the application of microprocessors in system design, and the economic aspects of system complexities are of major concern. All of these factors indicate the existence of a strong computer engineering program at Cornell.

Computer Operations in the ECE School

The mission of the computer operations department in the ECE School is to provide support for all aspects of computer activity in the School based on the use of cutting-edge computer technology. Under the direction of **Robert L. Beaver**, manager of computer operations, this objective is met by establishing a yearly plan that makes optimal use of current facilities and estimates future requirements in both use and acquisition of new equipment. Elements of the plan for fiscal year 2004–2005 are discussed below.

The computing equipment in ECE supported by the department is made up of Microsoft Windows and the UNIX environments Solaris, RedHat Linux, FreeBSD, Mac OS X, Suse Linux, and Fedora Linux. Other systems are available but without an official support policy for their operation. Each person in ECE—faculty, staff, or student—is allowed one username to access the various computing domains. The password for each domain may vary and must meet certain restrictions in complexity. Each person must have a Cornell NetID in order to obtain an ECE computing account and is required to sign a user policy to obtain or to keep an account. Student accounts expire at the end of each semester, but individuals have the opportunity to renew their accounts as needed. Faculty and staff are also allowed ECE e-mail accounts. Student e-mail accounts are not allowed at the present time. All aspects of the computing accounts can be managed by a visit to a specific URL.

The operations department provides daily user support related to computing and network problems or questions. Questions are handled by means of a system known as Request Tracker. While each staff member carries a cell phone and the manager has a land-line phone as well, the preferred method of communicating questions or problems is to send e-mail to a "help" address. A ticket is automatically created in the system that establishes a record of the request and allows an end user to see the status of all requests. Tickets are processed in order based on the number of people affected and in accordance with the following priority order: service outages, requests from the ECE director, university requests, faculty requests, and student requests.

The operations department supports the Microsoft (MS) Windows operating system Windows XP Professional, with the present server environment being MS Windows 2002. Goals for this domain for this fiscal year include: upgrading the server environment to MS Windows 2003, upgrading MS Office XP to MS Office 2003, and creating installation points for all Windows software in the network. Plans are in place for the installation of a system management server (SMS), a set of tools from Microsoft that assists in managing personal computers connected to the network. SMS will enable the network manager to create an inventory of all the hardware and software on the network and store it in a database. Authentication procedure in the Microsoft domain is also scheduled to migrate to a lightweight directory access protocol (LDAP), a set of protocols for accessing information directories.

Planned upgrades for the UNIX environments include migration to LDAP authentication, installation of network servers for Linux and Solaris, arrangement of automatic operating system (OS) updates for Linux, and upgrades of the Solaris operating system to version 9.

The ECE network consists of a fiber cable backbone that can bring 100 MB to 1 GB ethernet connections to desktops in the system. During this fiscal year, migration of the fiber cable to Rhodes Hall moved everyone over to the new network infrastructure. Due to cost concerns and current lack of demand, 1 GB ethernet ports were not installed in every office but connections will be made eventually to every available terminal, and intrusion and security options and a registration management system will be established in the network. An evaluation is in progress on GB needs and plans for switch upgrades to accommodate them, and a procedure is being examined that will provide a simpler method for faculty to determine Cornell Information Technologies' (CIT) network bandwidth charges. There are also plans for faculty and staff to have access to a virtual private network (VPN) that enables the Internet to be used as a medium for the transportation of data. Network service servers, including the domain name system (DNS), are also scheduled for an upgrade. DNS is an Internet service that translates alphabetic domain names into the more functional Internet protocol (IP) form.

The operations department supports seven academic laboratories in the ECE School, three general labs and four academic teaching labs. The general labs are the Sunlab located in Phillips 303 with 20 seats, the Windows lab in Phillips 318 with 60 seats, and the UNIX lab in Phillips 329 with 36 seats. (See page 14 of this issue for a display of the new AMD 64 equipment in this lab.) The four academic teaching labs are located in the undergraduate teaching facility located on the second floor of Phillips Hall, as described in the 1993 issue of *Connections*, but with updated various-model Dell PIV computers. Expansion goals for these labs for this fiscal year include migration of all computers to the ECE domain, migration of printing facilities to the quota management system in the School, and creation of a management account to facilitate maintenance and repair. Older computers from the old Phillips 329 lab will be relocated in an upgraded design lab in the facility.

Ongoing implementation of these planned upgrades of computer facilities and corresponding laboratory equipment augments the revisions in computer engineering teaching and research described in other sections of this issue, and helps to ensure the presence of a strong program in the discipline in the ECE School.

Asynchronous Computer Architecture Research

Directed by Rajit Manohar

The Computer Engineering Research Group

The Computer Engineering Research Group in the School of Electrical and Computer Engineering consists of Professors **Rajit Manohar, Martin Burtscher, José Martínez, Sally McKee,** and their graduate students. The group helped to found the Cornell Computer Systems Laboratory (CSL) that brings together faculty members with common interests from the ECE School, the Department of Computer Science, and the College of Engineering. Research in the ECE School has been augmented in recent months by receipt of major funding from several agencies. Other faculty members with interest in CSL include Assistant Professor **Bradley Minch,** who investigates analog and digital VLSI circuit design, and Professor **Keshav Pingali** of the Department of Computer Science, who has research interests in programming languages and computers for high-performance architectures. The principal research areas of the computer engineering group are described in the following four articles.

The August 2003 major power blackout in the United States is a classic example of a system that normally operates with all of its components acting in synchronism suddenly going into asynchronous mode. The generators in the affected areas pulled "out-of-step" with one another, clocks went awry, and the now incorrect timing mechanisms on protective devices, together with other abnormal functions, caused the transmission grid to split apart with unpleasant results. In this large-scale electric-power domain, clocks depend upon synchronous behavior of the network. In an odd turnabout, the so-called synchronous behavior of integrated electronic circuitry is controlled by clock settings. For certain applications in computer architecture, asynchronous behavior without clocks may be a more desirable mode of operation.

A very-large-scale integrated (VLSI) system today contains hundreds of millions of transistors. These transistors all operate concurrently to perform billions of computations per second. At first glance it may seem that orchestrating the computation being performed by these transistors is an insurmountable task. Over the past few decades, however, VLSI designers have developed a number of organizational principles that enable them to design very complex systems in a systematic manner. These principles also enable them to utilize the transistors effectively, thereby providing the ever-increasing performance that we have come to expect.

One of the basic organizing principles commonly used by VLSI designers today is the notion of a periodic clock signal that coordinates system activity. A chip is partitioned into components, and each component is given a task to perform and a time budget to be determined by the clock period in which it must complete the task. At the end of the clock period, information is communicated between components, and the components can now perform a new computation at the next clock period using information computed in previous periods. This simple idea, while being effective, can also introduce inefficiencies in design. The problem arises because the clock period is programmed to account for the slowest possible task performed by a component. Therefore, if some component finishes early, it must simply wait until the next clock period even though it might otherwise be able to perform useful work.

Since present-day technology scaling is reducing the feature sizes of the devices on a chip, we are now in a regime where the time required for communicating information, as determined by the delay along wires on a chip, is dominating the time it takes to actually compute the values being communicated! With increasing clock frequency (clock periods are now below 350 picoseconds), high-performance microprocessors can even reserve entire clock periods for simply communicating information from one point on a chip to another. Distributing a precise, periodic clock signal to different regions of a chip is also a non-trivial task.

Rajit's group is examining a class of VLSI systems that do not use clock signals for their operation. These asynchronous or clockless VLSI systems do not have some of the limitations previously outlined. The absence of a global clock signal means that the clock distribution problem doesn't exist. Since the activity of components on a chip is not synchronized to a periodic clock signal, each component can execute its task at the fastest possible rate without having to wait unnecessarily. Clockless circuits are also appealing because each component on a chip normally waits for data to arrive and can begin activation without waiting for the clock. Therefore there is no activity in components that do not participate in a particular operation, a condition that leads to a reduction in power consumption.

Elimination of the clock introduces sev-

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Asynchronous Computer Architecture Research

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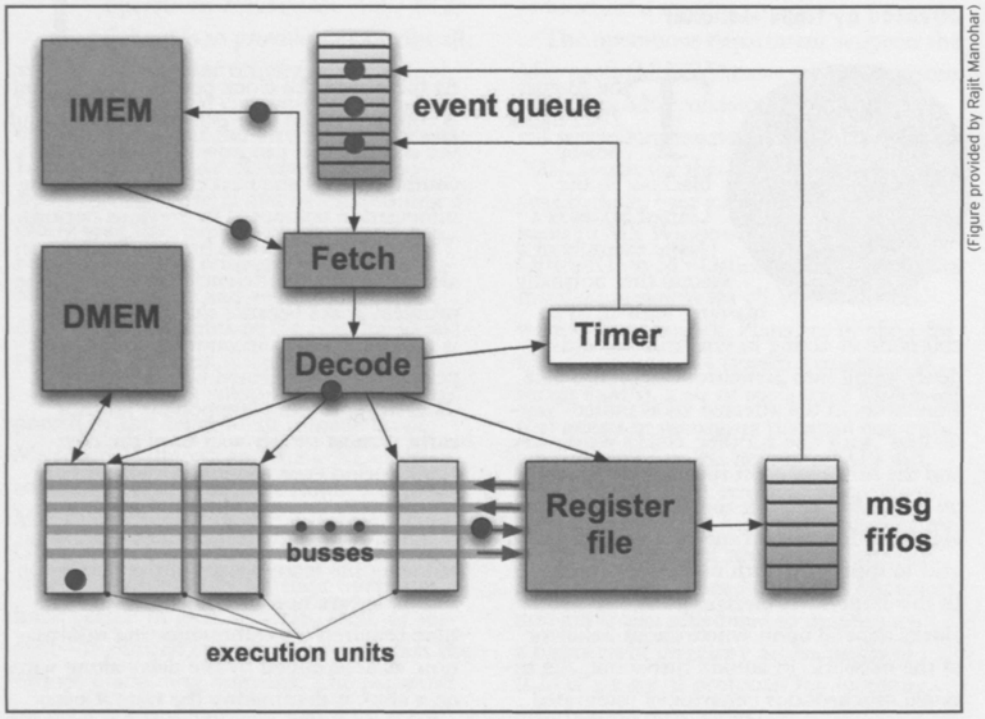

(Figure provided by Rajit Manohar)

Figure 2. An asynchronous processor pipeline with tokens corresponding to instructions being processed. The tokens are indicated by color.

eral challenges that must be addressed to make these systems a reality. The functionality provided by clock synchronization that informs components of data arrival is still required and must be provided by another mechanism. The current technique makes use of the "handshake protocol," which provides both communication and synchronization functions. If a component wishes to send data to another one, it simply sends the data and waits for the receiver to signal its receipt of the information. These data items can be thought of as "tokens" that flow through computation blocks, as illustrated in Figure 2. Once confirmation has been received the component can send the next data value. There are several variations and optimizations possible, but this basic concept is used by all asynchronous VLSI systems. This additional protocol constitutes an overhead cost introduced by eliminating the clock signal. One of the questions under examination is the determination of when the benefits of asynchrony outweigh the overhead costs.

Rajit Manohar, B.S. '94, M.S. '95, Ph.D. '98, all at the California Institute of Technology, and all in computer science, joined the ECE School as an assistant professor on August 15, 1998, and was promoted to associate professor on April 1, 2004. Rajit's research and teaching interests are in asynchronous VLSI design, computer architecture, concurrency, distributed systems, and formal methods. While at Caltech he held a National Semiconductor Corporation graduate fellowship, was a research assistant on studies of asynchronous VLSI, and as an instructor, taught a three-term graduate-level course: Concurrency in Computation. He also served as a student volunteer for Caltech's high-school teacher training program. Rajit, a member of the Institute of Electrical Electronic Engineers and the Association for Computing Machinery, is the co-author of twenty-six refereed journal and conference articles, and is co-inventor of eleven current and pending patents. His teaching assignments include computer organization and digital design, covering aspects of both clocked and asynchronous systems. He is one of the current maintainers of MAGIC, a VLSI layout editor that is used by courses nationwide.

Rajit is one of the founders of the Computer Systems Laboratory (CSL) that brings together faculty with common interests from the School of Electrical and Computer Engineering and the Computer Science Department at Cornell. The Computer Systems area encompasses both experimental and theoretical work growing out of topics in computer architecture, operating systems and compilers, programming languages and environments, distributed systems, VLSI design, and system specification and verification. The interdisciplinary composition of the research teams is one of the strengths of the Computer Systems Lab. Rajit directs the asynchronous VLSI and architecture research group in the Computer Systems Laboratory and uses formal synthesis methods for the design of provably correct, highly concurrent, reliable, and robust asynchronous systems. Some of the recent accomplishments of his group include the design of a high-performance asynchronous field-programmable gate array (FPGA) architecture that is twenty times faster than previously published asynchronous designs, and the design of the first microprocessor optimized for sensor network applications.

High-Performance Microprocessor Architecture Research

Directed by Martin Burtscher

An automatically controlled production line is an essential component of a modern large-scale manufacturing plant, but for proper operation each one of the many elements in the line is dependent upon the correct behavior of every other element in the line. If the operation of just one element is interrupted or delayed, the entire line may slow down or even stall until the difficulty is corrected. In much the same way, the desired seamless operation of a central processing unit (CPU) in a present-day computer system is highly dependent upon the coordinated behavior of a multitude of components and memory elements. For example, an instruction might load a value from the memory and that value activates the next step in the program. If the instruction is delayed, the entire program may be delayed with adverse economic consequences. To alleviate the high cost of such slow main-memory accesses, computer architects have proposed various speculation mechanisms, including a procedure known as load-value prediction. A load-value predictor guesses the result of load instructions, thus allowing dependent instructions to perform their tasks without having to wait for the memory access to complete its function. Unfortunately, costly mispredictions hinder the true potential of load-value prediction. Current microprocessor architecture research at the Cornell Computer Systems Laboratory (CSL) is concerned with building more accurate and faster load-value predictors with little or no extra hardware required.

Accesses to memory, especially loading information from memory, can degrade the performance of a processor in two ways. First, due to advances in the design of CPUs and the lag in corresponding improvement in memory speeds, memory accesses are slow and are becoming slower. Second, memory reads limit the available instruction-level parallelism because instructions based on the result of a load will stall until the memory access is complete, thereby potentially lengthening the critical path of a program. Load-value prediction addresses both problems by predicting the value of a load instruction. Dependent instructions can immediately consume the predicted value and are thus able to execute their assignments concurrently with the memory access. If the predicted value is incorrect, the speculation hardware must perform potentially expensive recovery actions. Consequently, load-value predictors are effective only if the benefit of the correct predictions outweighs the penalty incurred by the incorrect predictions. Prior work has proposed and evaluated a number of load-value predictors. The most sophisticated predictors are hybrids that consist of multiple component predictors and incorporate confidence estimators (see Figure 3). Confidence estimators dynamically decide which loads are worth predicting and filter out loads that are likely to result in a misprediction. Avoiding mispredictions is crucial because mispredicted loads cause recovery actions that slow down the processor. Recent research at CSL has investigated novel approaches to building more accurate and faster predictors, to reducing the size of predictors without degrading their performance, to improving the prediction coverage, and to reducing the predictors' power consumption. The following list summarizes some of the contributions of that work.

Compiler optimizations: Some load instructions are inherently unpredictable while others are unimportant because they do not affect the execution speed of a program. The CSL group has devised the first compiler optimizations to support value-prediction hardware by flagging such loads so that they do not have to be predicted at runtime. Skipping these loads lowers the predictors' power consumption and improves the overall performance because, relatively speaking, more hardware is available to predict the important loads.

Type-based optimizations: Most CPUs support several different load instructions. Some load floating-point values, others characters, and yet others large integer values. The group has been able to improve

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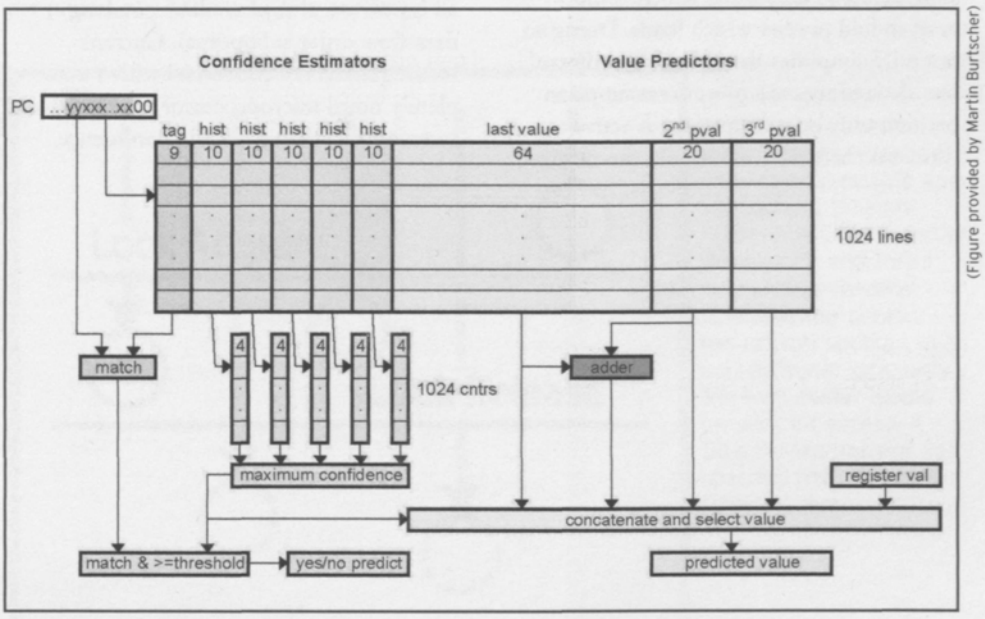

(Figure provided by Martin Burtscher)

Figure 3. A hybrid load-value predictor with confidence estimators.

High-Performance Microprocessor Architecture Research

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value predictors by taking advantage of information of this type, thereby allowing, for instance, detection and avoidance of aliasing in predictor tables. Moreover, loads of different types can be guided to different predictors, each of which is optimized for its type. Both techniques improve the prediction accuracy and reduce the power consumption. In addition, the latter technique reduces the predictor size because the table for character loads, for example, can be designed to be much smaller than that for floating-point loads.

Low-power hybrids: Not all load instructions prefer the same predictor, even among loads of the same type. For example, a 64-bit integer load could fetch a pointer from memory or the length of a vector, two very different values. Hence, it is necessary to combine the strengths of different predictors for best performance, as is done in hybrid predictors. Conventional hybrids use hardware to figure out which component predictor to use by running all components in parallel to detect which one is the best for a given load. This technique not only consumes considerable power but also increases the hybrid's size because each component has to be large enough to handle all loads. The group proposed profile-based and other approaches to determine which component should predict which loads. Doing so not only simplifies the hybrids' hardware but also reduces the power consumption because only one component is active at a time. Furthermore, the hybrid can be sized much smaller because no component needs to be large enough to handle all loads. This, in turn, means that the hybrid can be accessed faster, i.e., it provides its predictions sooner.

Self-optimizing, adaptive hardware: Predictor hardware is very general because it should improve the performance of every conceivable program. However, the speed of some programs may be increased substantially by a different predictor configuration. Moreover, programs go through phases, not all of which prefer the same configuration. Fixed predictor implementations cannot exploit these variations between programs and within programs. The CSL group is the first to devise self-optimizing predictors that reconfigure themselves on the fly to optimize the performance to the current program behavior. This technique outperforms all previously proposed schemes.

Superspeculation: Microprocessors fetch instructions in sequential program order, which unfortunately is not ideal for fast execution. That is why high-end CPUs internally reorder the instructions and execute them in data-flow order, that is, in the order in which the input operands of instructions become available. In the presence of value prediction, potentially all inputs are always available, making data-flow order suboptimal. Current investigations are concerned with a completely novel microprocessor core in which instructions are executed in confidence order, i.e., the instructions whose input operands are the most likely to be correct are executed first. Preliminary results show that such a core is able to deliver never before seen single-program performance.

Martin Burtscher, B.S. '94 (Swiss Federal Institute of Technology (ETH) Zurich), M.S. '96 (Swiss Federal Institute of Technology (ETH) Zurich), Ph.D. '00 (University of Colorado at Boulder), all in computer science, joined the ECE School faculty in July 2000 as an assistant professor. From 1998 to 1999, during his doctoral studies, he first served as head teaching assistant and then as instructor in Data Structures and Algorithms at the University of Colorado at Boulder in the Department of Computer Science. Martin teaches in the area of computer systems and directs his research toward high-performance microprocessor architecture, instruction-level parallelism, and compiler optimizations. Today's high-end, high-speed processors spend a lot of time waiting for memory. Predicting what will have to be done next allows them to execute useful instructions during these idle periods, which can significantly improve their performance. An important focus of Martin's recent research is the design, evaluation, and improvement of predictors to perform this function. He is a member of the IEEE and its Computer Society, the Association for Computing Machinery (ACM), and is the author of eleven refereed journal and conference articles in his fields of interest.

Parallel Computer Architecture Research

Directed by José F. Martínez

Perfect execution of a specific play in a professional football match requires coordination between all eleven members of the team, working in parallel, as it were, with careful attention to timing and signals, complete awareness of the position of each player, clear understanding of each individual's required task, and rapid deployment of counter moves to block actions by the opposing team, the whole synchronized to proceed smoothly to the desired end. While observers of the game may find the successful execution of such a play to be spontaneous, the reality lies in the "architecture" of the play devised by the coaches and in the training of the players. In much the same way, computer architecture, the study of the components that make up computer systems and how they are interconnected, is applied to the construction of software and hardware to produce the huge variety of computer applications of today.

When many computer elements are to be operated in parallel, successful application of the architecture is highly dependent upon proper synchronization of all of the "threads" in a given computer code, where the threads are units of concurrent execution composed of abstract data with instructions to initialize and run them. Programmers achieve synchronization by means of typical operations based on condition codes known as flags, execution barriers, and locks, together with determinations as to whether code sections will be in a race-free situation that may prevent unpredictable results due to multiple-access conditions. It is possible to program the elements of a system to avoid ambiguous operation, but the cost is generally prohibitive. A procedure that involves conservative placement of synchronization operations degrades performance due to unnecessary stalling of the threads. An alternative approach takes an optimistic viewpoint that allows recovery from mistakes as they occur. This new strategy, known as thread-level speculation (TLS), is supported by appropriate hardware that allows threads to speculatively execute their tasks to avoid barriers, busy locks, and unset flags, thereby achieving satisfactory performance.

The following discussion of TLS is a paraphrase of a December 2003 paper by José F. Martínez and Josep Torrellas, "Speculative Synchronization: Programmability and Performance for Parallel Codes," that has been selected to appear in IEEE Micro Top Picks from Computer Architecture Conferences:

Recent research in thread-level speculation (TLS) has produced results that describe a mechanism for optimistic execution of unanalyzable serial code in parallel. The TLS procedure extracts threads from a serial program and submits them for speculative execution in parallel with a safe thread. The goal is to extract parallelism from the code. Under TLS, special hardware checks for cross-thread dependence violations at runtime and forces offending speculative threads to squash and restart on the fly. At least one safe thread exists at all times. While speculative threads venture into unsafe program sections, the safe thread executes code without speculation. Consequently, even if all the speculative work is useless, the safe thread still guarantees that execution moves forward.

Speculative synchronization applies the philosophy behind TLS to explicitly parallel applications. Speculative execution allows application threads to move past active barriers, busy locks, and unset flags instead of waiting. A speculative thread uses its processor's caches to buffer speculatively accessed data, which cannot be displaced to main memory until the thread becomes safe. The hardware looks for conflicting accesses—accesses from two threads to the same location—that include at least one write operation and are not explicitly synchronized. If two conflicting accesses cause a dependency violation, the hardware rolls the offending speculative thread back to the synchronization point and restarts it in flight.

The TLS principle of always keeping one or more safe threads is the key to speculative synchronization (see Figure 4). In any speculative barrier, lock, or flag, safe threads guarantee forward progress at all times—even in the presence of access conflicts and insufficient cache space for speculative data. Two characteristics set speculative synchronization apart from lock-free optimistic synchronization schemes with similar hardware simplicity: always keeping a safe thread, and providing unified support for speculative locks, barriers, and flags. The complexity of the speculative synchronization hardware is modest—one bit per cache line and some simple logic in the caches—plus support

(continued on page 10)

(Figure provided by José Martínez)

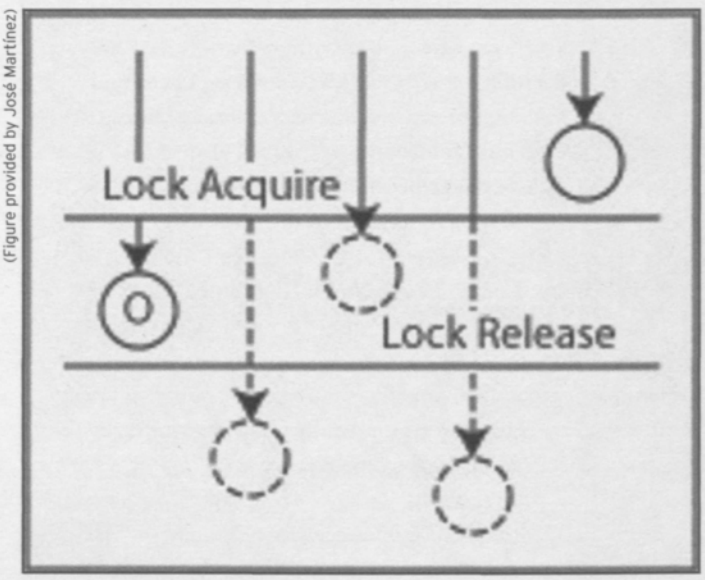

Figure 4. An example of a critical section protected by a speculative lock. Solid and dashed lines represent safe and speculative threads, respectively. Lock owner (labeled O) and three speculative threads concurrently access the critical section. In a conventional lock, only the lock owner would be allowed access. A fifth thread has not yet reached the critical section and remains safe.

Parallel Computer Architecture Research

(continued from page 9)

for checkpointing the architectural registers. Moreover, by retargeting high-level synchronization constructs to use this hardware, speculative synchronization becomes transparent to application programmers and parallel-forming compilers. Finally, conventional synchronization is compatible with speculative synchronization. In fact, the two can coexist at runtime, even for the same synchronization variables. When a set of five compiler and hand-parallelized applications was evaluated for speculative synchronization, the time lost to synchronization was found to be reduced by 34 percent on average.

José F. Martínez, B.S. '96 (Universidad Politénica de Valencia, Spain), computer science and engineering, M.S. '99, Ph.D. '02 (University of Illinois at Urbana-Champaign), both in computer science, joined the ECE faculty on August 15, 2002, as an assistant professor. He is a two-time recipient of the Spanish government's prestigious national award for academic excellence and was a Bank of Spain graduate fellow for four years. In 1998 he was inducted into the Phi Kappa Phi Honor Society for outstanding academic performance. In the ECE School, Professor Martínez is currently teaching computer architecture, parallel computer architecture, and topics in multithreaded and multiprocessor architectures. José is author or coauthor of a number of publications that have been presented in international conferences and symposia on computer architecture, such as Architectural Support for Programming Languages and Operating Systems (ASPLOS), International Symposium on Computer Architecture (ISCA), and the Annual International Symposium on Microarchitecture (MICRO). He is a member of the Association for Computing Machinery and the IEEE Computer Society.

As a member of the Cornell Computer Systems Laboratory (CSL), Professor Martínez's research interests include but are not limited to multithreaded and multiprocessor architectures for high performance and programmability, microarchitecture, and hardware-software interaction. His current research is concerned with speculative shared-memory architectures. The previously discussed TLS procedure has emerged as a promising architectural technology to boost the performance of difficult-to-analyze codes. José has proposed two main contributions of his work to TLS. In the first case a scalable multiprocessor architecture is based on a hierarchical approach that uses largely unmodified speculative chip-multiprocessors (CMPs) as building blocks. In the second case, an application of TLS is used to overcome conservatively placed synchronization in parallel codes. The proposed hardware solutions are quite simple, require no programming effort, and yield performance improvements that are very promising.

ECE School Research Funding

Total research funds expended in 2000-2001	$15,263,499
Total research funds for 2001-2002	$14,435,044
Percent decrease	5.4%
Total research funds expended in 2002-2003	$16,321,630
Percent increase	13.1%

The 2001–2002 research expenditure decreased since 2000–2001 because the school changed the reporting structure for calculation of expended research funds. During the past academic year the school has received gifts and equipment valued at over $4.5 M in support of faculty research, teaching, and special projects. In addition to the National Science Foundation and the Office of Naval Research, some of these sponsors include Sensor Systems, Advanced Micro Devices, BAE Systems, BF Goodrich, Emcore, Fuji Electric, General Electric, GTE/Verizon, Lutron Corporation, IBM, Intel, Microsoft Corporation, Northrup Grumman, Nova Crystals, NxtWave, Rockwell Scientific, RF Micro Devices, Triquent, Tiawan Power, and Zepton Networks. These generous grants from foundations and corporations, coupled with equally commendable gifts from many individuals, aid the recipients in their teaching and research and make it possible for the ECE School to establish and maintain a leading edge in the discipline.

Memory System Architecture Research

Directed by Sally A. McKee

For many years highway transportation in this country has been hampered by the inability of highway construction to keep up with the growing number of automobiles. Introduction of a new superhighway is soon followed by the familiar crowded traffic conditions. This unhappy condition has a direct parallel in computer system development where the rate of improvement in microprocessor speed is exceeding the rate of improvement in memory speed. Indeed, the projected eventual decline in improvement of computer system performance as a result of this bottleneck has become known as "the memory wall." Memory system architecture research attempts resolution of this dilemma by improving dynamic random access memory (DRAM) utilization (see Figure 5), increasing efficiency of high-speed memory storage mechanisms (caches) and decreasing periods of time during which one component in a system is waiting for another component to complete its function (latencies), and by exploiting parallelism at multiple levels, e.g., overlapping memory activity with central processing unit (CPU) activity or allowing more memory requests to be serviced at the same time.

Microprocessor speed is increasing much faster than memory system speed: Since 1987, the microprocessor performance has improved at an average rate of 55 percent per year; in contrast, DRAM latencies have improved by only 7 percent per year, and DRAM bandwidths by only 15–20 percent per year. The result is that the relative performance impact of memory accesses continues to grow. In addition, as instruction issue rates increase, the demand for memory bandwidth grows at least proportionately, possibly even superlinearly. Many important applications, e.g., sparse matrix, large-scale scientific computing problems, and database and computer-aided design (CAD) applications, do not exhibit sufficient locality of reference to make effective use of the on-chip cache hierarchy. For such applications, the growing processor/memory performance gap makes it more and more difficult to effectively exploit the tremendous processing power of modern microprocessors. Applications that suffer most are characterized by complex data structures, large working sets, and access patterns with poor memory reference locality. Examples of such codes can be found in myriad domains where memory stalls can account for the majority of the execution time of applications. Worse, the stall contribution as a fraction of total execution time increases as the performance gap between processors and memory continues to grow. Reduction of this memory stall time improves processor resource utilization, and will allow an application's performance to scale with improvements in process speed and technology.

The traditional approach to attacking the memory system bottleneck has been to build deeper and more complex cache hierarchies. Although caching works well for programs or parts of programs that exhibit high locality, many important commercial and scientific workloads lack the locality of reference that makes caching effective. Industry researchers report that memory bus and DRAM latencies cause processors to be idle up to 65 percent of the time on commercial database workloads, that the efficiency of current caching techniques is generally less than 20 percent of an optimal cache's, and that cache sizes are up to 2000 times larger than the size of an optimal cache. Although more recent computer architecture has produced better latency-tolerating mechanisms, the larger number of instructions in flight can also put more pressure on the memory system, depending on the characteristics of the application. No matter how hard we push it, traditional caching cannot bridge the growing processor-memory performance gap. A promising partial solution is based on the use of memory controllers.

Within the past six years, Professor McKee and her colleague Professor John Carter of the University of Utah, have attacked the memory problem with a unique approach to the memory controller—a general-purpose, uniprocessor system that improves performance within the cache hierarchy and the memory back end for both regular and irregular computations. It does this in three ways: by optimizing the use of DRAM resources in the memory controller backend, by prefetching data within the memory controller and delivering it to the processor only when requested, and by remapping previously unused physical addresses within the memory controller. Extending the virtual memory hierarchy by remapping those physical addresses allows optimizations that improve the efficiency of the system bus. The back end includes a parallel vector access (PVA) mechanism that optimizes the use of DRAM resources by gathering data in parallel within the memory controller. The PVA performs cache-line fills as efficiently as a normal, serial controller and performs strided vector accesses from three to 33 times faster. The scalable design is two to five times faster than other gathering mechanisms with similar goals at the cost of only a slight increase in hardware complexity. Professor McKee is working with Dr. Bronis de Supinski, a colleague at Lawrence Livermore National Laboratory, to develop a new coherence protocol and subsystem to go with remapping memory controllers such that multiple aliases (addresses or names referring to

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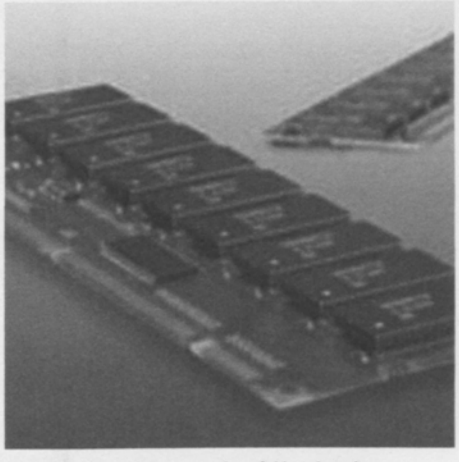


Figure 5. Photograph of the basic component upon which memory-system architectures are built.

Memory System Architecture Research

(continued from page 11)

memory locations) can exist in the system at once. The protocol has the potential to remove the biggest roadblock to the adoption of the memory controller technology developed to date.

Sally A. McKee, B.A. '85 (Yale University), M.S.E. '90 (Princeton University), Ph.D. '95 (University of Virginia), all in computer science, joined the ECE faculty on July 1, 2002, as an assistant professor and became a member of the Computer Science Graduate Field in September 2002. She was also an adjunct assistant professor at the University of Utah School of Computing during the 2002–2003 academic year. She has taught at the University of Virginia, the Oregon Graduate Institute of Science and Technology, Reed College, and the University of Utah, and has worked for Digital Equipment Corporation, Microsoft Corporation, AT&T Bell Laboratories, and Intel Corporation. Professor McKee has been the principal investigator on three National Science Foundation (NSF) projects with one currently in progress. She has participated in studies funded by the U.S. Department of Energy and by the Intel Foundation. As a member of IEEE, she has been active for several years in computer-related activities of the Institute. She is a member of the Advisory Committee of the IEEE Technical Committee on Computer Architecture, and has served as an organizing committee member of 12 international conferences on computer architecture and computing techniques. She is the author or coauthor of over 33 publications in refereed journals and conferences, and is the co-inventor of a U.S. patent. She is also a member of the Association for Computing Machinery, the IEEE Computer Society, the American Association of University Women, and the American Association for the Advancement of Science (AAAS). At Cornell, Professor McKee has received a Faculty Innovation in Teaching Grant and an early career award from the President's Council on University Women. This summer she will collaborate with researchers at the Universitat Politechna de Catalunya under a travel grant from the AAAS/NSF Women's International Science Collaboration Program.

Professor McKee's research interests include computer architecture, and, in particular, memory system architecture; high-performance computing; the interaction of compilers, operating systems, and architectures; hardware/software codesign; performance analysis and prediction; adaptability and accessibility. Her current research focuses on improving memory system performance at all levels. Under a recent award from NSF, along with researchers at Cornell and Georgia Tech, she is creating architectural and operating system-level foundations to enable autonomic high-performance computing systems. Projects under her supervision in the Cornell Computer Systems Laboratory include the design and evaluation of efficient, adaptable, high-performance memory systems and the systems software to exploit them, and the development of metrics and tools for analyzing memory hierarchy performance. In particular, in collaboration with Professor **Rich Caruana** (Department of Computer Science at Cornell), she is examining the application and adaptation of established machine-learning techniques to problems in computer engineering.

Teaching Integrative MEMS

The field of microelectromechanical systems (MEMS) not only crosses many areas of traditional disciplines laterally but also transcends vertically in the level of detail within each discipline. Students need to understand not only electromechanical transduction and microfabrication, but also how to use MEMS to change the world by knowing the experimental and analytical techniques to apply to a solution with the necessary level of detail. The spring 2004 course ECE 432, Introduction to Microelectromechanical Systems, taught by Associate Professor **Amit Lal,** addressed the problem of conveying the inventiveness in MEMS through multiple pathways. First, the lecture material was geared toward fundamental topics such as microfabrication, as well as electrostatic, magnetic, piezoelectric, and thermal effects at the microscale at the chip level. The different energy domains that come into MEMS were used as a way to unify the material. This lecture material, however, does not always translate to the kind of MEMS knowledge conducive to entrepreneurial work in the future.

A second approach allowed the students to gain hands-on experience in MEMS design. They were given access to three different process flows developed by the graduate students in the SonicMEMS group, including processes using bulk micromachining, surface micromachining, and nickel electroplating, all containing capacitive and piezoresistive sensor elements. This access to three processes for the students is unprecedented as far as is known here. The students chose one process flow to fit an idea that they wanted to implement. The student designs, based on integrated-circuit-design software, were fabricated by the four graduate students (**Serhan Ardanuc, Xi Chen, Shankar Radhakrishnan,** and **Abhijit Sathaye**) along with their own designs, and packaged (diced and wire-bonded) onto specially designed pc-boards. The fabricated devices consisted of mature concepts ranging from pressure and acceleration sensors, to more exotic concepts such as magnetic tweezers, optical light valves, microsurgical tools, and electrowetting devices. The students tested their devices and achieved a first-hand introduction to the complexities of packaging and the inaccuracies that occur during microfabrication. This exercise was not only very useful for the ECE 432 students, but also for the graduate students in the group since they were forced to understand their own processes in a very broad sense.

The third aspect of the MEMS instruction was to ask the students to dream up new ways to use micromachining and micromachines. This aspect was achieved by having the students write term papers that addressed a hypothesis of their interest. The resulting papers included MEMS microsatellites for space, micro propulsion, micro-air-balloons, nano-scale channels for molecular characterization, smart bullets, organic power, radioactive power, etc. A poster session was held for students to present the ideas and analyses that addressed their hypotheses.

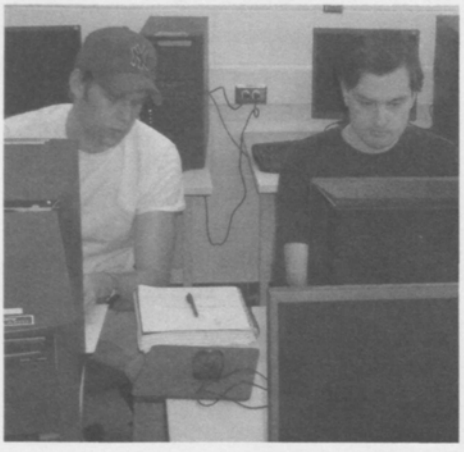
The combination of lecture material, hands-on experience on device design and testing the fabricated devices, along with applying the information to further advance the MEMS field, will hopefully lead to MEMS proliferation in companies in which the students will be employed to solve real-world problems.

Broadband Communications Research

The Cornell Broadband Communications Research Laboratory (CBCRL) in the ECE School was established to develop fundamental knowledge of the devices and circuits that occur in broadband communications systems by study of issues that impact the design of high-performance energy-efficient systems. Associate Professor **Kevin Kornegay,** director of the laboratory, leads a high-energy research group, consisting at present of 13 Ph.D. students and research staff who develop creative device and integrated-circuit solutions to design requirements set by the high standards that will be demanded of the next generation of wired and wireless communication systems. Typical applications are cellular telephone systems, high-performance networking, and optical communications. Among other goals, the research could lead to smaller and lighter devices with improved data rates and reduced power consumption. The research is supported by corporate and government sponsors. Corporate sponsors include Agilent, Cadence, Cascade-Microtech, Compaq, IBM, Intel and Qualcomm. National government and local sponsors are NSF, DARPA/MARCO (a subsidiary of the Semiconductor Research Corporation (SRC)), and the New York State Office of Science, Technology and Academic Research. A recent $200,000 gift from Qualcomm, Inc., will provide three new graduate student fellowships. A team of CBCRL graduate students won third place in the 2002–2003 SiGe (Silicon Germanium) Design Challenge, sponsored by the Semiconductor Research Corp. (SRC). Their project, entitled "A 10 Gb/s Integrated Optical Transceiver," is a good example of the research performed by the CBCRL group.

"Bleeding-Edge" Computer Technology

Director **Pollock,** at left, with **Abeezer S. Tapia** '02, AMD product marketing manager, center, and **Stephan G Meier** '89, AMD senior architect, at the AMD equipment donation ceremony in Phillips Hall on February 19, 2004.



A test run of the new AMD laboratory workstations.

Each AMD computer has a matching SONY liquid-crystal-display (LCD) monitor.

A recent donation of 40 top-of-the-line computers by Advanced Micro Devices (AMD) satisfies an urgent need for high-performance computing facilities in the ECE School. The computers, based on AMD Athlon 64-bit 3000+ processors with matching Sony liquid crystal displays (LCD), are located in Phillips Room 329, as shown on this page. The laboratory is designed principally for sophomores and juniors who take ECE 314, Computer Organization, a course that is required for all ECE and computer-science majors. The new facility will also support course ECE 475, Computer Architecture, course ECE 547, Computer Vision, and other courses requiring circuit and /or chip design.

It would appear that acquisition of these computers now places the School at the "cutting edge" of computer technology. Because of the highly advanced design of the new equipment, perhaps it is better to designate the AMD laboratory as being beyond the cutting edge and operating at the "bleeding edge." In that sense, the new computers will give students much greater computational ability and will also challenge them to devise ingenious solutions to problems that may occur due to possible instabilities of the novel 64-bit processors. Similarly, a comparison of the now well-established hybrid electric vehicle with the projected fuel-cell-powered auto suggests that the latter has many promising features but still "needs work," again an example of bleeding-edge technology.

Photographs by William C. Mutch

Students examine the new AMD laboratory equipment. **Robert L. Beaver,** ECE manager of computer operations, is standing at left.

Recent Faculty Accomplishments

Excellence in Teaching awards were announced at the College of Engineering Fall 2003 Awards Ceremony on November 6, 2003, in the Memorial Room of Willard Straight Hall.

All award recipients in the School are designated by a colored square (■).

■ Assistant Professor **Alyssa Apsel** (opto-electronic very-large-scale integrated systems), the Clare Boothe Luce Assistant Professor of Electrical and Computer Engineering, has been developing her research group and facilitating industry interactions with Agiltron, Lockheed Martin, and IBM corporations. During this academic year she was granted a CAREER award from the National Science Foundation for her proposal "Designing with Light: Comparative Analysis and Design of Optical Interconnects for Chip-to-Chip Communication," received a $50,000 award from the 2004 Lockheed Martin University Research Grants Program for her project "Resonant Monolithic Photodetectors and On-Chip Waveguides for Integrated Optoelectronics," and was asked to act as an associate editor for *IEEE Transactions on Circuits and Systems II*.

• Professor **Joseph M. Ballantyne** (opto-electronic devices and materials) has been on a leave of absence during the 2003–2004 academic year in Jerusalem, Israel.

■ Lecturer **John C. Belina** (bioelectronics) assistant director of the ECE School, was faced in the fall semester with a 40 percent increase in class size in course ECE 210, Introduction to Circuits for Electrical and Computer Engineering. More solid-state material was added in the course to prepare students for course ECE 315, Introduction to Microelectronics, in the spring term with Professor **J. Richard Shealy**. This move seems to have been successful according to student feedback, and it eased the transition to ECE 315's more intense treatment of devices. A significantly enhanced ethics component was added to ECE 210 this fall with the assistance of Professor **Ronald R. Kline** and **Park Doing**, B.S. '88, M.E.E. '93, post-doctoral associate in Science and Technology Studies. A videotape of the class discussion was made to help meet Accreditation Board for Engineering and Technology (ABET) direct evidence requirements. In his work with course ECE 402, Biomedical Instrumentation Design, a culminating design experience (CDE), John worked to significantly increase student exposure to the ABET design requirements, including the "Professional Components." This spring the design phase was moved ahead two weeks to deal with the end-of-the-semester workload issue of students in multiple CDEs so as to allow them more time for final report writing.

John was named by graduating senior and Merrill Presidential Scholar **Paul Anthony George** as the Cornell faculty member who made the most significant contribution to his college education and experience.

• Professor **Toby Berger** (information theory and communications), the Irwin and Joan Jacobs Professor of Engineering, was on sabbatical leave during this academic year at the University of Virginia in Charlottesville in the fall term and at Harvard University in the spring, where he taught new courses, made new research associations, gave several talks, and arranged for visits thereto by his graduate students. Toby continues to give presentations at major conferences and deliver invited lectures at several prestigious institutes concerning the interface between information theory and neuroscience. His work in this area has gained increasing recognition by the neurosciences community while simultaneously leading to new information-theoretic investigations into novel channel models. Toby is a co-principal investigator with **Sergio Servetto**, **Lang Tong**, and **Stephen Wicker** on the new National Science Foundation grant in the ECE School on wireless sensor networks.

• Associate Professor **Adam Bojanczyk** (computer engineering, parallel architecture, and algorithms for signal and image processing) has developed an algorithm for computing the total least-square solution to the orthogonal Procrustes problem.

■ Assistant Professor **Martin Burtscher** (computer systems, microprocessor architecture, compiler optimizations) was the recipient of a Michael Tien '72 Excellence in Teaching Award in 2003, became the principal investigator of a National Science Foundation Information Technology Research grant, and continued his research on his grant from Intel Corporation. During this academic year Martin diversified his research into compression and micro-architectural speculation, designed a new senior-level computer engineering course on high-performance processor architecture, and taught the course for the first time in the 2004 spring term.

• Professor **Hsiao-Dong Chiang** (analysis and control of nonlinear systems with applications to electric-power networks) has filed two USA and Patent Cooperation Treaty (PCT) patent applications on a nonlinear-indices-based lung-cancer diagnosis system now under extensive testing at a large hospital. He has also filed one PCT and Japanese patent jointly with Tokyo Electric Power Company, Tokyo, Japan, on a boundary controlling unstable (BCU) equilibrium point method for direct power-system transient stability. Hsiao-Dong is considering filing a patent application, through the Cornell Research Foundation, for his design of a novel paroxysmal atrial fibrillation identification system that achieves very high diagnosis sensitivity with acceptable specificity and requires very short duration, say 30 minutes, of heart rate variability (HRV) signals. He is also developing a dynamical trajectory-based global optimization methodology for solution of general nonlinear problems.

■ Associate Professor **David F. Delchamps** (control and system theory) was on sabbatical leave during the spring 2003 semester and spent much of the period studying game theoretical reasoning (coupled with dynamical-systems ideas and insights from the theory of mechanism design) to problems in the theory of evolutionary computation and to more general problems in the modeling and analysis of systems involving many interacting agents with limited shared information and conflicting objectives. He is planning to teach a new 400-level course in fall 2004 that addresses subject matter from the area(s) he has been exploring. During this academic year David has taken on a somewhat major new position as faculty co-chair of the Fraternities and Sororities Residential Initiative Programming Council. His principal responsibility in that position is to facilitate and promote faculty involvement with the Greek system along the lines of the Faculty Fellow and House Fellow programs associated respectively with the North and West Campus components of the Residential Initiative.

David was selected by members of the IEEE Student Branch to receive the 2003–2004 Professor of the Year Award.

■ Professor **Lester F. Eastman** (compound semiconductor materials, devices, and circuits), the John LaPorte Given Professor of Engineering, received the 2003 IEEE Microwave Theory and Technique Society Distinguished Educator Award. In recent research Lester has determined the lifetime of longitudinal optical phonons in high electric fields, for various (Ga) AlN/GaN heterojunctions. This is the key parameter, ranging from 350 to 800 femtoseconds, that limits electron channel velocity. This research was done in cooperation with Prof. Matulionis of Vilnius, Lithuania, with students **Yun-Ju Sun** and **Alexei Vertiatchikh**.

• Professor **Donald T. Farley** (radiowave and upper atmospheric physics), the J. Preston Levis Professor of Engineering, began phased retirement in July 2003. He still teaches a large course load in the fall semester, but does not teach in the spring, a pleasant arrangement that allows him to spend more time on research. This past semester Don prepared for NSF panel reviews of the Jicamarca Observatory in Peru and related activities, gave two invited lectures in Peru (one in Spanish), and is scheduled to give an invited talk in July in the United Kingdom.

(continued on page 16)

• Professor **Terrence L. Fine** (information theory, inference, and decision making in the presence of uncertainty), director of the Center for Applied Mathematics, has proposed revisions of the ECE undergraduate systems curriculum that effect a much-needed modernization of our basic systems curriculum, and, in so doing, also narrow the wide gap between electrical engineering systems and computer engineering. In this academic year two of Terry's Ph.D. candidates completed their studies, and he had two refereed journal papers accepted for publication in *IEEE Transactions.* A fall 2003 sabbatical enabled him to complete and send to Prentice-Hall his undergraduate textbook *Probability and Probabilistic Reasoning for Electrical Engineering and Computer Science.* The sabbatical also provided time for two weeklong visits to discuss research on the foundations of probability and to present invited talks. Progress was, and is, being made on his concept of chaotic probability for objective frequentist random phenomena.

■ Associate Professor **Zygmunt J. Haas** (wireless communication and networks, mobile systems) was the 2003 recipient of the Michael Tien '72 Excellence in Teaching Award and also received the Highly Commended Paper Award at the IEEE International Conference on Advanced Information Networking and Applications (AINA 2003) at Xidian University, Xian, China, March 27–29, 2003.

He was also reselected as IEEE Expert Lecturer for the IEEE Communications Society for 2002–2003 and 2003–2004. Zygmunt reports that in the past year, his group has made substantial progress in research on wireless networks scalability. In particular, both upper and lower bounds have been developed under most general conditions and the research has shown that the bounds are tight. These results are of significant importance to the sensor networks community; many researchers have expressed interest in this work and have asked for publication preprints. The group has also developed a scalable network simulator of hundreds of thousands of nodes (a capability that is orders of magnitude larger than that of any tool publicly available until now). Again, the interest from the ad hoc networking community has been well above the expected level. Current goals in research on Security of Ad Hoc Networks have been completed and substantial progress has been made in the area of applications of the ad hoc networking technology to biosystems.

■ Professor **David A. Hammer** (plasma physics, controlled fusion, intense ion beams), the J. Carleton Ward, Jr. Professor of Nuclear Energy Engineering, has been selected to receive the 2004 Plasma Science and Applications Award from the IEEE Nuclear and Plasma Sciences Society. David is being recognized by the society "for fundamental contributions to the understanding of intense relativistic electron beam propagation, intense ion-beam generation and propagation, innovative plasma diagnostic development for intense beam devices, x-ray source development using novel plasma pinches, and for his commitment to the mentoring of graduate students in the field of plasma science." This prestigious award is presented annually to an individual who has demonstrated "outstanding contributions to the field of plasma science." In recognition of this award, David will present a plenary address at the 2004 IEEE International Conference on Plasma Science in Baltimore in June. In research, David reports determination of the X-pinch x-ray source size through the Ph.D. thesis work of **Byungmoo Song.** This source is approximately one μm in size and therefore required novel measurement methods to be developed and implemented after standard measurement methods proved inadequate for such a small source. In another duty as program chair of the American Physical Society Division of Plasma Physics Meeting, October 27–31, 2003, David organized a five-day meeting involving 1,675 papers and approximately 1,550 people. Dave has also been elected the vice chair of the Division of Plasma Physics of the American Physical Society (APS/DPP). He had responsibility for the program of the annual meeting of the APS/DPP in November 2003. From November 2003 to November 2004, he is chairing the division.

■ Associate Professor **Sheila S. Hemami** (application-specific compression techniques for packet networks, networking aspects of visual communication, and multirate coding and transmission) has been active this academic year with IEEE affairs. She was appointed associate editor of the *IEEE Transactions on Signal Processing* and is also a member of the Image and Multidimensional Signal Processing Technical Committee of the IEEE that includes program committee membership for both IEEE International Conference on Image Processing and IEEE International Conference on Acoustics, Speech, and Signal Processing. In student activities, Professor Hemami helped organize an information session for undergraduates on procedures for applying for NSF graduate fellowships, and has written recommendation letters for ten undergraduates (a total of perhaps 60 letters) for various fellowship and graduate programs.

Professor Hemami received the 2003–2004 Ruth and Joel Spira Excellence in Teaching Award.

• Professor **C. Richard Johnson, Jr.** (adaptive control and signal processing) has received NSF funding for a three-year grant on blind adaptive channel shortening that is useful in multicarrier communication. Rick has also established multiyear (through 2006) interaction with French researchers P. Duhamel at Supélec École Supérieure D'Électricité and P. Regalia at l'Institut National des Télécommunications in ultrawideband receiver design and composite adaptive systems approach to receiver design.

■ Associate Professor **Edwin C. Kan** (modeling and fabrication of nanometer-scale devices) received the 2003 Robert '55 and Vanne '57 Cowie Excellence in Teaching Award. During this academic year Edwin's research group has made a number of significant developments in several areas of interest. A new chemoreceptive scheme has been pioneered for a complementary metal-oxide semiconductor (CMOS) interface to sense and actuate molecules in air and liquid based on nonvolatile charge in floating gate structures. Integration of carbon-based or nanowire-based structures on a silicon substrate provides another avenue of design optimization for which the group has been developing new techniques mainly on sensor applications. For nonvolatile memory scaling, the group has pioneered development of metal nanocrystal memories, a promising technology that will reduce memory hierarchy and provide portable, low-cost, large-volume, and fast-access memory systems. For transistor scaling, the group has worked on novel devices and circuits built from independently driven double-gate MOS field-effect transistors. New circuit topologies have been constructed for dynamic threshold and gain, internal feedback, cascade reduction, and adiabatic switching, which have distinctive advantages in power and speed over single-gate operations. In architecture, pulse-wave interconnects have been proposed that change the information representation from potential levels to pulses and hence provide much improved scaling behavior for delay and power of global interconnects.

• Professor **Michael C. Kelley** (upper atmospheric and ionospheric physics), the James A. Friend Family Distinguished Professor of Engineering, published his work under the 2002–2003 Fulbright Scholarship to the physics department at the University of Crete in Greece. Mike also completed work as a National Academy of Sciences committee chair with the responsibility of creating a ten-year vision for the field of atmosphere-ionosphere-magnetosphere science. The report has been reviewed, accepted, and published.

■ Professor **Paul M. Kintner** (atmospheric plasma physics) has been elected a fellow of the American Physical Society. He was recognized for his "investigation of microstructure, wave-particle interactions, and plasma acceleration in space plasmas using sounding rocket and satellite experiments and for innovative applications of global positioning systems (GPS) technology to space plasma experiments." On January 22, 2004, at 08:57 UT, Paul successfully launched the SERISO sounding rocket (see Figure 6) from Svalbard, Norway. In other research he obtained a patent for making GPS software receivers practical, and continued leading NASA's Geospace Mission Definition Team toward implementation of a satellite program. In preparation for the next ABET visit, Paul wrote the first draft of the ECE ABET Self-Study Questionnaire.

• Professor **Ronald M. Kline** (history of technology and electrical engineering) significantly extended the Bovay Program in the History and Ethics of Engineering by hiring post-doctoral associate **Park Doing,** B.S. '88, M.E.E. '93, giving ethics seminars in ENGRG 150 (500 students) and other courses, and creating a web site about the activities of the program (http://bovay.ece.cornell.edu). Ron continued his work on a book-length project on the history of information theory and cybernetics.

■ Associate Professor **Kevin T. Kornegay** (computer-aided design for VLSI circuits) has been awarded the provost's Ronay and Richard Menschel Award for Distinguished Scholarship for 2004. This award is in recognition of Kevin's strong research program in RF and VLSI circuits,

(Photograph by Steven P. Powell)

Figure 6. The SERISO sounding rocket payload with Cornell ECE faculty and students, Dartmouth Physics faculty and students, and NASA technicians. Professor Kintner is kneeling at lower left.

his mentoring of the ECE faculty, and his active involvement with student groups, especially the world champion autonomous underwater vehicle team. Kevin also received a 2003–2004 IBM Faculty Award, a highly competitive honor that recognizes the quality of his research program and its importance to IBM. The award was presented by the IBM Austin Center for Advanced Studies. Last year the Chicago Museum of Science and Industry selected Kevin for an exhibit that showcases contributions made by African Americans to the field of information technology. This exhibit is the centerpiece of the annual Black Creativity Program, and was on display from January 15 through March 1, 2003. The exhibit included a biography of Kevin and an account of his research on broadband communications systems. His autonomous underwater vehicle was also featured together with information about his student team at Cornell. A paper by Kevin's research group was selected by the Technical Program Committee of the Device Research Conference as one of the two best student papers for 2003. The formal award will be presented at the 2004 Device Research Conference at Notre Dame, Indiana, in June.

• Associate Professor **Amit Lal** (application of ultrasonic pulses to microelectromechanical systems (MEMS)) was promoted to associate professor in the School effective April 1, 2004. Amit reports achievement of 1 kHz linewidth for a micromachined silicon cell, a development that allowed his group to progress to Phase II of the chip-scale atomic clock program with a corresponding achievement of 2 percent energy conversion efficiency from radiation to electrical energy output. The group also demonstrated closed-loop control of silicon surgical tools. Amit developed lecture notes on radio frequency-MEMS for the 2004 spring term as part of course ECE 598, Contemporary Topics in Micromachined Microsystems, and added bipolar-junction transistor and diode laboratory components to course ECE 315, Introduction to Microelectronics, to make the lab more compatible with the increase in devices in the curriculum.

• Assistant Professor **Michal Lipson** (nanophotonics, optical nanostructures, optical telecommunications) reports receipt and maintenance of a research funding level of approximately $700,000 per year. Professor Lipson and her group have shown that the challenges to silicon nanophotonics are now being removed, so that the dream of all-optical circuitry is being brought closer to reality. In developments that have been demonstrated in the laboratory and reported in appropriate journals, the group has developed approaches for light coupling, guiding, switching, and modulation on silicon based on sub-micron-size highly confined structures. It is primarily this principle of manipulating light by confinement that has enabled the group to control light on silicon. The group was featured recently in the trade journal *EE Times* with an article on their work on techniques for making photonic microchips in which streams of electrons are replaced by beams of light. Her group's biggest accomplishment this year was the demonstration of an "optical solder" coupling light between a micro-scale fiber and a nanoscale waveguide. A paper on this topic is forthcoming in *Optics Letters*. In course ECE 437, Fiber and Integrated Optics, Professor Lipson has introduced a hands-on final project in which the

(continued on page 18)

students design and characterize "photonic chips." The lab is first of its kind at Cornell and is unique also among the top universities in this country.

• Associate Professor **Rajit Manohar** (asynchronous VLSI design, computer architecture, parallel computing) was promoted to associate professor in the School effective April 1, 2004. Rajit reports progress on the thesis research of several of his graduate students with topics including: energy-efficient architectures for sensor networks with design of the first sensor network processor for that project, mechanisms for energy-efficient asynchronous multiprocessor systems, highly non-deterministic dynamically scheduled architectures for asynchronous computation, fault-tolerant asynchronous circuits, and fault-tolerant architectures (joint with José Martínez). He expects to have test data for the first processor designed for sensor networks by the end of this summer, as well as data from the field programmable gate array (FPGA) design.

■ Assistant Professor **José Martínez** (multiprocessor architectures, microarchitecture, and hardware-software interaction) was selected to appear in IEEE Micro 2003 Top Picks from Computer Architecture Conferences. His paper, titled "Speculative Synchronization: Programmability and Performance for Parallel Codes," was one of 15 that were judged to have had a major impact on the field. José has been invited to join a program committee of a top computer architecture forum. He has also secured funding for equipment from Intel Corporation.

■ Assistant Professor **Sally A. McKee** (computer architecture, memory system architecture, high-performance computing) has received several awards during this academic year including a National Science Foundation Information Technology Recearch Award, a 2003–2004 Cornell President's Council on University Women Affinito-Stewart Award, and a 2003–2004 Cornell Faculty Innovation in Teaching grant that allowed her to create a new course, ECE 595, Real World Engineering, for master of engineering students headed for industry. Professor McKee initiated a productive collaboration with CS Professor **Keshav Pingali's** Intelligent Software Systems group that has resulted so far in one workshop paper and another paper in preparation. She has obtained funding from Intel Corporation and maintains active collaboration with Lawrence Livermore National Laboratory in California as well as with Technische Universität München in Germany.

■ Assistant Professor **Bradley A. Minch** (analog and digital VLSI circuit design) was named the 2002–2003 IEEE Outstanding Professor of the Year for his work on the course ECE 315, Introduction to Microelectronics.

■ Professor **Thomas W. Parks** (signal theory and digital-signal processing) has been named as a co-recipient of the 2004 IEEE Jack Kilby Signal Processing Medal, along with James McClellan, "for fundamental contributions to digital filter design and interpolation, especially for Parks-McClellan algorithm." The award consists of a gold medal, bronze replica, certificate, and a cash honorarium. Tom and his group have developed new algorithms for digital cameras. They worked with Texas Instruments Corporation to demonstrate the effectiveness of their algorithms in actual digital cameras.

• Professor **Clifford R. Pollock** (lasers and optoelectronics) the Ilda and Charles Lee Professor of Engineering and director of the School of Electrical and Computer Engineering, taught a section of course ECE 315, Introduction to Microelectronics, each week and enjoyed helping with the lab projects and especially talking to the students about the courses and plans. In research, Clif's group set up a femtosecond optical parametric oscillator and will begin exploring its use as a short-range (micron resolution) radar system for probing optical structures.

■ Assistant Professor **Farhan Rana** (semiconductor optoelectronics, device physics, ultra-fast optics, and quantum optics) received a National Science Foundation Faculty Early Career Development (CAREER) award of $400,000 for his proposal, "Semiconductor Lasers for Generating High Energy Ultrashort (sub-50 femtosecond) Optical Pulses: From Nanotechnology to Ultrafast Optics." During his first year at Cornell, Farhan has been setting up a research group in semiconductor optoelectronics. A large portion of the effort was devoted to bringing in sponsored research grants, setting up laboratories for semiconductor optoelectronics research, and developing the necessary course work for students interested in his research area. He developed two completely new courses related to semiconductor optoelectronics, quantum optics, and quantum electronics.

• Associate Professor **Anthony P. Reeves** (parallel computer systems, computer-vision algorithms) reports that the main achievements during this academic year result from the ongoing collaboration with **C. Henschke** and **D. Yankelevitz** at the Weill Medical College. Starting from the group's leadership position in research for lung cancer screening, progress has been made in a number of areas: The group has developed the ELCAP Management system (EMS), a unique central secure web-accessible database facility for managing lung cancer clinical trials that includes the capability of managing patient-specific information and medical images in a single environment.

The group is in the middle of the NY-ELCAP multi-center trial involving 13 different medical institutions that are all using the Cornell protocol and are sending computed tomography (CT) images to Cornell using the EMS. An international consortium, I-ELCAP, has been extended to pool data for lung-cancer research using the EMS. Twenty active sites are in this project including international collaborations from Israel, Spain, Italy, Switzerland, and France. Institutions from China and Canada are in the process of joining the project. The French national trial on screening for lung cancer (involving 10 sites) has adopted the EMS for their pilot study and a French language version of the system has been developed for their use. The group is participating in the National Institutes of Health Lung Image Database Consortium and on the EU/US spiral CT collaborative group to promote research in screening for the lung-cancer area and to provide a national database for test algorithms for computer-aided diagnosis of lung cancer. The research collaboration agreement with General Electric Company for lung-cancer management computer-aided design gives GE an exclusive use of the group's patents and the group will receive royalties from GE's products in this area. GE now has a product for lung cancer analysis that is based on these patents. Applications for new patents have been made this year on computer methods for pulmonary nodule characterization and detection. A set of results on computer methods for lung-cancer detection that is one of the first to achieve a practical false positive rate, was presented at the Radiological Society of North America conference this year.

• Assistant Professor **Anna Scaglione** (statistical signal processing, communication theory) was elected to membership in the IEEE Signal Processing for Communications Committee. Professor Scaglione is associate editor for *IEEE Transactions on Wireless Communications*, and was co-guest editor of the *Communication Magazine Special Issue on Power Line Communications.* In December 2003, she was a participant in the "NSF Workshop on Distributed Communications and Signal Processing for Sensor Networks."

■ Assistant Professor **Sergio D. Servetto** (networks, information theory, signal-processing applications) received a National Science Foundation Faculty Early Career Development (CAREER) award in 2003. He is a member of four IEEE technical committees on communication theory, four technical program committees of the Association of Computing Machinery, and also serves on an Information Processing on Sensor Networks Workshop technical committee. Sergio is one of the guest editors for a special issue of the *IEEE Journal on Selected Areas in Communications* on the topic "Fundamental Performance Limits of Wireless Sensor Networks."

• Professor **Charles E. Seyler, Jr.** (space plasma physics, theoretical and computational plasma physics), associate director of the ECE School, continued with ongoing curriculum revisions in the sophomore, junior, and culminating design experience courses, monitored progress of preparations for the upcoming ABET review, and continued in the development of course ECE 210, Introduction to Circuits for Electrical and Computer Engineers, by tightly integrating the lecture theory with fundamental laboratory analysis and design. In research, Charles continued with the development of advanced simulation models for study of auroral physics and to compare the results with recent data from multipoint satellite measurements.

• Professor **J. Richard Shealy** (development of compound semiconductors) served as a reviewer for *Applied Physics Letters, Electronics Engineering Texts, Transactions on Quantum Electronics, IEEE Transactions on Electronics & Electron Devices, Journal of Applied Physics, Journal of Crystal Growth*, and for National Science Foundation proposals.

• Professor **Michael G. Spencer** (growth of compound semiconductors and fabrication of discrete devices from these materials), director of

graduate studies in the School of Electrical and Computer Engineering, reports that his group has made several achievements in multiple areas of materials- and device-related work. In the characterization of GaN materials, the properties of GaN and related materials have been measured by means of Scanning Kelvin Probe Microscopy. This effort has resulted in several publications and presentations. The group has fabricated some of the world's best SiC microwave devices. The need for a heterojunction in these devices has been identified in order to improve their performance, and the group is currently working on the fabrication of such a device. The group has produced a process for the growth of bulk GaN materials. A patent disclosure on this process has been produced and first publications have been submitted. In collaboration with investigators at Wadsworth Laboratory, the group is developing a bio-mimetic sensor to detect toxins. This sensor is based on controlling ion channels imbedded in a lipid bilayer that mimics cell function. Initial fabrications have been made of test structures that are designed to measure fundamental properties of these devices.

• Professor **Chung-Liang Tang** (lasers, optoelectric devices, nonlinear and coherent optical processes), the Spencer T. Olin Professor of Engineering, reports that he has revised a draft of a comprehensive text book on quantum mechanics for solid-state and quantum electronics. This book is under contract with and will be published by Cambridge University Press.

• Professor **Robert J. Thomas** (control techniques for large-scale networks, analysis of microelectromechanical systems), director of the NSF Power Systems Engineering Center (PSerc) at Cornell, was on assignment to the U.S. Department of Energy in the fall semester of the 2003–2004 academic year. During that time he participated in the strategic planning for the new Office of Electric Transmission and Distribution and in the task force study of the August 14, 2003, blackout, wrote position papers and gave talks on behalf of the Department of Energy (DOE) to numerous technology and policy bodies, and taught a course at DOE. The PSerc consortium now consists of 13 universities with an industrial support of $1.55M from 40 companies and $650K from NSF. Continued alliance with four national laboratories has brought total funding to about $4.0M in 2004. The work at Cornell on market design and testing was chosen by NSF as one of three major successes to come out of PSerc, and of the three, it was chosen by NSF to represent a major NSF program success in their report to Congress.

■ Professor **James S. Thorp** (estimation and control of discrete linear systems applied to electric-power networks), the Charles N. Mellowes Professor of Engineering and former director of the School of Electrical and Computer Engineering, together with his student, **Jie Chen**, and Professor **Tim Mount** of the Department of Applied Economics and Management, won the award for best paper in The Complex Systems Track at the Hawaii International Conference in System Science in January 2004. Jim also reports development of a formulation of ancillary services (both reserves and reactive volt amperes (vars)) for electric power. The model is based on a set of critical contingencies (and corresponding probabilities) that define the need for the reserves. The co-optimization involves selecting a generation pattern that minimizes the total expected cost of supplying energy and paying for the required reserves. A side benefit is that locational shadow prices for both energy and reserves are obtained. That is, for the first time a rationale for ancillary services in different locations has been obtained. The results of the optimization are used to clear the market.

• Professor **Sandip Tiwari** (electronic and optical-semiconductor devices and compound semiconductors), the Lester B. Knight Director of the Cornell Nanofabrication Center (CNF) Knight Laboratory, reports development of the densest low-power nonvolatile memory in silicon, a patented structure that is being rapidly adopted by industry as a follower to the nanocrystal memory (an earlier invention) for the 10–30 nm dimension regime. Sandip's administrative contribution included the award of the National Nanotechnology Infrastructure Network to a Cornell-led partnership ($70M/5 years) and execution of the highly complex move of CNF to Duffield Hall. Evidence of success and worldwide recognition in the execution of CNF objectives are invited papers at the premiere conferences and participation and leadership of federal and international committees and bodies and of external advisory committees of a premier research university (Michigan).

• Professor **Lang Tong** (digital-signal-processing algorithms, estimation theory, wireless communication systems) was promoted to full professor effective January 1, 2004. During this academic year he became the principal investigator for a new Defense Advanced Research Project Agency (DARPA) contract for connectionless networks, and was also awarded a new NSF grant entitled Signal Processing for Random Access. Lang reports that his group has established an experimental testbed for acoustic sensor networks, and that he created a new course, ECE 608, Multiaccess Communication Theory.

• Professor **Stephen B. Wicker** (wireless information networks, digital communication systems, error-control coding, cryptography) reports that his group's proposal for an NSF Medium Information Technology Research grant was funded and the project is now under way. The topic, "Sensor Networks for Disaster Relief," brings together faculty in telecommunications (Wicker and Servetto), device technology (Spencer and Eastman), civil engineering (**O'Rourke**), economics (**Blume**), as well as biology (Burnham and Turner at Wadsworth Center). He hopes this effort will enhance ECE presence in the campus bio initiative. Steve taught course ECE 561, Error Control Codes, for the first time in eight years. He used the class as a testbed for an NSF-funded effort to introduce wireless PCs into the classroom. In a joint project with the Department of Computer Science, he had access to 50 laptops with 802.11 networking capability. The students used the networking capability to demonstrate error control coding on wireless links.

Staff News

Shanti Katta, M.S. '03, computer science (West Virginia University), joined the ECE School on July 21, 2003, as a Linux/UNIX research support specialist. She is responsible for managing installation, migration, and maintenance of 30+ remote Linux servers running Redhat 7.0–9.0 that support Associate Professor **Anthony Reeves's** Early Lung Cancer Action Project (ELCAP). Shanti came to the United States in the fall of 2000 after receiving the bachelor of science degree from Jawaharlal Nehru Technological University in Hyderabad, A.P., India. During her graduate study at West Virginia University she was also a graduate research assistant in the Department of Computer Science, where she contributed to building a highly scalable and available server infrastructure of the department and in the process became an expert in Linux Open Source procedures. Her hobbies include painting, coin collection, and poetry. When time allows, she enjoys outdoor activities such as camping, skiing, and hiking.

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Student Project Notes

The following projects are conducted principally by undergraduate students and several graduate students. The projects are interdisciplinary in nature, with student representation from all branches of the College of Engineering. The students perform all design, development, construction, and testing, seeking guidance from faculty advisors only as necessary.

For full-color photographs of these projects, see the insert in this publication. The ECE School credits the projects' students for contributing these photographs.

Unmanned Vehicle Systems Project

The Cornell University Autonomous Underwater Vehicle (CUAUV) team was started by sophomores in September 1999 under the supervision of ECE Associate Professor **Kevin Kornegay**, who continues as faculty advisor. Since its inception the team has entered the annual International AUV College Competition sponsored by the Association for Unmanned Vehicle Systems International and the National Science Foundation. The competing teams enter remotely controlled underwater vehicles that search for and record the presence of a specific number of objects. The competitions set out a series of objectives that become more challenging and require new additions and more sophisticated equipment each year. The submarine team has joined forces with the aerial group, Cornell University Unmanned Aerial Vehicle (CUUAV) team, whose mission is to fly an airplane autonomously to survey a large area, determine the location and orientation of a number of ground targets, collect the data, and land. These projects give students the opportunity to apply the knowledge learned in the classroom to systems-engineering tasks that demand serious organization, innovation, and teamwork to be successful. The two teams have evolved into an interdisciplinary group of about 60 mechanical, electrical, and computer science engineering students. The Cornell AUV team won first place in the sixth annual competition in San Diego, California, in August 2003, and the Cornell UAV team won first place in the first annual competition at Webster Field, Maryland, in July 2003. Both teams hope for equal success in this year's competition.

Enrollment and Graduation Statistics

Undergraduate Program

Year	Sophomores	Juniors	Seniors	Degrees
01-02	132	195	151	153
02-03	115	172	188	179
03-04	110	159	164	153

M. Eng. (Electrical) Program

Year	August	January	May	Degrees
01-02	29	11	57	97
02-03	28	11	68	107
03-04	18	17	69	104

M.S./Ph.D. Program

Year	Applicants	Admissions	Total Enrollment	Degrees
01-02	834	24	187	20 Ph.D., 6 M.S.
02-03	810	26	194	17 Ph.D., 13 M.S.
03-04	625	26	186	27 Ph.D., 7 M.S.

Note: Undergraduate students now affiliate with the School when the first term of sophomore math and physics is completed.

These figures indicate that over the past three years the undergraduate program has decreased moderately, the M.Eng. (Elec.) program has remained unchanged on average, and M.S./Ph.D. enrollment has remained unchanged on average.

Courtesy of Bruce Land

Students in course ECE 476, Digital System Design.

FSAE Racing Car Project

The Cornell Racing Formula Society of Automotive Engineers (FSAE) team consists of undergraduate and graduate students who design and build an open-wheel formula-style racecar to compete against 140 other colleges in May. The team is made up of four main subteams: chassis, engine, electronics, and business. The electronics team is responsible for the engine control module (ECM), which is designed completely in house and provides precise and fully customizable control of the engine package. The engine of choice is a Yamaha YZF-600R with custom intake and exhaust manifolds and fuel injection and is turbocharged via a Garrett GT12. Key parameters are easily modified via a real-time user interface with optional two-way real-time telemetry that is all done by the subteam. An onboard data acquisition system is constantly used for engine and chassis development as well as driver training. A traction control system (TCS) is implemented and employs a closed-loop algorithm based on data from three wheel-speed sensors. The TCS uses a spark-cutting torque/horsepower map to reduce power as required in traction-limited driving conditions such as sharp turns and acceleration. An electronic wastegate system has been developed with a stepper motor and closed-loop control to limit boost and back pressure to achieve more power from an airflow restricted motor. A custom LED dashboard supplies RPM, gear, and water temperature data to the driver. Cornell is one of the few teams to incorporate this amount of electronics into their FSAE car, but has always had positive results. In 2003, Cornell Racing won the Bosch Award for Engine Management, as well as placed third in acceleration, first in fuel economy and first in highest horsepower. On May 23, 2004, the team won its eighth world championship in Pontiac, Michigan.

ICE CUBE Satellite Project

Members of Ionospheric sCintillation Observation CUBESatellite project (ICE CUBE) have designed and built two small 10 cm satellites that will measure ionospheric disturbances using their on-board Global Positioning Systems (GPS) units after launch during fall 2004. The project, led by Professor **Mark Campbell** of M&AE, is designed to (1) give students who are passionate about space projects access to space and (2) produce valuable scientific data about "space weather." Each of the satellites is a self-contained unit with power (solar cells, Li-Polymer batteries, and power distribution), on-board communications for a space-ground link, a deployable gravity gradient boom, and various sensors with an on-board central pro-

cessing unit (CPU). The satellites will use a Cornell-designed GPS receiver from Professor **Paul Kintner's** GPS group in order to measure the fluctuations in the GPS signals; these fluctuations indicate small disturbances, or scintillations, in the ionosphere. The students will listen to and operate the satellite from a ground station atop Barton Hall on the Cornell campus in Ithaca. The ICE CUBE team, which averages 25 students per year, approximately 40 percent of whom are ECE undergrad and MEng students, has been working for three years toward an October 2004 launch from a Dnepr launch vehicle in Baikonur, Kazakhstan.

Hybrid Electric Vehicle Team

The 2003–2004 Cornell HEV team currently consists of approximately 40 interdisciplinary engineering students. Each student is assigned a specific project for the semester for which he or she designs, implements, and writes a detailed report. Although each student works on his or her individual project, a significant amount of teamwork is involved in putting the whole truck together. The project requires the combined experience of dozens of engineers, business students, and the leaders to run it all. The team is divided into several subteams for specific project goals.

Professors and Subteam Leaders

The project is under the general direction of **Albert R. George,** J. F. Carr Professor of Mechanical and Aerospace Engineering, and **John Callister**, M.S. '92, Ph.D. '96, Harvey Kinzelberg Director of Entrepreneurship in Engineering. With the subteam leaders, these people are the glue that holds the team together. They run the show, call the shots, and give out the grades, so they are treated well.

Business Team

The single most important job of the business team is corresponding with sponsors and developing sponsorship proposals and newsletters to send out on a bimonthly basis. The project webmaster is also a member of this subteam.

Engine and Powertrain Team

The engine team is given the responsibility of the Nissan SR20DET, a 2.0-liter, turbocharged, dual-overhead cammed, sequentially injected inline four-cylinder engine. This engine was chosen for its power, compact size, efficient use of fuel, and low weight. The engine team concentrates on improving the Nissan SR20DET engine's power production, reducing its environmentally harmful emissions, and increasing its fuel efficiency. The team accomplishes these goals through extensive dynamometer testing, the use of an emissions analyzer, and in-vehicle testing.

Chassis, Body, and Suspension Team

The goals of the chassis team include reducing the weight of the vehicle, installing a new electric HVAC compressor to reduce the consumption of gas, improving passenger comfort, and modeling everything in 3-D to help with the packaging.

Controls and Power Systems Team

The main task of the controls team is to create a controls strategy for ideal throttle distribution between the engine and motor so that maximum power output is achieved. This goal would involve an integration of various subsystems, namely a battery management system, data acquisition, telematics, and several monitoring sensors controlled by microcontrollers. A controller area network will provide the network interface between subsystems.

The overall project goal for this year is to exceed last year's finish and win the Future Truck competition.

Laboratory Design Project (ECE 476)

Starting with a program that generates a TV signal in real-time directly from software, the students add several features in order to make a digital oscilloscope that can read a voltage at about 15,700 samples/sec and display properly scaled voltages as a waveform on the TV monitor, set the time base for the oscilloscope, set the trigger mode and trigger level, freeze the last waveform, and compute the RMS voltage. The students are required to demonstrate satisfactory performance of their system to the laboratory instructor and to present a final written report. This exercise demonstrates a system with hard real-time constraints. A late synchronizing pulse is worthless. The TV gives the students rapid visual feedback when the timing is off—the image tears, rolls, or jitters depending on the nature of the timing problem. The exercise also demonstrates the need for synchronization between a fast interrupt-driven routine (video generation) and a slow human interface routine (pushbuttons and drawing).

More Tales from the Past

Your tales from the past are always welcome. Send us your favorite stories about professors, labs, classes, projects, stunts, or whatever you think made the EE/ECE School a special place. We'll print 'em as space allows.

The 2003 issue of *Connections* and the featured biotechnology research brought a number of pertinent comments and notable recollections. One in particular from **Randy Little**, B.E.E. '63, may be of considerable interest for its bio-related content and mention of well-remembered professors and some notable campus landmarks. Randy writes:

Your article "Biotechnology in the ECE School" was particularly timely and interesting. I can lend some further insight to the statement: "In 1963, late Professor **Clyde Ingalls**, E.E. '27 (RPI), offered EE 4593, Fundamentals of Acoustics, a lecture and laboratory course." One advantage of the five-year undergraduate engineering curriculum was that, particularly in that fifth year, it allowed students to pursue subjects of special interest in greater depth than might otherwise have been possible. Such was the case with EE 4593. Throughout my five years I had been working part-time in Cornell's famous Library of Natural Sounds as Dr. **P. P. Kellogg's** student assistant. In fact, while I was still in high school in Ithaca, it was Dr. Kellogg who suggested that I study electrical engineering, so that I would thoroughly understand the equipment and physical principles associated with biological acoustics. Looking toward that fifth year, I had planned to take Professor **True McLean's** course EE 4541, Applied Acoustics, but 1962 was the last year it was offered. I inquired about the possibility of organizing a new course on acoustics. Classmate and talented musician **Peter Lockner, B.E.E. '63,** was also interested in taking a course on acoustics, so Professor Ingalls agreed to offer such a course if we would agree to one condition. He selected *Fundamentals of Acoustics* by Kinsler and Frey as the primary text. The condition was that we teach each chapter ourselves, while he supervised by asking

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More Tales from the Past

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questions to ensure our grasp of the material and to stimulate thought beyond the text. What a wonderful formula for real learning, and where else but at Cornell could it have been done!

The "laboratory" for our course was also rather unusual. As a project I chose to investigate the acoustical properties of parabolic reflectors. This subject has deep roots at Cornell. During World War I, Professor **Harley Howe** of the physics department had developed a large parabolic reflector to help detect the sound of distant aircraft. In 1932 **M. Peter Keane** (Cornell B.S. '32) used that as a model to build a 33-inch parabolic reflector for use in bird sound recording, which was then being pioneered at Cornell by **Albert R. Brand** with the help of Peter Paul Kellogg. Professor McLean had helped to design and build improved amplifiers that could faithfully handle the higher frequencies of many bird sounds. From that time forward, the EE School and the Laboratory of Ornithology have continued to collaborate on bio-acoustical challenges. Everybody knew that parabolic reflectors worked marvelously well for concentrating weak bird sounds onto a microphone, but nobody had rigorously analyzed the acoustic response, nor actually measured those properties. Professors Kellogg, McLean, and Ingalls thought that would be the perfect project for me. (I had wanted to do that from the beginning, but approval comes much easier when the professors think of it as their own challenge.)

The theoretical treatment is a mathematical monstrosity involving Bessel functions, which, though I wished to solve it explicitly, was beyond the capabilities of my K&E "loglog-duplex-decitrig" slide rule and the meager computing facilities of 1963, from which I could at least produce a helpful qualitative solution. To say that the frequency response is not flat nor even linear would be an understatement, but the theoretical treatment proved to be quite useful in guiding reflector and microphone design choices to yield much improved systems. The experimental treatment was another matter. Lacking an anechoic chamber, my initial measurements were made on the roof of Phillips Hall, where echoes would be much less of a problem than within a closed environment.

Photo by William C. Mutch

Figure 7. Memory disks, past and present. The USB drive at lower right has a capacity of 40 MB.

Even so, the flat gravel roof created one primary reflection which, at certain frequencies, caused interference; and traffic on Campus Road added noise which sometimes obscured the test signal. Move to Plan B.

What was Plan B, you ask? When the WHCU AM transmitting antenna was moved from its location, which is now Hasbrouck Heights apartments, the old towers were moved to a field east of Hanshaw Road between the airport and Etna and were used in radio-astronomy and ionospheric research. The land around and beneath the towers was still doing what it had done before the towers came; it was growing hay. Plan B recognizes that a hayfield is much less reflection-prone than a flat gravel roof, and that the remote site has minimal traffic noise to obscure measurements. QED.

Professor Ingalls was inspired by that experience, I believe, to construct the anechoic chamber in Phillips Hall and to continue his work in acoustics until his retirement eight years later.

Another comment on a different topic came from **John Bzura**, B.S. '66, M.E.E. '67, Ph.D. '71, who writes:

I enjoyed the latest issue (summer 2003) of Connections, *and was moved to write about the wonderful tribute you wrote about Professor* ***Stan Zimmerman.*** *I took his course on High Voltage Technology in the spring of 1966, and if I recall correctly you also contributed to teaching that course. Anyway, it was very enjoyable and I appreciated the field trips too. The chance to tour General Electric Company's transformer facilities in Pittsfield is long gone, but the Great Hall for turbine/alternator assembly in Schenectady still remains in my mind. To get back to Stan, your tribute touched on many things I now know or worked on at some point in my ten years at Cornell. I knew a fair amount about the High Voltage Lab (or the Mitchell Street Lab when we worked there from 1967 to 1972) but it was enjoyable to learn more about cable testing prior to 1967 and the history of the building.*

Sam Linke reporting: In keeping with the advanced computer engineering topics discussed in this issue, it seems appropriate to comment here on an old friend of the past: the "floppy disk," as illustrated in Figure 7. The ancient (circa 1967) 8-inch disk belongs to Professor **Tony Reeves**, and I found an old 5.25-inch one in my desk. There are no longer any PC disk drives available in the ECE School to play these artifacts; perhaps one is hidden away somewhere in Ithaca. Of course there are plenty

of the now standard 3.5-inch 1.44 MB disks still available for use, but the current ultra-high-memory CDs and USB-drives will soon cause them to join their earlier counterparts as curiosities. The original so-called memory disks were encased in flexible plastic envelopes which wiggled when waved, hence the name "floppy," but Professor Emeritus **Chris Pottle** told me once that he thought the name may have come from "floating point operations per second." The first 8-inch disks were read-only units at 100 kB, but were rated at 250 kB when they were upgraded to double-sided read/write units. The 5.25 double-sided disks were rated at 360 kB. Comparison of these primitive numbers with the 100 to 200 MB memory disks of today offers a good example of the enormous progress in computer engineering that has occurred in the past 30 years.

Sam Linke

A Link Between Alumni and the School of Electrical Engineering

In this issue, we are continuing the "Positive Feedback" feature of previous years. The first twelve issues of *Connections* triggered a gratifying number of responses. We hope that this issue will stimulate even more returns of the coupon in the insert of this newsletter, or reports on your recent activities.

Note for Internet surfers: On the World Wide Web, the ECE School home page may be found at www.ece.cornell.edu. The College of Engineering's URL is www.engineering.cornell.edu.

Note: Our alumni file is somewhat incomplete. If you know of school alumni who are not receiving *Connections*, please urge them to send their names and addresses to **Jeanne Subialka,** B.S. '99 (ILR), Engineering Public Affairs, 248 Carpenter Hall, Ithaca, NY 14853.

Positive Feedback

Max H. Kraus, B.E.E. '49, emeritus member of the board of directors of the Cornell Society of Engineers (CSE), now retired and residing in Meadowbrook, Pennsylvania, attended the Engineering Conference in April 2004. He had not visited the campus for many years and enjoyed meeting and talking with old friends.

Simpson (Sam) Linke, M.E.E. '49, professor emeritus of electrical engineering at Cornell, was a member of a panel discussion at the CSE Conference in April on "The Coming of the Hydrogen Economy: Fact or Fantasy?"

William E. (Bill) Gordon, Ph.D. '53, designer of the Arecibo Observatory and distinguished professor emeritus at Rice University, was the keynote speaker in Puerto Rico on November 1, 2003, at the fortieth-anniversary celebration of the establishment of the facility. Bill, who now resides in Ithaca, New York, related the early history of the observatory to over 135 attendees at the event.

William L. (Bill) Simon, B.E.E. '54, book author/film and TV writer living in Rancho Santa Fe, California, and his twin brother, **David H. Simon**, B.E.E. '54, retired, living in Sherman Oaks, California, were on campus for their fiftieth reunion in June 2003. Bill was pleased afterwards to be able to obtain a photograph of the late Professor **L. A. Burckmyer**, whom he credited with encouraging him to start his writing career.

Alan S. Rosenthal, B.E.E. '60, M.S. New Jersey Institute of Technology, vice president and senior business data architect, Banc of America Securities, New York City, and a member of the board of directors of CSE, attended the CSE Conference in April 2004 and enjoyed meeting with old friends.

Randolph S. (Randy) Little, B.E.E. '63, M.S.E.E., Ohio State University, M.S. Mgmt., Pace University, retired venture manager, and hiatus member of the board of directors of CSE, enjoyed his attendance at the conference in April 2004. Randy has submitted an interesting account of some undergraduate experiences (see "Tales" on page 21 of this issue).

Peter G. Jessel, B.E.E. '65, M.S. '66, engineer, chief information officer, Towers Perrin in Stamford, Connecticut, has been an adjunct professor in the ECE School during this academic year, and has taught a course for ECE master of engineering students that is targeted at students who are interested in real-world computer systems.

Karl F. Miller, B.E.E. '65, M.E.E., Rensselaer Polytechnic Institute, manager, process improvement, Citi Steel USA, in Claymont, Pennsylvania, served as president of CSE this year and presided over the conference in April 2004.

Kenneth S. Schneider, B.S. '65, M.E.E. '66, Ph.D. '70, chairman and CEO Telebyte Broadband, Greenlawn, New York, reports that he continues to build his company with a focus on broadband test equipment. Ken writes that he remains in contact with his classmate **Jamil Sopher**, B.S. '65, M.E.E. '66, M.B.A. Harvard, staff associate, World Bank Group, Washington, D.C.

John J. Bzura, B.S. '66, M.E.E. '67, Ph.D. '71, principal engineer of former New England Power Service Company, now part of Transco in the United Kingdom, writes that he continues to monitor advanced technologies like all forms of distributed generation, power-line-carrier systems for Internet access over power distribution circuits, renewable energy and a few other things. John has submitted an interesting account of some undergraduate and graduate experiences (see "Tales" on page 22 of this issue).

Thomas W. Piwinski, B.S. '74, M.E.P.E., Rensselaer Polytechnic Institute, senior electrical engineer, New York Dormitory, Albany, New York, attended the CSE Conference in April 2004 and enjoyed meeting and talking with old friends.

Edward T. Lu, B.S. '84, NASA astronaut, spoke with Cornell President **Jeffrey S. Lehman**, B.A. '77, M.A. and J.D. '81, University of Michigan, from the orbiting International Space Station on October 16, 2003, as part of the new president's inaugural celebration.

Jennifer T. Bernhard, B.S. '88, M.S. '90, Ph.D. '94, Duke University, associate professor in the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, was the ECE colloquium speaker on April 6, 2004. Jennifer spoke on the topic "Antennas for the Twenty-first Century: Reconfigurable Radiating Systems."

Judith B. Cardell, B.S. and B.A. '89, Ph.D., Massachusetts Institute of Technology, Clare Boothe Luce Assistant Professor of Computer Engineering, Picker Engineering Program and Department of Computer Science, Smith College, was the speaker at an ECE seminar on April 15, 2004, on the topic "A Distributed Power System: Stability and Operation with Distributed Generation."

Eminent Professors' Fund

Twelve years ago the EE School established the Eminent Professors' Fund to honor the memory of notable members of the EE faculty of past years such as professors **Ralph Bolgiano, Jr., Henry Booker, Nelson H. Bryant, L. A. Burckmyer, Walter W. Cotner, Casper L. Cottrell, William H. Erickson, Clyde E. Ingalls, M. Kim, J. Peter Krusius, Charles A. Lee, Michel G. Malti, Malcolm S. McIlroy, True McLean, Wilbur Meserve, B. K. Northrop, Robert Osborn, Joseph L. Rosson, Howard G. Smith, Everett Strong, Joseph G. Tarboux, Stanley W. Zimmerman**, and others whom alumni may recall. The objectives of the fund are twofold: (1) to acquire specific grants to improve laboratory and research facilities in the ECE School, and (2) to establish endowments to provide ongoing financial support for undergraduate and graduate students. The ECE School has given high-priority status to the following activities:

- Establish an endowment fund to supplement the operating costs of the undergraduate computing center and the undergraduate teaching laboratory.
- Establish an endowment fund to provide financial support, on a yearly basis, for graduate and undergraduate students who serve as teaching assistants in our laboratories.
- Establish one-year fellowships to support professional-master's degree candidates for the M.Eng.(Electrical) degree.
- Establish a fund to support M.Eng.(Electrical) research projects.

Alumni who would like to contribute to the Eminent Professors' Fund should contact Professor **Clifford R. Pollock,** School of Electrical and Computer Engineering, Room 224, Phillips Hall.

ece ONLINE NEWS

New ECE Web Page Is Now On-Line

The ECE School web page has been extensively modified. The current version contains a guide for enrolled and prospective students, an updated alumni section, and general information about the school and faculty. Check it out at:

www.ece.cornell.edu

ECE Alumni On-Line

Alumni can visit the site by clicking on the "ECE Alumni" link of the main ECE School web page.

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