DESIGN OF INTEGRATED, EFFICIENT POWER AMPLIFIERS FOR

NEXT-GENERATION WIRELESS COMMUNICATIONS

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Ian Andrew Rippke

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DESIGN OF INTEGRATED, EFFICIENT POWER AMPLIFIERS FOR

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Ian Andrew Rippke, Ph.D.

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An integrated power amplifier and DC-DC converter are presented to create a variable supply voltage power amplifier to improve battery life in cellular handsets. This system has the ability to reduce the average battery current drawn by a handset power amplifier by operating at lower supply voltages when not transmitting at maximum power. This type of system has not been adopted because of the need for additional circuitry when used with traditional power amplifier modules. To be attractive to system designers, advanced power amplifiers need to exhibit the integration that has been seen in modern radio receivers. In this work, SiGe BiCMOS technology is harnessed to achieve the integration of both circuits on one die, presenting a solution to the desire for high efficiency in a single chip solution.

The design of power amplifiers in SiGe technology is explored, with a focus on the design of a WCDMA handset power amplifier for third generation mobile systems. The design challenges of such a circuit are presented, along with a design methodology involving a mix of time and frequency domain simulation techniques. Layout concerns are addressed in regards to the SiGe BiCMOS process, and their impact on power amplifier performance is highlighted. Measured results are presented which meet the linearity requirements of WCDMA.

A high switching frequency DC-DC converter is also examined, with a focus on integration of such a circuit with a power amplifier. The impact of frequency

selection and converter efficiency is analyzed, and several techniques to improve the efficiency are presented. Simulation and measurement results are presented which show excellent agreement over the broad range of converter operating conditions. An analysis method for determining the average reduction of battery current in a variable supply voltage system is presented, with results given for the DC-DC converter/power amplifier integrated system. The integration issues and system performance in regards to physical layout are discussed. The final system measurements show the successful performance of the power amplifier under variable supply voltage operation with the DC-DC converter. The results of this work demonstrate the feasibility of such an integrated, efficient power amplifier and provide a path for integration of advanced power amplifier systems with other transceiver components.

BIOGRAPHICAL SKETCH

Ian Andrew Rippke was born on July 28, 1978 to Mr. Robert Henry Rippke and Mrs. Marcia Ruth Rippke in Princeton, New Jersey. Ian graduated from Hempfield High School in Landisville, Pennsylvania in 1996. He received his undergraduate education from Lafayette College in Easton, Pennsylvania and graduated with Honors in May 2000 with a Bachelor of Science in Electrical Engineering. In August 2000, Ian began graduate study at Cornell University. He received a Master of Science in Electrical and Computer Engineering in October 2003. He completed his Doctor of Philosophy in Electrical and Computer Engineering with a minor in Applied Physics in 2005. Ian is currently a member of the Applications Engineering team at Xpedion Design Systems, Inc. in Allentown, Pennsylvania.

ACKNOWLEDGEMENTS

To my wife Kristie, who through her love, support, and patience

has taught me what truly matters in life

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1.1   Perspective

The field of radio-frequency integrated circuit (RFIC) design is experiencing a continuing push for integration and miniaturization of transmitters and receivers due to expanding consumer demand for wireless devices. Broad application of wireless technology requires chipsets that are small, robust, low power, and ultimately low cost. This has driven designers to integrate as much of the radio front-end as possible, with the ultimate goal being the reconfigurable single-chip radio that can accommodate multiple standards and applications through flexible and adaptable architecture [1]. The solution to this problem will come in the form of a low-cost, highly integrated radio architecture implemented in a mass-producible, commercially viable process.

However, the hurdles to such an implementation are numerous. In second generation (2G) cellular phones, the standards vary considerably in different areas of the world, and even in the United States several different standards share the workload of the cellular infrastructure. The move towards third generation (3G) cellular phones looked to unite these varied standards into a single platform of global interoperability. Recognizing the need for higher capacity, broader spectrum allocation, and global roaming, the Third Generation Partnership Program (3GPP) and its associated group 3GPP2 developed a standard that supports both the Global System for Mobile Communications (GSM) and the code-division multiple access (CDMA) standards popular in the United States and Japan [2]. The 3G standards from both groups make

use of wideband code-division multiple access (WCDMA) as the modulation format and access scheme. This provides the potential for up to 3.84 megabits per second (MBPS) of data transfer over the cellular interface. The evolution of cellular standards is shown in Figure 1. Through this harmonization of standards, the adoption of 3G will solve the primary problems of capacity and global accessibility.
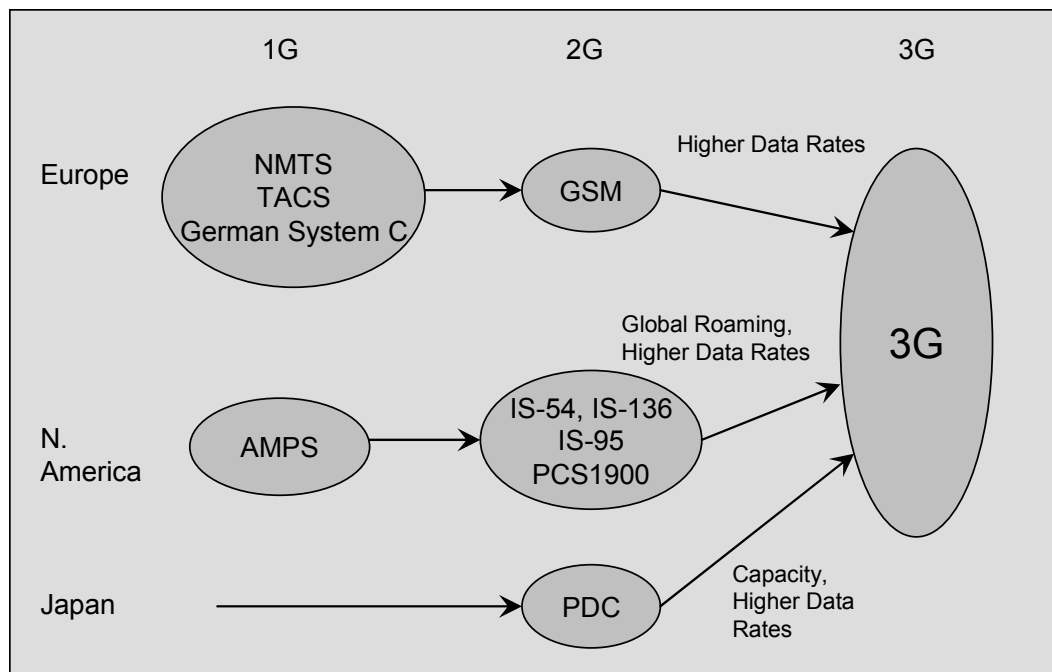
Figure 1. Evolution of cellular standards worldwide and specific needs for 3G

The hardware for realizing a reconfigurable radio exists in the baseband (digital) domain in the current multipurpose processors available for use in cellular handsets. The continued advances in scaling of complimentary metal-oxide semiconductors (CMOS) had provided fast, efficient processors with the capability to reconfigure on-the-fly through software. The main technological drawback to the realization of a single-chip radio has been the RF integration that is necessary for such a system. This is not to say that the RF portion of the chip has not benefited from advances in CMOS technology. Several successful integrated transceivers have been

developed in CMOS-only processes, paving the way for integration with baseband processing capabilities [3-6].

But despite the gains made in most areas of transceiver integration, the power amplifier (PA) remains a hurdle to the realization of single-chip radios and overall design integration. The original 1G and 2G power amplifiers made use of gallium arsenide (GaAs) metal-semiconductor field effect transistors (MESFETs) to provide high power devices. These depletion-mode devices often needed complex external circuitry to generate the negative gate voltages required to turn the devices on. This additional voltage generation/regulation circuitry has since been removed due to advances in III-V device technology. Current power amplifier module (PAM) technology for 2G systems is still based on III-V compound semiconductor technology, but primarily uses heterojunction bipolar transistors (HBTs) fabricated by molecular beam epitaxy (MBE). The HBTs are composed of various alloys of III-V compounds such as aluminum gallium arsenide (AlGaAs) and indium gallium phosphide (InGaP), along with GaAs as the epitaxial layers. These devices achieve the high performance of MESFET devices, but have the advantage of a positive base-emitter voltage control. The current power amplifier chips are packaged in a multi-chip solution with a silicon CMOS bias and control chip encased in the same plastic package. While less complicated than their MESFET counterparts, as a separate module and a different technology this approach continues to defy the advances of transceiver integration.

As the use of more exotic materials and devices like III-V HBTs continues to dominate the power amplifier market, this prevents integration with small, low cost silicon CMOS transceiver circuits. Many of the advances in modern RFIC chipsets such as multi-standard support and advanced linearization techniques have been made possible by the use of digital control techniques which are most easily implemented in silicon CMOS and achieve the greatest advantages when applied to a fully integrated

system. A linearized power amplifier offers higher performance because it can operate closer to saturation or can be tuned to trade-off linearity for efficiency when necessary [7]. Digital circuits can also be used to generate predistorted waveforms that can be used with high efficiency switching amplifiers. An entire transmitter can be linearized to allow the use of a cheaper, less advanced transmitter while still achieving the desired performance [8]. This can be an enabling technique for software defined radios to allow the use of multiple RF transceivers in a single handset, rather than requiring a single high-performance, frequency-agile transmitter. All these approaches and techniques point to the need for a power amplifier that can be integrated with a low-cost transceiver while offering improved efficiency to support the increased features of 3G cellular systems.

1.2   *Motivation*

The current commercial demand and emerging markets for wireless connectivity has motivated this work into integrated, efficient power amplifiers. Wireless standards and applications have evolved rapidly to become one of the fastest growing areas of IC technology. The requirements for these wireless devices are continuously expanding, requiring more and more capabilities from the wireless transceivers as well as the baseband processors. While advances in fabrication technology have allowed designers to shrink the size of their circuits while at the same time increasing their complexity, this often comes at the cost of increased power consumption as more and more features are added, including multiple-standard support for wireless networking and Bluetooth.

Current battery technology is not advancing at the same pace as wireless systems and standards, placing increasing demand on mobile transceivers to be energy efficient [9]. Lack of increased battery capacity could greatly impact the adoption of

3G services. Consumer demand for increased feature content is driving handset manufacturers to look for alternatives to the traditional lithium-ion rechargeable battery. Improved battery technologies are on the horizon, but are still in the development stage and will take several years to emerge into the commercial mainstream.

Adaptive systems are one way of dealing with the need for increased efficiency to provide longer battery life in mobile applications. The power amplifier remains a large consumer of energy in any RF transceiver system, often eclipsed only by advanced baseband and multi-purpose processors. Modern wireless standards require highly linear power amplifiers that often sacrifice efficiency to provide adequate linearity at maximum signal output. By leveraging a technology that allows integration of adaptive control features with the power amplifier, this balance between efficiency and linearity can be constantly adjusted to provide the maximum battery performance out of a mobile device. Adaptive efficiency control and integrated power amplifiers can overcome current battery limits while reducing transceiver size and cost in 3G systems.

1.3   New and Original Contributions

The design of power amplifiers in silicon-germanium (SiGe) technology has recently advanced to the point of commercial acceptance among handset designers who traditionally favored GaAs PA modules. Designing power amplifiers in this technology is still challenging and provides many hurdles that must be overcome through careful circuit design techniques. Additionally, high operating frequency (10-100 MHz) DC-DC converters are rarely used in low-power systems because of the losses associated with increased switching frequency. At these higher frequencies, however, DC-DC converters have the advantage of being integrated along with the

circuits they drive on a single substrate. The design of such converters presents challenges over traditional converter design that has been explained in this work. The combination of these two techniques leads to one of the first implementations of a single chip power amplifier/DC-DC converter that can realize the battery current savings of dynamic supply voltage adjustment while enabling true single-chip radio solutions in the future.

Chapter 2: Linear Power Amplifier Design Fundamentals

2.1 Overview

Engineers new to power amplifier design are often amazed by the elegant simplicity of the amplifier itself. It differs little from the textbook common-source or common-emitter amplifier, but the differences themselves are the critical distinctions between power amplifiers and their small-signal brethren. At the heart of understanding power amplifiers is a virtual alphabet soup of naming conventions, each describing the general operation of the amplifier in one or two simple letters.

Beneath this basic façade lies a world that has spanned the careers of many famous engineers, and continues to pique the interest of researchers worldwide. The ultimate challenge of delivering power efficiently has become increasingly more complex through the introduction of elaborate modulation schemes brought about by digital radios. Add to this the increasing performance of silicon technologies and the tried-and-true compound semiconductor devices, and the landscape begins to unfold on a dramatic field which is possibly the last haven of the mysterious 'black art' of microwave design.

But despite all these factors, power amplifier design still boils down to fundamental equations and assumptions that have withstood the test of time, ultimately providing the same starting point as the theory did for designers using vacuum tubes and kilowatts in the early days of radio technology.

This chapter presents an overview of power amplifiers, highlighting the current technologies used, their classes of operation, and techniques used in their design. The process overview will focus on emerging technologies that provide lower cost and increased integration potential. Because of the focus on high data rate communications, linear power amplifiers will be the primary topic of the discussion on classes of operation. Design techniques will cover some of the primary differences between power amplifiers and typical RF circuits, as well as the use of small signal analysis in PA design. Finally, a large-signal transient technique will be discussed as a starting point for linear power amplifier design.

2.2   Technologies

For a long time a discussion of microwave and RF power amplifier technology was a very short one, because the only technology of interest was the GaAs MESFET. Improvements in molecular beam epitaxy brought along the successors to the MESFET, the III-V compound HBT and high electron mobility transistor (HEMT). These devices continue to dominate the wireless power amplifier market. Yet with recent advances in compound semiconductor technologies and silicon device scaling, several technologies, while by no means new, are emerging in the power amplifier market as viable alternatives to III-V compound devices. This section will describe the emerging use of Silicon MOSFETs and SiGe HBTs in power amplifier design, with a focus on integrated transceiver applications.

2.2.1   RF Silicon CMOS Technology

Scaling of silicon CMOS and the desire for transceiver integration has resulted in a push for RF applications in this technology. Fully integrated CMOS transceivers have already found their place in several wireless standards [10], but almost always with the exception of the power amplifier. The desire to integrate all components of

the radio in a single technology, even on a single chip has motivated much of the research into CMOS power amplifiers.

Despite this integration desire, the technology itself presents several hurdles to be overcome. Foremost among these is the low breakdown voltages of advanced CMOS technologies. While baseband digital circuits are scaling to supply voltages of 1V [11], supplying the required power for many wireless standards requires a much higher supply voltage in order to limit the amount of current that needs to be sourced by the FETs. Counteracting the desire for a higher supply voltage for the PA is the ever-shrinking gate length of CMOS processes. To minimize short-channel effects, the gate thickness is also being reduced [11]. This results in decreasing gate-drain and gate-source breakdown voltages for device reliability. Circuit approaches such as cascoded devices can be used in these situations [12], but now the size of the overall circuit is increasing to accommodate these techniques.

Low cost digital CMOS processes also often lack the integrated passives that are necessary for RF power amplifier design. The lack of metal-insulator-metal (MIM) capacitors increases the process variability of any matching networks. Advanced capacitor architectures such as vertical mesh capacitors [13] can help alleviate this burden, but the close pitch of metal lines in digital processes also reduces the current handling at any level of metal. These thin, narrow metal traces also increase parasitic inductance in the circuit. Even in more "analog-friendly" CMOS processes, the limitation becomes the inductors that can be implemented on-chip. The conductive substrate of most silicon processes allows for large eddy currents that contribute to very low quality factors in inductors. To simplify integration and reduce time-to-market, it is desirable to have all the matching components on-chip, but the lossy silicon substrate limits the quality factor (Q) of on-chip inductors to around 10 at best in bulk CMOS processes [14]. The conductivity of the substrate also provides paths

for signals to couple between circuits or even different sections of the same circuit. This has pushed the power amplifier back into the module space, where advanced substrates such as low temperature co-fired ceramic (LTCC) are used, at increased cost, limited integration, and longer design cycle [15]. Yet the desire for single-chip integration and the benefits of having analog and digital components on one die continues to fuel the research into CMOS power amplifier design.

2.2.2 SiGe HBT Technology

SiGe BiCMOS technology has recently emerged as a viable candidate for power amplifier integration. The graded-base SiGe HBT can achieve the performance level of GaAs-based devices while maintaining integration capabilities enjoyed by CMOS technology. Integrated with a traditional CMOS process, the BiCMOS technology is considerably cheaper than GaAs from a process standpoint. SiGe achieves an almost 5x cost reduction compared to GaAs chips while only adding 10% to the cost of a comparable bulk silicon process. Of additional interest in PA applications, silicon offers three times the thermal conductivity of GaAs, making it an ideal substrate for these circuits [16].

The SiGe 6HP process from IBM represents a major advancement in the area of on-chip passive components in silicon substrates as well. This process includes an "analog metal" layer as the last metal layer of the process. This layer is a 4μm thick aluminum layer that has a much lower resistivity than traditional metal interconnect layers. This reduces series resistance in on-chip inductors, and also provides high current handling. Borrowing from DRAM technology, an oxide-filled deep-trench layer is available which effectively increases the distance between conductive elements such as the turns of an inductor and the low-resistivity silicon substrate. By lowering the series resistance, increasing the substrate spacing, and reducing eddy

currents, inductors with Q factor of 20 have been realized at RF frequencies upwards of 2GHz SiGe technology [17]. These higher quality passives can be used for interstage bias inductors in power amplifiers, though high current handling requirements still limits their use in the output stage of a power amplifier. A second use for the deep-trench structures is in isolation guard rings. These guard rings can be used to reduce the coupling of signals between blocks in a complex RF circuit, and also to shield critical lines from other signals that might inject noise in sensitive areas. These structures can be leveraged to increase the integration of RF circuits, even in the presence of noisy digital logic or high power signals from a power amplifier.

An initial drawback of SiGe technology was the low open-base breakdown voltage BVceo reported from initial technology studies. Reported breakdown voltages of 3-5.5V caused speculation that with voltage swings as high as twice the supply voltage at the output of the power amplifier, the technology would not be able to produce power amplifiers operating at current handset battery voltages.

Recent research indicates that the previous concern over BVceo as the limiting factor in SiGe power amplifiers is unwarranted, and that in fact the devices are capable of operating at voltages well above BVceo [18,19]. These devices will not only survive these voltages instantaneously; they also exhibit excellent reliability when exposed to extreme operating conditions [20]. Further research indicates that SiGe devices used for power amplifiers will not be limited by the Johnson limit, which states that the product of BVceo and the unity gain transition frequency f_T for a device is constant. Rather, the maximum frequency of oscillation f_{max} and the breakdown voltage with the base grounded through a resistance (BVcer) instead determine the performance characteristics of SiGe HBTs used in power amplifier applications [18]. These promising results, along with continued research into SiGe power amplifiers

and integration potential have helped establish SiGe technology as a likely candidate for future power amplifier products.

2.3   Classes of Operation

The general operation of a power amplifier falls into two categories: linear and nonlinear. The distinction between the two can become somewhat blurry in more advanced topologies, but historically this delineation has been maintained. In linear classes of amplifiers, the output power is a linear function of the input power over some desired power range. Beyond this linear range, the device is said to move into the "saturated" mode of operation, where the output power changes very little for increases in the input power. This represents one of the cases of nonlinear power amplifier operation. Nonlinear power amplifiers can also be designed as switching power amplifiers, where the transistor is used as a switch and the output signal is restored through harmonic filtering of the switch output. This section briefly describes nonlinear amplifiers and their various classifications, but focuses primarily on the linear classes of power amplifiers.

2.3.1   Linear Power Amplifiers

Linear power amplifiers are classified as class A, B, or AB. The difference in the types depends on their conduction angle, or for what fraction of a period of a sine wave the transistor is in the on-state. The concept of conduction angle is illustrated in Figure 2. Here, as the input voltage drops below the threshold of the device (V_T), the output current goes to zero until the input voltage rises above V_T again. The conduction angle is set by the bias point at of the input voltage, given here as V_q, or the quiescent point. The effect at the output, other than reducing the conduction angle of the signal, is also to reduce the DC level of the signal, given as I_q in Figure 2. The

benefits of such an approach are explained later. This graphical representation of conduction angle can also be given as an equation for the output current:

$$i(\theta) = \begin{pmatrix} I_{peak} \cos\theta & -\alpha/2 \leq \theta \leq \alpha/2 \\ 0 & \text{otherwise} \end{pmatrix} \qquad (2.1)$$

where α is the fraction of time that the amplifier is conducting signal.
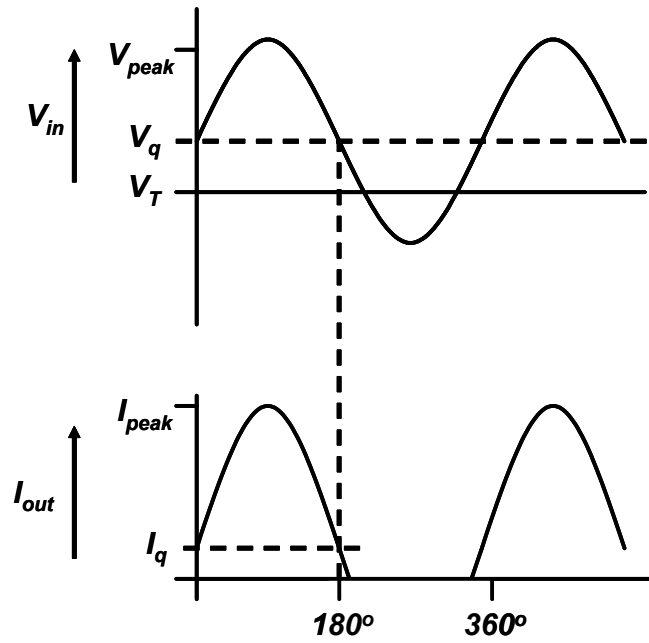
Figure 2. Reduced conduction angle of output current due to level of input signal

The desire to reduce the DC component of the output signal while maintaining linearity can be seen from the expression for power added efficiency (PAE). PAE can be written as

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}} \qquad (2.2)$$

PAE includes the RF power delivered to the amplifier, in addition to the RF output power and DC power. It can be seen from (2.2) that decreasing the DC component results in a higher PAE. This will be explained in more detail below.

2.3.1.1 Class A Amplifiers

In class A operation, the power amplifier conducts for the entire period of the sine wave, or 360° of conduction angle. The bias point of the amplifier is such that there is no clipping of the signal. This is the most linear class of operation from a harmonic generation standpoint, because there is ideally no signal distortion that can contribute harmonics other than the fundamental.

While the class A power amplifier provides the highest linearity, it suffers from a low efficiency. Because the bias points must be chosen as V_{peak} and I_{peak}, the maximum efficiency of a class A power amplifier is 50%. This comes from using the RMS values of the output voltage and current waveforms to determine the RF power.

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{V_{peak}/\sqrt{2} * I_{peak}/\sqrt{2}}{V_{peak} * I_{peak}} = \frac{1}{2} \text{ or } 50\% \qquad (2.3)$$

Here, η is the efficiency of the amplifier, expressed as the ratio of RF output power to DC power supplied to the circuit. So while linearity is maintained over the entire output power range, half the power supplied to the amplifier from the circuit is lost rather than converted into transmitted signal at RF frequencies.

2.3.1.2 Class B Amplifiers

A second choice for conduction angle in a power amplifier might be half the period of the sine wave, or 180° of conduction angle. This is known as class B operation. First instinct would say that this could not possibly be linear because half of the signal is clipped on each cycle. Yet Fourier analysis of the signal indicates that

because the output is now an even function, there are no odd harmonics generated through this clipping process [21]. The presence of a strong second harmonic content does impact the output signal, but usually harmonic termination methods are used to remove this harmonic content from the final output signal.

The advantage of using such a conduction angle is that the output signal at the fundamental is the same level as in the class A case, but the DC component of the current waveform is reduced by $\pi/2$, which gives a peak efficiency of $\pi/4$ or 78.5%. This is a significant improvement over the class A amplifier with the only caveat being the need for a proper second harmonic termination.

2.3.1.3 Class AB Amplifiers

Class AB amplifiers span the range of conduction angles between 180° and 360°. They have less second harmonic content that the class B amplifier, but the output signal is no longer an even function which introduces odd-order harmonic content as well. Often the designer will trade off linearity with efficiency in order to choose the bias point, and thus the conduction angle, of a class AB power amplifier.

2.3.2   Nonlinear Power Amplifiers

These classes of amplifiers are differentiated from the linear classes because the output power is not a linear function of the input power. As mentioned above, there are two general types of nonlinear amplifiers: saturated and switching.

2.3.2.1 Class C Amplifiers

Saturated amplifiers are class C amplifiers. Either through bias choice or signal level, they are designed to conduct for less than 180°. The requirements for this operation are either a very large input signal, or a negative bias level that reduces the

conduction angle by lowering the quiescent level below the threshold of the device. The output then is a mere fraction of the overall signal, resulting in reduced output power, increased harmonic content, and greatly increased efficiency. This operation is depicted in Figure 3.
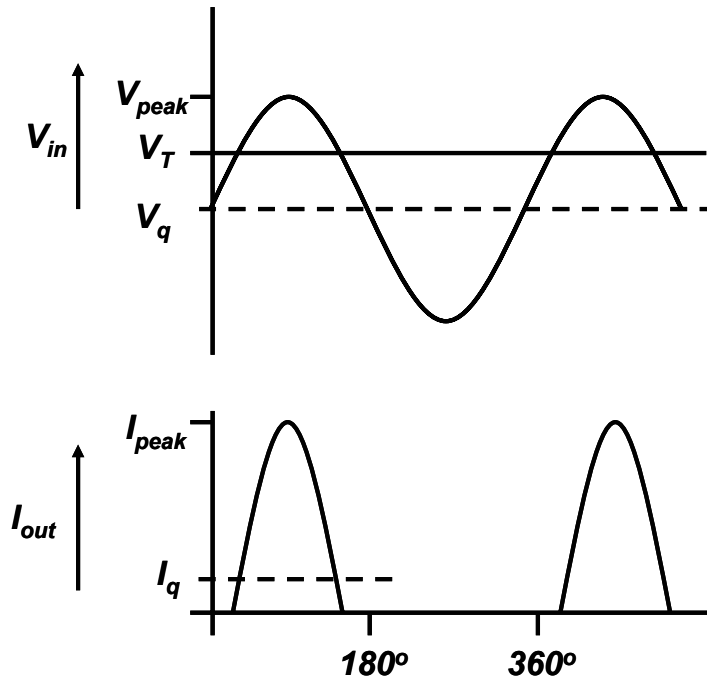
Figure 3. Reduced bias and conduction angle for class C operation

The further reduction of the DC level over the class B condition leads to efficiencies that are theoretically as high as 100%, however this is not practical because to achieve that efficiency, the conduction angle has gone to 0° and there is no RF power being delivered to the load. Similar operation is achieved when a linear amplifier is driven into saturation. As the output voltage can no longer support the required amplitude at higher input powers, the output signal begins to clip, and the output power saturates. In this condition, the output power level is no longer a linear function of the input level. This type of operation is used in GSM systems, where the

data is encoded entirely in the phase and not in a time-varying envelope, allowing the use of a nonlinear amplifier.

2.3.2.2 Class D, E, and F Amplifiers

These classes of amplifiers are all based on the use of the transistor as a switch. With the advent of CMOS as a potential candidate for RF power amplifiers, these classes of operation have gained increasing attention because of how well a MOSFET behaves as a switch. In a switching amplifier, theoretically 100% efficiency can be obtained **while still delivering power to the load,** unlike the class C amplifier. This is achieved by using reactive storage elements to preserve the signal when the devices are off. The basic switching amplifier and its important waveforms are given in Figure 4.
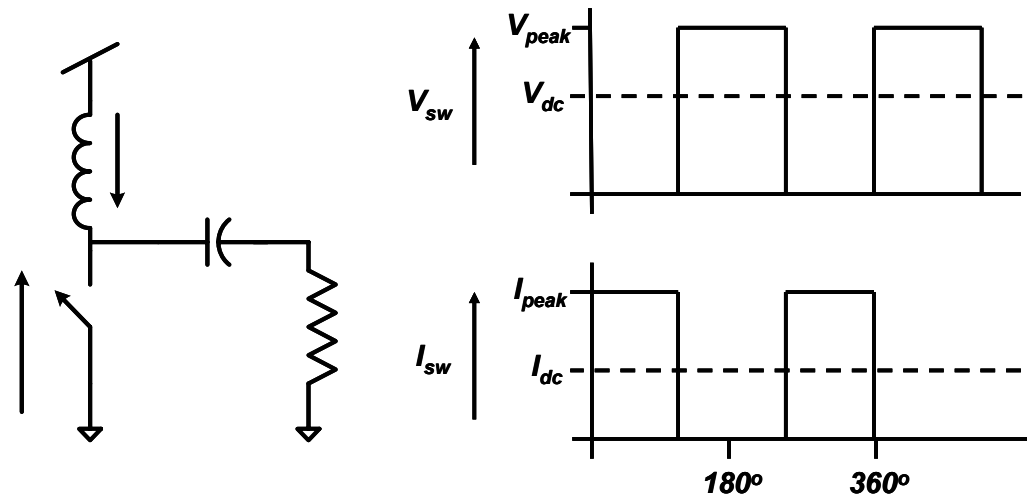
Figure 4. Switching power amplifier operational diagram and waveforms

Class D is a fairly straightforward implementation of the direct switching amplifier pictured above. Resembling a "push-pull" type of amplifier, the switch is used to create a square voltage wave at the output of the amplifier, while the current flows into a series resonant circuit at the output of the switch. When the switch is

connected to the supply, half the sinewave of current is provided to the resonant circuit, while when the switch is connected to ground, the negative half-sinewave is generated by the output resonant circuit. The goal of such an amplifier is to never have an overlap of switch current and switch voltage. The ideal design also assumes that there is no loss in the reactive elements. In a real device, the finite rise and fall times of the switch, as well as resistive losses in the passive elements will limit this efficiency, but designs have been reported with upwards of 75% efficiency when operating at RF frequencies [22].

In a class E amplifier, this approach is varied slightly. The switch toggles between open and closed rather than supply and ground. A capacitor across the output of the switch sources the charge when the switch is open. Again, a series resonant circuit is used in the output to regenerate the current at the fundamental frequency. In both class D and class E amplifiers, reactive components are used at the output of the amplifier to filter the square waves. In the case of a class E amplifier, this tuning is designed to minimize the crossover time between the current and voltage waveforms.

Class F takes a different approach and uses tuned networks to purposely enhance or add harmonic content to the output waveform. Less a switching amplifier and more of a clipping of overdriven amplifier, it uses the same principles of square waves to achieve its efficiency improvements. Just as a sine wave can exhibit a more "square-like" characteristic by adding third harmonic content, the waveforms in a class F power amplifier can be tuned in order to emulate a square-wave signal at the output.

Advances in RF CMOS technology and increasing need for long battery life will continue to spur research into switching amplifier topologies for wireless communications. Future wireless systems, such as ultra-wideband (UWB), that make use of pulsed RF transmissions could stand to make the best use of switching

amplifiers. Also, increased digital processing power in RF systems and the use of advanced waveform-shaping techniques could allow systems to exploit nonlinear amplifiers for the transmission of linear signals, realizing both high linearity and high efficiency transceiver systems.

2.4   Tuning and Matching

An important part of any RF circuit design is ensuring that the proper impedances are presented to each component in the circuit. In small-signal analysis, 50Ω is the standard for interface impedances to ensure a lossless transition of signal. The basic principle of operation of an RF power amplifier is to boost the small signal generated by the rest of the transmitter to a level that is powerful enough to be transmitted through an antenna, enabling wireless transmission of voice or data. The power amplifier does this by converting DC power at zero frequency to RF power at some higher frequency in the MHz to GHz range. The goal is to perform this conversion as efficiently as possible, thereby wasting very little energy in the power conversion.

2.4.1   Power Transfer and Load-line Matching

Basic circuit theory indicates that when concerned with power, the maximum transfer of power occurs when the interface impedances are the complex conjugate of each other. This is equivalent to the point where there is no power reflected back to the source, and all is being delivered to the load [23]. Figure 5 shows the setup for a resistively matched system.
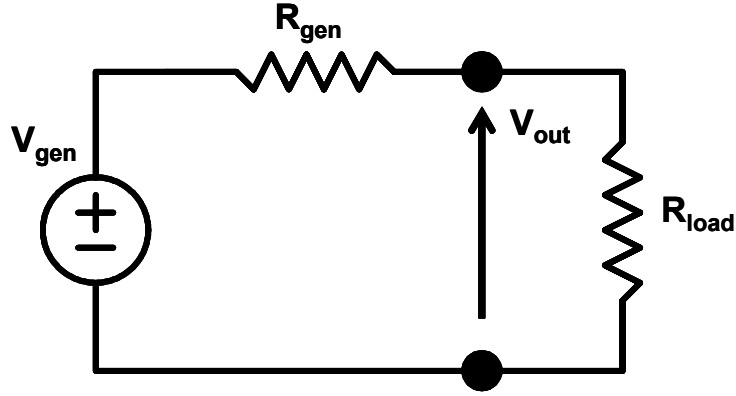
Figure 5. Load and generation resistance for calculation of maximum power transfer

The output power is given as

$$P_{out} = \frac{V_{out}^2}{R_{load}} \qquad (2.4)$$

where V_{out} can be represented in terms of V_{gen} through a voltage divider ratio.

$$P_{out} = \frac{\left[V_{gen} * R_{div}\right]^2}{R_{load}} \qquad (2.5)$$

where

$$R_{div} = \frac{R_{load}}{R_{load} + R_{gen}} \qquad (2.6)$$

Taking the partial derivative of P_{out} with respect to R_{load} and setting it equal to zero gives the condition that $R_{load} = R_{gen}$ for maximum power transfer. Using the complex representation of Z_{gen} and Z_{load} extends this analysis to all complex impedances, resulting in the complex conjugate relationship mentioned above.

In a situation where the system voltage is constrained, the maximum power transfer analysis begins to break down. The theory assumes small-signal operation, which is not the case in a power amplifier where the output voltage can swing as high as $2*V_{dd}$ for linear amplifiers. In this case, the maximum signal swing V_{max} is limited

to V_{dd}. As illustrated in Figure 6, if R_{load} was matched to R_{gen}, then the required voltage could be well above the supply rail. In this case, a load line match must be used, where

$$R_{load} = \frac{V_{max}}{I_{max}}$$ (2.7)

In this case, the system limitations result in a change in the output load from what would traditionally be expected from small-signal analysis. The effect of this type of match can be seen in Figure 7. The conjugate match provides higher gain, but because of the supply voltage necessary to maintain the Ohm's law relationship between I_{max} and R_{load}, the signal clips or compresses at a lower power level, given as P_{1dB}. At this point, the voltage swing has reached V_{max}, but the output current swing is far from I_{max}, resulting in less than the maximum power being delivered to the load. By using a load line match, the gain is reduced but the amplifier can now reach its full signal swing because of the choice of R_{load}. The new compression point using this approach is given as $P`_{1dB}$, and is the point where the output peak signal swing is both V_{max} and I_{max}, transferring the most power to the load.
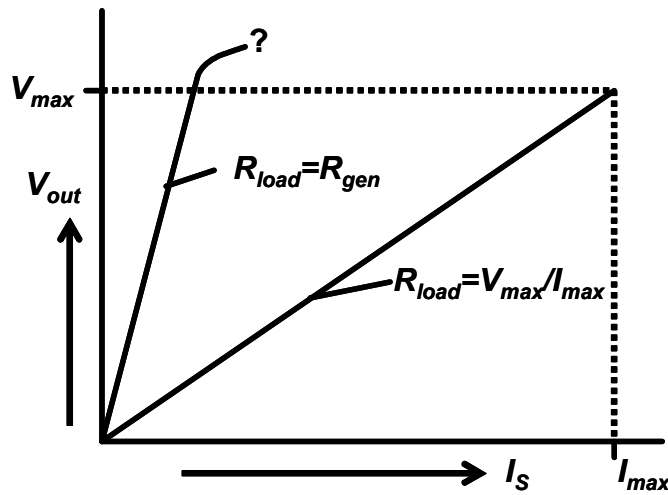
Figure 6. Conjugate match versus load line match under constrained system voltage
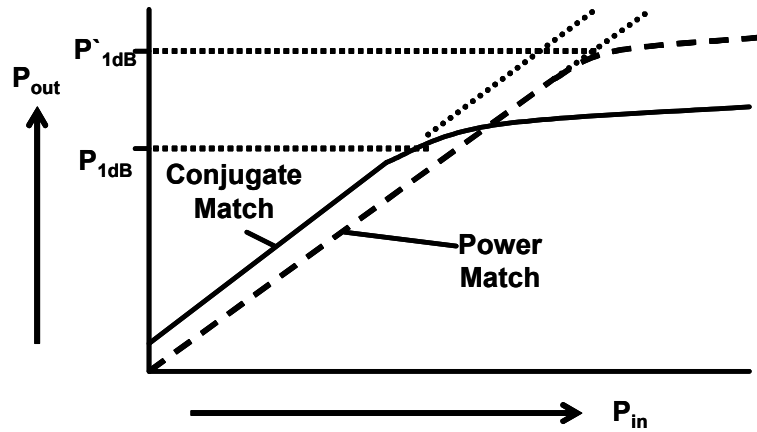
Figure 7. Input-output characteristic for a power amplifier with both conjugate match and load line match at output

This basic analysis is the starting point for design of most linear power amplifiers, with the load-line criteria determining the output matching components that are necessary to achieve the maximum desired power. From this point, the amplifier is designed "backwards" to the input, analyzing the performance requirements at each stage. This design approach will be explained in more detail later in this chapter.

2.4.2   *Small-signal S-parameter Analysis*

Traditional analysis techniques for RF and microwave circuits usually focus on the use of scattering or "S" parameter analysis for circuit design. Rather than present a review of s-parameter theory, this section will focus on some of the elements more pertinent to power amplifier design. S-parameters are primarily a small-signal design and analysis tool, but they can provide a starting point for power amplifier design as well. Impedance matching networks are most easily designed with the use of s-parameters and the smith chart, however this becomes challenging in power amplifiers because the impedances of the active components can change based on the signal level applied to them.

Stability is a constant concern in power amplifier design. High gain coupled with high signal swing and complex feedback paths through substrates, ground returns, and even the wiring traces themselves makes typical analysis approaches impractical. Traditionally, the stability of a circuit is determined by examining its transfer function and observing the behavior of the poles and zeros of the system. This is neither a simple nor intuitive approach for analyzing power amplifiers. Despite their apparent simplicity and similarity to traditional amplifiers, integrated multi-stage power amplifiers can have many complex feedback paths, such as substrate coupling, that are difficult to model in terms of traditional poles and zeros. A better approach to such a system is to model the power amplifier as a two-port network and analyze it in terms of power transmission and reflection, as is the case in s-parameter analysis. Theory states that for a two-port network to be stable, the real part of its impedance at the input and output must be positive for all frequencies and loads. Expressed in terms of the reflection coefficients Γ, the following criteria are established:

$$|\Gamma_S| < 1 \tag{2.8}$$

$$|\Gamma_L| < 1 \tag{2.9}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.10}$$

and

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2.11}$$

These criteria imply that the source and load are both passive, and the input and output impedances are also passive [23]. These equations can be manipulated to produce load and source stability circles on the smith chart. This provides a graphical

representation of what source or load impedances are required to have an unconditionally stable circuit.

When the input and output impedances are known, such as in a 50Ω system, the use of stability circles becomes excessive in examining the stability of the circuit. Instead, the stability factor K is introduced. Based solely on the s-parameters at each frequency, K can be used to ascertain and guarantee the stability of the circuit.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.12}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.13}$$

From these equations, the necessary and sufficient conditions for unconditional stability are

$$K > 1 \tag{2.14}$$

and

$$|\Delta| < 1 \tag{2.15}$$

With these conditions satisfied, the circuit will be unconditionally stable. Some circuits will exhibit *conditional* stability, where $K < 1$ and $|\Delta| < 1$. In these cases, stability circles are usually required to see what load and source impedances are required to operate the circuit in a stable fashion.

2.4.3 Time-domain Tuning

An interesting technique for the design of interstage matching circuits for a power amplifier comes in the form of time-domain tuning. This approach can best be

considered a transient replacement for large signal s-parameters. It has the added advantage of providing feedback to the designer on voltage levels and waveforms that might lead to transistor reliability issues or potential instability. The cost of such an approach is increased simulation time for very complex designs, though modern computer workstations are largely eliminating this concern.

The approach assumes the use of a two-element L-matching network for input and interstage matching, as shown in Figure 8. Time-domain tuning follows directly from the design methodology presented in the previous sections, beginning with the design of the output network and working backwards to the input. Proper device sizing and biasing concerns are dealt with directly and become an integral part of the technique.
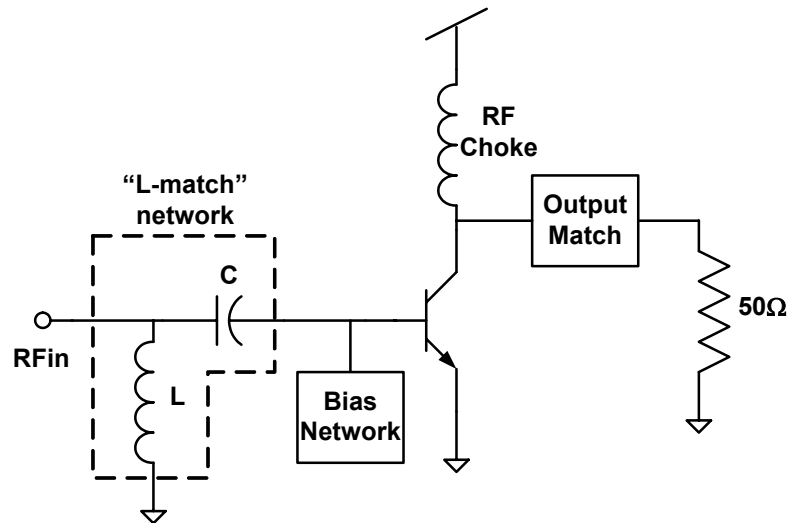
Figure 8. L-match at input to RF transistor using shunt-L, series-C configuration

Assume initially a simple two-stage linear amplifier, biased for class AB operation. Assuming accurate models, the impedances of the amplifier are going to be a function of the drive level provided at the input of each stage. To achieve the best performance at the maximum output power, the matching is done in the large-signal

region. Here it is assumed that the output matching network is already designed as described above, with the output transistor sized to deliver the appropriate amount of power to the converted load impedance.

From this point, the bias insertion network can be added. In the case of CMOS power amplifiers where there is no current into the gate (assuming negligible gate leakage current); this can be done with a suitably large resistance. For HBT based designs, the bias current can be sourced through an inductor that is resonated with a capacitor at the fundamental frequency, providing fairly large impedance compared to the input of the device.

The next step is to add a series capacitor in the signal path. It is assumed that the input impedance of the device will be fairly small, given the large transistor sizes needed to provide high output power. The capacitor transforms the impedance to a higher value to provide a load-line match for the first stage. To do this, an AC voltage source is attached to the input, and the voltage is set to the maximum peak-to-peak swing expected from the first stage. This is illustrated in Figure 9. Following from previous discussion, this would normally be twice the supply voltage, but a factor of safety of 10-20% is built into this voltage to prevent the first stage from saturating before the output. As mentioned before, this is a critical flaw the must be avoided for proper linear output.

The value of capacitor at the input is swept until the desired output voltage V_{out} is achieved. V_{out} should have a peak-to-peak swing of twice the supply voltage and should be the voltage that delivers the chosen maximum power into the output matching network. Alternatively, the voltage across the 50Ω termination can also be monitored.
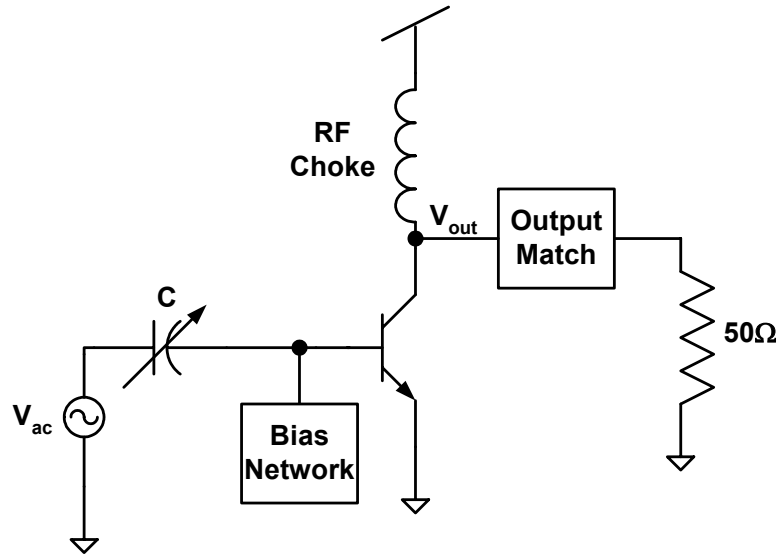
Figure 9. Determining series capacitor value using AC voltage source

Once the capacitance is determined, the shunt inductor can be added to the input of the circuit. This inductor is added to resonate with the series capacitor at the desired operating frequency, presenting a real impedance at the input of the matching network. This is done by adding an AC current source at the input as shown in Figure 10. In this step, the voltage at the input of the matching network is monitored while the value of inductance is varied. The goal is do develop the peak input voltage at that node, which corresponds to the point of resonance. Once the resonant value of inductance is found, the current level can be reduced or increased as necessary to develop the proper voltage level at the input, as determined in the previous step.

It is important to mention that this is an iterative process. The resonance of the network will depend on the drive level of the AC current source, because of the variations of the transistor input impedance with signal level. Thus once the value of current has been changed, a sweep over inductance value should be performed again to be sure the value still corresponds to the resonant peak of the network. Once this iteration is complete, the current level used in the simulation will be close to the operating current of the next stage of the amplifier, and can be used to properly size

the devices of that stage. In addition, by using this topology, the shunt inductor of the matching network can be used as the RF choke for the driver stage of the design, as shown in Figure 11.
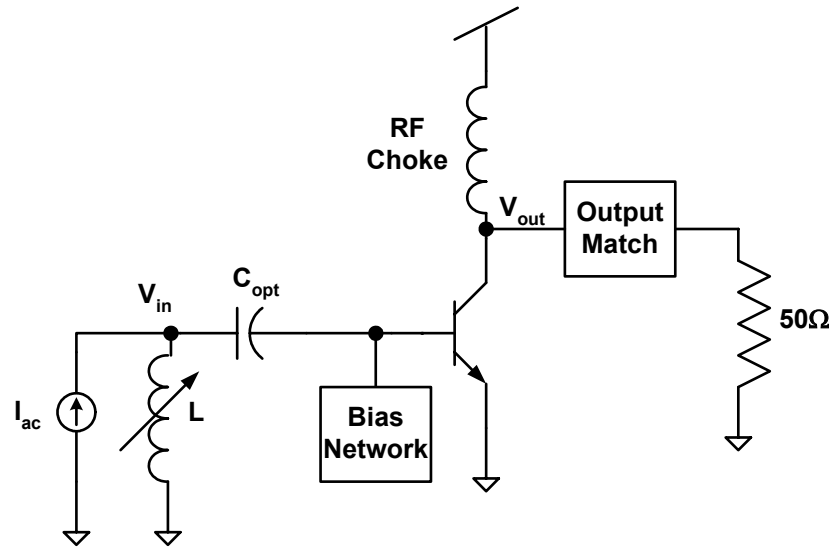
Figure 10. Determining shunt inductor value using AC current source
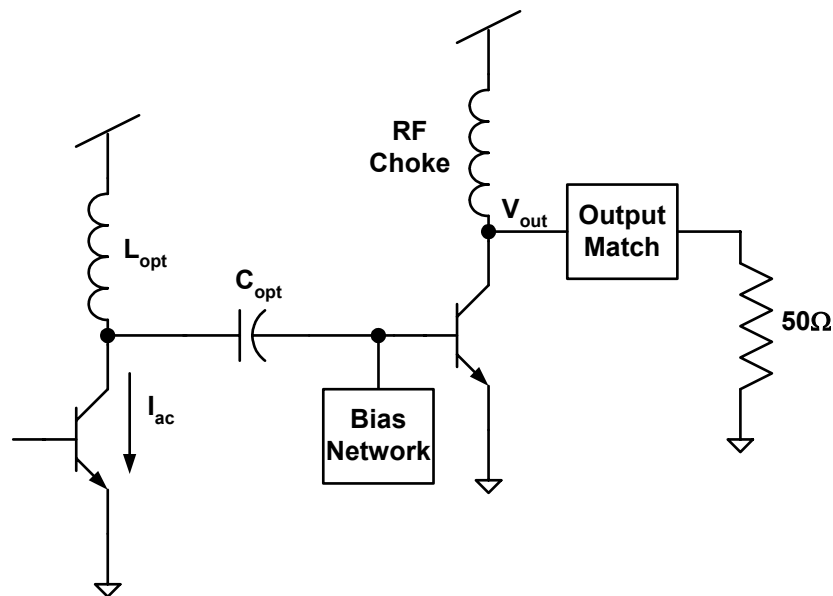
Figure 11. Addition of a driver stage, with operating current and choke inductor coming from interstage design

The time domain tuning approach can be repeated for the design of additional interstage matches depending on the number of stages needed in the power amplifier. This approach gives the designer a good feel for the signal levels that will be experienced in the final amplifier, more so than in a typical small-signal s-parameter design approach. The use of a load line match at the interstage boundaries ensures that the amplifier will not prematurely saturate, which is critical in the design of linear power amplifiers. It must also be stressed that this approach provides the **starting point** for a design, and that additional factors such as parasitic capacitances and inductances can de-tune the matching networks, resulting in reduced performance. Common optimization techniques available in most commercial simulation tools can be used to further refine the performance of the power amplifier as the design complexity increases.

2.5   Summary

This chapter provides an overview of power amplifiers and basic design techniques. The different classes of both linear and nonlinear power amplifiers were explained. The concept of a load-line match was presented, along with the required equations to design the output matching network of a linear power amplifier. S-parameter analysis for power amplifiers was introduced, with a focus on determining the stability of a circuit. Finally, the idea of time domain tuning was presented for use in the design of interstage matching networks in multi-stage power amplifiers. This background provides a starting point for the design of linear power amplifiers for RF circuit applications.

Chapter 3:   Efficiency Improvement Techniques for Power Amplifiers

3.1   *Introduction*

The maximum efficiency of an amplifier can be determined by its class of operation, as explained in chapter 2. Yet there are several techniques that can be used to improve the efficiency of a power amplifier throughout its operating region. These techniques are attracting more attention because of the incorporation of power control into wireless standards, as well as the use of non-constant envelope modulation schemes, such as CDMA and OFDM. In both of these cases, the transmitter may rarely or never transmit at the maximum output power, which shifts the focus on efficiency to lower power levels. The topics to be covered include dynamic biasing, architectures for improved efficiency, and finally variable supply voltage amplifiers.

3.2   *Dynamic Biasing*

The first and often simplest technique for improving the efficiency of a power amplifier is some type of adaptive bias control. This is achieved by default in the use of reduced conduction angle modes of operation (class AB, class B). In this case, the quiescent current of the power amplifier increases from a nominal value as the RF power increases. This can be expanded to offer 'low power' settings of bias current below a certain RF power threshold. This can be sensed on- or off-chip and bias

control can be implemented through various analog and digital feedback techniques. The variability of the gain in such a system is often the limitation of this approach.

This approach can be extended to provide a dynamic biasing scheme where the bias is adjusted to maintain the linearity requirements of the PA as well. By implementing a bias control circuit, the bias points of individual stages of the power amplifier can be adjusted to provide the minimum current necessary to meet linearity requirements at any given power level [24]. This approach offers improvements to both efficiency and linearity. Several challenges are presented by this approach, however. The system either has to adapt on-the-fly by having some method of sensing the linearity of the output signal, or the bias range must be set beforehand by the designer based on either simulation or initial measured results. The lack of a calibration feature for such a system may reduce its performance from chip to chip as process and environment change.

3.3   Linear, Efficient Architectures

3.3.1   Envelope Elimination and Restoration (EER)

The envelope elimination and restoration approach (also referred to as the Kahn technique after its inventor, Leonard Kahn) involves the use of two different amplification paths based on a polar decomposition of the RF signal [25]. This allows a nonlinear amplifier to be used to amplify the carrier (containing the phase data), while a lower frequency highly linear amplifier is used to amplify the envelope of the signal. These amplified signals are then combined at the output to produce an amplified version of the original signal. The general architecture of the system is given in Figure 12.
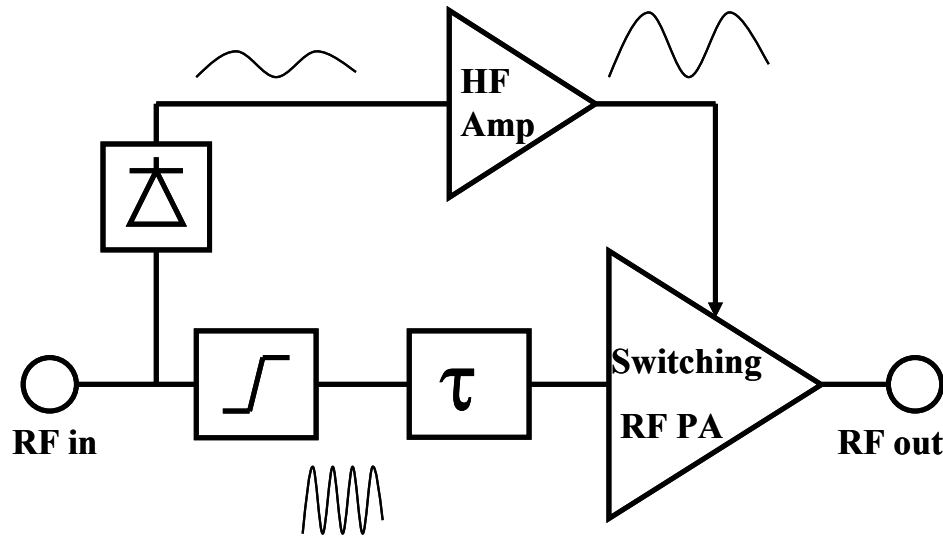
Figure 12. Envelope elimination and restoration (Kahn Technique) power amplifier architecture

The RF signal input to the system is passed through a limiter, effectively removing any amplitude modulation component. What remains is a fixed amplitude carrier that contains all the phase information for the transmitted signal. At the same time, an envelope detector strips off just the amplitude modulation or envelope of the signal. This is at a much lower frequency than the carrier, varying at the frequency of the baseband signal. This lower frequency signal can then be amplified by a much lower frequency amplifier, which ideally has a high efficiency. The limited carrier signal is then passed to a switching (or saturated) power amplifier that can amplify the carrier very efficiently as well. The two are recombined by applying the amplified envelope signal to the supply of the switching power amplifier, which re-modulates the carrier and produces an amplified version of the desired transmitted signal.

The one element not described yet is the delay block (τ in Figure 12). This block is very important for this system to work with modern digital modulation formats. Because data is contained in both the phase and the amplitude of the signal for non-constant envelope modulation, it is important to preserve this relationship after

the polar decomposition. If the recombined signal at the output has a time delay between the amplitude and phase information, the result will be reduced error vector magnitude (EVM) and ACPR performance, and ultimately loss of data [26]. This requirement is one of the current limitations on this type of amplifier, though prototype designs have been implemented [27]. The advances in DSP technology in baseband processing could eliminate many of the analog components in this technique by producing a direct polar-modulated waveform, making it once again viable for use in linear, efficient RF power amplifier and transmitter architectures [28].

3.3.2 *Doherty Amplifiers*

A second type of amplifier topology for improved efficiency is the Doherty amplifier. Based again on work done for high power tube amplifiers for broadcast purposes, this technique has become popular for modern RF power amplifiers because of the efficiency improvements it can offer as the carrier power is backed-off from its maximum. In this technique, the outputs of two amplifiers are combined in the proper phase alignment through the use of a passive power-combining network [29]. The basic configuration of the Doherty amplifier is shown in Figure 13.
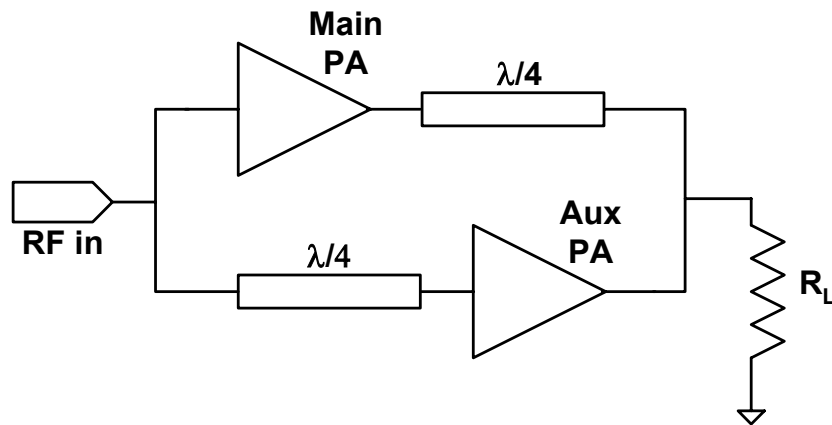
Figure 13. Block diagram of the traditional Doherty power amplifier architecture

Here, there are two PAs which operate in conjunction at high power to produce a linear signal. The λ/4 transmission lines act as the power combining network, the effect of which is to perform an active load-pull on the devices. The active load-pull technique is described in detail in [21], and summarized here. If a load resistance is acted upon by two generators that source complex currents $\mathbf{I_1}$ and $\mathbf{I_2}$, then the effective load impedance seen by generator 1 is modified to

$$\mathbf{Z_1} = R_L \left(1 + \frac{\mathbf{I_2}}{\mathbf{I_1}} \right) \tag{3.1}$$

The result is that if $\mathbf{I_2}$ is in phase with $\mathbf{I_1}$, $\mathbf{Z_1}$ is transformed to a higher resistive value, and likewise if $\mathbf{I_2}$ is 180° out of phase with $\mathbf{I_1}$, $\mathbf{Z_1}$ is reduced. In this respect, the amplifiers in the Doherty configuration act as generators that adjust the impedance seen at the output through proper combining of their power.

In a traditional Doherty amplifier, the main device typically saturates at ¼ of the maximum output power. Beyond this point, the auxiliary amplifier is used to source the power, providing a combined linear output up to the maximum output power. The results is to have a double efficiency peak, with one peak occurring at the maximum power, as expected, and the other at 6dB less, from the main amplifier. This technique as been extended to include multiple stages of amplifiers, producing an additional efficiency peak for each amplifier added [30].

The drawbacks for this approach are the need for the λ/4 transmission lines depicted in Figure 13. At typical cellular frequencies from 900MHz to 2GHz, these transmission lines consume considerable board/module space. In an industry looking for increased integration and smaller designs, this approach is directly opposed to that goal. Some work has been done to implement such a system using lumped elements in place of the transmission lines [31]. The performance of such an amplifier has proven comparable to the transmission line architecture, while occupying considerably

less board area. The linearity of such an approach may be an issue, possibly requiring further linearization to be a viable option for RF circuit applications.

3.4   Variable Supply Voltage

Another way in which the efficiency of a power amplifier can be improved is through the variation of the PA supply voltage. This seems counterintuitive because it was previously explained that power amplifiers are designed to have maximum efficiency based on their load-line characteristics, which constrain the problem by both the power amplifier current and the supply voltage. The initial reaction is that by varying the supply voltage, the load line would be changing and the efficiency would decrease.

This would be true if the supply voltage was reduced when the amplifier is operating at maximum power. The key to this approach is the variation of the output power with time. The average output power of a PA in a CDMA system, for example, is given as a probability density function provided by the CDMA Development Group (CDG) for both urban and suburban locales. Because of the high population densities of urban locations, this is the more commonly used distribution. This distribution is given in Figure 14.
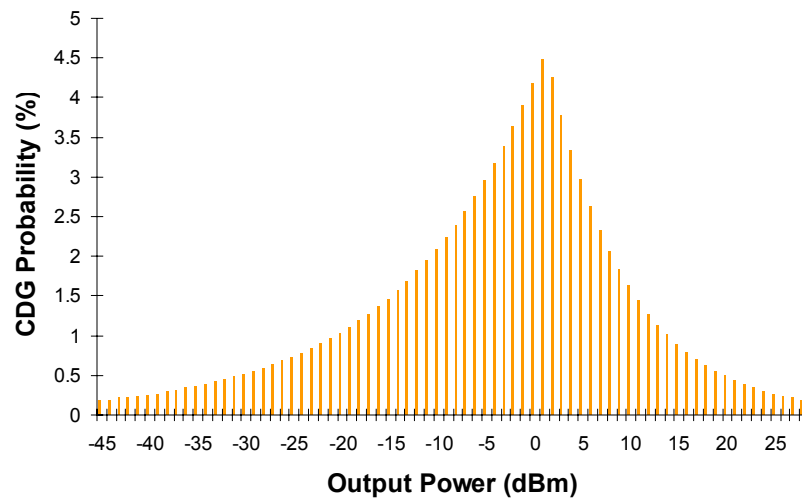
Figure 14. CDG probability curve for urban operation

Based on the CDG distributions, it can be seen that the power amplifier is operating at its maximum power quite infrequently. When the PA is not operating at maximum power, the current drawn by the PA is less than the ideal load-line approximation (assuming anything other than class A operation). The efficiency improvement can be viewed in either of two ways. First, if the current is changing and the output match is fixed, then the efficiency is degrading because the load-line condition is not being satisfied. This is illustrated in Figure 15(a). Here the DC bias current is reduced (as in class AB operation) at lower output power. Because the supply voltage is not changing, there is additional headroom in the signal swing that is not being utilized because the load line condition is not met. By reducing the supply voltage as in Figure 15(b), the efficiency is improved by moving the operating point to maintain the original load-line condition, ensuring operation near the peak current and voltage the amplifier is capable of delivering.
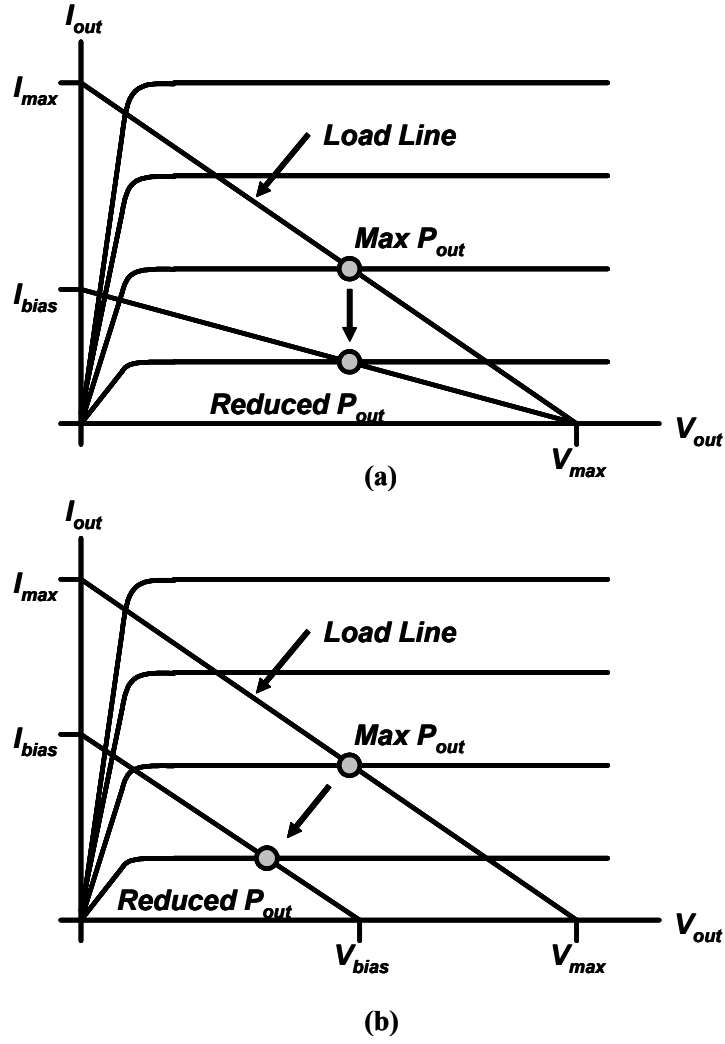
Figure 15. Representation of current-voltage characteristics of a power amplifier showing variation of operating point in a class AB amplifier under (a) normal operation and (b) variable supply voltage operation

A second way of viewing the efficiency improvement is to look at the DC power loss component of the efficiency. If power added efficiency (PAE) is defined as

$$PAE = \frac{P_{RFout} - P_{RFin}}{V_{DC} \cdot I_{DC}}$$

(3.2)

then at lower output power, reducing the DC supply voltage directly improves the PAE of the amplifier. This assumes that RF voltage swing is set entirely by the output matching network, which is a valid assumption, given the load-line approximation.

Although the benefits of a variable supply voltage have been addressed in part by several authors [32,33] there still exists a need for a concise, intuitive analysis that can accurately describe the system-level advantages of this approach. Despite the apparent efficiency improvement described above, the true performance advantage of a variable supply voltage using a DC-DC converter is best expressed through the application of the CDG probability curves to the analysis of the battery current drawn from the amplifier.

3.4.1   System Architecture

The variable supply voltage is best realized using some type of switching voltage converter. A linear regulator could be used to reduce the supply voltage, but the losses through the regulator would overshadow any efficiency improvements seen in the power amplifier. A switching converter provides high efficiencies over a broad range of load currents and output voltages. The general system architecture of an adaptive power amplifier employing this technique is shown in Figure 16.
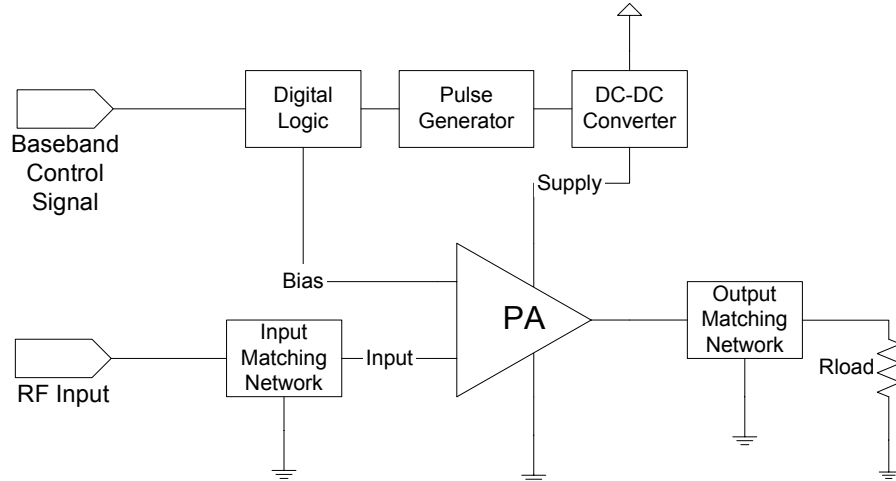
Figure 16. Variable supply voltage power amplifier system architecture

The power amplifier's supply voltage is provided through a DC-DC converter, which is in turn controlled by a power control signal from the baseband processor. This signal adjusts either the bias of the PA, the supply voltage, or both. The supply voltage in the DC-DC converter is controlled by a pulse generator that determines the duty cycle of the switches in the converter. The overall effect is to adjust the operating point and/or supply voltage of the amplifier based on the output power to be transmitted, where adjustments to the bias can be used to maintain a constant gain in the power amplifier, if so desired.

3.4.2   *Battery Current Analysis*

The total battery current drawn by a power amplifier using a variable supply voltage can be analyzed as follows. Assume initially that the amplifier is biased for class AB operation. In this case, the PA will have a low quiescent current at low RF power levels. The current drawn from the battery (I_{load}) will then increase linearly with the output power (in Watts) or on a linear-in-dBm scale, it will appear to increase exponentially as in Figure 17.
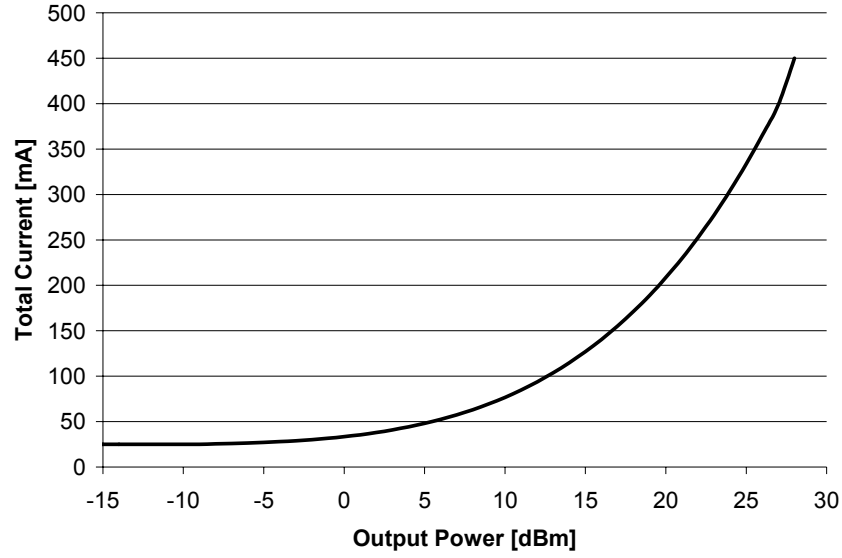
Figure 17. Typical class AB power amplifier DC current consumption versus output power

With the introduction of a DC-DC converter between the battery (V_{batt}) and the supply voltage of the power amplifier (V_{load}), the current drawn from the battery (I_{batt}) is no longer equal to the DC current of the power amplifier (I_{load}). It is instead given by the following equation,

$$I_{batt} = \frac{V_{load} \cdot I_{load}(P_{out})}{\eta \cdot V_{batt}} \qquad (3.3)$$

where η is the efficiency of the DC-DC converter. This is then combined with the probability density function of the output power $p(P_{out})$ based on the wireless standard of interest. The average battery current can then be found by multiplying $p(P_{out})$ by (3.3) and integrating.

$$\overline{I_{batt}} = \int p(P_{out}) * I_{batt}(P_{out}) \qquad (3.4)$$

The analysis becomes more complicated when the actual converter and power amplifier performance is included. The DC-DC converter will most likely not have a

constant efficiency versus load current. Additionally, the supply voltage is now being varied with the output power through the DC-DC converter. The analysis must be modified to include these variations.

$$I_{batt}(P_{out}) = \frac{V_{load}(P_{out}) * I_{load}(P_{out})}{\eta(V_{load}, I_{load}) * V_{batt}} \qquad (3.5)$$

By making V_{load}, and η functions of P_{out}, I_{batt} can now be defined as a function of the converter parameters.

The efficiency of the DC-DC converter, η, can be expressed as a function of P_{out} because of its relation to I_{load} and V_{load}. This will not be a direct relationship, but will rather be defined by the contour of the DC-DC converter efficiency versus both variables. The actual choice of supply voltage for the PA at any given power level will be determined by the designer on a case-by-case basis. With an expression for converter parameters expressed as a function of output power, the expression for average battery current can now be modified to be the integral of the new battery current weighted by the probability density function at each output power level.

$$\overline{I_{batt}} = \int p(P_{out}) * \frac{V_{load}(P_{out}) * I_{load}(P_{out})}{\eta(P_{out}) * V_{batt}} \qquad (3.6)$$

Once the designer has chosen the desired supply voltage range for the power amplifier and has determined the characteristics of the converter efficiency versus load voltage and load current, the battery current analysis can be used to show the average battery current savings that can be achieved by using a variable supply voltage approach.

3.5   *Summary*

While several architectures exist for realizing efficient linear power amplifiers, the variable supply voltage approach offers the most pronounced efficiency improvements while being realizable in an integrated form using current technology

processes. Due to the large operating range of output power required by CDMA systems, the variable supply voltage can best adapt to the required power level while providing adequate performance under efficiency control. A new method for calculating the overall battery current savings has been developed, providing designers with the ability to evaluate the overall talk-time improvement that can be offered by such a system. This analysis demonstrates the improvements that can be offered when such a system is combined with an existing power amplifier.

The key to the broad adoption of this approach, however, lies in the ability to integrate such supply voltage control on the same die as the power amplifier, thereby reducing the cost of such a system and providing efficiency improvement in a package consistent with current power amplifier modules. As transceiver integration progresses further, the control and adaptive capability can be extended to the entire radio with control originating from a baseband controller that can adjust various parameters to meet the needs of the system under changing environmental circumstances.

Chapter 4:   A WCDMA Power Amplifier in SiGe Technology

4.1   *Introduction*

Compound semiconductors such as GaAs have dominated power amplifier design for wireless communications. The advantages of semi-insulating substrates and high-performance devices have overshadowed the cost and integration advantages of silicon. With the introduction of the SiGe processes with their graded-base HBT devices, power amplifier designers now have an alternative to GaAs for cellular and wireless LAN applications. The integration capabilities of a silicon-based process that can deliver power performance are many. From simple bias circuits and power controls to fully integrated transceivers, the ability to craft power amplifiers in this technology opens the doors to new levels of RFIC integration. To date, several SiGe-based power amplifiers have been presented that meet the requirements of modern communications systems, including cellular and WLAN systems [34-40].

This chapter describes the challenges faced in the design of a differential SiGe power amplifier. The target application for this device is wideband CDMA (WCDMA) handset power amplifiers. The power amplifier design approach is described, including detailed information on the target specifications and the design of each stage of the amplifier. Simulation results are provided, and the layout techniques used in the design are highlighted. Finally, measured circuit performance is given, along with discussion of the testing procedure.

4.2 Power Amplifier Design

This WCDMA power amplifier was designed using the time-domain tuning approach explained previously. This basic design approach was augmented through the use of harmonic balance simulation tools to perform fast swept-power analysis, as well as advanced simulations such as two-tone and modulated waveform analysis. A differential architecture was chosen for the power amplifier to reduce its susceptibility to common mode noise on the power supply, as well as to reduce the effect of emitter inductance on the overall amplifier performance.

Time-domain tuning has the advantage of providing intuitive, visual feedback on the waveforms that are being applied to the amplifier, provided they are simple sinusoids. This allows the designer to monitor the swing of critical voltages and currents. Transient simulations begin to lose their appeal as the circuit become more complex and requires more and more time to simulate. Modern computer workstations can handle quite complex circuits in transient simulation, but even these have difficulty simulating large ranges of power levels or multiple-frequency inputs.

When these more advanced simulations become necessary, it is best to turn to a tool that uses harmonic balance simulation. Harmonic balance is a frequency domain technique that can handle complex signals and highly nonlinear circuits. This allows for large-signal simulations like power sweeps with single and multiple tones. These simulations are critical to establish the power performance of the amplifier, focusing on 1-dB compression point analysis and intermodulation distortion (IMD or IM3).

Simulation of critical design parameters such as adjacent channel power (ACPR) requires the use of even more complex simulation techniques. These simulations require a modulated signal to be passed into the amplifier to observe the impact of the circuit nonlinearities on the actual communication signal. Envelope

transient simulation can be used in this situation by combining harmonic balance analysis at the carrier frequency with transient analysis of the envelope of the modulated waveform [41]. The combination of the two simulations provides the designer with all the analysis tools required to determine the power amplifier performance.

4.2.1   Target Specifications

The target application of this power amplifier is the mobile handset power amplifier of a 3G WCDMA system. The system specifications are defined by the Third Generation Partnership Program (3GPP) and determine the transmit power, linearity, and band spectrum requirements. Within the required specifications, the designer is free to exercise his or her creativity in the circuit design. This is somewhat of a misnomer, however, because future specifications such as those presented by 3GPP have become so stringent that they push the designer into an established topology and class of operation.

As a non-constant envelope modulation scheme, WCDMA requires a highly linear power amplifier to prevent signal distortion upon transmission. Also, this non-constant envelope results in signal peaks that can be as much as 5dB above the average transmit power [42]. To handle this peak-to-average ratio (PAR), the amplifier's saturated power must be at least 5dB above the linear power, or the amplifier must be operated in the "backed-off" regime, operating at the maximum power possible while still maintaining the ACPR requirement [43]. The bandwidth of the signal transmitted in WCDMA is 3.84MHz, allowing for data communication rates upwards of 1 megabit per second (MBPS) [44]. The important parameters for power amplifiers in a WCDMA handset application as defined by the 3GPP organization are listed below in Table 1.

Table 1. Target specifications for WCDMA power amplifier

Specification	*Value*
Frequency Range	1.92-1.98GHz
Maximum Output Power	27dBm (power class 2)
Linearity (ACPR)	-33dBc @ 5MHz offset
	-43dBc @ 10MHz offset
Power Added Efficiency	$\geq 30\%$

It is important to note that the entire design procedure detailed here is an iterative process: as complexity is added through additional stages, layout parasitics, etc. it is important to examine the previous work that has been done to make sure that all previously calculated component values are still correct for the signals and impedances presented to each stage.

4.2.2 Output Matching Network Design

As mentioned in chapter 2, the output matching network is not so much an impedance matching network as it is an impedance *transformation* network. For maximum power transfer in a voltage (or current) constrained system, the power transfer must follow the load-line behavior, rather than the maximum power transfer theorem. This is most prevalent at the output of a power amplifier. To deliver the maximum power into 50Ω using a conjugate match would require a supply voltage of 7.1 volts for an output power of 27 dBm. Since this is not available in modern battery systems, the load-line match is used.

The optimal transformed load impedance is calculated using the following equation:

$$R_T = \frac{(V_{CC} - V_{CEsat})^2 * \eta_{OM}}{2 * P_{out}} \tag{4.1}$$

where V_{cc} is the supply voltage, V_{CEsat} is the collector-emitter saturation voltage (knee voltage), P_{out} is the maximum desired output power (in Watts) and η_{OM} is the efficiency of the output matching network. Using $V_{CC} = 2.7V$, $V_{CEsat} = 0.25V$, $P_{out} = 0.25W$ (24 dBm per side) and $\eta_{OM} = 0.89$ (~1 dB loss), R_T is calculated to be 10.7Ω.

The output matching network was chosen to be a series-L shunt-C matching network, as illustrated in Figure 18. This topology was chosen because the bondwire inductance that comes from packaging the chip can be included in the series inductance without degrading performance. If the inductance is realized as a transmission line, then the shunt capacitor placement can be varied along its length to tune the output match to the proper value during testing. The RF choke inductor is not shown for simplicity, but it can also be included as a shunt element to the left of the series inductor.
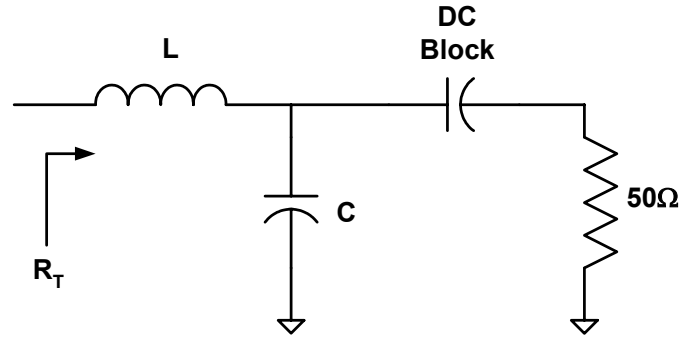
Figure 18. Topology of output matching network, including DC blocking capacitor

With R_T calculated, the component values for the output matching network can be found using the following equations:

$$X_C = \frac{R_O}{\sqrt{m-1}} \tag{4.2}$$

$$X_L = R_T * \sqrt{m-1} \tag{4.3}$$

where

$$m = \frac{R_O}{R_T} \tag{4.4}$$

X_C and X_L are the reactances of the matching network capacitor and inductor, respectively. R_O is the output impedance, in this case 50Ω, and R_T is the transformed load impedance previously calculated. Using (4.2) and (4.3), the values of C and L for a match at 1.95GHz are 3pF and 1.63nH, respectively. With the output match component values determined, the design of the output stage transistors can begin.

4.2.3 Output Stage Design

The output stage is composed of many devices connected in parallel to provide the desired output power to the transformed output impedance. Based on the desired output power, the peak RF current (per side) can be determined, which in turn dictates the size and multiplicity of the devices used. This can be calculated as

$$I_C^2 = \frac{2P_{out}}{R_T} \tag{4.5}$$

For this design, the maximum output current was calculated to be 306mA per side.

The devices chosen for this design are high-breakdown SiGe HBTs with maximum f_T of 27GHz. A two emitter finger device was chosen to provide increased device density, reducing the overall size and number of parallel devices. Based on previously published results [36], the desired emitter size was 20μm^2 per device, or 10μm^2 per finger. The width of the emitter fingers was chosen to be 0.8μm, giving an emitter length of 12.5μm. Based on f_T vs. collector current data, the peak f_T occurs when the devices are biased at 6mA per finger (for 12.5μm x 0.8μm emitter fingers), with maximum rated current at 7.5mA per finger. However, due to limitations in the

number of vias contacting the emitter fingers of the devices, safe operation limits the maximum current per finger to < 2mA. Despite this reduction in current, f_T for these devices is still estimated to be > 22GHz, allowing for adequate gain at 2GHz. Using this reduced current per finger, the output devices were sized to be $1200\mu m^2$ of emitter area each, or 60 parallel devices per side.

At high current levels, the heat dissipated by the HBTs can create positive thermal-electric feedback. Due to resistive losses and current distributions, this can be localized to one or a few devices or fingers. These local hot spots can lead to breakdown in the form of thermal runaway. Emitter ballasting is employed to prevent this thermal runaway in large signal operation [45]. The emitter ballasting resistors help distribute the current evenly between the emitter fingers of the devices to limit thermal differences between transistors. Both the driver and the output stage use 4Ω resistors in series with every two $10\mu m^2$ emitter fingers. Because of the large number of emitter fingers in both the driver and output stage transistors, the parallel resistance in the emitter is very small and has a minimal effect on the output voltage swing of each device.

4.2.4   Interstage Matching Network Design

Proper design of the interstage matching network can be critical in determining the success of a power amplifier design. It is a challenging area because it represents the interface between two nonlinear circuit elements. But by following a few basic rules of power amplifier design, the difficulties can be overcome and a good interstage match can be achieved.

The theorem of maximum power transfer says that to achieve the highest power transfer between impedances, they should be the complex conjugate of each other. The breakdown of this theorem has already been discussed in chapter 2, but

will be summarized here again. In a battery voltage constrained system such as a handset power amplifier, the peak RF voltage swing is twice the supply voltage. In most cases, this becomes the limiting bound on the power transfer, requiring a load-line analysis as mentioned previously.

The time-domain tuning technique can be used in this case to achieve that result without having to calculate the input impedance value of the output transistor (which can vary depending on the power delivered to the device). Again, this technique provides the optimum matching at the largest signal swing the device should experience, ideally giving the peak gain and efficiency performance.

The first step in any interstage design is to ensure that the first stage (referred to here as the driver stage) does not saturate before the second stage (the output stage). **This is the cardinal rule of linear power amplifier design.** If the stages driving the output saturate first, it becomes almost impossible to drive the output stage to its maximum linear power, resulting in sub-par performance. If the interstage matching network of such an amplifier is off-chip, it can be tuned to fix this problem. But increasing integration is pushing matching network on-chip, which would be a challenge to fix without resorting to fuses or laser trimming of the completed die, which increases production cost.

To design the actual network, a series capacitor was placed at the base of the output stage transistor. To supply bias to the device, a shunt LC tank was placed at the base of the transistor as shown in Figure 19. The tank values were chosen to resonate at the center of the frequency band of operation with a peak at 1.95GHz. This gave component values of $C = 3.52pF$ and $L = 1.8nH$.
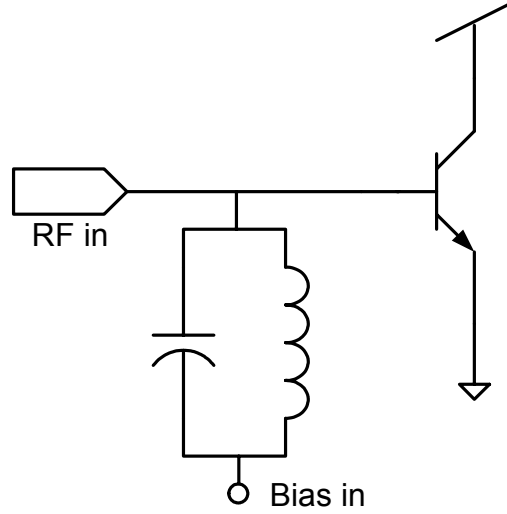
Figure 19. Tank circuit for amplifier base bias

To calculate the actual impedance of the tank, the Q of the inductor must be included in the analysis. The Q of the capacitor may also be included, but because an on-chip inductor is used, its Q factor will be considerably lower and will dominate the loss. Assuming an inductor Q of 12 (reasonable for a small on-chip spiral inductor in this technology [17]), the impedance of the tank is calculated as follows. First, the parallel resistance of the inductor is found based on its Q. This is given as

$$R_{LP} = Q\omega L \tag{4.6}$$

From this point, the impedance of the tank, Z_{tank}, can be written as

$$Z_{\tan k} = X_C \| X_L \| R_{LP} \tag{4.7}$$

where

$$X_C = \frac{1}{\omega C} \tag{4.8}$$

$$X_L = \omega L \tag{4.9}$$

or to simplify calculation, it can be expressed in terms of admittance,

$$Y_{\tan k} = Y_C + Y_L + G_{LP} \qquad (4.10)$$

where

$$Y_C = \omega C \qquad (4.11)$$

$$Y_L = \frac{1}{\omega L} \qquad (4.12)$$

and

$$G_{LP} = \frac{1}{R_{LP}} \qquad (4.13)$$

At the resonant frequency of the tank, the contributions made by the capacitor and the inductor will disappear from the admittance equation, leaving the minimum admittance $Y_{tank,min} = G_{LP}$.

$$\left| Y_{\tan k,min} \right| = \sqrt{G_{LP}^2 + \left(\omega L - \frac{1}{\omega C} \right)^2} = G_{LP} \qquad (4.14)$$

This gives a maximum tank impedance $Z_{tank,max}$ of $1/G_{LP}$ or 240Ω. While not very large, this impedance is high compared to the input impedance of the large parallel devices.

Once the bias tank was designed and included in the schematic, a sinusoidal voltage source at 1.95GHz was attached to the series capacitor. The value of this voltage was set at 80% of the peak swing of the output stage to help ensure that the driver stage will have the required headroom to prevent early saturation. This gave a value of 2.15V peak. Using the time-domain tuning technique, the value of the capacitor was swept until the voltage at the collector of the output stage reached its peak. The value of capacitor that achieved maximum output swing was found to be 0.6pF.

Once this value was determined, the voltage source was removed and a shunt inductor was attached to the capacitor. A sinusoidal current source at 1.95GHz was placed at the input of the network. This current source represents the output current of the driver stage transistor. An initial guess at the amplitude of the current source was made as $1/10^{th}$ the collector current of the output stage. Using this current, the inductor value was swept to find the resonant peak in the voltage developed across the current source. This value represents the inductance that resonates out the input capacitance of the network, providing a purely real impedance to the current source.

The goal of this approach is to find a current value and an inductor value that produce a resonant peak voltage of the value used in the first step, or 2.15V peak. This is an iterative process because as the current is decreased, the impedance of the network will change due to the drive-level dependence of the output stage transistor's input impedance. As the current is either reduced or increased from the starting guess, the inductance needs to be swept to ensure that the proper resonance is maintained. The final values for this circuit were 18mA of output current and 1.0nH of shunt inductance. This shunt inductor is then connected to the supply voltage and becomes the RF choke of the driver stage.

It is important to note that the driver stage transistor will have some finite output capacitance that will de-tune the interstage matching network. Once this stage has been designed and connected, the interstage match can be re-tuned by sweeping the value of the interstage inductor to find the value that causes a resonant peak in the collector voltage of the driver stage.

4.2.5   Driver Stage and Input Match Design

With the interstage match completed, the value of current from the final step of time-domain tuning can be used to size the driver stage devices. Using the rule of

thumb of 1mA per device (from the previous output stage design analysis), the driver stage was created with 5 parallel 20 μm^2 emitter area devices with two fingers each.

Once the driver stage devices were chosen, the input matching networks were designed. S-parameter simulations were used to design the input matching networks because they would interface with standard 50Ω cables for testing.   If a third stage would have been necessary, the steps described above for design of interstage matching networks would have been used. In this case, the margin for the voltage swing would have been reduced to 60% of the peak output swing to provide headroom to avoid early compression.

The same LC tank structure from the output stage was used for the driver stage bias input. The input match consists of the bondwire inductance, a series capacitor, and a shunt inductor. Basic s-parameter analysis was used to design the input match since the circuit would be matched to the 50Ω source impedance. The topology of the input matching network is shown in Figure 20. The final values for L and C were 2.5nH and 3.8pF, respectively.
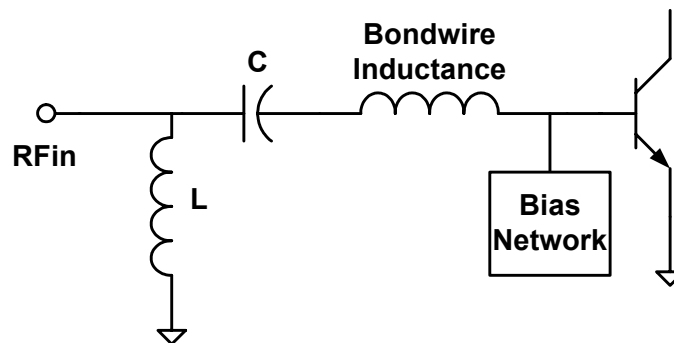
Figure 20. Input matching network topology for one half of the differential power amplifier

4.2.6   Final Circuit Schematic

The simplified circuit schematic for the full power amplifier is shown in Figure 21.
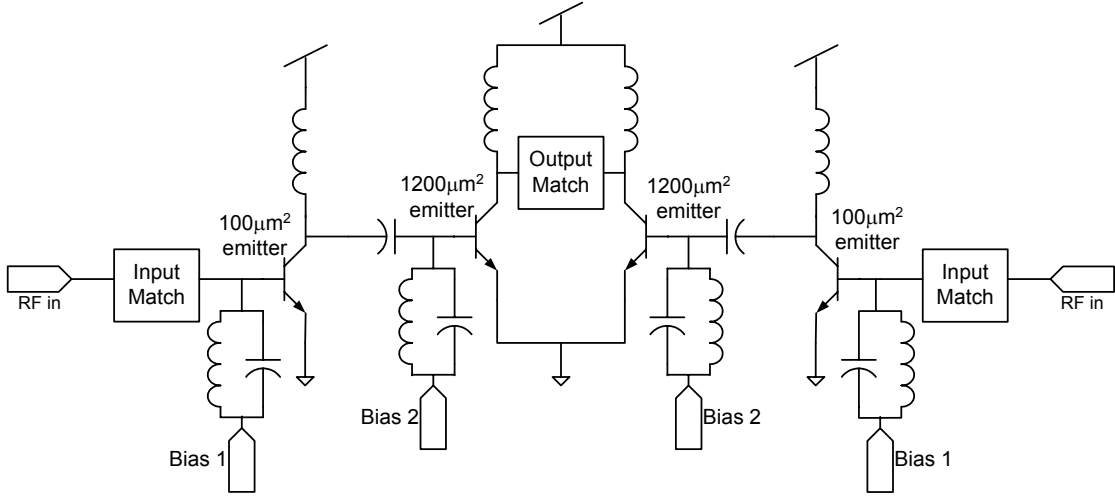
Figure 21. Final schematic of full power amplifier design

The differential structure of the power amplifier can be seen in the figure. The base biases for the two stages are provided through current mirror transistors also located on-chip. The common-mode node of the bias insertion points is heavily decoupled through the use of MOSFET capacitors to reduce the sensitivity of these nodes to common-mode signals such as ground-bounce. Not shown in the schematic are the bondwire inductances which are modeled at the chip to board interface. These bondwires are assumed to have approximately 1nH of inductance each, thus the use of parallel bondwires is assumed and reflected in the values used in simulation.

4.3   Simulation Results

The power amplifier is designed to operate in either class A or class AB while still achieving the desired gain and output power. The class AB power amplifier sacrifices small-signal gain for slight gain expansion at higher output power, which

improves the 1-dB compression point of the amplifier. For class A operation, the PA output stage is biased at 450mA collector current, while the driver stage is biased at 54mA. To bias the PA as a class AB amplifier, the output stage collector bias current is reduced to 140mA and the driver stage is reduced to 20mA. Small-signal S-parameter results for both classes of operation at 1.95GHz are given in Table 2.

Table 2. Simulated S-parameters for Class A and Class AB power amplifier at 1.95GHz

S-parameter	*Class A*	*Class AB*
S11	-16.6 dB	-13.0 dB
S22	-6.4 dB	-6.0 dB
S21	33.4 dB	31.4 dB
S12	-52.5 dB	-47.7 dB

Single-tone harmonic balance simulations were run using GoldenGate on both classes of operation to determine gain, output power, and PAE versus input power. Figure 22 and Figure 23 show gain and output power for class A and AB operation, respectively. P_{1dB} for the class A amplifier was 26dBm of output power, while for the class AB amplifier it was 24dBm of output power. The power added efficiency at the 1-dB compression point is 25% and 32% for class A and class AB, respectively.
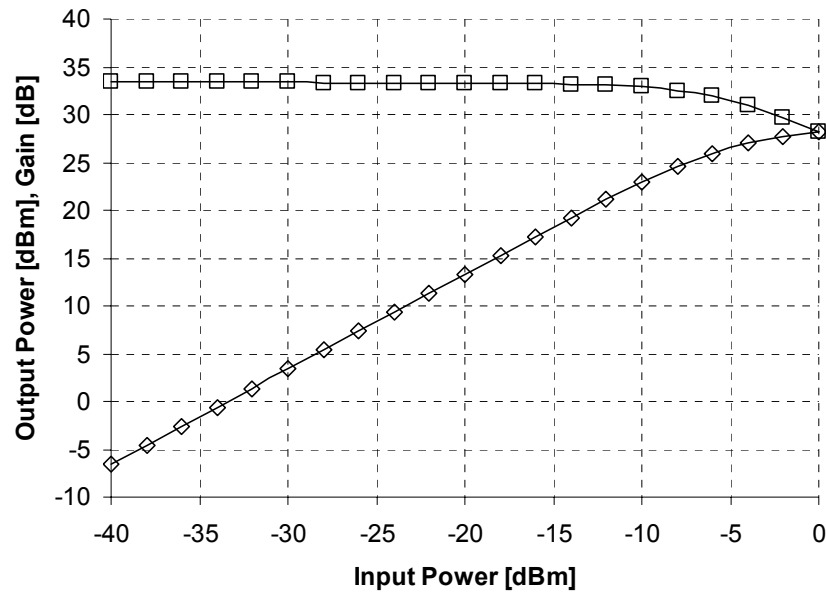
Figure 22. Simulated output power and gain vs. input power for class A biasing
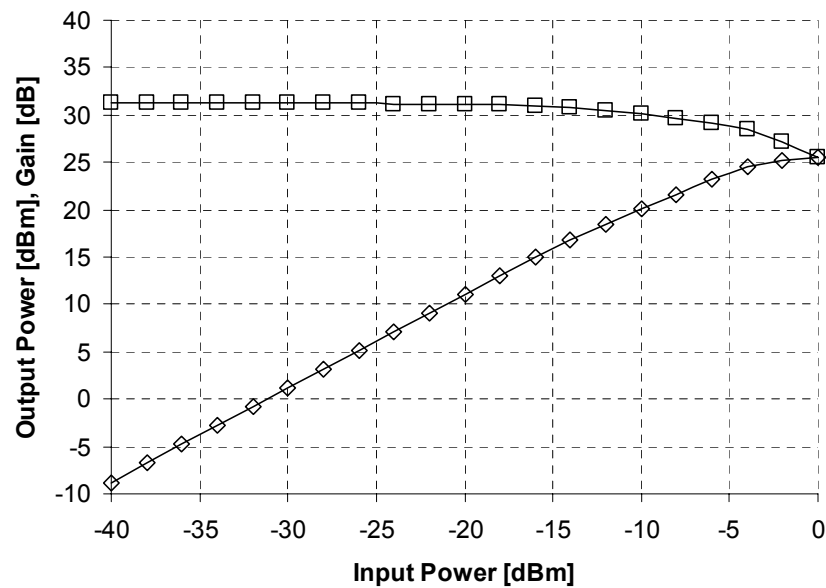
Figure 23. Simulated output power and gain vs. input power for class AB biasing

These results indicate that to achieve the target specifications, the power amplifier should be operated in class AB, thereby attaining both the gain and PAE

goals. The class A operation exhibits a larger linear output power range, which could be of benefit for meeting ACPR requirements, but at the cost of reduced efficiency.

4.4   Layout Techniques

Layout is a critical issue that must be addressed in all power amplifier designs. The additional resistance, capacitance, and inductance presented by the physical layout of the circuit can have a large impact on the tuning and performance of the power amplifier. The IBM SiGe 6HP technology includes several elements that help reduce these effects in layout. The process has 6 layers of metal with a top "analog metal" (AM) layer that is 4μm thick, separated from the previous layer by 3μm of oxide. This layer has a DC current handling of 6.17*(w-0.06) mA, where w is the width of the trace in microns. This is almost 5x the handling of the lower metal layers. The sheet resistance R_S of this layer is much lower also, because of the increased thickness. R_S for the AM layer is only 7 mΩ/□. These parameters make the analog metal layer highly desirable in PA design and alleviate many of the traditional layout concerns.

Because of the sheer size of the output stage transistor and the current levels in the amplifier, large runs of metal are required to connect all the parallel devices, as well as connecting the transistor to the rest of the circuit. At this point, it is instructive to mention the Greenhouse equation. This is a useful tool for estimating the inductance of metal runs in IC layout. The equation is a method of calculating the inductance of a long, flat bar of metal [46]. Greenhouse showed that for a thin-film inductor with rectangular cross section, the inductance can be given as

$$L = 0.002 \cdot l\{\ln[2l/(a+b)] + 0.50049 + [(a+b)/3l]\} \qquad (4.15)$$

where *l* is the length of the bar and *a* and *b* are the rectangular dimensions of the cross section. Using this equation, estimates can be made for the parasitic inductance of long runs of metal used in layout of the power amplifier. These are important to include in simulation, because they can be significant, on the order of hundreds of picohenries depending on the thickness and length of the run. Yet increasing the width of any traces also increases the parasitic capacitance to the substrate, which should also be analyzed to find an optimum trace size for critical wires.

4.4.1 Critical Layout Areas in Power Amplifiers

As mentioned above, the layout of medium to high power amplifiers must be carefully considered when designing the circuit. One of the most critical concerns is ground inductance. Any inductance presented at the emitter of the transistors will act as a voltage divider with the device itself, reducing the amount of signal transferred to the base of the transistor. This is illustrated in Figure 24, where the transistor is replaced by a simple small-signal model. The effect of the inductance is to reduce the output voltage for a given input voltage by reducing the voltage drop across the base-emitter junction of the transistor, thereby reducing the current g_m*V_{be}. This directly impacts the gain of the amplifier and the power transferred to the next stage. Ground inductance is a particular problem in single-ended designs where it can be very difficult to have a low inductance path to ground, depending on the technology and packaging of the chip.
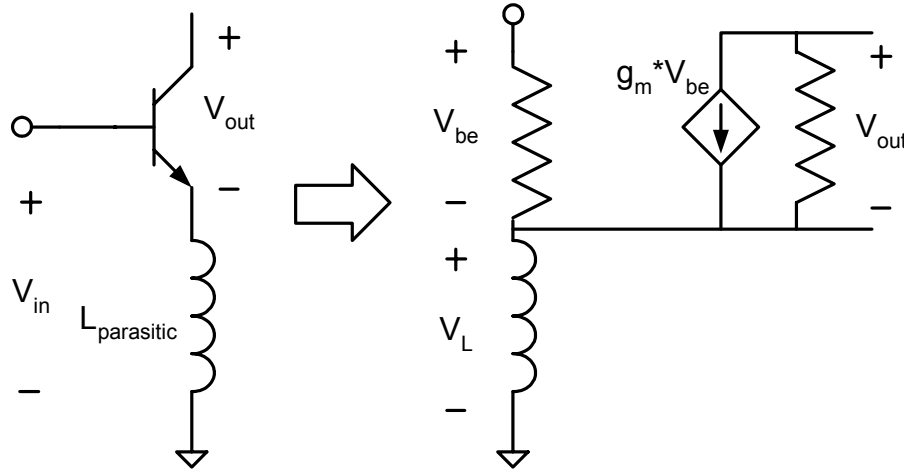
Figure 24. Parasitic inductance in emitter acting as voltage divider

The concern over parasitic inductance in the emitter is the main motivation behind the choice of a differential architecture, despite the added requirements of a power combiner at the output. This topology is also favored in integrated wireless local area network (WLAN) power amplifiers because of the reduced packaging cost and the ability to easily connect the power amplifier on-die with other differential transceiver circuitry [47].

With six levels of metal and their necessary interconnects, via resistance is another possible source of loss in the layout. Large numbers of parallel vias were used to minimize the resistance, as well as limit the amount of current passing through any given via for reliability purposes. With regards to reliability, the HBTs themselves were placed using the 'reliability layout' option which brought connections to the collector and emitter up to the Metal 2 layer (M2) and included large M2 traces for each collector contact. Reliability was further improved by increasing the base Metal 1 layer metallization to 1μm of width for each of the 3 device base contacts.

4.4.2   Large Parallel Transistor Layout

A major challenge in the design of power amplifiers is achieving the best efficiency from the output stage of the device. It is important to minimize the parasitic losses to maximize the power transferred to the output matching network. This becomes difficult because of the large size of the output device necessary to generate half a watt (27dBm) of power or more, depending on the application. To evaluate and discuss the tradeoffs, it is necessary to examine the layout techniques used for large parallel transistors.

In a common-emitter configuration (which is most common for output stages of HBT power amplifiers) the largest amount of current flows from the collector to the emitter, requiring large contacts to prevent excessive resistance. At the same time, the RF input signal is applied to the base of the device. This signal may already be fairly high power, because the gain of the output stage may only be 8-10 dB. As a result, the base resistance should also be kept to a minimum by using short, wide contacts for the base.

The unity gain transition frequency (f_T) of the device will decrease as the size of the emitter is increased, which limits the maximum available gain of the devices. It is therefore important to trade off the current handling of each device to satisfy the gain requirements of the circuit. It is impractical to create a device with large enough emitter area and base contacts to source all the current required by the power amplifier output stage. The solution to this is a combination of multiple device "fingers" (emitter contacts) and paralleling of many such devices.

In the IBM 6HP design kit, the HBTs are available in several sizes and configurations. The technology offers high performance n-p-n transistors with f_T of 45GHz and also high breakdown devices with f_T of 27GHz and BVCEO of 5.4V [48]. The latter of the two devices was chosen for the power amplifier because of this higher

breakdown voltage. The device chosen for this design is shown in Figure 25. This device is a two finger device, indicating that there are two separate emitter contacts, surrounded by three base contacts. The two collector contacts are located on the left and right of the device. For the output stage of this power amplifier, the devices were chosen to have an overall emitter area of $20\mu m^2$ per cell, giving them a maximum rated current handling of 15mA. The layout of this stage is shown in Figure 26. A close-up view of a single row of transistors including their ballasting resistors is given in Figure 27. The devices on the top in the figure are the HBTs, and the devices to the bottom are the emitter ballasting resistors. The base is contacted in Metal1, while the collector contacts come in on Metal3. This is done to increase the distance between any overlapping metal to minimize parasitic base-collector capacitance.
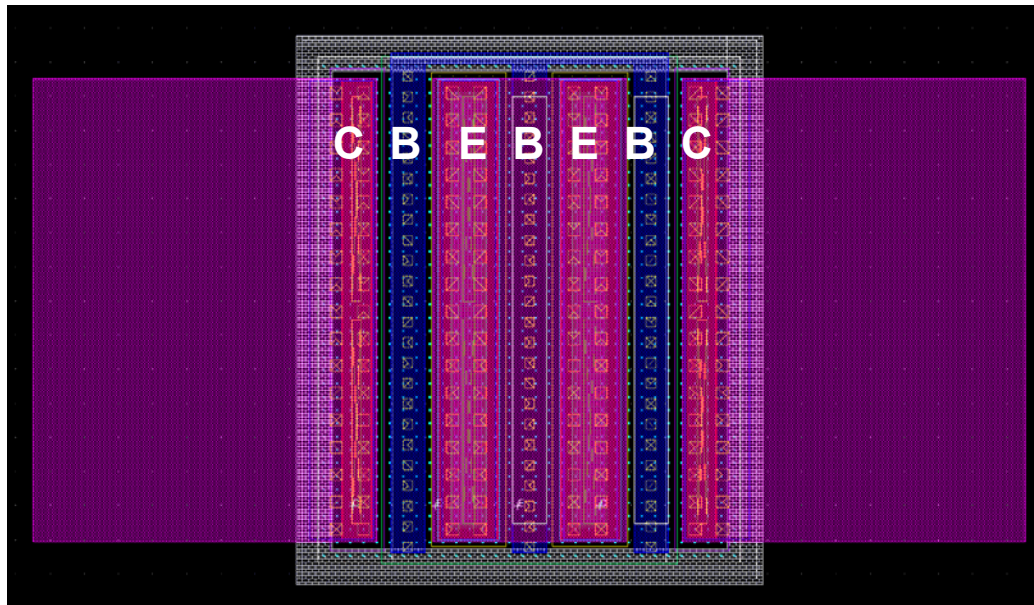
Figure 25. Two finger high breakdown SiGe npn transistor layout

The emitter contacts come out on Metal2 and then drop down to Metal1 to contact the ballasting resistors. The ballasting resistors are a parallel combination for each device to allow for a lower overall resistance. Because of the resistors available

in the process, a smaller resistor could not be made to have the desired value, so the parallel approach was required. This has the additional advantage of providing a wider path for the current flowing from the emitter of each device.
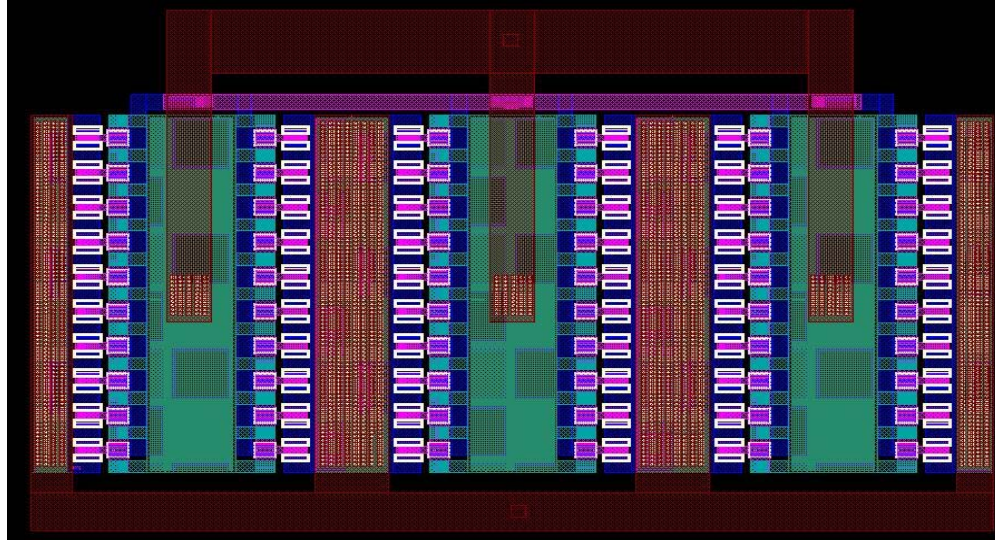
Figure 26. Layout of output stage transistor for one half of differential PA
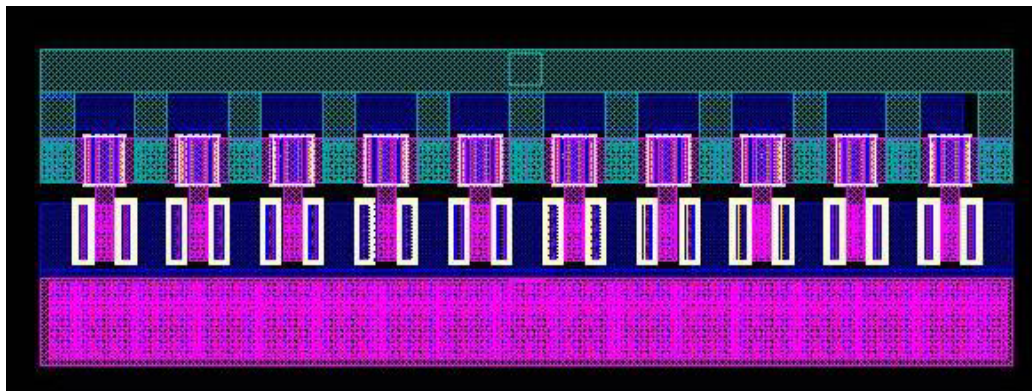
Figure 27. Layout of 10 transistor cell for parallel structure

The natural result of a large metal area in layout is parasitic capacitance. While efforts have been made to minimize this, there still exists a large capacitance between the collector of the device and the substrate. In this layout, the extracted collector-substrate capacitance is 1.5pF. This directly impacts the output matching of

the power amplifier, requiring a re-tuning of the output matching components to account for this extra capacitance. The effective circuit presented to the output matching network is given in Figure 28.
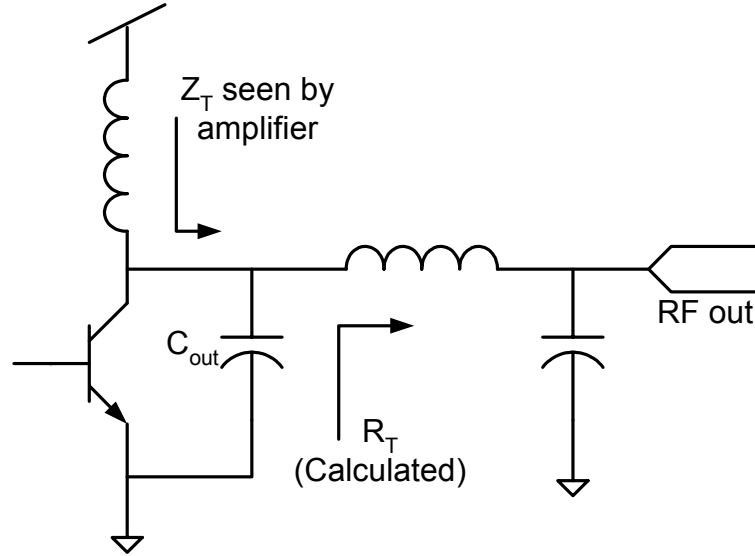
Figure 28. Effect of output capacitance on output matching network

To account for this additional capacitance, the series inductance is increased to present a complex impedance replacing R_T. The additional inductive component of this impedance is cancelled by the output capacitance and in turn presents the desired R_T to the amplifier itself.

4.4.3 Electromigration Concerns

Because of the high power output, many areas of the layout will experience both high current and high electric fields at any given time. This is a concern because of electromigration in the metal itself. Electromigration is the redistribution of metal atoms (in this case aluminum) due to high currents, temperatures, and high electric fields [49]. As a large amount of electrons flow through the metal, they encounter non-idealities in the lattice structure. These can be in the form of lattice vacancies,

impurities, or even grain boundaries between crystals of different orientations. The momentum transfer between the electrons and the atoms of the metal due to these non-idealities causes a diffusion of the metal in areas of high crystal distortion. Electromigration can cause small "cracks" in the metal traces or can cause "voiding" where the metal contacts the semiconductor. Both are of major concern to designers because they pose issues to the reliability and lifetime of a product.

In this design, electromigration was mitigated by using thick traces of metal whenever dealing with high-current lines. The guidelines for metal line width vs. current density are given in the IBM BiCMOS6HP design manual [50]. Following these guidelines allowed for proper line widths to handle the desired currents. To limit problems with voiding, the device current was kept at a fraction of the rated current for the device. Each HBT was limited to 4mA peak current (2mA per finger) to ensure proper operation, even though the device itself was rated at 15mA. As mentioned previously, this reduced the gain available from the devices, but was still acceptable for this application.

4.4.4 Final Power Amplifier Layout

Taking all the concerns listed above into account, the final layout is given in Figure 29. Effort was taken to ensure the design was symmetric to assure the differential performance of the power amplifier. The signals enter from the left and the right sides, and exit from the top of the power amplifier, directly off the collector terminals of the large devices. The biasing and interstage matching is kept along the center of the die to minimize the wiring distance from the common-mode point to the transistors.
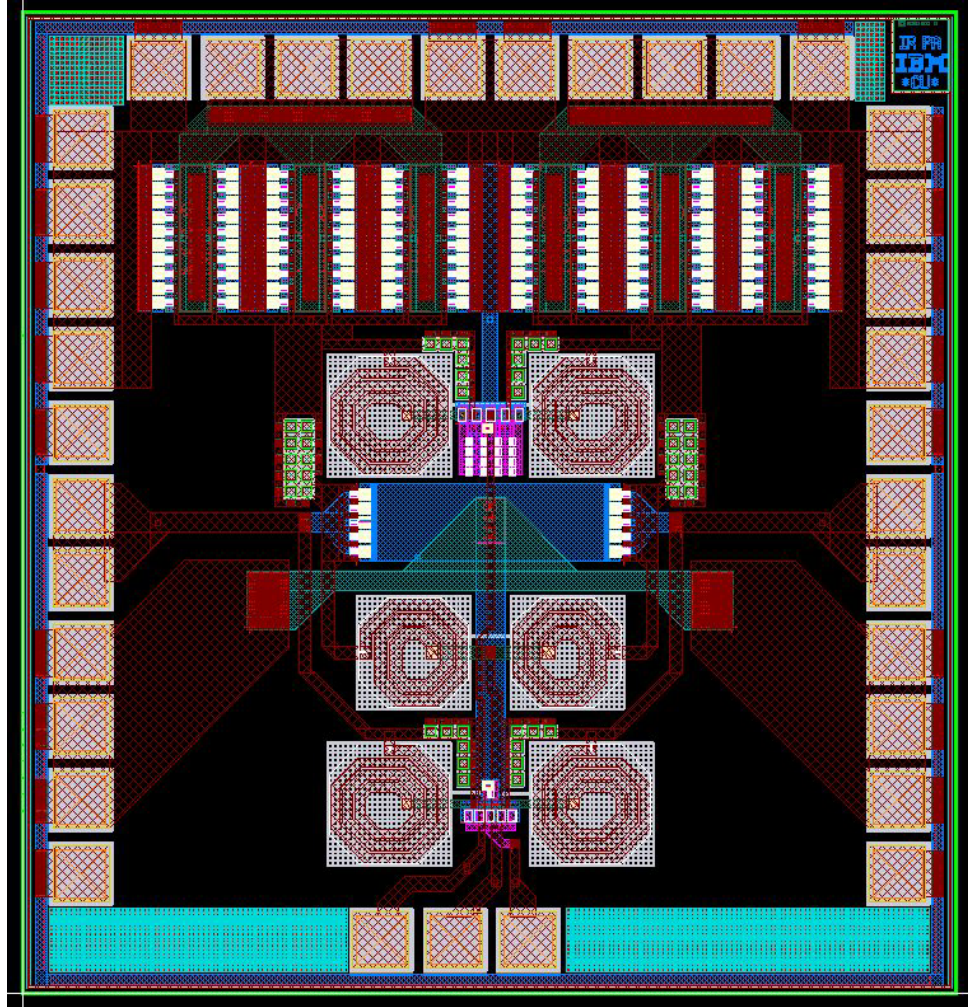
Figure 29. Completed Power Amplifier Layout in SiGe 6HP

The pairs of inductors are, from top to bottom, the output stage base bias inductors, the interstage matching/driver stage collector choke inductors, and the driver stage base bias inductors, respectively. Each pair of base bias inductor also includes the parallel tank capacitors mentioned earlier. The current mirror biasing circuits are located between the inductors, and include decoupling capacitors at the common-mode nodes.

4.5 *Board Design for Testing*

Most commercial power amplifiers for cellular applications are provided as power amplifier modules (PAMs). A module usually consists of a compound semiconductor power amplifier die, a CMOS control/bias circuit die, wire bonds for matching and connectivity, and occasionally low-profile passive components for additional matching elements. This is all housed in packages as small as a 3x3mm 12 pin surface mount package.

While this level of integration is necessary for commercial products, it is beyond the scope of typical research and development work. To test this power amplifier, the more economical (and lab-friendly) approach of chip-on-board was used. In this approach, the power amplifier die is bonded to a printed circuit board (PCB). Wire bonds are made directly between the chip and the PCB. Transmission lines are patterned directly on the board, and any required passive components are soldered to the board, along with the required RF/DC connectors.

4.5.1 *Matching Network Design*

Once the chip-on-board approach was chosen, the previous lumped element input and output matching networks were replaced by combination transmission line/lumped element networks. The parameters for the transmission lines were determined based on the parameters of the PCB used. The board used is a 2-layer FR-4 board with 2 oz. copper plating. The copper is capped by a layer of tin soldermask to allow easy component population. The important parameters for this process are listed in Table 3.

Table 3. PCB transmission line parameters for FR-4 material

Parameter	Value
Dielectric constant (FR-4)	4.1
Loss tangent (FR-4)	0.035
Conductivity (Copper)	5.88×10^7 S/m
Frequency	1.95 GHz

Using the values given in Table 3, the required dimensions were calculated for a 50Ω grounded coplanar waveguide (CPW) transmission line. The structure of the grounded CPW is given in Figure 30. This structure was used because the second layer of the PCB is designed as a ground plane, and ignoring its presence could have affected the impedance analysis. The final dimensions for the transmission line are given in Table 4.
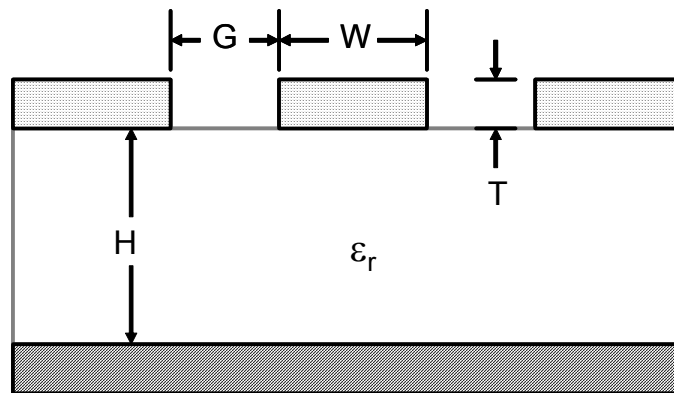
Figure 30. Grounded coplanar waveguide structure

Table 4. 50Ω transmission line parameters

Parameter	*Value*
Width (W)	54 mil
Gap (G)	10 mil
Height (H)	62 mil
Thickness (T)	2 mil
Calculated Impedance	49.9 Ω

Based on these design parameters, a 50Ω grounded coplanar waveguide was substituted for the series inductance in the output matching network. This allows the output inductance to be tuned by adjustment of the placement of the shunt capacitance, providing easy compensation for variations in bondwire inductances. The 50Ω lines also provide direct matches to the RF connectors. Using the transmission lines, the output match has a loss of 0.89dB. The blocking capacitors were realized as 100nF 0805 surface mount capacitors to provide a DC block without impacting the RF signal at 1.92-1.98 GHz.

At the input, 50Ω traces were again used to provide matches to the RF connectors and to allow adjustment of the input matching inductance by varying placement of the shunt capacitance.

4.5.2   PCB Design

The board was designed using the IVEX Winboard PCB tool for Windows. It was fabricated through PCBexpress using their 2-day design fabrication service. A photograph of the completed board is shown in Figure 31.   As mentioned previously, the board is a 2-layer FR-4 with copper traces. The goal of the board design was to

create a test fixture that could be adjusted to optimize the performance of the power amplifier. The CPW transmission lines can be shunted at any point using capacitors to adjust the matching impedance. Large ground planes were desired to minimize the inductance seen at the board level. These ground planes are perforated at the edges to provide good connection between the top and bottom layers. DC biases are brought in on a 6 pin DC header connector with two ground pins for improved connection and the ability to add decoupling capacitors if necessary.
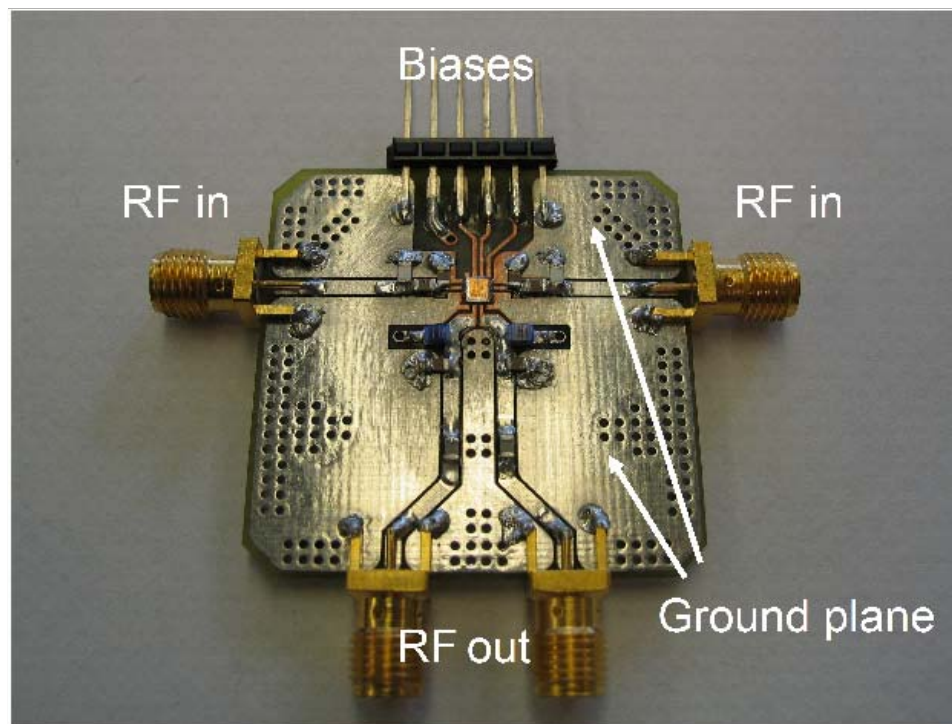
Figure 31. Completed board design with power amplifier and all passive components attached

4.6   Measurement and Testing

The fabricated power amplifier occupies 2mm x 1.8mm of die area. A die photo of the PA is given in Figure 32.
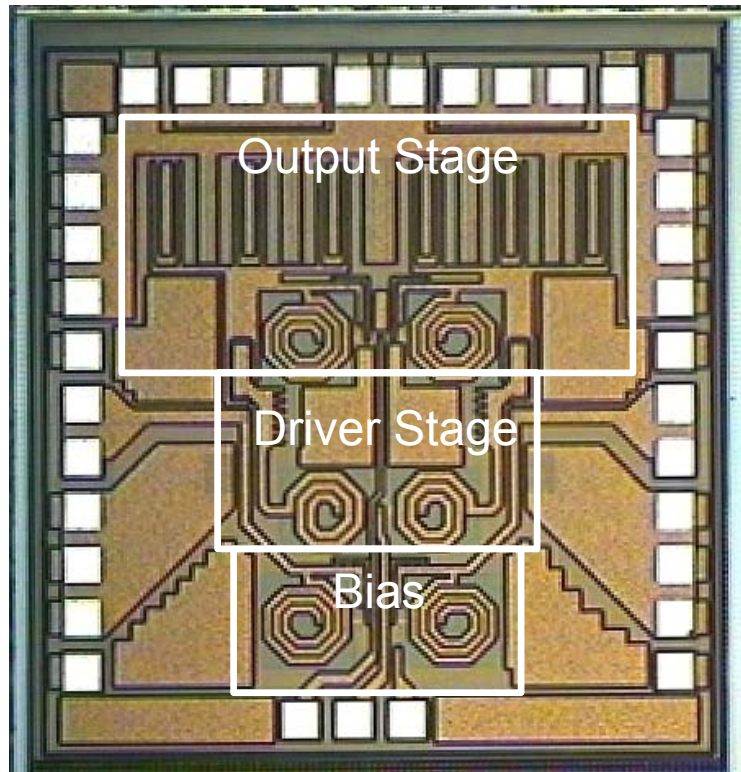
Figure 32. 6HP differential power amplifier die photo

The testing setup for the power amplifier was composed of two Agilent E3631A power supplies, an Agilent E8364B PNA series network analyzer, an Agilent 8564EC spectrum analyzer, and an Agilent 84000 series RFIC tester. The biases were supplied using the power supplies through a breadboard setup that allowed fine control of the base bias current. The network analyzer was used for S-parameter measurements, while the RFIC tester was used for large signal power sweeps and for analysis using WCDMA modulated waveforms. ACPR measurements were taken using the spectrum analyzer. A diagram of the test setups is given in Figure 33.

Power Supplies

Network Analyzer

PA

(a)

Power Supplies

Signal Generator

PA

Spectrum Analyzer

(b)
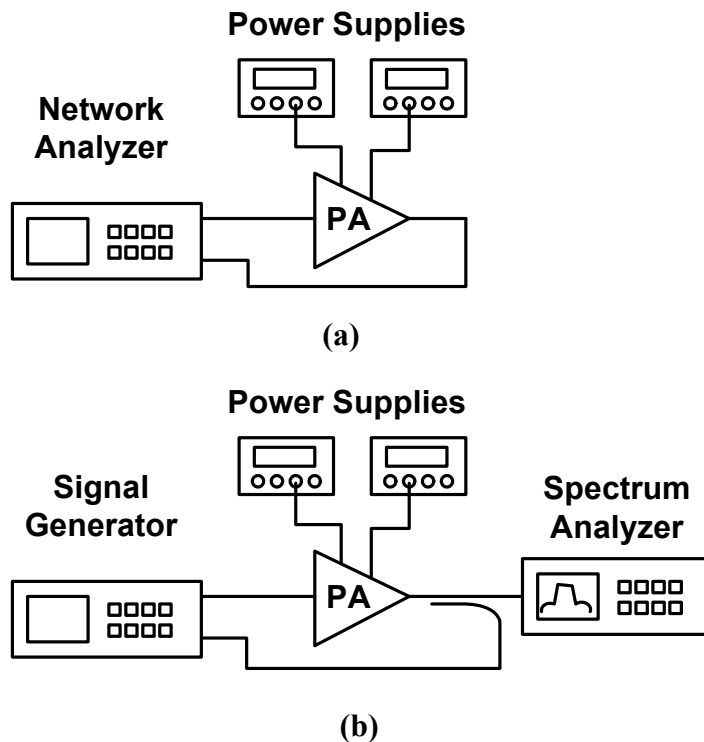
Figure 33. Test setup for (a) S-parameter measurement and (b) output power and ACPR measurement

Initial measurement of the power amplifier indicated a stability problem upon biasing. With only biases applied, the power amplifier had an output signal at 1.67GHz when measured on the spectrum analyzer. While not a high power output, the tone was distinct above the noise floor at -40dBm output power. This prompted a closer analysis of the s-parameters at that frequency. This analysis revealed that the stability factor K was indeed slightly < 1 for the frequencies from 1.65-1.69GHz. Simulation analysis revealed this same instability. This illustrates the need to run stability analysis before tapeout of a design. The most likely scenario is that final simulations were run over the narrow transmit band of the power amplifier, making final component adjustments for peak performance. At the same time, these parameter changes may have induced instability at a different frequency without the designer's knowledge. If such an analysis had been run, this problem could have been avoided.

Because of the integrated and differential nature of the interstage matching networks and bias networks, it was not possible to add the typical RC feedback to the input stage to trade gain for stability. Instead, a shunt capacitance was added at the board level just before the RF input wirebonds. The value of this capacitor was swept to find the appropriate size component to stabilize the amplifier. The final value was 4.0pF, which was available as a surface mount component. This capacitor de-tunes the input match to reduce the gain to a level that prevents oscillation in the amplifier.

After stabilizing the design in simulation, the capacitor was added to the board and the PA was tested again. The biases were applied, but could only be raised to a certain level before the PA would become unstable again. The maximum stable bias values were 20mA collector current for the driver stage and 147mA collector current for the output stage. This places the power amplifier in class AB operation. The effect of the reduced bias is to reduce the 1dB compression point and saturated power of the amplifier.

Measured small-signal s-parameters for the stabilized power amplifier at 1.7GHz are given in Table 5. The value of S_{11} is degraded because of the addition of the capacitor at the input match. The first measurements made on the stabilized PA are shown in Figure 34. It can be seen that the output power saturated at 20dBm, with an output 1dB compression point of 11dBm and a peak PAE of 11%. From these measurements, it was determined that the series inductance of the output matching network was not large enough, indicating that the shunt capacitors had been placed too close to the die. Moving the capacitors further back along the 50Ω trace increased the series inductance, improving the output match.

Table 5. Measured s-parameters for stabilized power amplifier at 1.7GHz

S-parameter	*Value*
S11	-4 dB
S22	-8 dB
S21	26.4dB
S12	-40.1 dB
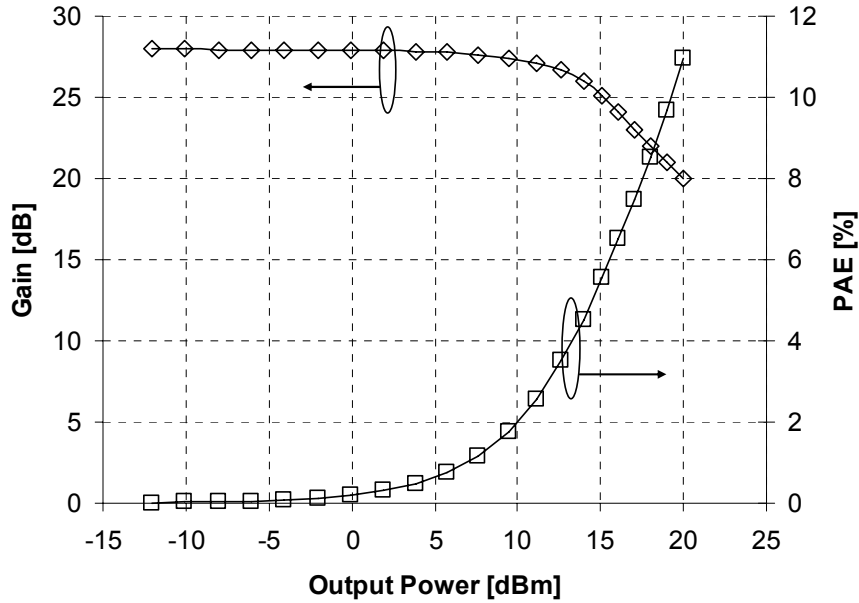
Figure 34. Gain and PAE vs. output power for PA with low compression point

After moving the capacitors, the output power, gain, and PAE improved to near the levels seen in simulation under class AB biasing. These results are given in Figure 35. It can now be seen that the saturated output power is 25.4dBm, while the 1dB compression point has increased to 20.1dBm. The small-signal gain has also improved to 31.2dB.
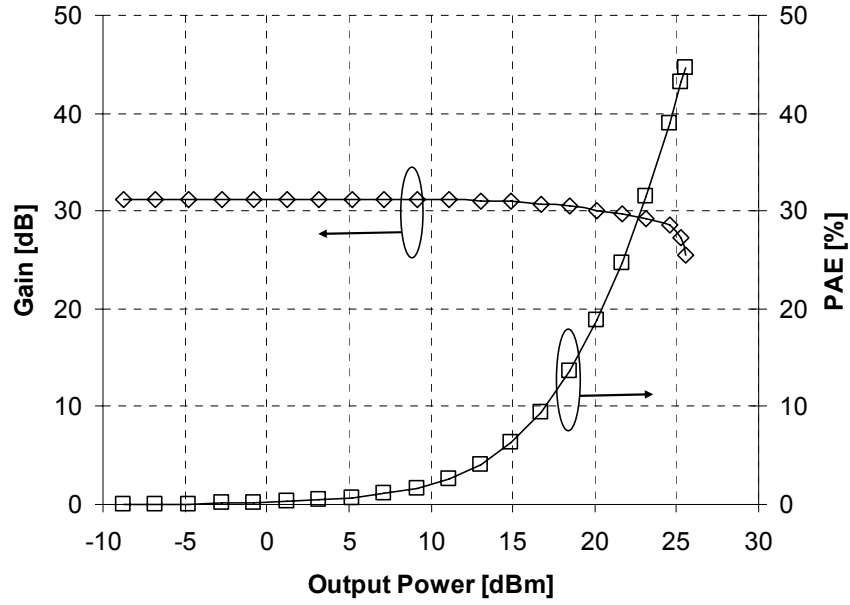
Figure 35. Gain and PAE vs. output power for adjusted output matching network

Rather than delivering 25dBm of linear power and 28dBm of saturated power as originally designed, the PA now provides 21dBm of linear power and 25.4dBm of saturated power. With adjustment of the on-chip matching networks with the new bias levels, the amplifier could be re-tuned to provide the original design goals for P_{1dB} and P_{sat}.

A summary of the power amplifier performance is given in Table 6. Gain for the power amplifier was 31.2dB, which exceeded the target for the design. As mentioned previously, the 1dB compression point was 21dBm, which is lower than the design goal because of the de-tuning required to stabilize the amplifier. Likewise, the saturated output power is also lower than the target by 3.6dBm. Because of the early compression, the power added efficiency of the amplifier was lower than desired, at 22%. However, from Figure 35 it can be seen that PAE increases to almost 50% as the amplifier is driven into compression. With a re-tuned interstage and input

matching network, the goal of >30% PAE at P_{1dB} could be achieved. The ACPR results show that the amplifier still meets the WCDMA requirements for linearity at the 1dB compression point. Based on this, if the amplifier were re-tuned to achieve a higher compression point, the ACPR value should still meet the specification requirement.

Table 6. Measured power amplifier performance

Parameter	*Target*	*Measured*
Gain	30dB	31.2dB
P_{1dB}	25dBm	21dBm
P_{Sat}	28dBm	25.4dBm
PAE @ P_{1dB}	>30%	22%
ACPR @ P_{1dB}, 5MHz offset	-33dBc	-36.2dBc

4.7   Summary

A differential SiGe power amplifier has been designed and tested. The class-AB PA achieves several of the design goals, and meets WCDMA linearity requirements while delivering 21dBm of output power. The circuit was designed and fabricated in IBM's SiGe 6HP technology. Critical layout concerns in power amplifier design were identified, and the steps taken to mitigate their effects on the PA performance were discussed. The testing setup, including the circuit board and matching network design were highlighted. Final measurement results were given for the initial stabilized PA design, as well as a re-tuned design that achieved higher output power. This design is one of the first demonstrations of a differential SiGe

power amplifier, and the first to be fabricated in the BiCMOS 6HP technology. This power amplifier illustrates the capabilities of SiGe to provide performance similar to GaAs while offering the potential for integration with CMOS circuitry.

Chapter 5:   A Variable Supply Voltage Power Amplifier

5.1   Introduction

The implementation of a variable supply voltage power amplifier for WCDMA is one application of SiGe power amplifier technology. The use of the CMOS component of the IBM Bluelogic SiGe 6HP BiCMOS process provides the necessary devices for the design of the required on-chip DC-DC converter. This integration can lead to a power amplifier whose overall average battery current is 50% less than its traditional PA counterpart.

As discussed in chapter 3, a variable supply voltage power amplifier uses a DC-DC converter to reduce the supply voltage when the amplifier is not operating at maximum output power. A block diagram highlighting the technologies used for each component is shown in Figure 36. This design builds on the WCDMA power amplifier core described in chapter 4.
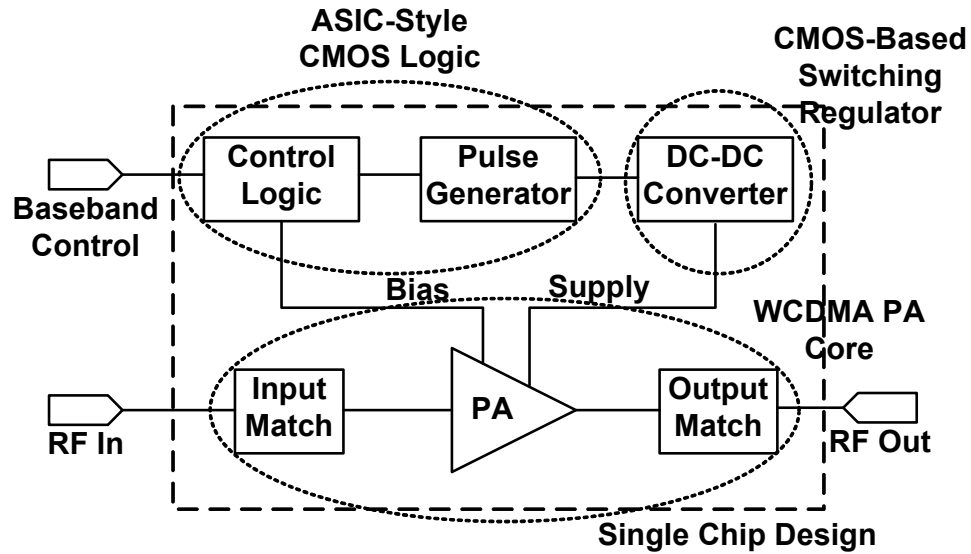
Figure 36. System block diagram of power amplifier with variable supply voltage

The overall design methodology for this DC-DC converter is described, including the choice of frequency, passive components, and device sizes. Several methods of improving the efficiency of DC-DC converters are presented, along with the approaches that were chosen for this converter. A rigorous mathematical analysis of the losses in the converter is followed by description of the final circuit, including simulation results. Traditional analog converter feedback control loops are discussed as well as techniques for the implementation of a digital control loop. The design and layout issues of the combined power amplifier/DC-DC converter chip are explained, and finally, measured results for the complete variable supply voltage power amplifier are presented.

5.2 DC-DC Converter Design

The idea of using a DC-DC converter to vary the supply voltage of a power amplifier is not new, as presented above under efficiency control techniques. However, the idea of integrating the converter onto the same chip as the power

amplifier has not been possible because of the use of multiple processes. In traditional power amplifier design, the PA exists as one die, usually on a GaAs substrate, while any control circuitry is implemented as a separate CMOS chip on a silicon substrate. The closest such an approach could come to integration is at the module level, where the two chips, transmission lines, and often other passives would be integrated inside a larger module package.

With the advent of SiGe BiCMOS technology, it is now possible to leverage the silicon substrate and a mature CMOS processes to integrate the two functions on a single die. The hurdles and challenges of designing power amplifiers in SiGe technology have been described above. The DC-DC converter and control circuit design is explained in this section. This design is based on work submitted to the 2003 SRC SiGe Design Contest and presented in [51].

5.2.1 *Buck Converter Design Overview*

The goal of the DC-DC converter is to transform the current from a fixed voltage to a current at a lower potential. This has been done traditionally with AC currents through the use of wire-wound transformers. In the realm of DC current, linear regulators are often used to supply a lower potential, but the losses can be very high in such an approach, depending on the current levels. To overcome this hindrance, switch-mode converters were developed. Perhaps the simplest implementation is the step-down (or 'buck') converter, which delivers an output voltage lower than the supply voltage. This is also the type of converter implemented in this variable supply voltage power amplifier.

The basic buck converter, shown in Figure 37, consists of a transistor switch, a low-voltage Schottky diode, and an LC filter network at the output [52]. When the switch is open, current flows to the inductor and increases linearly until the switch is

closed. At this point, the load current is sourced by the inductor as it transforms the energy stored in its magnetic field to electric current. The diode is included to prevent the voltage at node V_x from dropping below ground and discharging the capacitor at the output. The filter capacitor serves to reduce the fluctuation in the output voltage seen by the load. By its inclusion, the voltage and current waveforms at the load are 'smoothed' to appear more like a DC value than an AC signal.
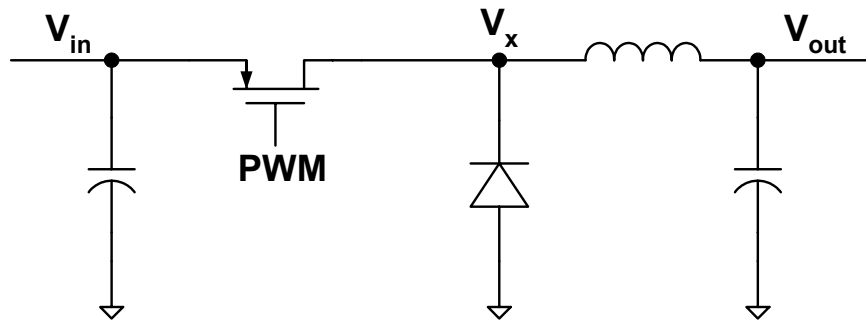
Figure 37. Basic buck converter topology

While this is an acceptable solution for discrete implementations of the buck converter, the diode losses start to become a dominant factor in the circuit, and most CMOS processes do not include such a diode in their standard libraries. As a result, a new topology was created which replaces the diode with another CMOS switch, which effectively clamps the voltage at node V_x when it is turned on. This switch is often referred to as the synchronous rectifier (SR) because it is clocked in opposition to the main switch, as shown in Figure 38 [53].
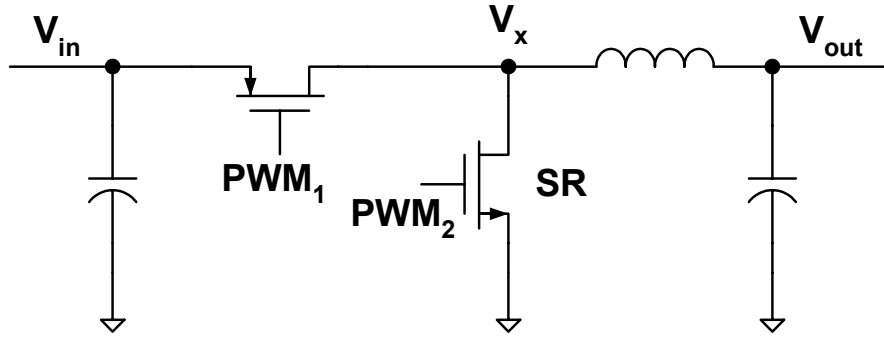
Figure 38. Buck converter with nFET synchronous rectifier

5.2.2 Filter Components

With the basic topology of the converter presented, one of the critical steps in designing to meet required specifications is the choice of filter component size. The two design parameters that limit these choices are the peak-to-peak current swing in the inductor and the ripple in the output voltage. Because of the integrating behavior of the output capacitor, the current waveform across the output inductor will resemble a triangle wave. The peak-to-peak inductor current ripple can determine the mode of operation of the converter, as described below. The general goal for high efficiency is to have the peak-to-peak ripple no greater than twice the minimum load current supplied by the converter. The value of inductance can be calculated as

$$L = \frac{V_{battery}}{4 f_{sw} \Delta I_L} \tag{5.1}$$

where f_{sw} is the switching frequency of the converter, and ΔI_L is the peak-to-peak inductor current.

Once the value of inductor is chosen, the output capacitor value can be determined. The output current ripple is usually specified for the given application to reduce the spurious frequency content of the output voltage. For noise-sensitive applications, this ripple must be sufficiently low to ensure proper operation of the circuit being supplied by the DC-DC converter. The capacitor value can be calculated

based on the worst-case scenario when the converter is operating at its lowest load current and output voltage, giving the smallest duty cycle for the PFET switch. This results in the largest droop on the output capacitor between charging cycles. The output voltage ripple calculation is given in (5.2).

$$V_{ripple} \leq \frac{1}{8 f_{sw}^2 LC} \tag{5.2}$$

This states that the output ripple voltage will be no larger than the value calculated in (5.2), thus the choice of capacitor is made to satisfy the system requirements even when the converter is operating in the worst-case conditions.

5.2.3 Transistor Sizing

Transistor sizing is important in converter design because it determines the loss characteristics of the switches. When balancing switching and conduction loss, a tradeoff must be made in the size of the devices. Larger device width will provide lower series resistance (reduced R_{DSon}) which will reduce conduction loss, but large devices will also have larger gate area resulting in higher gate capacitance and more loss due to switching. It has been shown that the optimum device size balances these two loss mechanisms [54]. When they are balanced, the device will be operating at the peak of the parabolic efficiency curves for the specified output voltage and load current.

An additional concern with large devices is the amount of drive circuitry needed for each gate. The larger the switch device, the larger the devices needed for driving it, and the longer the drive chain. From digital design, it is known that for maximum speed, a chain of inverters should be scaled in size by the ratio *e*. It is possible to increase this number if the goal is minimum rise/fall time, rather than overall speed (i.e. the frequency of the square wave is not the limiting factor). Based

on the analysis in [54], a ratio of 5 was chosen for the IBM BiCMOS 6HP technology. Even with a higher ratio, the increase in inverter size and number will result in more loss in the converter because of both the charge needed to drive the next inverter in the chain, and the overlap of the current and voltage waveforms during the finite transition time from high to low in each inverter. This additional gate drive circuitry must be included in circuit analysis because the loss in these circuits can be as high as the gate drive loss of the switch itself.

5.2.4   *Frequency Selection*

For applications in handheld wireless devices, the frequency of operation of the converter is a critical issue for consideration. A high switching frequency would result in increased switching losses in the converter, but would also create harmonics that would fall well outside of the bandwidth of the baseband signal. The factors affecting the choice of the switching frequency are:

- required size of passive components (inversely proportional to frequency)
- unwanted in-band interference that may result from switching harmonics
- switching losses (proportional to frequency)

Thus, there is a trade-off required in selecting the converter switching frequency: higher frequencies result in smaller passives, which improve integration density, but they also result in higher switching losses.

The switching frequency should also be selected such that the harmonics do not fall within the WCDMA transmit band (1920-1980 MHz) [44] and such that the output voltage ripple mixing with the transmitted signal does not produce any products that may also fall within the transmit band. This requires a switching frequency greater than 60MHz. It can be shown that for a square wave signal of any duty cycle only odd harmonic components exist. As such, analysis was performed to find the size and

location of frequency windows greater than 60MHz which do not have odd harmonics that will fall in the transmit band. The results of this analysis are given in Figure 39.
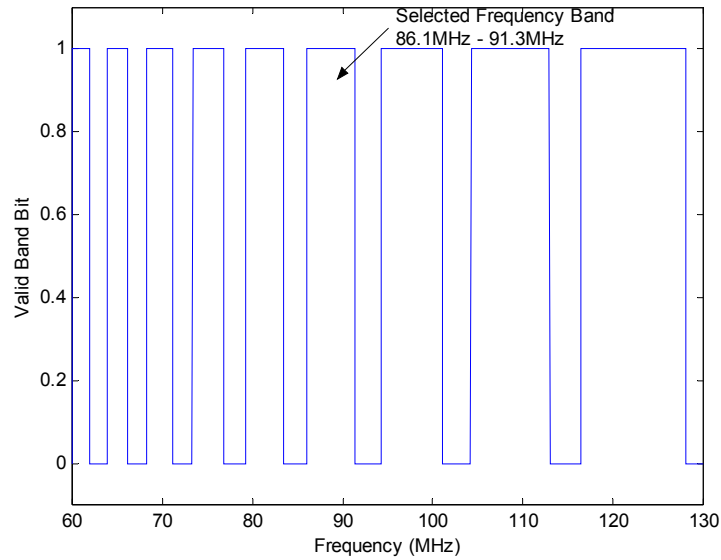
Figure 39. Frequency selection analysis results for buck converter in WCDMA applications

In Figure 39, a "1" represents a valid frequency choice, while a "0" indicates a frequency that will contain harmonics or mixing products in the transmit band of the power amplifier. Based on this analysis, 89 MHz was chosen as the frequency of operation. This frequency band of 5.2MHz allows for potential inaccuracy in the oscillator due to process or temperature variations.

Another concern is the low-load condition of operation in the converter. At low load current, the switching losses dominate, reducing the efficiency. Some designs alleviate this concern by using a pulse-skipping technique, where at low load conditions the switching frequency of the converter is decreased to improve the efficiency [55]. This is not possible in this design because of the stringent frequency requirements of the wireless system that the converter is interfacing with.

A switching frequency of 89MHz is considered very high for a DC-DC converter. Because switching losses are proportional to frequency, high frequency operation is often avoided to achieve the highest efficiency. But with continuous scaling of CMOS devices, it is increasingly possible to use shorter gate length transistors to achieve more performance with less gate capacitance. As the technology scales, the advantages for DC-DC converter design are twofold: the shorter gate length decreases the on-resistance of the device, and the smaller gate dimensions reduce the switching losses due to charging the gate capacitance. With the 0.25μm CMOS technology used for this design, a higher switching frequency can be used while still achieving adequate converter efficiency.

5.2.5   CCM/DCM Operation

Traditional buck converters are usually operated in the continuous conduction mode (CCM) to achieve the highest operational efficiency and simplify the converter design. This mode of operation occurs when the synchronous rectifier is on for the entire time the upper switch is off. An illustration of CCM inductor current is shown in Figure 40 for both high load current and low load current.
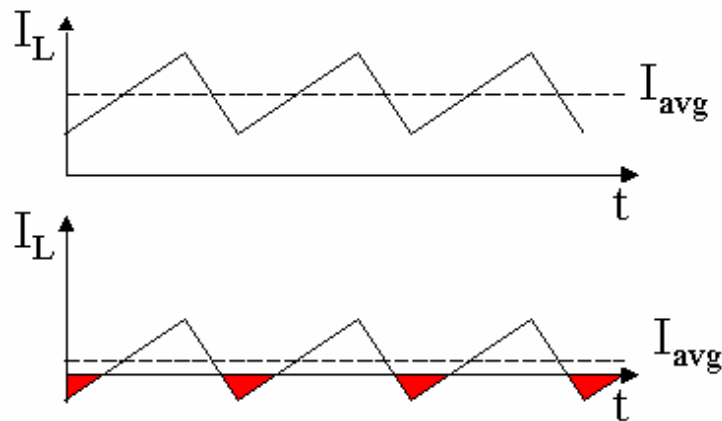
Figure 40. Continuous conduction mode inductor current for high (top) and low (bottom) average load current

The shaded area of the inductor current waveform represents negative inductor current. At low load current, the peak-to-peak inductor current will be larger than the average current, resulting in a period of time where the inductor current is negative. This is charge being pulled off the output capacitor and shunted to ground through the synchronous rectifier. This operation reduces the efficiency of the converter because this output capacitor charge has to be replenished before the appropriate output voltage can be restored. This also causes increased ripple at the output of the converter because of the reduction of charge. This type of operation is desirable from a component standpoint, however, because it allows the use of a smaller inductor. Based on (5.1), a smaller inductor will produce a larger peak-to-peak current swing, leading to negative inductor current at low average load current.

To counteract this loss of charge, the synchronous rectifier can be turned off, eliminating the conduction path to ground. This is known as discontinuous conduction mode (DCM). The inductor current in this mode of operation is shown in Figure 41.
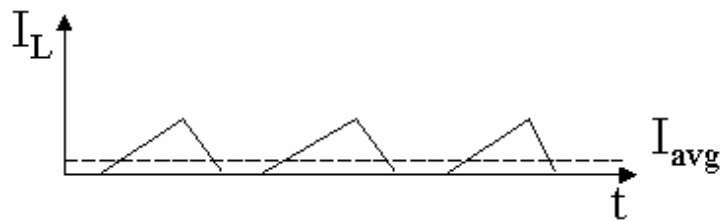
Figure 41. Discontinuous conduction mode inductor current waveform

When the synchronous rectifier is turned off, the current and voltage in the output filter resonate at the fundamental frequency of the filter. This does produce some loss due to the finite Q of the filter, but provides significant efficiency improvement over the continuous conduction mode of operation for low average load current [56], allowing the use of a smaller inductor.

5.2.6   W-Switching

Another technique the can be used to improve the efficiency of a DC-DC converter is known was W-switching, or active device sizing. This technique was first proposed in [57] to provide improvements in efficiency at low load current. In this design, the concept of W-switching has been extended to maintain the balance between switching and conduction losses at each output voltage level, as mentioned above. Because the large transistor gate area contributes a significant amount of capacitance, the switching losses begin to dominate the efficiency of the device in "low-load" conditions, which occur when the converter is operating near its minimum load current rating.

To combat the increased switching losses at low load current, portions of the large parallel devices are disabled, effectively removing their gate capacitance from the switching loss calculation. This can be seen in Figure 42, which depicts a single "W-block" with an enable switch in the drive circuitry. Several of these W-blocks are then connected in parallel to provide the overall switches and drive circuitry as shown in Figure 43.
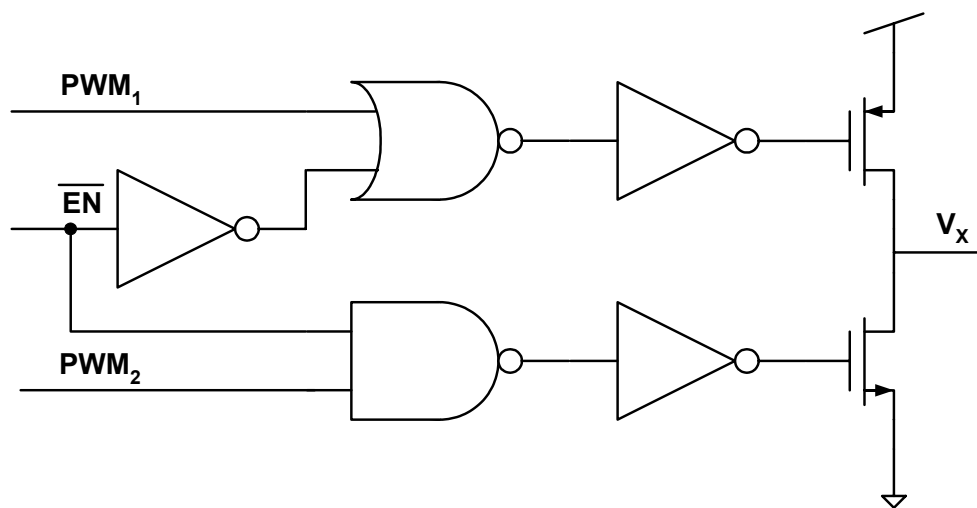
Figure 42. W-block used to vary effective gate width of switch transistors
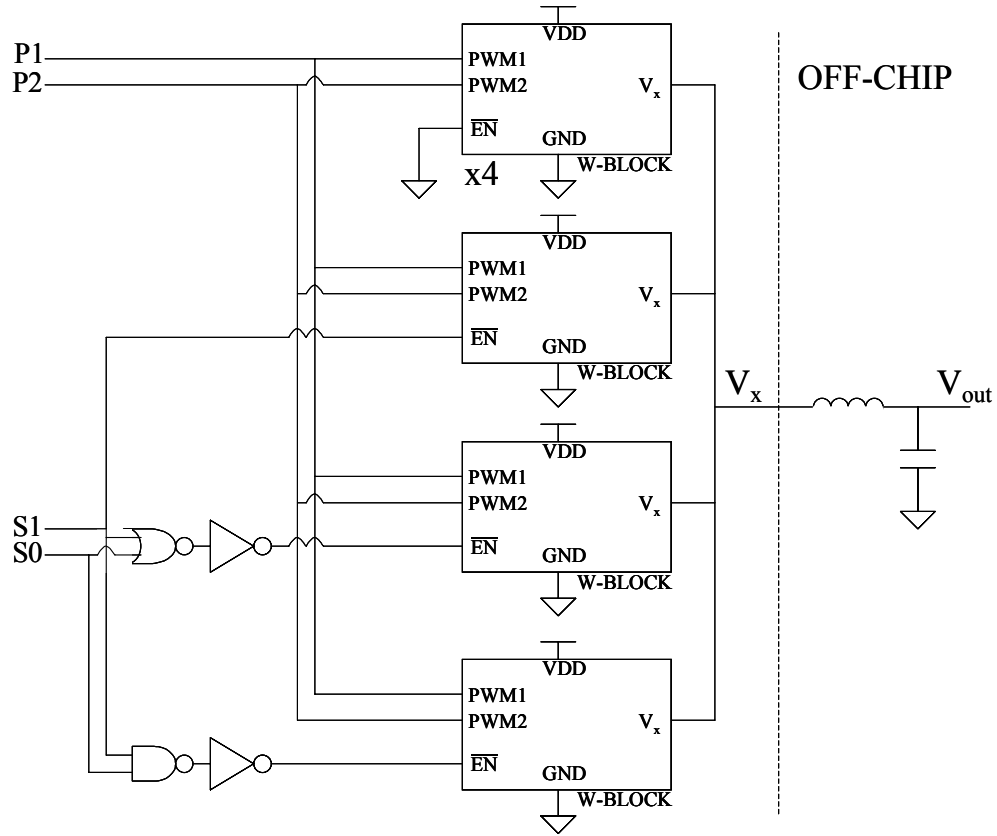
Figure 43. Parallel connection of W-blocks to create the PFET and NFET switches of a buck converter

The drawback of such an approach is that the conduction losses are increased as device width is decreased, but because of the low load current, conduction losses are very low to begin with, so increasing them only helps to regain the balance between switching and conduction losses to ensure operation at the peak efficiency for the given load conditions.

5.2.7 *Comprehensive Loss Analysis*

The losses in a DC-DC converter are what determine the efficiency at different load currents and output voltages. It has already been mentioned that to achieve the peak efficiency, the switching losses must be equal to the conduction losses. The

various loss mechanisms are described here, broken down into the two categories of switching and conduction loss.

5.2.7.1 Conduction Losses

Any losses due to (or proportional to) the average current flowing through the converter are considered to be conduction losses. One of the most conspicuous sources is due to the finite resistance presented by the FET switches when they are in the "on" position. The drain-source resistance of a FET is governed by its geometry: a longer gate will have higher resistance, while a wider gate will lower the resistance. If the resistance per unit area, R_{DS0} is known for a technology, the final value of R_{DSon} can be calculated as follows:

$$R_{DSon} = \frac{L_{gate} R_{DS0}}{W_{gate}}$$
(5.3)

Once the on-resistance is known for each device, the power loss due to this resistance can be calculated as a function of load current. The overall power losses, $P_{C,PFET}$ and $P_{C,NFET}$ are given below.

$$P_{C,PFET} = i_{load}^2 R_{DSon,PFET} D$$
(5.4)

$$P_{C,NFET} = i_{load}^2 R_{DSon,NFET} \left(1 - D - \frac{t_d}{T}\right)$$
(5.5)

where

$$D = \frac{V_{out}}{V_{battery}}$$
(5.6)

$$T = \frac{1}{freq}$$
(5.7)

and

$$t_d = 300\,ps$$

The time t_d is the dead time between the PFET turn-off and the NFET turn-on. This delay is introduced to prevent a period where both devices are on which results in "crowbar" current when there is a direct path between the supply and ground. D is the ratio between the output voltage of the converter and the battery voltage. As long as the converter is in CCM operation, D is also the duty cycle of the PFET PWM signal.

Another source of conduction loss is due to the parasitic resistance of the inductor. This is composed of both the DC resistance of the windings, as well as the frequency-dependent resistance that determines the Q factor of the inductor. This loss is calculated in similar fashion to the FET conduction loss, and is given by

$$P_{C,inductor} = i_{load}^2 R_{inductor} \tag{5.8}$$

The final source of conduction loss in this analysis is due to the body diode conduction of the NFET. Because of the inclusion of a "dead time" between the PFET turn-off and the NFET turn-on, for a short time the load current will be supplied by the inductor and will flow through the body diode of the NFET. As seen in Figure 44, the drain-bulk junction of an NFET forms a p-n junction diode.
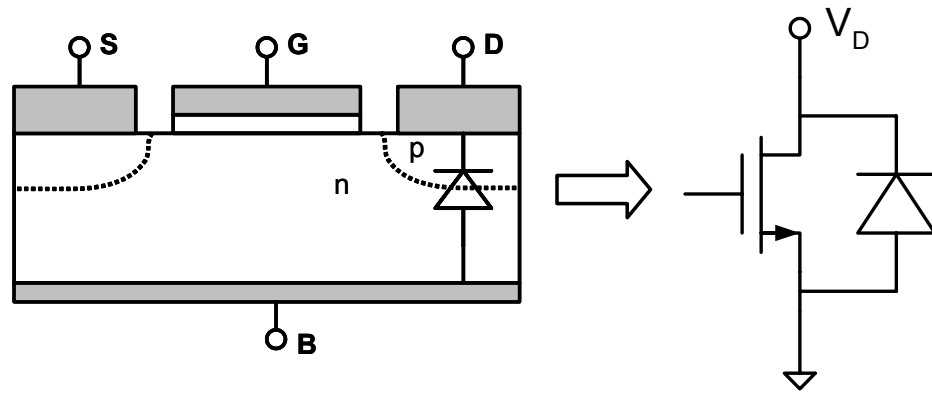
Figure 44. Body diode from drain to bulk in NFET and its equivalent circuit representation

This diode is usually reverse biased due to the voltage on the drain. However, once the PFET turns off, to maintain the flow of current to the load the inductor will force the voltage at node V_x (in Figure 38) to a negative value to establish the appropriate potential across the inductor, allowing it to maintain the current flow. During this brief period of time, the body diode will become forward-biased and will conduct current. The losses will be proportional to the dead time t_d, the load current, and the voltage across the diode.

$$P_{C,diode} = 2\left(\frac{t_d}{T}\right)i_{load}V_{diode} \qquad (5.9)$$

5.2.7.2 Switching Losses

The FET switch devices in a DC-DC converter usually have large gate periphery to accommodate the low on-resistance required for high efficiency operation. This presents a design challenge because this large gate has a capacitance associated with it that must be charged and discharged on each switching cycle to turn the switch on and off. Additionally, during the turn-on and turn-off of the device, the finite rise and fall times $t_{r,f}$ cause more losses due to the period of time when the device is partially on and partially off, providing a path through the device. These loss mechanisms comprise the switching losses in a DC-DC converter.

The gate capacitance will also be proportional of the length and width of the device, similar to the on-resistance. Knowing the capacitance per unit area, C_{g0}, the total gate capacitance for each device can be calculated as

$$C_g = (WL)C_{g0} \qquad (5.10)$$

The losses due to charging and discharging the FET gate can then be calculated similarly to a digital circuit as

$$P_{SW,PFET} = C_{g,PFET} V_{battery}^2 f \tag{5.11}$$

and

$$P_{SW,NFET} = C_{g,NFET} V_{battery}^2 f \tag{5.12}$$

The use of $V_{battery}$ in (5.11) and (5.12) implies that the circuit driving the gate of the FETs is also connected to the battery potential. If this drive circuitry is at a different supply voltage, that value should be used in place of $V_{battery}$.

The final component of switching losses comes from the finite rise and fall time of the transistors. As the switch transistors move from the off-state to the on-state (and on-to-off as well) there is a period of time when the voltage and current waveforms overlap, resulting in power loss in the device. Assuming the rise time and fall times are the same through design, the loss can be expressed as

$$P_{SW,rise,fall} \cong i_{load} V_{battery} \left(\frac{t_{r,f}}{T} \right) \tag{5.13}$$

where

$$t_r = t_f = t_{r,f} = 500\,ps \tag{5.14}$$

These design equations can be combined to provide a theoretical analysis of the efficiency of a DC-DC converter. The total power loss is the sum of all the individual losses.

$$P_{loss,total} = P_{C,PFET} + P_{C,NFET} + P_{C,inductor} + P_{C,diode} + P_{SW,PFET} + P_{SW,NFET} + P_{SW,rise,fall} \tag{5.15}$$

The efficiency of the converter is given as

$$\eta_{converter} = \frac{i_{load}V_{out}}{\left(i_{battery}V_{battery} + P_{loss,total}\right)} \tag{5.16}$$

It can be seen from (5.16) that the efficiency is a function of the load current, output voltage, battery current, battery voltage, and overall power loss, calculated above. This can be simplified to give dependence on only two variables, i_{load} and V_{out}. By substituting (5.6) into (5.16), efficiency can be expressed as

$$\eta_{converter} = \frac{i_{load}V_{out}}{\left(i_{battery} \, V_{out}/D + P_{loss,total}\right)} \tag{5.17}$$

Additionally, the battery current can be approximated as

$$i_{battery} = i_{load}D \tag{5.18}$$

for continuous conduction mode operation. Substituting (5.18) into (5.17) gives

$$\eta_{converter} = \frac{i_{load}V_{out}}{\left(i_{load}V_{out} + P_{loss,total}\right)} \tag{5.19}$$

which simplifies to

$$\eta_{converter} = \frac{1}{1 + P_{loss,total}} \tag{5.20}$$

Because $P_{loss,total}$ is a function of load current and output voltage, the efficiency can be plotted as a contour over both variables. This is shown below in Figure 45 for a converter operating at 100MHz with an output voltage range of 1-3.4V and load current range from 30-500mA.
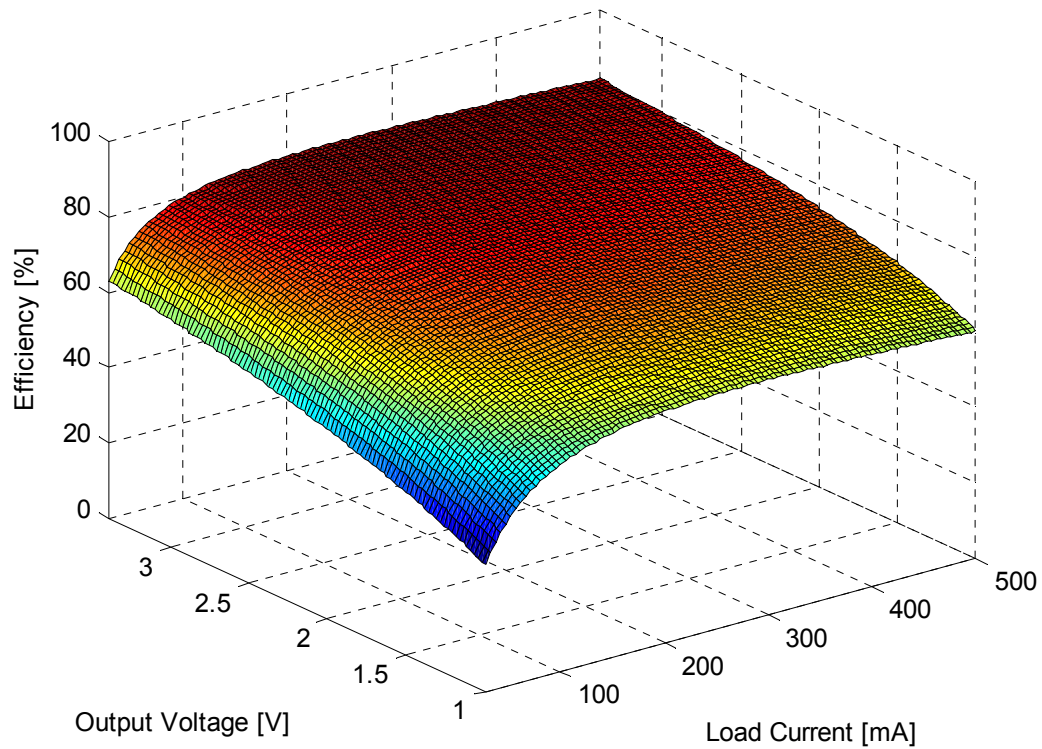
Figure 45. Efficiency vs. load current and output voltage for a 90MHz converter operating from 1-3.4V and from 30-500mA

This contour plot as given in Figure 45 can be used in the design of variable supply voltage systems to provide the designer with a good estimate of the converter efficiency that is expected at any given operating point of the devices being powered by the converter. By having this information available, system performance analysis can be done to determine the tradeoffs necessary in the converter design to achieve the desired goals.

5.2.8 Circuit Design

Following the design approach outlined above, the DC-DC converter was designed to interface with a differential WCDMA power amplifier to realize a variable supply voltage power amplifier. With a low-load current of 150mA and a maximum

current of almost 500mA, the power amplifier had a large load variation that must be handled by the converter. Additionally, the converter must be able to operate from 1V to 2.7V. Based on these requirements, the final component values and device sizes are given in Table 7.

Table 7. DC-DC Converter Parameters

Parameter	*Value*
Switching frequency	89MHz
Filter inductor	10.1nH
Filter capacitor	100nF
PFET size (W/L)	7mm / 0.35μm, with W variable in 1mm increments down to 4mm.
Efficiency at 1V, 150mA	63%
Efficiency at 2.7V, 450mA	85%

As mentioned above, the converter uses active device sizing to maintain the balance between switching and conduction loss as the load current and output voltage are decreased. This is accomplished using the W-blocks shown in Figure 42. The enable function is controlled by a block of selection logic that allows for two select bits, S0 and S1, to realize the four device sizes in a binary fashion. The logic table for the device size corresponding to the select bits and output voltage is given in Table 8.

Table 8. Device width versus select bits

PFET / NFET Width	S1	S0	V_{out}
7.0mm / 3.5mm	0	0	2.7V
6.0mm / 3.0mm	0	1	2.2V
5.0mm / 2.5mm	1	0	1.7V
4.0mm / 2.0mm	1	1	1.2V

By varying the width with these select bits, the system could be coupled to a baseband controller or processor (or digital control loop) that would be able to adjust the converter to improve performance as needed by the system.

5.2.9   Simulation Results

The pulse width modulator signals are specified by their duty cycles P1 and P2, as indicated in Figure 46. The overall period of the waveform is maintained at 11.3ns, or 89MHz. PWM1 drives the PFET switch, while PWM2 drives the synchronous rectifier. The value of D is 500ns, and represents fixed delay to prevent the PFET and NFET from being on at the same time and providing a direct path from supply to ground. This 500ns delay is chosen based on the worst rise/fall time of the inverter drive chain.
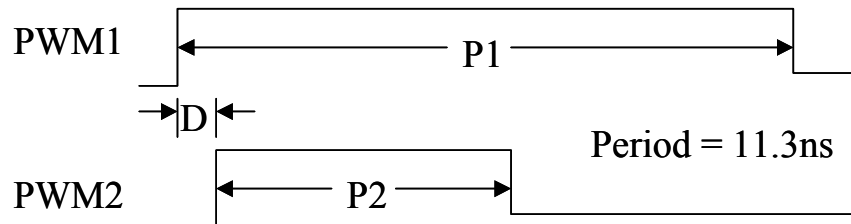
Figure 46. Pulse width modulator waveform characteristics

Using these PWM signals, the converter can be simulated over the operating range of output voltages. Figure 47 shows the simulated waveforms for the switching node V_x, the inductor current I_L, the output voltage, and the two pulse width modulator signals, PWM1 and PWM2. These waveforms are for an output voltage of 1.8V and a load current of 100mA. Similar waveforms were used to evaluate the performance of the converter over the entire output voltage and load current range.
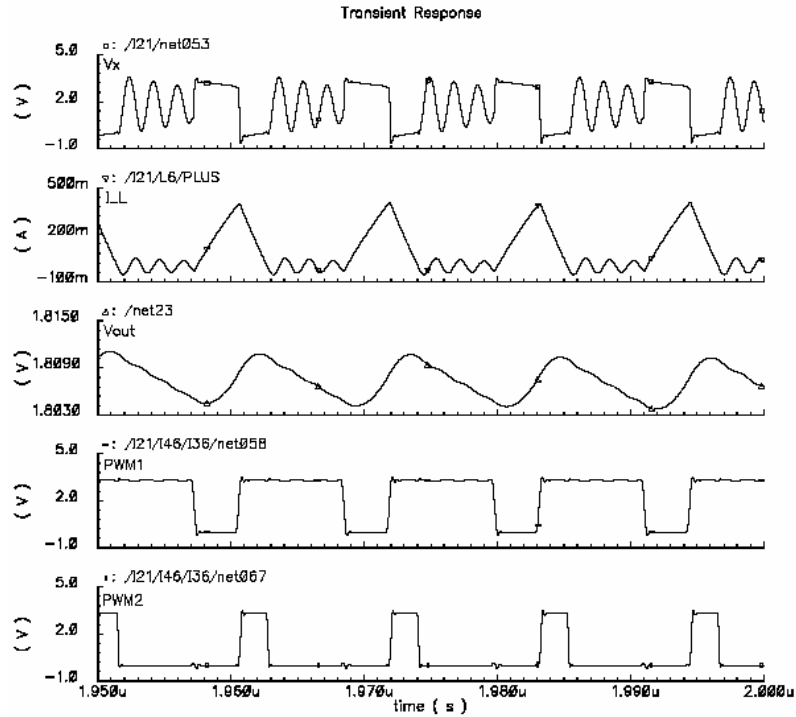
Figure 47. Simulated converter waveforms for output voltage of 1.8V and 100mA of load current

Based on analysis of the converter waveforms, the converter efficiency is given in Table 9. These results are compiled for the operating characteristics of the WCDMA power amplifier, with the device sizes chosen at the appropriate output condition to maintain the balance between conduction and switching loss. The battery voltage is 3V, with the 2.7V output voltage case representing the pass-through

condition where the PFET is on for the entire period. In this case the loss is due only to the value of R_{DSon} for the PFET transistor.

Table 9. Simulated DC-DC converter performance

Output voltage	PFET width	Load current	Battery current	Efficiency
2.7V	7mm	270mA	267mA	91%
2.2V	6mm	220mA	197mA	82%
1.7V	5mm	170mA	130mA	74%
1.2V	4mm	150mA	92mA	65%

The use of the active device sizing has a considerable impact at low voltage and low load current. The efficiency at 1.2V degrades from 65% to 47% if the full 7mm device is used because of the increased switching losses. These results include the converter and the associated switch drive chain inverters, as well as the control logic used to select the device width.

5.2.10 Layout

The DC-DC converter design has several unique layout issues associated with it that have to be addressed to ensure proper operation. Similar to the power amplifier layout, the DC-DC converter will also need to handle large amounts of current, which indicates the need for large metal traces. In this case, however, the increased capacitance associated with such traces is not detrimental to the performance, and can actually serve to reduce the output ripple of the converter.

The active device sizing of the converter, mentioned above, requires separate blocks that can be enabled or disabled depending on the operation of the converter. This is achieved through the use of parallel blocks that contain their own chain of

inverters to drive the final gates. This distributed drive approach also helps to reduce RC delay between the different blocks. This also helps to synchronize the turn-on/turn-off of the power transistors as they all see similar RC time-constants, something that would not be the case for a large transistor with a single driver circuit.

The layout of a single block is shown in Figure 48, with the parallel combination of all seven blocks depicted in Figure 49.
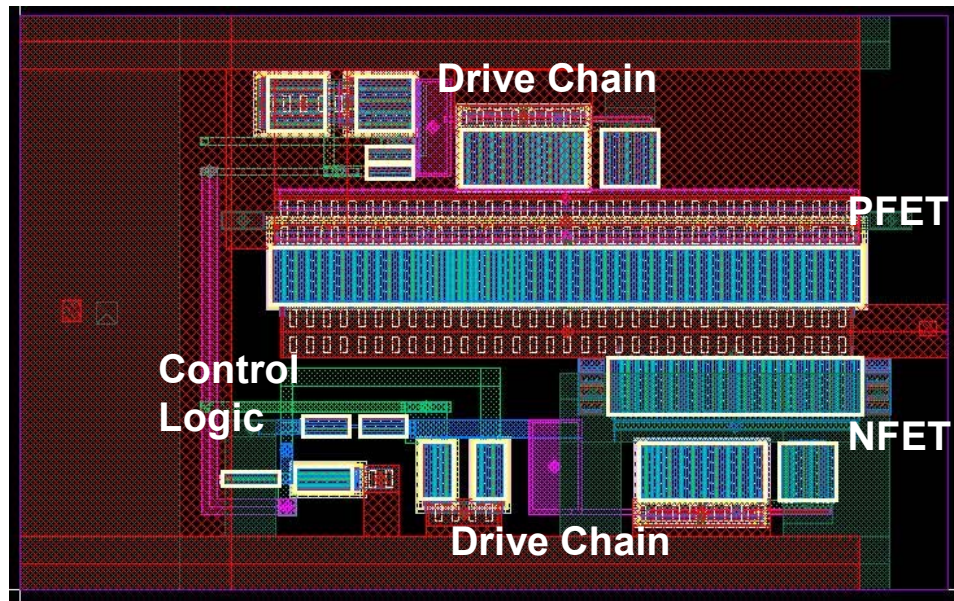
Figure 48. Layout of single distributed drive "W-block" of converter
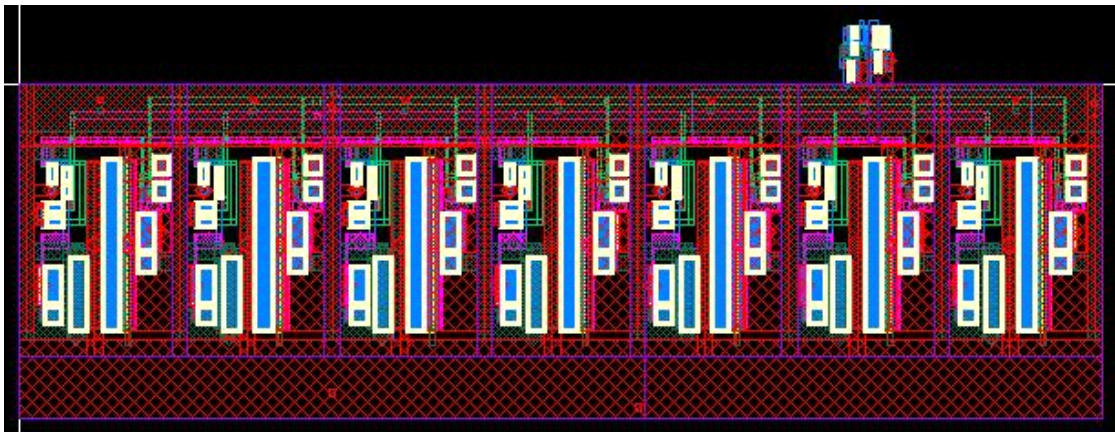
Figure 49. Layout of completed converter

In Figure 49, the supply voltage and ground run along the top of the layout, directly over top of each other. This is by design to increase the decoupling capacitance between the supply and ground. The output node that connects to the series inductor is at the bottom of the figure. The small block in the upper right is an additional control logic block that controls the logic in the separate W-blocks.

To provide proper well-biasing and isolation, all PFET n-wells are contacted along the entire length of the well and connected to V_{DD}. The wells are then surrounded by an oxide deep-trench moat to improve substrate isolation. Numerous substrate contacts attached to the ground bus are also placed alongside the NFETs to sweep up substrate noise current and provide a solid body reference for the devices.

5.3   *Control Circuitry Design*

For operation under varied load and supply conditions, it is important for a DC-DC converter to employ a feedback control loop. This loop ensures that the converter will continue to operate as desired and in an efficient manner despite changes in load current and supply voltage. It is also important that the loop bandwidth be high enough to allow the system to react to required output voltage changes in a timely manner and in accordance with the power update frequency of the target application. A diagram of a basic control loop for a DC-DC converter is given in Figure 50.
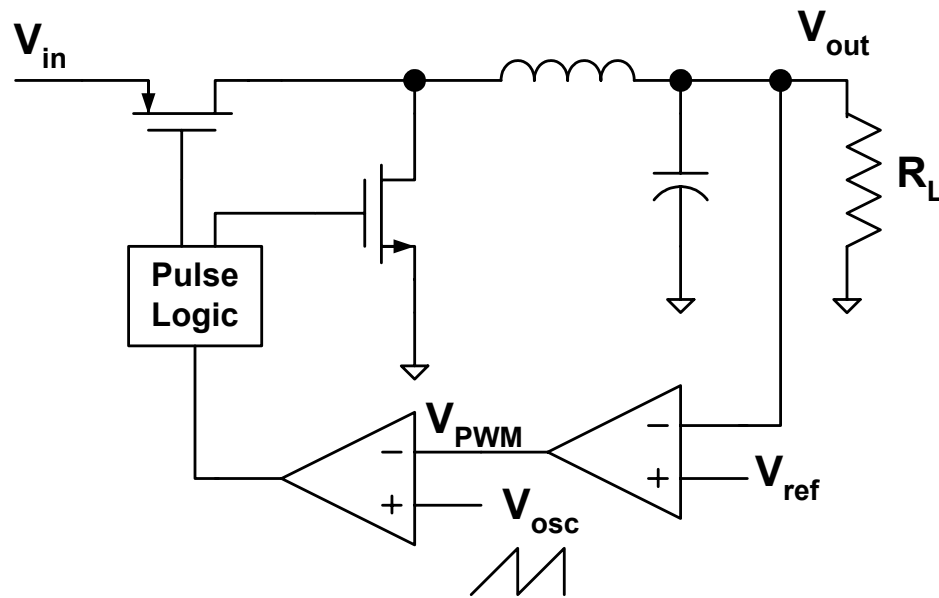
Figure 50. Basic feedback control loop for a buck DC-DC converter

This general control loop senses the output voltage and varies the width of the pulses applied to the switches to regulate the output voltage to a set reference. The bandwidth of the control loop is important to ensure rapid response to changes in the supply voltage or the load current. To determine the characteristics of the loop, a transfer function of the DC-DC converter must first be developed.

5.3.1 Converter Transfer Function

The standard buck DC-DC converter described above can be modeled as a system composed of several transfer functions. The various blocks that compose the converter transfer function are illustrated in Figure 51.
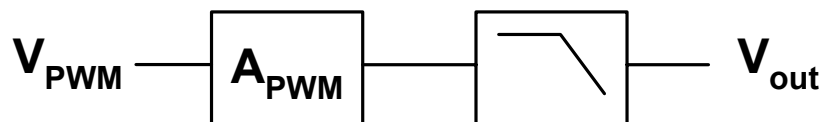
Figure 51. Open-loop transfer function of buck DC-DC converter

The first block represents the "gain" of the pulse width modulator and power switch. This is the change in the output voltage due to a corresponding change in the PWM control voltage.

$$A_{PWM} = \frac{V_{out}}{V_{PWM}} \tag{5.21}$$

The LC filter has the expected transfer function exhibiting an underdamped complex-pole pair at the resonant frequency. The effective series resistance (ESR) of the capacitor must also be accounted for, and produces a zero above the resonant frequency.

$$\omega_{filter} = \frac{1}{\sqrt{LC}} \tag{5.22}$$

$$\omega_{ESR} = \frac{1}{R_{ESR}C} \tag{5.23}$$

For this converter, L = 10.1nH and C = 100nF. This gives a filter frequency of 5MHz. Assuming an ESR of 0.02Ω, the ESR zero frequency is at 79.6MHz. This zero is far enough away from the filter frequency to be ignored for most of the following analysis. If a lower Q capacitor is used, this zero will need to be considered in the loop compensation analysis. Based on these values, the bode plot for the open-loop transfer function is given in Figure 52.
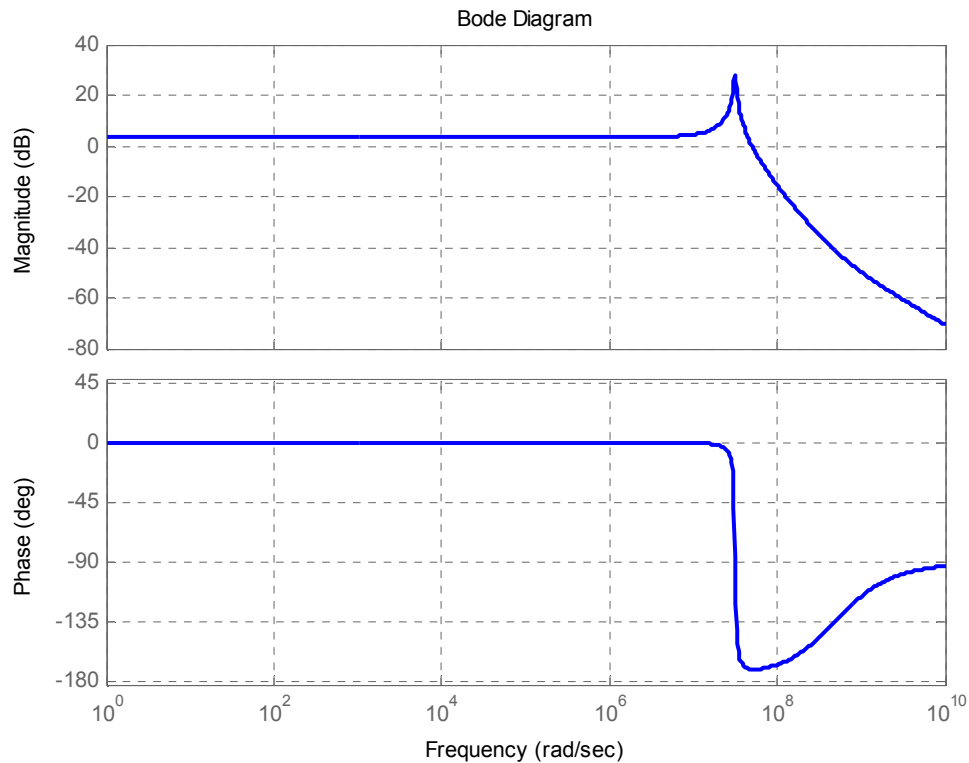
Figure 52. Bode plot showing magnitude and phase of open-loop converter frequency response

The phase response of this system is nearly 180 degrees at the filter resonant frequency, which could lead to instability in the control loop if appropriate phase margin is not maintained. Complete control loop design, which includes analysis of the phase margin and choice of the appropriate compensation network, is beyond the scope of this project but for purpose of discussion, the two most common types of control are presented below.

5.3.2   *Voltage and Current Mode Control*

The control loop must sense some element of the output of the controller in order to adjust the input to maintain stability. This sensing can come in the form of voltage-mode or current-mode control. Voltage mode control senses the output

voltage of the converter directly and applies this voltage (or a divided-down version of it) to an error amplifier. In current mode control, some form of sense resistor is used to monitor the current in the inductor and the resulting sense voltage is used to adjust the PWM. Both modes have different requirements from a system level, as well as their own advantages and disadvantages.

5.3.2.1 Voltage Mode Control

A block diagram of the voltage mode control loop was shown in Figure 50. Here, the output voltage is compared with a reference voltage to create an error voltage. This is compared with a sawtooth waveform to create a variable-width pulse to control the converter switches. The advantage of voltage mode control is that the object of interest, namely the output voltage, is sensed directly by the feedback network. This gives a linear relationship to between the duty cycle of the PWM and the output voltage. The voltage feedback network is straightforward to stabilize, but the circuit requirements for this network are greater than in current mode control. As was mentioned in the discussion of the converter transfer function, the output LC filter network exhibits a double pole at the resonant frequency of the network. This double pole contributes a 90 degree phase shift that impacts the phase margin of the feedback loop considerably.

5.3.2.2 Current Mode Control

The most common setup for current mode control is depicted in Figure 53. In this approach, the peak inductor current I_L is sensed and compared to the output voltage. This forms the inner current control loop. There is also an outer voltage loop that determines the threshold for the current loop. The operation of the control begins when the SR latch is set high by the pulse oscillator once each period of the converter.

With the high-side switch on, the current through the inductor will ramp up, increasing the sense voltage V_{sense}. When a certain threshold is reached for the sense voltage (determined by the error amplifier in the outer voltage loop), the SR latch is reset, ending the on-time of the high side switch. In this loop, the output voltage is controlled by ensuring that the peak current through the inductor is maintained each cycle.
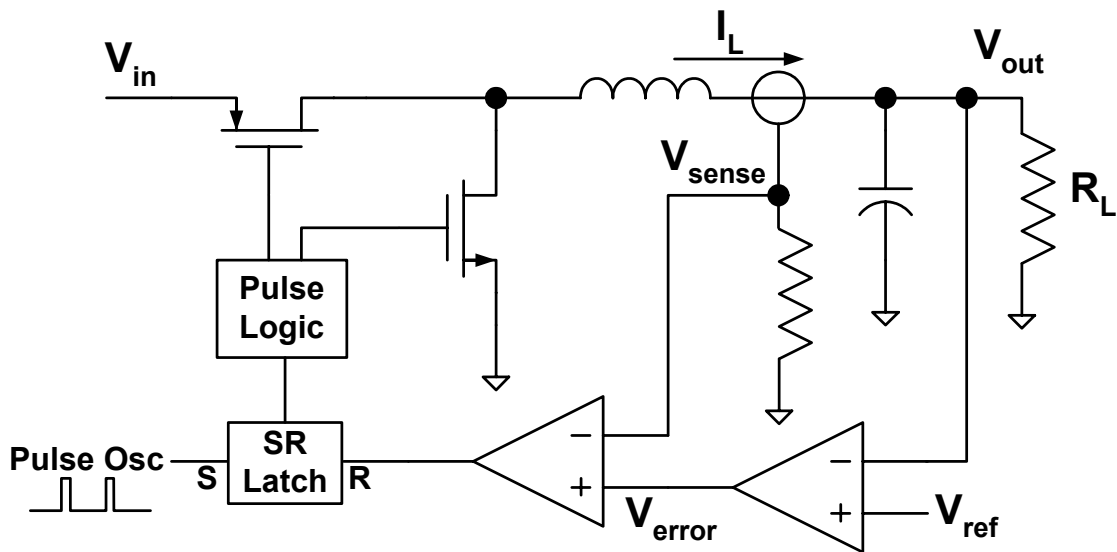
Figure 53. Current mode control feedback loop for buck DC-DC converter

5.3.3 Digital Control Circuitry

With increasing integration between the radio and the baseband in modern RFICs, it is of interest to examine digital methods of control for a DC-DC converter. In the specific application of a variable supply voltage power amplifier, the baseband system can provide power update signals directly as control bits, allowing direct control of the radio components by the baseband processor. This type of control has been discussed before [58,59] but has not been implemented in an RFIC application.

Digital circuitry naturally lends itself to uses in pulse width modulators at high frequencies. In this application, the pulse width would be determined by using a

tapped ring oscillator or tapped delay line, as shown in Figure 54. The resolution of the pulse width output is determined by the number of taps used in such a system, and is thus configurable for many applications.
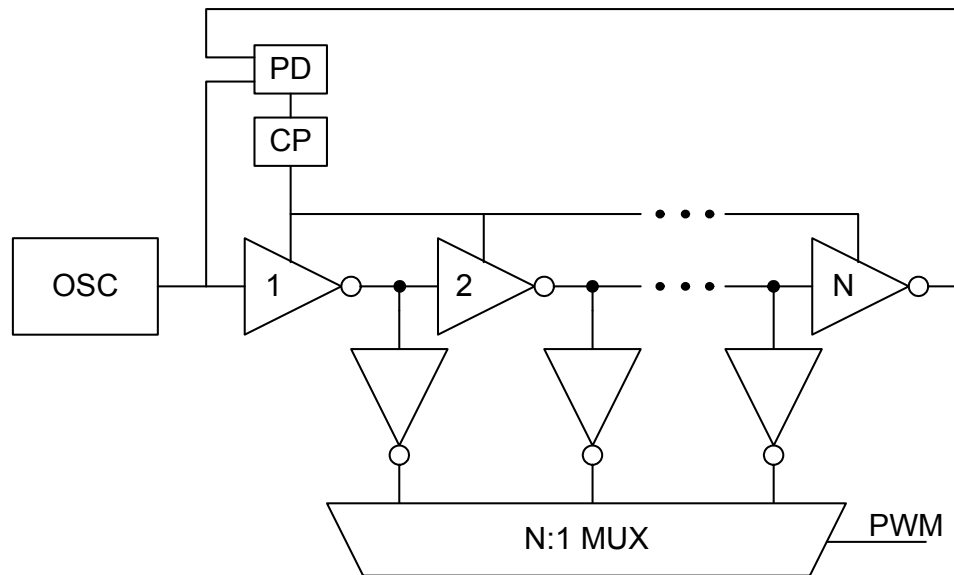
Figure 54. System diagram of a digital pulse width modulator

The system in Figure 54 represents a complete pulse width modulator circuit, including reference clock and delay locked loop (DLL). The DLL is used to synchronize the delay line to the oscillator frequency, ensuring proper PWM frequency and pulse width. This is composed of a phase detector (PD) which controls a charge pump (CP) used to increase or decrease the supply voltage of the delay elements, thereby slowing them down or speeding them up as necessary. This type of system can compensate for changes in the delay line due to temperature and process variations, assuming a stable clock reference.

5.4   System Analysis

5.4.1   Power Amplifier Performance

The effect of a varying supply voltage on power amplifier performance is most evident in the output power and gain versus input power. Because of the reduced supply voltage, the compression point can be seen to decrease because of the output signal clipping at a lower output power. Also, the gain will vary somewhat with the reduced supply voltage because the bias point is changing due to the finite output conductance of the transistors. With such large devices as are used in the power amplifier, however, this change in gain should be minimal, with a variation of only a few dB. The output power versus input power for the varying output stage supply voltage is given in Figure 55.
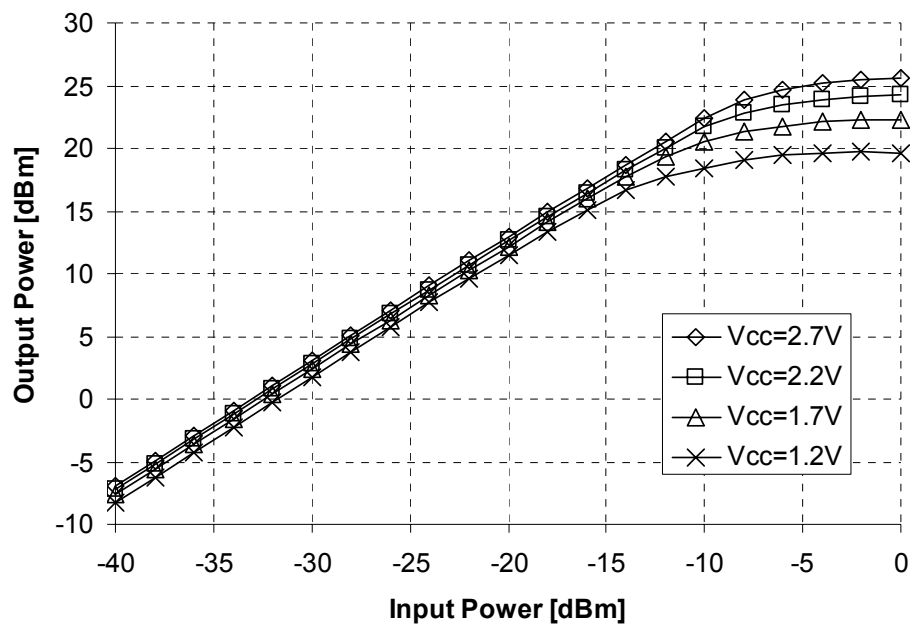
Figure 55. Power amplifier output power variation with change in output stage supply voltage
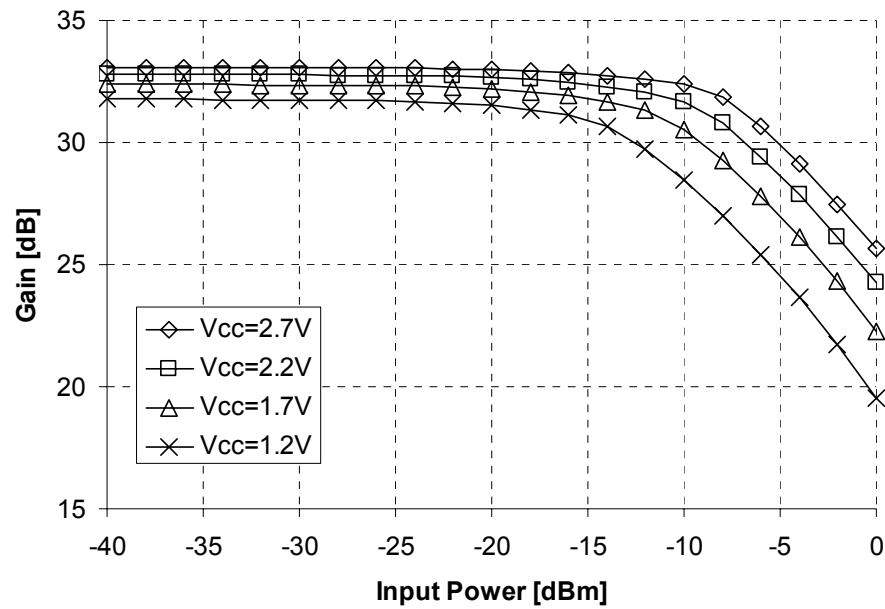
Figure 56. Power amplifier gain variation with change in output stage supply voltage
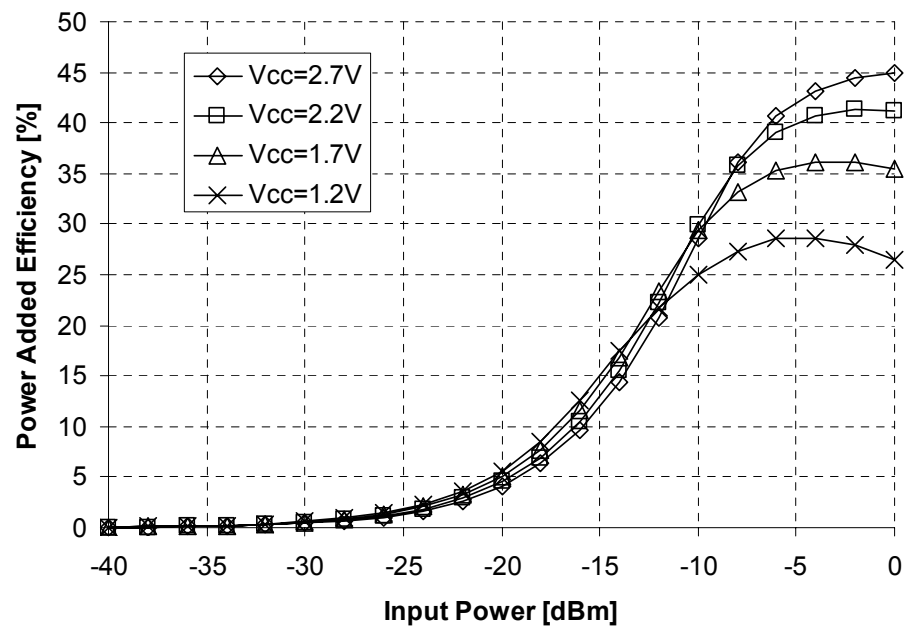
Figure 57. Power amplifier PAE variation with change in output stage supply voltage

Figure 56 shows the change in gain as the supply voltage of the output stage is reduced. The overall change in gain from full supply voltage (2.7V) to 1.2V is only 1.3dB, which is well within the open-loop output power change tolerance of a WCDMA system. The gain curves also illustrate the change in compression point as the supply voltage is reduced. The power added efficiency improvement with reduced supply voltage is given in Figure 57. This indicates that the most improvement is seen around -15dBm input power, with an improvement in PAE of 3%. While this seems to be a very small improvement, the overall system efficiency improvement is seen to be much greater when presented in the proper analysis form as explained in chapter 3.

5.4.2 Chip Layout Issues

Both components of the variable supply voltage system were laid out on a single die for fabrication in the IBM 6HP process. The integration of such a system posed several challenges in layout, due primarily to the potential signal coupling between the converter and the power amplifier. While analysis of the power amplifier indicated that a 1% ripple in the supply voltage at the converter frequency would not impact the output RF signal, in an integrated system there is always the possibility of introducing larger signals to the PA through substrate coupling. To help eliminate the possibility of such substrate coupling, three separate deep-trench guard rings were used to surround the DC-DC converter, with substrate contacts connected to the ground path of the DC-DC converter only. Additionally, the grounds for the converter and power amplifier were kept separate on-chip and only combined at the board level where large amounts of supply decoupling was available.

The power amplifier architecture itself provides some immunity to signals coupled in through the supply and ground lines. Because of the differential architecture, the system will exhibit a rejection of signals that appear at the common-

mode points in the circuit. The addition of decoupling capacitance at these nodes also helps prevent interference because the nodes should be very low impedance at the frequency of the DC-DC converter.

5.5   *Measurement and Testing*

The final chip containing both the converter and the power amplifier is shown in Figure 58. For testing of the combined system, the chip had to be mounted on a board that contained the required passive components for both the power amplifier and the DC-DC converter.
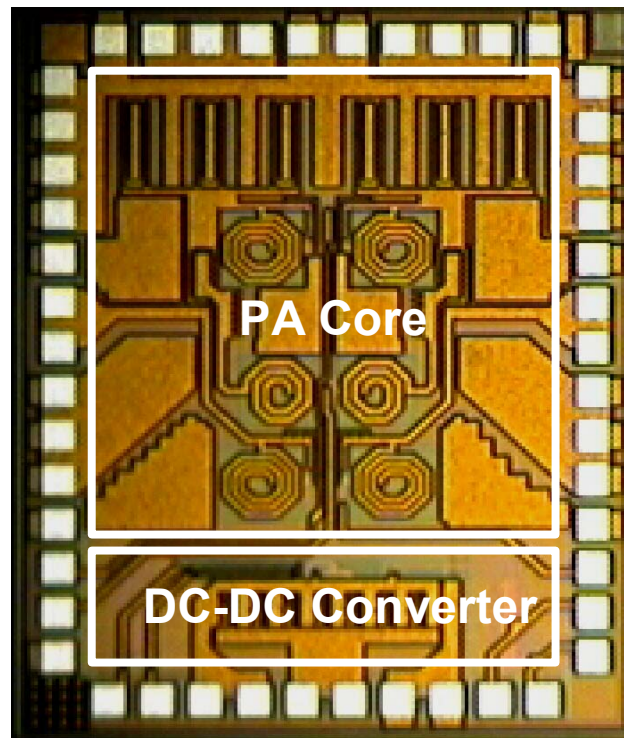
Figure 58. Combined power amplifier and DC-DC converter die photo

The large traces of metal visible at the bottom of the chip in Figure 58 are, from left to right, the supply voltage, the output voltage, and the converter ground. The two PWM signals are brought in to the left of the supply voltage connection, and

the two select bits, S0 and S1, are connected to pads to the right of the ground supply. This allows for room on the board to place the off-chip filter components and make connection to the power amplifier output stage supply voltage.

5.5.1 Board Design for Testing

The system board was designed based on the board for the stand-alone power amplifier. It was designed using IVEX Winboard PCB software and fabricated through PCBexpress. The board design was altered to include space for the required passive components and connectors for the DC-DC converter. Because of the high switching frequency of the converter, the two pulse-width modulator signals are brought in on 50Ω coplanar waveguide transmission lines and terminated with 50Ω chip resistors. This minimized signal degradation due to the board traces. Because the signals drive high-impedance gates, there is still the possibility of signal distortion as they are launched onto the chip due to the final trace and the bondwire inductance. Both pulse width modulator signals and the converter supply voltage are brought onto the board using 50Ω SMB connectors.

A solderable jumper system was also used to allow independent testing of the converter and the power amplifier, as well as the combined system. For converter-only testing, a chip resistor is placed on the board as the load for the converter. The converter can be bypassed entirely for PA testing, and the load resistor can be removed from the system via another jumper to enable the combined system testing. The final board design with all components mounted is shown in Figure 59.
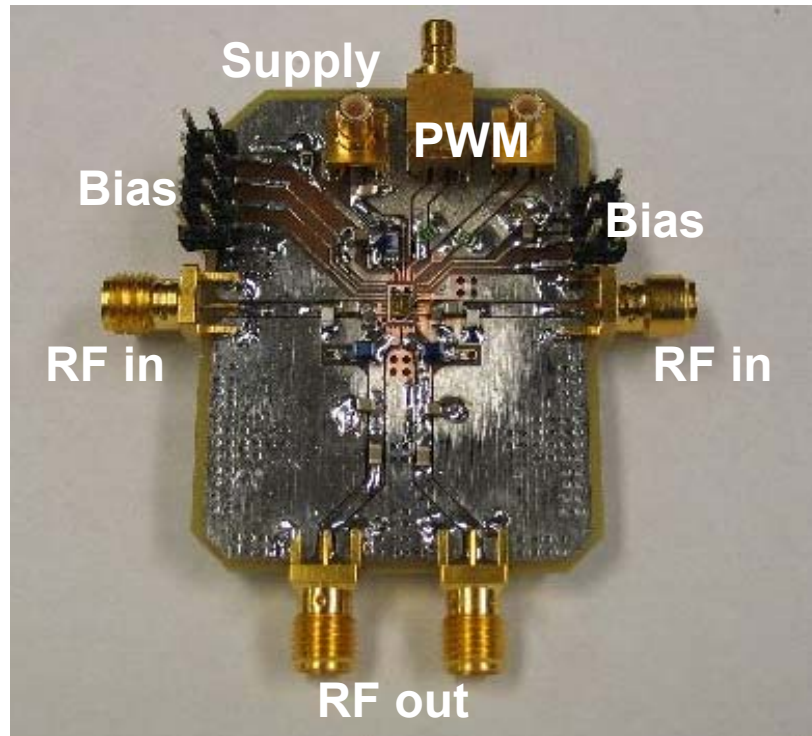
Figure 59. Populated PA/converter board for measurement

The PA/converter chip was mounted to the board and wirebonded to the appropriate connecting pads. The wirebonds were made with aluminum wire with a maximum current handling of 500mA. The bonds were kept as short as possible to minimize inductance, and in paths where high current or low inductance were essential, several bonds were used for improved performance and reliability.

5.5.2 Converter Performance

The DC-DC converter was tested using an Agilent 8133A Pulse Generator to provide the PWM signal for the converter. The output was measured on a Tektronix TDS724A digitizing oscilloscope. A diagram of the test setup is shown in Figure 60. As mentioned above, the pulse signals were driven into 50Ω transmission lines on the board to prevent ringing and harmonics that could arise using a non-controlled impedance trace. The signals were then conditioned on chip by buffers to sharpen

edges of the signals as they reached the converter. The board was initially set up for converter-only testing using a 10Ω resistor for the load resistor. The results are given for a 3V supply voltage over various output voltages and device sizes (based on select bits) in Table 10.
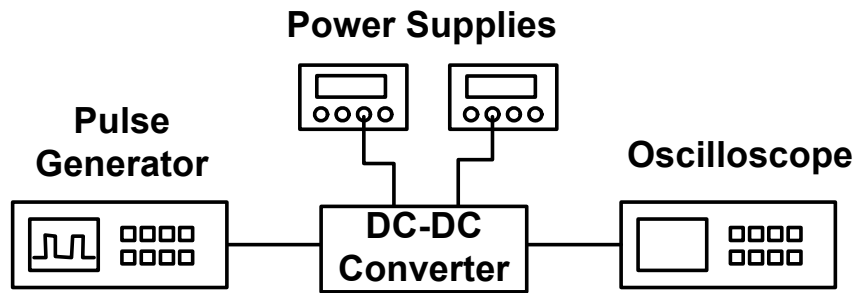
Figure 60. Test setup for DC-DC converter measurement

Table 10. Measured DC-DC converter results

V_{out}	S1	S0	PFET width	Duty cycle	Load current	Supply current	Measured Efficiency	Simulated Efficiency
2.68V	0	0	7.0mm	100%	268mA	266mA	90%	91%
2.24V	0	1	6.0mm	90%	224mA	204mA	82%	84%
1.72V	1	0	5.0mm	75%	172mA	139mA	71%	74%
1.21V	1	1	4.0mm	50%	121mA	79mA	62%	65%

Despite the use of controlled impedance transmission lines, the pulse edges were still slowed by the impedance mismatch of the board to chip connections. This resulted in an increase in the current drawn by the first buffer of the three buffer stages on chip. This additional current draw was verified in simulation, and removed from the supply current used in the efficiency calculations. The total current consumption by the buffers was 8mA for a 50% PWM duty cycle. An additional source of loss not

accounted for in simulation is due to the delay between the PFET turn off and NFET turn on. This was simulated as 500ns, but because of the variable delays that arose from the slowing of the pulses and lack of fully controlled impedance this delay could have varied in either direction. A slower delay time would mean that the devices were both on for a period of time, wasting current in a direct path from supply to ground. A longer delay time would increase the body diode conduction, resulting in an increase in this source of loss. This could easily account for the 1-3% difference in measured versus simulated efficiency in the converter.

5.5.3 System Efficiency Analysis

The advantages of the variable supply voltage, as explained in chapter 3, are most evident through an analysis of the overall reduction in battery current offered by such an approach, rather than examination of the PAE improvement of the amplifier. This analysis can now be applied to this power amplifier, given the drive current of the power amplifier and the measured efficiency of the DC-DC converter. The analysis assumes a linear variation in supply voltage from 2.7V at P_{out}=28dBm to 1.2V at P_{out}=15dBm. From this point on, the power amplifier operates off the 1.2V supply. The battery current drawn by the power amplifier in both fixed and variable supply voltage operation is shown in Figure 61. For the highest power levels, the variable supply power amplifier actually draws more current than the fixed supply version, because the efficiency is not 100% at the highest supply voltage values. This is not a major concern because statistically the power amplifier will be operating infrequently at those power levels.
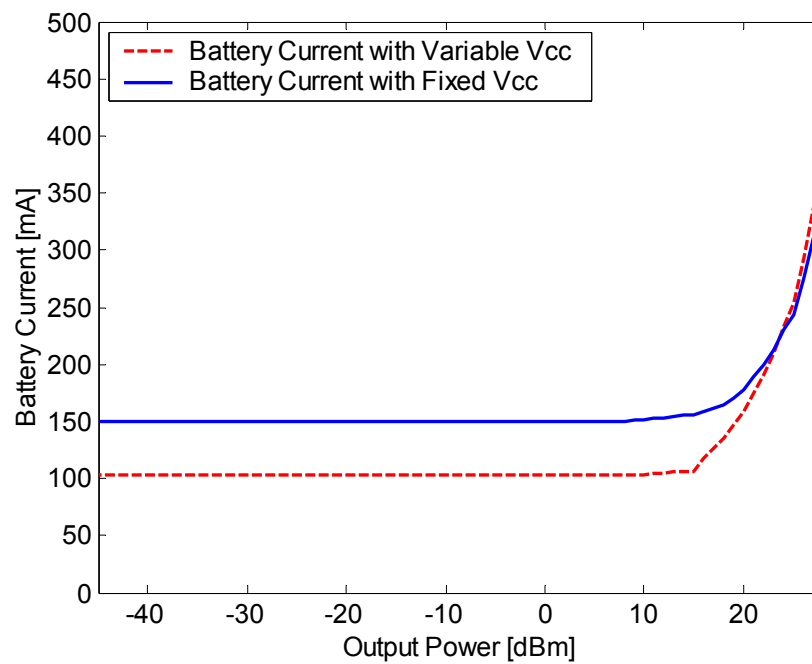
Figure 61. Battery current drawn by the power amplifier for both fixed and variable supply voltage

When this battery current is averaged using the probability density function for CDMA shown in chapter 3, the resulting reduction in average battery current is given in Table 11.

Table 11. Measured average battery current for fixed and variable supply voltage

	Average Battery Current	*Average Power Consumption from a 3V Battery*
Fixed Supply	152.9mA	459mW
Variable supply	107.1mA	321mW
Percent Reduction	30%	

Based on this analysis, the variable supply voltage power amplifier is seen to consume on average 30% less power than when operating from a fixed supply. This is a 10x increase in efficiency compared to that seen by examination of the power added efficiency curves given in Figure 57, indicating the need for the more detailed analysis just performed. This improvement corresponds directly to a 30% talk-time improvement in a WCDMA handset application.

5.5.4 *System Performance*

The total system performance was tested using the Agilent 8133A pulse generator and the Agilent E8364B PNA series network analyzer. The power supplies were used to provide the bias to the power amplifier, and also the select bits and supply voltage for the DC-DC converter. The test setup is given in Figure 62. The operation of the power amplifier under varying supply voltages was confirmed through observation of the power amplifier small-signal gain on the network analyzer. Additionally, the input power from the network analyzer was increased to observe the gain compression characteristic at each voltage level, while the DC current drawn by the power amplifier was also monitored.
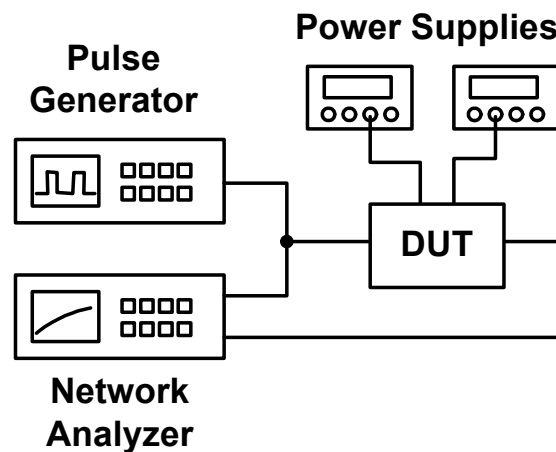
Figure 62. Test setup for combined DC-DC converter and power amplifier measurement

The first measurement made using the network analyzer was the small signal gain, S_{21}, of the power amplifier. For a given output voltage (determined during converter-only testing), the measured and simulated values of S_{21} are given in Table 12. These results show only a slight difference in simulated vs. measured results. The discrepancy corresponds to the difference between simulated and measured small signal gain for the PA by itself. The overall measured change in gain is 1.4dB, which is very close to the 1.3dB predicted in simulation.

Table 12. Measured vs. simulated PA small signal gain under variable supply voltage operation

Converter Output Voltage	Simulated S_{21}	Measured S_{21}
2.7V	32.5dB	31.2dB
2.2V	32.1dB	30.8dB
1.7V	31.6dB	30.3dB
1.2V	31.2dB	29.8dB

Next, the input power was varied to observe the compression characteristics of the power amplifier under variable supply voltage operation. The results are shown in Figure 63. These measurements provide insight into the linearity of the power amplifier under varying voltage conditions.
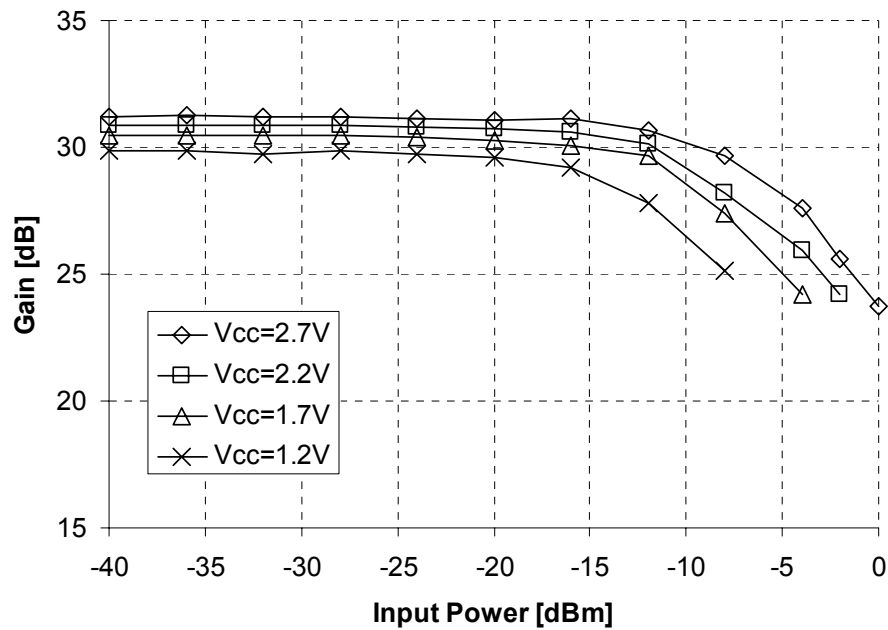
Figure 63. Measured gain compression under variable supply voltage operation

The compression characteristics of the amplifier are very similar to the large signal simulations performed at varying supply voltages. The limited data points at high input power were due to instability in the amplifier as it was pushed further into compression. Based on these gain compression results, the linearity of the amplifier should be similar to the measurements made on the standalone PA assuming the output power is below the 1dB compression point for a given output voltage.

5.5.5   Comparison to Other Designs

As was mentioned in chapter 3, the variable supply voltage power amplifier has previously presented in discrete implementations, though never as a fully integrated system. A survey of those other designs is presented here to provide a comparison and highlight the advantages of the single-chip solution. Table 13 gives a summary of several aspects of the variable supply voltage systems that have been implemented.

Table 13. Comparison of previously published variable supply voltage systems

	Technology (converter / PA)	*Converter type*	*Switching frequency*	*Fixed supply efficiency*	*Variable supply efficiency*	*Integrated system*
[60]	CMOS / GaAs IG-FET	Class S modulator	5MHz	2.2%	11.2%	No
[32]	GaAs HBT / GaAs MESFET	Boost converter	10MHz	3.89%	6.38%	No
[33]	CMOS / LDMOS	Buck/boost converter	500kHz	1.53%	6.78%	No
This work	**SiGe BiCMOS**	**Buck converter**	**89MHz**	**4.53%**	**6.61%**	**Yes**

The efficiency mentioned in Table 13 is the average efficiency of the amplifier, η, defined as

$$\eta = \frac{\overline{P}_{out}}{\overline{P}_{in}} \tag{5.24}$$

This represents the ratio of the average RF output power to the average input power drawn from the battery. In this system, the average efficiency for the fixed supply voltage is 4.53%, while it improves to 6.61% with the use of the variable supply voltage system. While these numbers appear small, this represents a 46% increase in average efficiency for the power amplifier. This is possible because of the large reduction in battery power brought about through the use of the switching converter. This gain in efficiency is comparable to previously published results, all of which used higher efficiency, non-integrated voltage converters operating at lower switching frequencies.

The three previous implementations have all lacked a common technology platform to allow system integration. The designs in [32] and [60] both implement

higher than average switching frequencies to improve the system response to spurious signals. The class S modulator in [60] is very similar to a buck converter, while in [32] a boost converter was used to increase the supply voltage from 3V nominal to 10V at peak output power. The converter in [32] is a discrete implementation, while [33] and [60] offer IC based converter designs, though [33] is similar to this work as it relies on external control circuitry. This comparison demonstrates the differences between this research and the previously published results, and presents what the author believes is the first ever fully integrated variable supply voltage power amplifier. The system is seen to achieve comparable performance to previously demonstrated variable supply voltage systems while offering the advantages of a single chip solution which makes this technology attractive to handset manufacturers.

5.6 Summary

A power amplifier with integrated DC-DC converter has been implemented in SiGe BiCMOS. The converter was designed using the CMOS component of the BiCMOS process, and integrated on the same die as an existing WCDMA power amplifier. The converter used various techniques to improve the low load efficiency to allow operation in a variable supply voltage power amplifier system.

The DC-DC converter was measured and an analysis of the battery current savings for this system was performed using the analysis technique presented in chapter 3, indicating an almost 30% reduction in average battery current. Measurements were performed on the combined system to verify the power amplifier performance under variable supply voltage operation. Overall, the results predict that this system will be able to perform adequately in a cellular handset application, and that such integration is possible in a technology such as SiGe BiCMOS. The system

realizes the goals of variable supply voltage for efficiency improvement as well as integration of such a system on a single chip.

Chapter 6: Conclusions and Suggestions for Further Research

6.1 Summary

The increasing needs of modern communications systems have continually driven the RFIC community to seek improvements in circuit design and integration techniques. The rapid advance of wireless technology has prompted research into CMOS and SiGe radios to deliver increased performance at lower cost. Power amplifiers have been one of the last components of modern communications systems to find a path to integration in these technologies. This research has demonstrated the advantages of using a technology that offers high integration capability for the design of power amplifiers. The integrated system presented here is the first single chip embodiment of a variable supply voltage power amplifier capable of delivering considerable battery current savings, thus increasing system battery life and extending handset talk-times.

Specific achievements and contributions include a WCDMA power amplifier designed and fabricated in SiGe BiCMOS to illustrate that such circuits can be realized in this technology, as well as a CMOS DC-DC converter that was designed to occupy the same die as the power amplifier. This enables an efficiency improvement scheme to demonstrate the integration possibilities of a technology such as SiGe BiCMOS. The combined system achieves a significant reduction in average battery current while providing a low-cost path to a single chip radio.

6.1.1   WCDMA Power Amplifier Design in SiGe BiCMOS

A power amplifier that targets the third generation WCDMA communications standard has been designed in a SiGe BiCMOS process. The differential power amplifier meets the linearity requirements of WCDMA while delivering 21dBm of output power to a 50Ω load. The amplifier was designed with integrated interstage matching networks, requiring only input and output matching networks off-chip. The circuit demonstrates the design possibilities using SiGe BiCMOS for next generation wireless power amplifiers.

6.1.2   High Frequency DC-DC Converter Design

A high frequency DC-DC buck converter was designed by utilizing the high-voltage CMOS component of the SiGe BiCMOS process. The 0.35mm gate length provided reduced series resistance in the PFET switches which allowed for the use of smaller overall device width. The associated reduction in gate capacitance reduced the switching losses in the converter, which was essential to implement a switching frequency at 89MHz. With such a high switching frequency, the converter can be used in sensitive applications such as wireless handset power amplifiers, which was the chosen application of this converter. The completed converter achieves a peak efficiency of 90%, while operating at an efficiency of 63% in its lowest supply voltage and load current configuration. This is possible because of the use of several efficiency improvement techniques, most notably discontinuous conduction mode operation and active device sizing, which had not previously been combined in the same converter.

6.1.3   Single Chip Variable Supply Voltage Power Amplifier

SiGe BiCMOS was used as an integration platform for both a WCDMA power amplifier and a high frequency DC-DC converter. Such a system has been

implemented previously through multiple chips or discrete circuit components, but never before as a single chip power management solution. The power amplifier performance varies little as the supply voltage is decreased, with the most notable changes being the 1dB compression point and the gain, which varies by only 1.4dB over the entire supply voltage range of 1.2 to 2.7V. The combined circuit reduces the average battery current consumed by the power amplifier by 30% while improving the average efficiency by 46%, providing a direct increase in handset talk time and battery life. The variable supply voltage technique is applicable to all linear RF power amplifiers and is limited only by the efficiency of the converter that can be designed in the give technology. This system implementation demonstrates the potential for such an integrated system for use in a 3G handset power amplifier, and will hopefully serve as a starting point for more research into power amplifier integration.

6.2   Suggestions for Further Research

6.2.1   Improved Power Amplifier Performance

This work has demonstrated the power amplifier performance capability of the IBM SiGe 6HP technology, but more work is required to deliver a power amplifier that meets all the specifications of a WCDMA system. Improvements to the matching design of the power amplifier, as well as stabilization at high power are necessary to meet the required output power criteria for the specification. Analysis of system linearity up to the target output power of 27dBm is also required to meet the needs of 3G systems. The high quality factor passives available in the 6HP technology could be used to explore further matching network integration in the power amplifier. Furthermore, EM field analysis could be used to integrate an input or output matching balun on-chip to convert the input or output from differential to single-ended to interface with currently available transmit chain components. Finally, power amplifier

for other communications standards such as wireless LAN could be explored to extend the applications of SiGe in the power amplifier market.

6.2.2 DC-DC Converter Control System

The DC-DC converter implemented in this system still requires externally supplied pulse width modulated signals for proper operation. A continuation of this research would include control loop analysis and design to provide a self-contained DC-DC conversion system for an integrated power amplifier. For maximum efficiency improvement, the supply voltage should be continually variable based on the output power required in the power amplifier. The current approach is based on a "binned" or step-like change in the power supply voltage at different output power thresholds. This step approach could remain in use for the active device sizing, but be replaced with continuous control for the output voltage value. Such a system could also be extended to accept feedback on output power from an on-chip power detector or from a digital baseband power update signal. Digital control loops could also be explored to provide a more direct interface with baseband systems and power control in 3G handsets.

6.2.3 Complete Transmitter Power Control

This work represents a starting point in the use of adaptive power management in modern communications ICs. The integration afforded by SiGe technology could be leveraged to design a complete transmit chain for cellular applications. Integration issues of such a system could be explored, with the goal of realizing a single chip transmitter. Following such work, the variable supply voltage concept could be extended to enable power control from the baseband processor over the entire transmitter. Power amplifier and transmitter linearization could also be implemented

in an integrated transmitter system, allowing a trade-off between efficiency and linearity depending on the current mode of operation and system requirements.

Another approach afforded by the integration potential of a SiGe transmitter would be a full transceiver chip making use of the BiCMOS capabilities of the technology. This would allow the study of the impact of integrated power amplifiers on receiver performance, which is currently not possible because of the mixed technologies used in such systems. The ultimate goal of the single-chip radio would drive designers to seek solutions to integration issues that might arise, possibly resulting in improved receiver architectures or integration techniques for such circuits.

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