DESIGN OF CMOS NEURAL PROBES UTILIZING MICRO-COIL MAGNETIC NEUROSTIMULATION

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Neural prostheses that stimulate the neocortex utilizing electrical stimulation via implantable electrodes have been used to treat a wide range of neurological and psychological disorders. However, fundamental limitations of implantable electrodes have limited the prosthesis effectiveness as there remains concerns over their long-term stimulation efficacy and inability to create precise patterns of neural activity. Latest developments in micro-magnetic technology have shown that magnetic stimulation from micro-coil-based neural probes is capable of modulating neural behavior while circumventing the limitations of implantable electrodes. This is due to the induced electric fields from magnetic stimulation being spatially asymmetric, avoiding the simultaneous stimulation of passing axons, as well magnetic fields having high permeability to biological substances, allowing for complete device encapsulation. While these devices have been shown to modulate neural activity in both *in vitro* and *in vivo* experiments, the lack of reconfigurable hardware on the probe fixes the location of the neurostimulation sites post-implantation. This works explores how co-designing CMOS circuitry, micro-coil design, and nanofabrication processing can be used to fabricate the next generation of micro-coil-based neural probes, capable of spatially programmable micro-magnetic neurostimulation.

BIOGRAPHICAL SKETCH

Edward Szoka was born on September 2, 1991. From 2009-2013 he attended Cornell University and graduated with a Bachelor of Science and Master of Engineering degree. In 2014 Edward continued his education at Cornell University, enrolling in the Ph.D. program in Electrical and Computer Engineering, joining Professor Alyosha Molnar's research group. His research focuses on integrated circuit design for CMOS micro-coil neurostimulator probes and blocker tolerant RF receivers.

To my parents.

ACKNOWLEDGEMENTS

This thesis is the culmination of many years of hard work, and it would not have been possible without the help of many people I have met along this academic journey. I would like to begin by thanking Alyosha Molnar, who took a risk my senior year of undergraduate studies by offering students the opportunity to have their analog integrated circuits final project fabricated in a modern process. While the designed imager did not work and I learned how catastrophic one bit flip could be, the project inspired me to change my career path from hardware design in the aerospace industry to pursuing a Ph.D. in integrated circuits.

This research could not have been done without the help of my colleagues. Sunwoo Lee personally trained me on how to perform the nanofabrication steps necessary to release the neural probes from the original chip packaging, helped with the initial *in vitro* experiments that provided the preliminary results necessary to pursue the research discussed in this thesis, and was the best clean room chemical buddy someone could ask for at three in the morning. I would also like to thank Zach Boynton, Daniel Palmer, and Thomas Tapen for their technical assistance regarding circuit design and lab measurements, and for making the late nights of drawing rectangles to fabricate our circuits much more enjoyable.

I would also like to thank my neurobiology collaborators who made it possible to get meaningful data that showed the proposed neural probes were functional in a biological setting. Shelley Fried, Seung Woo Lee, and Jae-Ik Lee at Massachusetts General Hospital for their technical discussions on designing the micro-coil-based neural probes and for the opportunity to perform *in vitro* experiments on the early iterations of the probes. Furthermore, Thomas Cleland and Jesse Werth in the Department of Psychology provided an opportunity to

perform neurobiology experiments with the proposed neural probes and taught me how to process and analyze recorded neural signals.

This research would also not have been possible without the support from the staff working at the Cornell NanoScale Science and Technology Facility and the Cornell Center for Materials Research for keeping the facilities operational, even during the pandemic. I would like to thank Chris Alpha, Tom Pennell, Jeremy Clark, and John Grazul for training me on all the nanofabrication equipment and fixing the tools when they mysteriously stopped working while I was using them.

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CHAPTER 1

INTRODUCTION

The use of electrical stimulation through implantable electrodes has enabled the development of neural prostheses to treat neurological disorders and restore sensory and motor functionality. The first neural prosthetic to be implanted in a human patient was the cochlear implant in the late 1970s, with the University of Melbourne designing and implanting the first multi-channel cochlear implant in a profoundly deaf patient in 1979 [29]. However, it would be roughly another 20 years before neural prosthesis were deployed to treat other neurological diseases, with deep brain stimulators receiving FDA approval for treating Parkinson's disease and clinical trials for the Argus I retinal implant beginning in 2002 [39, 149]. While this gap in neurotech development is in part due to requiring more neurobiology studies to understand how to treat more neurological diseases, this is also in part due to CMOS technology scaling down from 10 µm nodes down to 100 nm from 1970 to 1998 [106], enabling the creating of smaller and/or more complicated implantable circuitry.

Jumping forward approximately another 15 years to the mid-2010s and the neural prostheses development has improved upon past designs such that patients with two cochlear implants can now experience sound localization through head-related transfer functions implemented in audio signal processing units [6], profoundly blind patients with retinal implants show improvement when performing orientation and mobility tests in a laboratory setting [51], and deep brain stimulators have been expanded to treat other neurological diseases, such as epilepsy, while also being part of a closed-loop system capable of detecting and suppressing epileptic seizures [120]. While these prostheses improve-

ments have aided in treating these neurological diseases, fundamental limitations associated with electrical stimulation through the implantable electrodes prevent the prostheses from replicating lost sensory functionality as patients with cochlear implants struggle with speech detection in noisy environments and patients with retinal implants can only detect large shapes to aid them during navigation tasks.

The first limitation arises from the spatially symmetric electric field produced by implantable electrodes. This prevents specific neurons from being targeted, limiting the effective stimulation spatial resolution as passing axons from nontargeted regions are activated [10,50,115,140]. The unintended activation of other regions can lead to a variety of problematic side effects produced by the neural prosthesis [35,43,46]. While there have been efforts to enhance the stimulation spatial resolution utilizing multiple electrodes, the results have yielded marginal improvements while requiring more complicated electrode structures and driving circuitry [18,146]. The next limitation arises from concerns over the long-term viability of electrical stimulation from implantable electrodes as the stimulation efficacy degrades over time. This is caused by inflammatory reactions generated in response to the neural prosthesis implantation, leading to glial scarring encapsulation around the electrode, which increases the neural activation thresholds [17,49,65,103]. While neurostimulation hardware is designed to allow programmability to increase the stimulation current and re-elicit neural behavioral responses, the increase in the tissue impedance from glial scarring reduces the available headroom for the electrode driver circuitry, potentially preventing the hardware from producing sufficient stimulation currents [26,104,139]. The final discussed limitation is that the electrode-tissue interface is prone to electrochemical effects (such as hydrolysis and corrosion)

that can damage the electrode and/or surrounding tissue if charge transfer levels per phase are too high [30, 91].

Efforts to overcome these limitations have been addressed by changing the neuromodulation modality. One approach is to use optogenetics where the technique genetically modifies targeted neurons to express light-sensitive ion channels, known as opsins, on their membrane [16]. This approach improves the spatial resolution of stimulus as light can be focused to a precise resolution through optical components and only the genetically modified neurons will respond to the light stimulus. Furthermore, optoelectrode neural probes can be fabricated with micro-LEDs that are on the scale of stimulating micro-electrodes that can be entirely encapsulated, thus eliminating the electrode-tissue interface [92]. However, optogenetics to be used in human therapeutics suffer from the safety and difficulty concerns over the viral gene delivery. Furthermore, foreign body responses, such as glial scarring encapsulation, surround the optoelectrode probe and cover the micro-LEDs, thus reducing the stimulation efficacy over time [107].

Magnetic stimulation is another well-established approach for modulating neural activity that overcomes all the previously mentioned limitations with both micro-electrodes and optoelectrodes. Traditionally, this has been explored using transcranial magnetic stimulation (TMS) which utilizes large coils positioned adjacent to the scalp to modulate activity of cortical neurons [8]. The magnetic fields induce electric fields within the brain of the patient, and if the gradient of the electric field is sufficiently strong, there will be activated neural activity [115, 116]. Since the induced electric fields in the brain are located far away from the coils, the electric field gradients are too weak to activate neu-

ral activity. However, pyramidal neurons located at the top of the brain have a significant bend in their axon geometry, allowing the induced electric fields to produce an effective gradient along the bend of the axon to generate local membrane depolarization sufficient to generate action potentials [118].

Initial assumptions claimed that magnetic stimulation would be limited to TMS as implantable coils could not produce fields strong enough to modulate neuronal activity. However, developments in micro-magnetic technology have created implantable micro-coils that produce sufficient spatially asymmetric induced electric fields to avoid the activation of passing axons, thus confining the effective stimulation region [76, 77, 119]. Furthermore, since magnetic fields have a high permeability to biological tissue and biocompatible materials, their stimulation efficacy is not weakened by glial scarring and can be completely encapsulated in materials that mitigate the implantation response [21, 53, 122]. This is an improvement over implantable electrodes that require openings in the encapsulation layer and can suffer from water infiltration due to weak bonding between the encapsulation layer and exposed electrode surface [80, 81]. While implantable micro-coils devices on the scale of implantable electrodes have been shown to modulate neural behavior in *in vitro* and *in vivo* experiments, these devices lack reconfigurable hardware that is more commonly seen in implantable electrode systems, thus fixing their stimulation sites after implantation [40, 66].

The work in this thesis builds upon the current state of micro-coil-based neural probes by integrating CMOS technology with the micro-coil design to develop neural probes capable of spatially programmable micro-coil-based magnetic stimulation.

1.1 Dissertation Overview

The rest of this dissertation is organized as follows:

- **Chapter 2** discusses the CMOS implementation of a programmable micro-coil as well as the nanofabrication process to release the neural probes from the original chip packaging. *In vitro* experiments with the proposed probe are done in conjunction with a commercial MEA and mouse olfactory bulb slices to record changes in neural behavior.
- **Chapter 3** builds upon the work in Chapter 2 by co-optimizing independent CMOS coil drivers with the micro-coils to maximize the induced electric field gradients. Characterization of micro-coil-based stimulation artifacts is also performed with recording electrodes located on the surface of the probe above the programmable stimulation sites.
- **Chapter 4** improves on the design proposed in Chapter 3 by upgrading to a high voltage SOI-CMOS process and integrating neural recording amplifiers capable of tolerating stimulation artifacts produced by micro-coil magnetic neurostimulation.
- **Chapter 5** introduces a high-compliance CMOS current DAC topology that can be used to bias neural amplifiers operating on a low supply voltage. Furthermore, this technique can be expanded to the output stage of current drivers to reduce the headroom consumed by such circuitry.
- **Chapter 6** explores baseband filtering circuit techniques to enhance the selectivity of highly tunable radio frequency (RF) filters built with passive mixer-first receivers. While the discussed focus is in the RF domain, these

techniques can be applied to lower frequencies to suppress out-of-band interferers produced during micro-coil magnetic stimulation.

CHAPTER 2

NEURAL PROBE UTILIZING CMOS-BASED PROGRAMMABLE MICRO-COIL FOR MAGNETIC STIMULATION

2.1 Introduction

Electrical stimulation delivered through implantable electrodes has allowed for the development of neural prostheses to treat various neurological and psychological disorders [3, 12, 105, 123]. Despite the progression and development of neural prostheses there are several fundamental limitations associated with electrical stimulation in conjunction with implantable electrodes that limit the long-term viability of this approach. The first limitation is the inability to target specific types of neurons or limit the stimulation area to a confined region. This arises from the produced electric fields from monopolar electrodes (distant return electrode) being spatially symmetric as well as the high sensitivity passing axons have to prosthetic stimulation [115]. This can cause the effective stimulation region from spreading beyond the local area surrounding the electrode and limit the ability to produce precise patterns of neural activity [10,50,140]. Efforts to enhance the stimulation spatial resolution utilizing multiple electrodes (bipolar drive or hexagonal configurations) have reported marginal improvement, but require more complicated electrode structure and driving circuitry [18,146]. Another limitation arises from the long-term implantation of micro-electrodes as the stimulation effectiveness degrades over time. One of the causes for this is from the formation of glial scarring around the electrodes and can lead to complete encapsulation around the electrode, thus limiting their effectiveness over time [42, 112]. While it is possible to increase the stimulation current to re-

elicit neural behavioral responses, the increased tissue impedance from the glial scarring seen by the electrode reduces the available headroom for the electrode driver circuitry, potentially preventing the hardware from producing sufficient current to elicit neural responses or significantly increasing the neurostimulator supply voltage [26, 104, 139]. The final discussed limitation of electrodes is the electrode-tissue interface is prone to electrochemical effects (such as hydrolysis and corrosion) that can damage the electrode and/or tissue if charge transfer levels per phase are too high [30, 91].

Magnetic stimulation from implantable micro-coils overcomes the addressed limitations inherit with electrical stimulation from implantable electrodes. The lack of a confined stimulation region seen in electrode-based electrical stimulation is overcome by the induced electric fields in magnetic stimulation being spatially asymmetric, thus avoiding the activation of passing axons [15, 78]. Furthermore, magnetic fields have a high permeability to biological tissue and therefore their efficacy is not diminished by glial scarring encapsulation. Finally, the lack of direct contact to the tissue allows for complete encapsulation in biocompatible materials that mitigate the implantation response [21, 53, 122]. This is in contrast to implantable electrodes that require openings in the encapsulation and suffer from water infiltration through weak bonding between the exposed electrode and encapsulation material [80, 81].

Initial micro-coil-based neurostimulation utilized commercial multilayer inductors coated with parylene C. While the inductors were capable of suppressing neural activity in *in vitro* experiments with mouse subthalamic nucleus slices [79], their cross-sectional area is $500 \times 500\,\mu m$, roughly 100× larger than commonly implantable electrodes. Recent developments in implantable micro-

coil technology have produced devices capable of eliciting neural behavior in both *in vitro* and *in vivo* experiments while being a similar size to their implantable electrode counterparts [76, 77]. However, the lack of reconfigurable hardware in these devices fixes their stimulation sites after implantation when it is common for an implantable electrode-based neural probe to contain multiple stimulation sites controlled by programmable hardware [41, 66].

To address the lack of hardware reconfigurability in present micro-coil devices, a programmable micro-coil using CMOS technology with subsequent nanofabrication steps is developed to produce a neural probe capable of spatially programmable magnetic neurostimulation sites [130]. This study builds upon the prior work by exploring the spatial extent of the programmable micro-coil magnetic stimulation under various programmable states and stimulation amplitudes. *In vitro* experiments record the neural response of mitral/tufted cells in mouse olfactory bulb slices across a commercial microelectrode array (MEA). Action potentials across the array are recorded, identified into clusters, and changes in the spiking behavior to the stimulus across the array is compared across the programmable micro-coil states and stimulation amplitudes.

2.2 Physics and Simulations

2.2.1 Electromagnetic Theory

For a device to stimulate neural tissue a sufficient gradient in the E-field must be produced along the axon of a neuron to generate local membrane depolarization sufficient to generate action potentials or synaptic release. This has been

demonstrated with previous micro-coil based neural probes by flowing current through a wire that travels down one edge of the probe, bends at the tip of the probe, and returns along the opposite edge [80, 81]. The bend generates a local spatial gradient in the magnetically induced E-field, determined by the bend geometry. The proposed programmable micro-coil design contains periodic segments along the probe where the current can be programmed to cross between opposite sides, creating multiple sites with programmable gradients in the E-field along a single probe.

The derivation for the induced E-field for a solenoid can be found in [77] and is expressed as:

$$\vec{E} = -\frac{\mu_0 N \frac{\partial i}{\partial t}}{4\pi} \cdot \oint \frac{dl}{\vec{R}} \tag{2.1}$$

Where μ_0 is the permeability of free space, N is the number of coil turns, i is the electric current flowing through the micro-coil, $\vec{R}$ is the vector between the coil and target segment at which $\vec{E}$ is being calculated, and dl is the infinitesimal element of the coil.

From this, the spatial gradients $\partial Ex/\partial x$, $\partial Ey/\partial y$, $\partial Ez/\partial z$ can be calculated as a function of the distance to the micro-coil. For example, the x, y gradients for a wire that progresses along the x-axis, forms a right-angle at the origin, then progresses along the y-axis can be shown as:

$$|\partial Ex/\partial x| = |\partial Ey/\partial y| = \frac{\mu_0 N \frac{\partial i}{\partial t}}{4\pi \cdot \sqrt{x^2 + y^2 + z^2}} \tag{2.2}$$

Where the sign of the gradient terms is set by the direction of the current

flow and bend orientation. If multiple such wire turns are present in the same plane the resulting gradient is the sum of the gradients induced by each turn. Concatenating two such turns results in either no gradient or approximately double the gradient strength depending on the relative signs of the current in the two wires.

2.2.2 Electromagnetic Modeling

To accurately predict the location and strength of the local E-field gradients the programmable micro-coil neural probe is modeled using the Magnetic and Electric Field (mef) module within COMSOL Multiphysics. Finite element method (FEM) simulations are performed to calculate the spatial gradients of the induced E-fields arising from the current flow through the programmable micro-coil under different states. The model is shown in Fig. 2.1 and consists of the micro-coil traces and switchable metal traces (including approximations for the switches) to control the current flow within the micro-coil over a conductive silicon substrate etched in the shape of a probe. Simulations are done with the programmable micro-coil under three different states: through, short, and cross (Fig. 2.1C-E). The programmable micro-coil states are modeled by adjusting wire boundaries to allow current to flow through desired paths while presenting a high impedance to the undesired paths. The aluminum micro-coil traces have a cross-sectional dimension of $2.5 \times 25\,\mu m$ with a wire spacing of $50\,\mu m$. The silicon substrate has a cross-sectional dimension of $60 \times 110\,\mu m$ and a length of $715\,\mu m$, with the last $45\,\mu m$ tapering to a point. The switchable traces split the original $2.5\,\mu m$-thick traces into two separate traces to allow the current to switch which side of the probe the current is flowing along. The dimensions

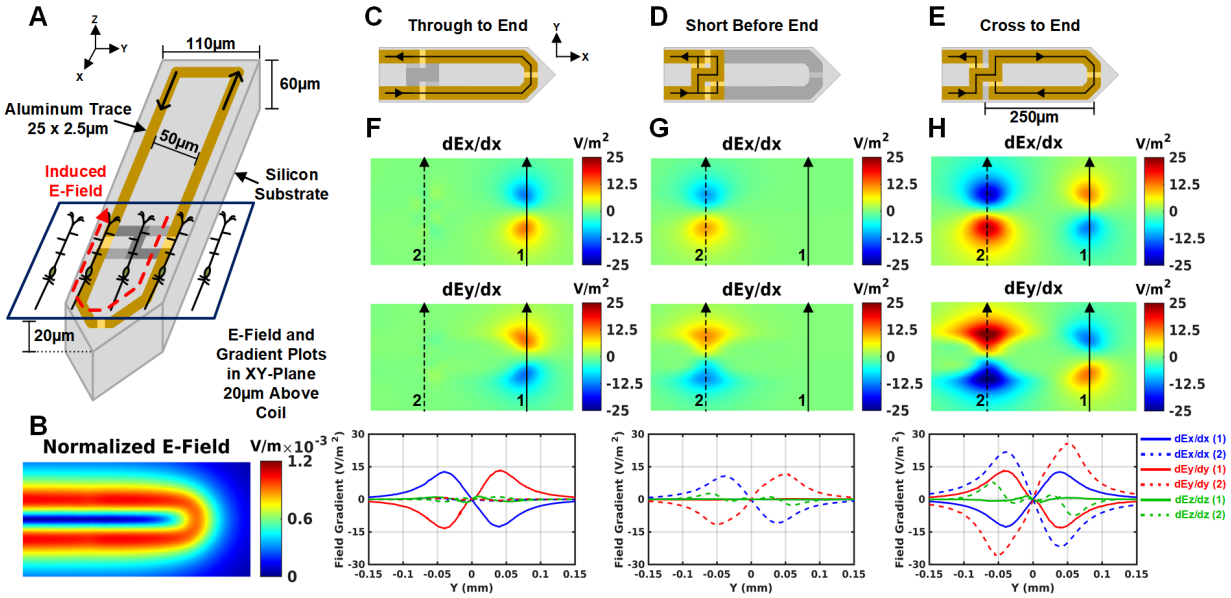

Figure 2.1: Electromagnetic simulations for various programmable micro-coil configurations. (A) Conceptual diagram for micro-coil based magnetic stimulation for the 'through' state. (B) Normalized induced electric field in the xy-plane 20 µm above the neural probe. (C) Neural probe in the 'through' state. Metal traces that are disconnected to emulate the switching network are grayed out. Black lines show the current flow throughout the micro-coil used in the simulations. (D) 'Short' state. (E) 'Cross' state. (F-G) Spatial gradients of the electric field along the x- and y-axes for the configurations used in C-E. The line plots show the field gradients along the y-axis over the tip of the probe (solid lines) and the switch network (dashed lines).

of the probe results in a cross-sectional area comparable to micro-fabricated intracortical electrodes that are routinely implanted without causing significant damage to the neural tissue [69, 136].

A similar simulation environment is built as in [76] where the modeled neural probe is surrounded in a 1 mm^3 medium with the properties of gray matter (electrical conductivity: σ = 0.27 S/m; relative permittivity: ϵ_r = 12,000) [137]. The environment was selected to allow for simulation comparisons to previous studies and was split up using a finer mesh with the programmable micro-coil is simulated in a closed loop configuration. The programmable micro-coil is

sufficiently long such that the induced E-fields from the input current ports do not affect the simulation results near the programmable stimulation sites. The input of the programmable micro-coil is a 5-kHz, 150-mA sinusoidal current and initial counter-clockwise direction (Fig. 2.1A, black arrows). The current flow throughout each simulated programmable micro-coil state is shown in Fig. 2.1C-E. The induced E-fields and their spatial gradients produced by the programmable micro-coil are calculated in COMSOL Multiphysics along a plane 20 µm above the coils surface. The value of 20 µm is selected based on the size of the cell body for mitral cells as well as accounting for the expected encapsulation thickness during nanofabrication processing [99].

2.2.3 Simulation Results

The resulting normalized E-field for the 'through' state is plotted on a plane 20 µm above the surface of the probe. The E-field is strongest directly above the programmable micro-coil traces (Fig. 2.1B). The spatial gradients along the x- and y-axes (dEx/dx and dEy/dy) are plotted in the same plane for the three programmable states (Fig. 2.1F-H). Consistent with other studies the strongest field gradients appear above where the current flow is changing directions and the polarity for the gradients are flipped (positive peak of dEx/dx is located at the negative peak of dEy/dy and vice-versa) [76–78]. For the 'through' state the maximum gradients for dEx/dx and dEy/dy are 12.60 and 13.37 V/m^2 respectively. There are small gradients present around the switch network that are over six times weaker than the gradients present around the tip of the probe. These unintentional gradients arise from the current flow through the modeled switches. Furthermore, there are unintended E-field gradients along the z-axis

that located along the sides of the silicon probe and are over a magnitude in strength weaker than the x,y gradients (maximum dEz/dz 1.54 V/m^2).

When the programmable micro-coil is set to the 'short' state the stimulation sites move from the tip of the probe to over the switch network. The maximum field gradients for dEx/dx and dEy/dy are 10.70 and 11.82 V/m^2 respectively. The slight decrease in the field gradient strengths is attributed to the increase in routing area needed for the switch network, thus decreasing the current density flowing through the micro-coil traces. As seen in the 'through' state there are gradients along the z-axis located along the side of the probe with a maximum strength of 2.64 V/m^2 respectively. The z-axis gradients arise from the silicon substrate shaping the electric field. Finally, since the impedance from switch network looking towards the tip of the probe is made to be an open-circuit there are no unintended field gradients present at the tip of the neural probe.

In the 'cross' state there are now two sets of stimulation sites: one present at the tip of the probe and one above the switching network. The maximum x, y gradient strengths at the tip are 12.60 and 12.91 V/m^2 respectively, while the gradients over the switch network increase to 21.80 and 25.76 V/m^2 respectively. The increase in the gradient strengths over the switch network is caused by the current flowing along the x-axis switching directions and the current flowing along the y-axis being doubled. The maximum z-axis gradient located over the switching network is 7.81 V/m^2, showing that while the 'cross' state produces the strongest stimulation gradients, it also has the worst orientation-based selectivity. However, the ratio of the x, y gradients to the z-axis gradient is at least 2.7, suggesting that fine tuning the stimulation current can keep the unintentional E-field gradients from stimulating passing axons, thus preserving

the orientation-based selectivity by not stimulating neurons orientated orthogonally to the plane of the probe.

The x, y gradient strengths are also observed on a plane 100 µm above the surface of the coil to explore the capability of the programmable micro-coil to stimulate neurons farther away from the surface of the probe. For all programmed micro-coil states the field gradient strengths decreased by a factor of ten suggesting that the proposed neural probe is capable of only stimulating neurons near the surface of the probe. The simulation results suggest that the proposed neural probe is capable of targeting different neuronal regions, such as individual layers of the neocortex, while maintaining confined, effective stimulation regions.

2.3 Neural Probe Design and Fabrication

2.3.1 Circuit Design

The proposed neural probe system is shown in Fig. 2.2. The system is designed with four programmable stimulation sites. The first three programmable stimulation sites are implemented with a switching network, where the current flowing through the network is controlled by a two-bit digital input. The final programmable stimulation site is implemented with a single switch that either passes or blocks current from flowing towards the tip of the probe. The switching networks can be programmed into one of the following states: through, cross, short, or open-circuit. The switches are implemented with CMOS transmission gates with the NFETs and PFETs sized at a width-length ratio of 1.5

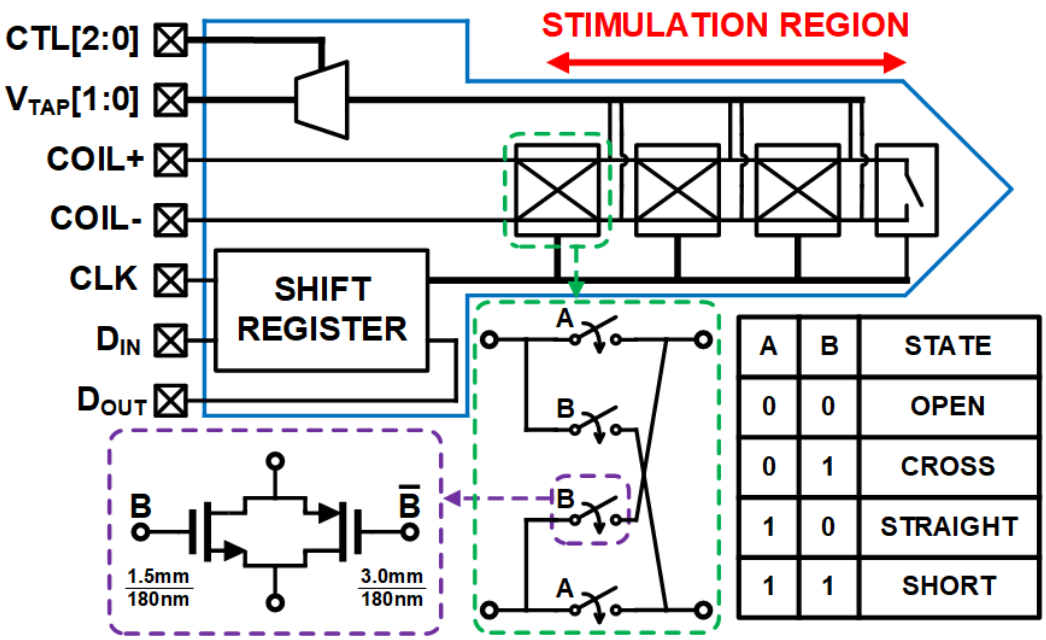

Figure 2.2: High-level diagram of the proposed neural probe with the circuit implementation of the programmable micro-coil neurostimulation sites.

mm to 180 nm and 3 mm to 180 nm respectively. The sizing of the FETs was selected to allow for a maximum stimulation current of 200 mA while ensuring that no transistor observed a junction voltage above the 2 V breakdown limit. The backend circuitry around the pads consists of a programming interface as well as testing peripherals. The programming interface is implemented with a shift register and buffers to drive the bits along the probe to the switching networks. The testing peripherals consist of multiplexed coil segments to verify the coil current direction based off the voltage measured along each segment.

2.3.2 Probe Release Nanofabrication Processing

Neural probes are thinned down and released from the original chip packaging through a series of nanofabrication steps. The process begins by deposit-

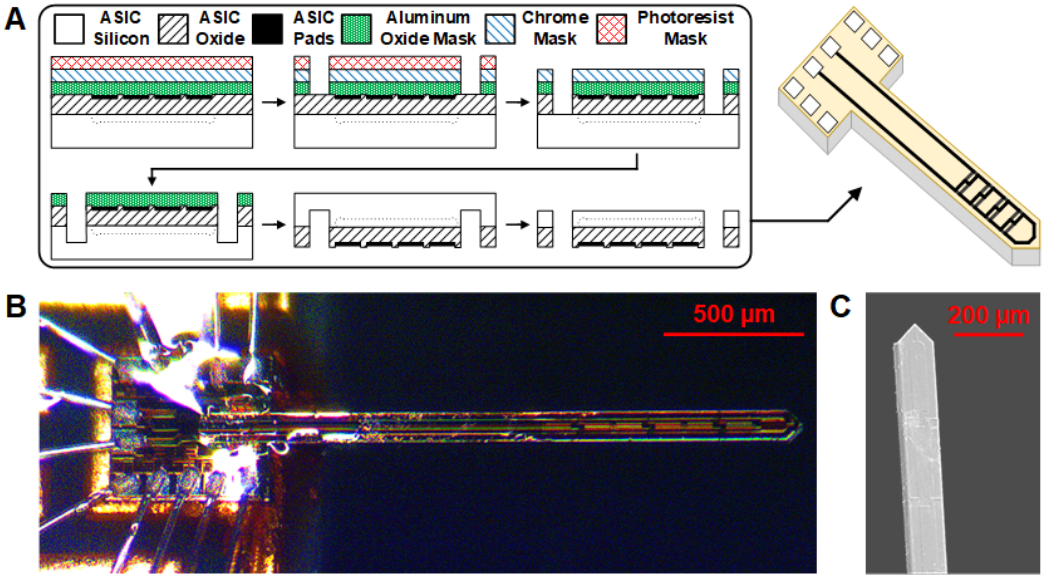

Figure 2.3: Post-nanofabrication processing. (A) Nanofabrication process to release the neural probes from the original chip packaging. Mask layers that are no longer used are etched away between the shown steps. (B) Micrograph of an encapsulated neural probe. (C) SEM image of stimulation sites of a released neural probe.

ing Al_2O_3 and Cr using atomic layer deposition (ALD, Oxford ALD FlexAL) and sputter deposition (ATC-Orion 5 UHV with Load-Lock by AJA International INC) techniques respectively. The layers serve as the silicon etching and oxide etching masks and are patterned in the shape of a probe using contact photolithography (ABM Contact Aligner) as well as wet etching and plasma etching processes. The oxide layer is etched using a CF3/O2 inductively coupled plasma (ICP, Oxford Plasmalab 100 ICP RIE) etch to expose the bulk silicon. Trenches are etched into the bulk silicon using a deep reactive ion etch (DRIE, Unaxis SLR-770 ICP Etcher) process down to the desired probe thickness of 60 µm. The chips are flipped upside down and the backsides are cleaned using mechanical polishing as well as plasma etching processes. Then the previous silicon DRIE process is used to etch the back of the bulk silicon until the neural probes are released. The nanofabrication process to release the probes is

shown in Fig. 2.3.

The released probes are mounted to a carrier printed circuit board (PCB) using conductive silver epoxy (8330S-21G Silver Conductive Epoxy, MG Chemicals) and electrically connected with wire bonds (Westbond 7400A). The wire bonds are protected using a clear epoxy (EPO-TEK 301, Epoxy Technology) before the entire assembly is coated with approximately 4 µm of parylene C (PDS 20210 Labcoter 2) to ensure that traces from the neural probe or the PCB are not making direct contact to the tissue or solution during experiments. At this point the proposed neural probe nanofabrication processing and assembly is complete as there are no electrodes that require openings in the encapsulation layer.

2.4 Experimental Methods

2.4.1 Hardware Design

The neural probes are originally fabricated in a 180 nm one poly, six metal CMOS technology process (Fig. 2.4). The probes are originally packaged in a diced piece of bulk silicon with approximate dimensions of 5 × 5 mm with a thickness of roughly 300 µm. After release the insertable shank of the probe is roughly 1900 µm long with a cross-sectional area of 60 × 110 µm and a back-end area of roughly 500 × 500 µm. Due to the non-linear resistance of the FETs in the switch networks dominating the micro-coil impedance, custom hardware is designed to ensure the desired current flows through the programmable micro-coil. The analog output of a DAQ (USB-6218, NI) is connected to a custom push-

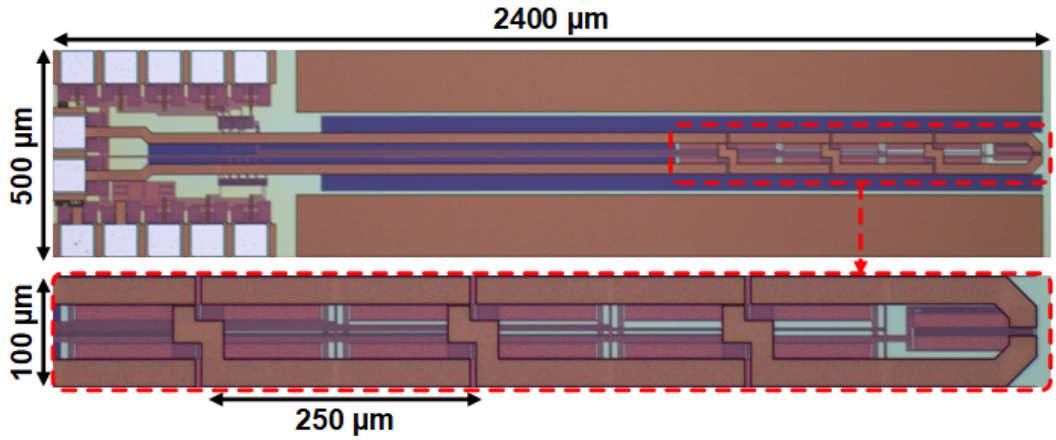

Figure 2.4: Micrograph of an unreleased neural probe and stimulation sites.

pull current driver with a gain of 200 mA/V. The input coil terminals as well as the multiplexed segments are monitored with an oscilloscope (MSO2014B, Tektronix, Inc.) to ensure safe operation of the probe. The custom hardware also regulates the supply voltage delivered to the probe and level shifts the programming bits produced by the programming DAQ (USB-6251, NI) and is shown in Fig. 2.5.

The stimulation waveform is a 50% duty-cycled ramp waveform with a frequency of 10 Hz. During *in vitro* testing a train of 50 of ramp waveforms are delivered to the programmable micro-coil. The selection of a 10 Hz stimulation frequency based off the known theta rhythms observed in olfactory bulb slices [64]. The selection of the ramp stimulation waveform is selected to produce short, strong bursts in the induced E-field.

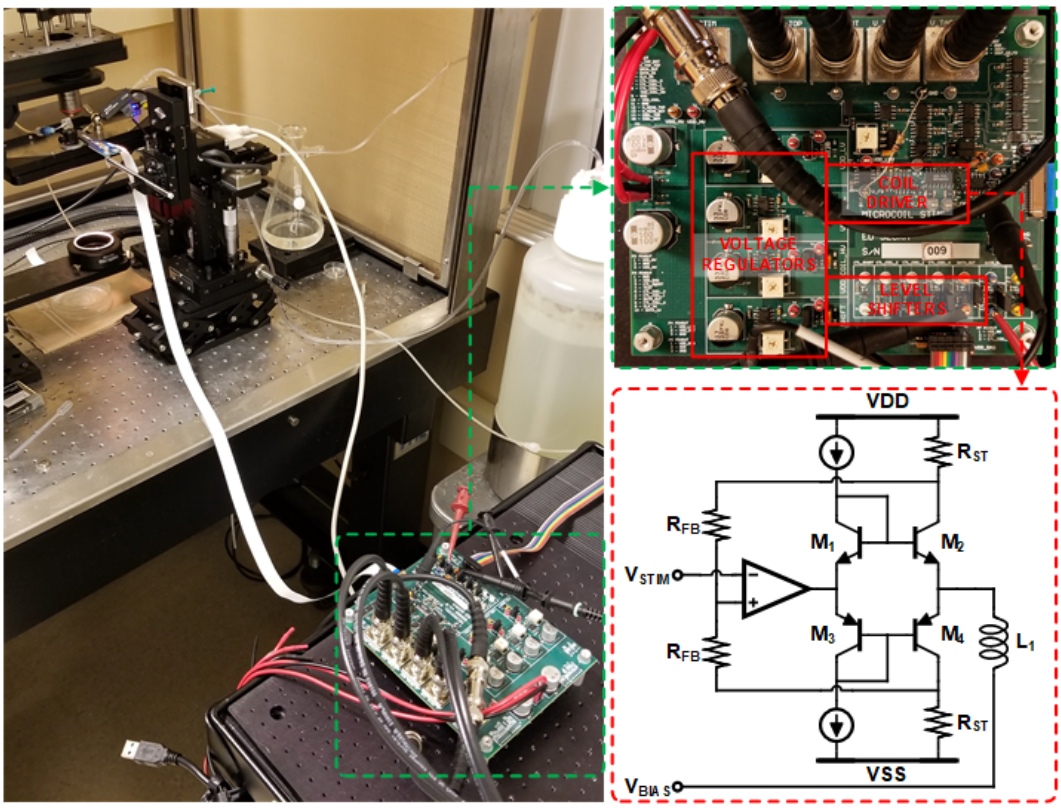

Figure 2.5: *In vitro* test experiment setup with custom PCB to program, power, and drive the micro-coil. Circuit implementation of push-pull current driver is shown.

2.4.2 In Vitro Olfactory Bulb Slice Experiments

In vitro testing is done on 300 µm-thick slices of mouse olfactory bulbs from 5-12 week-old mice. The tissue is horizontally sliced with a vibrating microtome and bathed with oxygenated artificial cerebrospinal fluid (aCSF) at 34°C during recordings. Slices are aligned to the MEA by locating bands of spontaneous activity that indicate the mitral cell and external plexiform layers [108]. The programmable micro-coil neural probe is placed on top of the slice above the band showing the most activity. Neural activity is then recorded throughout the trials of delivering the desired stimulation waveform to the probe for various programmed micro-coil states and stimulation currents. The placement of

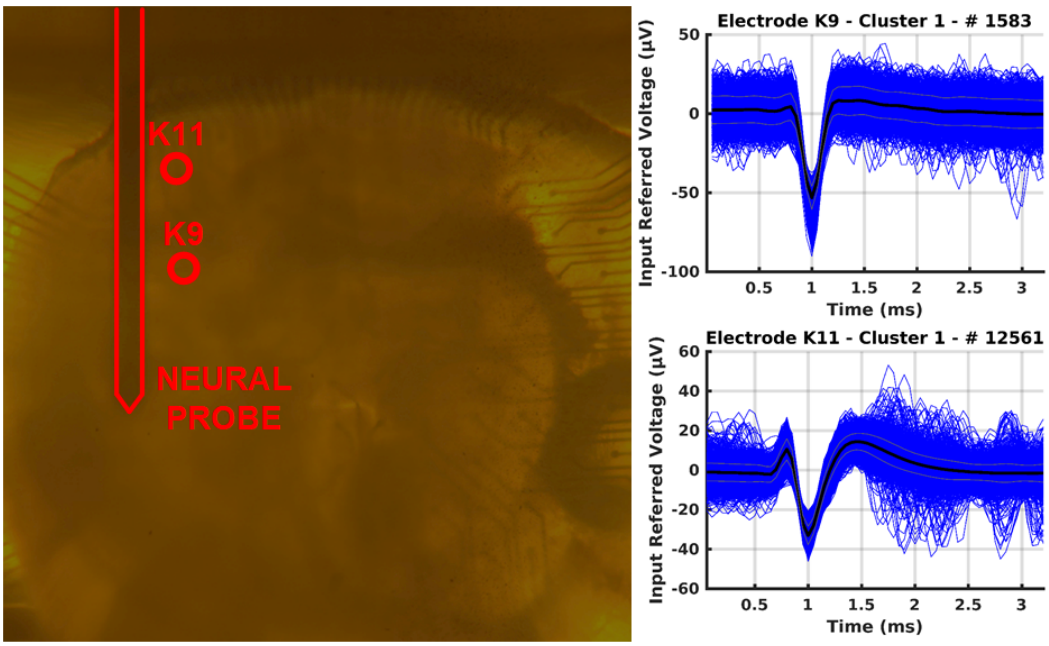

Figure 2.6: Micrograph of *in vitro* experiment setup with time-aligned spikes detected by [24] on electrodes K9 and K11. The olfactory bulb slice is placed on top of the electrode array and the proposed probe lays flat on top of the slice.

the proposed probe to the tissue and MEA is shown in Fig. 2.6. Note that the recordings are measured on the bottom of the slice and the stimulation is occurring on the top slice. Since the slice is too thick to directly stimulate recordings occurring on the bottom of the slice, the measurements are recording indirect stimulation responses and statistical analysis is used to determine if the programmable micro-coil stimulation affected the recorded neural behavior of the slice.

Spikes and local field potentials (LFPs) are recorded using a 120-electrode MEA (MultiChannel Systems) with titanium nitride electrodes (30 µm diameter, 30-50 kΩ impedance, 200 µm pitch). The electrodes are embedded within a thin polyimide foil that is perforated (20-90 µm diameter) to facilitate perfusion and oxygenation of the slice from both sides and to draw the slice down against the MEA with a gentle vacuum, which improves the signal-to-noise ratio and

enables the use of thicker slices with correspondingly richer lateral connectivity. Recordings are bandpass filtered (1 Hz – 3.3 kHz) and amplified (1200x) before sampling at 20 kHz with a bit depth of 24 bits per sample. This enables spikes to be recorded at a high resolution even at amplifications low enough to also record LFPs.

2.4.3 Data Analysis

Recorded data are zero-phase (forward and reverse) refiltered between 300 Hz – 3 kHz prior to offline spike sorting and unit identification using the WaveClus software package [24]. Well-isolated candidate units are analyzed as single-unit data when: (1) all spike events have amplitudes greater than 4 standard deviations above the voltage signal (thresholded based on the signal-to-noise ratio of the individual recording), and (2) the number of spike pairs with an interspike interval below 3 ms (the refractory period) is less than 1% of the total spikes for that unit. Any spikes not clearly separable by these criteria are treated as multiunit data. These conservative spike sorting criteria are designed to minimize how often spikes from separate units are incorrectly combined into single-unit datasets, thus adding reliability to subsequent analyses of spike-mediated information.

The normalized difference is used to quantify the neural response to the stimulation train and is defined by the following equation:

$$ND = \frac{N_{STIM} - N_{POST}}{N_{STIM} + N_{POST}} \tag{2.3}$$

Where N_{STIM} is the number of detected spikes during the stimulation train and N_{POST} is the number of spikes detected for an equal amount of time after the stimulation train. Strong excitatory and inhibitory responses approach values of +1 and -1 respectively, while a value of 0 corresponds to no effect on neural spiking behavior. The Wilcoxon signed-ranked test is then used on all the trials for each programmed micro-coil state to determine the statistical significance of the neural response. P values less than 0.01 are regarded as statistically significant.

2.5 Experimental Results

2.5.1 Micro-Coil State Effect on Neural Response

Testing consists of three trials driving each tested programmable micro-coil state with six trains of fifty 10 Hz ramp waveforms (150 mA peak amplitude, 50% duty cycled, negative ramp polarity) spaced 10 seconds apart. Input referred electrode voltages near the probe prior to digital filtering are shown in Fig. 2.7. Stimulation artifacts are present during recording and are on the order of 100 µV across the entire MEA. Since this study is only analyzing action potentials and the stimulation artifacts are in the frequency domain of LFPs (due to our choice of stimulation waveform), the artifacts are suppressed by a digital high-pass filter.

The stimulation artifacts are caused by electrical coupling from the micro-coil traces and appear mostly as a common-mode signal. This is confirmed during *in vitro* testing as the strength of the stimulation artifacts decrease as the

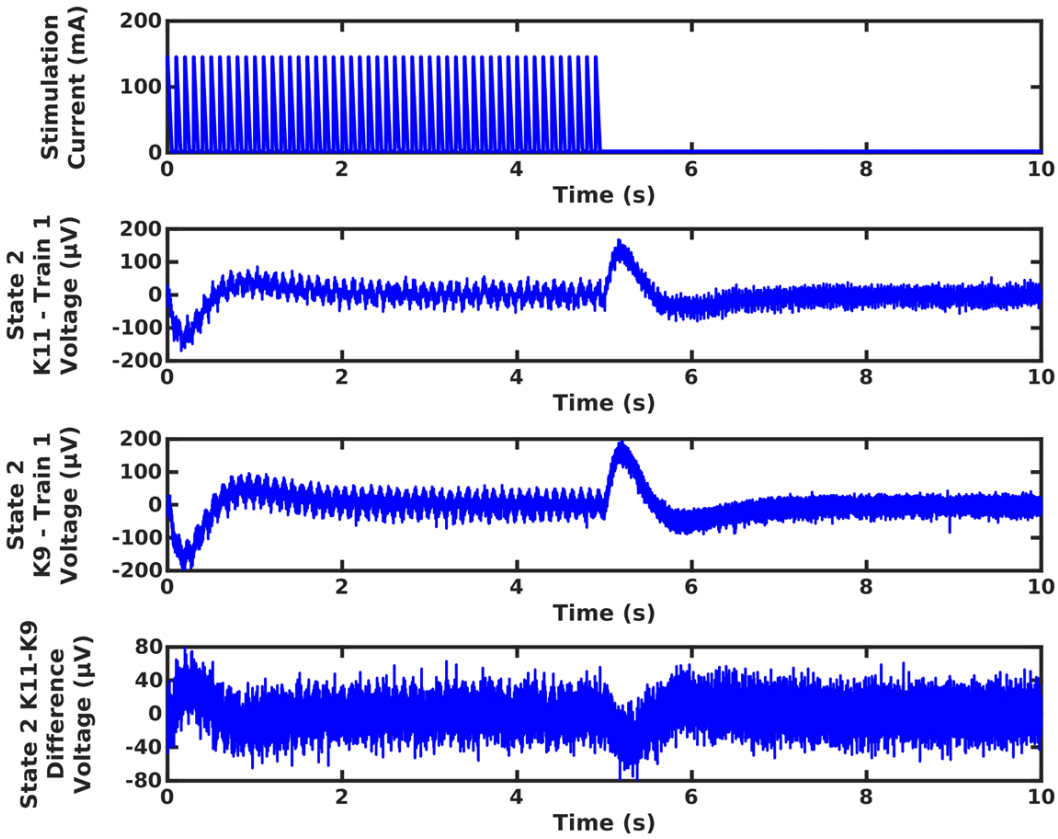

Figure 2.7: Input referred voltages for electrodes K9 and K11 (spaced 400 µm apart) prior to digital bandpass filtering. Bottom row shows the difference between the electrode voltages highlighting that most of the stimulation artifact appears as a common-mode signal.

programmable micro-coil shortens in length, thus decreasing the voltage seen along each micro-coil segment for the same stimulation current. It is possible to use signal processing techniques to remove the mostly common-mode artifact when processing the recorded neural behavior in the LFP frequency band.

Fig. 2.8 shows stimulation aligned recorded data for electrode K11 when the micro-coil is programmed into state 2 (see Fig. 2.9 for state configurations). Note that the filtered electrode waveform contains three unique recorded neurons classified by [24]. However, only the most dominant cluster shows any neural response to the stimulus as the dot plot shows clear inhibition during

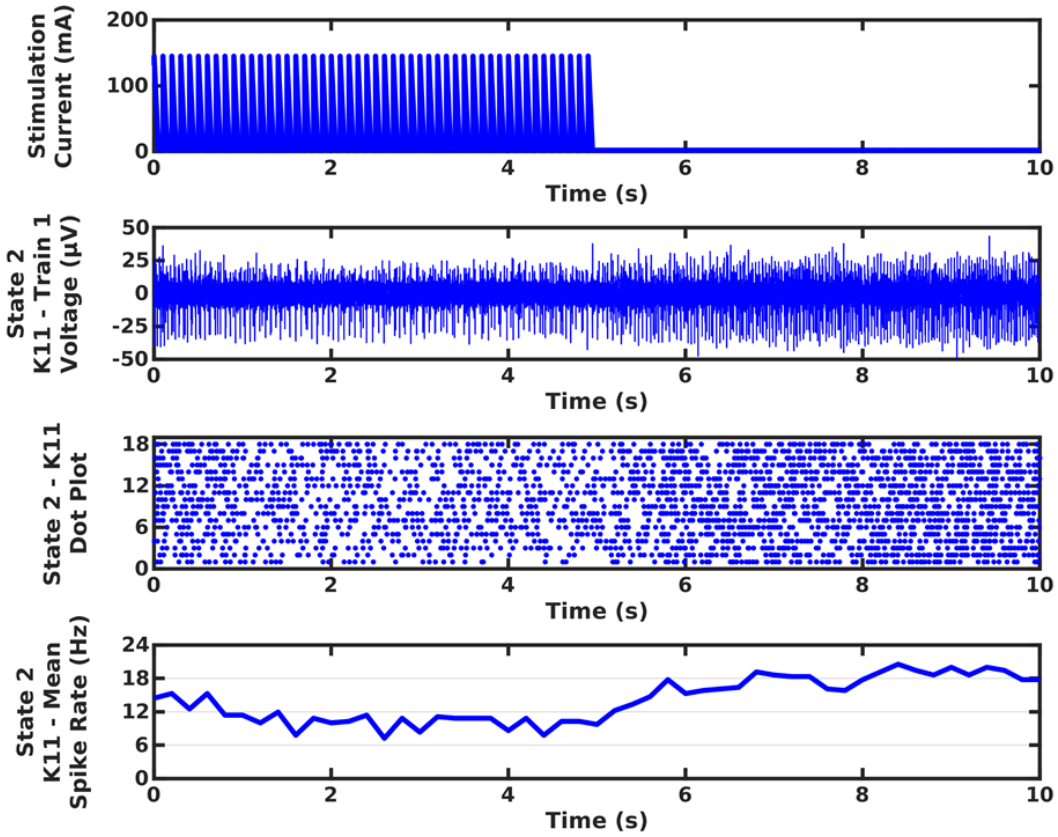

Figure 2.8: Transient measurements of the stimulation current and filtered input referred voltage for electrode K11. Stimulation aligned dot plots are shown for all eighteen stimulation trains as well as an average spike rate over a 200 ms window for the dominant cluster identified by [24]. Two other clusters are identified but show no response to the stimulation train.

the stimulation train. The average firing rate of the cluster increases by a factor of about 1.86 after the completion of the stimulation train.

Fig. 2.9 summarizes the recorded activity observed by electrodes K9 and K11 from all the stimulation trains in each micro-coil state. Electrode locations relative to the probe are shown in Fig. 2.6. The stimulation response for each trial is quantified as the normalized difference and the statistical significance of the response is determined by the Wilcoxon signed-rank test. Electrode K11 shows significant inhibitory modulation when the micro-coil sites close to the

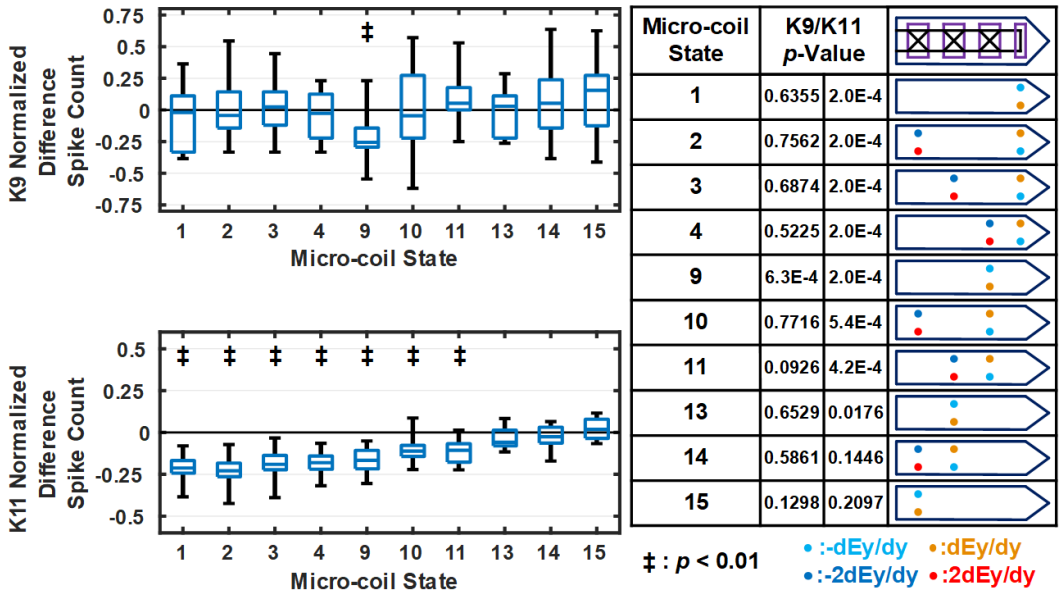

Figure 2.9: Box plots for the normalized difference spike count of electrodes K9 and K11 for all tested micro-coil states. Whiskers extend to the minimum and maximum values. Stimulation sites and p-values for the Wilcoxon signed-rank test are shown for each state.

tip are activated with diminishing inhibitory effects as the stimulation sites retract away from the tip. All statistically significant micro-coil states have a stimulation site located at either the tip of the probe or 250 µm away from the tip.

The neural response observed on electrode K9 shows an inhibitory response to the stimulation train when the micro-coil is programmed to state 9, with no significant response observed when programmed in any of the other tested states. Note that micro-coil state 9 has a unique stimulation site not observed on other tested micro-coil states. All other states with a stimulation site present at the same location as state 9 (250 µm from the tip of the probe) have the polarity of the stimulation sites flipped. All significant neural responses to the stimulation train have an inhibitory response, caused by the preferential activation of bulbar interneurons which deliver widespread lateral inhibition onto mitral/tufted cells observed on the underside of the slice.

2.5.2 Impact of Stimulation Ramp Polarity

Testing on the same slice was also performed with ramp waveforms with a flipped ramp polarity (positive ramp polarity), while leaving the other parameters for the stimulation train unchanged. This flips the polarity of the induced E-field while keeping the thermal and electrical coupling effects consistent with the previously discussed trials. The observed response on electrode K11 is similar for both stimulation waveforms where the strongest inhibitory responses are observed when there are stimulation sites present at the tip of the probe. The inhibitory response is slightly stronger when using the positive ramp waveforms as the normalized difference increases from a value of 0.22 to 0.31 when stimulation sites are present around the tip of the probe.

However, when using the positive ramp stimulation waveform there were no statistically significant observed responses on electrode K9. Comparisons between the stimulation ramp polarities for micro-coil state 9 is shown in Fig. 2.10. The dot plot shows a large variation in neural behavior for stimulation trains 1 – 18 (positive ramp) while there is consistent inhibitory behavior for stimulation trains 19 – 36 (negative ramp) as spiking activity increases post-stimulation. This increase in post-stimulation spiking can also be seen in the bar graph and spike binning plots and contributes to the negative ramp dataset having a negative normalized difference with a median value of -0.25. Meanwhile, the positive ramp dataset shows a larger variance centered around a median normalized difference value of zero.

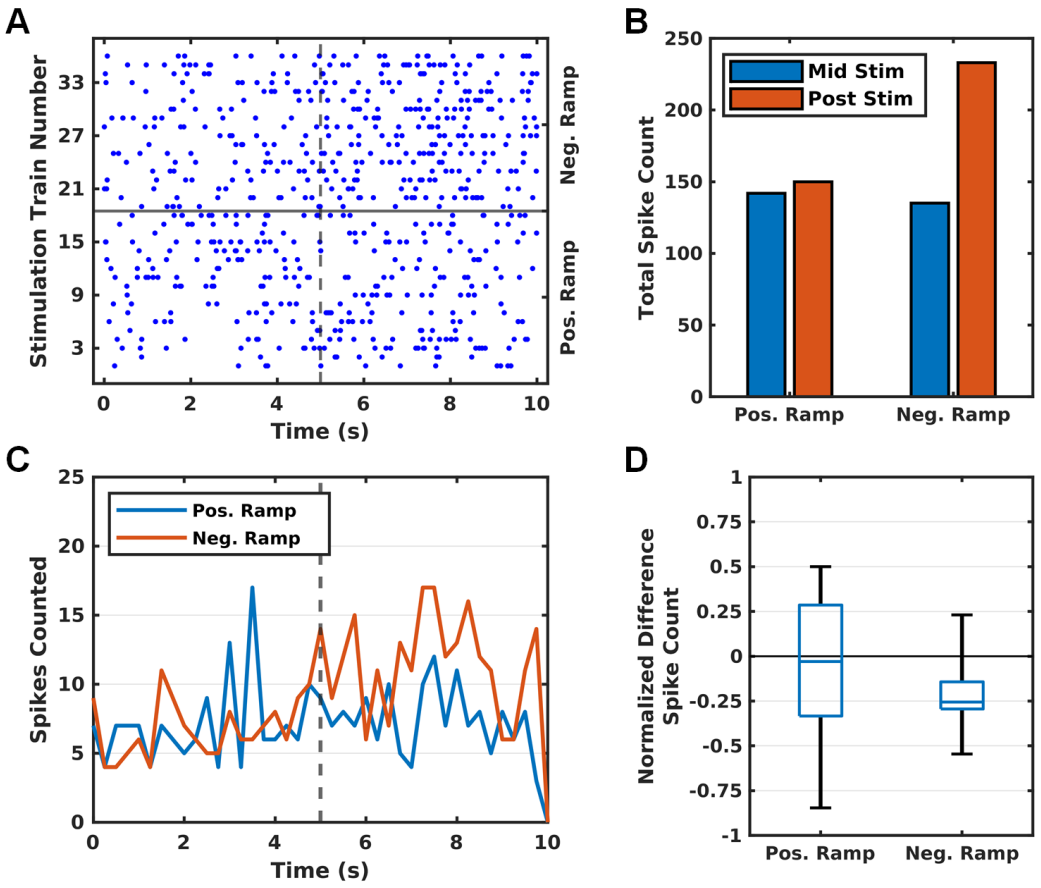

Figure 2.10: Comparison between micro-coil state 9 neural responses to positive and negative ramp waveform stimulation trains. (A) Stimulus aligned dot plot. (B) Total spike count during and after stimulation. (C) Spikes counted over a 250 ms window. (D) Normalized difference box plot.

2.5.3 Spatial Extent of Neural Response

To analyze the spatial extent of the neural response across the entire electrode array the mean of the normalized difference for all detected clusters is calculated for the negative ramp polarity waveform trials. Only electrodes that recorded a minimum of 500 total spikes across each of the three trials are analyzed. This prevents electrodes that did not record significant neural activity from creating insignificant data. The results are shown in Fig. 2.11 for micro-coil states with zero switching networks programmed in the 'cross' state to limit the stimulation

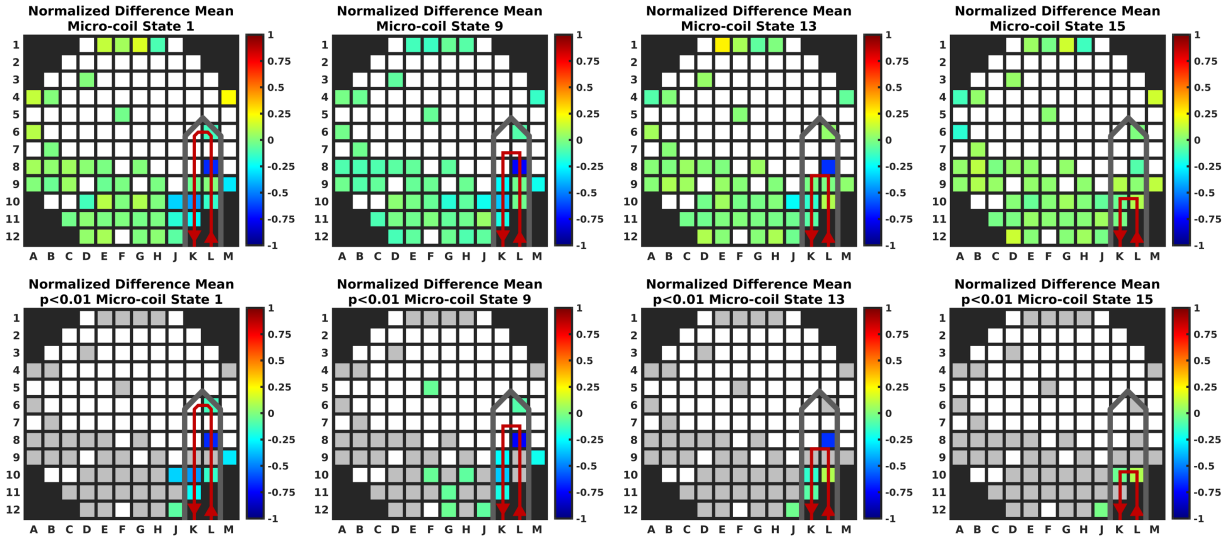

Figure 2.11: Mean normalized difference for all detected clusters plotted across the MEA for non-crossing micro-coil states. The neural probe location and programmed micro-coil current flow are shown over the array (width not to scale). Top row shows data for all electrodes that have a minimum of 500 detected spikes for all three trials. Bottom row shows data for electrodes where the normalized difference is statistically significant with a p-value less than 0.01 from the zero-median Wilcoxon signed rank test.

site to the end of the current flow through the programmable micro-coil.

The strongest inhibitory responses are located near the location of the probe. As the bend of the micro-coil current retracts further away from the tip of the probe, the measured inhibitory effects also retract along the array. Furthermore, the measured normalized difference also weakens as the stimulation sites retract from the tip. This can be seen as micro-coil state 1 has the strongest inhibitory effects located in the bottom right corner of the MEA while micro-coil state 15 shows limited neural response.

Since the data plotted across the array is the mean of the normalized difference it is possible that some of the effects observed across the array are affected by statistical outliers during the trials. Therefore, the bottom row of Fig. 2.11

grays out all data that does not meet the statistical significance criteria for the Wilcoxon signed-rank test. The majority of the of the statistically significant electrode sites are located around the bottom right corner of the MEA near the probe. Micro-coil state 9 (250 µm from the tip of the probe) shows the most widespread inhibition across the array, with the inhibitory effect is weaker than what is observed near the probe. This is the only programmed micro-coil state that shows statistically significant inhibitory responses on electrode locations away from the location of the probe.

2.5.4 Stimulation Current Threshold

Experiments were also done to observe the neural response across varying strengths of the stimulation waveform, using a slice from a different olfactory bulb than previously discussed experiments. The tip of the probe was placed over electrode E4 as it was the region of the slice showing the most neural activity. The stimulation current increased up to 200 mA in 20 mA increments. Fig. 2.12 shows stimulation-aligned recorded waveforms for electrode E5 for current amplitudes of 160, 180, and 200 mA to explore the neural network dynamics. There are two different neurons recorded on electrode E5: one with an amplitude up to 200 µV (cluster 1) and another with an amplitude under 100 µV (cluster 2).

As the stimulation current increases, the time for the inhibitory effect to begin decreases (180 mA, 2.05 s; 200 mA, 0.65 s). Furthermore, as the stimulation current increases the measured amplitudes of the recorded spikes decreases. This decrease in the action potential amplitude can be attributed to shunting in-

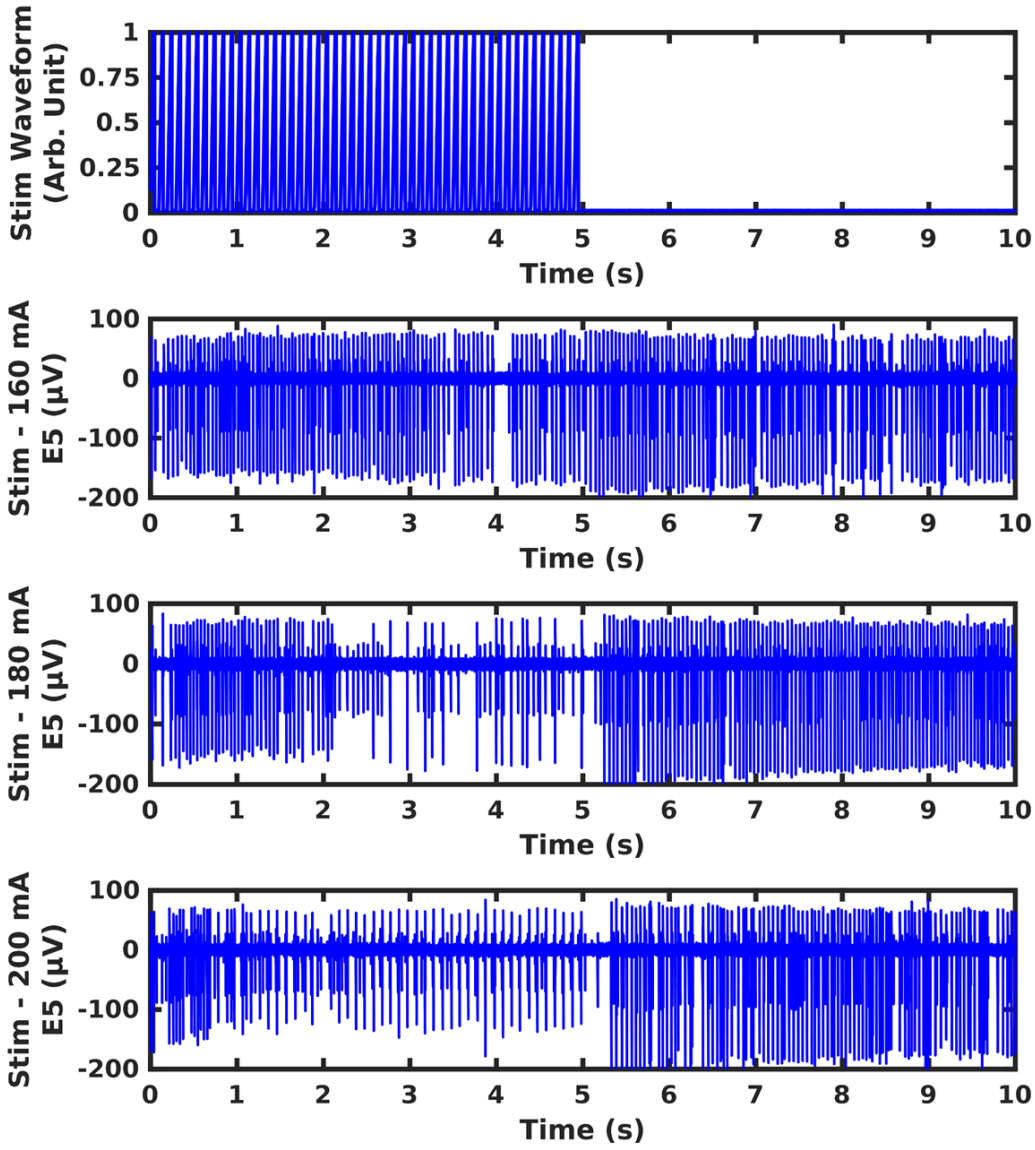

Figure 2.12: Stimulation aligned voltage waveforms of the measured electrode E5 response to the stimulation train for current amplitudes of 160, 180, and 200 mA.

hibition, caused by the activation of interneurons, causing a reduction in extracellular currents measured by the recording electrodes in the MEA [20,114,134].

Fig. 2.13 shows the mean normalized difference over three trials for electrode E5 across the tested stimulation current range for both recorded clusters. Micro-coil state 1 (current flow down to the tip of the probe) shows no large

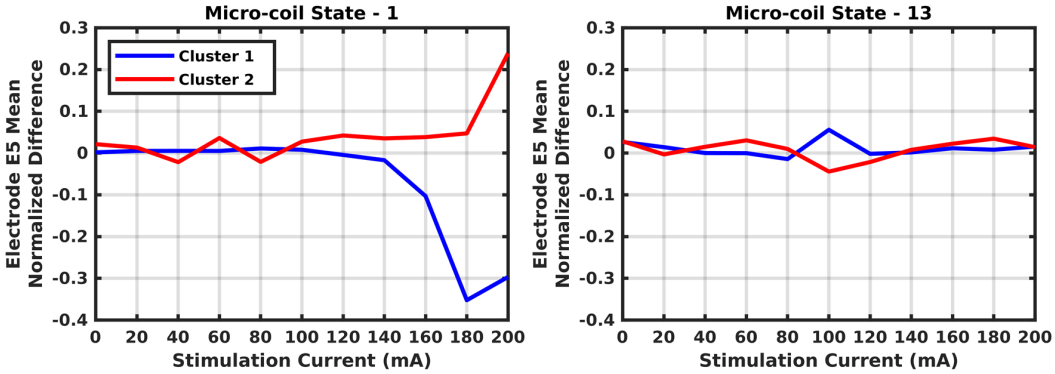

Figure 2.13: Mean normalized difference for electrode E5 plotted across the current amplitude over three trials for micro-coil states 1 and 13 (current flow through to the tip and through to 500 µA from the tip).

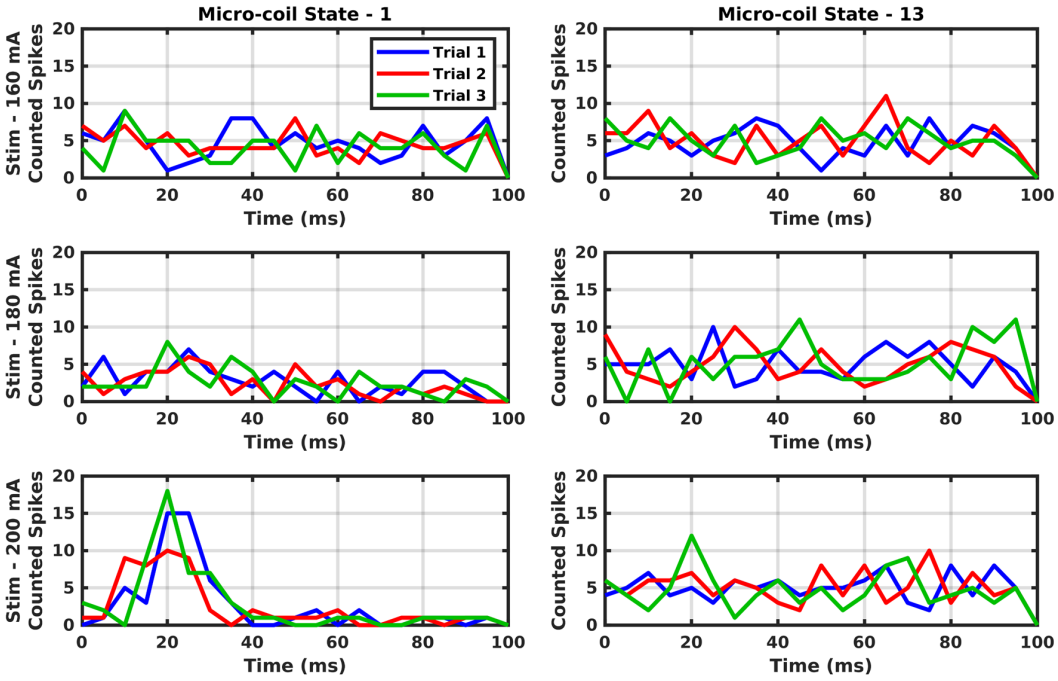

Figure 2.14: Spike counted in 5 ms windows for each of the three trials for micro-coil states 1 and 13. Stimulation current values shown are 160, 180, and 200 mA.

neural response for current amplitudes up to 160 mA. At 180 mA there is a significant increase in the inhibitory response for cluster 1, suggesting that the inhibitory response has a binary response with an activation threshold. When the stimulation current is increased to 200 mA there is an increase in the normalized difference for both clusters (due to lack of activity after the stimulation

train). Micro-coil state 13 (current flow down to 500 µm from the tip of the probe) shows no neural response to any of the stimulation amplitudes.

Cluster 1 also fires consistently with each stimulation ramp waveform with a 200 mA stimulation current. Stimulus-aligned bins are created to count each recorded action potential for each waveform in the train. Fig. 2.14 shows the results for both micro-coil states 1 and 13, and stimulation currents 160, 180, and 200 mA for all three trials. Bin windows are set to 5 ms and are aligned to the steep gradient in the ramp waveform. For micro-coil state 1 at 200 mA there is clear synchronized spiking occurring around 20 ms after each ramp waveform.

2.6 Discussion

2.6.1 Stimulation Current Comparisons

The stimulation currents for the proposed programmable micro-coil neural probe are approximately an order of magnitude larger than those used in *in vitro* studies from previously designed micro-coil-based neural probes [76, 77]. However, there are several differences in the experiment set up that have a significant effect on the necessary stimulation current. While the tissue slices used also have a thickness of 300 µm, the slice was a V1 coronal slice from a Thy1-GCaMP6f transgenic mouse, allowing for fluorescent imaging of the direct neural response on the top side of the tissue slice. It is plausible that there was evoked neural activity from the programmable micro-magnetic stimulation at lower amplitudes, but the effect was not strong enough to propagate to the bottom of the slice.

Furthermore, the fluorescent imaging experiments placed the stimulation sites of the probes directly over the proximal axon of the targeted neuron as it has the highest sensitivity to stimulation [38,58,128,141]. Additionally, the used stimulation waveform was a single period of a sinusoidal current as opposed to a ramp waveform. This causes the induced E-field to have a tri-phasic waveform, where the duration of the second phase is longer than the first and last phase, which is thought to reduce the threshold needed for activation [110,121] It is feasible that the necessary stimulation current of the proposed neural probe will decrease by changing the *in vitro* experimental setup to use transgenic mouse slices to measure the direct stimulation response on the top of the slice, as well as using better probe positioning and stimulation waveform optimization.

Finally, it is also possible to modify the design of the proposed programmable micro-coil neural probe to include recording electrodes and integrated neural amplifiers to measure changes in the neural behavior at the surface of the probe. Electromagnetic simulations with electrodes above the stimulation sites show no degradation in the magnitudes of the induced E-fields. Using the measured stimulation artifacts 300 µm away from the surface of the probe, the expected stimulation artifacts measured by electrodes on the probe are on the order 100 mV. Modern neural recording front ends are capable of recording neural signals in the presence of differential artifacts as large as 200-mV_{pp} and common-mode artifacts as large as 700-mV_{pp} without distortion [22, 23, 62]. The nanofabrication release processing can be modified to deposit platinum recording electrodes while also using a thinner insulation layer that does not suffer from water infiltration around the electrode openings [82–84].

2.6.2 Stimulation Current and Heat Reduction

Measurements need to be done to observe the temperature changes in the aCSF bath or tissue near the probe. Temperature measurements from similar micro-coil based neural probes suggests that it is unlikely to observe more than a 1°C change in temperature during stimulation [77,119], which is less than the threshold for thermal activation of neurons [27, 34, 37]. The increase in temperature during stimulation can be reduced more by lowering the stimulation current as joule heating is proportional to I^2R.

While changing the experimental setup could decrease the necessary stimulation current to observe evoked neural behavior, it is also possible to improve the hardware design of the proposed programmable micro-coil. The derived expression for the induced E-field shows that the magnitude is proportional to the number of turns in the micro-coil. This has been verified by fabricated multi-turn single layer micro-coils as well as electromagnetic simulations for multi-layer micro-coils [76]. While there are concerns about the design and fabrication of a multi-layer micro-coil using the process discussed in [76, 77], this is mitigated when co-designing the micro-coil with CMOS technology. Furthermore, since the nonlinear switch resistance dominates the coil impedance, turns can be added to the micro-coil design without a significant increase in the coil resistance.

2.6.3 Future Control Experiments

The discussed data shows clear signs of recorded neuromodulation from the programmable micro-magnetic stimulation. However, control experiments are

needed to completely isolate other forms of neuromodulation. Previous micro-coils ensured the integrity of the coil insulation by regularly measuring the coil impedance to ground to ensure there was under 10 µA of leakage current [76–78, 119]. The thicker encapsulation layer used (1 µm of oxide from the CMOS chip, 4 µm of parylene C) should ensure that the impedance of the programmable micro-coil is greater than 250 MΩ (and thus a leakage current under 10 µA). However, since the proposed probe is implemented with active circuitry, a different approach is needed to measure the leakage current. This can be confirmed by measuring the current flowing in and out of the programmable micro-coil and comparing the difference.

It has been previously discussed that the heat produced by the programmable micro-coil is unlikely to exceed the threshold for thermal activation of neurons. Similar *in vitro* experiments presented in this work can be performed where the steep gradients in the stimulation current waveform are removed. This allows for similar joule heating while eliminating strong gradients in the induced E-field. Finally, it has been shown that capacitive currents transmitted through insulation layers can effectively evoke neuronal activation [36]. This can be tested by running the coil in an open-circuit configuration and applying a voltage across the programmable coil terminals.

2.7 Conclusion

This work proposes a neural probe that co-designs micro-coils, CMOS technology, and nanofabrication techniques to enable spatially programmable micro-coil magnetic neurostimulation sites. The programmable micro-coil is imple-

mented using programmable switching networks to allow the micro-coil current path to change along the probe, changing the locations of the gradients of the induced electric fields, thus changing the locations of the neurostimulation sites. Nanofabrication techniques are used to thin down and release the probes from the original foundry chip packaging. *In vitro* testing of the neural probe was done with slices of a mouse olfactory bulb in conjunction with an MEA yielding observable changes in neural behavior to given stimulus patterns under specific programmable micro-coil states. The observed neural response to the stimulus was an inhibitory response mostly localized around the location of the probe.

CHAPTER 3

CMOS MICRO-MAGNETIC NEUROSTIMULATOR UTILIZING OPTIMIZED MULTI-TURN MICRO-COILS

3.1 Introduction

Electrical stimulation delivered through implantable electrodes has allowed for the development of neural prostheses to restore sensory and motor functionality [3, 12, 105, 123]. However, there are fundamental limitations with electrical stimulation using implantable electrodes that limit this approach. The first limitation is the produced electric fields are spatially symmetric, which prevent specific neurons from being targeted, limiting the effective stimulation spatial resolution [10,50,140]. This arises from the produced electric fields from monopolar electrodes (distant return electrode) being spatially symmetric as well as the high sensitivity passing axons have to prosthetic stimulation [115]. Efforts to enhance the stimulation spatial resolution utilizing multiple electrodes (bipolar drive or hexagonal configurations) have reported marginal improvement, but require more complicated electrode structure and driving circuitry [18,146]. The next limitation arises from concerns over the long-term viability of microelectrodes as the stimulation effectiveness degrades over time. One of the causes for this is from the formation of glial scarring around the electrodes [42, 112], which can lead to complete encapsulation around the electrode and limit their stimulation effectiveness over time. While it is possible to increase the stimulation current to re-elicit neural behavioral responses, the increased tissue impedance from the glial scarring seen by the electrode reduces the available headroom for the electrode driver circuitry, potentially preventing the hardware

from producing sufficient current to elicit neural responses [26,104,139]. The final discussed limitation of electrodes is the electrode-tissue interface is prone to electrochemical effects (such as hydrolysis and corrosion) that can damage the electrode and/or surrounding tissue if charge transfer levels per phase are too high [30,91].

Magnetic stimulation through implantable micro-coils overcomes the addressed limitations of implantable electrodes. The induced electric fields from magnetic stimulation are spatially asymmetric and can avoid the activation of passing axons, confining the effective stimulation region [15,76,77]. Furthermore, magnetic fields have a high permeability to biological tissue and biocompatible materials. Therefore, the micro-coil-based stimulation efficacy is not weakened by glial scarring and can be completely encapsulated in biocompatible materials that mitigate the implantation response [21,53,122]. This is in contrast to the implantable electrodes that require openings in the encapsulation and suffer from water infiltration through weak bonding between the exposed electrode and encapsulation material [80,81]. Recent developments in implantable micro-coil technology have produced devices capable of modulating neural behavior in *in vitro* and *in vivo* experiments. However, these devices lack reconfigurable hardware that is more commonly seen in implantable microelectrode systems, thus fixing the stimulation sites after implantation [41,66].

Recent work has utilized CMOS technology in the micro-coil design with additional nanofabrication processing to develop a neural probe capable of spatially programmable micro-coil magnetic stimulation [130]. However, that work did not use multi-turn micro-coil designs to decrease the necessary stimulation current. Furthermore, the design was one long programmable micro-coil that

required very large switches in order to keep the micro-coil voltage below the transistor breakdown voltage during stimulation. This, in turn, reduces the current density flowing through the switches, thus reducing the maximum induced electric field. The proposed neural probe co-optimizes the micro-coil design with integrated CMOS current drivers to provide spatially programmable neurostimulation sites from multi-turn, independently driven micro-coils. Furthermore, a four-wire interface is implemented to use the current inputs and supply as the programming interface. This reduces the number of necessary terminals needed to connect the neural probe to external circuitry, reducing the packaging size.

3.2 Electromagnetic Simulations

3.2.1 Electromagnetic Modeling

Stimulating neural tissue requires a sufficient gradient in the electric field to be produced along the axon of a neuron to generate local membrane depolarization. The electromagnetic derivation for the induced electric fields produced by the current flowing through the micro-coil can be found in [77]. The proposed design utilizes an array of independently driven multi-turn micro-coils to change the location of the electric field gradients, while reducing the necessary stimulation current. Electromagnetic simulations are performed using the Magnetic and Electric Field (mef) module within COMSOL Multiphysics to predict the location and strengths of the local E-field gradients. Finite element method (FEM) simulations are performed to calculate the spatial gradients of

the induced E-fields arising from the current flow through the micro-coils under different conditions. Fig. 3.1 shows the model consisting of two multi-turn, multi-layer micro-coils (four layers, four turns per layer) over a conductive silicon substrate etched in the shape of a probe. Simulations are performed with the micro-coils driven under the following conditions: one coil is driven clockwise, both coils are driven in the same direction (clockwise), both coils are driven in opposite directions (Fig. 3.1B-D). The aluminum micro-coil traces have a cross-sectional dimension of 4.07×0.5 µm with a wire spacing of 1 µm and layer spacing of 0.85 µm. The silicon substrate has a cross-sectional dimension of 60×110 µm and a length of 715 µm, with the last 45 µm tapering to a point. The dimensions of the probe results in a cross-sectional area comparable to microfabricated intracortical electrodes that are routinely implanted without causing significant damage to the neural tissue [69, 136].

The simulation environment models the neural probe surrounded in a 1 mm^3 medium with the properties of gray matter (electrical conductivity: σ = 0.27 S/m; relative permittivity: ϵ_r = 12,000) [137], similar to previously used environments to allow for direct comparisons to prior studies [76, 130]. The environment was split with a finer mesh with the micro-coils simulated in a closed-loop configuration. The micro-coil input terminals are sufficiently distanced from the micro-coil turns such that they do not affect the simulated E-field gradients. The stimulation currents driven through the micro-coils are 5-kHz, 10-mA sinusoidal waveforms with their current directions defined in Fig. 3.1B-D. The induced E-fields and their spatial gradients are calculated within COMSOL Multiphysics along a plane 20 µm above the surface of the probe, selected based off the typical cell body size for mitral cells and the expected probe encapsulation thickness [99].

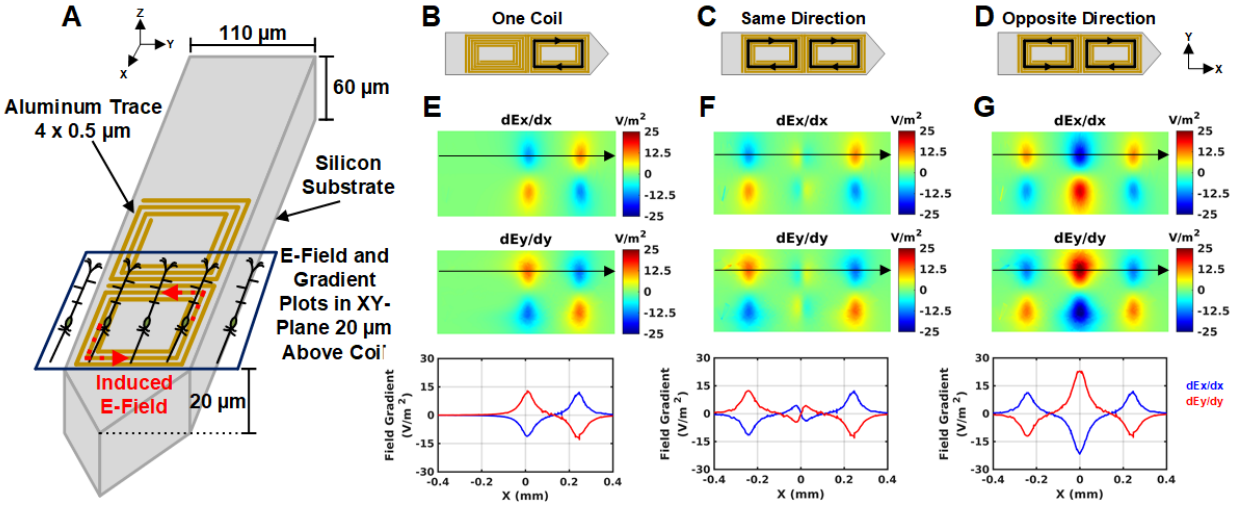

Figure 3.1: Electromagnetic simulations for a neural probe with two multi-turn micro-coils under various current direction configurations. (A) Conceptual diagram for micro-coil based magnetic stimulation with the induced electric field direction shown for the bottom micro-coil current driven clockwise. (B) Neural probe with one micro-coil driven clockwise. Black lines show the current flow throughout the micro-coil used in the simulations. (C) Both micro-coils driven clockwise. (D) Micro-coils driven in opposite directions. (E-G) Spatial gradients of the electric field along the x- and y-axes for the configurations used in B-D. Line plots show the field gradients along the x-axis over the upper stimulation sites.

3.2.2 Simulation Results

The strongest field gradients are located above the locations where the current flow is changing directions where the positive peaks for the dEx/dx gradients are located where the negative peaks for the dEy/dy gradients are located (and vice-versa), consistent with previous studies [76–78,130]. When only one micro-coil is driven the stimulation sites appear over opposite corners of the micro-coil. The maximum gradient values for dEx/dx and dEy/dy are 12.13 and 12.89 V/m^2 respectively. There are no induced E-fields produced over the adjacent micro-coil since there is no current flowing through the coil. When both micro-coils are driven with the same stimulation current, flowing in the same direc-

tion, the stimulation sites move to the outer corners of the two micro-coils. The simulation results are similar to the one micro-coil case, with the maximum gradient values for dEx/dx and dEy/dy are 12.19 and 12.34 V/m^2 respectively. There is also a smaller set of unintentional E-field gradients located between the micro-coils where the maximum gradient values for dEx/dx and dEy/dy are 4.38 and 4.32 V/m^2 respectively. These gradients are produced by the magnetic fields from the two micro-coils not completely cancelling out at their contiguous boundary.

When the micro-coils currents are flowing in opposite directions the strongest gradients appear between the two micro-coils. The maximum gradient values for dEx/dx and dEy/dy are 21.24 and 23.93 V/m^2 respectively, nearly doubling the maximum gradients from the previously micro-coil configurations. This increased gradient strength is caused by the current flow along the x-axis flipping directions, while the current flow along the y-axis is doubling. In each of the micro-coil configurations there are gradients along the z-axis present along the side of the silicon substrate that is approximately four times weaker than the strongest dEx/dx or dEy/dy gradients. However, with proper selection of the stimulation current value, the dEz/dz gradients can be kept below the stimulation threshold while maintaining the dEx/dx and dEy/dy gradients above the threshold, maintaining neuron orientation selectivity.

The simulation results suggest that a neural probe utilizing multiple multi-turn micro-coils can produce the maximum E-field gradients by driving adjacent micro-coils in opposite directions, producing programmable neurostimulation sites located between adjacent micro-coils. This suggests that the proposed probe is capable of targeting different neuron regions, such as individual layers

of the neocortex. These results show that maximum E-field gradients are similar to the maximum E-field gradients produced by neural probe utilizing a programmable micro-coil (maximum gradients for dEx/dx and dEy/dy values of 21.81 and 25.77 V/m^2 respectively) [130]. This work used a 5kHz 150 mA stimulation current for the electromagnetic simulations, suggesting that the proposed multi-turn micro-coil neural probe is capable of invoking neural activity while reducing the necessary stimulation current by a factor of 7.5. Finally, additional simulations modeling metal-insulation-metal (MIM) capacitors over the stimulation sites show negligible difference in the strength of the E-field gradients. This suggests that a micro-coil based neural probe can be designed while also recording nearby neural activity with electrodes integrated on the top plate of the MIM capacitors [60, 82, 83].

3.3 Neural Probe Design

3.3.1 System Overview

The proposed neural probe system is shown in Fig. 3.2. The backend circuitry of the probe contains a four-wire interface to allow the supply and differential coil input terminals to double as the programming interface. The programming interface controls the state of the ternary (non-inverting, inverting, or off) push-pull current drivers to control which of a set of four separate micro-coils are active and the direction the current flows through them. This is implemented by passing both input current signals into a push-pull driver with eight parallel outputs, producing eight differential current pairs. Each output is cross-

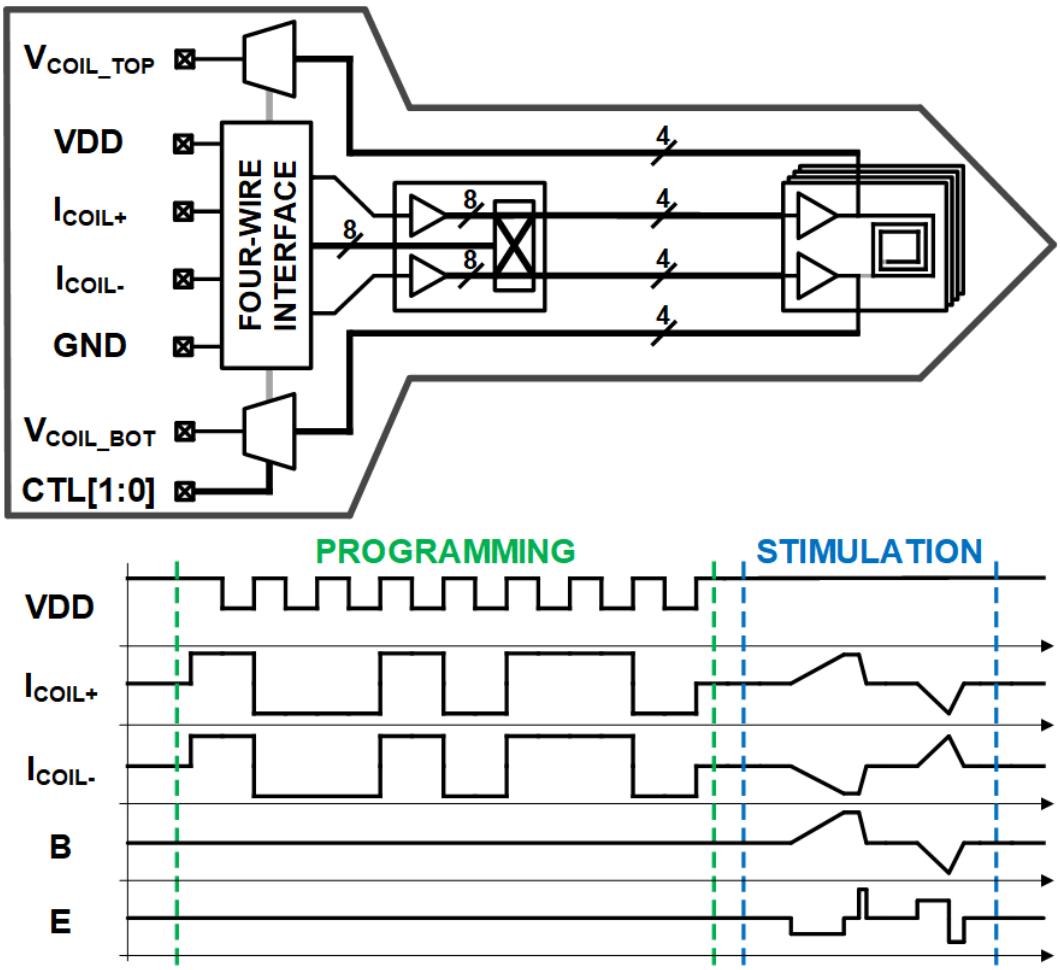

Figure 3.2: System architecture of the proposed neural probe. Waveform plot shows an example of the supply and differential coil input signals during programming and stimulation, as well as the expected magnetic field and induced electric field.

connected to its opposite-sign counterpart and routed down the probe to its dedicated micro-coil driver, with one such dedicated driver per micro-coil. Current flow through the current drivers and switch network for each ternary driver configuration can be seen in Fig. 3.3. When one driver output is active the cross-connected output is disabled. The micro-coils and their drivers are located near the tip of the probe, with the micro-coil terminals multiplexed off chip to characterize the maximum stimulation current.

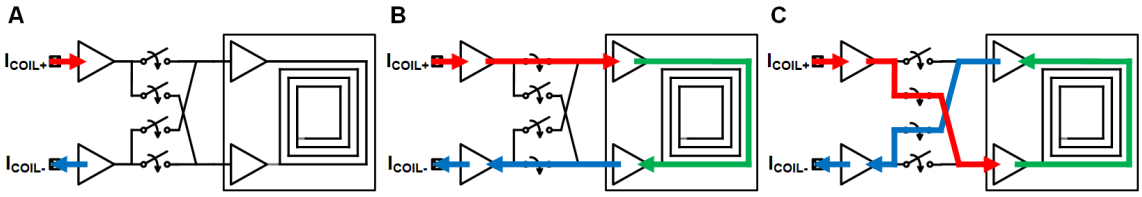

Figure 3.3: Conceptual diagram of programmable ternary driver configurations to drive the micro-coil drivers. Red and blue arrows show the push and pull current flow for the positive and negative terminal ternary drivers respectively. Green arrows show the current flow through the micro-coil. (A) Micro-coil driver disabled. (B) Micro-coil driver non-inverting configuration. (C) Micro-coil driver inverting configuration.

Since it is not necessary to program the neural probe during stimulation, programming signals can be multiplexed with the power supply and differential stimulation current to use only four terminals. This decreases the number of necessary pads, thus decreasing the backend area and increasing the possible length of the insertable shank. During programming the supply cyclically drops beneath a threshold voltage, set by a PTAT driving a diode stack, to generate the programming clock. The common mode of the differential coil inputs serves as the programming data. This, in turn, moves the common mode of the micro-coils during programming; however, there is no current flowing through the micro-coils, and therefore there are no induced electric fields and no inadvertent stimulation during programming.

3.3.2 Circuit Design

Four-Wire Interface

The circuit implementation of the four-wire interface and push-pull current drivers is shown in Fig. 3.4. The supply of the four-wire interface powers a

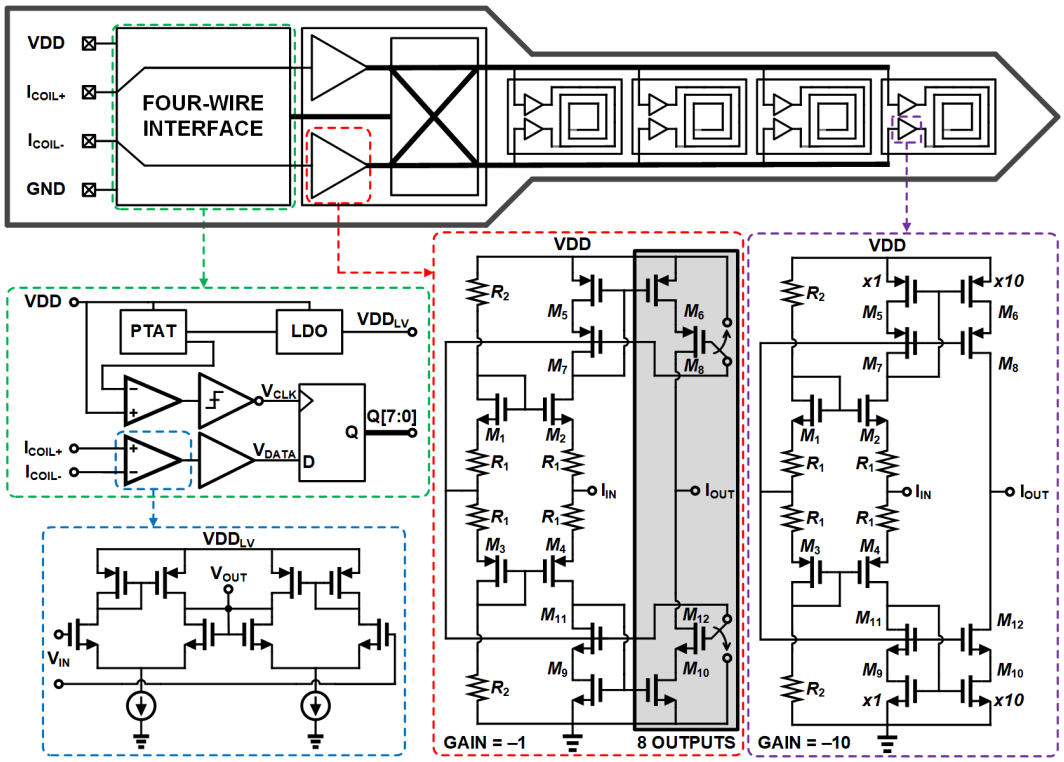

Figure 3.4: Circuit implementation of the four-wire interface, ternary current drivers, and micro-coil drivers.

PTAT (implemented with startup circuitry to ensure proper operation) to generate bias currents for amplifiers, current starved logic, and bias voltages. A low-dropout regulator produces a constant supply voltage for the digital circuitry. The clock is generated by comparing VDD to a bias voltage and is buffered by an inverting Schmitt trigger to prevent local drops in the digital supply voltage from generating multiple clock edges. The differential coil inputs are buffered by a pair of high output impedance differential pair amplifiers connected in unity gain feedback, with the common mode extracted by connecting the outputs of the amplifiers together. The programming bits are stored in a current starved shift register and are level shifted back to VDD to control the ternary push-pull drivers.

Push-Pull Current Driver

The ternary current drivers and micro-coil drivers use the same push-pull topology, selected for its bidirectional current flow that allows for easy change in current direction through the micro-coil without the need for large switches. Resistors R_1 trade-off between the input current range and the quiescent bias current. Given a specified maximum input current and assuming all transistors are sized to have the same overdrive voltages R_1 can be solved for from the following equation:

$$VDD = 4V_{OD} + V_{TH} + I_{IN}R_1 \tag{3.1}$$

In the case where current is flowing into the node I_{IN} of the micro-coil driver, V_{TH} and $2V_{OD}$ arise from the devices M_9, M_4, with the remaining $2V_{OD}$ coming from the cascode output stage of the ternary current driver. Assuming a supply voltage of 3.5 V, a threshold voltage of 700 mV, and overdrive voltage of 300 mV, R_1 is selected to be 500 Ω to allow an input current range of ±3.2 mA. This is selected to ensure that the maximum output current of the micro-coil driver is limited by the output stage across all process corners.

Reducing the value of R_1 does not drastically increase the quiescent current consumption of the current driver with the inclusion of transistor pairs M_1, M_2 and M_3, M_4 operating in class AB. The bias current of the push-pull driver is set by the component stack containing $2R_1$, $2R_2$, and diode connected FETs M_1 and M_3. Applying Kirchhoff's voltage law yields the following expression for the bias current I_B:

$$VDD = 2I_B[R_1 + R_2] + \eta_1 V_T \ln\left(\frac{I_B}{I_{S1}}\right) + \eta_3 V_T \ln\left(\frac{I_B}{I_{S3}}\right) + 2V_{TH} \tag{3.2}$$

Where $\eta_{1,3}$ and $I_{S1,3}$ are device parameters for M_1 and M_3 operating in sub-threshold. The value of R_1 is already selected to set the maximum input current range, leaving the only free parameters to set the bias current as R_2 and the size of the M_1 and M_3. Through simulations the bias current is set to 40 µA with the sizes of M_1 and M_3 set to 60 µm/350 nm and 90 µm/350 nm respectively, and the value of R_2 set to 12 kΩ.

The output of the current driver is the parallel outputs of cascoded PFET and NFET current mirrors. Cascoded outputs are used to ensure accurate current mirroring over the wide range of coil voltages present during stimulation. The ternary driver outputs can be disabled by switching the PFET and NFET cascode gate voltages to supply and ground respectively. The output devices are sized such that the ternary current drivers have unity current gain and the micro-coil drivers have a current gain of ten.

Stimulation Artifact Amplifier

An iteration of the micro-coil based neural probe is designed with electrodes placed over the programmable stimulation sites to observe neural activity near the surface of the probe. There are three possible effects that can create stimulation artifacts on the input of a neural amplifier: electrical coupling from the voltage present across the coil, magnetic coupling from the current flowing through the coil, and induced currents from the magnetic stimulation detected by the electrodes. Due to the uncertainty of the stimulation artifact mechanisms,

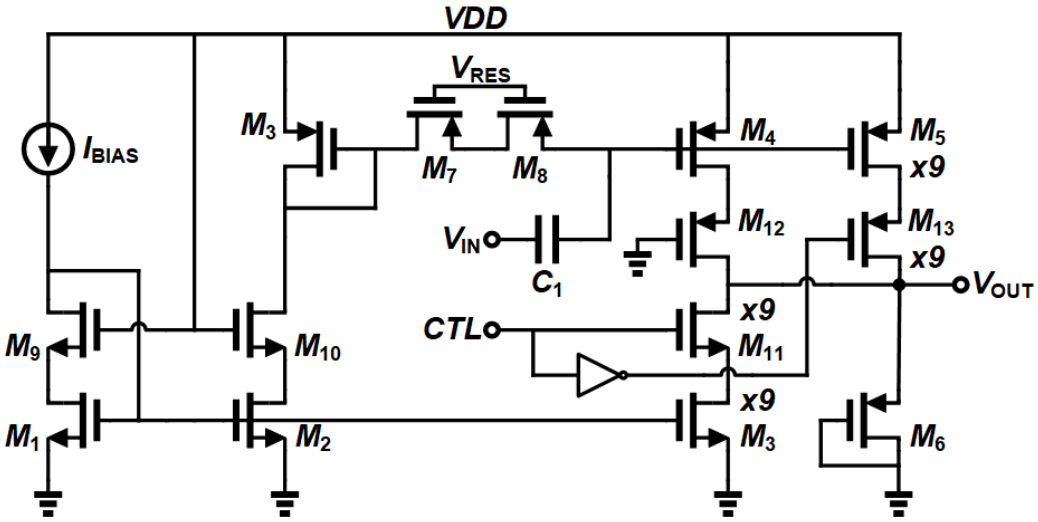

Figure 3.5: Schematic of the stimulation artifact amplifier.

the amplifiers are designed to prioritize artifact characterization from micro-coil based magnetic neurostimulation.

The circuit schematic for the stimulation artifact amplifier is shown in Fig. 3.5. The amplifier topology is a single ended design, which is chosen to prioritize stimulation artifact measurements across the electrode locations. The electrode signal is AC-coupled through capacitor C_1 to the gates of transistors M_4 and M_5. The high pass filter corner frequency is set by C_1 and the pseudo-resistor made up from transistors M_7, M_8. The corner frequency of the high pass filter is set by adjusting the gate voltage, which is brought externally through a pad on the backend of the probe.

Accurate amplifier gain is set by using a diode connected load, so the gain is set by the sizing ratio between the input devices and the load. This allows for accurate characterization of the stimulation artifact along the probe across process corners. The programmable gain is controlled by the input signal CTL. When high M_{11} and M_{13} are turned on setting the transconductance of the am-

plifier to $10g_m$ and the load $1/g_m$. When CTL is low M_{11} and M_{13} are turned off and the amplifier is set to unity gain.

The dominant noise sources come from the thermal noise from the pseudo-resistor, the flicker noise from the largest NFET transistors (M_1 and M_3), and the flicker noise of the input bias current (NFET transistors in the PTAT). Simulations show that when the amplifier gain is set to ten the input referred noise is 30 µVrms for a bandwidth of 100 Hz - 10 kHz. While this high noise floor is not ideal for neural amplifiers, this is sufficient for characterizing stimulation artifacts that could impose linearity constraints on neural amplifiers while simultaneously recording large action potentials. The single ended topology is prone to changes in the supply voltage during stimulation, which can be problematic as the stimulation artifact amplifier and micro-coil current drivers are both connected to the same supply. To reduce stimulation supply coupling the traces are routed down the probe separately and are only connected at the back-end of the probe where the resistance of the supply traces is insignificant.

3.3.3 Coil Optimization

The micro-coil design and push-pull amplifiers are co-designed to maximize the produced magnetic field. The maximum field is proportional to the total turns in the micro-coil and to the maximum current that can flow through the coil. Fig. 3.6 shows that the supply traces are routed long distances to the micro-coil drivers. Due to the parasitic resistance from the supply traces, it is advantageous to increase the number of turns per layer in the micro-coil, reducing the current for a given voltage across the coil, and lowering the voltage drop across

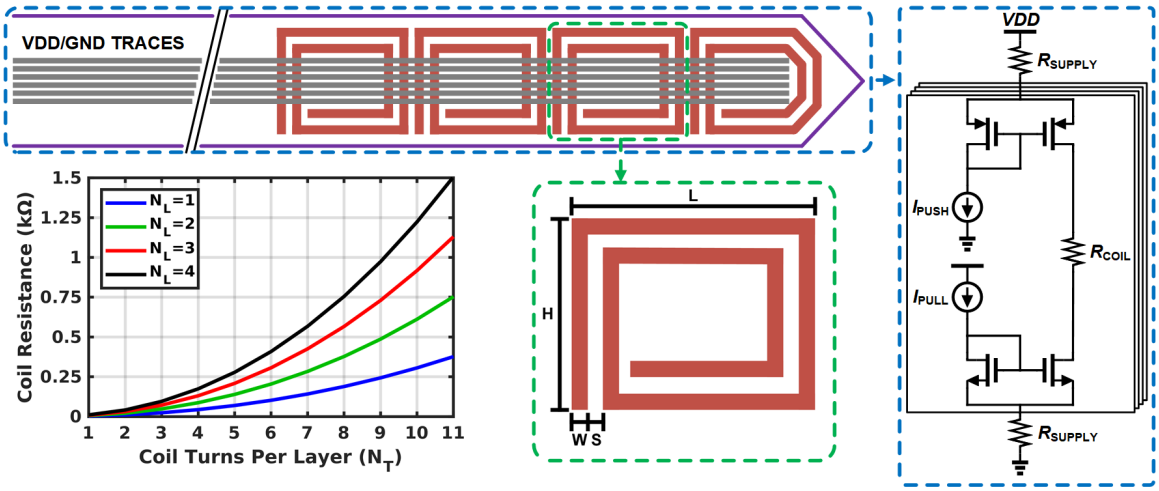

Figure 3.6: Conceptual diagram showing long supply routing to coil drivers adding parasitic resistance and removing available headroom for the micro-coil. Plot shows how micro-coil resistance scales with an increase in the number of coil turns per metal layer.

the supply traces. However, as the number of turns within an allotted coil area increases, the resistance scales super linearly because of increasing amounts of area spent on spacing between micro-coil turns. The equation for the micro-coil resistance is:

$$R_{COIL} = N_L \rho W[2N_T(H+L) - (8[N_T - 1] + 1)(W+S)] \tag{3.3}$$

Where H and L are the dimensions of the micro-coil, N_T and N_L are the number of turns per layer and the number of layers, W and S are the trace width and spacing, and ρ is the resistivity of the metal. Furthermore, the following constraint is needed to ensure the turns stay within the allotted coil area:

$$N_T W + (N_T - 1)S \leq W_{MAX} \tag{3.4}$$

Where W_{MAX} is allotted coil area width. The micro-coil optimization results

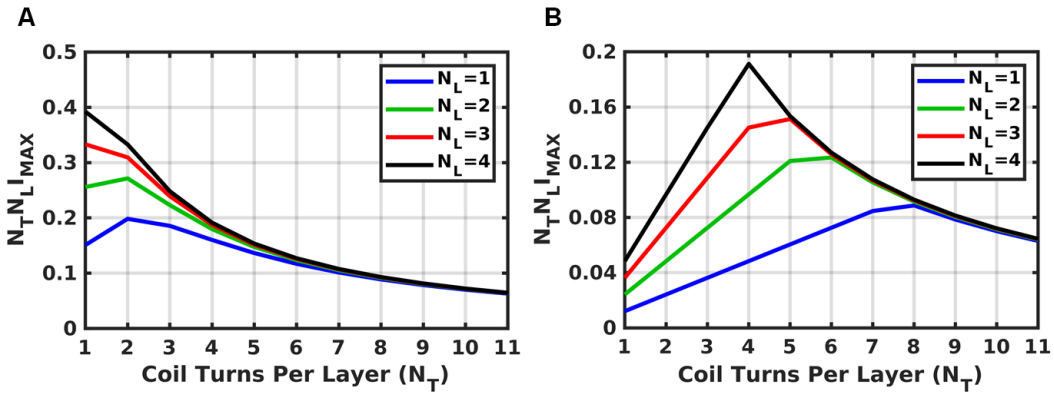

Figure 3.7: Coil optimization results. (A) No current driver area constraint yields a maximum equivalent current when the micro-coil uses four metal layers with one turn per layer. (B) Limiting the current driver area to fit inside the micro-coil yields a maximum equivalent current when the micro-coil uses four metal layers with four turns per layer.

are shown in Fig. 3.7. Based on the resistivity of the traces and desired coil dimensions, an optimization shows the maximum magnetic field is produced when there is only one turn per layer (with four layers used), yielding a turns to maximum current product of 427 mA. However, the required current to produce this maximum magnetic field cannot be achieved with reasonably sized current drivers. Therefore, an additional constraint to the coil optimization accounts for the maximum current that can be produced by a current driver that can fit inside the micro-coils. The final optimization results in the maximum magnetic field produced by a micro-coil using four metal layers with four turns per layer, with dimensions of 250 $\times$ 100 µm and a turns to maximum current product of 194 mA. Based off of prior biological studies with programmable micro-coil neural probes, this will produce E-field gradients capable of modulating neural activity [130].

While this optimization should give a very good approximation of the maximum magnetic field, there are parameters unaccounted for. Process variations

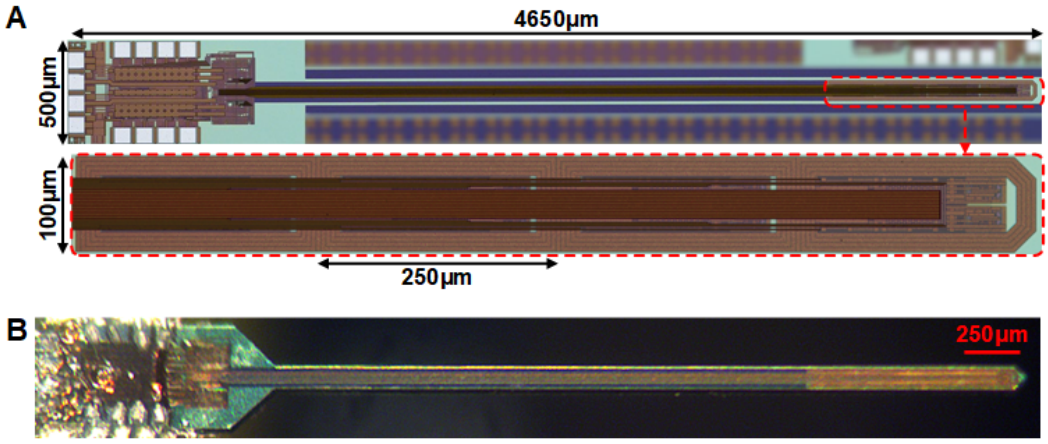

Figure 3.8: Micrograph of the proposed probe. (A) Unreleased probe with zoom in on micro-coils with internal drivers. (B) Released and encapsulated probe.

can change the threshold voltages of the FETs, adjusting their overdrive voltage and current density, and thus impacting the optimization results. Furthermore, the optimization assumes that each micro-coil layer contributes equally to the produced magnetic field. Improvements can be made by weighing the contribution each layer has on the produced magnetic field differently and allowing for a different number of turns on each layer.

3.4 Measurement Results

The neural probes were fabricated in a 180 nm 1P6M CMOS process and shown in Fig. 3.8. The probes are released using the nanofabrication process discussed in [130] and have a shank length and width of roughly 3900 µm and 110 µm respectively. Neural probes consist of four micro-coils using four metal layers to produce sixteen total turns with dimensions of 250 x 100 µm. The supply traces are routed as twenty alternating VDD/GND traces in the middle of the probe to ensure that the supply currents do not produce unintended magnetic

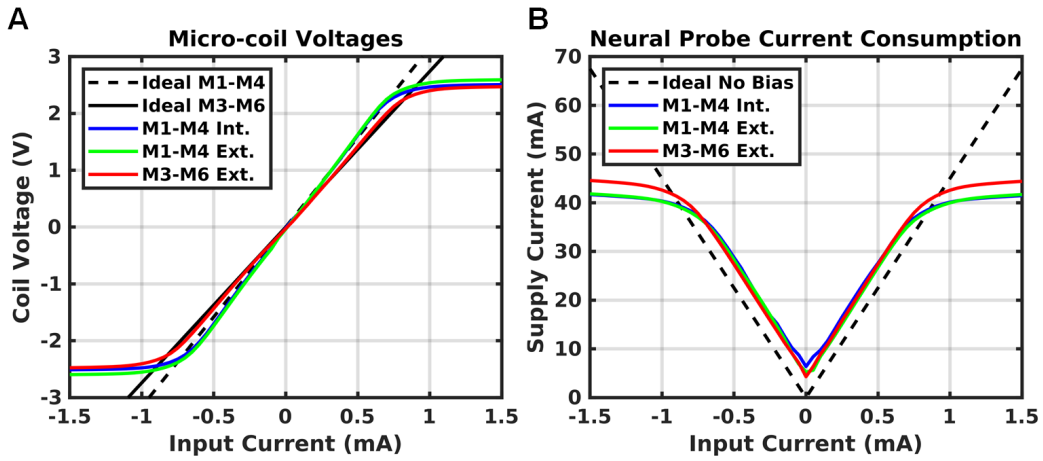

Figure 3.9: Plots comparing the micro-coil voltage and supply current consumption against the neural probe input current.

fields. Three variations of the coils were fabricated where the current drivers are located either inside or outside the coil array and utilizing different metal layers for the micro-coil design. A custom circuit board is designed to handle the four-wire interface communication, produce the differential stimulation current, and measure the micro-coil terminal voltages.

3.4.1 Micro-Coil Characterization

Released micro-coils were characterized by sweeping the stimulation current and measuring the differential micro-coil voltages to determine the maximum stimulation current before coil driver saturation. Tests were done in room temperature phosphate buffered saline (PBS, Gibco 10010-023, pH 7.4 (1X)), and with stimulation waveforms similar to those used in [130]. Current-voltage plots are shown in Fig. 3.9 comparing the three micro-coil and driver configurations. The plots show that maximum stimulation current for the micro-coils using the bottom four metal layers is roughly 8.5 mA. The design using the

top four metal layers shows a higher maximum stimulation current of 9 mA, which is due to the thicker top metal layer, thus reducing the resistance of the micro-coil and the headroom it consumes. Note that the micro-coil driver output current compression begins roughly 150 µA before flatlining at the previously reported values.

Furthermore, since the top of the micro-coil is closer to the surface of the probe, the induced electric field gradients will be stronger than those from micro-coils using the bottom four metal layers. The current consumption plot shows the expected linear scaling of the current consumption until coil driver saturation, with variations in the bias currents across designs due to process variations affecting the bias points of the transistor pairs operating in class AB mode.

3.4.2 In Vitro Olfactory Bulb Slice Experiments

In vitro testing is done on 300 µm-thick slices of mouse olfactory bulbs from 5-12 week old mice. The tissue is horizontally sliced with a vibrating microtome and bathed with oxygenated artificial cerebrospinal fluid (aCSF) at 34°C during recordings. Slices are aligned to the MEA by locating bands of spontaneous activity that indicate the mitral cell and external plexiform layers [108]. The neural probe is placed on top of the slice above the band showing the most activity. The placement of the proposed probe to the tissue and MEA is shown in Fig. 3.10. Testing consisted of driving the micro-coils with stimulation trains of fifty 10 Hz ramp waveforms (1 mA peak amplitude input current, 50% duty cycled, negative ramp polarity) spaced ten seconds apart while observing changes in

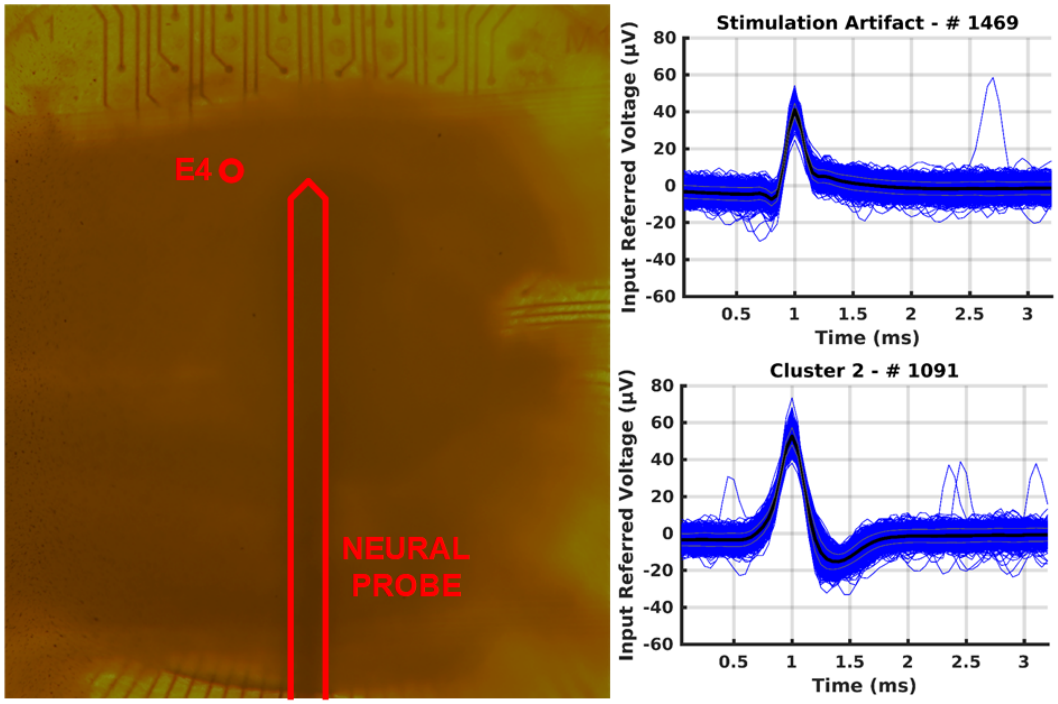

Figure 3.10: Micrograph of the *in vitro* experiment set up with time-aligned spikes and stimulation artifacts detected by [24] on electrode E4. The olfactory bulb slice is placed on top of the electrode array and the proposed probe lays flat on top of the slice.

neural behavior. Note that the recordings are measured on the bottom of the slice and the stimulation is occurring on the top slice. However, the tissue slice is too thick for the micro-coil stimulation to directly stimulate neurons recorded on the bottom slice [77, 130].

Spikes and local field potentials (LFPs) are recorded using a 120-electrode MEA (MultiChannel Systems) with titanium nitride electrodes (30 µm diameter, 30-50 kΩ impedance, 200 µm pitch). The electrodes are embedded within a thin polyimide foil that is perforated (20-90 µm diameter) to facilitate perfusion and oxygenation of the slice from both sides and to draw the slice down against the MEA with a gentle vacuum, which improves the signal-to-noise ratio and enables the use of thicker slices with correspondingly richer lateral connectivity.

Recordings are bandpass filtered (1 Hz – 3.3 kHz) and amplified (1200x) before sampling at 20 kHz with a bit depth of 24 bits per sample. This enables spikes to be recorded at a high resolution even at amplifications low enough to also record LFPs.

Recorded data are zero-phase (forward and reverse) re-filtered between 300 Hz – 3 kHz prior to offline spike sorting and unit identification using the WaveClus software package [24]. Well-isolated candidate units are analyzed as single-unit data when: (1) all spike events have amplitudes greater than 4 standard deviations above the voltage signal (thresholded based on the signal-to-noise ratio of the individual recording), and (2) the number of spike pairs with an interspike interval below 3 ms (the refractory period) is less than 1% of the total spikes for that unit. Any spikes not clearly separable by these criteria are treated as multiunit data. These conservative spike sorting criteria are designed to minimize how often spikes from separate units are incorrectly combined into single-unit datasets, thus adding reliability to subsequent analyses of spike-mediated information.

Unit identification is able to differentiate between spikes and stimulation artifacts of similar amplitudes. Fig. 3.11 shows preliminary results using a neural probe with micro-coils using the bottom four metal layers and internal drivers. The highlighted stimulation train is configured to have the two inner coils run current in opposite directions to generate the strongest gradient in the electric field, while the outer coils are disabled. The dot plot for electrode E4 shows that the stimulation waveform has an inhibitory effect on the recorded activity, consistent with the results found in [130], while reducing the stimulation power consumption by a factor of five.

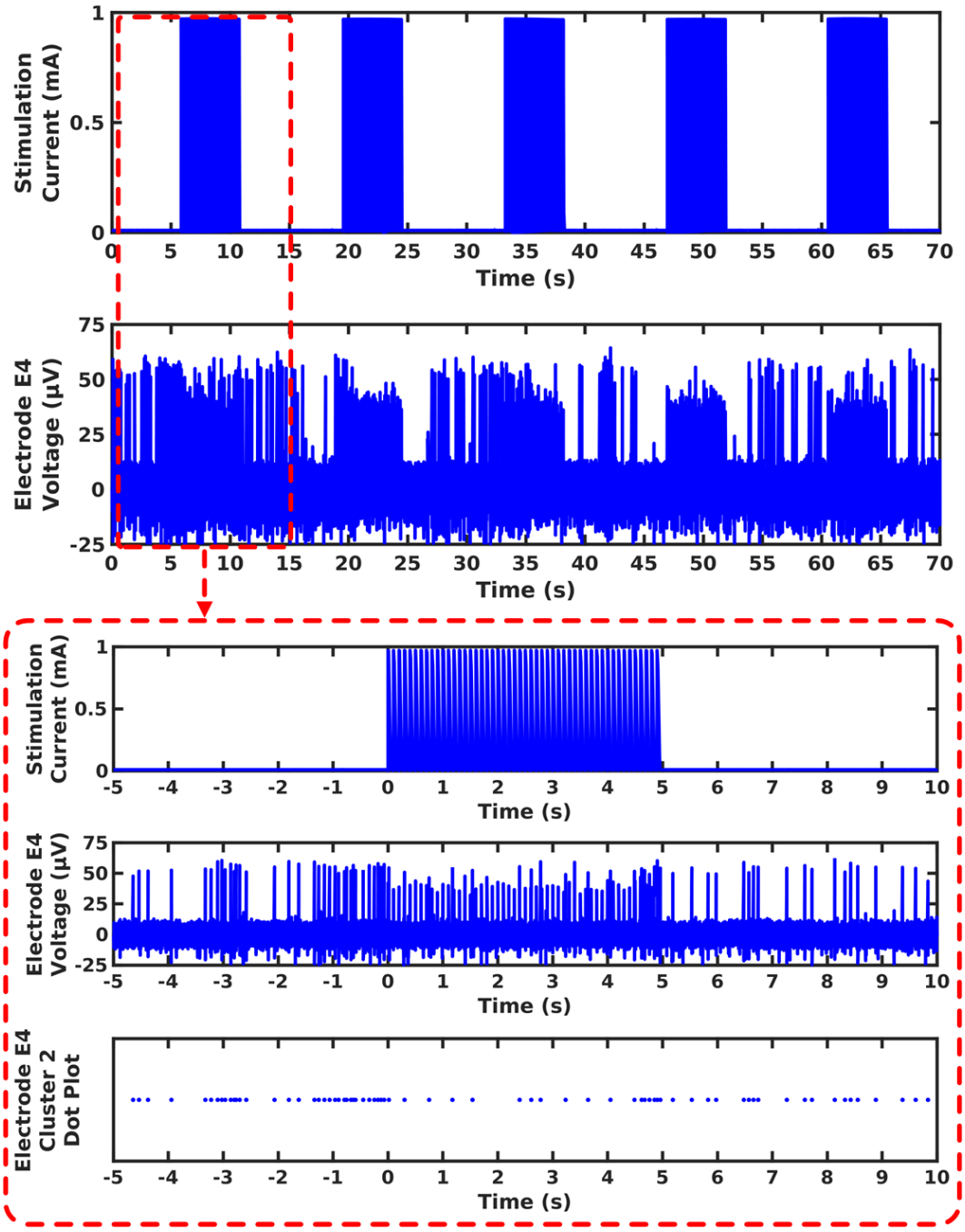

Figure 3.11: Transient measurements for the stimulation current and filtered input referred voltage for electrode E4. Zoom in of the first stimulation train highlights the inhibitory response observed on electrode E4. The dot plot highlights when the recorded neuron fires.

Note that the micro-coil neurostimulation is not capable of directly stimulating the recorded mitral/tufted cells on the bottom of the slice. It is likely that there is invoked neural behavior at lower stimulation currents and the effect is not strong enough to propagate to the bottom of the slice [119]. Since the proposed probe is unable to directly stimulate the recorded neurons on the bottom of the slice, it is advantageous to design a micro-coil neural probe that is also capable of measuring neural activity near the surface of the probe.

3.4.3 Stimulation Artifact Characterization

The tested micro-coil neural probe variation is configured with the micro-coil traces using the bottom four metal layers and the micro-coil drivers are placed outside of the micro-coils. This allows the AC-coupling MIM capacitor to be placed directly above the stimulation sites on top of the micro-coils and allow the stimulation artifact amplifier to be placed near the electrodes inside the micro-coils. The passivation layer above the AC-coupling MIM capacitors has a 25 µm × 25 µm opening to platinize the top of the MIM capacitor to integrate platinum recording electrodes into the micro-coil neural probe design. The platinization is done using a lift-off process with AZ-nLOF 2020 photoresist and sputter deposition (ATC-Orion 5 UHV with Load-Lock by AJA International INC) to deposit 10 nm of Cr (used as an adhesion layer) and 100 nm of Pt.

The ASICs are then encapsulated in 2 µm of parylene C (PDS 20210 Labcoter 2) to prevent unused bond pads from making direct contact to the saline bath. Openings in the parylene encapsulation are made using contact photolithography (SPR220-3.0 photoresist, ABM Contact Aligner) and an oxygen plasma etch

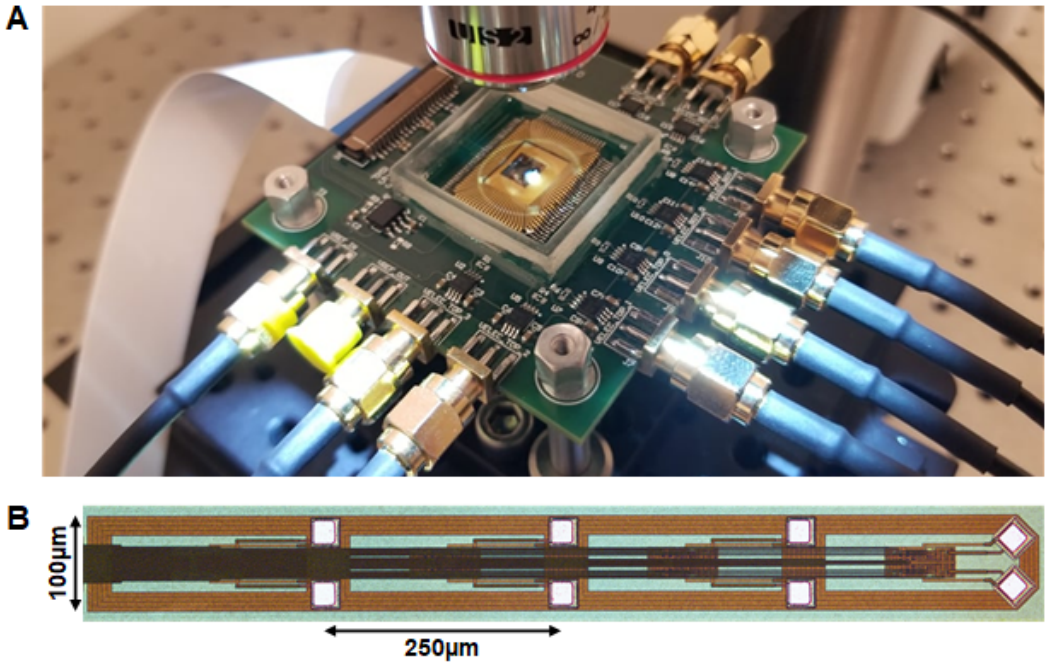

Figure 3.12: Encapsulated breakout micro-coil with recording electrodes. (A) Test circuit board with saline containment ring. (B) Micrograph of micro-coils and recording electrodes with etched openings in the encapsulation.

(Oxford PlasmaLab 80 RIE System). The neural probe is electrically connected to a test circuit board via wire bonds (Westbond 7400A) and a 3D printed ring (Objet30 Pro 3D Printer) is secured around the chip package to contain the saline. Finally, the wire bonds and all exposed metal from the chip package are coated in a clear epoxy (EPO-TEK 301, Epoxy Technology) to prevent any direct electrical contact to the saline from causing hydrolysis or corrosion. The test circuit board and processed recording electrodes are shown in Fig. 3.12. The electrode outputs are buffered by INA821 instrumentation amplifiers, configured to have unity gain. The outputs are filtered by a 10 kHz single pole, passive low pass filter before being sampled.

The transfer function is measured by directly driving one of the electrode inputs through a wire bond with a function generator (3322A, Agilent Tech-

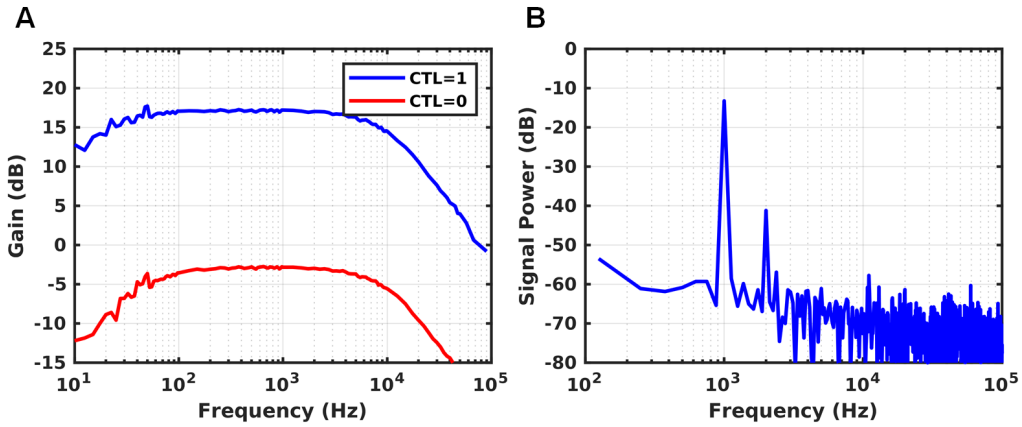

Figure 3.13: Stimulation artifact amplifier transfer function for both gain settings and output PSD for the amplifier in the higher gain setting with a 1-kHz sinusoid, 20 mV_{pp} input.

nologies, Inc.) and measuring the output with an oscilloscope (MSO2014B, Tektronix, Inc.). The measured transfer function and output PSD is shown in Fig. 3.13. When the gain selection bit CTL is set high the measured in-band gain is 17 dB with a high pass corner frequency of 20 Hz. The gain decreases to -3 dB and high pass corner frequency moves to 40 Hz when CTL is set low. The in-band gain is 3 dB less than expected and is attributed as loss from the PFET source followers that buffer the amplifier outputs off-chip. The PSD plot shows an SNDR of 28 dB and SFDR of 40 dB, with the SNDR limited by the second harmonic nonlinearity commonly seen in single-ended open-loop amplifiers [132].

Fig. 3.14 shows the measured stimulation artifacts when the middle coils are driven in opposite directions, the outer coils are inactive, and the artifact amplifier is set to the higher gain setting. Since the dominant source of the stimulation artifact occurs from electrical coupling from the micro-coil voltage, the majority of the stimulation artifact appears as a common-mode signal for electrodes located over the same micro-coils. The strongest stimulation artifact is measured on the electrodes over the tip of the probe over an inactive micro-coil.

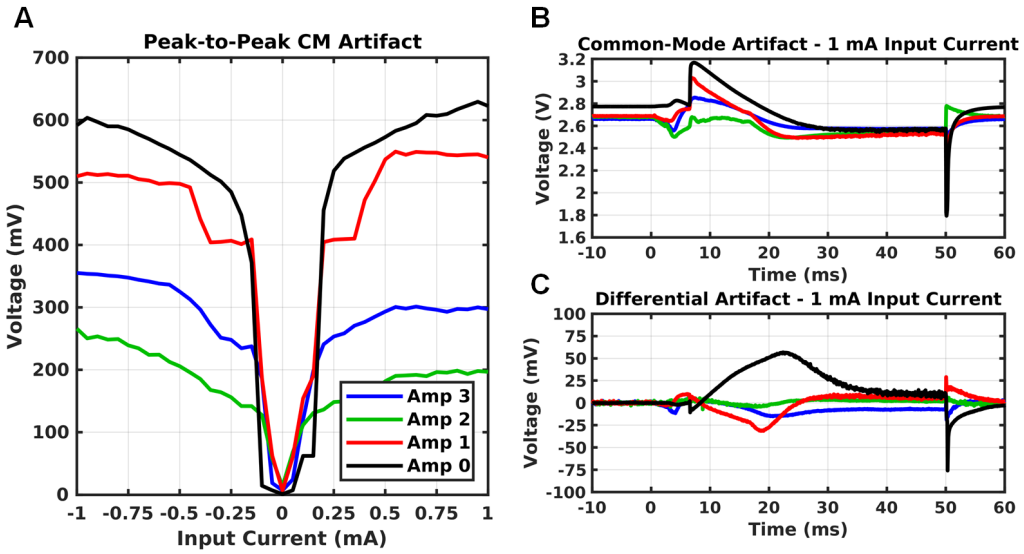

Figure 3.14: Micro-coil-based stimulation artifact measurements. Artifacts peak-to-peak voltages are measured during stimulation and ignore the RC decay post stimulation. Transient measurements of the common-mode and differential artifact are shown across all amplifier pairs for a peak stimulation current of 1 mA. Amplifier 0 measures the electrodes at the tip of the probe.

This is caused by both micro-coil terminals being driven by cascoded current mirror outputs, thus are driven by a high output impedance source where the output voltage nodes are poorly defined. Therefore, the common-mode voltage for inactive micro-coils is prone to coupling from adjacent micro-coils, causing rail-to-rail perturbations that, in turn, couple onto the recording electrodes. The common-mode artifacts coupling onto electrodes over inactive micro-coils can be significantly suppressed by implementing common-mode feedback in the micro-coil driver circuitry.

The maximum common-mode stimulation artifact is measured across the input stimulation current range of ±1 mA with the same waveform parameters used in the previously mentioned *in vitro* experiments. The maximum measured common-mode artifact from the trials is 630 mV_{pp}, which corresponds to an input-referred stimulation artifact of 90 mV_{pp}. Note that the stimula-

tion artifact is only measured during the stimulation waveform and ignores the RC decay that occurs during the sharp gradient of the stimulation waveform. This is because the RC decay settles back to DC in only a few milliseconds and optimization of the stimulation waveform can eliminate the sharp gradient all-together [76,77,110,121]. The largest differential artifact measured is 70 mV_{pp}, corresponding to a 10 mV_{pp} input referred signal. Therefore, a neural amplifier with a typical noise floor of 5 μV_{rms} must have a dynamic range of 66 dB to handle the differential artifact without nonlinearities causing lost neural signal recordings, exceeding the limits of traditional neural recording front ends [60,61,97,102].

3.5 Discussion

3.5.1 Comparisons to Prior Micro-coil Neural Probes

The power consumption during stimulation for the proposed multi-turn micro-coil probe has decreased from the previous *in vitro* study for a CMOS micro-coil based neural [130]. Measurements show the proposed probe consumes 140 mW (40 mA on a 3.5 V supply), while the previous probe consumed 375 mW (150 mA on a 2.5 V supply). Note that approximately half of the measured stimulation current consumption is being used to drive two micro-coils, while the rest of the of measured current is spent on the ternary current driver as well as the quiescent bias current of the inactive micro-coil drivers. While the stimulation power consumption is reduced by only a factor of 2.7, the stimulation current is reduced by a factor of 15 which allows for a more integrated and scalable

neural probe design as the individual micro-coil drivers can fit inside the area of a micro-coil.

The stimulation current of the proposed neural probe is roughly four times larger than the single-turn micro-coils used in prior *in vitro* experiments [76,81]. However, this can be attributed to the differences in the experimental set up that have a significant impact on the necessary stimulation current. The slices used were V1 coronal slices from a Thy1-GCaMP6f transgenic mouse, allowing for fluorescent imaging of the direct neural response on the top side of the tissue slice. Furthermore, the neural probe was placed such that the stimulation sites are located directly over the proximal axon of the targeted neuron as it has a higher sensitivity to stimulation [38,58,128,141]. Finally, the stimulation waveform used was a single period sinusoidal current as opposed to a ramp waveform. This was selected as the induced E-field has a tri-phasic waveform where the duration of the second phase is longer than the first and last phase, which is thought to reduce the necessary activation threshold [38,58,128,141].

It is feasible that the lower stimulation currents of the proposed neural probe were modulating neural behavior around the probe on the top of the olfactory bulb slice with the invoked behavior not strong enough to propagate to the bottom of the slice where the MEA was recording neural activity. Furthermore, with finer probe placement relative to the desired neurons and with further optimization of the stimulation waveform it is possible for the proposed neural probe to stimulate neural activity while consuming less power than prior micro-coil based neural probes.

3.5.2 Nanofabrication Process for Recording Electrodes

It was previously discussed that one of the benefits to using magnetic stimulation from micro-coil-based neural probes was the probes could be entirely encapsulated in biocompatible materials, eliminating the concern of water infiltration through weak bonding between exposed electrodes and encapsulation material [80, 81]. However, this is no longer the case when designing micro-coil based neural probes with integrated recording electrodes. Recent work has shown that depositing insulation materials, such as SiO_2 or Si_xN_y, using a combination of atomic layer deposition (ALD) and plasma enhanced chemical vapor deposition (PECVD) can allow for long term chronic electrical recordings [84]. This process provides robust encapsulation while also reducing the encapsulation thickness down to roughly 1 µm [84]. This decrease in the encapsulation thickness (compared to 5 µm parylene encapsulation used) would increase the E-field gradient strengths seen by neurons on the surface of the probe by 20%.

3.5.3 Design of Stimulation-Tolerant Neural Amplifier

Traditional neural amplifiers are designed to amplify both local field potentials (1 - 200 Hz) and action potentials (200 - 5 kHz) while maintaining a low noise floor, sufficiently high common mode and power supply rejection, and consuming low power and area to be scalable for mass recordings [47]. However, this topology has its limitations for closed-loop neuromodulation systems as the stimulation artifacts appear in-band and are several orders of magnitude larger than the neural signals. Traditional neural amplifiers are not suitable for measuring large signals due to the highly non-linear pseudo-resistor used for

creating the low frequency high pass filter. Furthermore, stimulation artifacts cause amplifier saturation, resulting in loss of neural recording until the amplifier settles back to normal operating conditions.

Electrical stimulation artifacts vary by the electrode geometry and application and can be on the scale of 1 V with nonlinear electrochemical reactions making it very difficult to suppress the artifact on a stimulation electrode [124]. Recording front ends that are not capable of handling stimulation artifacts of this scale disable the recording front end until the electrode voltage settles back to the operating voltage range [14]. Modern neural recording front ends have increased the operating voltage range by recording neural signals in the presence of differential artifacts as large as 200-mV_{pp} and common-mode artifacts as large as 700-mV_{pp} without distortion [22, 23, 62]. While these topologies are unable to handle large electrical stimulation artifacts occurring near stimulation electrodes, they are capable of handling the stimulation artifacts produced by micro-coil magnetic stimulation, allowing for simultaneous neural recordings at the stimulation sites.

3.6 Conclusion

This work proposes a neural probe that co-optimizes the micro-coil design with CMOS current drivers to maximize the electric field gradients and reduce the necessary stimulation current. Independently driven multi-turn micro-coils allow for spatially programmable neurostimulation sites between adjacent micro-coils. A four-wire interface is used to reduce the number of pads on the probe backend by using the supply and differential current inputs as the programming

clock and data signals respectively. The electrical performance of the probes is characterized in a phosphate buffered saline bath. Preliminary *in vitro* testing of the neural probes is done with slices of a mouse olfactory bulb in conjunction with an MEA showing changes in neural behavior.

CHAPTER 4

SIMULTANEOUS MICRO-COIL NEUROSTIMULATION AND ELECTRODE RECORDING SITES ON INTEGRATED SOI-CMOS NEURAL PROBE

4.1 Introduction

The use of electrical stimulation through implantable electrodes has allowed the development of neural prostheses to treat neurological disorders and restore sensory and motor functionality. Deep brain stimulation (DBS) has been shown to effectively reduce the symptoms associated with diseases such as Parkinson's disease and epilepsy [11, 70, 142]. Furthermore, cochlear prostheses have also been effective in restoring the sensation of hearing to profoundly deaf patients [144,145]. While this success has prompted development of neural prostheses for various applications including visual prostheses [2,105,123], limb prostheses [109,126], and treating other neurological disorders [33,48,63], there are fundamental limitations with electrical stimulation inherit with implantable electrodes that limit this approach.

The first limitation arises from the spatially symmetric electric field produced by implantable electrodes. This prevents specific neurons from being targeted, limiting the effective stimulation spatial resolution as passing axons from nontargeted regions are activated [10,50,115,140]. The unintended activation of other regions can lead to a variety of problematic side effects produced by the neural prosthesis [35, 43, 46]. While there have been efforts to enhance the stimulation spatial resolution utilizing multiple electrodes, the results have yielded marginal improvements while requiring more complicated electrode

structures and driving circuitry [17, 146]. The next limitation arises from concerns over the long-term viability of the electrical stimulation from implantable electrodes over time. Inflammatory reactions generated in response to the neural prosthesis implantation can lead to glial scarring encapsulation around the electrode and increase the neural activation thresholds over time [17, 49, 65, 103]. While neurostimulation hardware is designed to be programmable to increase the stimulation current and re-elicit neural behavioral responses, the increase in the tissue impedance from glial scarring reduces the available headroom for the electrode driver circuitry, potentially preventing the hardware from producing sufficient stimulation currents [26, 104, 139]. The final discussed limitation is that the electrode-tissue interface is prone to electrochemical effects (such as hydrolysis and corrosion) that can damage the electrode and/or surrounding tissue if charge transfer levels per phase are too high [30, 91].

Magnetic stimulation is another well-established approach for modulating neural activity that overcomes limitations observed with implantable electrodes. Traditionally, this has been explored using transcranial magnetic stimulation (TMS) which utilizes large coils positioned adjacent to the scalp to modulate activity of cortical neurons [8]. Developments in micro-magnetic technology has produced implantable micro-coils that utilize the spatially asymmetric induced electric fields to avoid the activation of passing axons, thus confining the effective stimulation region [76, 77, 119]. Furthermore, since magnetic fields have a high permeability to biological tissue and biocompatible materials, their stimulation efficacy is not weakened by glial scarring and can be completely encapsulated in materials that mitigate the implantation response [21, 53, 122]. This is an improvement over implantable electrodes that require openings in the encapsulation layer and can suffer from water infiltration due to weak bonding

between the encapsulation layer and exposed electrode surface [80, 81]. While implantable micro-coils devices on the scale of implantable electrodes have been shown to modulate neural behavior in *in vitro* and *in vivo* experiments, these devices lack reconfigurable hardware that is more commonly seen in implantable electrode systems, thus fixing their stimulation sites after implantation [40, 66].

Recent work has addressed the lack of programmable stimulation sites by incorporating CMOS technology into the micro-coil design with additional nanofabrication processing. The first of such neural probes utilized programmable switching networks to develop a programmable micro-coil to change the location of the stimulation sites [130]. However, this work did not utilize multi-turn micro-coil designs to reduce the necessary stimulation current and required very large switches in order to keep the micro-coil voltage below the transistor breakdown voltage during stimulation. The large switches reduce the current density flowing through the switches, thus reducing the maximum induced electric field. More recent work has addressed these shortcomings by co-optimizing the micro-coil design with integrated CMOS current drivers to provide spatially programmable stimulation sites from multi-turn, independently driven micro-coils [129] Fig. 4.1 shows a simplified overview of how a neural probe stimulates neurons above the surface of the probe through magnetic stimulation by driving the bottom micro-coil.

This work proposes a neural probe that builds upon the prior CMOS micro-coil-based neural probes by utilizing a high voltage SOI-CMOS process to co-optimize the multi-turn micro-coils with independent integrated current drivers. By using a higher supply voltage for the micro-coil drivers, there is more headroom available to the micro-coil, thus allowing for more turns to re-

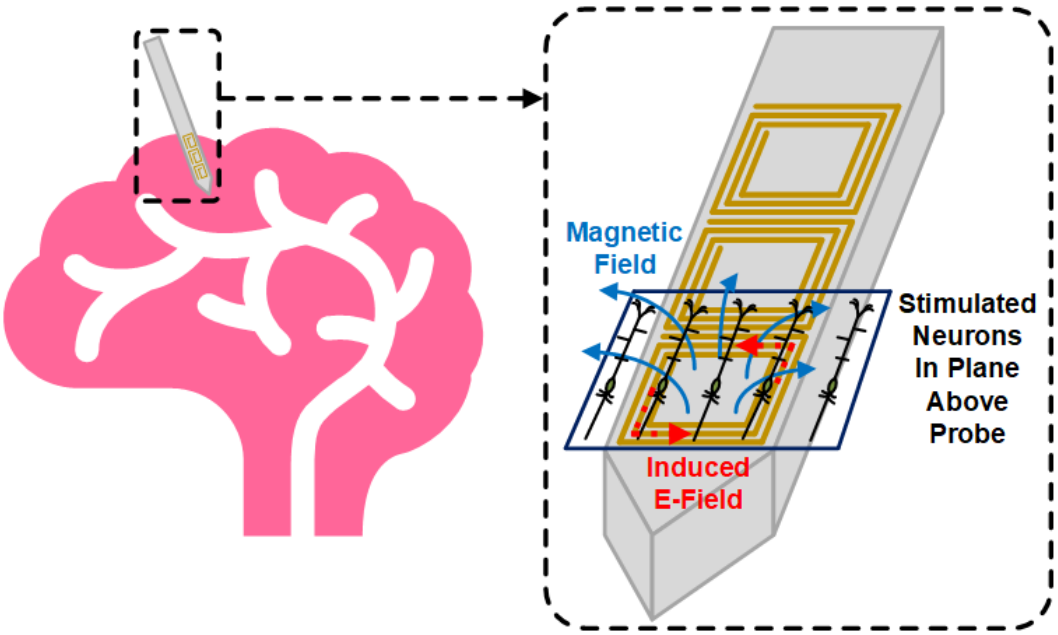

Figure 4.1: Conceptual diagram illustrating magnetic field lines produced by the micro-coil as well as the induced electric field.

duce the necessary stimulation current. Furthermore, by incorporating SOI-CMOS technology there are more opportunities to explore how the bulk substrate affects the induced electric fields. The insulation layer can be used as an etch-stop layer to selectively etch and shape the backside carrier silicon layer [143]. Finally, to address the lack of neural recording capabilities to enable to enable a closed-loop implantable neural front end, electrode sites are placed directly above the micro-coil stimulation sites with neural amplifiers designed to record the neural signals, taking advantage of the significantly smaller stimulation artifacts produced by micro-coil magnetic stimulation [19,45,130,133]. The risk of water infiltration is mitigated by taking advantage of modern nanofabrication techniques used by implantable CMOS neural recording nodes [84].

4.2 Electromagnetic Simulations

4.2.1 Electromagnetic Modeling

Stimulating neural tissue requires a sufficient gradient in the electric field to be produced along the axon of a neuron to generate local membrane depolarization. The electromagnetic derivation for the induced electric fields (E-fields) produced by the current flowing through the micro-coil can be found in [77]. Electromagnetic simulations are performed using the Magnetic and Electric Field (mef) module within COMSOL Multiphysics to predict the location and strengths of the local E-field gradients. Finite element method (FEM) simulations are performed to calculate the spatial gradients of the induced E-fields arising from the current flow through the micro-coils under varying substrate shapes. The model consists of two four-turn, single-layer micro-coils over a silicon substrate etched in various probe-shaped structures. Simulations are performed with both micro-coils driven in opposite directions.

The aluminum micro-coil traces have a cross-sectional dimension of $4.79 \times 1.0\,\mu m$ with a wire spacing of $0.28\,\mu m$. The substrate of the SOI CMOS process consists of a thin device silicon layer, over a thin insulation layer, over a carrier silicon layer. This is modeled as a thin device silicon layer over a carrier silicon layer to simplify the simulations, with the boundary conditions set to electrical insulation to prevent potential induced eddy currents from flowing between layers. The device silicon substrate has a cross-sectional dimension of $4.5 \times 110\,\mu m$ and a length of $715\,\mu m$, with the last $45\,\mu m$ tapering to a point. E-field gradients are compared against two carrier silicon shapes: an extension of the device layer so the total substrate thickness is $60\,\mu m$ and a substrate that

is cut inwards such that it does not sit underneath the micro-coils and stimulation sites (thickness still 60 µm). The dimensions of the probe results in a cross-sectional area comparable to micro-fabricated intracortical electrodes that are routinely implanted without causing significant damage to the neural tissue [69, 136].

The simulation environment models the neural probe surrounded in a medium (0.8 × 0.3 × 0.25 mm) with the properties of gray matter (electrical conductivity: σ = 0.27 S/m; relative permittivity: ϵ_r = 12,000) [137], similar to previously used environments to allow for direct comparisons to prior studies [76, 129, 130]. The environment was split with a finer mesh with the micro-coils simulated in a closed-loop configuration. The micro-coil input terminals are sufficiently distanced from the micro-coil turns such that they do not affect the simulated E-field gradients. The stimulation currents driven through the micro-coils are 5-kHz, 37.5-mA sinusoidal waveforms with their current directions defined in Fig. 4.2A-B. The induced E-fields and their spatial gradients are calculated within COMSOL Multiphysics along a plane 15 µm above the surface of the probe, selected based off the typical cell body size for mitral cells and the expected probe encapsulation thickness [99].

4.2.2 Simulation Results

Consistent with prior studies, the strongest E-field gradients are located above the locations where the current flow is changing directions in the micro-coil, with positive peaks for dEx/dx gradients located where negative peaks for dEy/dy gradients are located (and vice-versa) [76, 77, 129, 130]. The dEx/dx,

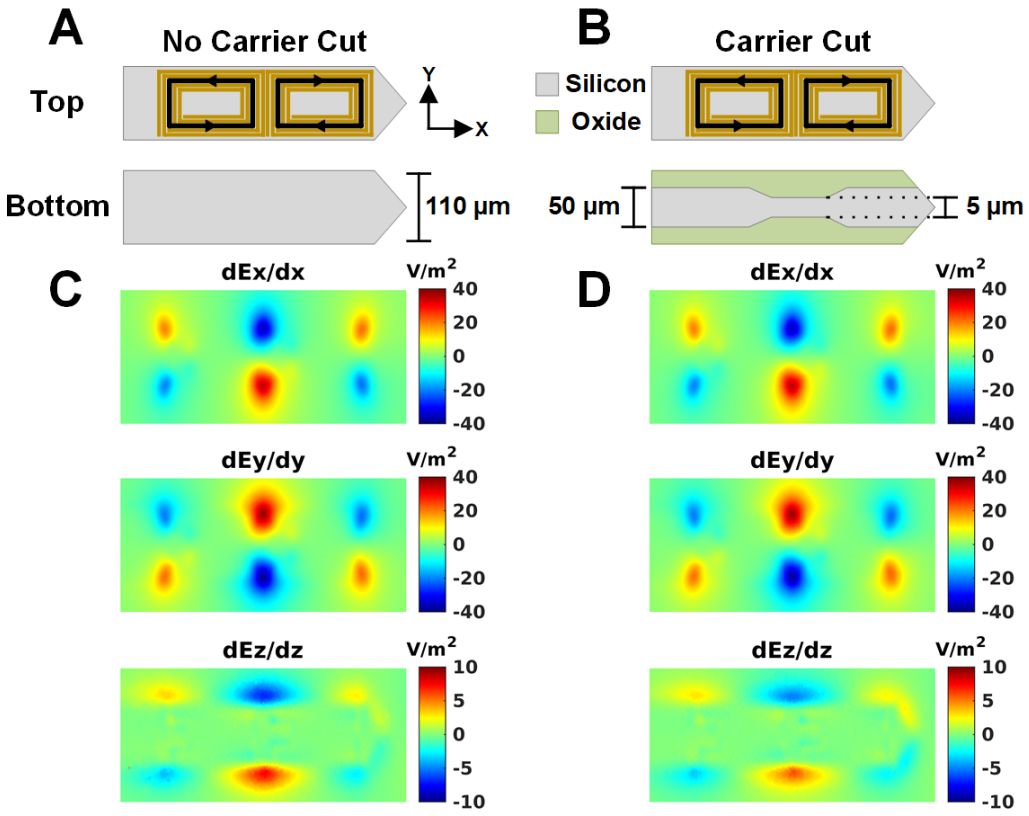

Figure 4.2: Electromagnetic simulations for a neural probe with two multi-turn micro-coils driven in opposite directions with various probe shapes. (A) No patterning on the carrier silicon layer. (B) Carrier silicon layer is 50 µm in width and is tapered down to 5 µm underneath the contiguous boundary of the micro-coils. (C-D) Spatial gradients of the electric field along the x-, y-, and z-axes for the carrier silicon layer configurations used in A-B.

dEy/dy, and dEz/dz gradients for the carrier silicon layer etched in the same probe shape as the device silicon layer are shown in Fig. 4.2C. The maximum gradients for dEx/dx and dEy/dy are 34.86 and 37.89 V/m^2 respectively. The maximum gradient for dEz/dz is 7.50 V/m^2 where the peak is offset by 14 µm along the y-axis off the edge of the probe. This is caused by the magnetic fields produced by the micro-coils passing through the modeled substrate; however, the induced E-fields are re-shaped due to the substrate modeled as an electrical insulator along the boundary. This results in the field gradient ratios dEx/dx

over dEz/dz and dEy/dy over dEz/dz of 4.65 and 5.05 respectively. Note that if there is no modeled substrate these ratios exceed values over 1000 and the asymmetry of the induced electric fields is maximized.

All the field gradients for the carrier silicon layer etched such that it tapers inward, away from the strongest stimulation sites, are plotted in Fig. 4.2D. The maximum values for dE/dx and dEy/dy field gradients 34.89 and 37.41 V/m^2 respectively, with the slight differences from the previous carrier silicon layer shape attributed slight variations in the mesh shape. The maximum gradient for dEz/dz decreases to 5.88 V/m^2, increasing the gradient ratios for dEx/dx over dEz/dz and dEy/dy over dEz/dz to 5.93 and 6.36 (roughly 25% improvement). The theoretical minimum for the dEz/dz gradient would be when the carrier silicon layer is completely etched away, yielding a value of 3.44 V/m^2. While it is not feasible to manufacture a probe where the micro-coil array is on the order of 1 mm long with a thickness of 4.5 µm, this suggests that there are further explorations on etching the carrier silicon layer to maximize the selectivity of targeted neurons in the plane of the probe to vertically oriented passing axons.

4.3 Neural Probe Design

4.3.1 System Overview

An overview for the system architecture of the proposed neural probe is shown in Fig. 4.3. The backend circuitry contains a programming interface that controls a pair of programmable single-ended to differential current amplifiers and a pair of multiplexers that control which differential coil taps and neural ampli-

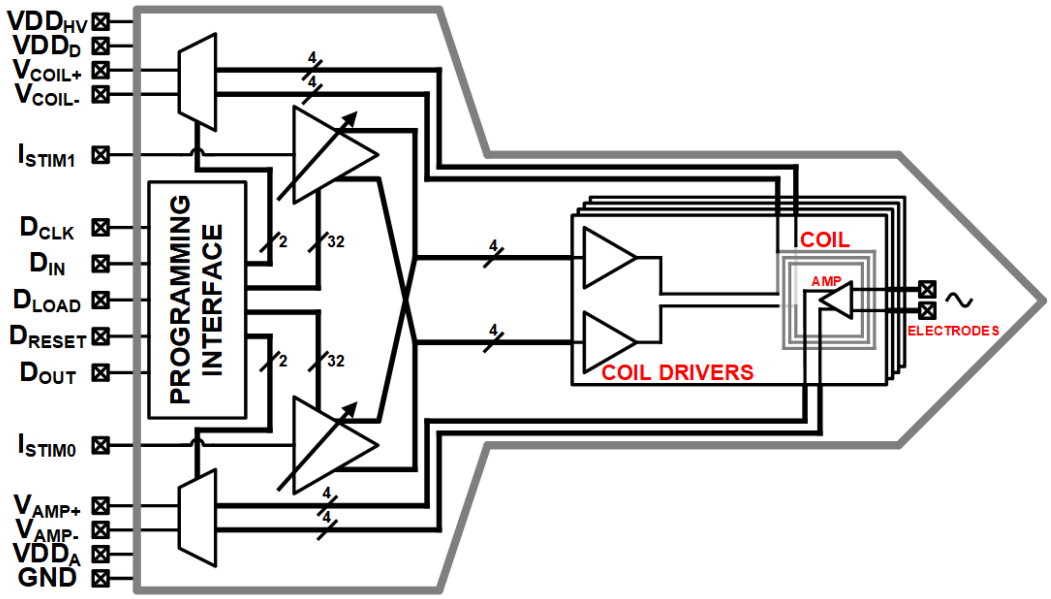

Figure 4.3: System architecture of the proposed neural probe.

fier outputs are brought off-chip. The programming interface and multiplexers operate on a 5V supply, the programmable current amplifiers and micro-coil drivers operate on a 10V supply, and the neural amplifiers operate on a 1V supply with all circuits sharing the same ground. Instead of having a differential stimulation current input as seen in prior work [129, 130], the proposed system has two independent single-ended stimulation current inputs. The programmable current amplifiers drive the micro-coil drivers that are located along the shank of the probe, outside of the micro-coils. This allows the neural amplifiers to be placed within the micro-coils, near the recording electrode sites located above the programmable micro-coil neurostimulation sites. Since the micro-coil taps observe an approximate 0 - 10 V swing and the multiplexer operates on a 5 V supply, a voltage divider consisting of 750 kΩ high density resistors reduce the measured micro-coil tap voltage swing before being buffered by an NFET source follower. The NFET source follower can be disabled and bypassed to allow more accurate micro-coil characterization.

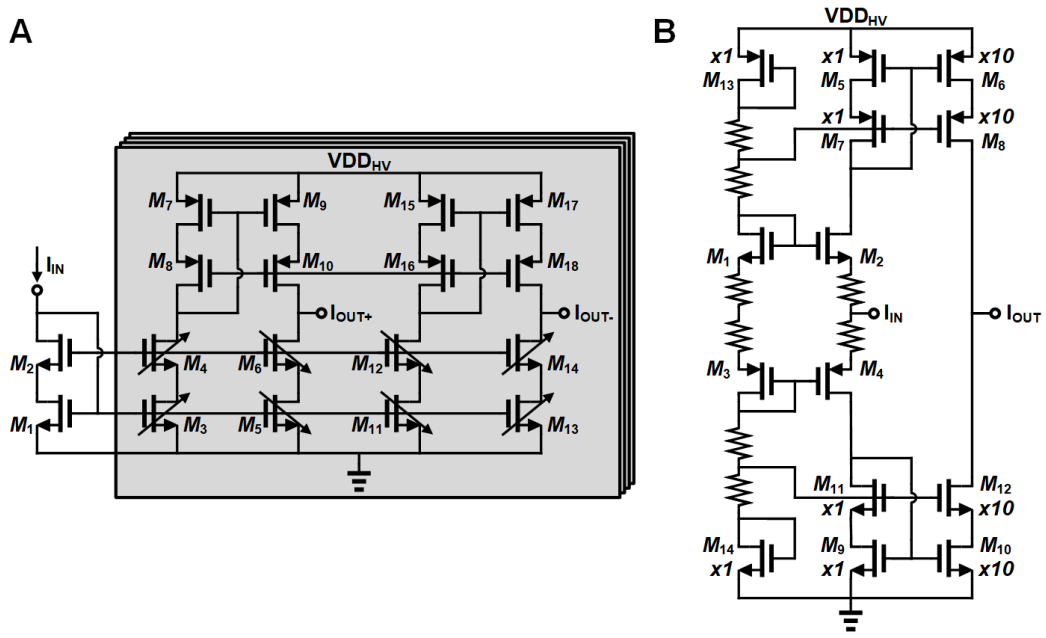

Figure 4.4: Circuit implementation for micro-coil stimulation current blocks. (A) Programmable current amplifier. (B) Push-pull micro-coil driver.

Programmable Current Amplifier

The input current of the programmable current amplifier passes into a cascoded, diode-connected NFET load. The gate of transistor M_1 is shared by four 3-bit NFET current DACs where the current gain is controlled by switching the cascode gate voltage between the cascode bias voltage and ground. To push current into the I_{OUT+} node, the M_3 current DAC must be set to a non-zero 3-bit value while M_5 is set to zero. This allows the input stimulation current to be copied and/or multiplied by transistor M_3, copied by the cascoded PFET current mirror consisting of transistors M_7 - M_{10}. Since M_5 is disabled, all the current is sourced out of the node I_{OUT+}.

To sink the current from node I_{OUT+} the M_5 current DAC is now set to a non-zero 3-bit value while M_3 is disabled, which then disables the PFET DAC. To enable a differential current output to drive the micro-coil drivers, a replica

circuit is created to drive the I_{OUT-} node where the DAC values of transistor pairs M_3, M_{13} and M_5, M_{11} must match. The programmable current amplifier has four parallel copies to drive each of the independent micro-coil driver pairs. Note that the high voltage FETs that are used cannot exceed a V_{GS} voltage of ±5 V.

Instead of using a push-pull driver seen in prior work and level shifting the digital logic to 5 - 10V to control the high voltage PFETs, this amplifier topology was selected as it operates on VDD_{HV} supply, while being easily programmable by logic running on the VDD_D supply [129]. Note that because the input stimulation current cannot be negative, the programmable current DAC must be programmed to switch directions to implement a full sinusoid stimulation current with no DC offset. The programmable current amplifier is shown in Fig. 4.4A.

Push-Pull Current Driver

The micro-coil driver uses a similar push-pull topology discussed in prior work [129]. This topology is selected due to its bidirectional current flow that allows for easy change in current direction through the micro-coil without consuming area needed for large switches. As discussed in prior work, the value of the resistor trades-off between the input current range and the quiescent bias current. Assuming a supply voltage of 10 V, an overdrive voltage of 700 mV, and a threshold voltage of 750 mV, the resistor value is selected to be 12.5 kΩ to set the input current range to approximately ±515 µA. To further reduce the bias current transistor pairs M_1, M_2 and M_3, M_4 are introduced and operate in class AB. The bias current is set by the diode connected transistors M_1, M_3, M_{13}, M_{14},

and the six equivalent resistors. The circuit schematic of the micro-coil driver is shown in Fig. 4.4B.

The mirroring and biasing transistors have an NFET and PEFT unit sizing of 24 µm/500 nm and 60 µm/500 nm respectively. The class AB transistors are optimized to have an NFET and PFET sizing of 6 µm/500 nm and 15 µm/500 nm respectively. Simulations show an expected quiescent bias current of 950 µA per push-pull micro-coil driver. The output of the driver is the parallel output of cascoded PFET and NFET current mirrors with a current gain of 10. This output topology is selected to ensure accurate current mirroring over the wide swing of voltages present across the coil during stimulation, while the gain is selected to minimize the voltage drop across the supply traces routed down the probe.

Neural Amplifier

Due to the uncertainty of the stimulation artifacts that micro-coil-based magnetic stimulation will produce in the selected SOI-CMOS process, the neural amplifier is designed to be as flexible as possible. The design utilizes an inverter-based core, selected to provide a higher g_m for an equivalent bias current [52,75], which leads to a better input-referred noise level. Fig. 4.5 shows the circuit schematic for the neural amplifier. The inverter-based differential pair, consisting of M_1, M_2 and M_3, M_4, is loaded by diode-connected NFETs M_5, M_6. This sets the in-band gain as the ratio of the transconductances of the inverter-based differential pair and the diode-connected load. Therefore, the amplifier gain can be made programmable by controlling the bias currents for the inverter-based differential pair and/or diode-connected load. Common-mode feedback is introduced to the inverter-based differential pair and is implemented with PFETs

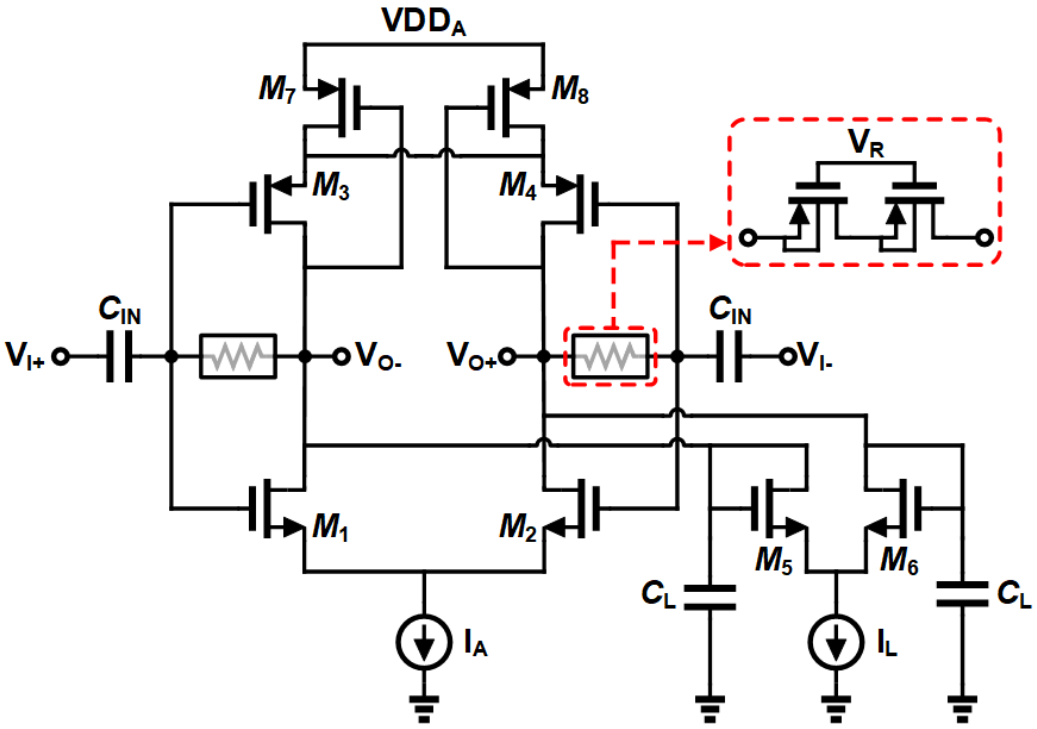

Figure 4.5: Schematic of the neural recording amplifier core. Source follower buffers are not shown.

M_7 and M_8. This is done to suppress the large common-mode stimulation artifacts present during micro-coil-based neurostimulation [129, 130].

The high-pass filter corner frequency is set by the metal-insulator-metal (MIM) input capacitor and the feedback biasing transistor. While past work has shown it is possible to implement a corner frequency less than 10 Hz with a single transistor [83], the proposed design utilizes two PFET transistors as the large pseudo-resistor to improve the differential input voltage range. Furthermore, the high-pass filter frequency is made programmable by controlling the gate of the pseudo-resistors with an off-chip bias voltage [117]. The low pass corner frequency is set by the shunting load capacitors C_L and the transconductance of the diode-connected load. Due to sizing constraints this corner frequency is roughly around 100 kHz, as opposed to a more traditional corner frequency

value for measuring action potentials of 10 kHz or less [47, 60, 61, 83].

4.3.2 Coil Optimization

The coil optimization from prior work is used to maximize the produced magnetic field by co-designing the micro-coils and push-pull amplifiers [130]. Previously, the limiting constraint on the optimization was the lack of headroom for the micro-coil as the resistance increases super-linearly as the number of coil-turns increases. The optimization for a 3.5 V supply in a standard CMOS process yielded a micro-coil with a total of 16 turns (four layers with four turns per layer, dimensions of $250 \times 100\,\mu m$) with a maximum turns-current product of 194 mA.

At first glance, with the supply voltage increasing from 3.5 V to 10 V, it appears that a significantly higher turns-current product can be achieved for a micro-coil with the same dimensions. This is the case when ignoring any area constraints for the push-pull amplifiers as the maximum turns-current product of 874 mA is achieved with a micro-coil utilizing two turns per layer over four layers, over double what is achieved on a 3.5 V supply. However, when constraining the area of the micro-coil driver to fit inside the micro-coil, the turns-current product reduces to 192 mA with the micro-coil having 52 total turns (13 turns with four turns per layer). Increasing the supply to the absolute maximum device voltage of 11 V only increases the turns-current product to 205 mA with the same 52-turn micro-coil.

This is due to the high voltage SOI-CMOS transistors having a worse current density than the transistors in a traditional CMOS process as there is a lot

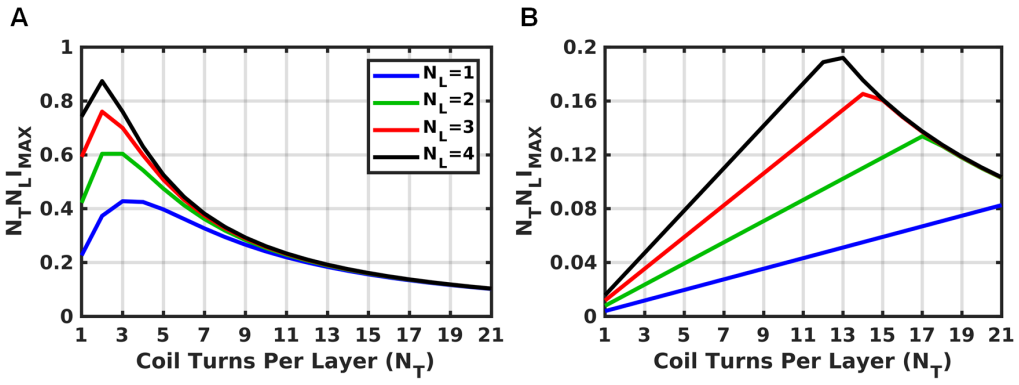

Figure 4.6: Micro-coil optimization results. (A) No circuit area constraint yields a maximum current-turns product when using four layers and two turns per layer. (B) Applying the circuit area constraint yields a maximum current-turns product when using four metal layers with thirteen turns per layer.

of routing overhead needed to ensure the transistors do not breakdown under higher voltages. Furthermore, the SOI-CMOS transistors are sized to have a higher overdrive voltage than the CMOS transistors from prior work to ensure the circuitry would fit within the micro-coil. While the coil optimization does not yield a massive improvement in the maximum producible magnetic field, the power consumed during maximum stimulation per active micro-coil driver reduces from 42 mW down to 37 mW.

4.3.3 Probe Release Nanofabrication Processing

Modifications to the nanofabrication process used for releasing the neural probes from the original chip packaging in prior work are made to address the additional substrate insulation layer [130]. The process uses the same etching mask layers by depositing Al_2O_3 and Cr using atomic layer deposition (ALD, Oxford ALD FlexAL) and sputter deposition (ATC-Orion 5 UHV with Load-Lock by AJA International INC) techniques respectively. The Al_2O_3 will con-

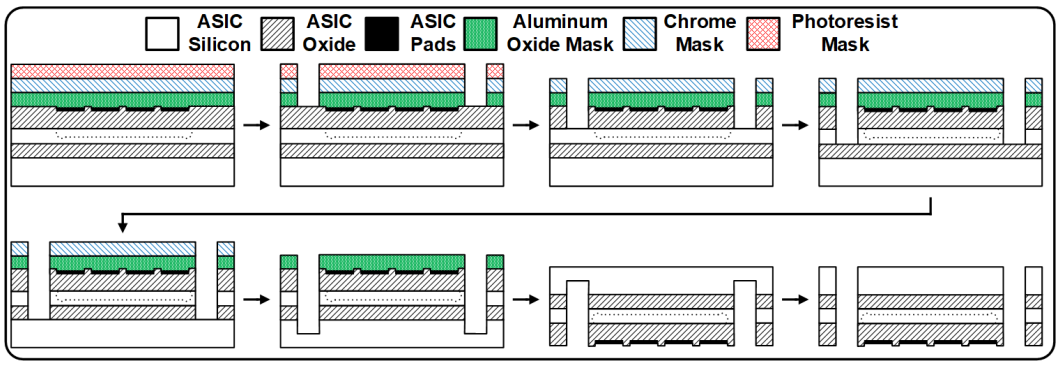

Figure 4.7: Post-nanofabrication process to release the neural probes from the original SOI-CMOS chip packaging. Note that the steps do not include electrode exposure and platinization.

tinue to be used as the etching mask during the silicon trench etching in the wafer handle silicon layer. However, now the Cr will be used for the thermal oxide layer surrounding the metal traces, the device silicon layer, and the insulation layer between the device layer and wafer handle. Due to material constraints (no metal etching masks) when using the deep reactive ion etch (DRIE) process used to etch the handle wafer layer (Unaxis SLR-770 ICP Etcher), the Oxford Cobra ICP etcher is used for etching the device silicon layer. The modified nanofabrication process is shown in Fig. 4.7. Note that the discussed nanofabrication process does not cover electrode exposure or platinization as that is discussed in detail in other work [84].

4.4 Results

The neural probes were fabricated in a 180 nm 1P6M SOI-CMOS process and shown in Fig. 4.8. The probes are designed to have a probe length and width of roughly 2900 µm and 110 µm respectively. Neural probes consist of four microcoils using the bottom four metal layers to produce 52 total turns with dimen-

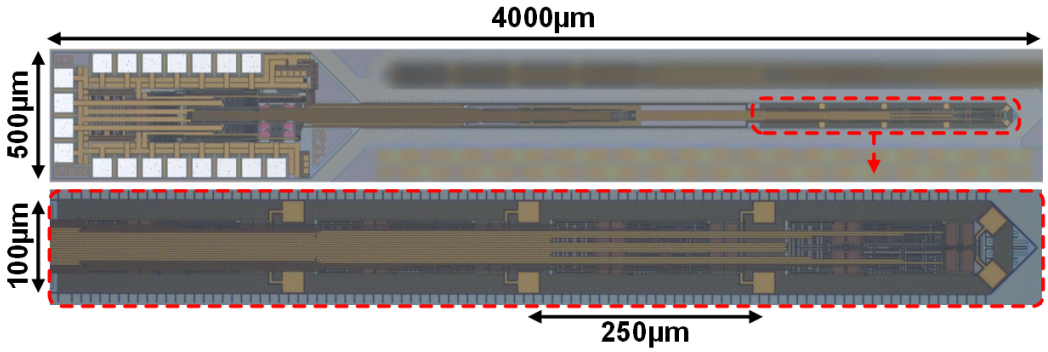

Figure 4.8: Micrograph of an unreleased neural probe and stimulation sites.

sions of 250 × 100 µm. The deep trench isolation layer is used to break up device silicon substrate layer underneath the micro-coils in 10 µm pitch segments. This can potentially improve stimulation efficiency at higher frequencies by reducing the effect of induced eddy currents in the substrate. Furthermore, the supply traces are routed as twenty alternating VDD/GND traces in the middle of the probe to ensure that the supply currents do not produce unintended magnetic fields.

The neural amplifiers are placed inside the micro-coils to minimize the routing distance between the electrode sites and the amplifier inputs. The foundry nanofabrication process utilized high-density metal-insulator-metal (MIM) capacitors that used four metal layers. Therefore, the electrodes could no longer be integrated onto the AC-coupling capacitor of the neural amplifier as seen in other work [60,83]. The top metal layer is used for creating the electrode and for routing to the neural amplifier. A metal layer between the electrode and micro-coil is used as a ground shield to reduce electrical coupling from the micro-coil to the electrode during stimulation. The micro-coil drivers are spaced 500 µm away from micro-coil array to ensure that no inadvertent current flow through the micro-coil drivers impact the induced E-fields above the micro-coils.

While the neural probes have been fabricated, the performance of the probes has not been electrically verified in a test bench environment. However, an earlier iteration of the probes consisting of the micro-coil drivers has been characterized on a lab bench. While this iteration is missing the neural amplifiers and electrodes, the placement of the micro-coils and drivers are identical, yielding results that can be expected from the most recent neural probe iteration. The tested probes have not been released from the original chip packaging. Therefore, the micro-coil characterization consists of measurements from unreleased probes while the neural amplifier characterization will consist of Cadence simulations.

4.4.1 Micro-coil Characterization Measurements

Unreleased micro-coils are characterized by sweeping a DC input stimulation current and measuring the differential micro-coil voltages to determine the maximum stimulation current before micro-coil driver saturation. Current-voltage plots are shown in Fig. 4.9 for input current gain settings of 1x, 2x, and 3x with two of the four micro-coils active. The plots show a maximum input current of 390 µA, 190 µA, and 130 µA respectively, each corresponding to a maximum current-turns product of approximately 200 mA. Note that this is a 47% improvement from prior multi-turn micro-coil work, suggesting there is a significant improvement in the maximum induced E-field when using a high voltage process [129]. Comparisons between the proposed neural probe and prior work are summarized in Table 4.1.

The current consumption of the neural probe is shown for the three gain set-

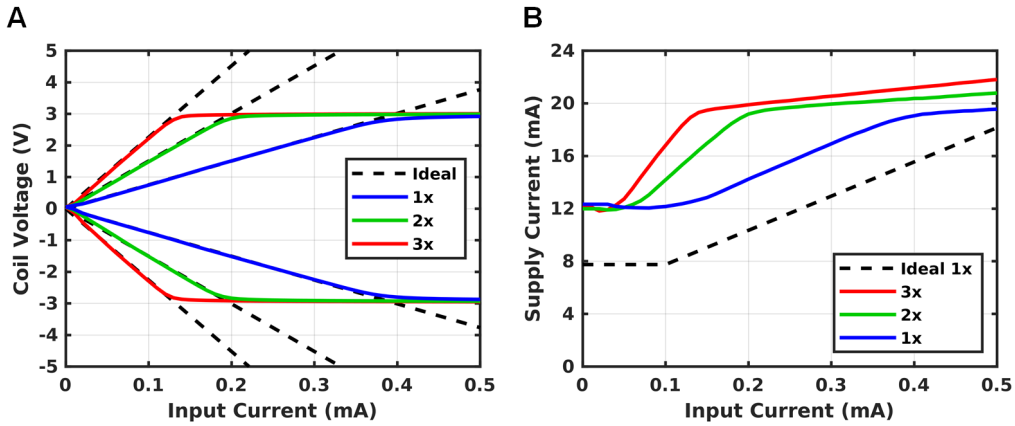

Figure 4.9: Micro-coil characterization measurements. (A) Measured differential micro-coil voltages across the input stimulation current under all programmable current amplifier gain settings. (B) Current consumption of the neural probe under all current gain settings.

tings as well as the simulated 1x gain setting when there is no micro-coil driver output saturation. The quiescent bias current of the micro-coil driver dominates the current consumption at lower input current values. There is a roughly 4.25 mA difference between the simulation and measured 1x gain setting supply currents. This can be attributed to the fabricated neural probe transistors operating closer to the worst-case power consumption process corner where the overdrive voltages of the transistors are lower than expected. The operating process corner also explains why the measured maximum current-turns product is higher than the coil optimization prediction. Future iterations can implement power gating to eliminate the quiescent bias current on unused micro-coil drivers [59,135].

Table 4.1: Comparison With Prior Programmable Micro-coil Neurostimulators

Reference	[130] NER'21	[129] BioCAS'21	**This Work**
Technology (nm)	180	180	**180 SOI**
Supply (V)	2.5	3.5	**10**
Topology	Programmable Micro-coil	Multi-turn Micro-coils	**Multi-turn Micro-coils**
Coil Turns	1	16	**52**
Maximum Coil Current (mA)	200	8.5	**3.9**
Maximum Current-Turns Product (mA)	200	136	**203**

4.4.2 Neural Amplifier Simulation Performance

Due to the uncertainty of the stimulation artifacts produced from micro-coil-based magnetic neurostimulation in the used SOI-CMOS process, the neural amplifier is designed for flexibility. The differential output of the amplifier is buffered by a pair of PFET source followers as the output is routed down the probe before being multiplexed off-chip. All measurements are shown with the measured signals at the output of the PFET source followers. The supply voltage, bias currents, and bias voltages are all generated off-chip to allow for power, noise, and linearity trade-offs post-fabrication. Fig. 4.10 shows the transfer function and input-referred noise spectrum of the neural amplifier operating at a 1 V supply with the amplifier bias current of 4 µA. Changing the load bias current from 40 nA to 4 µA adjusts the in-band gain from 22 dB down to 7.6 dB. Note that there is a 2.7 dB attenuation caused by the source followers.

The high-pass corner frequency is controlled by the bias voltage on the gate of the pseudo-resistor. Adjusting the bias voltage from 700 mV to 900 mV shows

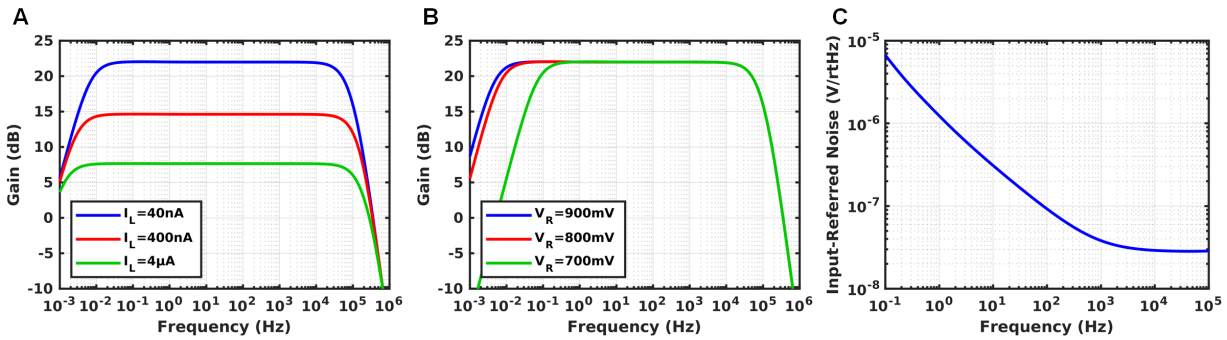

Figure 4.10: Small-signal simulation results for the neural amplifier. (A) Transfer function under varying load bias currents. (B) Transfer function under varying pseudo-resistor bias voltages. (C) Input-referred noise spectral density.

a corner frequency range of 64 mHz to 5 mHz, corresponding to an effective resistance range of 920 GΩ to 12 TΩ. While these corner frequencies are far slower than expected neural signals in the local field potential frequency range, it is important to have such low corner frequencies to shape the thermal noise from the pseudo-resistor completely out of the neural frequency band. The input-referred noise plot is shown in Fig. 4.10C under the nominal amplifier settings (load bias current of 40 nA, pseudo-resistor gate voltage of 800 mV). The integrated input-referred noise from 1 Hz to 10 kHz is 4 μV_{RMS} while consuming 4.5 µW of power. The noise is dominated by the differential inverter input devices with 47% of the noise attributed to their flicker noise and 43% attributed to their thermal noise. Note that the noise floor can be reduced further by utilizing chopping circuit techniques [7, 22, 54, 61, 89].

Fig. 4.11 summarizes the linearity performance of the neural amplifier through power spectral density (PSD) plots. A one-tone test is done with a 30 mV_{pp}, 1-kHz sinusoid to simulate the largest expected differential in-band stimulation artifact. The measured SNDR is 36 dB with the third harmonic as the largest source of distortion. While the amplifier has an in-band 1 dB com-

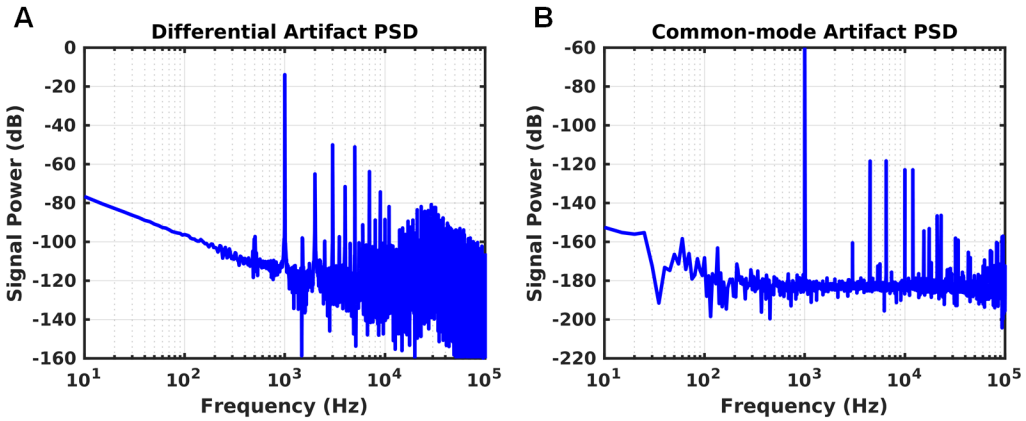

Figure 4.11: Output PSD plots in the presence of large in-band interferers. (A) 30 mV_{pp}, 1-kHz sinusoid differential input. (B) 2 mV_{pp}, 1-kHz sinusoid differential input and 250 mV_{pp}, 5.5-kHz sinusoid common-mode input.

pression point for an input signal of 55 mV_{pp}, expansive nonlinearities start contributing to the output at around 10 mV_{pp}. While this measured SNDR is worse than current state-of-the-art, the stimulation artifact produced by electrical coupling is known and the intermodulation nonlinearities are static. Therefore, if there is no amplifier saturation the SNDR can be improved in post-signal processing [13]. A two-tone test is done with a 2 mV_{pp}, 1-kHz differential signal and a 250 mV_{pp}, 5.5-kHz common-mode signal to simulate the largest expected common-mode stimulation artifact. The measured SNDR is 60 dB with the largest nonlinear terms produced by the second-order intermodulation terms.

4.5 Discussion

4.5.1 Further Reductions in Stimulation Current

While switching to a high voltage process did yield a 49% improvement on the maximum current-turns product for optimized micro-coils with integrated current drivers, this does not overcome the three to four orders of magnitude difference between electrical and magnetic stimulation discussed in prior work [76, 77, 119]. Designing future micro-coil-based neural probes in more modern processes may allow for further marginal improvements as the increased number of available metal layers can increase the micro-coil turns, while increasing the resistance linearly. However, it is unlikely that this approach will reduce the stimulation current to the order of 100 µA. One approach to further reduce the stimulation current is to combine electrical and magnetic stimulation to trade-off between the advantages of both neurostimulation modalities. Another approach is to build upon the neuromodulation technique to target deep brain stimulation through temporally interfering electric fields [44]. Adjacent micro-coils can be modulated with waveforms with frequencies on the order of 1 MHz, significantly higher than the frequencies used for neuromodulation [56], but differ the two frequencies within the dynamic range of neural firing. This allows the sinusoidal stimulation frequencies used in prior work to be generated by frequencies three orders of magnitude larger, and due to the time derivative in the equation for the induced E-field, the magnitude of the E-field will be three orders of magnitude stronger [76, 77, 79, 119].

Table 4.2: Comparison With Prior Neural Recording Front Ends

Reference	[96] JSSC'12	[60] BCAS'13	[22] JSSC'17	[89] JSSC'19	[7] TBCAS'17	[23] JSSC'18	**This Work**
Technology (nm)	65	180	40	180	130	40	**180 SOI**
Supply (V)	0.5	1.8	1.2	1.8	1.2	1.2	**1.0**
Power (µW)	5.04	6.84	2.8	3.2	18	2.8	**4.5**
Bandwidth	200 - 10 kHz	20 - 50 kHz	200 - 5 kHz	200 - 5 kHz	1 - 5 kHz	1 - 5 kHz	**1 - 10 kHz**
INR (μV_{RMS})	4.9	4.3	5.3	2.1	5.0	6.35	**4.0**
NEF	5.99	3.4	4.4	1.56	7.0	1.15	**3.18**
Input Impedance (Ω)	1G	61M*	1.6G	440M	N/A	1.52G	**136M****
Area (mm^2)	0.013***	0.003	0.069	0.200	0.018	0.113***	**0.012**

* Calculated with 2.6 pF input capacitance at 1 kHz.
** Measured at 1 kHz.
*** Area includes ADC.

4.5.2 Neural Amplifier Comparisons

The proposed neural amplifier is compared against state-of-the-art designs that record action potentials in Table 4.2. To minimize the stimulation artifact coupling to the neural amplifier input, the amplifier must fit inside the area of the micro-coils of 0.013 mm^2. Neural amplifiers that utilize circuit techniques to improve their input signal range exceed this area requirement, even though the circuits were designed in a smaller technology node [22, 23]. The proposed amplifier has an area of 0.012 mm^2, with 23% of the area consumed by the source followers to buffer the signals off-chip. The source followers can be replaced with $\Sigma\Delta$- ADCs that can be made to fit in the same area, allowing for local digitization while preventing further sources of coupling from corrupting the recorded neural signals as it is routed along the probe [96].

The stimulation artifacts produced by micro-coil-based magnetic stimulation allows for simpler, and thus smaller, neural amplifier topologies. Recent work has shown a neural recording front end capable of maintaining a signal-

to-interferer ratio of 40 dB in the presence of a 700 mV_{pp} common-mode stimulation artifact with *in vitro* measurements showing suppression of a 381 mV_{pp} common-mode signal [23]. However, electrode stimulation artifacts present at the stimulation sites can be significantly larger than the tested values. Using a traditional neural amplifier topology with common-mode feedback shows a signal-to-interferer ratio of 60 dB in the presence of the maximum expected magnetic stimulation artifact.

4.6 Conclusion

This work proposes a neural probe that builds upon the state of the art in implantable micro-coil-based neurostimulators. The probe is designed in a high voltage SOI-CMOS process to allow for the design of four fifty-two turn micro-coils that are co-optimized with integrated current drivers to maximize the induced E-field and reducing the stimulation current. Recording electrodes are designed over the micro-coil stimulation sites with neural recording amplifiers placed inside the micro-coils, enabling simultaneous stimulation and recording of neural activity near the surface of the probe. The electrical performance of the micro-coil stimulation has been characterized on a lab bench, with future work measuring the neural amplifier performance.

CHAPTER 5

A HIGH-COMPLIANCE CMOS CURRENT DAC

5.1 Introduction

Current mirrors are one of the most important building blocks in analog integrated circuit design as they are used to perform current amplification, biasing, active loading, and level shifting. Current mirrors are constrained by their requirements for accuracy, noise, input/output impedances, and voltage compliance range. These requirements are typically traded-off against each other as noise, accuracy, and impedance are improved by increasing V_{DSAT} of a CMOS current mirror, however increasing V_{DSAT} also increases the necessary minimum voltage across the output of the mirror to maintain accurate mirroring, thus setting the minimum power dissipation. Technology scaling has led towards the trend of reducing the supply voltage, thus increasing the demand of low voltage, low power circuits in radio and biomedical analog front ends [54, 57, 90]. Fig. 5.1 shows a traditional differential amplifier with an active load, requiring $2V_{DSAT}$ of headroom to keep the current sources in saturation. Note that as the supply decreases so does the available headroom, causing the current sources to operate on the transition edge between the saturation and triode regions. This leads to a degradation in the output impedance which negatively impacts performance metrics such as gain, common-mode rejection ratio, and unity gain frequency.

Prior work has improved upon the commonly used low voltage cascode current mirror by utilizing a feedback amplifier to replicate the output voltage of the mirror onto the drain of the mirror reference device [113]. Other work

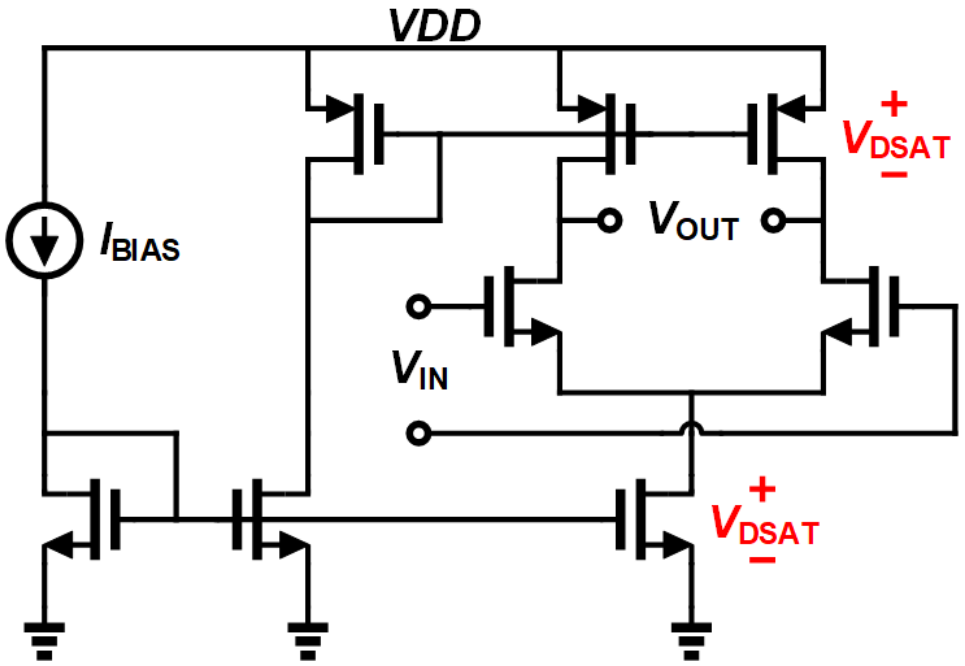

Figure 5.1: Traditional differential amplifier with an active load showcasing the consumed headroom needed for the current sources to remain in saturation.

has explored bulk driven mirror topologies to relax the threshold limitation imposed on the input and output voltages [152]. However, this approach suffers from current offset error, low bandwidth, and higher power consumption [98]. While these disadvantages can be mitigated through the use of feedback amplifiers, this adds to the circuit complexity and significantly increases the total area of the current mirror [127].

The proposed mirror topology is shown in Fig. 5.2 and builds upon the traditional current mirror by adding two additional transistors and an additional reference current. This extends the output voltage range of the current mirror well below V_{DSAT} while maintaining a constant current and no degradation to noise or matching. Transistors M_1 and M_2 form a traditional current mirror with current gain N, implemented such that L_2=L_1 and W_2=NW_1. The two additional transistors, M_3 and M_4, replicate the drain voltage on M_2 onto the drain

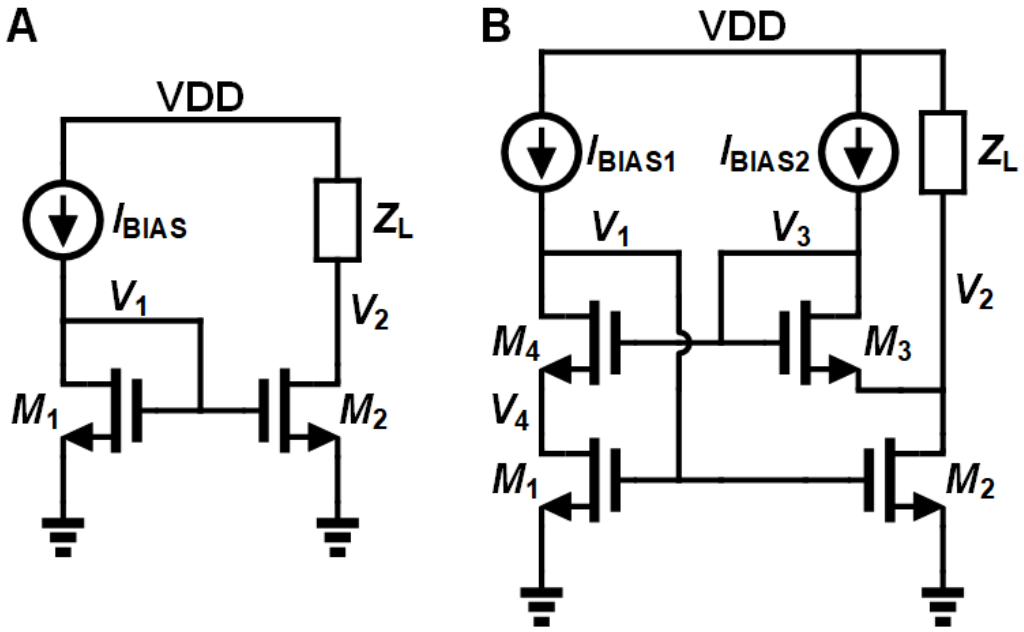

Figure 5.2: Current mirror circuit schematics. (A) Traditional CMOS current mirror. (B) Proposed enhanced CMOS current mirror.

of M_1. Since the mirrored devices also share the same gate-source voltage, this results in M_1 and M_2 maintaining a wide range of accurate mirroring over a wide range of bias conditions, including both saturation and deep triode. This work will discuss the analysis to design the proposed high-compliance current mirror, as well as how to convert the topology into a programmable current digital-to-analog converter (DAC).

5.2 High-Compliance Current Mirror Analysis

5.2.1 First-Order DC Large Signal

The core of the proposed current DAC utilizes a high-compliance current mirror. Transistors M_1 and M_2 share both gate and source nodes. The drain of M_2 is the

output of the current mirror and is also connected to the source of M_3, which is a diode-connected device biased by I_{BIAS2}. By sizing M_3 and M_4 such that V_{GS3}=V_{GS4} while keeping M_4 is in saturation, M_4 behaves as a source-follower and replicates V_2 onto V_4. This is implemented by sizing M_3 and M_4 to the same length and scaling their widths such that W_3/W_4=I_{BIAS2}/I_{BIAS1}. The value of V_1 is set by negative feedback as I_{D4}=I_{D1} and any difference between I_{D1} and I_{BIAS1} will charge or discharge the gate capacitances of M_1 and M_2, adjusting V_1 such that I_{D1} balances towards I_{BIAS1}.

The large signal DC analysis begins by defining the overdrive voltage on M_1 and M_2 in saturation as V_{DSAT}=$(I_{BIAS1}/k_1)^{1/2}$. When V_2¡V_{DSAT} both M_1 and M_2 operate in triode their behavior can be approximated using the square-law model:

$$I_{D2} = Nk_1(V_1 - V_{TH} - V_2/2)V_2 \tag{5.1}$$

$$I_{D1} = Nk_1(V_1 - V_{TH} - V_4/2)V_4 \tag{5.2}$$

Since V_2=V_4, then V_1 settles to a value where I_{D1}=I_{BIAS1} and I_{D2}=NI_{BIAS1} calculated by:

$$V_1 = V_{TH} + \frac{V_2}{2} + \frac{V_{DSAT}^2}{V_2} \tag{5.3}$$

Thus, the feedback causes V_1 to increase to compensate for the decreased value of V_2. Under the condition where V_3-V_1¡V_{TH}, M_4 enters triode and V_4 no longer tracks V_2. However, provided that $(I_{BIAS2}/k_3)^{1/2}$¡V_{TH}, M_1 and M_2 will be

operating in saturation where the mirror performance is relatively insensitive to V_2. Note that the circuit ultimately fails when V_1 approaches the supply voltage VDD, thus saturating the current source I_{BIAS1}. However, second-order effects become dominant well before this failure mode and will be discussed in future sections.

5.2.2 Small Signal

The complete small signal model of the proposed current mirror is presented in Fig. 5.3. The general circuit behavior can be translated to an effective output impedance relating V_2 to I_2. Assuming that M_3 and M_4 operate as an ideal voltage replica between V_2 and V_4 and the mirror has a current gain of N, the relationship between V_2 and I_2 can be simplified to the following expression:

$$\frac{I_2}{V_2} = \frac{sN(N+1)(sC_{GD1}C_{GS1} + g_{m1}C_{GD1} + C_{GD1}/r_{O1} + C_{GS1}/r_{O1})}{g_{m1} + s([N+1]C_{GS1} + NC_{GD1})} \tag{5.4}$$

The equivalent RC circuit for this expression is shown in Fig. 5.3B where:

$$C_1 = N(N+1)\left(C_{GD1} + \frac{C_{GD1} + C_{GS1}}{g_{m1}r_{O1}}\right) \tag{5.5}$$

$$C_2 = \frac{NC_{DS1}C_{GS1}}{NC_{DS1} + (N+1)C_{GS1}} \tag{5.6}$$

$$R_S = \frac{NC_{GD1} + (N+1)C_{GS1}}{N(N+1)(g_{m1}C_{GD1} + C_{GD1}/r_{O1} + C_{GS1}/r_{O1})} \tag{5.7}$$

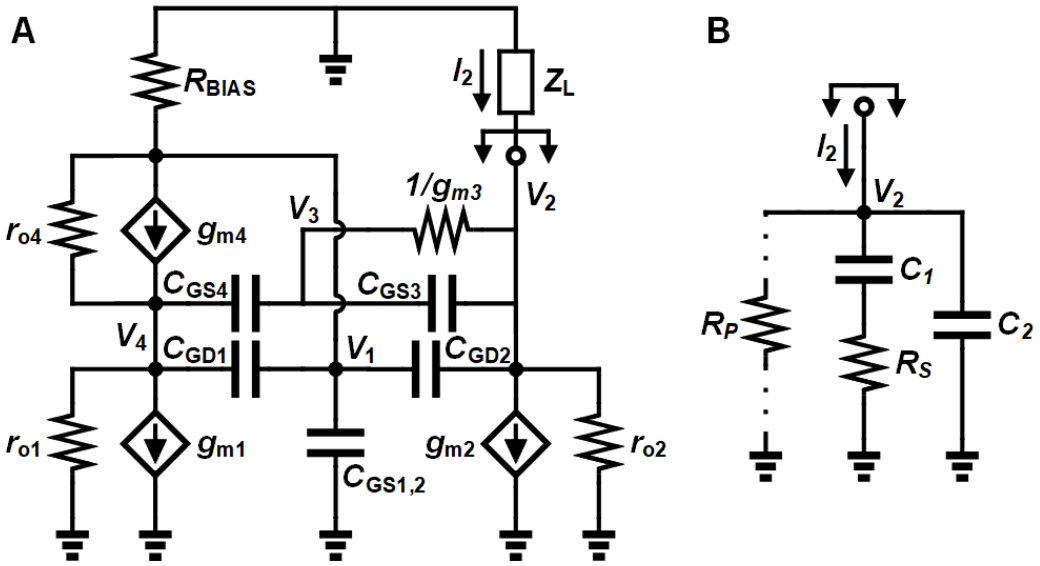

Figure 5.3: Small signal circuit model for the enhanced current mirror. (A) Small signal model of complete transistor circuit. (B) Equivalent output impedance model assuming $V_2 \approx V_4$.

While this simplification is imperfect, it shows that the main positive feedback loop only operates for frequencies less than $1/(R_S C_1) \sim \omega_T/N$, where ω_T is the unity current gain frequency for M_1 and M_2. This implies that delays caused by M_3 and M_4 are only relevant if there are strong effects below this frequency. However, since the largest capacitances associated with these transistors (C_{GS3} and C_{GS4}) operate to increase the coupling between V_2 and V_4, the capacitances should act to enhance the operation of the circuit at higher frequencies, as opposed to introducing delay. Ideally R_P, the low frequency output impedance, should be infinite. However, as will be shown later in this work, the value will depend upon a variety of second order effects.

5.2.3 Mismatch and Output Resistance

Mismatch between transistors can be well approximated as being completely due to V_{TH} mismatch. The two important matching parameters are between transistor pairs M_1, M_2 and M_3, M_4. Therefore, these mismatches can be modeled into two voltage deviations: ΔV_2=V_{TH2}-V_{TH1} and ΔV_4=V_{TH4}-V_{TH3}. The impact of ΔV_2 on the output current I_O is given by ΔI_O=$\Delta V_2 N g_{m1}$, which is the same behavior observed in an unenhanced current mirror. However, ΔV_4 has the effect of slightly mismatching V_{DS1} relative to V_{DS2} where the effect becomes proportionally stronger with V_2. Combining these effects shows that ΔI_O has the following dependency on V_2, ΔV_2, and ΔV_4:

$$\frac{\Delta I_O}{I_O} = \Delta V_2 \frac{2V_2}{V_{DSAT}^2} + \Delta V_4 \left(\frac{1}{V_2} - \frac{V_2}{V_{DSAT}^2} \right) \tag{5.8}$$

The derived expression shows a DC dependence of I_O on V_2 implying there is a finite real impedance on the output node of the enhanced mirror. The equivalent conductance due to mismatch can be calculated by taking the derivative of ΔI_O with respect to V_2, yielding the following expression:

$$g_{OUT} = I_O \left(\frac{2\Delta V_2}{V_{DSAT}^2} - \frac{\Delta V_4}{V_{DSAT}^2} - \frac{\Delta V_4}{V_2^2} \right) \tag{5.9}$$

Note that the modeled mismatch in ΔV_2 and ΔV_4 can be either positive or negative, and therefore g_{OUT} can also take on either sign. Furthermore, other forms of mismatch can be described as mismatch in k, which can also be incorporated into this framework. Mismatch between k_3 and k_4 will attribute to a shift in V_{GS3} relative to V_{GS4} and is modeled within the value of ΔV_4. Mismatch

between k_1 and k_4 behaves as a change in the mirror ratio and has no additional effect on g_{OUT}.

The output resistance of M_4 can influence the effective output resistance of the enhanced mirror. When V_{DS4}=V_1-V_2 is not equal to V_{DS3}, the output resistance of M_4 generates the following effective voltage mismatch:

$$\Delta V_{4RO} = \frac{V_1 - V_2 - V_{GS3}}{r_{O4} g_{m4}} = \frac{V_{TH} - V_{GS3} - V_2/2 + V_{DSAT}^2/2V_2}{r_{O4} g_{m4}} \tag{5.10}$$

Note that since V_{GS3}¿V_{TH} the effective voltage mismatch from r_{O4} will take on negative values when M_2 enters triode, and then become increasingly positive as V_2 approaches zero. The resulting output conductance is as follows:

$$g_{OUT} = \frac{-I_O}{r_{O4} g_{m4}} \left(\frac{V_{GS3} - V_{TH}}{V_2^2} + \frac{V_{GS3} - V_{TH}}{V_{DSAT}^2} + \frac{V_2}{V_{DSAT}^2} - \frac{V_{DSAT}^2}{V_2^3} \right) \tag{5.11}$$

Similarly to the expression for ΔV_{4RO}, g_{OUT} also takes on negative values as V_2 falls below V_{DSAT} then becomes positive as V_2 continues to decrease.

The final source of contributing to the output resistance of the enhanced mirror is the output resistance of the current source I_{BIAS1}. This is reflected to the output as a function of V_1, resulting in an increasing output conductance as V_2 decreases in the following expression:

$$g_{OUT} = -\frac{N}{R_{BIAS1}} \frac{dV_1}{dV_2} = \frac{N}{2R_{BIAS1}} \left(\frac{V_{DSAT}^2}{V_2^2} - 1 \right) \tag{5.12}$$

Each of the previously discussed effects on output impedance (ΔV_2, ΔV_4, r_{O4}, R_{BIAS1}) can be modelled as parallel conductances. The terms that limit the

operating range of the enhanced current mirror are r_{O4} and R_{BIAS1} since they lead to a decreased output impedance as V_2 decreases. Furthermore, the operating range can be further limited by the worst-case values of ΔV_2 and ΔV_4.

5.2.4 Stability

Since ΔV_2 and ΔV_4 can each be positive or negative values, and ΔV_{4RO} can be negative for some values of V_2, it is possible for the DC output resistance of the enhanced current mirror to be a negative value. This can potentially lead to instability if the magnitude of the real part of the load impedance presented to the mirror is larger than the magnitude of this effective negative output resistance. Specifically, stability is guaranteed if the load resistance meets the following requirement:

$$R_L < \frac{1}{g_{m2}} \frac{V_{DSAT}}{|\Delta V_2| + |\Delta V_4| - \Delta V_{4RO}} \tag{5.13}$$

Note that for most biasing scenarios, such as generating tail currents, this requirement is easily met as $V_{DSAT} >> |\Delta V_2| + |\Delta V_4|$ and R_L is usually on the order of $1/g_{m2}$. However, for other current driving scenarios, such as driving high resistance multi-turn micro-coils, this requirement must be checked.

5.2.5 Noise

Noise in the enhanced mirror is not substantially worse than it would be if it was unenhanced ($V_2 > V_{DSAT}$) with only a slight degradation due to noise from I_{BIAS2}.

As V_2 decreases beneath V_{DSAT}, V_1, which increases the channel conductance and the thermal noise current on the drains of transistors M_1 and M_2. Note that the thermal noise current is roughly proportional to the channel conductance, which is roughly proportional to V_1-V_{TH}. Therefore, the thermal current noise i_d^2 increases roughly proportional to V_1-V_{TH} [138]. Flicker noise experiences an opposite effect as flicker noise will decrease as V_{DS} decreases, even if I_D remains constant [55]. Thus, the noise changes as V_2 decreases and V_1 correspondingly increases, however this change depends on the noise mechanism and upon the degree to which the enhanced current mirror is driven into triode.

5.3 Simulation Results

The proposed enhanced current mirror and a traditional mirror are simulated in Cadence using 180 nm NMOS transistors. The devices are sized to have V_{DSAT} = 200 mV for a bias current of 20 µA. To model the previously discussed mismatch, voltage sources are added the sources of M_2 and M_4 to emulate mismatch between the transistor pairs. Fig. 5.4 shows the output current as well as the output conductance g_{OUT} over a varying load voltage. The dashed lines indicate the range ±10 mV of perturbation on the source of M_2, showing that mismatch mainly impacts the current mirroring accuracy. The headroom improvement produced by the enhanced current mirror provides an equivalent current at a load voltage of 35 mV to the traditional current mirror at a load voltage of V_{DSAT} = 200 mV, yielding over a factor of 5.7 improvement.

Fig. 5.5 compares how ΔV_2 and ΔV_4 vary from each other. While ΔV_2 mostly impacts the mirroring accuracy, there is still minor effects to the en-

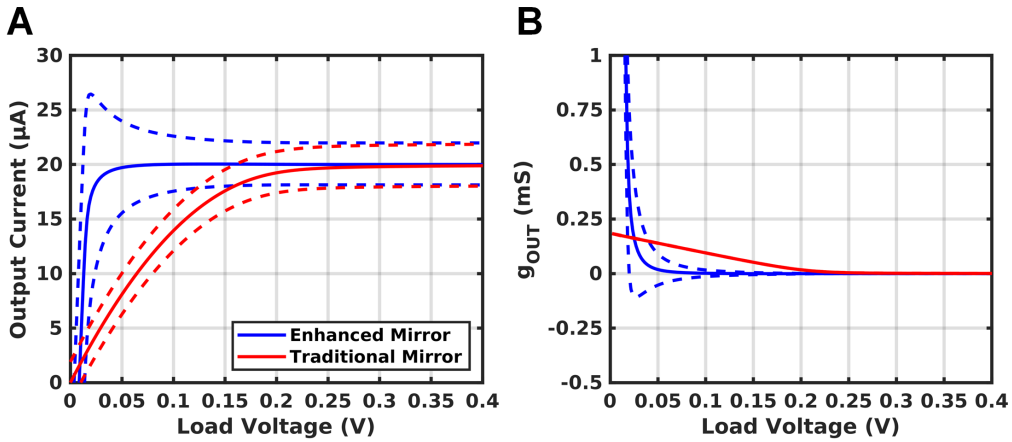

Figure 5.4: Simulation results comparing the enhanced current mirror to a traditional current mirror. (A) I-V curves over varying load voltage. (B) g_{OUT}-V curves. Dotted lines indicate bounds produced by ΔV_2 ranging from ±10 mV.

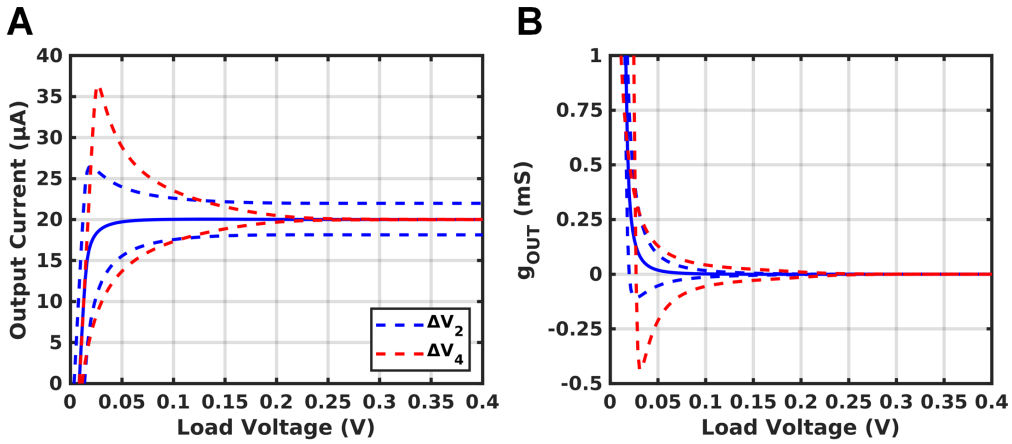

Figure 5.5: Simulation results comparing the impact of ΔV_2 and ΔV_4 on the enhanced current mirror. (A) I-V curves over varying load voltage. (B) g_{OUT}-V curves. Dotted lines indicate bounds produced by ΔV_2 and ΔV_4 ranging from ±10 mV.

hanced compliance region, potentially causing g_{OUT} to go negative for low load voltages. Meanwhile, ΔV_4 has no impact on the mirroring accuracy when the load voltage is greater than V_{DSAT}. However, as this mismatch contributes to inaccuracies between the voltage replication of V_2 onto V_4, ΔV_4 has a stronger impact on the mirroring accuracy when the load voltage is less than V_{DSAT}, capable of producing larger negative values for g_{OUT}.

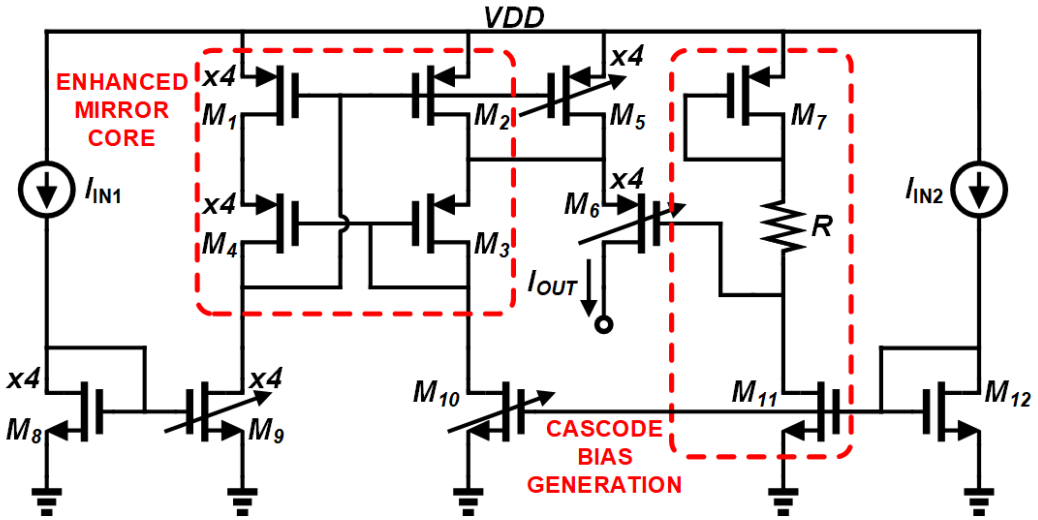

Figure 5.6: Proposed current DAC circuit schematic with enhanced current mirror core.

5.4 Proposed High-Compliance Current DAC

The proposed current DAC is shown in Fig. 5.6 and utilizes a PFET configuration of the previously mentioned high-compliance current mirror. The feedback circuitry of the high compliance mirror is sized to be one quarter of the width of the mirroring transistors to reduce the static power consumption. The gate, source, and drain of the enhanced mirror core output device M_2 are connected to a 4-bit binary weighted PFET current DAC. Since the enhanced mirror reverts back to a traditional current mirror for load voltages larger than V_{DSAT}, a programmable bank of cascode transistors (denoted as M_6) are added to match the digital DAC setting of M_4 to ensure accurate mirroring over a wide range of load voltages. Note that as the load voltage approaches the supply voltage, M_6 will fall into extreme triode and will have minimal impact on the current DAC output.

To add more range to the current DAC the input current sources are mirrored

onto a pair of NFET current DACs to supply I_{BIAS1} and I_{BIAS2} to the enhanced mirror. This is implemented as a 2-bit DAC capable of multiplying the input current by an integer value from 1 through 4. Due to the sizing difference in the enhanced current mirror, I_{IN1} must be four times larger than I_{IN2}. Furthermore, I_{IN2} is copied over to produce the PFET cascode bias voltage using a diode-connect PFET transistor and resistor. Additional switching circuitry is added to the schematic to disconnect transistor M_3 from the enhanced current mirror, thus breaking the feedback loop, and adding the appropriate connections to revert the mirror to a traditional cascoded current mirror. Furthermore, to mirror can operate as a traditional current mirror by setting I_{IN2} to a sufficiently large value to have the cascode devices operate in severe triode.

5.5 Measurements

The proposed high-compliance current DAC was fabricated in a 180 nm CMOS process. The micrograph of the circuit is shown in Fig. 2.4. The entire circuit, including bond pads, consumes 400 µm × 645 µm, with the current DAC only consuming an area of 252 µm × 48 µm. Note that half this area is dedicated to the switching networks to change the enhanced current mirror to the traditional current mirror.

Fig. 5.8 shows the measured output current and output conductance across the load voltage, which is defined as the difference between the supply and output voltages. I_{IN1} and I_{IN2} are set to 20 µA and 5 µA respectively with the PFET and NFET DAC settings set to unity current gain. The enhanced mirror is capable of achieving an output current of 19.3 µA with a load voltage of only 15 mV,

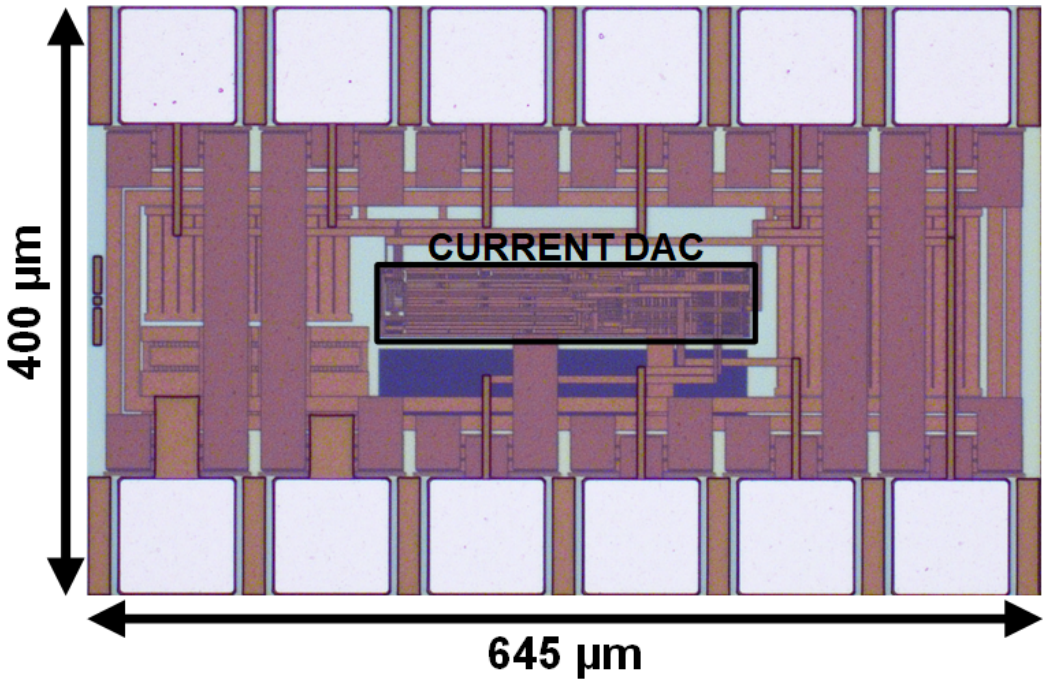

Figure 5.7: Chip micrograph.

the equivalent output current value when the cascoded current mirror has a load voltage at the designed V_{DSAT} of 200 mV. This is achieved while minimizing the overshoot current to 250 nA. The output conductance plots (achieved by taking the derivative of the measured output current data with respect to the load voltage) shows that the output impedance is significantly improved for the enhanced mirror as the load voltage decreases beneath V_{DSAT}. Note that the output conductance value of the enhanced mirror achieves a minimum value of −3.7 µS for a load voltage of 65 mV. Fig. 5.9 shows the impact of changing the value of I_{IN2}, the bias current used for the feedback path in the enhanced mirror. The differences in I_{IN2} to its nominal value creates offset current errors for load voltages approaching and surpassing V_{DSAT}. Lower values of I_{IN2} increases the overshoot for low load voltage, causing stability concerns, while higher values of I_{FB} decreases the range of voltages for accurate current mirror while guaranteeing stability for all loads.

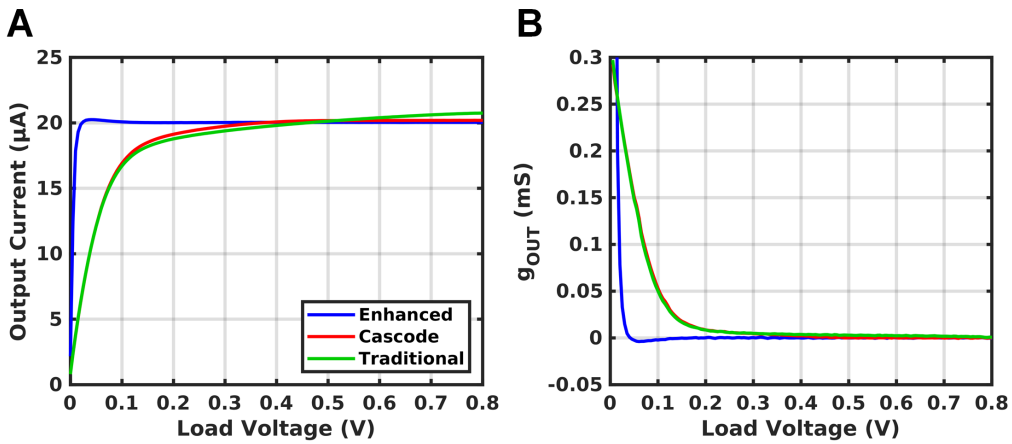

Figure 5.8: Measured performance of enhanced current mirror, cascoded current mirror, and traditional current mirror. (A) I-V curves over varying load voltage. (B) g_{OUT}-V curves. The load voltage is defined as the difference between the supply and output voltages.

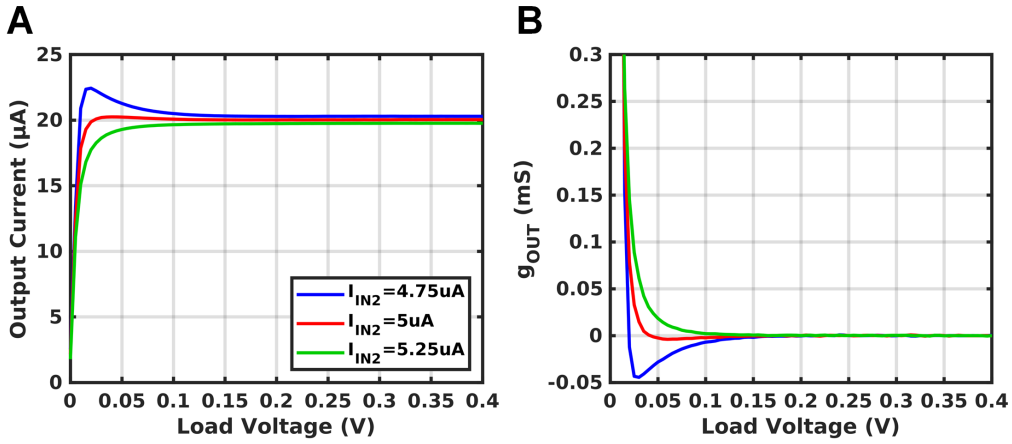

Figure 5.9: Measured performance of enhanced current mirror with varying I_{IN2}. (A) I-V curves over varying load voltage. (B) g_{OUT}-V curves. The load voltage is defined as the difference between the supply and output voltages.

Fig. 5.10 shows the current output across the load voltage for various current gain settings for the PFET and NFET DACs. Across all PFET current DAC settings the I-V curve maintains a similar shape with the output current value amplified by the DAC value. However, the NFET DAC shows that as the current gain value increases the duration of the range of the load voltage with accurate mirroring decreases. This is due to the increased current values increasing the

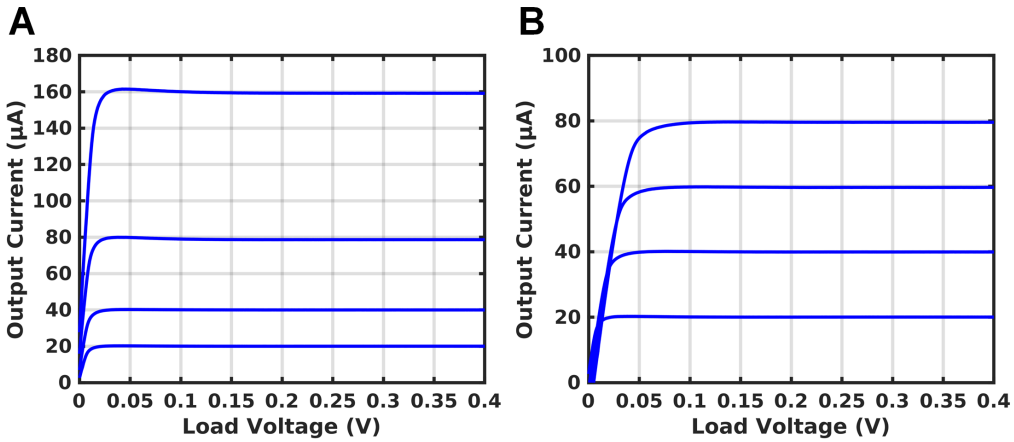

Figure 5.10: Enhanced current mirror output current across load voltage. (A) PFET DAC settings for current gain values of 1, 2, 4, and 8. (B) NFET DAC settings for current gain values of 1, 2, 3, and 4. The complimentary DAC is set to unity current gain.

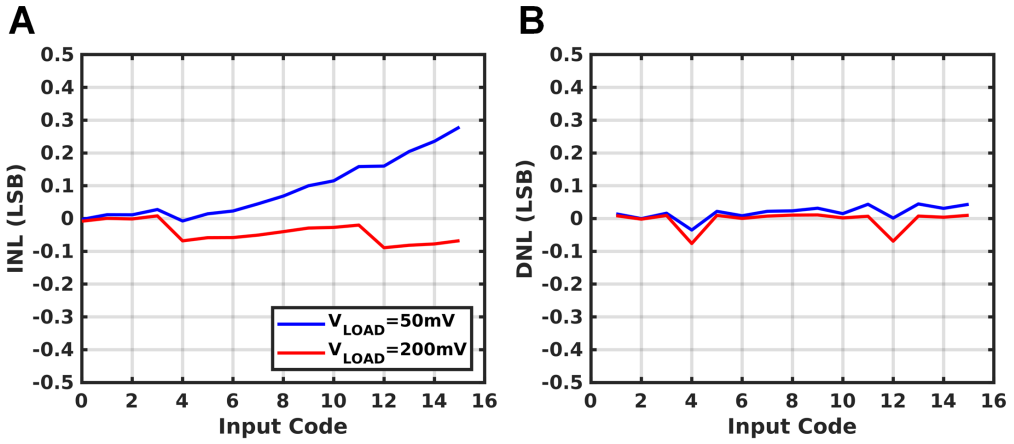

Figure 5.11: Linearity performance of the enhanced PFET current DAC. (A) INL. (B) DNL. NFET current DAC set to unity current gain.

value of V_{DSAT} of the enhanced current mirror devices. The linearity performance of the 4-bit PFET enhanced DAC is summarized in Fig. 5.11. The INL and DNL are compared for load voltages of 50 and 200 mV to compare when the mirroring transistors in the enhanced DAC are operating in triode and in saturation. The INL tends to degrade when the enhanced mirror is operating in triode for larger input codes as the overshoot of the output current increases.

This can be attributed to mismatch between the transistors within the DAC as the larger codes tend to undershoot the correct output current when operating in saturation.

5.6 Conclusion

This work presents a simple enhancement to the standard CMOS current mirror that extends its operational range well below the V_{DSAT} of the devices with minimal addition to power, area, and circuit complexity. Analysis is done to discuss the improvements over the traditional current mirror, as well as the limitations of the enhanced mirror topology. The enhanced current mirror is then expanded upon to be a current DAC, while designing switchable circuitry to draw direct comparisons to the traditional and cascoded current mirror. Measurements show accurate current mirroring down to a supply-load voltage difference of 25 mV with the mirroring transistors operating with a V_{DSAT} of 200 mV.

CHAPTER 6

DESIGN AND ANALYSIS OF BASEBAND CIRCUIT TECHNIQUES TO ENHANCE CHANNEL SELECTIVITY IN PASSIVE MIXER-FIRST RECEIVERS

6.1 Introduction

As the number of wireless devices continues to grow, future wireless receivers require stringent interference tolerance as the likelihood of data corruption from strong out-of-band (OOB) blockers increases, while also remaining flexible to use any available space on the wireless spectrum. Furthermore, higher data rates are desired, necessitating an increase in channel bandwidth while reducing the guard bands used for filtering [85, 86, 95]. Historically, surface acoustic wave (SAW) and film bulk acoustic resonator (FBAR) filters have been used for their high linearity when suppressing OOB blockers. However, these filters are not tunable, have a large area footprint, increase the cost of each receiver, and introduce 1-3 dB in-band loss. Therefore, it is much more desirable to design SAW-less wireless receivers utilizing CMOS technology and integration.

Software-defined radio front ends have utilized passive mixer-first receivers (also known as N-path filters) as they offer necessary characteristics for next-generation wireless receivers. While the CMOS passive mixer has been known for some time [68,93,151], deep sub-micron CMOS technology has enabled them to displace traditional active mixers in many applications [5, 9, 25, 31, 148, 150]. Much of the initial work on such circuits have shown promise in the 100 MHz to low GHz bands and have mostly employed simple single-pole RC loading to generate a one-pole roll-off [5,27,32,101,147], which is upconverted to a second-

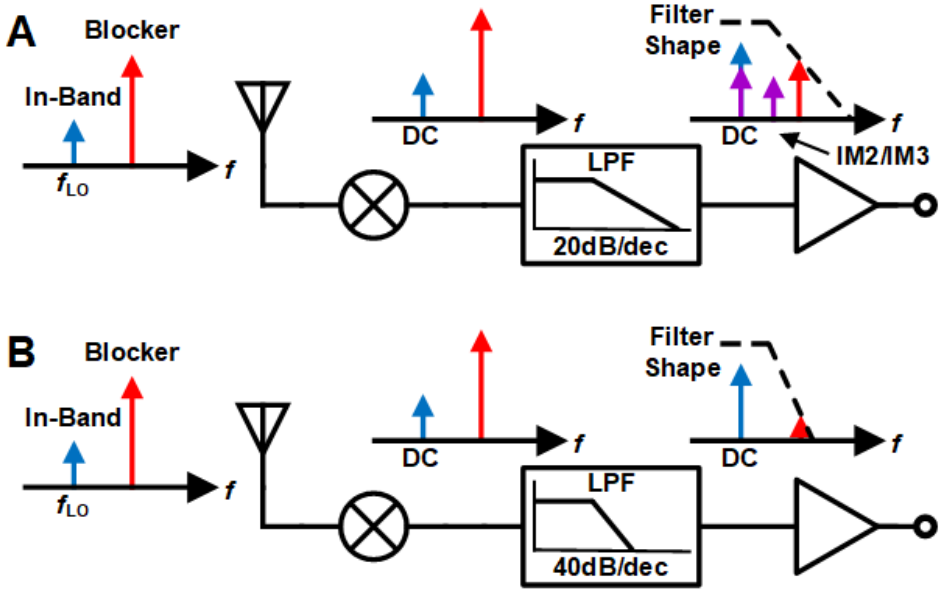

Figure 6.1: Signal spectrum through passive mixer-first receiver system of (A) a tradition single-pole baseband low pass filter (LPF) where band-edge blockers create intermodulation (IM) terms and (B) an enhanced baseband LPF that suppresses the band-edge blocker enough to eliminate the IM terms.

order bandpass filter (BPF) centered around the switching frequency. Most such circuits have been less successful at reaching higher frequencies while maintaining sufficient linearity, acceptable noise, and good close-in interferer tolerance.

A more crowded and dynamic wireless spectrum requires flexible receivers capable of covering a wider range of frequencies with sharper selectivity to allow alternate-channel suppression and linearity comparable with fully OOB signals. Fig. 6.1 shows how band-edge blockers can produce significant distortion products in the receiver band. Past work has improved the RF filter selectivity, and thus extend linearity, by cascading N-path filters, coupled together through g_m cells [32]. While this approach realized a sixth-order BPF, the g_m cells limit the achievable linearity. Other work has also explored using g_m–C filtering to achieve enhanced selectivity; however, this suffers from insufficient band-edge linearity [27]. Finally, higher-order RF filtering has been shown by cascading

two passive BPF stages while also implementing a bottom-plate mixing technique [87]. However, the technique results in large parasitic capacitance at the RF input, causing signal loss, leading to poor noise figure (NF) and limited RF frequency range.

To enhance linearity and channel selectivity it is ideal to suppress OOB interferers at the RF input without generating large voltages on internal nodes of the baseband circuitry at OOB frequencies. This is accomplished by modifying the baseband filter topology seen in passive mixer-first receivers [5]. While some topologies have proposed a higher than one-pole baseband filter roll-off, the design trades-off between the filter sharpness at the band edge and the duration of the enhanced roll-off [125]. To maximize the receiver's ability to suppress close-in OOB blockers, the baseband filter must maintain enhanced roll-off until the baseband impedance is significantly less than the on-resistance of the mixer switches. This work proposes two distinct baseband circuit topologies that generate higher-order baseband impedance roll-off, resulting in higher-order RF band-pass filtering in passive mixer-first receivers: 1) positive capacitive feedback similar to [71, 88] and 2) an active shunting notch circuit similar to [1]. Compared to [131], this work will discuss the filter concepts in more depth, analyze the filter transfer function, and explore trade-offs regarding noise and linearity.

6.2 Receiver Architecture

Improving the IIP3 and compression point of the RF receiver requires strong OOB blockers to be rejected at the beginning of the receiver system with steep

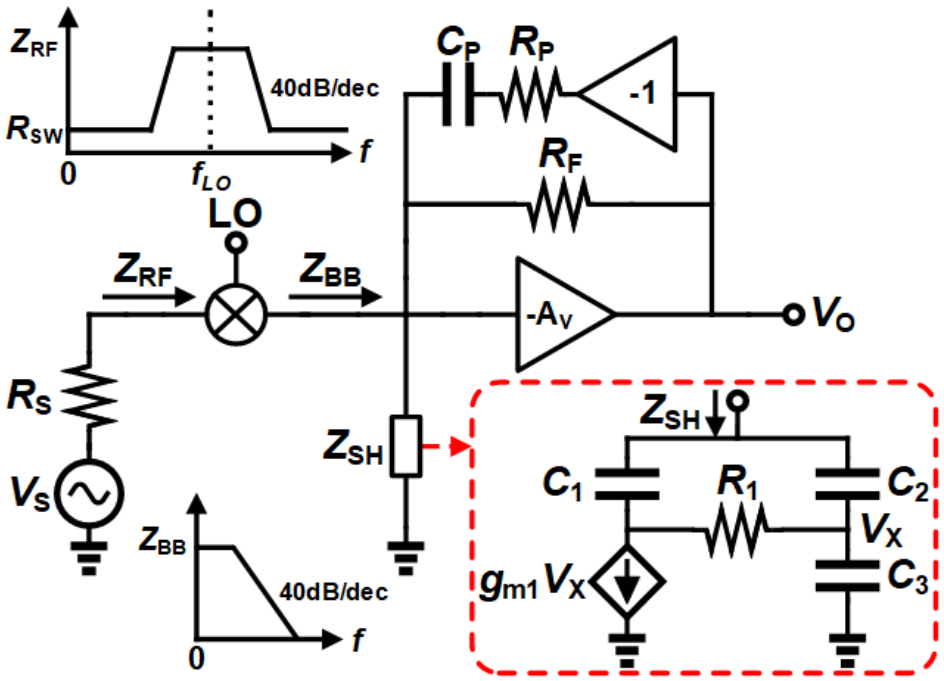

Figure 6.2: High-level diagram of the proposed receiver with both enhanced selectivity techniques shown.

filtering. While this is traditionally accomplished with SAW filters at the RF input, the proposed solution utilizes CMOS technology scaling and passive-mixer first receivers to overcome the disadvantages associated with large, static filters. Traditional passive-mixer first receivers achieve this by the shunt capacitance interacting with the source impedance through the passive mixer to obtain RF filtering [5, 27, 32, 101, 147]. The resulting baseband first-order LPF is frequency shifted to a second-order RF bandpass filter (BPF), centered around f_{LO}. Low-noise impedance matching is done by utilizing the Miller effect with a high R_F value around the baseband amplifier, modeled as an ideal amplifier (infinite input impedance, no output impedance) with finite gain A_V [5].

Fig. 6.2 shows two distinct techniques how second-order baseband LPF can be achieved, thus being shifted by the passive mixer to a fourth-order RF BPF centered around f_{LO}. The first proposed technique utilizes positive capacitive

feedback (similar to [88]) to extend the bandwidth of the filter. Z_{SH} is configured to be a traditional shunting capacitance and the positive feedback creates negative capacitance, cancelling the shunting capacitance at the filter corner frequency, thus effectively extending its bandwidth while creating a second-order LPF. R_P is added to the positive feedback path to limit the frequency range of the positive feedback to improve stability and receiver performance (discussed in detail later in this work).

The second proposed technique utilizes an active shunting notch to achieve the second-order baseband LPF. In this configuration the positive capacitive feedback path is disabled and Z_{SH} is configured as the circuit shown in Fig. 6.2. An active inductor is created with components R_1, C_3, and g_{m1} to create a resonant notch circuit with C_1. However, this would also create a resonant peak when interacting with the parasitic shunting capacitance on the input of the baseband amplifier. Therefore, C_2 is added to the circuit to effectively create a frequency-limited active inductor.

6.3 Circuit Implementation

The proposed receiver architecture is shown in Fig. 6.3, comprising two chips: an LO and mixer chip, and a baseband filter chip. The quadrature LO pulse generation circuitry (seen in [94]) drives the mixers with 4-phase 25% duty-cycle clock pulses. These pulses are generated from a $2f_{LO}$ that is first divided by two using a Johnson counter using high-speed emitter-coupled logic (ECL) before passing to high-speed ECL AND gates to produce the 4-phase waveforms. The clock pulses are finally amplified with push-pull drivers to provide sufficient

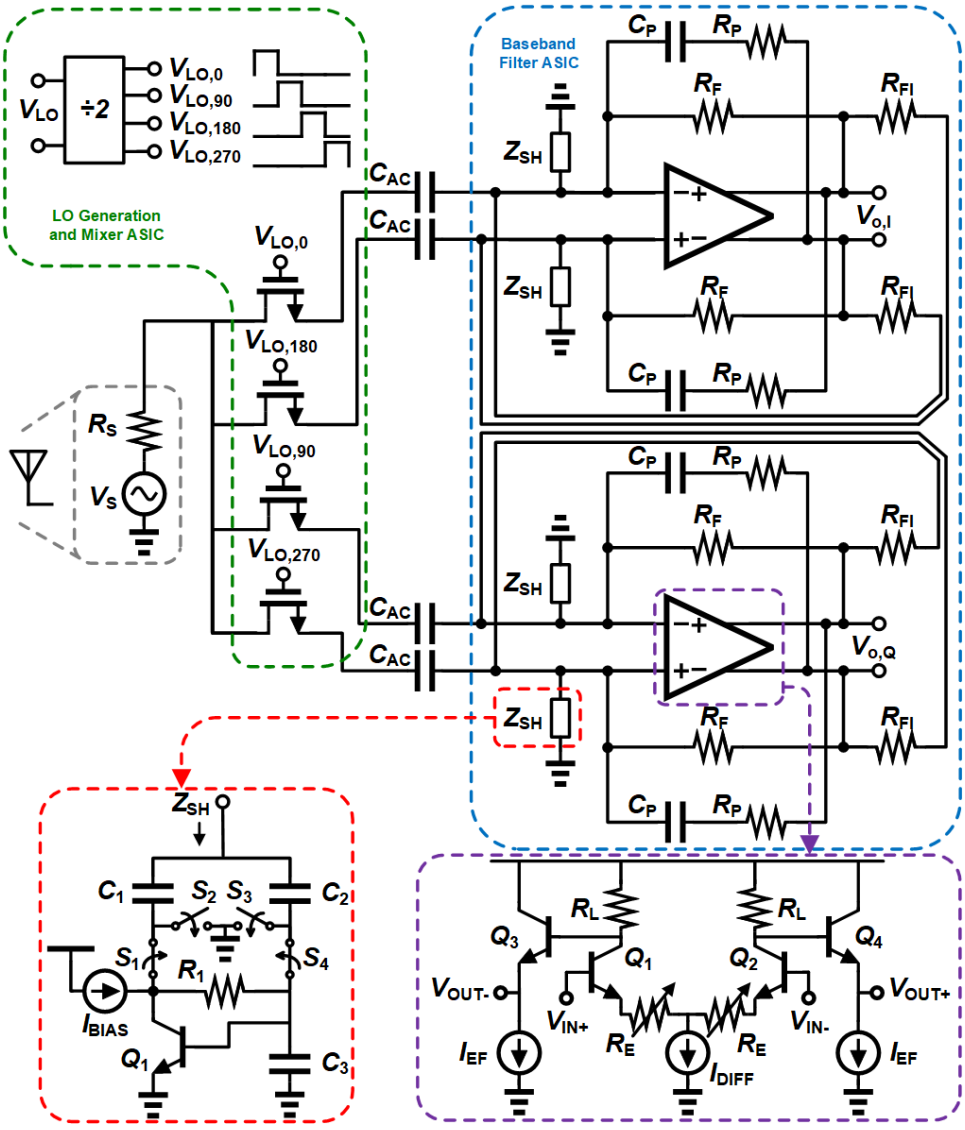

Figure 6.3: Circuit implementation of the baseband filter integrated into the proposed receiver.

amplitude swing as well as rise and fall times on the gates of the passive mixer devices. Note that all the clock generation circuitry is implemented with SiGe bipolar junction transistors. The mixer outputs are AC-coupled to the baseband amplifier input via off-chip capacitors to isolate varying DC levels between the two chips. The baseband amplifier is designed to be flexible with a -3dB LPF bandwidth range of 40 to 130 MHz, adjustable gain from 10 to 24dB, and se-

lectable filtering modes as most shown passives are programmable. To account for parasitic capacitance and complex source impedance seen at the RF port, complex feedback is also implemented by using resistors as seen in [5].

The baseband amplifier topology is a degenerated common-emitter differential pair with emitter follower output buffers. This topology was selected for its simplicity as the voltage gain is approximately R_L/R_E. Furthermore, making the gain programmable by adjusting the degeneration resistance produces a trade-off between noise and in-band linearity. This is useful as large in-band signals are sufficiently above the noise floor such that noise performance can be scaled back to prevent in-band distortion from corrupting the received signal. Emitter follower output buffers are used to reduce the output impedance of the amplifier, preventing the creation of additional poles and zeros around the filter corner frequency, thus impacting the filter shape. Furthermore, the emitter followers ensure there is sufficient current drive to capacitors in the positive feedback path.

The shunting impedance circuit contains a switching network to configure the circuit to operate as a shunting capacitance or as the proposed shunting notch circuit. The g_m circuit is implemented with an NPN SiGe transistor, biased by a current source injected into the collector node of the transistor. Note that it is desirable to keep C_3 as small as possible and therefore is implemented from the parasitic capacitances present on that node, dominated by the base emitter capacitance from the transistor. Details regarding the impact of C_3 on the filter performance is discussed later in this work.

6.4 Positive Capacitive Feedback Circuit Analysis

6.4.1 Transfer Function

The derivation of the voltage transfer function from the positive capacitive feedback technique is to analyze V_i in terms of V_S shown in Fig. 6.4A. Note that since this analysis is done in the baseband domain, the shown source impedance R_S is actually $\gamma R_{S,RF}$ where γ is an impedance transform term [4]. Using the Miller effect the input impedance of the baseband amplifier can be broken down into three parallel conductances with the following equation:

$$Z_{IN}^{-1} = sC_{SH} + \frac{1 + A_V}{R_F} + \frac{sC_P(1 - A_V)}{1 + sR_PC_P} \tag{6.1}$$

Solving for Z_{IN} as a product of poles and zeros with the value $R_F/(1 + A_V)$ defined as R_0 yields the following form for the transfer function:

$$Z_{IN} = R_0 \frac{1 + \omega/\omega_z}{s^2/\omega_n^2 + s/(\omega_n Q) + 1} \tag{6.2}$$

Where $\omega_z = (R_PC_P)^{-1}$, $\omega_n = 1/\sqrt{R_0R_PC_{SH}C_P}$, and the quality factor Q is as follows:

$$Q = \frac{\sqrt{R_0R_PC_{SH}C_P}}{R_0C_{SH} + R_PC_P + (1 - A_V)R_0C_P} \tag{6.3}$$

Furthermore, the term α is defined as the ratio between ω_z and ω_n. Fig. 6.4B shows that α not only sets the duration of the second-order filter roll-off, but it also sets the bandwidth extension from the traditional single-pole baseband

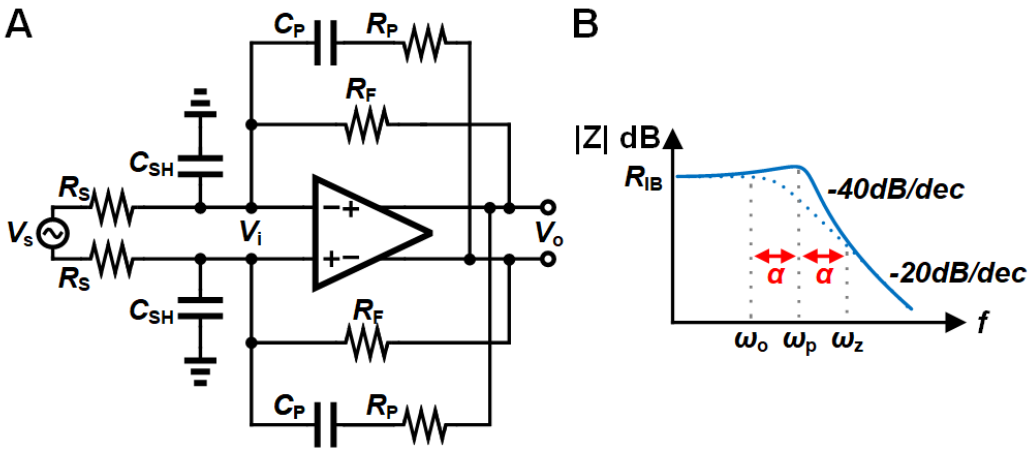

Figure 6.4: (A) Proposed positive capacitive feedback baseband filter loading impedance-translated RF source. (B) Conceptual impedance transfer function showing the bandwidth extension from the positive feedback.

filter. Note that while increasing the value of α increases the frequency range of the positive feedback, and thus increases the roll-off of the baseband filter, the purpose of the filter is for the impedance roll-off to drop beneath the mixer switch on-resistance. Typically, the value of α should be around 3 to 4, as larger values can reduce the phase margin of the baseband filter, leading to stability concerns, as well as have a negative impact on noise and linearity. Fig. 6.5 shows the impact of the positive feedback components C_P and R_P on the input impedance transfer function compared to the single-pole baseband filter. While both component values impact the Q factor and location of ω_z, C_P has a stronger influence on Q and R_P moves ω_z with relatively minor changes to Q.

Calculating the voltage transfer function $H_{BB,S}$ is performed by calculating the impedance divider between the previously calculated input impedance of the baseband filter Z_{IN} and the impedance-translated source impedance R_S. Given that $R_0 = R_S$ for impedance matching the transfer function can be written in the following form:

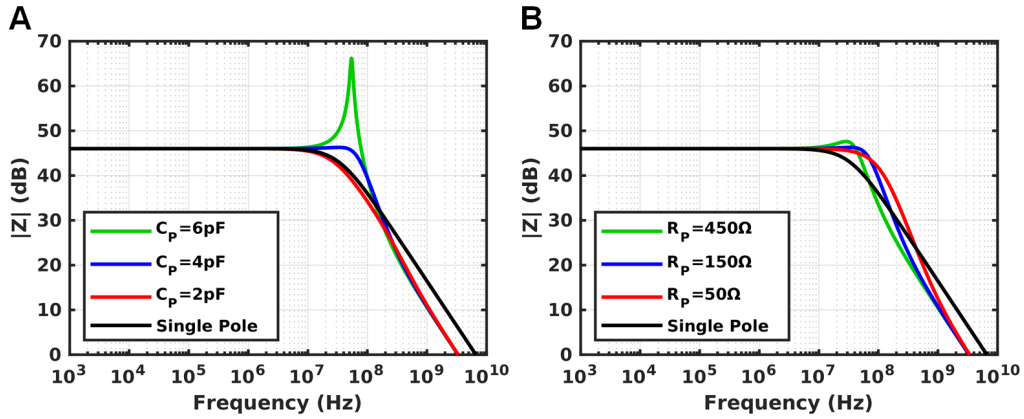

Figure 6.5: Impedance transfer functions of the positive capacitive feedback baseband filter sweeping the values of (A) C_P and (B) R_P. Default values for other components in the plots are R_S=200 Ω, R_F=2200 Ω, R_P=150 Ω, C_{SH}=48pF, C_P=3pF, and A_V=10.

$$H_{BB,S} = \frac{V_i}{V_S} = \frac{1}{2}\frac{1+\omega/\omega_{z,H}}{s^2/\omega_{n,H}^2 + s/(\omega_{n,H}Q_H) + 1} \tag{6.4}$$

Where $\omega_{z,H} = (R_P C_P)^{-1}$, $\omega_{n,H} = \sqrt{(R_S/2)R_P C_{SH} C_P}$, and the quality factor Q_H is as follows:

$$Q_H = \frac{\sqrt{(R_S/2)R_P C_{SH} C_P}}{(R_S/2)C_{SH} + R_P C_P + (1-A_V)(R_S/2)C_P} \tag{6.5}$$

When designing the baseband filter the starting known specifications are typically the desired gain, bandwidth, and quality factor. Parameters relating to the passive mixer such as the number of phases and on-switch resistance will set the impedance-translated source impedance and α respectively. Solving for the passive components begins with setting $R_F = R_S(1+A_V)$ for impedance matching. Furthermore, based off of the desired value of α and the filter bandwidth, the location of the zero is defined as $\omega_{z,H} = \alpha\omega_{n,H}$. Based off of the feedback resistor and the desired bandwidth the shunting capacitance is calculated by

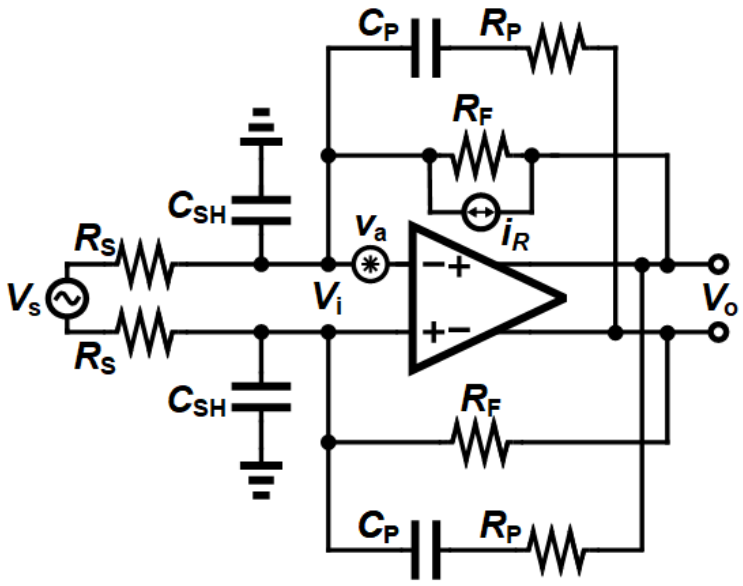

Figure 6.6: Proposed positive capacitive feedback baseband filter loading impedance-translated RF source with modeled noise sources.

$C_{SH} = \omega_{z,H}(R_0 + R_S)/(R_0^2\omega_{n,H}^2)$. Finally, the remaining two components, C_P and R_P, are solved by using the equations for Q_H and $\omega_{z,H}$.

6.4.2 Noise and Linearity

Fig. 6.6 shows the impedance-translated source impedance loaded by the positive capacitive feedback baseband filter with the dominant noise sources modeled. The baseband amplifier noise is modeled as an input-referred voltage noise source and the thermal noise from R_F is modeled as a parallel current noise source. To simplify the analysis the thermal noise associated with R_P is ignored as the value of R_P is significantly less than R_F and the noise is AC-coupled through C_P, thus only contributing to the integrated NF during the bandwidth extension set by α.

Modeling the baseband amplifier noise source $\overline{v_a^2} = 4kT\gamma/g_m$ where γ is the

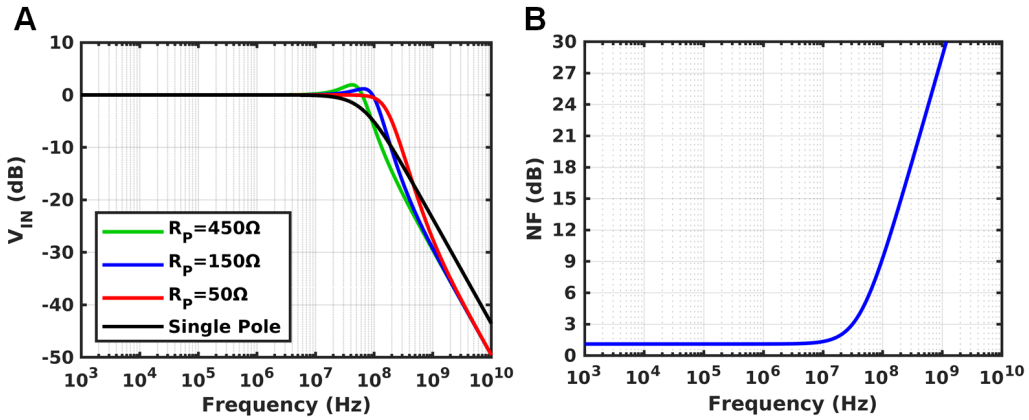

Figure 6.7: (A) Input voltage transfer function while sweeping the value of R_P. Note the transfer function is scaled by a factor of two to adjust for the loss from the input matching. (B) Noise figure across frequency. Default values for other components in the plots are R_S=200 Ω, R_F=2200 Ω, R_P=150 Ω, C_{SH}=48pF, C_P=3pF, A_V=10, g_m=50mS, and γ=2.

noise coefficient for the process and assuming sufficiently large gain A_V for the baseband amplifier, the noise factor F can be approximated as:

$$F \approx 1 + \frac{1}{A_V + 1} + \frac{\gamma[1 + (\frac{2\alpha\omega}{\omega_{n,H}})^2]}{g_m R_S} \tag{6.6}$$

The transfer function and NF over frequency are shown in Fig. 6.17. While α is an important parameter for providing sufficient roll-off to suppress OOB blockers, the baseband amplifier contribution noise scales with $4\alpha^2$ due to the positive feedback path. Therefore, the design of the baseband amplifier must be to prioritize low noise.

The positive feedback path also introduces an additional linearity constraint as the baseband amplifier must also have sufficient output current drive to apply potentially large voltage signals on the capacitor without slewing. This is implemented with NPN emitter followers with sufficient bias current to ensure that the baseband amplifier is not the limiting factor on the band-edge linearity.

Note that to maintain the noise and linearity performance observed in traditional single-pole baseband filter designs, extra power must be consumed.

6.5 Shunt Notch Feedback Circuit Analysis

6.5.1 Transfer Function

Similar to the positive capacitive feedback analysis, the transfer function using the shunting notch technique is performed by analyzing V_i in terms of V_S in the baseband domain. The analyzed circuit is shown in Fig. 6.8. The equations for the impedance of Z_{SH} and Z_{IN} can be found in equations (6.7) and (6.8) respectively, with plots showing the impedance transfer function in Fig. 6.9. The expression for Z_{SH} is an exact while the expression for Z_{IN} assumes that both $g_{m1}R_0$ and $g_{m1}R_1$ are significantly greater than 1, and C_1, C_2 are significantly larger than C_3. These assumptions infer that the real pole located at C_3/g_{m1} does not impact the shape of the complex poles and zeros. Simulation comparisons show that the assumptions overestimates the filter Q within 10% and simplifies the flat-band post complex poles and zeros from $(R_0/[g_{m1}R_0+1])(C_2/[C_2+C_3])$ to $1/g_{m1}$.

Calculating the transfer function through the impedance divider from the shunt notch baseband filter and the translated source impedance R_S yields equation (6.9). The equation can be written into the following form:

$$H_{BB,S}(s) = \frac{H_0(s^2/\omega_{z,H}^2 + s/(\omega_{z,H}^2 Q_{z,H}) + 1)}{(1 + s\frac{C_3}{g_{m1}})(s^2/\omega_{n,H}^2 + s/(\omega_{n,H}^2 Q_{n,H}) + 1)} \tag{6.10}$$

Where $H_0 = R_0/(R_0 + R_S)$, $\omega_{z,H} = \sqrt{gm/(R_1C_1C_2)}$, $\omega_{n,H} = 1/\sqrt{(R_S||R_0)R_1C_1C_2}$, and the Q factors have the following equations:

$$Q_{z,H} = \frac{\sqrt{(R_1C_1C_2)/g_{m1}}}{(C_1 + C_2)/g_{m1}} \tag{6.11}$$

$$Q_{n,H} = \frac{\sqrt{(R_S||R_0)R_1C_1C_2}}{(R_S||R_0)(C_1 + C_2)} \tag{6.12}$$

The transfer function plots for the shunt notch baseband filter topology are shown in Fig. 6.10. C_1 and C_2 set the corner frequency of the filter. As R_1 increases the Q factors for the complex poles and zeros also increases and increasing g_{m1} decreases the flat-band after the complex poles and zeros. Similar to the positive feedback filter design, the shunting notch filter design begins with the known specifications for gain, bandwidth, quality factor, as well as the number of passive mixer phases and the on-switch resistance. The initial passive components to solve for begins with $R_F = R_S(1 + A_V)$ for impedance matching and for $g_{m1} < 1/R_{SW}$ to ensure OOB linearity is dominated by the passive mixer and not the baseband filter. Finally, defining the total shunting capacitance as $C = C_1 + C_2$ and using the equations for $\omega_{n,H}$ and $Q_{n,H}$ solves for the values of C and R_1. Note that there are not enough controllable circuit parameters to also

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$$Z_{SH} = \frac{(1 + sR_1C_1)(s^2\frac{R_1}{g_m}C_1[C_2 + C_3] + s\frac{C_1+C_2+C_3}{g_m} + 1)}{(s[C_1 + C_2])(1 + s\frac{C_3}{g_m})(s^2R_1^2C_1[\frac{C_1C_2}{C_1+C_2}] + sR_1[C_1 + \frac{C_1C_2}{C_1+C_2}] + 1)} \tag{6.7}$$

$$Z_{IN} = R_0\frac{s^2\frac{R_1}{g_m}C_1C_2 + s\frac{C_1+C_2}{g_m} + 1}{(1 + s\frac{C_3}{g_m})(s^2R_1R_0C_1C_2 + sR_0[C_1 + C_2] + 1)} \tag{6.8}$$

$$H_{BB,S}(s) = \frac{R_0}{R_S + R_0}\frac{s^2\frac{R_1}{g_m}C_1C_2 + s\frac{C_1+C_2}{g_m} + 1}{(1 + s\frac{C_3}{g_m})(s^2(R_0||R_S)R_1C_1C_2 + s(R_0||R_S)[C_1 + C_2] + 1)} \tag{6.9}$$

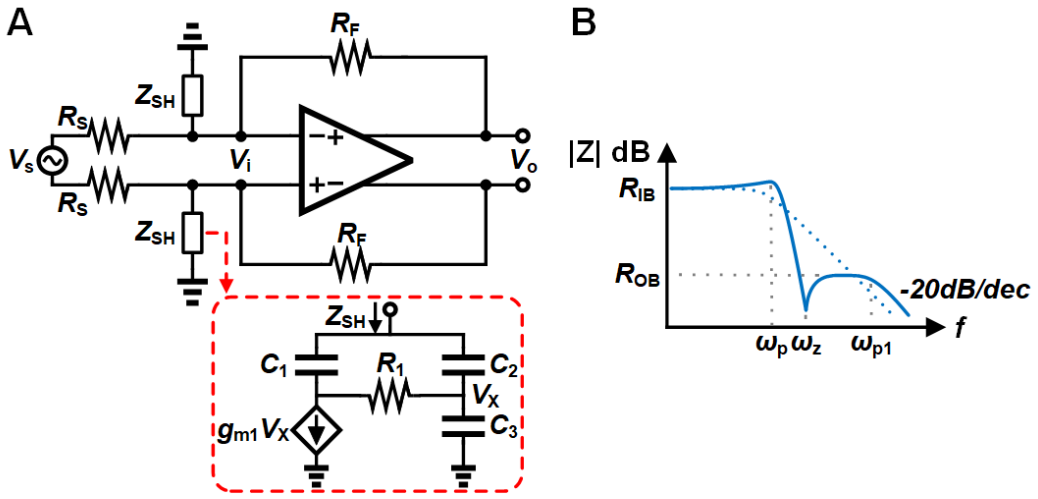

Figure 6.8: (A) Proposed shunting notch baseband filter loading impedance-translated RF source. (B) Conceptual impedance transfer function showing the notch effects over the traditional single-pole baseband filter.

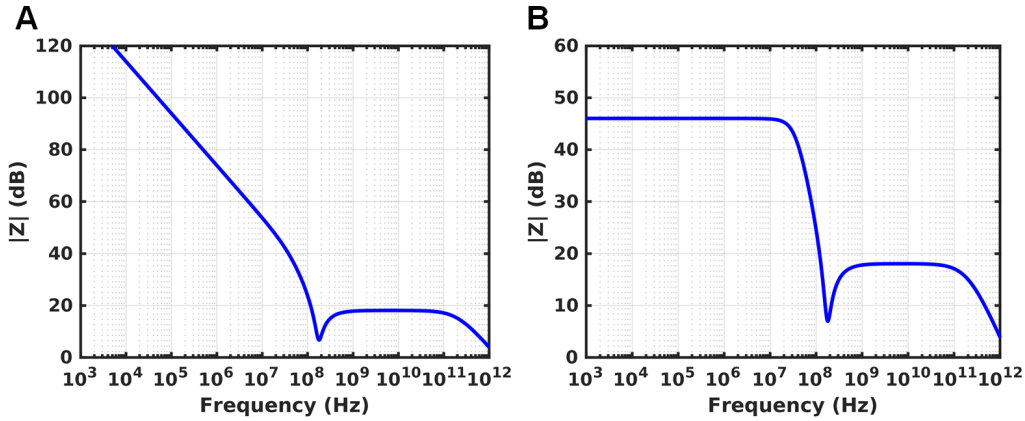

Figure 6.9: Impedance transfer function for the (A) shunting notch circuit and (B) the shunting notch circuit in parallel with the baseband amplifier with resistive feedback. Default values for other components in the plots are R_S=200 Ω, R_F=2200 Ω, R_1=400 Ω, g_{m1}=125mS, C_1=16pF, C_2=16pF, C_3=100fF, and A_V=10.

independently design for $\omega_{z,H}$ and $Q_{z,H}$. Finally, trading off between C_1 and C_2 does not have a significant impact on the transfer function. As long as the total capacitance C remains constant the changes to $\omega_{n,H}$ and $Q_{n,H}$ will be relatively minor.

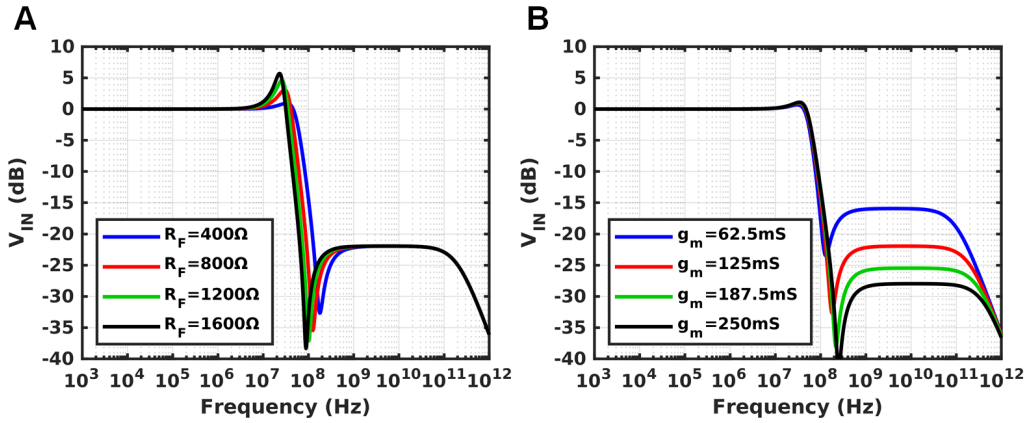

Figure 6.10: Input voltage transfer function while sweeping the value of (A) R_1 and (B) g_{m1}.

6.5.2 Noise Performance

Fig. 6.11 shows the impedance-translated source impedance loaded by the shunting notch baseband filter with the dominant noise sources modeled. As seen in the positive feedback analysis, the baseband amplifier noise is modeled as an input-referred voltage noise source and the thermal noise from R_F is modeled by a parallel current noise source. In the shunting notch circuit itself, the thermal noise from g_{m1} and R_1 are also modeled as parallel current noise sources. Finally, C_3 is removed from the circuit analysis as its contribution is insignificant up to the desired filter bandwidth. Modeling the amplifier input-referred noise as $4kT\gamma/g_m$ and assuming the baseband filter is impedance matched ($R_F = R_S(1 + A_V)$), the noise factor equation is derived as follows:

$$F = 1 + \frac{1}{A_V + 1} + \frac{\gamma}{g_m R_S}|\mathbf{A}|^2 + \frac{R_1}{R_S}|\mathbf{B}|^2 + \frac{4\gamma}{g_{m1} R_S}|\mathbf{C}|^2 \tag{6.13}$$

$$\mathbf{A} = \frac{(1 + s\frac{C_3}{g_{m1}})(s^2 R_S R_1 C_1 C_2 + sR_S[C_1 + C_2] + 1)}{s^2 \frac{R_1 C_1 C_2}{g_{m1}} + s\frac{C_1 + C_2}{g_{m1}} + 1} \tag{6.14}$$

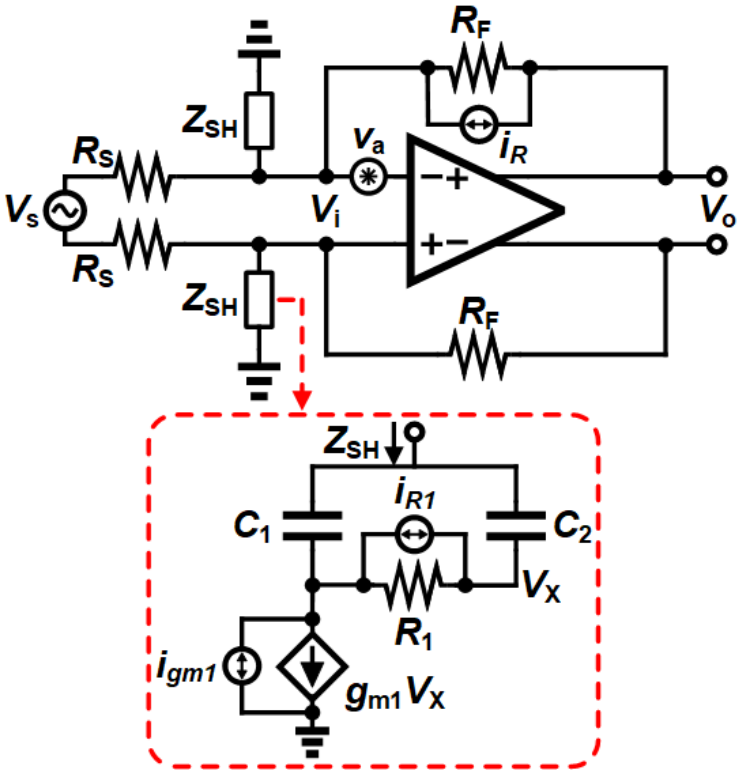

Figure 6.11: Proposed shunting notch baseband filter loading impedance-translated RF source with modeled noise sources.

$$\mathbf{B} = \frac{sR_S C_1}{s^2 \frac{R_1 C_1 C_2}{g_{m1}} + s\frac{C_1+C_2}{g_{m1}} + 1} \tag{6.15}$$

$$\mathbf{C} = \frac{(s\frac{R_S}{2}[C_1+C_2])(s^2\frac{R_1 R_S C_1 C_2}{2} + s[\frac{R_S}{2}(C_1+C_2) + \frac{R_1 C_1 C_2}{C_1+C_2}] + 1)}{(1+s\frac{R_S}{2}[C_1+C_2])(s^2\frac{R_1 C_1 C_2}{g_{m1}} + s\frac{C_1+C_2}{g_{m1}} + 1)} \tag{6.16}$$

Where **A** is the noise contribution of the baseband amplifier, **B** is the noise contribution of R_1, and **C** is the noise contribution of g_{m1}. The noise contribution of R_1 dominates the noise contribution of g_{m1}. This occurs since part of the current noise from R_1 generates a voltage signal on the node V_X, which is then amplified by $g_{m1}R_1$ and is then AC-coupled onto the input of the baseband amplifier through C_1. Equation (6.15) shows this through the numerator term

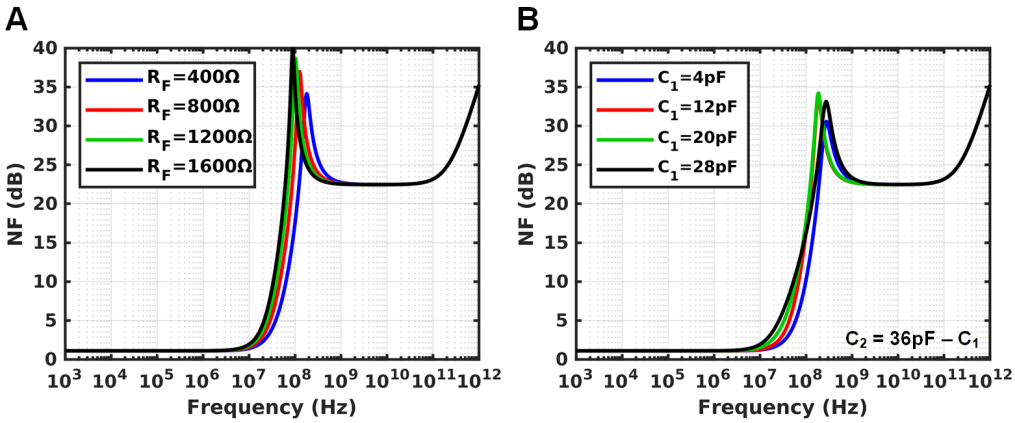

Figure 6.12: Noise figure plotted over frequency while sweeping the values of (A) R_1 and (B) C_1 and C_2. Default values for other components in the plots are R_S=200 Ω, R_F=2200 Ω, R_1=400 Ω, g_{m1}=125mS, C_1=16pF, C_2=16pF, C_3=100fF, A_V=10, g_{ma}=50mS, and γ=2.

sR_SC_1 as the larger C_1 is, the stronger the noise AC-coupling effect onto the input is. This suggests that for low-noise applications it is preferred for C_2 to be larger than C_1. Note that the shunting notch provides a lower noise enhanced base-band filter when compared to the positive capacitive feedback as the noise only AC-couples around the corner frequency as opposed to having noise degradation from positive feedback. Integrated NF plots for swept values of R_1, C_1, and C_2 can be found in Fig. 6.12.

6.5.3 Linearity Constraints

The addition of the g_m cell in the shunting notch circuit introduces a source of nonlinearity as the output must handle amplified band-edge blockers that AC-coupled onto node V_X through C_2. While it is possible to design low-noise, very linear g_m cells to use within the shunting notch [67, 100], there are trade-offs that can be made within the shunting notch circuit itself. Although C_3 has been

ignored for the majority of the analysis of the shunting notch circuit, it does produce a capacitor divider with C_2 on the node V_X. Therefore, to improve linearity by reducing the size of the blocker signal on V_X, C_2 should be reduced, which in turn increases C_1 to keep $\omega_{n,H}$ consistent. Note that this is the opposite for optimizing the noise performance of the circuit, and therefore by implementing C_1 and C_2 with programmable capacitor banks, linearity and noise can be traded-off depending on the application and wireless spectrum conditions.

6.6 Measurement Results

The proposed baseband filter chip as well as the LO generation and mixer chip were fabricated in a 130 nm SiGe BiCMOS technology process. The chips are fixed to the test circuit board with silver conductive epoxy and bonded directly to the test board. Fig. 6.13 shows the baseband filter chip, consuming a total area chip including pads of 2000 µm × 2500 µm, while the active area consumes 2.46 mm^2. The chip is designed to consist of four differential baseband filters with harmonic recombination and source followers to provide quadrature outputs capable of driving 100 Ω differential loads in conjunction with an eight-phase passive mixer, preventing the area to be as compact as possible. Since the chip is tested with a four-phase passive mixer, on-chip switches short the inputs and outputs of adjacent baseband filters and bypass the harmonic recombination. A wideband 180° hybrid coupler is used to provide a differential LO input and the RF input is provided through a bias tee and RF probe to reduce the losses caused by the board traces and wire bonds. Losses associated with the cables, bias tee, and probe are de-embedded from all shown measurements.

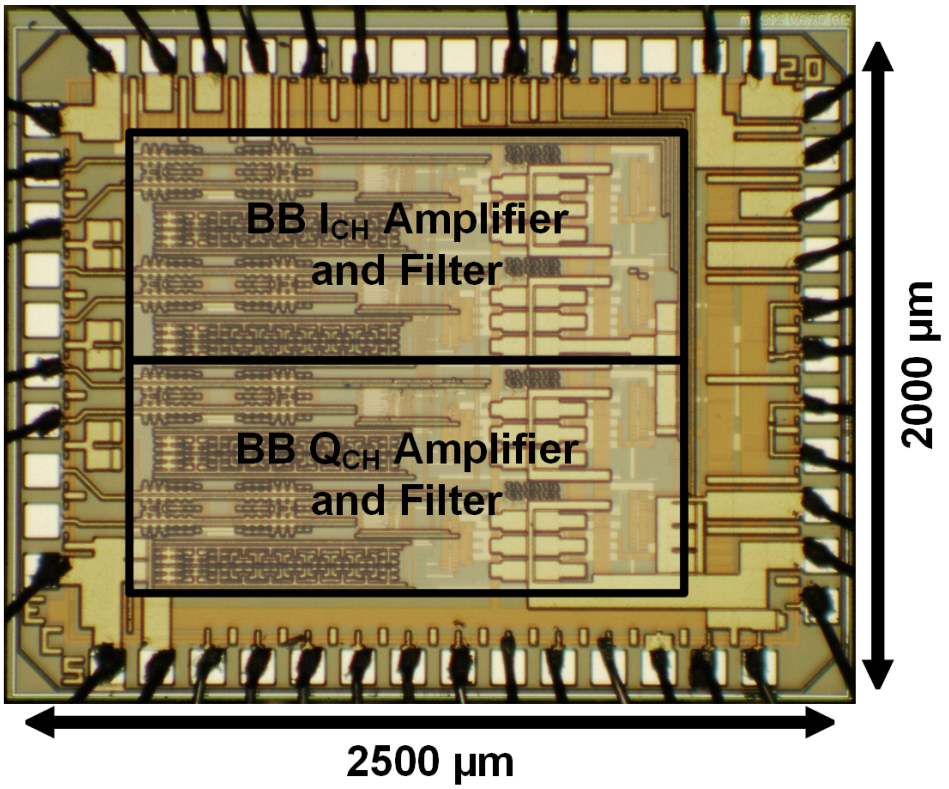

Figure 6.13: Chip micrograph.

6.6.1 Gain and Z_{11}

The RF signal consists of a tone of -30 dBm and is swept around the desired receiver center frequency, while the baseband output is measured on a spectrum analyzer to obtain the conversion gain. Fig. 6.14 shows the measured Z_{11} (inferred from the S_{11} measured by a network analyzer) and gain for the three baseband filter topologies (single pole, shunting notch, and positive capacitive feedback) using the same amount of shunting capacitance. The asymmetries in the measured plots are caused by the passive mixer down-converting the parasitic capacitance present on the RF input and are partially compensated by programming the complex-feedback resistors. The enhanced selectivity filters have an in-band impedance of 41 Ω where the impedance flattens off in the range of

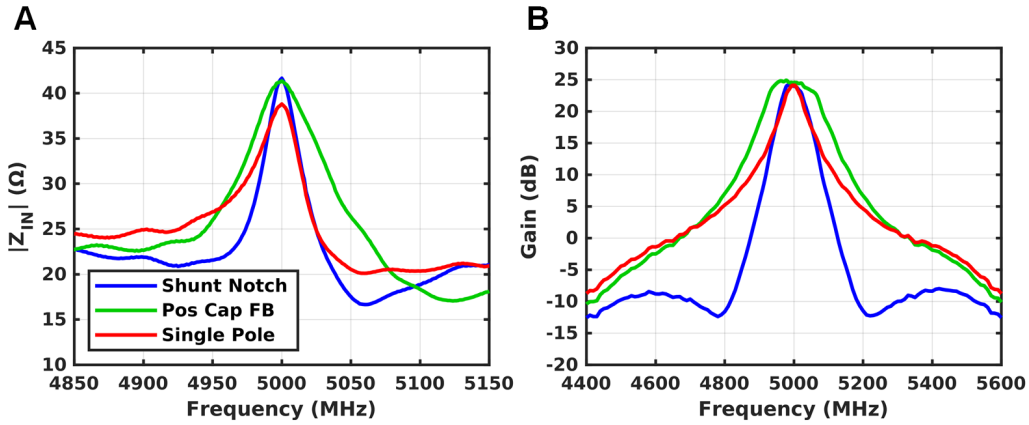

Figure 6.14: Measured (A) Z_{11} and (B) gain over RF frequency for the three baseband filter topologies. f_{RF} is set to 5 GHz.

20 - 25 Ω.

The shunting notch bandpass filter has a 3dB-bandwidth of 70 MHz, extending the bandwidth by roughly 10 MHz from the single pole filter. The measured filter roll-off from 35 to 70 MHz (from the corner frequency to twice the corner frequency) is 8.7 dB while the gain roll-off from 70 to 140 MHz is 15.86 dB. An ideal Butterworth filter has gain roll-offs of 9.3 and 11.8 dB for these frequency ranges respectively. The shunting notch produces a better gain roll-off further away from the corner frequency than the ideal Butterworth filter as the complex zeros creating the high-Q resonant notch in the transfer function contributes to the gain roll-off.

The positive capacitive feedback increases the bandpass filter 3-dB bandwidth to 150 MHz with gain roll-offs from 75 to 150 MHz and 150 to 300 MHz of 9.74 and 10.15 dB respectively. The reduced roll-off from the 150 to 300 MHz range is caused by the zero located at baseband frequency of $(2\pi R_P C_P)^{-1}$ = 225 MHz. While this zero reduces the gain roll-off, as long as the zero is located where the mixer switch on-resistance dominates the baseband impedance the

filter will not dominate the linearity constraints caused by OOB interferers.

6.6.2 Linearity

While in-band linearity is limited by the baseband amplifier and OOB linearity is limited by the mixer switch on-resistance, the band-edge linearity is more difficult to compare across topologies as the -3 dB bandwidth different receivers varies. Therefore, as discussed in [86], the linearity measurements are plotted across the relative frequency offset normalized to the -3 dB baseband bandwidth. Fig. 6.15A shows the measured B1dB as a function of normalized offset blocker frequency for f_{RF} = 5 GHz and a desired signal of 5.001 GHz (f_{BB} = 1 MHz) with a signal strength of -30 dBm. The blocker frequency is swept from 5 MHz to 500 MHz offset the RF center frequency. The three filter topologies show an in-band B1dB less than -10 dBm, an OOB B1dB of +1.85 dBm, and a B1dB around -7 dBm when $\Delta f/BW_{BB} = 1$. The single pole filter reaches the OOB linearity when $\Delta f/BW_{BB} = 6.7$. The enhanced filter topologies significantly improve upon this as the positive capacitive feedback topology and shunting notch reaches the OOB linearity when $\Delta f/BW_{BB} = 2.7$ and 1.7 respectively.

IIP3 measurements are performed on all three filter topologies using a two-tone test, with the measurements shown in Fig. 6.15B for f_{RF} = 5 GHz. The frequencies are selected such that $f_1 = f_{RF} - \Delta f$ and $f_2 = f_{RF} - 2\Delta f + 1$ MHz, allowing the produced IM3 product to always be at a baseband frequency of 1 MHz. For the same $\Delta f/BW_{BB}$ values from the B1dB tests, the positive capacitive feedback and shunting notch achieve IIP3 values of +19 dBm and +20 dBm respectively. The measurements show that the enhanced filter shapes also en-

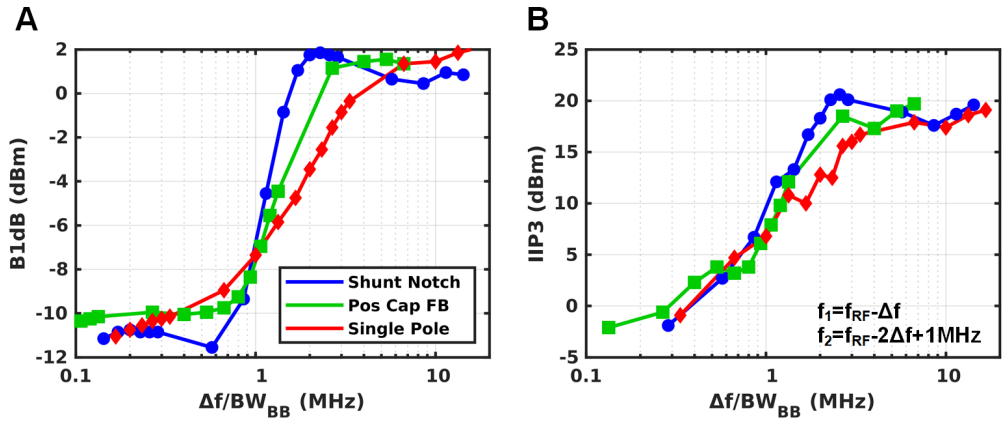

Figure 6.15: Measured (A) B1dB and (B) IIP3 over the relative blocker frequency offset normalized to the -3 dB bandwidth for the three baseband filter topologies. f_{RF} is set to 5 GHz.

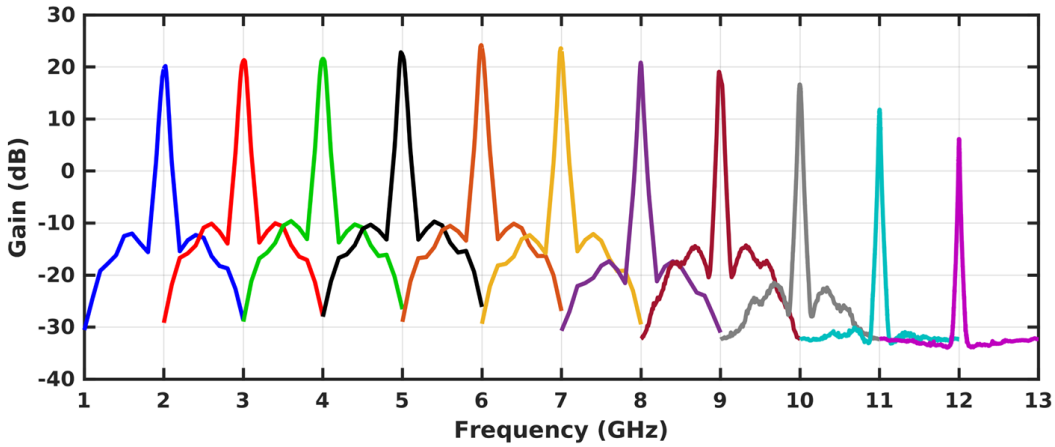

Figure 6.16: Measured shunting notch filter transfer function over f_{RF} swept from 1 to 12 GHz.

hance the filter band-edge blocker tolerance. The shunting notch filter shows a higher increase in the linearity plots over the positive capacitive feedback filter, consistent with the measured transfer function. Furthermore, the shunting notch has an increase in both the B1dB and IIP3 linearity measurements at the notch frequency that is not present in the single pole or positive capacitive feedback filters, suggesting that the shunting notch topology can be optimized to boost the linearity at the notch.

6.6.3 Gain and NF Across RF Frequency

The measured transfer function for the shunting notch filter is shown in Fig. 6.16. Measurement results show the receiver operates from 2 to 11 GHz with significant gain roll-off beyond 9 GHz, where an external clock $2f_{LO}$ up to 22 GHz is applied. The limitation is from the CMOS passive mixer as the LO buffers and baseband filter have been shown to operate beyond 11 GHz using a GaAs passive mixer in other work [94]. Fig. 6.17 shows the conversion gain and double sideband (DSB) NF from 2 to 8 GHz for the shunting notch filter. The conversion gain is over 20 dB from 3 to 8 GHz with a maximum gain of 24 dB at 6 GHz. The DSB NF ranges from 8.9 to 11.4 dB over the f_{RF} frequency range. Due to lab equipment limitations, completely accurate DSB NF measurements could not be obtained while simultaneously sampling the four quadrature baseband outputs. Therefore, only one differential baseband output is amplified by a low-noise high bandwidth amplifier before the output is sampled by a spectrum analyzer. To compensate for the asymmetries among the I and Q channels, error bars of ±1 dB are added to the reported NF measurements.

The single pole and shunt notch filters have a measured NF at f_{RF} of 11±1 dB, while the positive capacitive feedback NF measurement is 12±1 dB. The noise figure is dominated by the high on-resistance of the mixer switches and from noise injection from the LO. While the high on-resistance on the mixer switches was selected to ensure the RF receiver could operate above an f_{RF} frequency of 10 GHz while using CMOS switches from a 130 nm process, an oversight in the LO circuitry led to a higher LO noise injection contribution than expected. This higher-than-expected NF masked the significant differences between the NF contributions from the baseband filter topologies.

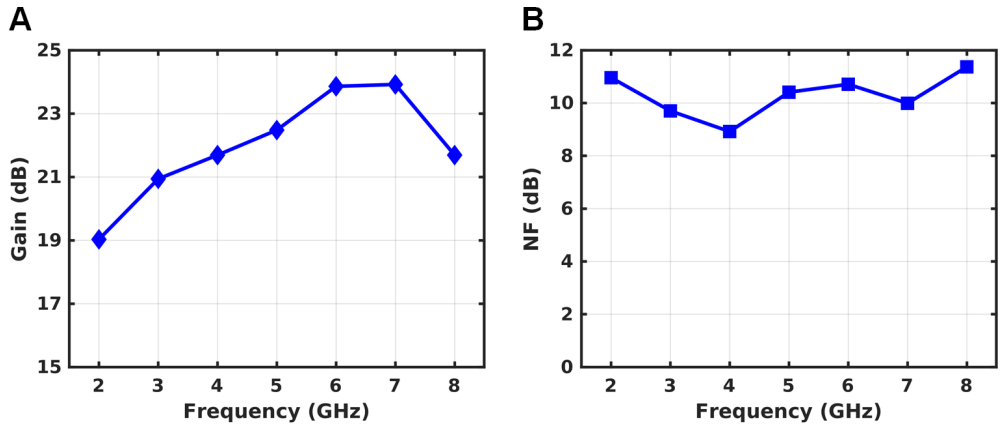

Figure 6.17: Measured shunting notch filter (A) gain and (B) DSB NF over f_{RF} swept from 1 to 8 GHz. NF data tolerance is ±1 dB.

6.6.4 Power Consumption

The LO chip operates on a 4.5-V supply for the LO buffers and the baseband filter chip operates on a 4.0-V supply for the amplifiers, with both chips using a 2.5-V supply for the programming interface. The LO chip consumes 1466 to 1494 mW of power over the receiver operating frequency range. The power consumption for the LO chip is higher than necessary to drive the CMOS mixer switches as it was designed to drive GaAs mixer switches, which have higher parasitic capacitances and require a larger voltage swing. The shunting notch topology consumes 656 mW and the positive capacitive feedback topology increases the power consumption to 674 mW, with the increased power needed for the emitter followers to drive the capacitive feedback to improve band-edge linearity. The high baseband power consumption is needed to maintain the NF contribution from the degenerated common emitter differential pair under 4 dB. Ideally, the power consumption could be reduced to increase the NF contribution since the receiver DSB NF is dominated by the LO and mixer switches. However, significant reduction of the amplifier bias current raises the DC out-

put voltage to non-ideal levels, drastically degrading the linearity performance.

6.6.5 Performance Comparison

It has been discussed that the proposed positive capacitive feedback and shunting notch decrease the band-edge width of the filter to transition from in-band to OOB linearity receiver limitations. By defining the capacitor-bandwidth product metric (C-BW_{BB}), the total baseband capacitance multiplied by the baseband bandwidth, comparisons can be made to see which filter designs use the least capacitance for their bandwidth to observe their area efficiency. The single pole design has a C-BW_{BB} product of 465 pF·MHz. The shunting notch filter increases the C-BW_{BB} product slightly to 620 pF·MHz, which is expected as the Q factor of the complex poles pushes out the 3-dB bandwidth. The positive capacitive feedback increases this product further to 1376 pF·MHz, over double the value from the shunting notch topology, caused by the added capacitors in the positive feedback loop nulling out the shunting capacitance to extend the bandwidth.

The shunting notch filter appears to be the superior topology for narrower baseband filter applications (sub 100 MHz) due to the slightly improved band-edge roll-off and reduced area. However, the shunting notch filter has issues in higher bandwidth applications as the parasitic capacitance of the g_m constituting C_3 is no longer significantly smaller than C_1 and C_2, increasing the flat-band impedance after the shunting notch. Furthermore, the parasitic capacitances associated the input of the baseband amplifier begins to dominate the baseband impedance, reducing the Q of the filter. The positive capacitance topology excels for wider baseband bandwidth application as the additional capacitance in

Table 6.1: Comparison With Prior Art

Reference	*JSSC10* [5]	*JSSC15* [28]	*RFIC15* [101]	*ISSCC17* [87]	*JSSC18* [86]	*JSSC20* [72]	*JSSC21* [125]	**This Work**	**This Work**
Architecture	Mixer-first	Mixer-first +2nd order baseband	Mixer-first with positive resistive feedback	N-path filters with bottom-plate mixing	Mixer-first with positive capacitive feedback	Mixer-first with 40 dB/dec roll-off	Mixer-first with 2nd order BB NC TIA	**Mixer-first with positive capacitive feedback**	**Mixer-first with shunting notch**
Technology	65nm	65nm	65nm	28nm	45nm SOI	28nm	180nm	**130nm SiGe BiCMOS**	**130nm SiGe BiCMOS**
f_{RF} (GHz)	0.1-2.4	0.5-3	0.7-3.8	0.1-2.0	0.2-8	0.2-2	0.2-1.2	**2-11**	**2-11**
Gain (dB)	40-70	50	40	16	21	13	31.4	**10-24**	**10-24**
BW (MHz)	20	2-60	20	13	20	18	36	**80-260**	**80-260**
B1dB (dBm)	10 $\Delta f/BW_{BB}$=5	-10 $\Delta f/BW_{BB}$=4	3 $\Delta f/BW_{BB}$=5	13 $\Delta f/BW_{BB}$=12.3	12 $\Delta f/BW_{BB}$=4	12 $\Delta f/BW_{BB}$=3.3	12 $\Delta f/BW_{BB}$=7	**1.2 $\Delta f/BW_{BB}$=2.5**	**1.8 $\Delta f/BW_{BB}$=1.75**
OOB IIP3 (dBm)	25 $\Delta f/BW_{BB}$=5	-4.8 $\Delta f/BW_{BB}$=4	26 $\Delta f/BW_{BB}$=5	44 $\Delta f/BW_{BB}$=12.3	39 $\Delta f/BW_{BB}$=4	33.3 $\Delta f/BW_{BB}$=4.4	39.8 $\Delta f/BW_{BB}$=10	**19 $\Delta f/BW_{BB}$=2.5**	**20 $\Delta f/BW_{BB}$=1.75**
NF (dB)	4±1	3.8-4.7	2.5-4.5	6.3	2.3-5.4	4.3-7.6	3.4-4	**12±1**	**11±1**
Supply (V)	1.2/2.5	1.2/2.5	1.2	1.2/1.0	1.2	1.2	1.8	**4.5/2.5† 4/2.5‡**	**4.5/2.5† 4/2.5‡**
Power (mW)	37-70	RX:76-168 LO:54-194	27-75	38-96	50+30/GHz	Active Z:100 TIA:43 LO:3.6-36	RX:19.8 LO:45-135	**RX:674 LO:1466-1494**	**RX:656 LO:1466-1494**
Area (mm^2)	2.5	7.8	0.23	0.49	0.8	0.48	0.54	**1.42†, 2.46‡**	**3.4†, 1.42‡**

† LO generation ASIC
‡ Baseband filter ASIC

positive feedback will cancel out the dominant parasitic capacitances to extend the filter bandwidth. This is desirable for next generation wireless devices operating the mm-wave range that need the larger bandwidth to further increase the data rates [111].

When compared to prior work, the SiGe LO buffer drivers allow the proposed RF receiver to operate at significantly higher frequencies despite driving mixer switches in a much longer technology node, contributing to a higher noise figure than prior work. Between the two proposed enhanced filter topologies, the RF bandwidth ranges from 80 to 260 MHz, achieving a bandwidth over 3.7 times larger than prior work. This work proposes the smallest $\Delta f/BW_{BB}$ ratio showing that this work has the smallest transition band before the mixer switches dominate the OOB linearity. However, while part of this is caused by the enhanced linearity of the proposed baseband filters, this is also in-part caused by the poor OOB linearity from the mixer switch on-resistance. A summary of this work when compared to prior work is shown in Table 6.1.

Recent work has shown that it is possible to combine multiple enhanced baseband filtering techniques to achieve greater than 40-dB/decade RF selectivity [73, 74]. This suggests that the positive capacitive feedback and shunting notch circuit techniques can be combined and co-designed to achieve up to fourth-order baseband filter roll-off.

6.7 Conclusion

This work proposes two baseband filter techniques to enhance the selectivity of mixer-first receivers utilizing positive capacitive feedback and a shunting notch circuit. These techniques improve the filter shape by utilizing a complex pole pair to achieve higher than single order baseband filter roll-off while also maintaining a sufficient Q to prevent significant signal loss at the corner frequency. Both baseband filter topologies are analyzed and discuss how to engineer the corner frequency, quality factor, bandwidth, NF, and linearity while also going over the advantages and shortcomings when comparing the two designs. Measurements show that that the enhanced baseband filter topologies are capable of achieving high-order roll-off than the traditional single pole filter and achieve a OOB linearity at a smaller blocker frequency offset.

BIBLIOGRAPHY

[1] Mohammed Abdulaziz, Eric A. M. Klumperink, Bram Nauta, and Henrik Sjöland. Improving receiver close-in blocker tolerance by baseband g_m-c notch filtering. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 66(3):885–896, March 2019.

[2] A K Ahuja, J D Dorn, A Caspi, M J McMahon, G Dagnelie, L daCruz, P Stanga, M S Humayun, R J Greenberg, and Argus II Study Group. Blind subjects implanted with the argus ii retinal prosthesis are able to improve performance in a spatial-motor task. *British Journal of Ophthalmology*, 95(4):539–543, 2011.

[3] Richard A. Andersen, Eun Jung Hwang, and Grant H. Mulliken. Cognitive neural prosthetics. *Annual Review of Psychology*, 61(1):169–190, 2010.

[4] Caroline Andrews and Alyosha C. Molnar. Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(12):3092–3103, Dec 2010.

[5] Caroline Andrews and Alyosha C. Molnar. A passive mixer-first receiver with digitally controlled and widely tunable rf interface. *IEEE Journal of Solid-State Circuits*, 45(12):2696–2708, Dec 2010.

[6] Sebastián A. Ausili, Martijn J. H. Agterberg, Andreas Engel, Christiane Voelter, Jan Peter Thomas, Stefan Brill, Ad F. M. Snik, Stefan Dazert, A. John Van Opstal, and Emmanuel A. M. Mylanus. Spatial hearing by bilateral cochlear implant users with temporal fine-structure processing. *Frontiers in Neurology*, 11, 2020.

[7] Arezu Bagheri, Muhammad Tariqus Salam, Jose Luis Perez Velazquez, and Roman Genov. Low-frequency noise and offset rejection in dc-coupled neural amplifiers: A review and digitally-assisted design tutorial. *IEEE Transactions on Biomedical Circuits and Systems*, 11(1):161–176, 2017.

[8] A. T. Barker, R. Jalinous, and I. L. Freeston. Non-invasive magnetic stimulation of human motor cortex. *The Lancet*, 1:1106–1107, May 1985.

[9] F. Behbahani, Y. Kishigami, J. Leete, and A.A. Abidi. Cmos mixers and polyphase filters for large image rejection. *IEEE Journal of Solid-State Circuits*, 36(6):873–887, June 2001.

[10] M. Behrend, A. Ahuja, M. Humayun, R. Chow, and J. Weiland. Resolution of the epiretinal prosthesis is not limited by electrode size. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 19:436–442, 2011.

[11] Alim Louis Benabid, Stephan Chabardes, John Mitrofanis, and Pierre Pollak. Deep brain stimulation of the subthalamic nucleus for the treatment of parkinson's disease. *The Lancet Neurology*, 8:67–81, Jan. 2009.

[12] Sliman J. Bensmaia and Lee E. Miller. Restoring sensorimotor function through intracortical interfaces: progress and looming challenges. *Nature Reviews Neuroscience*, 15(5):313–325, 2014.

[13] Dinesh Bharadia, Emily McMilin, and Sachin Katti. Full duplex radios. In *Proceedings of the ACM SIGCOMM 2013 Conference on SIGCOMM*, SIGCOMM '13, page 375–386, New York, NY, USA, 2013. Association for Computing Machinery.

[14] Richard A. Blum, James D. Ross, Edgar A. Brown, and Stephen P. DeWeerth. An integrated system for simultaneous, multichannel neuronal stimulation and recording. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(12):2608–2618, 2007.

[15] Giorgio Bonmassar, Seung Woo Lee, Daniel Freeman, Miloslav Polasek, Shelley Fried, and John Gale. Microscopic magnetic stimulation of neural tissue. *Nature communications*, 3:921, 06 2012.

[16] Edward S Boyden, Feng Zhang, Ernst Bamberg, Georg Nagel, and Karl Deisseroth. Millisecond-timescale, genetically targeted optical control of neural activity. *Nature Neuroscience*, 8(9):1263–1268, 2005.

[17] Christopher R. Butson, Christopher B. Maks, and Cameron C. McIntyre. Sources and effects of electrode impedance during deep brain stimulation. *Clinical Neurophysiology*, 117(2):447–454, 2006.

[18] Christopher R. Butson and Cameron C. McIntyre. Current steering to control the volume of tissue activated during deep brain stimulation. *Brain Stimulation*, 1(1):7–15, 2008.

[19] Natalie Butz, Armin Taschwer, Sebastian Nessler, Yiannos Manoli, and Matthias Kuhl. A 22 V compliant 56 μW twin-track active charge balancing enabling 100% charge compensation even in monophasic and 36% amplitude correction in biphasic neural stimulators. *IEEE Journal of Solid-State Circuits*, 53(8):2298–2310, 2018.

[20] G. Buzsáki. The Hippocampo-Neocortical Dialogue. *Cerebral Cortex*, 6(2):81–92, 03 1996.

[21] Andres Canales, Xiaoting Jia, Ulrich Froriep, Ryan Koppes, Christina Tringides, Jennifer Selvidge, Chi Lu, Chong Hou, Lei Wei, Yoel Fink, and Polina Anikeeva. Multifunctional fibers for simultaneous optical, electrical and chemical interrogation of neural circuits in vivo. *Nature biotechnology*, 33:277–284, 01 2015.

[22] Hariprasad Chandrakumar and Dejan Marković. An 80-mVpp linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference. *IEEE Journal of Solid-State Circuits*, 52(11):2811–2828, 2017.

[23] Hariprasad Chandrakumar and Dejan Marković. A 15.2-ENOB 5-kHz BW 4.5- μW chopped CT ΔΣ-ADC for artifact-tolerant neural recording front ends. *IEEE Journal of Solid-State Circuits*, 53(12):3470–3483, 2018.

[24] F. J. Chaure, H. G. Rey, and R. Quian Quiroga. A novel and fully automatic spike sorting implementation with variable number of features. *Journal of Neurophysiology*, 120(4):1859–1871, 2018.

[25] F. Chen and B. Leung. A 0.25-mw low-pass passive sigma-delta modulator with built-in mixer for a 10-mhz if input. *IEEE Journal of Solid-State Circuits*, 32(6):774–782, June 1997.

[26] Kuanfu Chen, Zhi Yang, Linh Hoang, James Weiland, Mark Humayun, and Wentai Liu. An integrated 256-channel epiretinal prosthesis. *IEEE Journal of Solid-State Circuits*, 45(9):1946–1956, 2010.

[27] Ritchie Chen, Gabriela Romero, Michael G. Christiansen, Alan Mohr, and Polina Anikeeva. Wireless magnetothermal deep brain stimulation. *Science*, 347(6229):1477–1480, 2015.

[28] Run Chen and Hossein Hashemi. Dual-carrier aggregation receiver with reconfigurable front-end rf signal conditioning. *IEEE Journal of Solid-State Circuits*, 50(8):1874–1888, 2015.

[29] Graeme M. Clark. The multiple-channel cochlear implant: the interface between sound and the central nervous system for hearing, speech, and language in deaf people—a personal perspective. *Philosophical Transactions of the Royal Society B: Biological Sciences*, 361(1469):791–810, 2006.

[30] Stuart F Cogan, Kip A Ludwig, Cristin G Welle, and Pavel Takmakov. Tissue damage thresholds during therapeutic electrical stimulation. *Journal of Neural Engineering*, 13(2):021001, Jan. 2016.

[31] Ben W. Cook, Axel Berny, Alyosha Molnar, Steven Lanzisera, and Kristofer S. J. Pister. Low-power 2.4-ghz transceiver with passive rx front-end and 400-mv supply. *IEEE Journal of Solid-State Circuits*, 41(12):2757–2766, Dec 2006.

[32] Milad Darvishi, Ronan van der Zee, and Bram Nauta. Design of active n-path filters. *IEEE Journal of Solid-State Circuits*, 48(12):2962–2976, Dec 2013.

[33] Pelle P. de Koning, Martijn Figee, Pepijn van den Munckhof, P. Richard Schuurman, and Damiaan Sameer A. Denys. Current status of deep brain stimulation for obsessive-compulsive disorder: A clinical review of different targets. *Current Psychiatry Reports*, 13:274–282, 2011.

[34] João L. Carvalho de Souza, Jeremy S. Treger, Bobo Dang, Stephen B.H. Kent, David R. Pepperberg, and Francisco Bezanilla. Photosensitivity of neurons enabled by cell-targeted gold nanoparticles. *Neuron*, 86(1):207–217, 2015.

[35] Günther Deuschl, Jan Herzog, Galit Kleiner-Fisman, Cynthia Kubu, Andres M. Lozano, Kelly E. Lyons, Maria C. Rodriguez-Oroz, Filippo Tamma, Alexander I. Tröster, Jerrold L. Vitek, Jens Volkmann, and Valerie Voon. Deep brain stimulation: Postoperative issues. *Movement Disorders*, 21(S14):S219–S237, 2006.

[36] Max Eickenscheidt, Martin Jenkner, Roland Thewes, Peter Fromherz, and Günther Zeck. Electrical stimulation of retinal neurons in epiretinal and subretinal configuration using a multicapacitor array. *Journal of Neurophysiology*, 107(10):2742–2755, 2012.

[37] Kyungsik Eom, Changkyun Im, Seoyoung Hwang, Seyoung Eom, Tae-Seong Kim, Hae Sun Jeong, Kyung Hwan Kim, Kyung Min Byun, Sang Beom Jun, and Sung June Kim. Synergistic combination of near-infrared irradiation and targeted gold nanoheaters for enhanced photothermal neural stimulation. *Biomed. Opt. Express*, 7(4):1614–1625, Apr 2016.

[38] Shelley I. Fried, Aaron C. W. Lasker, Neal J. Desai, Donald K. Eddington, and Joseph F. Rizzo. Axonal sodium-channel bands shape the response

to electric stimulation in retinal ganglion cells. *Journal of Neurophysiology*, 101(4):1972–1987, 2009.

[39] John Gardner. A history of deep brain stimulation: Technological innovation and the role of clinical assessment tools. *Social Studies of Science*, 43(5):707–728, 2013.

[40] B. Ghane-Motlagh and M. Sawan. A review of microelectrode array technologies: Design and implementation challenges. In *2013 2nd International Conference on Advances in Biomedical Engineering*, pages 38–41, 2013.

[41] B. Ghane-Motlagh and M. Sawan. A review of microelectrode array technologies: Design and implementation challenges. In *2013 2nd International Conference on Advances in Biomedical Engineering*, pages 38–41, 2013.

[42] Warren M. Grill, Sharon E. Norman, and Ravi V. Bellamkonda. Implanted neural interfaces: Biochallenges and engineered solutions. *Annual Review of Biomedical Engineering*, 11(1):1–24, 2009.

[43] Warren M. Grill, Adam M. Simmons, Scott E. Cooper, Svjetlana Miocinovic, Erwin B. Montgomery, Kenneth B. Baker, and Ali R. Rezai. Temporal excitation properties of paresthesias evoked by thalamic microstimulation. *Clinical Neurophysiology*, 116(5):1227–1234, 2005.

[44] Nir Grossman, David Bono, Nina Dedic, Suhasa B. Kodandaramaiah, Andrii Rudenko, Ho-Jun Suk, Antonino M. Cassara, Esra Neufeld, Niels Kuster, Li-Huei Tsai, Alvaro Pascual-Leone, and Edward S. Boyden. Noninvasive deep brain stimulation via temporally interfering electric fields. *Cell*, 169:1029–1041, Jun. 2017.

[45] Michael Haas, Patrick Vogelmann, and Maurits Ortmanns. A neuromodulator frontend with reconfigurable class-b current and voltage controlled stimulator. *IEEE Solid-State Circuits Letters*, 1(3):54–57, 2018.

[46] Marwan I. Hariz. Complications of deep brain stimulation surgery. *Movement Disorders*, 17(S3):S162–S166, 2002.

[47] R.R. Harrison and C. Charles. A low-power low-noise cmos amplifier for neural recording applications. *IEEE Journal of Solid-State Circuits*, 38(6):958–965, 2003.

[48] Jason S. Hauptman, Antonio A. F. DeSalles, Randall Espinoza, Mark Se-

drak, and Warren Ishida. Potential surgical targets for deep brain stimulation in treatment-resistant depression. *Neurosurgical Focus FOC*, 25(1):E3, 2008.

[49] Jasmine M. Henderson, Malcolm Pell, Dudley J. O'Sullivan, Elizabeth A. McCusker, Victor S.C. Fung, Philippa Hedges, and Glenda M. Halliday. Postmortem analysis of bilateral subthalamic electrode implants in parkinson's disease. *Movement Disorders*, 17(1):133–137, 2002.

[50] Mark H Histed, Vincent Bonin, and R. Clay Reid. Direct activation of sparse, distributed populations of cortical neurons by electrical microstimulation. *Neuron (Cambridge, Mass.)*, 63(4):508–522, 2009.

[51] Allen C. Ho, Mark S. Humayun, Jessy D. Dorn, Lyndon da Cruz, Gislin Dagnelie, James Handa, Pierre-Olivier Barale, José-Alain Sahel, Paulo E. Stanga, Farhad Hafezi, Avinoam B. Safran, Joel Salzmann, Arturo Santos, David Birch, Rand Spencer, Artur V. Cideciyan, Eugene de Juan, Jacque L. Duncan, Dean Eliott, Amani Fawzi, Lisa C. Olmos de Koo, Gary C. Brown, Julia A. Haller, Carl D. Regillo, Lucian V. Del Priore, Aries Arditi, Duane R. Geruschat, and Robert J. Greenberg. Long-term results from an epiretinal prosthesis to restore sight to the blind. *Ophthalmology*, 112(8):1547–1554, 2015.

[52] B.J. Hosticka. Dynamic cmos amplifiers. *IEEE Journal of Solid-State Circuits*, 15(5):881–886, 1980.

[53] Jui-Mei Hsu, Loren Rieth, Richard A. Normann, Prashant Tathireddy, and Florian Solzbacher. Encapsulation of an integrated neural interface device with parylene c. *IEEE Transactions on Biomedical Engineering*, 56(1):23–29, 2009.

[54] Jiannan Huang, Farah Laiwalla, Jihun Lee, Lingxiao Cui, Vincent Leung, Arto Nurmikko, and Patrick P. rcier. A 0.01-mm¡sup¿2¡/sup¿ mostly digital capacitor-less afe for distributed autonomous neural sensor nodes. *IEEE Solid-State Circuits Letters*, 1(7):162–165, 2018.

[55] K.K. Hung, P.K. Ko, C. Hu, and Y.C. Cheng. A physics-based mosfet noise model for circuit simulators. *IEEE Transactions on Electron Devices*, 37(5):1323–1333, 1990.

[56] Bruce Hutcheon and Yosef Yarom. Resonance, oscillation and the intrinsic frequency preferences of neurons. *Trends in Neurosciences*, 23(5):216–222, 2000.

[57] Jaeho Im, Jacob Breiholz, Shuo Li, Benton Calhoun, and David D. Wentzloff. A fully integrated 0.2v 802.11ba wake-up receiver with -91.5dbm sensitivity. In *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 339–342, 2020.

[58] J Jeng, S Tang, A Molnar, N J Desai, and S I Fried. The sodium channel band shapes the response to electric stimulation in retinal ganglion cells. *Journal of Neural Engineering*, 8(3):036022, may 2011.

[59] Hailin Jiang, M. Marek-Sadowska, and S.R. Nassif. Benefits and costs of power-gating technique. In *2005 International Conference on Computer Design*, pages 559–566, 2005.

[60] Ben Johnson, Shane T. Peace, Thomas A. Cleland, and Alyosha Molnar. A 50µm pitch, 1120-channel, 20khz frame rate microelectrode array for slice recording. In *2013 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pages 109–112, 2013.

[61] Ben Johnson, Shane T. Peace, Albert Wang, Thomas A. Cleland, and Alyosha Molnar. A 768-channel cmos microelectrode array with angle sensitive pixels for neuronal recording. *IEEE Sensors Journal*, 13(9):3211–3218, 2013.

[62] Seobin Jung, Paul Kwon, David Piech, Michel Maharbiz, Jan Rabaey, and Elad Alon. A 2.7-µW neuromodulation AFE with 200 mVpp differential-mode stimulus artifact canceler including on-chip LMS adaptation. *IEEE Solid-State Circuits Letters*, 1(10):194–197, 2018.

[63] Patrick J. Karas, Sungho Lee, Joohi Jimenez-Shahed, Wayne K. Goodman, Ashwin Viswanathan, and Sameer A. Sheth. Deep brain stimulation for obsessive compulsive disorder: Evolution of surgical stimulation target parallels changing model of dysfunctional brain circuits. *Frontiers in Neuroscience*, 12:998, 2019.

[64] Leslie M. Kay, Jennifer Beshel, Jorge Brea, Claire Martin, Daniel Rojas-Líbano, and Nancy Kopell. Olfactory oscillations: the what, how and what for. *Trends in Neurosciences*, 32(4):207 – 214, 2009.

[65] Young-Tae Kim, Robert W Hitchcock, Michael J Bridge, and Patrick A Tresco. Chronic response of adult rat brain tissue to implants anchored to the skull. *Biomaterials*, 25(12):2229–2237, 2004.

[66] Maria Kindlundh, Peter Norlin, and Ulrich G. Hofmann. A neural probe process enabling variable electrode configurations. *Sensors and Actuators B: Chemical*, 102(1):51–58, 2004. Selected papers from Transducers 03.

[67] E.A.M. Klumperink and B. Nauta. Systematic comparison of hf cmos transconductors. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 50(10):728–741, Oct 2003.

[68] Rahul M. Kodkani and Lawrence E. Larson. A 24-ghz cmos passive subharmonic mixer/downconverter for zero-if applications. *IEEE Transactions on Microwave Theory and Techniques*, 56(5):1247–1256, May 2008.

[69] Andrew Koivuniemi, Seth J. Wilks, Andrew J. Woolley, and Kevin J. Otto. Chapter 10 - multimodal, longitudinal assessment of intracortical microstimulation. In Jens Schouenborg, Martin Garwicz, and Nils Danielsen, editors, *Brain Machine Interfaces: Implications for Science, Clinical Practice and Society*, volume 194 of *Progress in Brain Research*, pages 131–144. Elsevier, 2011.

[70] Morten L. Kringelbach, Ned Jenkinson, Sarah L.F. Owen, and Tipu Z. Aziz. Translational principles of deep brain stimulation. *Nature Reviews Neuroscience*, 8:623–635, Aug. 2007.

[71] Sashank Krishnamurthy and Ali M. Niknejad. Enhanced passive mixer-first receiver driving an impedance with 40db/decade roll-off, achieving +12dbm blocker-p1db, +33dbm iip3 and sub-2db nf degradation for a 0dbm blocker. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 139–142, June 2019.

[72] Sashank Krishnamurthy and Ali M. Niknejad. Design and analysis of enhanced mixer-first receivers achieving 40-db/decade rf selectivity. *IEEE Journal of Solid-State Circuits*, 55(5):1165–1176, May 2020.

[73] Sashank Krishnamurthy and Ali M. Niknejad. Synthesis and design of enhanced ¡italic¿n¡/italic¿-path filters with 60-db/decade rf selectivity. *IEEE Solid-State Circuits Letters*, 3:522–525, 2020.

[74] Sashank Krishnamurthy and Ali M. Niknejad. An enhanced mixer-first receiver with distortion cancellation, achieving 80-db/decade rf selectivity and +8-dbm b1db for adjacent channel blockers. *IEEE Solid-State Circuits Letters*, 4:64–67, 2021.

[75] F. Krummenacher. Micropower switched capacitor biquadratic cell. *IEEE Journal of Solid-State Circuits*, 17(3):507–512, 1982.

[76] S. W. Lee, K. Thyagarajan, and S. I. Fried. Micro-coil design influences the spatial extent of responses to intracortical magnetic stimulation. *IEEE Transactions on Biomedical Engineering*, 66(6):1680–1694, June 2019.

[77] Seung Woo Lee, Florian Fallegger, Bernard D. F. Casse, and Shelley I. Fried. Implantable microcoils for intracortical magnetic stimulation. *Science Advances*, 2(12), 2016.

[78] Seung Woo Lee and Shelley Fried. Magnetic stimulation of subthalamic nucleus neurons using micro-coils for deep brain stimulation. *International IEEE/EMBS Conference on Neural Engineering*, pages 133–135, 11 2013.

[79] Seung Woo Lee and Shelley I. Fried. Suppression of subthalamic nucleus activity by micromagnetic stimulation. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 23(1):116–127, 2015.

[80] Seung Woo Lee, Kyou Sik Min, Joonsoo Jeong, Junghoon Kim, and Sung June Kim. Monolithic encapsulation of implantable neuroprosthetic devices using liquid crystal polymers. *IEEE Transactions on Biomedical Engineering*, 58(8):2255–2263, 2011.

[81] Seung Woo Lee, Jong-Mo Seo, Seungmin Ha, Eui Tae Kim, Hum Chung, and Sung June Kim. Development of Microelectrode Arrays for Artificial Retinal Implants Using Liquid Crystal Polymers. *Investigative Ophthalmology & Visual Science*, 50(12):5859–5866, 12 2009.

[82] Sunwoo Lee, Alejandro J. Cortese, Paige Trexel, Elizabeth R. Agger, Paul L. McEuen, and Alyosha C. Molnar. A 330μm×90μm optoelectronically integrated wireless system-on-chip for recording of neural activities. In *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, pages 292–294, 2018.

[83] Sunwoo Lee, Alejandro Javier Cortese, Aasta Parin Gandhi, Elizabeth Rose Agger, Paul L. McEuen, and Alyosha Christopher Molnar. A 250 μm × 57 μm microscale opto-electronically transduced electrodes (MOTEs) for neural recording. *IEEE Transactions on Biomedical Circuits and Systems*, 12(6):1256–1266, 2018.

[84] Sunwoo Lee, Alejandro Javier Cortese, Aaron Mok, Chunyan Wu, Tianyu Wang, Ju Uhn Park, Conrad Smart, Shahaboddin Ghajari, Devesh Khilwani, Sanaz Sadeghi, Yanxin Ji, Jesse H. Goldberg, Chris Xu, Paul L. McEuen, and Alyosha Christopher Molnar. Fabrication of injectable micro-scale opto- electronically transduced electrodes (motes) for physiological monitoring. *Journal of Microelectromechanical Systems*, 29(5):720–726, 2020.

[85] Shao-Yu Lien, Shin-Lin Shieh, Yenming Huang, Borching Su, Yung-Lin Hsu, and Hung-Yu Wei. 5g new radio: Waveform, frame structure, multiple access, and initial access. *IEEE Communications Magazine*, 55(6):64–71, June 2017.

[86] Yuan-Ching Lien, Eric A. M. Klumperink, Bernard Tenbroek, Jon Strange, and Bram Nauta. Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback. *IEEE Journal of Solid-State Circuits*, 53(5):1348–1360, May 2018.

[87] Yuanching Lien, Eric Klumperink, Bernard Tenbroek, Jon Strange, and Bram Nauta. 24.3 a high-linearity cmos receiver achieving +44dbm iip3 and +13dbm b¡inf¿1db¡/inf¿ for saw-less lte radio. In *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 412–413, Feb 2017.

[88] Yuanching Lien, Eric Klumperink, Bernard Tenbroek, Jon Strange, and Bram Nauta. A mixer-first receiver with enhanced selectivity by capacitive positive feedback achieving +39dbm iip3 and lt;3db noise figure for saw-less lte radio. In *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 280–283, June 2017.

[89] Deng Luo, Milin Zhang, and Zhihua Wang. A low-noise chopper amplifier designed for multi-channel neural signal acquisition. *IEEE Journal of Solid-State Circuits*, 54(8):2255–2265, 2019.

[90] Liangjian Lyu, Dawei Ye, and C.-J. Richard Shi. A 340nw/channel neural recording analog front-end using replica-biasing lnas to tolerate 200mvpp interfere from 350mv power supply. In *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–4, 2019.

[91] Douglas McCreery, Victor Pikov, and Philip R Troyk. Neuronal loss due to prolonged controlled-current stimulation with chronically implanted microelectrodes in the cat cerebral cortex. *Journal of Neural Engineering*, 7(3):036005, May 2010.

[92] Adam E. Mendrela, Kanghwan Kim, Daniel English, Sam McKenzie, John P. Seymour, György Buzsáki, and Euisik Yoon. A high-resolution opto-electrophysiology system with a miniature integrated headstage. *IEEE Transactions on Biomedical Circuits and Systems*, 12(5):1065–1075, 2018.

[93] Ahmad Mirzaei, Hooman Darabi, John C. Leete, Xinyu Chen, Kevin Juan, and Ahmad Yazdi. Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers. *IEEE Journal of Solid-State Circuits*, 44(10):2678–2688, Oct 2009.

[94] Matthew Morton, Yan Chen, Alyosha Molnar, Edward Szoka, and Robin Ying. The rf sampler: Chip-scale frequency conversion and filtering enabling affordable element-level digital beamforming. In *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, pages 1–5, Oct 2018.

[95] Naser Mousavi, Zhiheng Wang, Danijela Cabric, and Ramesh Harjani. A 0.4–1.0 ghz, 47 mhop/s frequency-hopped txr front end with 20 db in-band blocker rejection. *IEEE Journal of Solid-State Circuits*, 54(7):1917–1928, July 2019.

[96] Rikky Muller, Simone Gambini, and Jan M. Rabaey. A 0.013 mm^2, 5 μw, dc-coupled neural signal acquisition ic with 0.5 v supply. *IEEE Journal of Solid-State Circuits*, 47(1):232–243, 2012.

[97] Rikky Muller, Hanh-Phuc Le, Wen Li, Peter Ledochowitsch, Simone Gambini, Toni Bjorninen, Aaron Koralek, Jose M. Carmena, Michel M. Maharbiz, Elad Alon, and Jan M. Rabaey. A minimally invasive 64-channel wireless µecog implant. *IEEE Journal of Solid-State Circuits*, 50(1):344–359, 2015.

[98] Marc W. Murphy, Ezz I. El-Masry, and Amro M. Elshurafa. A high compliance input and output regulated body-driven current mirror for deep-submicron cmos. In *2006 International Conference on Microelectronics*, pages 13–16, 2006.

[99] Shin Nagayama, Ryota Homma, and Fumiaki Imamura. Neuronal organization of olfactory bulb circuits. *Frontiers in Neural Circuits*, 8:98, 2014.

[100] B. Nauta. A cmos transconductance-c filter technique for very high frequencies. *IEEE Journal of Solid-State Circuits*, 27(2):142–153, Feb 1992.

[101] Anders Nejdel, Mohammed Abdulaziz, Markus Törmänen, and Henrik Sjöland. A positive feedback passive mixer-first receiver front-end. In *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 79–82, May 2015.

[102] Kian Ann Ng and Yong Ping Xu. A low-power, high cmrr neural amplifier system employing cmos inverter-based otas with cmfb through supply rails. *IEEE Journal of Solid-State Circuits*, 51(3):724–737, 2016.

[103] M. S. Nielsen, C. R. Bjarkam, J. C. Sørensen, M. Bojsen-Møller, N. Aa. Sunde, and K. Østergaard. Chronic subthalamic high-frequency deep brain stimulation in parkinson's disease – a histopathological study. *European Journal of Neurology*, 14(2):132–138, 2007.

[104] Emilia Noorsal, Kriangkrai Sooksood, Hongcheng Xu, Ralf Hornig, Joachim Becker, and Maurits Ortmanns. A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants. *IEEE Journal of Solid-State Circuits*, 47(1):244–256, 2012.

[105] Richard A Normann, Bradley A Greger, Paul House, Samuel F Romero, Francisco Pelayo, and Eduardo Fernandez. Toward the development of a cortically based visual neuroprosthesis. *Journal of Neural Engineering*, 6(3):035001, May 2009.

[106] Archana Pandey. Recent trends in novel semiconductor devices. *Silicon*, 2022.

[107] Ramin Pashaie, Polina Anikeeva, Jin Hyung Lee, Rohit Prakash, Ofer Yizhar, Matthias Prigge, Divya Chander, Thomas J. Richner, and Justin Williams. Optogenetic brain interfaces. *IEEE Reviews in Biomedical Engineering*, 7:3–30, 2014.

[108] Shane T. Peace, Benjamin C. Johnson, Guoshi Li, Martin E. Kaiser, Izumi Fukunaga, Andreas T. Schaefer, Alyosha C. Molnar, and Thomas A. Cleland. Coherent olfactory bulb gamma oscillations arise from coupling independent columnar oscillators. *bioRxiv*, 2017.

[109] P. Hunter Peckham and Jayme S. Knutson. Functional electrical stimulation for neuromuscular applications. *Annual Review of Biomedical Engineering*, 7(1):327–360, 2005.

[110] Angel V. Peterchev, Stefan M. Goetz, Gregory G. Westin, Bruce Luber, and

Sarah H. Lisanby. Pulse width dependence of motor threshold and input–output curve characterized with controllable pulse parameter transcranial magnetic stimulation. *Clinical Neurophysiology*, 124(7):1364–1372, 2013.

[111] Farshad Piri, Matteo Bassi, Niccolò Lacaita, Andrea Mazzanti, and Francesco Svelto. A >40db irr, 44% fractional-bandwidth ultra-wideband mm-wave quadrature lo generator for 5g networks in 55nm cmos. In *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, pages 368–370, Feb 2018.

[112] Vadim S. Polikov, Patrick A. Tresco, and William M. Reichert. Response of brain tissue to chronically implanted neural electrodes. *Journal of Neuroscience Methods*, 148(1):1–18, 2005.

[113] M. Quarantelli, M. Poles, M. Pasotti, and P. Rolandi. A high compliance cmos current source for low voltage applications. In *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03.*, volume 1, pages I–I, 2003.

[114] Michael C. Quirk, Kenneth I. Blum, and Matthew A. Wilson. Experience-dependent changes in extracellular spike amplitude may reflect regulation of dendritic action potential back-propagation in rat hippocampal pyramidal cells. *Journal of Neuroscience*, 21(1):240–248, 2001.

[115] James B. Ranck. Which elements are excited in electrical stimulation of mammalian central nervous system: A review. *Brain Research*, 98(3):417–440, 1975.

[116] F. Rattay. The basic mechanism for the electrical stimulation of the nervous system. *Neuroscience*, 89(2):335–346, 1999.

[117] Hamidreza Rezaee-Dehsorkh, Nassim Ravanshad, Reza Lotfi, Khalil Mafinezhad, and Amir M. Sodagar. Analysis and design of tunable amplifiers for implantable neural recording applications. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 1(4):546–556, 2011.

[118] Mario Rosanova, Silvia Casarotto, Andrea Pigorini, Paola Canali, Adenauer G. Casali, and Marcello Massimini. *Combining Transcranial Magnetic Stimulation with Electroencephalography to Study Human Cortical Excitability and Effective Connectivity*, pages 435–457. Humana Press, Totowa, NJ, 2012.

[119] Sang Baek Ryu, Angelique C Paulk, Jimmy C Yang, Mehran Ganji, Shadi A Dayeh, Sydney S Cash, Shelley I Fried, and Seung Woo Lee. Spatially confined responses of mouse visual cortex to intracortical magnetic stimulation from micro-coils. *Journal of Neural Engineering*, 17(5):056036, oct 2020.

[120] M. Tariqus Salam, Jose Luis Perez Velazquez, and Roman Genov. Seizure suppression efficacy of closed-loop versus open-loop deep brain stimulation in a rodent model of epilepsy. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 24(6):710–719, 2016.

[121] R. Salvador, S. Silva, P.J. Basser, and P.C. Miranda. Determining which mechanisms lead to activation in the motor cortex: A modeling study of transcranial magnetic stimulation using realistic stimulus waveforms and sulcal geometry. *Clinical Neurophysiology*, 122(4):748–758, 2011.

[122] Tarun Saxena, Lohitash Karumbaiah, Eric A. Gaupp, Radhika Patkar, Ketki Patil, Martha Betancur, Garrett B. Stanley, and Ravi V. Bellamkonda. The impact of chronic blood–brain barrier breach on intracortical electrode function. *Biomaterials*, 34(20):4703–4713, 2013.

[123] E. M. Schmidt, M. J. Bak, F. T. Hambrecht, C. V. Kufta, D. K. O'Rourke, and P. Vallabhanath. Feasibility of a visual prosthesis for the blind based on intracortical micro stimulation of the visual cortex. *Brain*, 119(2):507–522, Apr. 1996.

[124] Jonathan Scott and Peter Single. Compact nonlinear model of an implantable electrode array for spinal cord stimulation (scs). *IEEE Transactions on Biomedical Circuits and Systems*, 8(3):382–390, 2014.

[125] Prateek Kumar Sharma and Nagarjuna Nallam. Breaking the performance tradeoffs in n-path mixer-first receivers using a second-order baseband noise-canceling tia. *IEEE Journal of Solid-State Circuits*, 55(11):3009–3023, Nov 2020.

[126] Lynne R. Sheffler and John Chae. Neuromuscular electrical stimulation in neurorehabilitation. *Muscle & Nerve*, 35(5):562–590, 2007.

[127] Kriangkrai Sooksood. Wide current range and high compliance-voltage bulk-driven current mirrors: Simple and cascode. In *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pages 240–242, 2016.

[128] Greg Stuart, Jackie Schiller, and Bert Sakmann. Action potential initiation and propagation in rat neocortical pyramidal neurons. *The Journal of Physiology*, 505(3):617–632, 1997.

[129] E. C. Szoka, J. C. Werth, T. A. Cleland, S. Fried, and A. Molnar. Cmos neural probe with multi-turn micro-coil magnetic stimulation. In *2021 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2021.

[130] E. C. Szoka, J. C. Werth, S. Lee, J. Lee, A. J. Cortese, T. A. Cleland, S. Fried, and A. Molnar. Neural probe utilizing programmable micro-coil magnetic stimulation. In *2021 10th International IEEE/EMBS Conference on Neural Engineering (NER)*, pages 651–654, 2021.

[131] Edward C. Szoka and Alyosha Molnar. Circuit techniques for enhanced channel selectivity in passive mixer-first receivers. In *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 292–295, June 2018.

[132] Yonghui Tang and R.L. Geiger. Effects of open-loop nonlinearity on linearity of feedback amplifiers. In *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, volume 2, pages II–II, 2002.

[133] Armin Taschwer, Natalie Butz, Manuel Köhler, Daniel Rossbach, and Yiannos Manoli. A charge balanced neural stimulator with 3.3 V to 49 V supply compliance and arbitrary programmable current pulse shapes. In *2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pages 1–4, 2018.

[134] H. Tsubokawa and W. N. Ross. Ipsps modulate spike backpropagation and associated [ca2+]i changes in the dendrites of hippocampal ca1 pyramidal neurons. *Journal of Neurophysiology*, 76(5):2896–2906, 1996. PMID: 8930242.

[135] Preeti Verma, Arti Noor, Ajay K. Sharma, and Sampath Kumar V. Power gating and its repercussions—a review. In *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, pages 1–6, 2016.

[136] R.J. Vetter, J.C. Williams, J.F. Hetke, E.A. Nunamaker, and D.R. Kipke. Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex. *IEEE Transactions on Biomedical Engineering*, 51(6):896–904, 2004.

[137] Tim Wagner, Felipe Fregni, Uri Eden, Ciro Ramos-Estebanez, Alan Grodzinsky, Markus Zahn, and Alvaro Pascual-Leone. Transcranial magnetic stimulation and stroke: A computer-based human model study. *NeuroImage*, 30(3):857–870, 2006.

[138] Bing Wang, J.R. Hellums, and C.G. Sodini. Mosfet thermal noise modeling for analog integrated circuits. *IEEE Journal of Solid-State Circuits*, 29(7):833–835, 1994.

[139] James D. Weiland and Mark S. Humayun. Retinal prosthesis. *IEEE Transactions on Biomedical Engineering*, 61(5):1412–1424, 2014.

[140] Andrew C. Weitz, Devyani Nanduri, Matthew R. Behrend, Alejandra Gonzalez-Calle, Robert J. Greenberg, Mark S. Humayun, Robert H. Chow, and James D. Weiland. Improving the spatial resolution of epiretinal implants by increasing stimulus pulse duration. *Science Translational Medicine*, 7(318):318ra203–318ra203, 2015.

[141] P. Werginz, S.I. Fried, and F. Rattay. Influence of the sodium channel band on retinal ganglion cell excitation during electric stimulation – a modeling study. *Neuroscience*, 266:162–177, 2014.

[142] Thomas Wichmann and Mahlon R. DeLong. Deep brain stimulation for neurologic and neuropsychiatric disorders. *Neuron*, 52:197–204, Oct. 2006.

[143] K.R. Williams, K. Gupta, and M. Wasilik. Etch rates for micromachining processing-part ii. *Journal of Microelectromechanical Systems*, 12(6):761–778, 2003.

[144] Blake S. Wilson and Michael F. Dorman. Cochlear implants: current designs and future possibilities. *Journal of rehabilitation research and development*, 45:695–730, 2008.

[145] Blake S. Wilson, Charles C. Finley, Dewey T. Lawson, Robert D. Wolford, Donald K. Eddington, and William M. Rabinowitz. Better speech recognition with cochlear implants. *Nature*, 352:236–238, Jul. 1991.

[146] Yan T. Wong, Norbert Dommel, Philip Preston, Luke E. Hallum, Torsten Lehmann, Nigel H. Lovell, and Gregg J. Suaning. Retinal neurostimulator for a multifocal vision prosthesis. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 15(3):425–434, 2007.

[147] Charles Wu, Yanjie Wang, Borivoje Nikolic, and Christopher Hull. A passive-mixer-first receiver with lo leakage suppression, 2.6db nf, gt;15dbm wide-band iip3, 66db irr supporting non-contiguous carrier aggregation. In *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2015.

[148] Dong Yang and Alyosha Molnar. A widely tunable active duplexing transceiver with same-channel concurrent rx/tx and 30db rx/tx isolation. In *2014 IEEE Radio Frequency Integrated Circuits Symposium*, pages 321–324, June 2014.

[149] Lan Yue, Paulo Falabella, Punita Christopher, Varalakshmi Wuyyuru, Jessy Dorn, Paulo Schor, Robert J. Greenberg, James D. Weiland, and Mark S. Humayun. Ten-year follow-up of a blind patient chronically implanted with epiretinal prosthesis argus i. *Ophthalmology*, 122(12):2545–2552.e1, 2015.

[150] Jing-Hong Conan Zhan, Brent R. Carlton, and Stewart S. Taylor. A broadband low-cost direct-conversion receiver front-end in 90 nm cmos. *IEEE Journal of Solid-State Circuits*, 43(5):1132–1137, May 2008.

[151] Sining Zhou and M.-C.F. Chang. A cmos passive mixer with low flicker noise for low-power direct-conversion receiver. *IEEE Journal of Solid-State Circuits*, 40(5):1084–1093, May 2005.

[152] Zhangming Zhu, Jianbin Mo, and Yintang Yang. A low voltage bulk-driving pmos cascode current mirror. In *2008 9th International Conference on Solid-State and Integrated-Circuit Technology*, pages 2008–2011, 2008.