

MICRO AND MILLIMETER WAVE CIRCUIT DESIGN IN SILICON WITH
CONSIDERATIONS FOR NOISE REDUCTION AND ON-CHIP PASSIVE
ELEMENTS

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Amid the exponentially growing demand of wireless multimedia applications, the need for exceptionally high performance communication devices has leapt to the forefront of electronic design. Advances in the speed of the silicon transistor and increased complexity of the integrated circuit metallization stack, along with sophisticated Electro-Magnetic (EM) simulation software has fortified the capability to meet new and seemingly unrelenting requirements on a platform common to most consumer electronics.

A comprehensive design approach for implementing micro and millimeter wave wireless transceiver front-end circuits is proposed. The design methodology exploits the aforementioned advances to ensure successful implementation of radio frequency circuits operating anywhere from 2-100 GHz in both standard silicon CMOS and silicon germanium (SiGe) BiCMOS technologies. In this dissertation the most substantial work performed is on the design and characterization of a variety of low noise amplifiers (LNAs). In the LNA arena, a new figure-of-merit (FOM) equation is proposed. Other successful demonstrations of transceiver circuits are also covered such as a direct down converter featuring an active balun at 94 GHz, and radio frequency identification (RFID) tags with an active transmitter at 24 GHz and 60

GHz. The methodology is not limited to the above circuits. It can be applied to a myriad of other circuits where the operating frequency is high, noise must be curtailed and the dimensions of passive structures are comparable to the signal wavelength.

Many of the techniques employed are intended to combat the limitations of the silicon substrate; even beyond the frequency limitations of the devices, and towards overcoming and in some cases exploiting the parasitic effects of interconnect wiring at increased frequencies. Simulation and Measurement results from the circuits are presented and an integrated simulation environment is proposed to simplify the design flow. Several successful hardware demonstrations confirm the validity of the proposed design methodology. Summaries are given at the end of each chapter and future research direction is highlighted at the end of the dissertation.

BIOGRAPHICAL SKETCH

Javier Alvarado Jr. was born on October 24, 1979 in Panama City, Panama to Javier and Dilcia Alvarado and came to the United States in 1981. He grew up in New York City with siblings Jonatan and Jellissa under the watchful eyes of his parents and grandparents. Javier graduated from Brooklyn Technical High School in Brooklyn, NY in 1997. He received his undergraduate education from Cornell University in Ithaca, NY. He graduated Cum Laude in May 2002 with a Bachelor of Science in Electrical and Computer Engineering. Beginning in August 2002 Javier continued his studies at Cornell University, receiving a Masters of Science degree in Electrical and Computer Engineering in August 2005, and a PhD in Electrical and Computer Engineering with a minor in Earth and Atmospheric Sciences in August 2007. During his education, Javier spent over a year working with the Corporate Technology Group at Intel Corporation in Hillsboro, OR and another year performing research at the Georgia Electronic Design Center at the Georgia Institute of Technology in Atlanta, GA. In 2004 Javier was the recipient of a GEM fellowship sponsored by Intel.

To My Family and Friends for Their Love and Support

ACKNOWLEDGEMENTS

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Finally, I would like to whole heartedly thank all the members of the Office of Minority Educational Affairs and the Diversity Programs in Engineering office at Cornell, especially Malinda Smith and Elisa Johnson for ensuring my development as a socially responsible and culturally aware individual through many years of mentorship. I must also give thanks to the National Society of Black Engineers. This organization has been absolutely vital to my academic and professional success by providing endless opportunities for career development, collegiate scholarships, and social networking.

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Chapter 1: Introduction

1.1 Overview

Technology scaling and the stability of Moore's law have paved the way for ever faster transistors, with transition frequencies (f_t) exceeding 100 GHz and 200 GHz for today's 90nm CMOS and 120nm SiGe, respectively. The realization of functional circuits operating at or above half f_t is a difficult task, and the subject of much of this dissertation. The primary advantages of silicon-based technologies are the promise of high levels of integration and low manufacturing cost.

Throughout the past decade or so, the wireless communication industry has experienced tremendous expansion that has been fueled by many factors such as advancement of silicon technology, an abundance of internet users, profound investment from governments and industries, consumer demands for more robust mobile voice and data solutions, and interest in biomedical applications. Despite the many differences and developments in the back-end and signal processing schemes from analog wireless technology to newer digital technology, the wireless transceiver front-end architecture has remained relatively constant. In a common wireless transceiver system, a received signal on the antenna needs to be filtered and amplified before it is down-converted to a signal at much lower frequency than its carrier. The transmitting procedure is the roughly the reverse of the receiving process.

1.2 Motivation

Operation at high frequencies can support several interesting and important multi-gigabit/sec (Gb/s) applications such as, personal area networks for downloading media to mobile devices, Gb/s wireless for undeterred network connections, and high data rate point-to-point communication, and indoor video transmission. The key technology challenges for these applications are low-noise operation and high output power capability.

The fact that every wireless radio has to occupy a part of the spectrum, and with exponentially increasing number of wireless devices used daily, radio spectrum has become a precious resource. Recent spectrum auction price of more than two billion dollars for a 120 MHz of spectrum between 1.8 GHz and 1.9 GHz [1] shows just how valuable and competitive the wireless service industry has become. Due to the enormous cost in acquiring additional spectrum, many innovative solutions have surfaced to increase spectrum usage efficiency such as Ultra Wide Band, which covers a wide range of spectrum (3.1 to 10.6 GHz) with very little interference to existing signals within the spectrum [2].

Moving to higher frequencies with larger bandwidth allocations can conquer many of the limitations of contemporary systems, albeit while introducing new challenges. The millimeter wave (mm-Wave) frequency range can accommodate new potential applications such as automotive radar, medical imaging, and security, in addition to the aforementioned. Operation at such high frequency minimizes the size of the antenna which allows for on-chip integration. The ultimate goal is envisioned to be fully integrated systems (Antennas, RF, Analog and Digital components on one die using a single silicon process). Currently, the most feasible mm-Wave bands for these applications are from 56-64 GHz, 71-76 & 81-86 GHz, and 92-100 GHz. Additional bands exist beyond 100 GHz with even larger bandwidth allocations, and it

is anticipated the design techniques developed in this dissertation will be applicable to designing at those higher frequencies with further advances in silicon f_t .

1.3 Contributions to the Field

The work presented in the following chapters contributes to the field of wireless communications by developing certain design techniques and methodologies for micro and mm-Wave circuit design, and employing them in useful applications including the fastest reported silicon radio frequency identification (RFID) transponder, the highest reported figure-of-merit (FOM) for both a 60 and 90 GHz silicon low-noise amplifier (LNA), the lowest reported Noise Figure for both a 60 and 90 GHz silicon amplifier, the largest reported 3dB-bandwidth W-band LNA. The W-band receiver front-end reports the highest Conversion Gain published in silicon-based designs. A newly developed figure-of-merit equation is also proposed to the field which ranks broadband LNAs. Vital to this work is the development of techniques which enable single substrate integration, where we are able to fully exploit the benefits of silicon by eliminating interchip transitions. A number of new design techniques and inventions are presented for the RFID development, most notably the system architecture and an introduction of a floating-bulk voltage multiplier in CMOS. LNA pursuits have lead to the development of a passive noise reduction layout technique and a new concept in SiGe device sizing which essentially exploits parasitic capacitances in order to tune unilateral and current gain peaking for operation frequencies upwards of 100 GHz.

1.4 Chapter Overviews

In chapter 2, combating the limitations of high frequency radio design in silicon technology is examined. This discussion includes overcoming the constraints of the silicon fabrication process, device modeling, and passive modeling. In chapter

3 we introduce the general methodology for successful implementation of high frequency transceiver circuit design. The design approach and measured results for passive noise reduction in SiGe microwave LNAs at 2.14, 2.45 and 5.25 GHz are discussed. In chapter 4 we present novel mm-Wave amplifier design techniques and measurement procedures along with schematics. Included in this chapter are several LNA examples from 60 GHz up to 100 GHz in SiGe and a proposed novel FOM equation. In chapter 5 a 94 GHz direct down-converter, with an integrated double-balanced mixer and active balun in SiGe is described. In chapter 6 the discussion shifts to the detailed design of mm-Wave passive RFID transponders in 90nm CMOS. We concluded in chapter 7 with future research directions.

Chapter 2: Facing Challenges of Radio Design in Silicon

2.1 Overview

In this chapter constraints on the design of micro and mm-wave front-end integrated circuits are discussed, along with how they are combated. At high frequency, the loss through the silicon substrate becomes extreme, and isolation between active components is a serious issue for a designer to consider. Phenomena such as cross talk, substrate coupling, and substrate noise corrupt sensitive signals between devices. In addition to the aforementioned restrictions, issues associated with accurate passive element modeling and simulating also exist. Transistor gate leakage current and parasitics (especially un-modeled parasitics) also can be a great hindrance. The objective of this chapter is to outline some of the difficulties a designer faces when creating circuits at very high frequencies and to propose a design technique to overcome these issues. This leads to the remaining chapters that describe several successful design implementations and details of their validation.

2.2 Constraints from Active Silicon Device Modeling

Constraints from CMOS and SiGe active devices are due to aspects of their fabrication process, and poor or even non-existent device modeling for deep sub-micron transistor technology. Since some key fabrication parameters are protected commercial secrets, the following discussion is based on issues common to all silicon processes, which share the same fundamental principles in active device operation.

Therefore conclusions drawn from the generic process are applicable to all CMOS and SiGe hetero-junction bipolar transistor (HBT) based design.

Difficulty of active device modeling (i.e., transistor behavior) increases with operating frequency. At high frequency a simple model, such as the one in Figure 2-1, often fails to consider many complex physical effects that are critical for design success. In radio frequency integrated circuit (RFIC) design, one must optimize each device for power, noise, linearity and small/large signal parameters. All of which are functions of device size, biasing point, temperature, process and frequency. These dependencies are not always linear and often must be realized experimentally to fit and/or correct modeling equations.

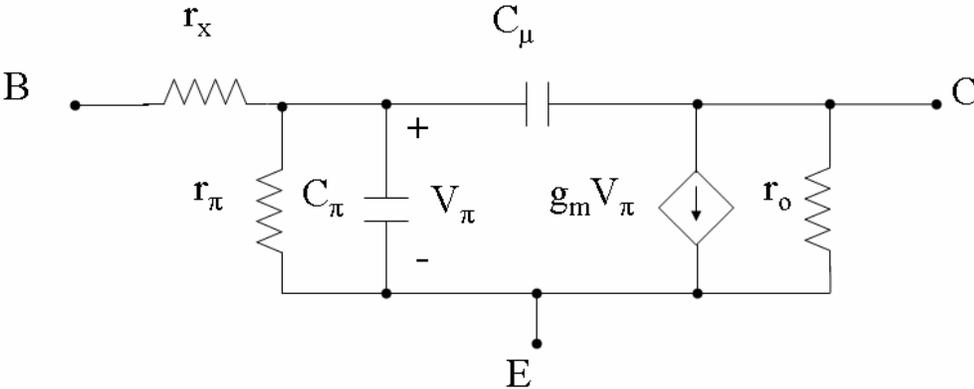


Figure 2-1: Simple BJT Small Signal Model

Accurate transistor modeling is the vital to the successful design of very high frequency RFICs. However, complex model accuracy comes at the expense of simulation speed and resources. A good compromise for achieving both high simulation speed and model accuracy for silicon devices has and continues to be the topic of many research efforts. One example of a SiGe HBT model for high frequencies presented by [3] is illustrated in Figure 2-3. This is one step closer to the desired “perfect” solution.

The model depicted in Figure 2-3 derives its parameters from actual tests performed for a single device under desirable testing conditions and a high level of accuracy [3]. Some of the illustrated device parameters are linearly extrapolated and some are not. Extrapolation methods depend on both actual data points and knowledge of device physics, which in turn often dictates relationships between device size and its parameters. According to [3][3], simulated scattering parameters (S-Parameters) of this model match measurement results within 10% error at 40 GHz. In addition, the derived noise model predicts noise figures of the device within 0.1 dB of measurement at 5GHz. However, the model generates much larger error in predicting noise figure at higher frequencies; this is attributed mostly to substrate loss [3].

A very practical issue that contributes to high frequency model inaccuracy is

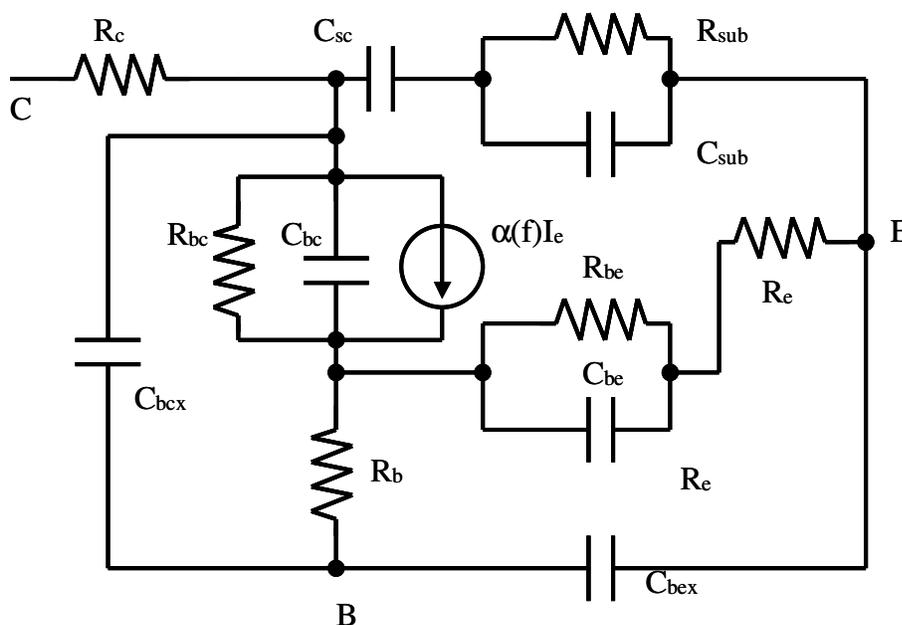


Figure 2-2: Example of a SiGe HBT high frequency model

that extracted device parameters quite often have a strong dependency on test setup. This is due to the passive structures and interconnects required between test equipment

and the device under test which contribute to the overall parameter extraction. An improperly de-embedded structure will lead to inaccurate modeling parameters. One must also realize that there are limitations imposed by foundry models over device parameters which can harm critical circuit performance due to variations of those parameters that are dependant on temperature, process, and bias conditions.

2.3 Silicon Substrate Loss

A major factor that makes III-V compound process technologies such as GaAs and InP attractive for micro and millimeter wave IC design, is their low-loss substrate. Given the small dimensions (submicron) of modern processing technology, devices are placed very close to each other despite having completely different functionality in the overall system. Inevitably noise, cross-talk and coupling of signals between adjacent devices becomes a serious issue in analog and RF circuits where each circuit element should be isolated from one another. In silicon, the lossy substrate introduces finite resistance to ground, and now unwanted paths between various devices, which attenuates and corrupts critical signals. This is illustrated in Figure 2-3 [4].

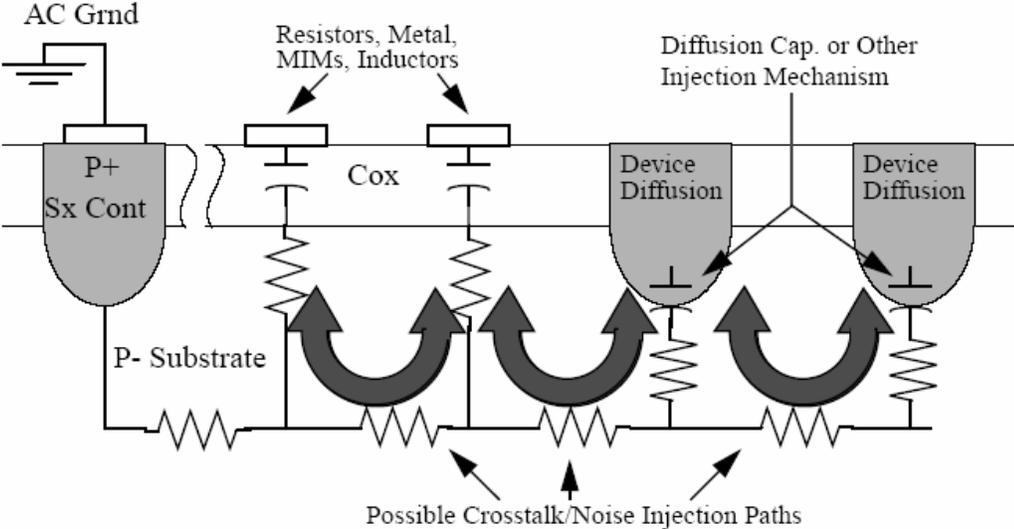


Figure 2-3: Lossy Substrate Noise and Coupling Paths

According to [5] and [6], the SiGe P- substrate resistivity is 11-20 $\Omega\cdot\text{cm}$ with a substrate thickness of 300 μm , which means that the substrate can be viewed as a thermal noise source. The problem of substrate coupling becomes increasingly evident as the number of noise generators (active devices) grows. For instance, in a mixed-signal application, thousands of transistors may inject noise into the substrate especially during clock switching. Increasing the physical spacing between critical or sensitive sections of a chip might seem to help, however, many mix-signal systems can be so heavily blended separation is very difficult. What must also be considered is increased distance requires longer interconnects, degrading performance [7].

In order to lessen the negative effects (crosstalk, coupling, and noise) of the lossy (lightly-doped) P- substrate, continuous rings of P+ grounded substrate contacts around sensitive circuits can be employed. These structures, known as guard rings, provide a low impedance path to ground for charge carriers produced in the substrate. This is the basis of the noise reduction technique described in Chapter 3 and is heavily utilized throughout this dissertation. The desired effect is shown in Figure 2-4 [4].

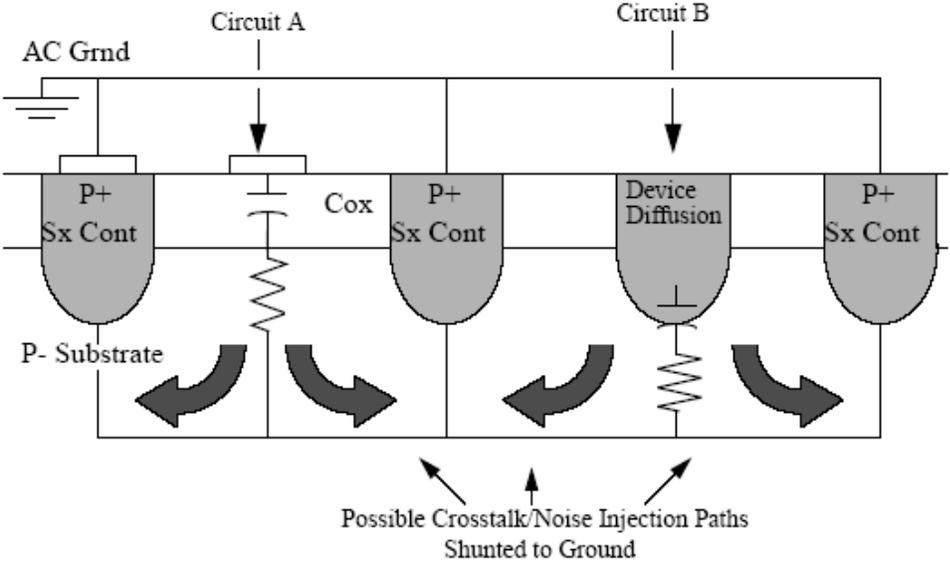


Figure 2-4: Low Resistance Path to Ground

2.4 Constraints from Passive Elements

Passive circuit elements (passives) are critical components of micro and millimeter wave IC design. The definition of passive structures discussed here includes elements such as filters, capacitors, pads, resistors, inductors, transmission lines, etc, elements that are located in the back-end layers. In addition, the semi-resistive silicon substrate places limitations on the quality factor (Q) of on chip passives. Figure 2-5, a realistic model for an on chip inductor, clearly shows an unwanted voltage divider formed between the inductor and the bulk. One can easily show that, the lower the substrate resistivity, the greater the coupling and in turn the lower the Q. For this reason, passive elements must use on-chip enhancements to shield signals from the substrate as much as possible. Metal ground plates, bipolar implant blocks, and if available, deep trenches (substrate cutouts), are employed in order to raise the bulk resistance below passive elements and hence improve their quality factor.

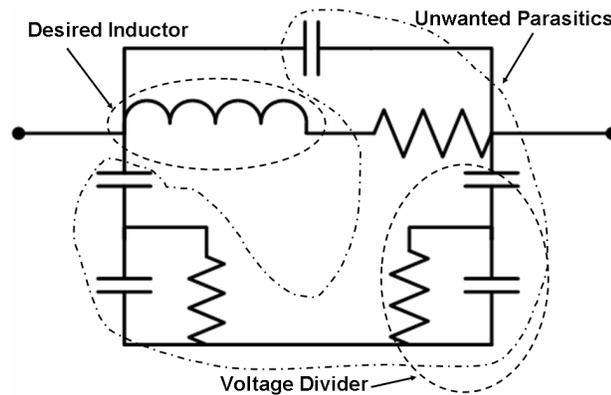


Figure 2-5: Representation of an On Chip Inductor Model

As if the lossy substrate itself wasn't constraining enough, current submicron silicon processes have very strict local and global density design rules that require the

presence of each available layer throughout a fabricated circuit. This seriously restricts the Q , size, and types of passive structures that can be effectively used. Some processes are so strict that a simple microstrip line cannot be fabricated without rule waivers or risk of highly inaccurate modeling. Given all these limitations, a combination of microstrip and coplanar transmission line becomes the ideal choice for an on-chip transmission line for MM Wave IC design. This hybrid transmission line, shown in Figure 2-6, is also used to help reduce noise and coupling using a conductive path to ground the substrate (CPGS) technique, is described in Chapter 4 and in [8].

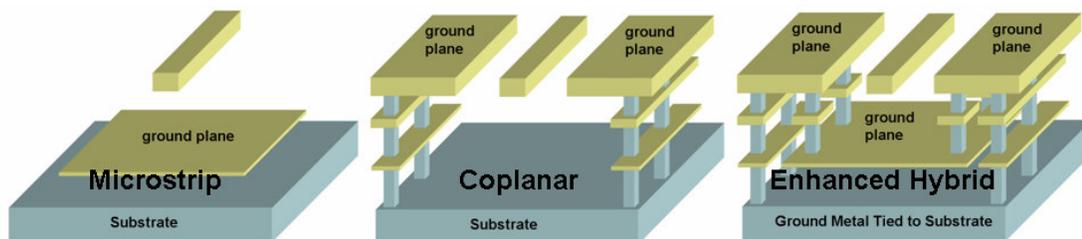


Figure 2-6: Microstrip, Coplanar, and Hybrid T-lines

Figure 2.6 shows the difference between microstrip line, coplanar line, and the combination of both, which is the ideal choice for high frequency applications. In the microstrip line, signal wave propagation is in hybrid mode, namely both TE and TM. This complicates the analysis and model accuracy of microstrip lines. In order to improve on the microstrip line, a coplanar structure that introduces additional ground planes to the signal line can be combined to make a semi-enclosed box (Hybrid-T). The result is EM lines mostly confined by the surrounding ground structures and thus analysis of this structure is simplified and more accurate as stated in [9].

2.4.1 Electro-Magnetic Modeling

Accurate Electro-Magnetic (EM) modeling plays an important part in determining the robustness of passive structures. With the emergence of myriads of EM software on the market like, Micro-Wave Office (MWO) from Applied Wave Research, integrating EM simulation into the overall circuit simulation and design flow becomes easier. Some products such as HFSS from Ansoft Corporation or Sonnet from Sonnet Software offer a simulation environment that integrates directly into a layout tool in Cadence or ADS.

EM simulation is the ultimate tool in determining a passive structure's response under a wave excitation, but the setup is usually difficult and error-prone. To evaluate the correctness of a particular setup, a basic transmission line structure can be drawn using circuit CAD tools. Then the structure can be imported to the EM tools for scattering parameter (S-parameter) extraction. If the ports are set up correctly, the simulated S-parameters should match that of the foundry models, where EM simulation and actually measurement data are used to guarantee the model robustness. With confidence in the EM simulation setup, many structures in the layout environment can be imported for a thorough evaluation. Secondary effects such as skin effect and proximity effect will be taken into account, yielding parameters that closely replicate reality.

For passive structures with complex geometries, simple models that predict its frequency response fairly accurately at low frequencies often fail when extrapolated to higher frequencies. Therefore it is necessary to use mesh-based EM simulation tools to have much more accurate high frequency predictions. However, running EM numerical simulations takes a lot of resources and usually becomes unrealistic for a large chip where many passive structures are laid out. This requires one to model individual passives for their responses as well as interconnects between structures.

Figure 2-7 depicts a hybrid transmission line modeled in HFSS and a T-junction, used to interconnect three other structures, in MWO.

Another challenge in using EM simulation is the complexity of simulation setup. Even though several EM simulation software vendors have come up with ways to simplify structure import from CAD tools familiar to circuit designers (Ansoftlinks from Ansoft Corporation, for example), the port setup, which is responsible for mimicking the real EM wave excitation, can be complicated and error-prone. Unfortunately, an incorrect port setup usually results in wrong simulation data and renders final circuit simulation results useless. Therefore, if available a designer should use more than one EM tool for verification purposes.

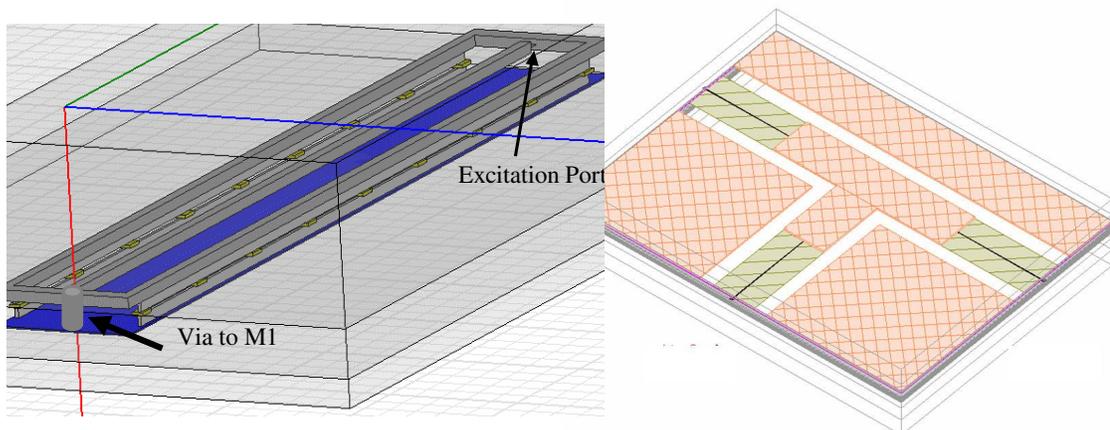


Figure 2-7: Hybrid T-line in HFSS and T-junction in MWO

2.4.2 Parasitic Extraction

Current circuit design environments have established methods of extracting parasitics associated with a particular layout. The extraction procedure is facilitated by metal layer proximities and dimensions. Their capacitances and resistances are calculated by some foundry-defined predetermined method. Inductance extraction is more difficult to determine because it is defined in a loop and the return path needs to

be known in order to be extracted. In addition, inductance is also affected by magnetic coupling between adjacent conductors. Furthermore, inductance is a frequency dependent parameter dictated by geometry. Finally, skin effect and proximity effect must also be considered in determining the inductor Q. There has been concentrated research on inductance extraction such as, FASTHENRY from MIT [10]. However, all the available methods are not automated and refined at the same level of RC extraction and therefore manual intervention in the design flow is required.

At very high frequency it becomes critical for any extraction method to account for parasitic components existing in the layout. In reality, however, extraction methods competent for low frequency extraction often fail at high frequencies. An accurate solution is needed for successful implementation of mm-Wave IC circuit design which does not introduce a significant increase in simulation time and effort. In this dissertation, all interconnect wiring is minimized and/or modeled wherever possible.

2.5 Proposed Design Flow for Radio Frequency Silicon Circuits

Traditionally, microwave RF circuit design in silicon usually began with circuit simulation; and then a schematic was drawn on a layout cell. The layout cell was extracted and compared to the original schematic to ensure correctness of connections. The extraction step adds parasitics on interconnects between each component. Simulation on the extracted design was the final stage in verifying the circuit performance and the designer did little or nothing to optimize the post-extraction design as long as design specifications were met. In mm-Wave IC design, this flow needs to be modified because parasitics become vital in matching networks and often vastly alter the performance of the initial schematic. A new design flow is

proposed here to give full considerations of parasitic effects on circuit performance, as well as substrate conditioning. Figure 2-8 illustrates the new proposed design flow.

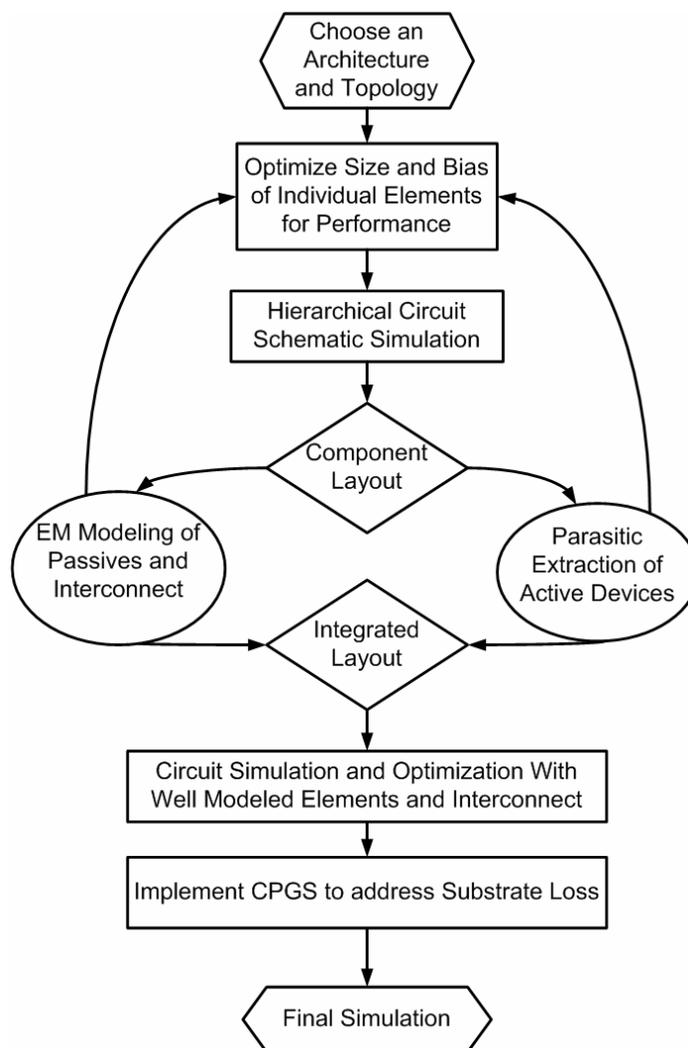


Figure 2-8: Proposed Silicon RF Design Flow

Schematic design begins with the choice of architecture and topology, which should be based on research of other successful implementations and good reasoning concerning innovations. Active devices and passives are part of the chosen topology. These should be optimized based on performance metrics (i.e., peak gain, noise figure,

signal swing, phase noise, etc.) and power consumption requirements. During the schematic simulation phase of the flow, the designer should try to record the overall circuit performance by paying close attention to the contribution of each component. This should be done in a hierarchical fashion so that different views/versions (schematic, extracted, S-parameter model, etc.) can be readily interchanged and back annotated. With added parasitics, some circuit parameters need to be modified and a laid out again. This is an iterative process and each time device parameters are altered, layout dimensions may have to change and thus new extraction is needed. However, if the original layout contains elements that are relatively stable, along with some foresights into the chip layout process, one can save tremendous amount of design time. For example, in the situation where three passive elements share a common node (i.e. t-lines), thus creating a T-junction as in Figure 2-7, a single EM model can be created. This model can be directly applied in schematic at every three element intersection and accurately simulated without ever going to the layout.

Utilizing hierarchy and EM simulation to observe parasitic effects and model interconnect helps to greatly minimize the number of unknowns, which maximizes ones chances for a successful design implementation. Implementing the conductive path to ground the substrate (CPGS) technique will ensure that noise, crosstalk and other ill-mannered bulk effects will be minimized. At the end of the design flow, one should see simulation results with well modeled elements and interconnects that closely represent reality.

2.6 Summary

This chapter discussed constraints on the design of micro and mm-wave front-end integrated circuits, and how they should be combated in order to successfully design RFICs in current silicon technology. Phenomena such as cross talk, substrate

coupling, and substrate noise that corrupt sensitive signals were examined. Other difficulties associated with modeling of silicon circuits at very high frequencies were also brought to attention. Models of silicon devices at high frequencies are derived from data extracted from device under test at certain conditions. Those data are extrapolated to fit all sizes and all operating conditions. At high frequencies improper de-embedded test setup can skew device parameters by a large margin, thus making it less reliable. Emphasis on the importance of parasitic extraction, and EM modeling of interconnects were also made. An integrated simulation environment was proposed and a novel design flow was presented. The following chapters will expand on the issues discussed in this chapter with several examples that illustrate how an optimized design methodology can make circuits more robust and their development process more efficient.

Chapter 3: Design of Microwave LNAs in SiGe

3.1 Overview

This chapter presents the design of LNAs for microwave RF applications in a 47 GHz f_t SiGe BiCMOS technology. Some discussion of LNA basic concepts is also offered for completeness. Circuit design, simulation as well as measurement results are discussed. The previously mentioned parasitic-aware circuit design methodology is used to maximize circuit performance and minimize impact of unwanted parasitics. Some discussion of LNA fundamentals along with topology choice is offered. This chapter demonstrates the validity of the proposed conductive path to ground the substrate (CPGS) design technique by comparing several identical designs with and without its implementation.

The fundamental goal of a low-noise amplifier is to provide gain to a signal, while adding very little noise. Since the LNA is the first gain stage in a receiver path, its' noise figure dominates that of the overall receiver [11]. After the LNA stage, the subsequent receiver components add noise to an already amplified signal, leading to a much better signal-to-noise ratio than an un-amplified signal. The LNA is an essential front-end component of which high performance is demanded. A respectable LNA should perform the aforementioned basic functions, while consuming little power and maintaining linear behavior over a wide input range. A superior LNA should be capable of doing all the things a respectable LNA can do in normal settings as well as perform soundly in a harsh environment (extreme temperatures) at equal or lower

fabrication cost. Of course these demands are difficult to meet since many of the LNA parameters are interrelated and have associated tradeoffs. A few universally known tradeoffs include: 1) *Gain vs. Noise Figure*: The higher gain the more inherent noise in the amplifier; high gain requires high DC bias current which increase base and collector shot noise. 2) *Gain vs. Linearity*: The higher the gain the lower the lower the 1dB compression point and the lower the input referred third-order intercept (IIP3). 3) *Input Match vs. Noise Figure*: The best noise figure is not obtained at the optimal input conjugate matching network. Due to these tradeoffs and more, an optimal LNA solution can only be achieved through compromise [12].

3.2 LNA Fundamentals

Low noise amplifiers are employed in the receivers of many wireless systems and are often vital to their performance. They must be able to operate while simultaneously contributing very little noise to the input signal, amplifying the signal significantly enough to mitigate the noise effects of later stages, accommodate a large range of input powers, typically while consuming very low power. An example of a wireless transceiver demonstrating the placement and application of the LNA can be seen in Figure 3-1.

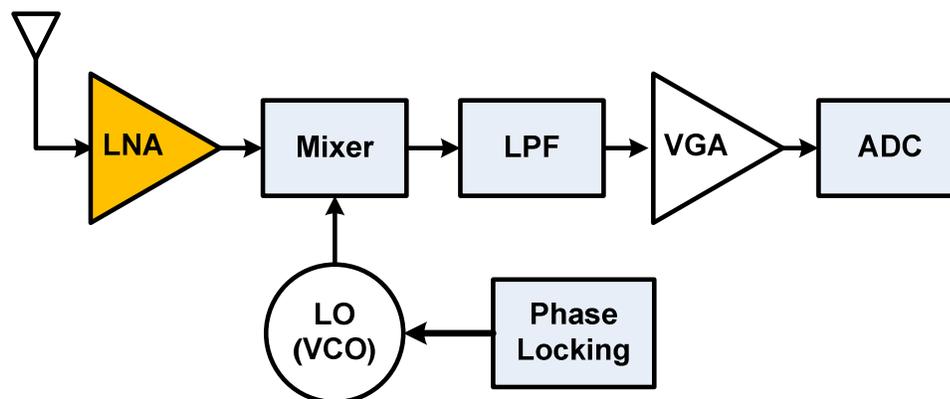


Figure 3-1: A simplified receiver block diagram

The LNA is also the first active circuit in the receive path of a transceiver. Assuming that the noise contribution of the antenna and is small the LNA is the most noise sensitive circuit in the system. Consider the following relationship for determining input referred noise of a receiver containing m cascaded stages [11]:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \frac{NF_3 - 1}{A_{p1}A_{p2}} + \dots + \frac{NF_m - 1}{A_{p1}\dots A_{p(m-1)}} \quad (3.2.1)$$

Where NF_m is the noise figure and A_{pm} is the available gain of stage m. From this relationship it can be seen that beyond achieving low noise the LNA (amplifier # 1) can lower the overall noise figure of the system by achieving high gain. In most receivers the contributions of the later stages are but a fraction of that of the LNA on the total system noise figure; however this may not be the case in the instance of a LNA with an extremely low noise figure or gain.

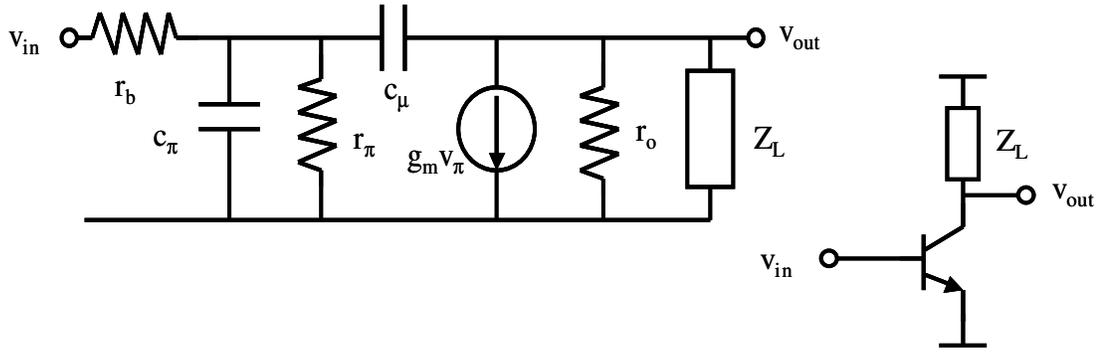


Figure 3-2: Common-emitter configuration and simplified small signal model

The most common configuration for an amplifier is common-emitter, shown in Figure 3-2. This is the simplest way to amplify a signal. Consider the small signal equivalent of the common-emitter circuit also shown in Figure 3-2. Using small signal analysis, the transfer function can be described as:

$$\frac{V_{out}}{V_{in}} = \frac{S - \frac{g_m}{c_\mu}}{c_\pi r_b [S^2 + S \left(\frac{1}{c_\pi \cdot r_b \parallel r_\pi} + \frac{1}{(c_\mu + c_\pi) \cdot Z_L \parallel r_o} + \frac{g_m}{c_\pi} \right) + \left(\frac{1}{c_\pi \cdot r_b \parallel r_\pi \cdot Z_L \parallel r_o} \right)]} \quad (3.2.2)$$

Simplifying this equation to gather more insight, the sum of gain adjusted C_μ and C_π clearly act as the principal pole in this circuit. From this pole it is easy to see that the transfer function is dominated by the base to collector capacitance C_μ and circuit power gain is significantly affected. Also the two capacitors, C_μ and C_π , will limit the bandwidth the amplifier. C_π will shunt RF input power to ground, and C_μ will introduce feedback at high frequencies. Since the voltage gain at the output node is $V_{out} = -g_m V_\pi (r_o \parallel Z_L)$, we get a multiplication factor applied to the capacitance C_μ , determined by the voltage ratio at either side of the capacitor and can be described as[13]:

$$C_{eq} = C_\mu \left(1 + g_m \left(\frac{r_o Z_L}{r_o + Z_L} \right) \right) \quad (3.2.3)$$

Which is an input referred effective shunt capacitance. Assuming r_π is large and using (3.2.3) the 3-dB roll-off frequency can be derived from the parallel combination of C_{eq} and C_π as:

$$\omega_{3dB} = \frac{1}{(R_s + r_x) (C_\pi + C_{eq})} \quad (3.2.4)$$

Equation (3.2.4) shows that while C_{μ} is typically quite small, it can have a very large impact on the bandwidth of the systems due to the exaggeration of its effect caused by the voltage imbalance across it. This along with a few other serious drawbacks of the common-emitter amplifier prevents its use in high frequency applications. However, much insight can be obtained from analyzing its noise performance using Figure 3-3, the following is observed:

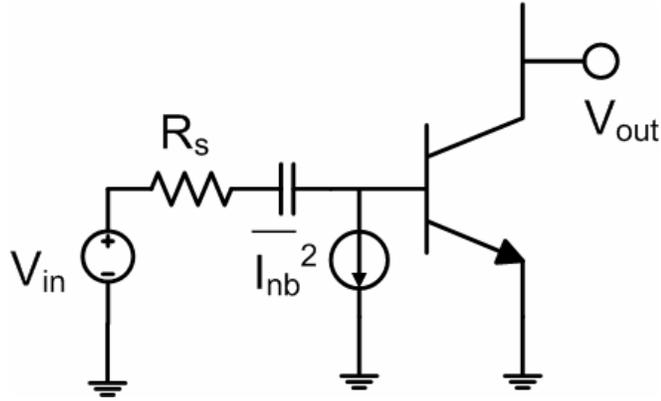


Figure 3-3: Common-emitter noise analysis

$$\overline{I_{nb}^2} = 4kT \frac{I_c / \beta}{2V_T} \quad (3.2.5)$$

$$\overline{V_{tot}^2} = 4kT \left(R_s + r_b + \frac{1}{2} g_m + \frac{g_m R_s^2}{2\beta} \right) \quad (3.2.6)$$

$$NF = \frac{\overline{V_{tot}^2}}{4kTR_s} = 1 + \frac{r_b}{R_s} + \frac{1}{2g_m R_s} + \frac{g_m R_s^2}{2\beta} \quad (3.2.7)$$

$$R_{s,opt} = \sqrt{\beta(1 + 2g_m r_b)} / g_m \Rightarrow NF_{min} \approx 1 + \sqrt{(1 + 2g_m r_b) / \beta} \quad (3.2.8)$$

The noise figure (NF) of the common-emitter amplifier is analyzed above can be controlled (to some extent) by manipulation of the device size and bias point.

Minimizing noise and maximizing gain amplification are essential in designing a quality LNA. However, those are not the only LNA characteristics that must be considered, linearity is also a vital metric. The linearity or how linear an amplifier, is gauged by resilience against intermodulation (mixing of two strongly interfering signals with the desired signal after amplification) and gain compression (the dynamic range of constant gain with respect to input power).

If we describe the input voltage signal to the LNA as:

$$x(t) = A \cos(\omega t) \quad (3.2.9)$$

Then the output voltage becomes:

$$y(t) = k_1 A \cos(\omega t) + k_2 A^2 \cos^2(\omega t) + k_3 A^3 \cos^3(\omega t) + \dots \quad (3.2.10)$$

The first few components of (3.2.10) can be described in terms of a dc shift, the fundamental output at ω , a second-order harmonic term at 2ω , and a third-order harmonic term at 3ω as follows:

$$y(t) = \frac{k_2 A^2}{2} + \left(k_1 A + \frac{3k_3 A^3}{4}\right) \cos(\omega t) + \frac{k_2 A^2}{2} \cos(2\omega t) + \frac{k_3 A^3}{4} \cos(3\omega t) \quad (3.2.11)$$

The small-signal gain is obtained by neglecting harmonics, in (3.2.11) it is k_1 . Gain compression occurs when harmonic components become comparable to the fundamental causing the gain to change with input amplitude. In RF circuits this is often quantified by the point at which the input power level causes the amplifier gain to be lowered by 1-dB known as “1-dB compression point,” or $P_{1\text{db}}$ [14].

The other performance metric that characterizes linearity in RF circuits is the “input third-order intercept point,” or IIP3. If we now describe the input voltage signal to the LNA as:

$$x(t) = A \cos(\omega_1 t) + A \cos(\omega_2 t) \tag{3.2.12}$$

The output signal will now contain the intermodulation (IM) products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. When spaced closely and are within the bandwidth of the amplifier, these product terms are of major concern. This is due to the fact that the fundamental ω_1 term grows linearly with input amplitude while the IM product grows as the cube of the input amplitude. This phenomenon is illustrated in Figure 3-4. IIP3 is obtained from an extrapolation of the fundamental and IM3 output power versus the input power. It is the point at which the power in the third-order product and the fundamental tone intersect.

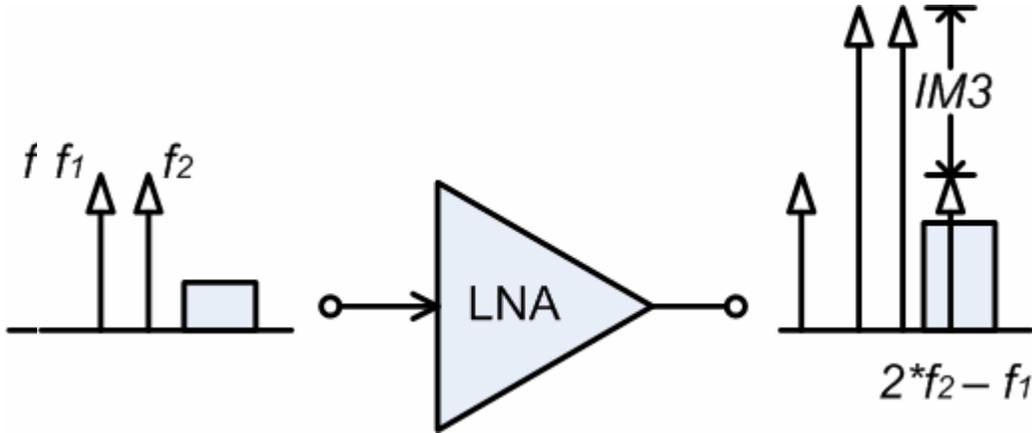


Figure 3-4: Desired Signal Band Corrupted by Intermodulation

3.3 LNA Topology Choice

3.3.1 Choosing an Amplifier Configuration

Choice of circuit topology is a vital step in any design. Tradeoffs among maximum & minimum performance limits, design specifications, technology restrictions, and implementation practicality all play a role in topology choice. In low noise amplifiers a designer strives to achieve high gain, low noise figure, high linearity all while consuming very little power. The first and most important decision that must be made is the transistor configuration.

The common-emitter amplifier configuration in Figure 3-2, though attractive for its simplicity in design and implementation, is hampered greatly by the miller effect by the base to collector capacitance C_{μ} . Yet another issue with the common emitter configuration is that the circuit can be potentially unstable at high frequencies. This is again due to the presence of C_{μ} acting as feedback network for the amplifier. Since this common-emitter configuration has so many drawbacks, it is not realistic to use this simple configuration to design a high frequency circuit. Therefore it is worthwhile to explore other possibilities.

The next amplifier configuration under consideration is the common-base, illustrated in Figure 3-5, which has the benefit of duplicating input current to the output. Using a simplified small signal analysis, where resistance between base and emitter and collector to emitter is omitted, the transfer function can be shown to be:

$$\frac{V_{out}}{V_{in}} = \frac{g_m Z_L}{1 + sC_{\mu} Z_L} \quad (3.3.1)$$

What equation (3.3.1) shows is the pole of the transfer function is solely decided by load and C_{μ} so the Miller effect is eliminated compared to equation (3.2.2). This configuration also offers improvement in reverse isolation, the inverse of the gain transfer function. This would lead one to conclude that the common-base amplifier performs better in high frequency operation than the common-emitter amplifier. However, according to [15] the common-base is generally unsuitable for use as a low-noise input stage due to its current gain which causes any noise current at its output to be referred directly to the input without reduction. Any serious degradation or hindrance in noise performance is unacceptable, therefore eliminating the common-base amplifier as a viable solution.

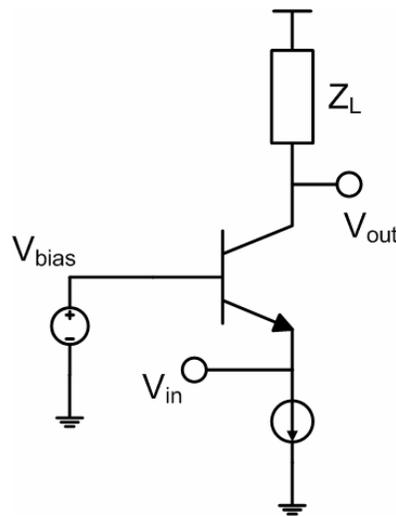


Figure 3-5: Common-base amplifier configuration

The single transistor configurations are fairly simple to analyze. However, they have drawbacks that make them unsuitable for robust high frequency performance. In order to maximize circuit potential, another circuit topology must be identified for a more optimal solution for a low noise amplifier design.

Following the discussion above, it is obvious that in high frequency operation, Miller capacitance needs to be avoided as much as possible. This essentially means the collector and the base of a transistor must not see voltage gain. Another type of amplifier topology that avoids voltage swing on the collector-base junction is the cascode. In a cascode configuration, shown in Figure 3-6, a combination of a common-emitter with a common-base stacked between its collector and the load [16] is employed.

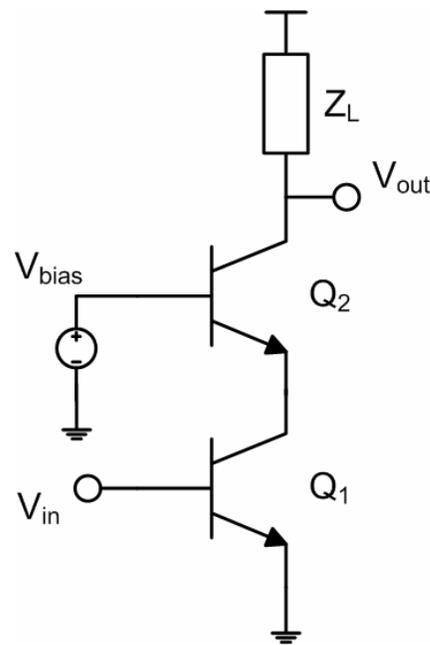


Figure 3-6: Cascode amplifier configuration

The cascode amplifier provides a viable solution to deal with the issues presented in the other amplifier configurations. The most important issue addressed by the cascode is the degradation of the Miller effect compared to the common-emitter. In the previous analysis of the Miller capacitance it was observed that effective input referred capacitance was determined by the load resistance, R_L . By

introducing a cascode the load resistance is replaced with the input resistance of the common-base stage, r_e . Since r_e is much less than the load resistance (typically) the effective input referred capacitance is very close to the miller capacitance, which is typically quite small. Another way of analyzing this is considering that the collector-emitter junction between the input and cascode stages is largely current mode, and therefore does not support the voltage differential that causes the multiplication factor of the miller capacitance [17]. This topology has many benefits over the conventional aforementioned amplifier configurations, including increased gain and improved reverse isolation. In terms of stability, the path from V_{out} to V_{in} is further enhanced by the transistor stack-up. Since the current swing through the cascode is approximately the same as that through the input stage ($g_m v_\pi$ vs. $\alpha g_m v_\pi$), the output load of the amplifier can be much larger than r_o , instead becoming $r_o(1+g_m r_\pi)$. From this a new gain relationship can be written as:

$$\frac{V_{out}}{V_{in}} = -\alpha g_m V_\pi \left(\frac{r_o (1 + g_m r_\pi) Z_L}{r_o (1 + g_m r_\pi) + Z_L} \right) \quad (3.3.2)$$

The disadvantages of the cascode topology are some degradation in linearity due to reduced output swing, larger voltage headroom is often required and it increases the number of noise sources in the circuit. However, the noise analysis of cascode amplifiers conducted in [18] reveals the cascode and common-emitter have similar noise figures. The noise figure of the cascode amplifier can be accurately described by equation (3.3.3):

$$NF = 1 + \frac{r_b}{R_s} + \frac{1}{2g_m R_s} + \frac{g_m R_S}{2\beta} + \frac{g_m R_S}{2} \left(\frac{f}{f_T} \right)^2 + \frac{1}{2g_m^2 R_c R_s} + \frac{R_S}{R_C} \left(\frac{f}{f_T} \right)^2 \quad (3.3.3)$$

Also, recalling from equation (3.2.7) the NF of the common-emitter amplifier:

$$NF = 1 + \frac{r_b}{R_s} + \frac{1}{2g_m R_s} + \frac{g_m R_s^2}{2\beta} \quad (3.3.4)$$

The difference/additional terms in (3.3.3) and (3.3.4) represent the noise contributions introduced by the common-base device. They include the shot noise term due to additional base current, shot noise from the collector, and Gaussian & frequency dependent noise from the collector current and resistance. These additional frequency dependant contributors are relatively small for microwave applications designed at operating frequencies less than 10% of peak f_i .

The bandwidth extension, increased gain, improved isolation, and immunity to the miller effect can obviously be viewed as more beneficial over the aforementioned disadvantages. So the decision to utilize the cascode configuration over the other topologies is justified with confidence.

3.3.2 Device Sizing, Bias Network and Matching Topology

After undergoing a semi-rigorous discussion in the previous section, the cascode amplifier configuration was finally chosen. Noise performance, gain potential, and bandwidth capability were all described. Now the conversation shifts to the implementation of passives and bias network in order to achieve optimal performance in a 50Ω system. As an added benefit to providing good forward gain and high reverse isolation, the cascode allows for the realization of unilateral matching

networks. This essentially means that the input and output matching networks can be designed and optimized nearly independently without affecting each other [19]. So the tradeoffs between achieving a good input match (S_{11}) vs. noise figure, high gain vs. low noise, and high gain vs. high linearity are much easier to reconcile. A superior LNA should be capable of enhancing the signal-to-noise ratio as compared to an unamplified signal while adding very little noise, consuming little power, maintaining linear behavior over a wide input range, and be capable of performing soundly in a harsh environment (extreme temperatures).

Addressing how to comprise the list of performance tradeoffs begins with bias level and device sizing. The bias point (current density) at which maximum f_T (peak current gain) and minimum noise figure NF_{\min} occur at different levels. Since f_T increases with increasing current density (J_C) the gain required by the application should set the lower limit of the J_C . The noise figure requirement and power consumption specifications set the upper limit of the J_C . Within the range in which all sets of requirements are satisfied, the current density should be chosen to maximize linearity (IP3) [14].

Once the current density is chosen, the bias networked can be designed. The specifications require that that the LNA be able to perform soundly in harsh environments (extreme temperatures). Also, the bias network should not consume much power, so employing a simple resistive network is out of the question. Instead the only viable solution is to utilize a bandgap reference bias that exhibits proportional to absolute temperature (PTAT) behavior. The PTAT bias circuit, shown in Figure 3-7, should provide an increase in bias current through the cascode to compensate for the loss in the amplifier's transconductance that occurs at rising temperatures. Ideally, the LNA should not exhibit a change in gain with temperature. However, a more realistic requirement is to maintain a relatively constant gain, with less than .01dB/°C roll off

from 50 - 150 °C. The overall temperature coefficient (TC) of the bias circuit must obviously be a somewhat large positive quantity. To help insure the PTAT behavior, an n-type implant resistor was chosen for $R3$ with a TC of 1940 ppm/°C. Its resistance increases rapidly with temperature, which in turn leads to an increase in the cascode bias current [20]. Transistor $Q3$ is sized as a small fraction of the common-emitter transistor in the cascode to minimize power consumption.

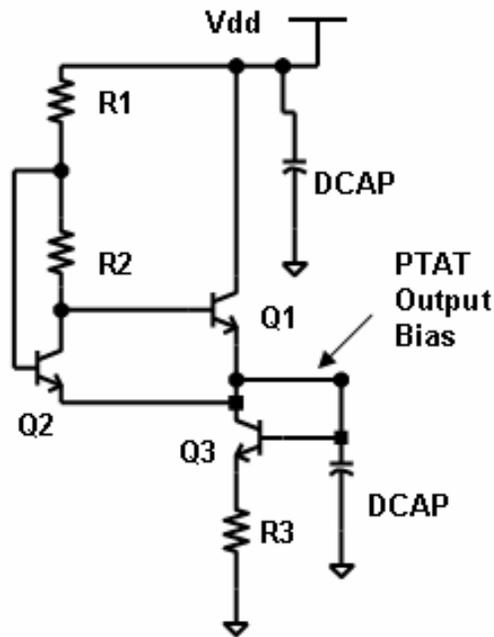


Figure 3-7: PTAT Bias Network

Device sizing is reduced to choice in emitter length because minimum emitter width yields the lowest possible NF_{min} and highest possible f_T . The design problem now becomes how to size the emitter length and choose a matching network needed to provide a simultaneous noise and power match while remaining within power consumption specs. As simple as the goal seems it is actually bit challenging because optimal noise match typically will not occur at an impedance of 50Ω , it normally is at

a much higher impedance, and of course minimum power reflection or optimal performance can only be achieved when the load and source impedance are complex conjugates. Conveniently, an S-parameter and dc simulation using ADS or Cadence with the setup shown in Figure 3-8 can be used to identify and optimize NF_{min} , J_C , f_T , power consumption, S-parameters and the input & output impedance of the cascode. In all actuality, the configuration in Figure 3-8 is the most essential to the design because all the insightful information that it can provide.

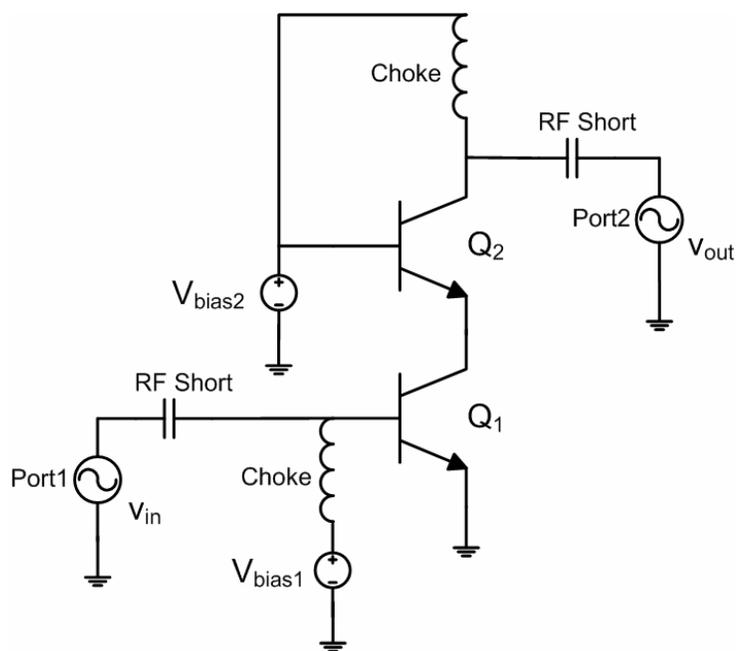


Figure 3-8: Simulation schematic used to gather vital performance information

Using the simulation setup above, the input impedance to the cascode is mainly capacitive at high frequencies. The challenge at hand is to produce a resistive component at the input impedance without increasing the noise figure. A popular

method employed is to use emitter inductive degeneration, illustrated in Figure 3-9.

The new input impedance of the amplifier becomes:

$$Z_{in} \approx \omega_T L_e + j\omega L_e + \frac{1}{j\omega C_\pi} \quad (3.3.5)$$

To obtain the desired 50Ω input resistance, the emitter inductor can be sized using:

$$L_e \approx \frac{50\Omega}{2\pi f_T} \quad (3.3.6)$$

The input match for optimal noise and power transfer performance can now be obtained using a series inductor at the base sized to tune the capacitive input [14].

There are, of course, other tradeoffs associated with inductive degeneration. Foremost, the degeneration inductor L_e acts to lower the g_m of the input stage, limiting the gain and thereby inhibiting the LNAs ability to isolate successive noise stages. However, lowering g_m helps to greatly improve linearity due to the reduced input signal swing. Another drawback of inductive degeneration is the size of the inductor required, which can increase substantially the physical dimensions of the LNA. This however, can be offset by the reduction in size required for the series base inductor.

To assist in assuring that a match, which optimizes performance, can be achieved a discrete capacitor, C_{be} , can be inserted between the base and emitter to assist C_π , which is fixed from device sizing, and L_e at resonance. This is drawn schematically and in the small signal model in Figure 3-9. This additional capacitor provides a bypass to low frequency variations across the base-emitter junction which minimizes 3rd order products. Also, it aids in lowering actual noise figure by

reducing the size requirement of the inductors, which can have large parasitic resistance, and by filtering the base resistance at resonance with C_{π} .

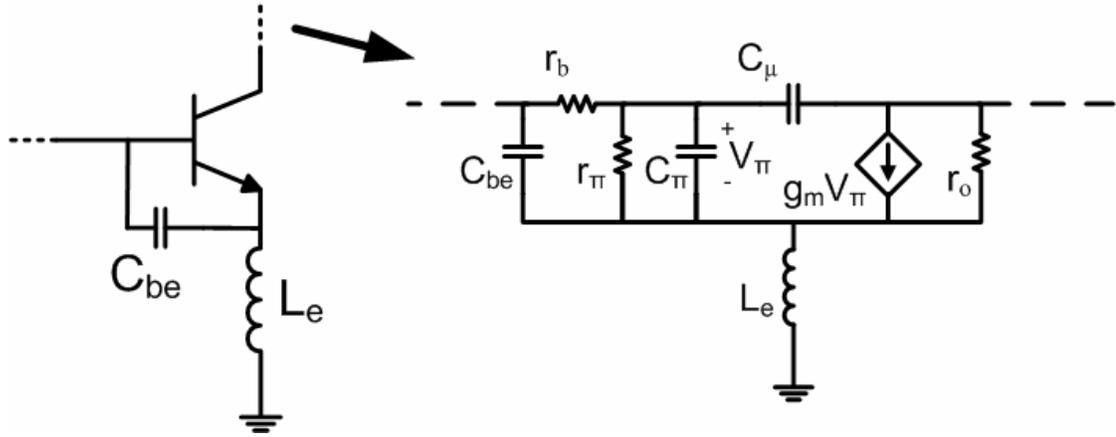


Figure 3-9: Simultaneous Noise and Impedance Matching

In an ideal scenario the series base inductor (L_b), degeneration inductor (L_e) and bypass capacitor (C_{be}) would be purely reactive with infinite Q and would not introduce noise. However, this is not the case so of course the matching network alters the noise figure. When the cascode amplifier is matched exactly to 50Ω following the discussion above, its NF can be accurately described by [21]:

$$NF = 1 + \frac{r_b}{R_s} + \frac{f_T}{f_o Q_L g_m R_s} + \frac{1}{2\beta} \cdot \left(g_m R_s + \frac{1}{g_m R_s} + \frac{f_o}{f_T} \right)^2 + \frac{g_m (R_s + 2r_b)}{2} \left(\frac{f_o}{f_T} \right)^2,$$

$$Q_L \cong \frac{2\pi f_o (L_e + L_b)}{R_s} = \frac{1}{2\pi f_o R_s (C_{\pi} \parallel C_{be})} \quad (3.3.7)$$

The output match is much less complicated and employs a typical LC network to create the desired match 50Ω . Active and passive device sizing comes into play in order to match the impedance transformation simpler by minimizing the number of elements required. Since the biasing of the common-emitter portion of the cascode amplifier sets the current consumption, a designer has the luxury of sizing the common-base as needed to provide the match.

The overall circuit topology for narrow band LNA in the micro frequency range is displayed in Figure 3-10. In addition to the major elements discussed in detail above, there are some additional components necessary for successful design implementation. The large isolation resistor ($3K$ to $6K \Omega$ s) is required to protect the RF section from the bias network. Also, the overall topology employs large decoupling capacitors on every DC node/bias node in order to stabilize the circuit by shunting any fluctuations to ground.

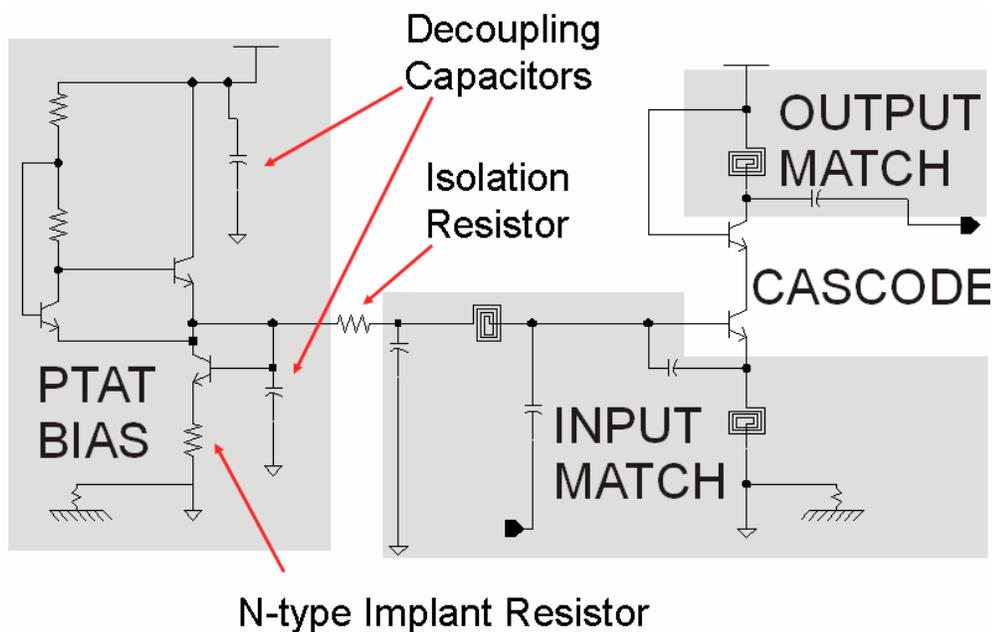


Figure 3-10: Overall Narrowband Microwave LNA Circuit Topology

3.4 Noise Reduction Technique

In radio frequency circuit design, the substrate has been known as noisy, lossy, and a source for undesired crosstalk/coupling. Ironically, though there are a variety of substrates used in many different types of fabrication processes, the substrate is still generally blamed for common design issues. The most common substrate types are categorized as follows: Good Conductors (*Very Low Resistance*), Good Insulators (*Very High Resistance*), and Poor Conductors (*Moderate Resistance*). Each substrate type has its own distinct characteristics, which govern the different ways noise and coupling should be handled. This work addresses the poor conductor substrate type, which due to its finite resistance provides an opportunity for noise and interference signals to propagate between adjacent circuits in a layout. The strategic placement of substrate contacts, blocking of bipolar implants, and deep trench isolation lattice near high frequency active circuit elements; in conjunction with an uniformly distributed AC/DC ground plane, help to provide means of reducing noise injection. Essentially, the goal is to provide a highly conductive path to ground the substrate (CPGS) for the entire circuit, so that noise, coupling/crosstalk can be shunted to a lower resistance ground path. To demonstrate the effectiveness of CPGS a family of low-noise amplifiers (LNA) is compared in this portion of the dissertation [6].

Recalling from Figures 2-3 and 2-4, the issue and the desired treatment of the poor conductor substrate type is once again illustrated in Figures 3-11 and 3-12 [4]. In the p- silicon bulk, the lossy substrate introduces finite resistance to ground, and unwanted paths between various components, which attenuates and corrupts critical signals. This can ruin the fundamental performance goal of an LNA. Noise, cross-talk and coupling of signals between adjacent devices are a serious issue in analog and RF circuits and must be addressed.

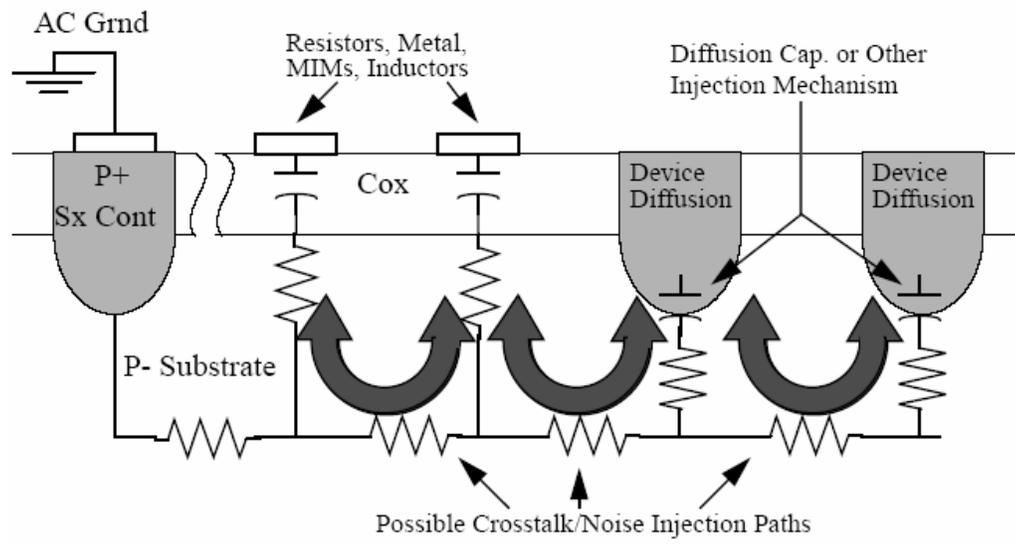


Figure 3-11: Lossy Substrate Noise and Coupling Paths

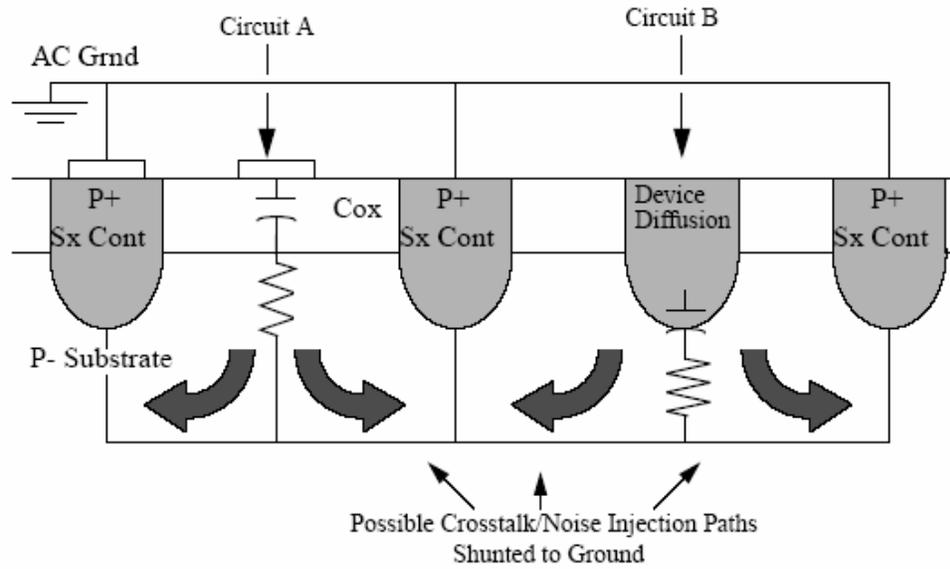


Figure 3-12: Low Resistance Path to Ground

The substrate used for the all of the designs in this dissertation is considered a poor conductor because of its P-type bulk with a resistivity of 11-20 Ω -cm [5]. Due to this semi-resistive nature, crosstalk and coupling between high frequency components can be significant, as shown in Figure 3-11. Additionally, the P- substrate can be viewed as a thermal noise source. In order to reduce potential noise injection and coupling through the bulk, a uniform conductive (AC and DC) ground path from the top metal down to the substrate (utilizing many substrate contacts and vias) is implemented throughout the entire circuit layout. This provides a means of controlling the bulk potential. Placing grounded substrate contacts near active circuit components minimizes the resistance path to AC ground, which reduces noise injection. This most wanted result is illustrated in Figure 3-12. Figure 3-13 illustrates CPGS along with the use of bipolar block and deep trench lattice to isolate the high frequency element by removing the PWELL around it. With these structures in place, the most plausible crosstalk/coupling and noise injection paths are shunted to ground [6].

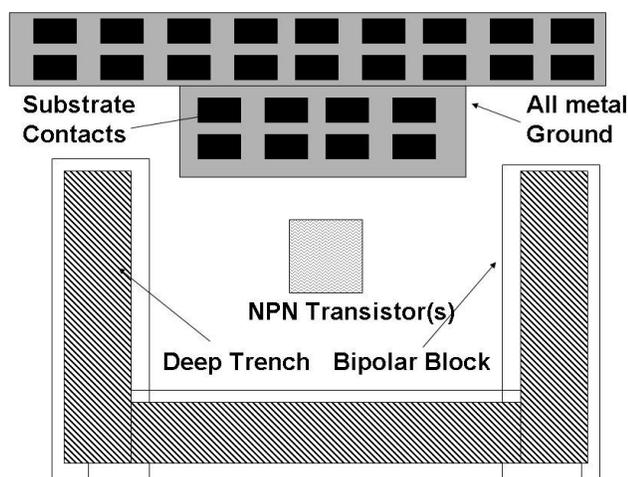


Figure 3-13: Conductive Path to Ground the Substrate Near RF Circuit Elements

3.5 Microwave Low Noise Amplifier Design

The fundamental goal of a low-noise amplifier is to provide gain to a signal, while adding very little noise. Since the LNA is the first gain stage in a receiver path, its noise figure dominates that of the overall receiver. So any improvement in its gain to noise ratio would be valuable. In order to demonstrate the effectiveness of the CPGS technique a host of narrow band microwave LNAs at 2.14, 2.45 and 5.25 GHz were designed and fabricated in IBM's 5HP SiGe BiCMOS.

The 5HP process features three aluminum metal layers, heterojunction bipolar transistors (HBTs) with a peak f_T of 47 GHz, and a wide variety of passive components such as metal-insulator-metal (MIM) capacitors and spiral inductors. This technology was utilized in order to take advantage of the lower cost associated with using a relatively mature process while still benefiting from the high performance characteristics of SiGe HBTs. These LNAs are fully integrated, using on chip passives and the topology described in earlier, which traditionally makes it difficult to achieve lower noise figures. However, a monolithic design is significantly more cost effective than a design with external components.

To ensure a fair experimental comparison, the only difference between the LNAs is the use of CPGS technique, as in Figure 3-14, near the active circuit elements. In the case without CPGS, the grounded substrate contacts are not placed near the active elements. Each LNA in this experiment was designed using the exact same circuit topology, shown in Figure 3-10, 2.5 volt supply, and component values. A die photo of the 2.45 GHz LNA device under test is shown in Figure 3-15.

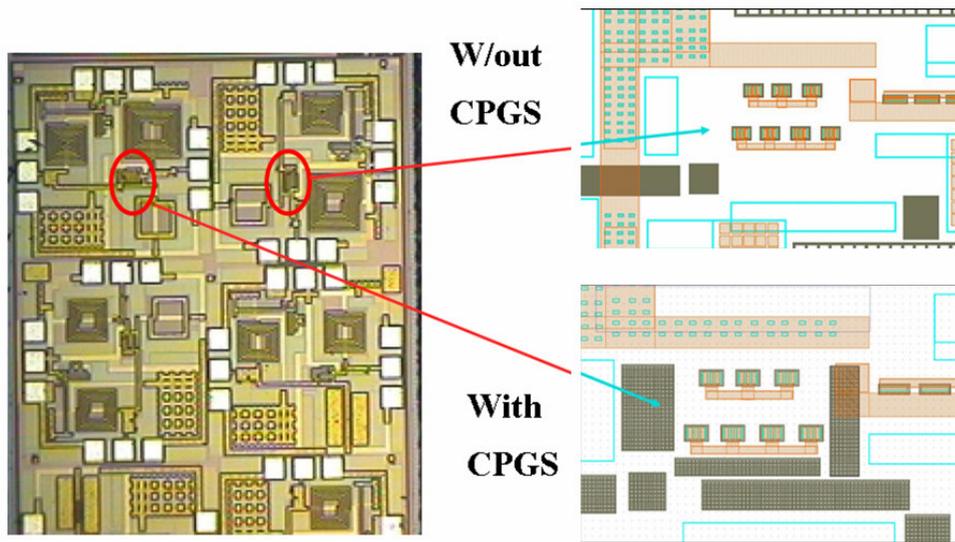


Figure 3-14: Conductive Path to Ground the substrate (CPGS) Experiment

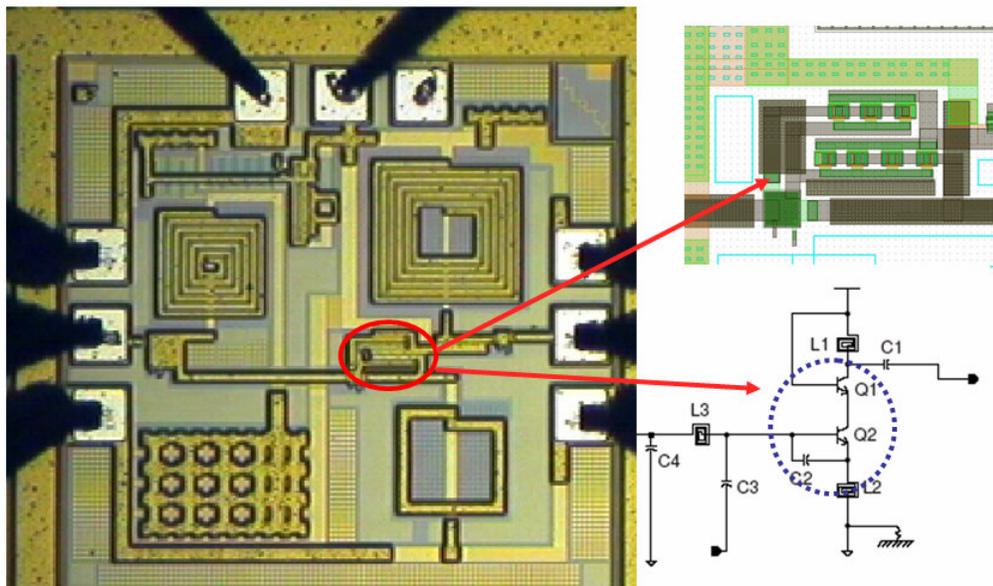


Figure 3-15: 2.45 GHz LNA Device Under Test

3.6 Experimental Results

The fabricated LNAs were characterized using the Agilent 84000 RFIC Tester. The 84000 has the capability to fully characterize amplifiers up to 18 GHz. S-parameters, NF, 1-dB compression ($P_{1\text{dB}}$), IP3, and DC power consumption. The measurements summarized in Table 3-1 confirm that utilizing the CPGS technique near the high frequency circuit components does indeed decrease (improve) the overall noise figure as well as reduce the DC power consumption of the LNA in each case. By using CPGS the resistance of the ground path to the substrate is reduced significantly. At 2.14 GHz, the CPGS technique enhances the LNA performance in every category including a reduction in noise figure and an increase in gain by 0.82 dB and 2.5 dB respectively. At 5.25 GHz, the noise is reduced by 1.88 dB while the gain has risen by 5.3 dB. Also in the lower frequency designs, the linearity (IIP3) is improved by an average of 2 dBm because of the improved power handling capability.

The high temperature performances of the CPGS LNAs are shown in Table 3-2. The PTAT bias circuit is verified to work effectively as the respective gain of these LNAs remain relatively flat. The linearity is also quite impressive; even at 75°C the worst case IIP3 is +5 dBm. A comparison of the S-Parameters for the 5.25 GHz LNA is shown in Figure 3-16. This work is benchmarked against several other published low-noise amplifiers in Table 3-3. The performance metrics highlighted in Table 3-3 represent the state-of-the-art, as of November, 2005. Also, included in the table is a figure of merit (FOM) defined as the ratio of peak Gain to the product of NF and DC power consumption:

$$FOM = \frac{G}{NF \cdot P_{DC}} \quad (3.5.1)$$

Table 3-1: Performance Comparison of LNAs with and without CPGS

LNA Metric	With CPGS			Without CPGS		
Freq (GHz)	2.14	2.45	5.25	2.14	2.45	5.25
NF (dB)	1.37	1.68	2.25	2.19	2.02	4.13
Gain (dB)	18.8	18.2	17.4	16.3	18.7	12.1
IIP3 (dBm)	+11.4	+7.8	+7.0	+9.3	+6.0	+8.0
Current mA	5.56	5.56	5.19	5.74	6.00	5.65

Table 3-2: High Temperature Performance with CPGS

LNA Metric	55 Degrees			75 Degrees		
Freq (GHz)	2.14	2.45	5.25	2.14	2.45	5.25
NF (dB)	1.86	2.19	2.56	1.98	2.74	2.83
Gain (dB)	17.9	17.6	16.5	17.9	17.3	15.9
IIP3 (dBm)	+9.5	+6.7	+6.2	+8.6	+6.0	+5.6
Current mA	6.28	6.10	5.44	6.60	6.50	5.73

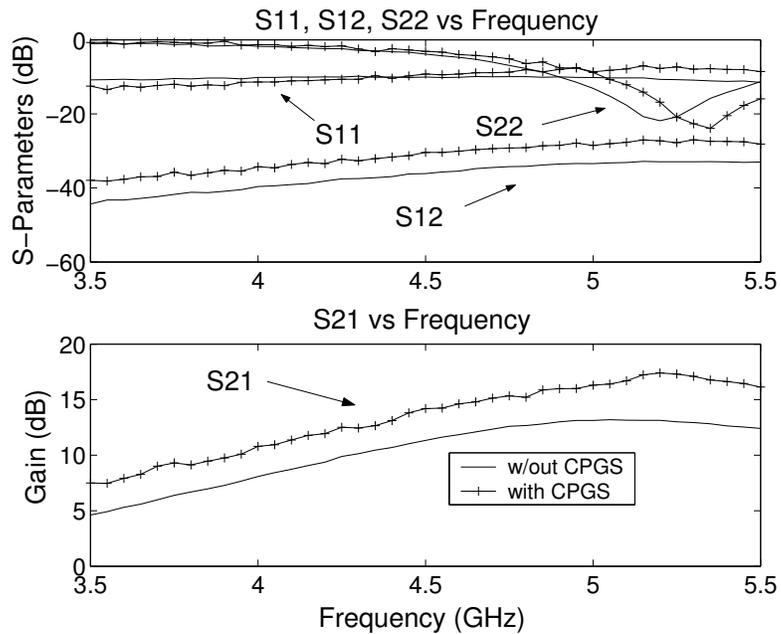


Figure 3-16: Comparison of measured S-Parameter data of the 5.25 GHz LNAs

Table 3-3: Comparison of Narrowband Microwave LNAs

LNA Performance at Room Temperature	This Work	Infineon Tech. 2003 [22]	Maxim 2003 [23]
Frequency (GHz)	2.45	2.4	2.45
Gain (dB)	18.2	15.5	17
Noise Figure (dB)	1.68	0.96	2.0
Output Match (dB)	-25.3	-13.3	-10
Input Match (dB)	-10.7	-11.5	-15
Rev. Isolation (dB)	-32.6	-21.7	-30
IIP3 (dBm)	+7.8	+11.6	-3
Input Comp (dBm)	-21	-11.6	-13
DC Power (mW)	13.9	20.1	29.1
Monolithic	Yes	No	Yes
Technology	47 GHz f_T 0.5 SiGe	70 GHz f_T SiGe	35 GHz f_T SiGe
FOM (mW^{-1})	0.78	0.80	0.29
PTAT Bias	Yes	No	Yes

LNA Performance at Room Temperature	This Work	IBM 2004 [24]	Swiss Federal Institute 2003 [25]	This Work	STMicroelectronics 2003 [26]	Info & Comm. Univ. Korea 2005 [27]
Frequency (GHz)	2.14	2	2.2	5.25	5.5	5.25
Gain (dB)	18.8	16.5	12	17.4	18.7	20
Noise Figure (dB)	1.37	1.1	2.5	2.25	3.9	1.5
Output Match (dB)	-28.5	-9	-10	-21.0	-18	-20
Input Match (dB)	-12.0	-7	-20	-8.0	-12	-18
Rev. Isolation (dB)	-31.7	-	-	-27.8	-	-
IIP3 (dBm)	+11.4	+4.3	+5.4	+7.0	-3.5	-5
Input Comp (dBm)	-	-	-12	-19	-13.9	-16
DC Power (mW)	13.9	18	9.75	13	26.4	12
Monolithic	Yes	Yes	No	Yes	Yes	Yes
Technology	47 GHz f_T 0.5 SiGe	120GHz f_T 0.18 SiGe	0.13 CMOS	47 GHz f_T 0.5 SiGe	0.35 SiGe	0.18 CMOS
FOM (mW^{-1})	0.99	0.83	0.49	0.60	0.18	1.1
PTAT Bias	Yes	Yes	No	Yes	No	No

3.7 Summary

This chapter described the fundamentals of low noise amplifiers including the discussion of essential metrics such as NF and IP3. The methodology for designing monolithic narrowband microwave LNAs was presented which covered tradeoffs, topology choice and noise implications with equations. This chapter also presented a passive noise reduction design technique that helps to ensure optimal design performance.

An experiment was conducted and presented on the design and characterization of a family of fully integrated LNAs designed with and without CPGS (a conductive path to ground a P- substrate) near the active device region has been presented. The LNAs were developed in IBM's 5HP 0.5 μ m, 47 GHz f_T , SiGe technology. The measured results demonstrate a decrease in noise figure by 1.88 dB, 0.34 dB, and 0.82 dB at 5.25 GHz, 2.45 GHz, and 2.14 GHz respectively. By using this passive noise suppression technique, the resistance of the ground path to a P-substrate is reduced significantly, resulting in much improved circuit performance in LNAs. This technique can easily be applied to more advanced (higher f_T devices) fabrication processes with similar substrate types to drastically improve RF circuit performance [6].

Chapter 4: mm-Wave Low Noise Amplifier Designs

4.1 Motivation

Moving to higher frequencies with larger bandwidth allocations can conquer many of the limitations of contemporary systems, albeit while introducing new challenges. The millimeter wave (mm-Wave) frequency range can accommodate new potential applications such as automotive radar, medical imaging, security, and so much more. Operation at such high frequency minimizes the size of the antenna which allows for on-chip integration because the signal wavelength literally becomes on the order of one to tens of millimeters. The ultimate goal is envisioned to be fully integrated systems (Antennas, RF, Analog and Digital components on one die using a single silicon process).

Advances in the speed of the silicon transistor and increased complexity of the integrated circuit metallization stack; along with sophisticated Electro-Magnetic (EM) simulation software has fortified the capability to realistically pursue this goal. A comprehensive design approach for implementing micro and millimeter wave wireless transceiver front-end circuits is proposed. The design methodology exploits the aforementioned advances to ensure successful implementation of radio frequency circuits in both standard silicon CMOS and silicon germanium (SiGe) BiCMOS technologies.

In this chapter the LNA is the focus because of its vital role in the receiver and the techniques developed can be applied to a myriad of other circuits where the operating frequency is high, noise must be curtailed and the dimensions of passive structures are comparable to the signal wavelength. LNA pursuits have lead to the enhancement of the passive noise reduction layout technique developed in the

previous chapter. Also, a new concept in SiGe device sizing which essentially exploits parasitic capacitances in order to tune unilateral and current gain peaking for operation frequencies upwards of 100 GHz is discussed.

Many of the techniques employed are intended to combat the limitations of the silicon substrate; even beyond the frequency limitations of the devices, and towards overcoming and in some cases exploiting the parasitic effects of interconnect wiring at increased frequencies. Simulation and Measurement results from the circuits are presented and an integrated simulation environment is proposed to simplify the design flow. A number of successful hardware demonstrations confirm the validity of the proposed design methodology. In the LNA arena, a new figure-of-merit (FOM) equation is proposed.

4.2 A Novel Unilateral and Current Gain Peaking Technique¹

In millimeter wave circuit design, paying close attention to detail is at the heart of the formula for success. A designer should be conscious of the benefits and consequences of each choice and decision made during the design process and the associated impact on performance; hopefully minimizing the ones that hurt, and optimizing ones that help. Recalling Figure 2-8, the comprehensive design flow proposed in this dissertation promotes one to pay very close attention to detail and provides a process in which a designer will make well informed and/or even innovative design choices. The design flow is once again illustrated in Figure 4-1.

Following the discussion of the methodology utilized in choosing an LNA topology in the previous chapter; the cascode configuration is chosen as the basis for

¹ Parts of this section had been submitted to [34][35]; notification of acceptance will be announced by early February 2008.

the amplifiers designed in this chapter. A conscious decision was made to target maximum RF output power while consuming minimal DC power.

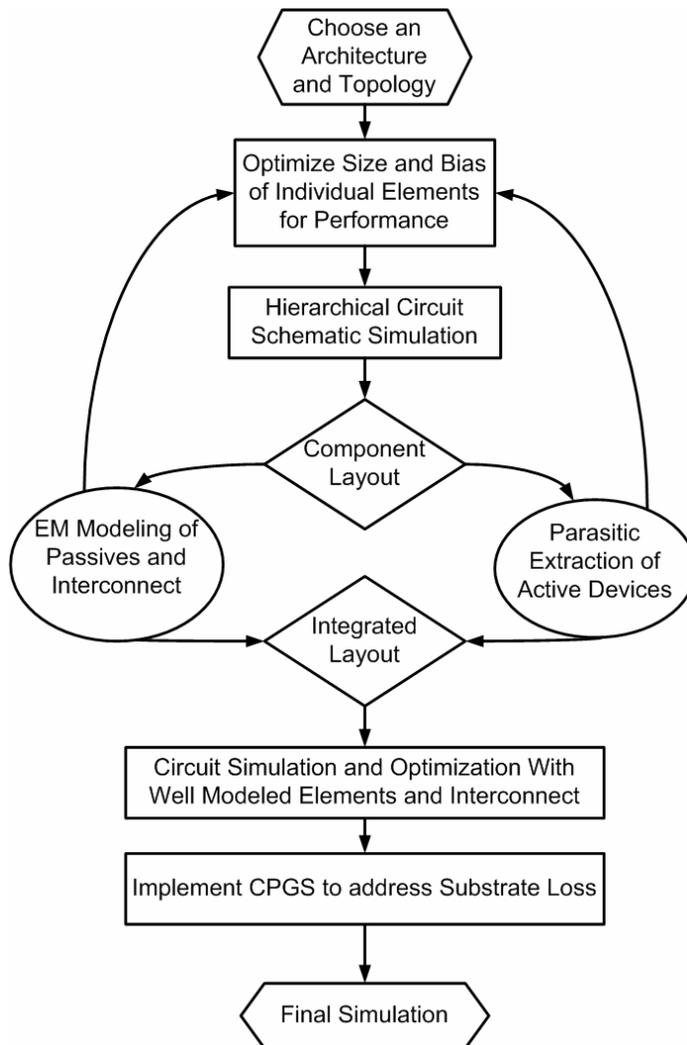


Figure 4-1: Proposed Silicon RF Design Flow

In this pursuit of optimizing gain performance, different definitions and types of gain were examined closely in simulation up to a few hundred GHz, which led to the discovery of parasitic gain peaking. During the procedure of choosing transistor sizes & bias points, component layout, and parasitic extraction; the optimization process considered & examined short circuit current gain (h_{21}), maximum available gain (MAG), transducer gain (G_T), maximum stable gain (MSG), and Mason's unilateral gain (MUG). After a few iterations, h_{21} , MAG and MUG peaking, and the frequency shifting of this peaking was observed for un-matched cascode amplifiers with the same transistor device values but, different component layout (different parasitics). The layouts are illustrated in Figure 4-2.

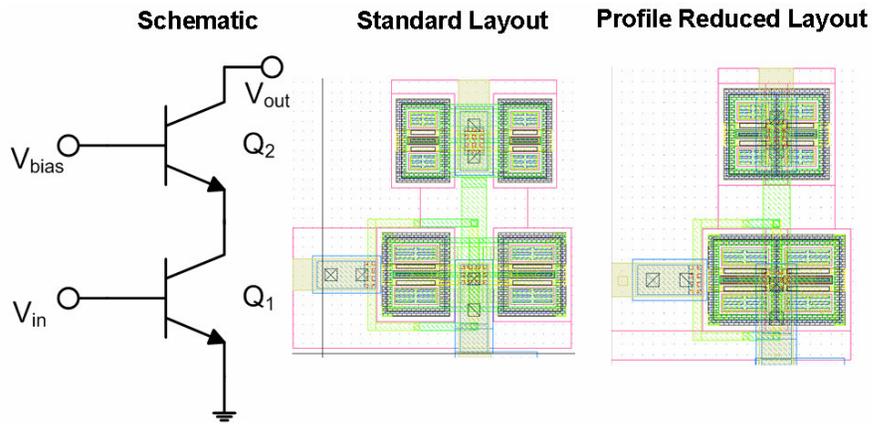


Figure 4-2: Standard Layout and Profile Reduced Layout of Cascode Transistors

In common practice many RF circuit designers only observe & optimize G_T and h_{21} , who's extrapolated magnitude $|h_{21}|^2$ at unity yields the transition frequency f_T . Observing the other dynamic characteristics beyond the target operating frequency is usually regarded as impractical because current instrumentation limitations place an upper frequency bound of 110 GHz for reliable measurements. However, a close examination of the maximum available gain (MAG or G_{max}) of the cascode transistors

revealed a very interesting behavior. The transfer function (frequency response) appears to observe a feed-forward pole(s) introduced by the parasitic capacitance obtained from layout. This additional capacitance reduces the f_T and f_{max} as one would normally expect, however, the frequency at which the anticipated loss in gain occurs much farther out in frequency than is predicted by schematic simulation. This phenomenon is shown in Figure 4-3.

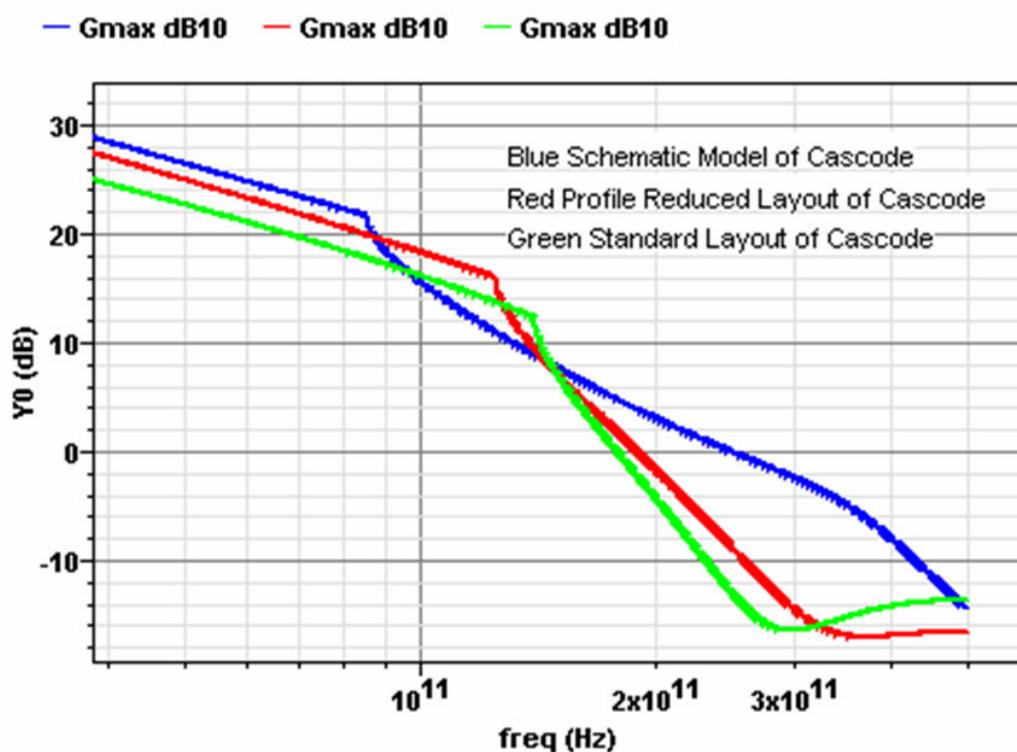


Figure 4-3: Feed-Forward Pole Shifting of the Maximum Available Gain (G_{max}) due to Parasitic Capacitance from Layout

Examining the behavior of Mason's unilateral gain (G_{mux} or MUG) reveals an even more profound outcome. Let us first, however, gain some appreciation and insight of mason's unilateral gain. As defined both in [28] and [29], the MUG is the

maximum power gain that can be obtained from a two-port network after it has been made unilateral. A device embedded in a network such that it has no reverse transmission of signals is defined to be unilateral. MUG is an intrinsic property of devices and is invariant with respect to linear lossless four-port embeddings, thereby making it an extremely useful figure of merit [28].

Observing the G_{mux} for the cascode options of Figure 4-2, Figure 4-4 reveals different frequency points at which MUG predicts a tremendous amount of gain. This is quite interesting in that the transistor sizes remain constant the different layout configurations, introduce different amounts of parasitic capacitance. This is consistent with the theory of invariant intrinsic network behavior in [28].

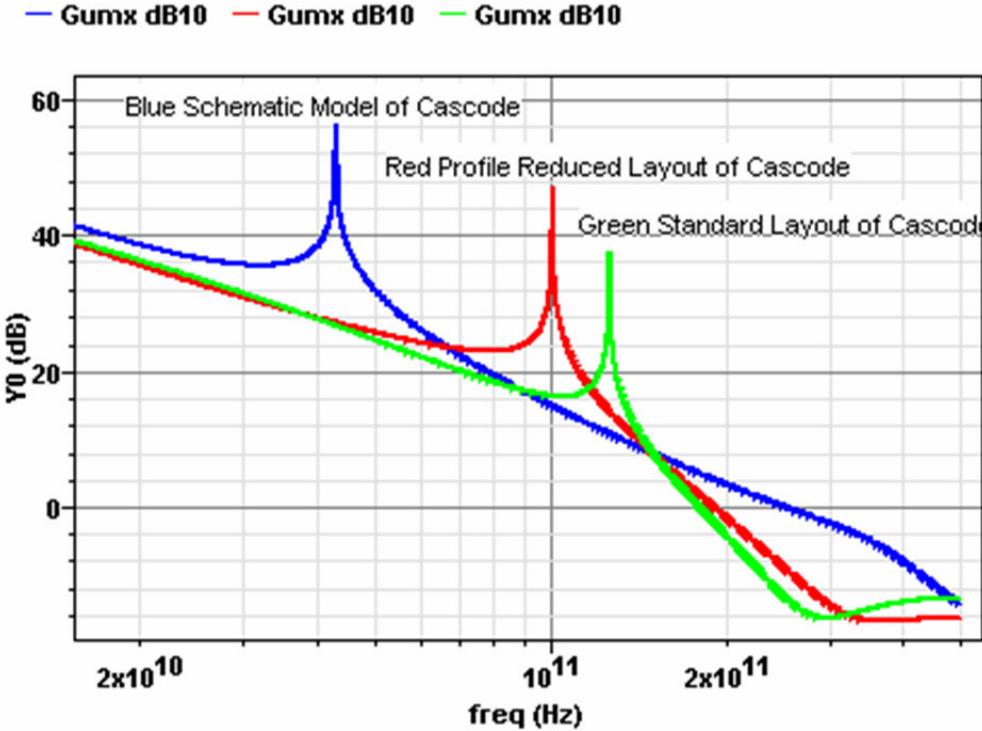


Figure 4-4: Feed-Forward Pole Shifting of the Unilateral Gain Peaking (G_{mux}) due to Parasitic Capacitance from Layout

The peak gain observed can be manipulated for maximum device performance with no extra DC power expense and no penalty in noise figure. The parasitic capacitances added to the transistors causes the device's self resonance and transfer function to shift. Figure 4-5 illustrates how the simple small signal model of a common emitter is modified due to layout parasitics.

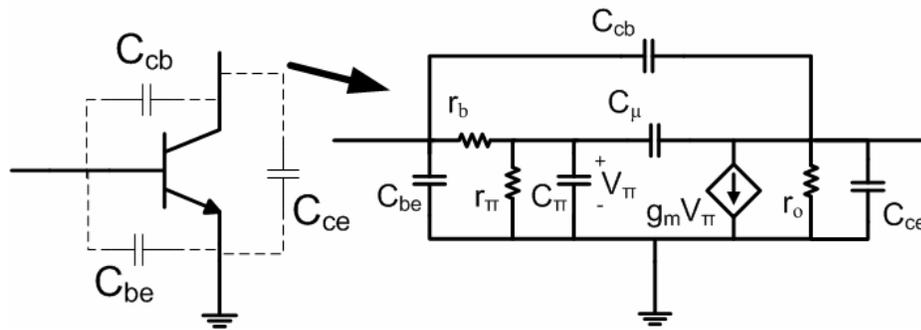


Figure 4-5: Parasitic Capacitances Introduced by Layout

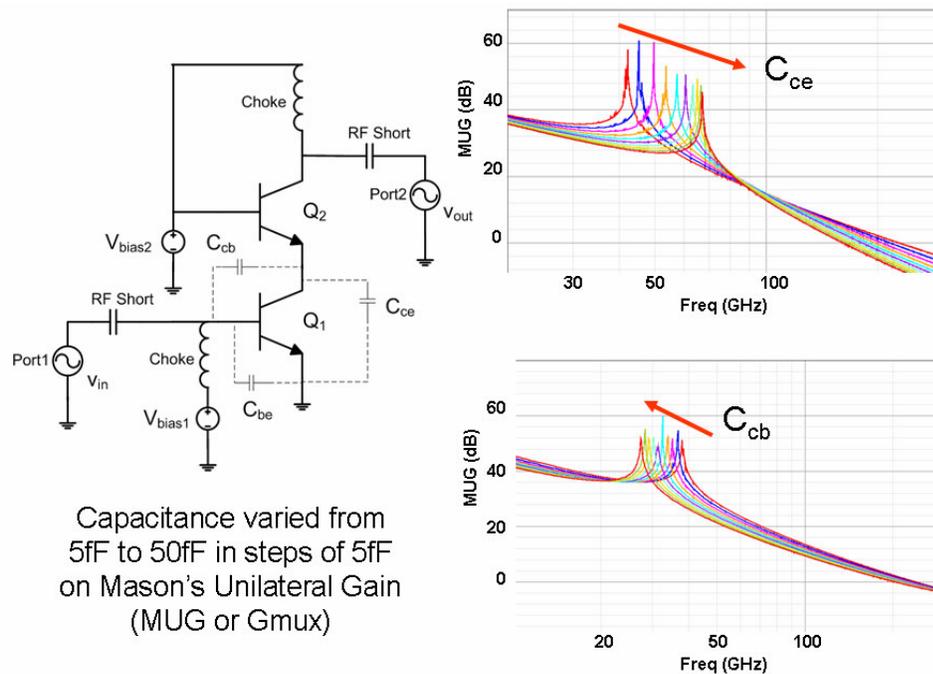


Figure 4-6: Tuning Peak of *MUG* with Parasitic Capacitance

From Figure 4-6 we see that the parasitic capacitance introduced from the layout on the transistor can be sized (tuned) to yield peak performance at the design frequency of interest with some careful layout techniques. The frequency at which the peak of G_{mux} occurs is directly proportional to the size of C_{ce} . The parasitic capacitor C_{ce} (the additional capacitance from the collector to the emitter ground) has a feed forward effect on the transfer function. On the other hand, the parasitic capacitor C_{cb} (the additional capacitance from the collector to the base) acts very much like the miller capacitance C_{μ} in that the transfer function is dominated by the base to collector capacitance such that circuit power gain and bandwidth is significantly affected by it. The frequency at which the peak of G_{mux} occurs is inversely proportional to the size of C_{cb} . In order to minimize the size of this additional miller capacitance the Profile Reduction technique is employed. Essentially what Profile Reduction means is to minimize the physical dimension (profile) of a transistor device as in Figure 4-2. It is employed in Silicon Germanium processes by combining the sub-collector and deep-trench lattice boundary of any parallel transistors. This is a concept adapted from Silicon CMOS devices which place parallel transistors in the same well and multiple devices are represented by fingers that share drain and source layers between them.

In Figure 4-7 the measured current gain (h_{21}) of an LNA designed employing the Unilateral Gain Peaking, and Profile Reduction techniques is shown along side the G_{mux} of the schematic and extracted versions of the cascode transistor devices used in the design. The measured current gain is clearly much larger than predicted level of the schematic version of the cascode. This verifies that the Unilateral Gain Peaking technique is not just a theoretical or simulation artifact!

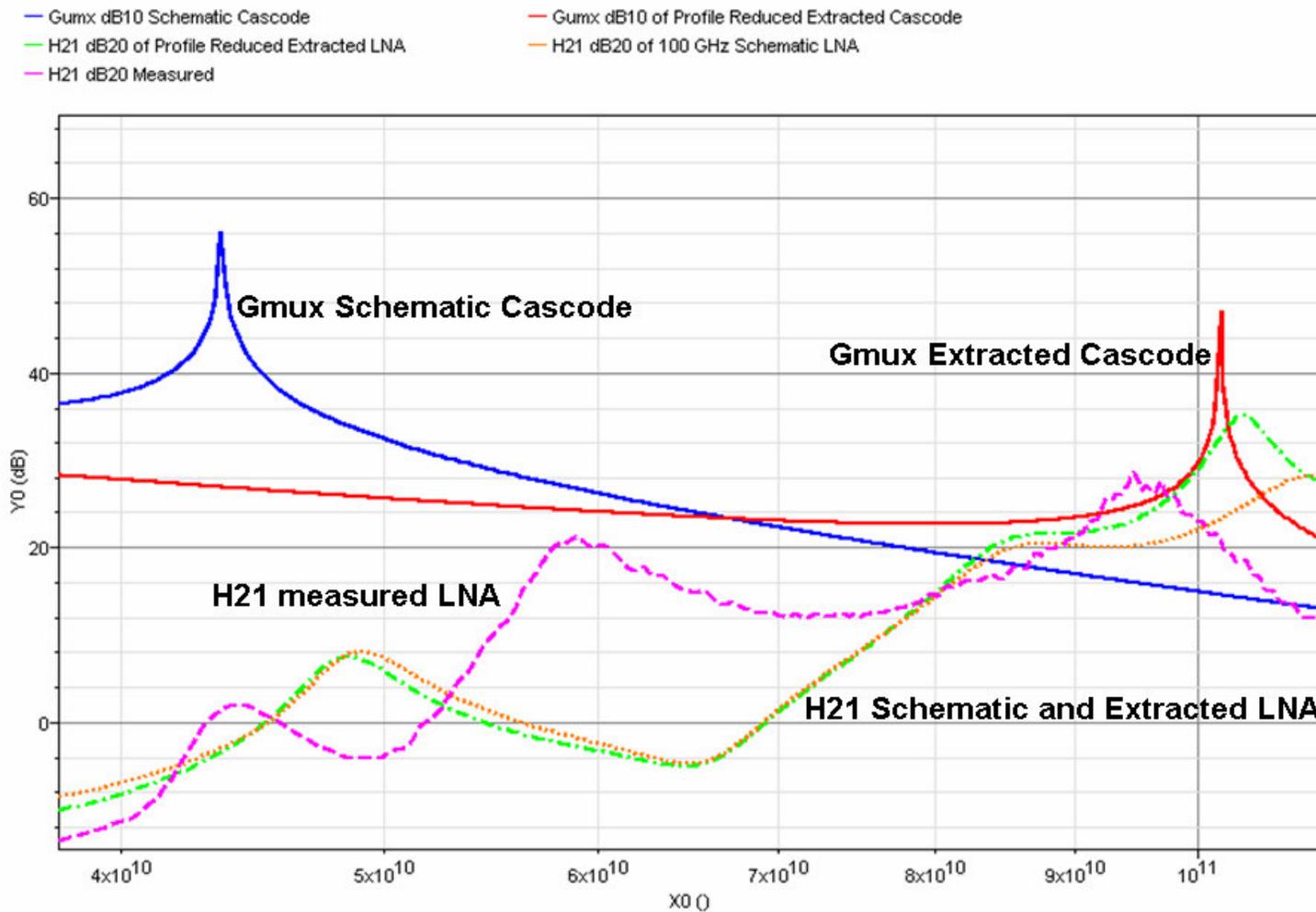


Figure 4-7: Measured LNA Current Gain alongside Unilateral Cascade Gain

4.3 Enhanced Hybrid Transmission Line

This work makes enhancements on the hybrid transmission line model provided with the IBM 8HP design kit. This upgrade of the transmission line (t-line) structure plays a major role in the implementation of the CPGS technique at 60GHz since the bulk-tied ground plane is part of its framework. The on-chip T-line structure used for impedance matching and as an RF-choke is shown in Figure 4-8. Verified using Ansoft HFSS, the characteristic impedance is 60Ω with a quality factor of ~ 24 and loss factor $\alpha \sim 0.4\text{dB/mm}$ at 60 GHz. It is similar to the model described in [9], however, the difference is the ground plane in this form is used to control the bulk potential. The P- substrate can be viewed as a thermal noise source. In order to reduce potential noise injection and coupling through the bulk, a uniform conductive (AC and DC) ground path from the top metal down to the substrate (utilizing many substrate contacts and vias) is implemented throughout the entire circuit layout. This provides a means of controlling the bulk potential. Placing grounded substrate contacts near active circuit components minimizes the resistance path to AC ground, which reduces noise injection [8].

As if the lossy substrate itself wasn't constraining enough, modern deep submicron silicon processes have very strict local and global density design rules that require the presence of each available layer throughout a fabricated circuit. This seriously restricts the Q, size, and types of passive structures that can be effectively used. Some processes are so strict that a simple microstrip line cannot be fabricated without rule waivers or risk of highly inaccurate modeling. Given all these limitations, a combination of microstrip and coplanar transmission line becomes the ideal choice for on-chip transmission line for MM Wave IC design and is illustrated in Figure 4-8. This is because a clever designer can take advantage of the inherent structure of the T-

line, which has a ground plane along its sides and below it, by using multi-layered structures to distribute the conductive path to ground and more easily satisfy the demanding process density and design rule requirements.

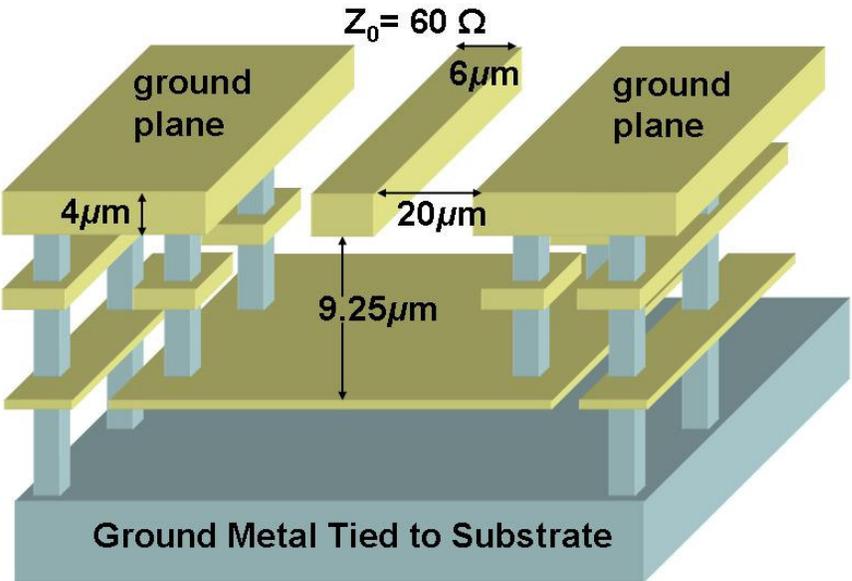


Figure 4-8: Enhanced Hybrid Transmission Line (not to scale)

Not shown in Figure 4-8 is the patterned cutouts of the ground plane below the signal line. These cutouts force the return current of the wave signal through the coplanar ground plane which is physically farther away; this translates to a higher inductance for the transmission line. The forward transmission S-parameter response (both magnitude and phase) for a 100-micron section of the Hybrid Transmission Line is displayed in Figure 4-9.

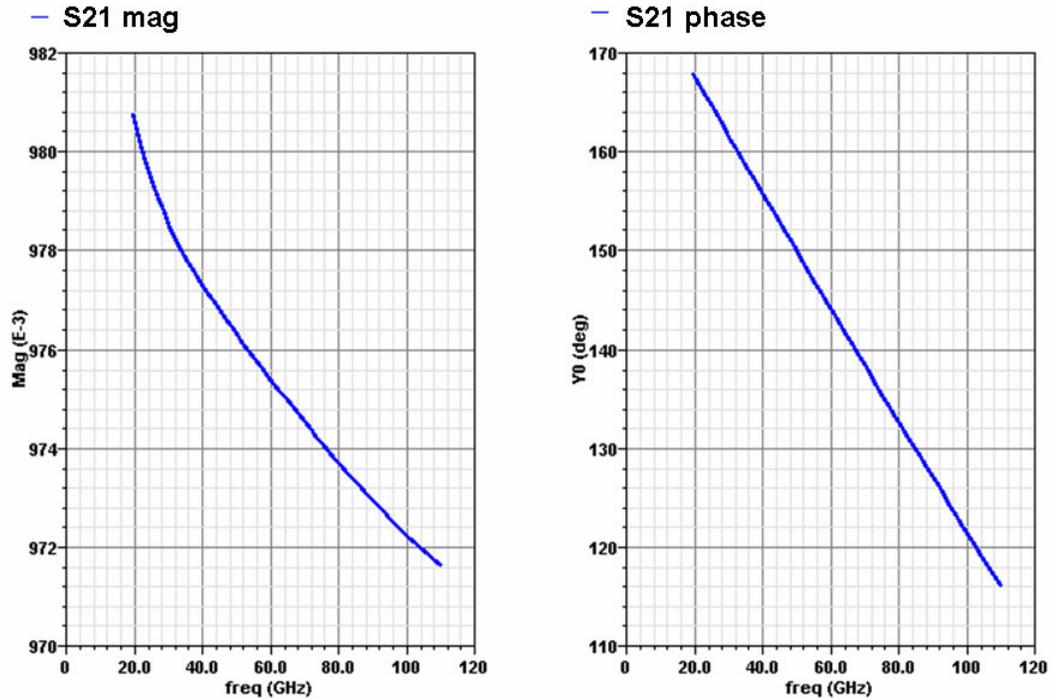


Figure 4-9: 100-micron Segment Hybrid Coplanar T-line S-parameter Response

4.4 mm-Wave Amplifier Measurement Procedures

Measuring devices in the mm-Wave is challenging on multiple levels. From a practical stand point it is quite expensive because the required tools and equipment has to be custom made and orders can take months to be manufactured. Another challenge is that the measurement procedures for millimeter wave devices under test must also be designed with as much detail as the device itself. There are many components and interconnect involved, so creating schematics for test procedures is not only a good practice but, also required to guarantee successful measurement setups in the laboratory.

4.4.1 Noise Figure Measurement

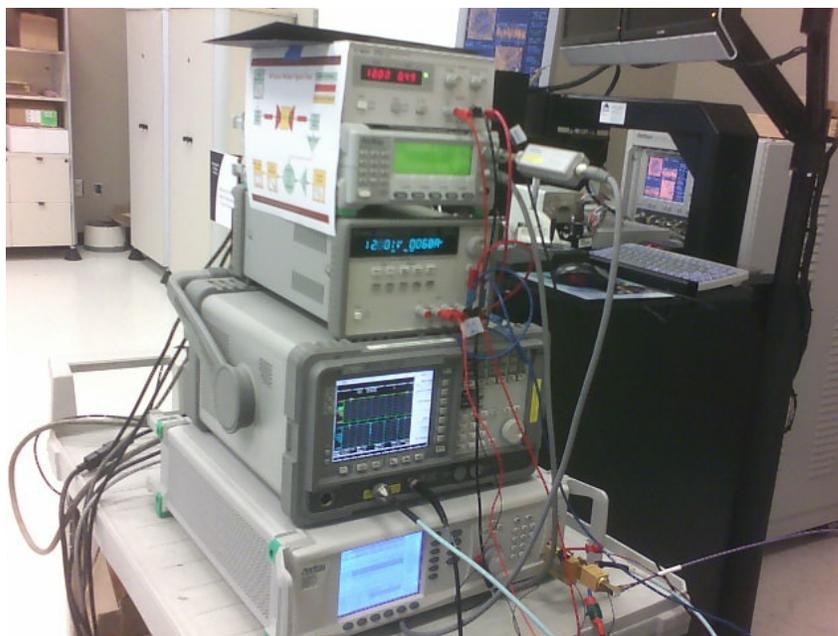
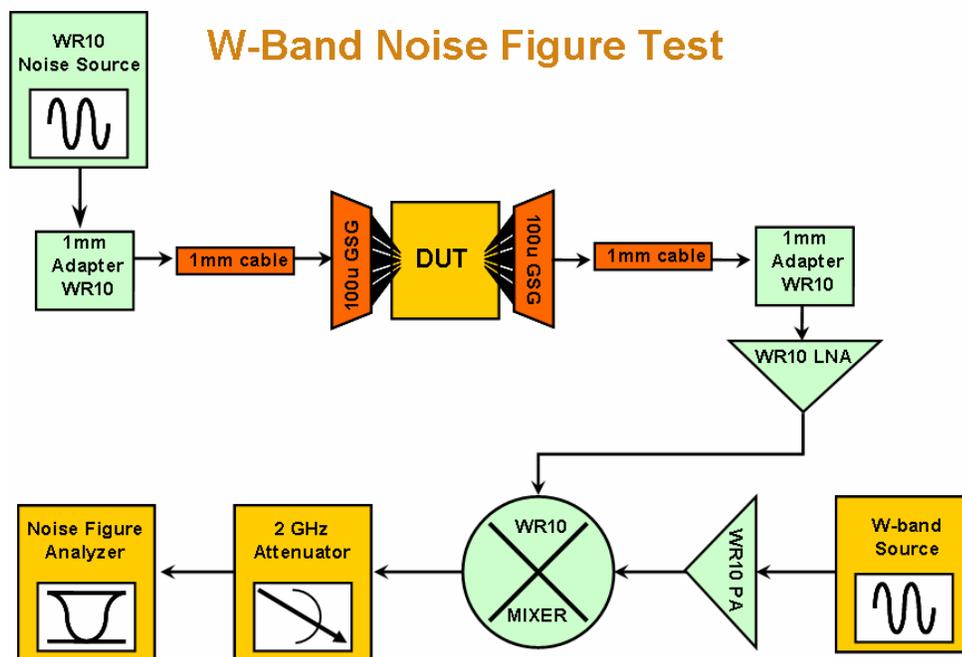


Figure 4-10: Noise Figure Measurement Schematic and Hardware Setup

The millimeter wave noise figure measurement, illustrated in Figure 4-10, requires a direct down conversion to a frequency at which the noise figure meter/analyzer can handle. In this experiment the signals of interest near 100 GHz must be mixed down to about 1.5 GHz. Due to the losses associated with the cables, probes, interconnect and the mixer device, amplification is needed and extensive calibration procedures are required for accuracy.

4.4.2 Linearity Measurements

Like the noise figure experiment the linearity measurements require down conversion in order to identify the signals of interest with the available lab equipment. However, to measure IIP3 two source signals are required. Recalling Figure 3-4, Figure 4-11 illustrates the fundamental goal of the “input third-order intercept point,” or IIP3 measurement. The IIP3 measurement schematic is shown in Figure 4-12. The “1-dB compression point,” or P_{1dB} measurement is similar to IIP3 using only one signal source and is illustrated in Figure 4-13.

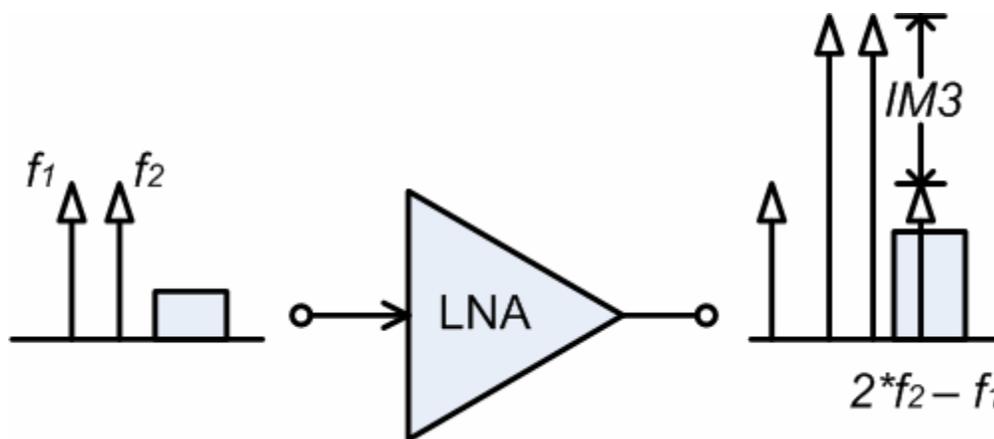


Figure 4-11: Desired Signal Band Corrupted by Intermodulation

IIP3 Linearity Test

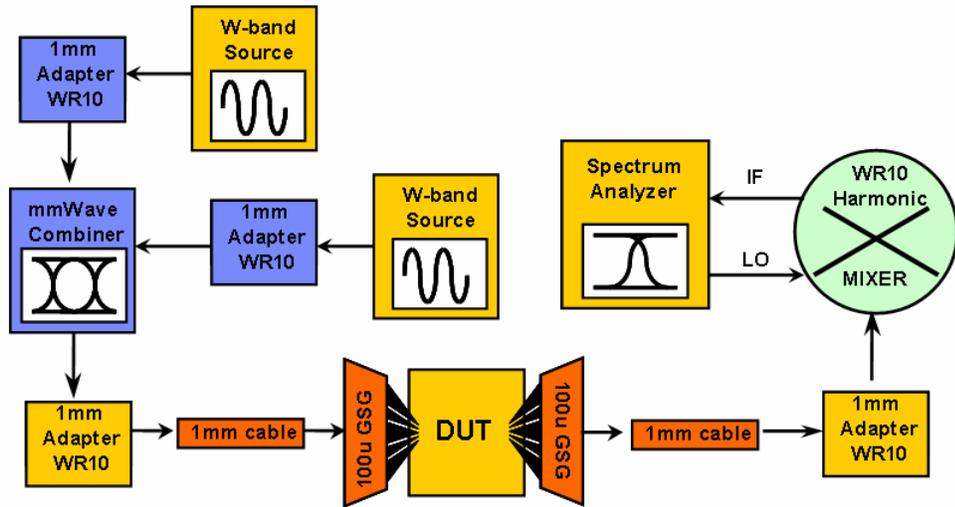


Figure 4-12: IIP3 Measurement Schematic

1dB Compression Point Test

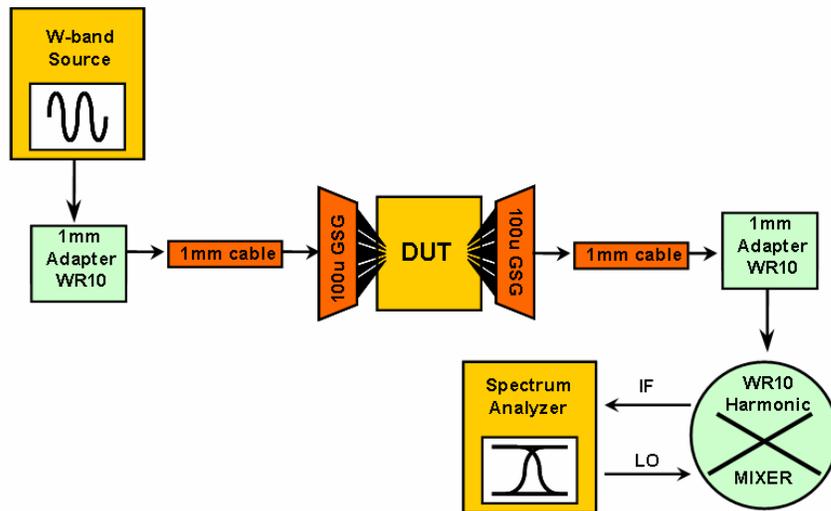


Figure 4-13: 1-dB Compression Measurement

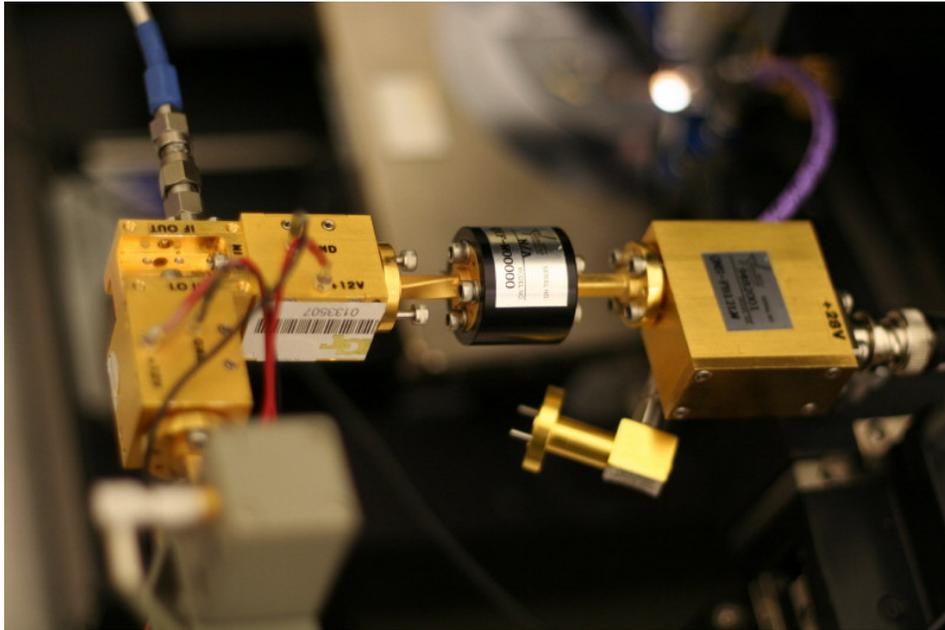


Figure 4-14: mm-Wave Measurement Hardware Blocks

4.5 60 GHz LNA Designs

4.5.1 Single Stage 60 GHz LNA

The design and characterization of a fully integrated V-band (60 GHz) LNA designed with an enhanced Hybrid Transmission Line and a CPGS (a conductive path to ground a P- substrate) is now presented. The LNA was developed in IBM's 8HP 0.12 μm , 200 GHz f_T , SiGe technology. The measured results demonstrate a peak gain of 14.5 dB, a Noise Figure of 4.1 dB with DC power consumption of only 8.1 mW. The amplifier provides 12dB of gain with an average NF of only 5 dB over the entire band of interest. This device has the highest known reported figure of merit for a silicon based 60 GHz LNA as of June 2007. By using the CPGS passive noise suppression technique along with the enhanced Hybrid T-line, the resistance of the

ground path to a P- substrate is reduced significantly, resulting in much improved circuit performance. This technique was adopted from a proven lower frequency application and was applied to this more advanced process in order to help improve RF circuit performance [8].

The schematic used in the single stage design is shown in Figure 4-15. An unconventional series capacitive network was employed to obtain the value needed for a 50 Ω input match. The DC nodes are decoupled with many metal-insulator-metal (MIM) and metal-oxide-semiconductor (MOS) bypass capacitors. The bias circuitry is isolated from the input of the gain stage through a $\lambda/4$ -wave transformation. Each element in the circuit, including interconnect, was extracted in order to carefully examine and minimize parasitic effects. A micrograph of the fabricated chip is shown in Figure 4-16. Total chip area, including pads, is less than 1mm² for the LNA [8].

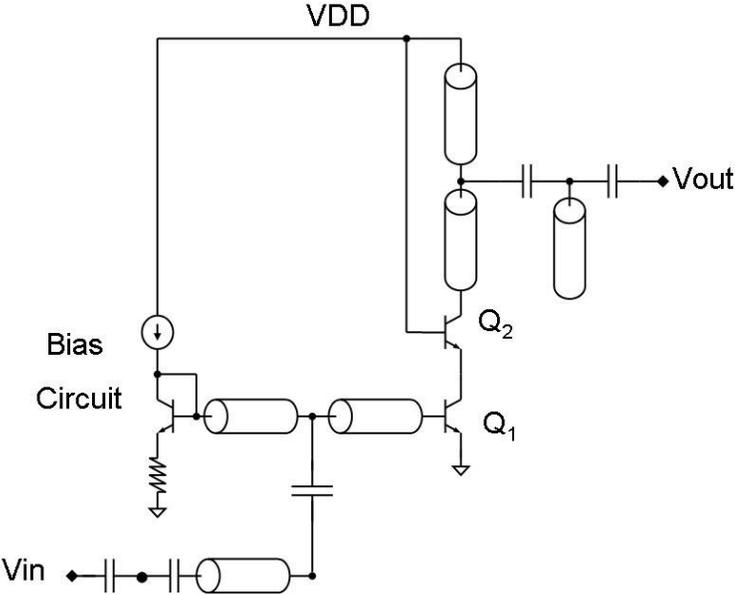


Figure 4-15: Simplified Single Stage 60 GHz LNA Schematic

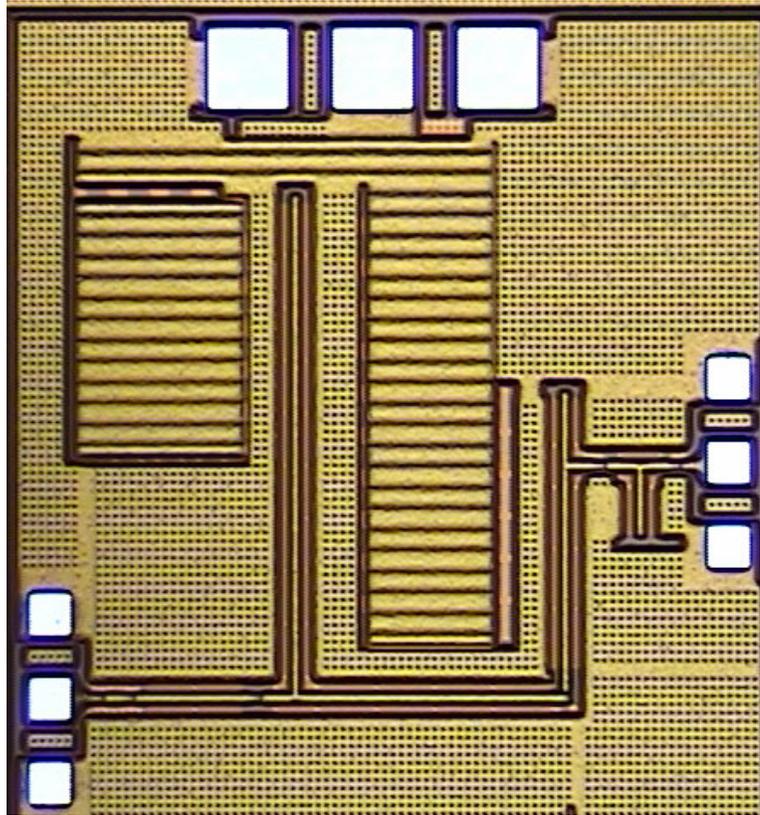


Figure 4-16: Single Stage 60 GHz LNA Die Photo $0.9 \times 1.0 \text{ mm}^2$

The fabricated LNA was characterized using test equipment and components from Agilent, Cascade, Quinstar, and Anritsu. The Noise Figure was measured to be 4.1 dB at 59 GHz using the down conversion mixing technique described earlier and is displayed with simulation results in Figure 4-17. As of June 2007, this LNA has the lowest known reported Noise Figure for a 60 GHz silicon amplifier. The S-Parameters were measured directly (without conversion) and are shown with simulation results in Figure 4-18. The Gain and Noise Figure are illustrated together in Figure 4-19. The peak Gain of 14.5 dB occurs at 59 GHz and the amplifier provides a minimum of 12 dB from 57 – 64 GHz with an average NF of 5 dB. The

LNA is able to deliver this performance while consuming only 4.5 mA from a 1.8 V supply. The measured output 1-dB compression point is +1.5 dBm, resulting in a power efficiency of 17.4%. The simulated IIP3 with 50 MHz tone spacing varies from -5 dBm to +8 dBm, the extrapolated IIP3 is -2 dBm based on the measured input 1-dB compression point of -12 dBm shown in Figure 4-18. The Model-to-Hardware correlation for this work is very good.

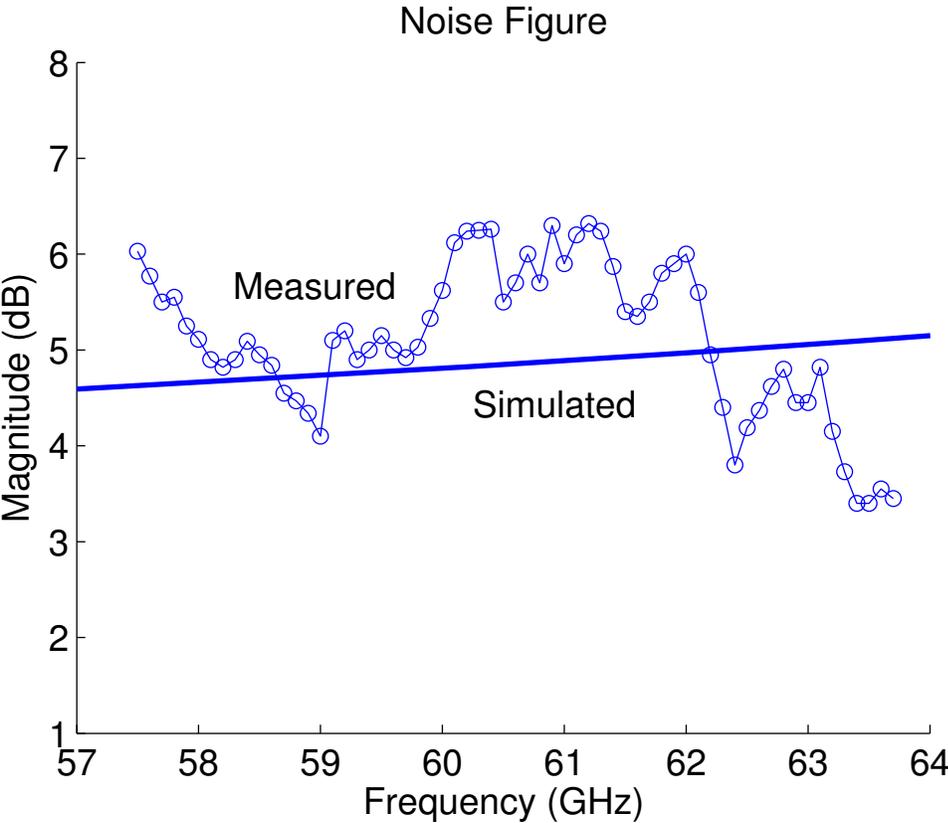


Figure 4-17: Measured and Simulated Noise Figure data

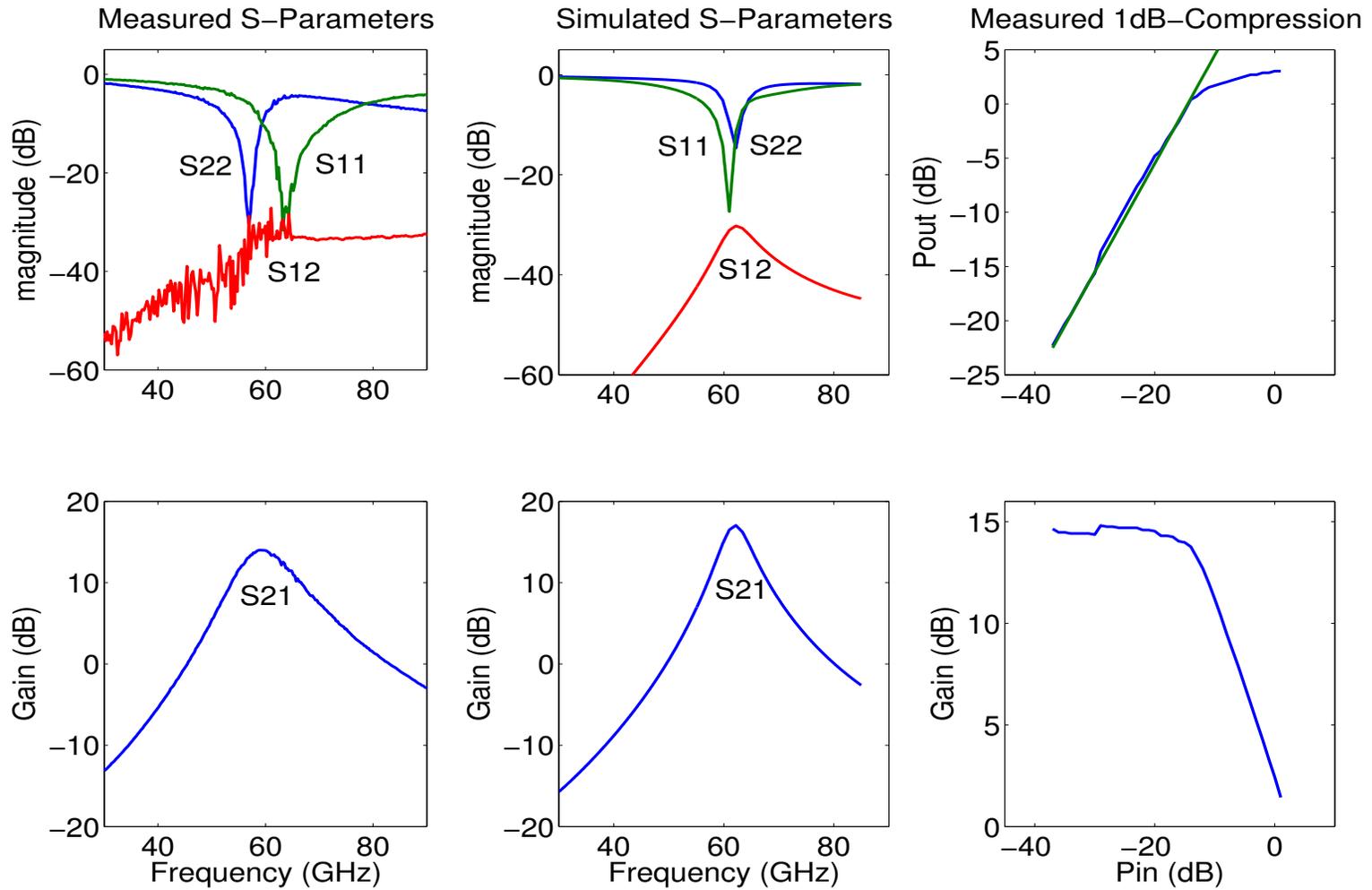


Figure 4-18: Simulated and Measured S-Parameter data of the 60 GHz LNA

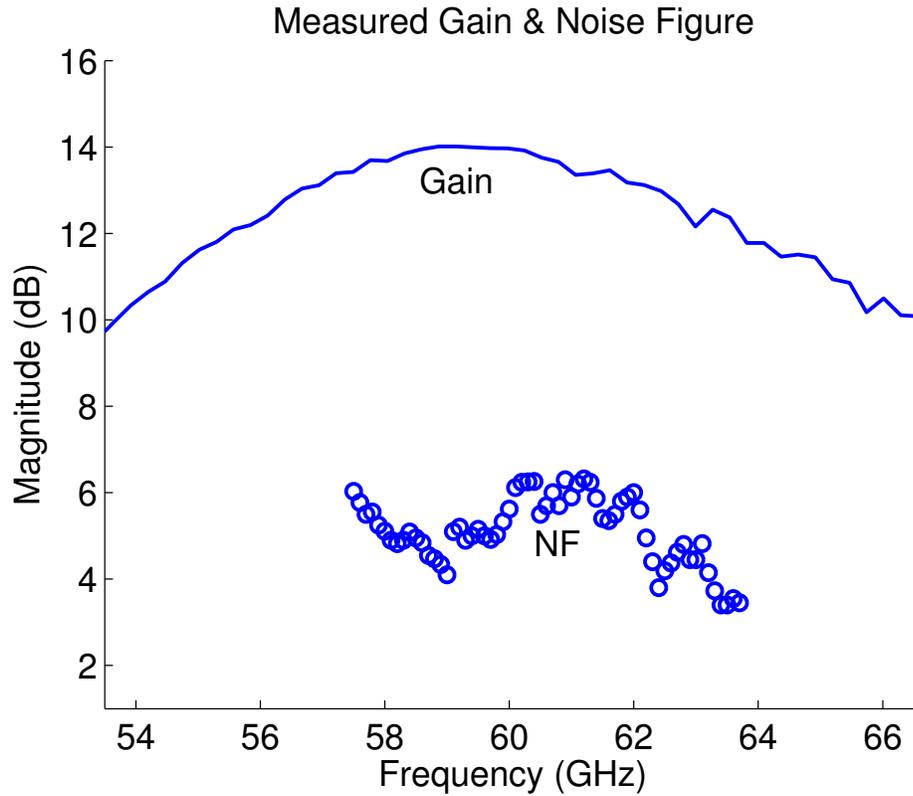


Figure 4-19: Measured Gain and Noise Figure data of the Single Stage 60 GHz LNA

The performance results for the single stage 60 GHz LNA are summarized and benchmarked against the current (as of June 2007) state-of-the-art 60 GHz LNAs in Table 4-1. This device has the highest known reported figure of merit and lowest measure noise figure for a 60 GHz LNA. The highlighted terms in Table 4-1 represent the best results amongst the state-of-the-art amplifier designs. The figure of merit (FOM) used in Table 4-1 is defined as:

$$FOM_{LNA} = \frac{G \cdot IIP3 \cdot f}{(NF - 1) \cdot P_{DC}} \quad (4.5.1)$$

Table 4-1: Comparison of State-of-the-Art 60 GHz LNAs

LNA Metric	Floyd [30]	Gordon [31]	This Work	Heydari [32]	Yao [33]
Frequency (GHz)	61.5	65	59	62	58
Bandwidth (GHz)	8	5 (est)	10	5	5 (est)
Gain (dB)	14.7	14	14.5	12.2	14.6
Noise Figure (dB)	4.5	10.5 (sim)	4.1	6 (sim)	4.5 (sim)
IIP3 (dBm)	-8.5	-6	-2	+2	-6.8
DC Power (mW)	10.8	34	8.1	10.4	24
Technology	200/290 GHz f_T / f_{max} SiGe HBT	160/160 GHz f_T / f_{max} SiGe HBT	200/290 GHz f_T / f_{max} SiGe HBT	140/200 GHz f_T / f_{max} 90nm CMOS	140/170GHz f_T / f_{max} 90nm CMOS
Gain Stages	2	2	1	2	2
Area	0.6 x 0.9 mm ²	0.3 x 0.4 mm ²	0.9x1.0mm ²	0.38x1.27mm ²	0.35x0.4mm ²
FOM (mW ⁻¹)	13.1	1.2	82.5	50.2	8.1

4.5.2 Multi Stage 60 GHz LNA

One can easily deduce from Table 4-1 that many millimeter wave amplifier designs utilize multiple stages in order to achieve a high level of performance. The 60 GHz amplifier featured in the previous section was able to achieve the highest FOM and lowest noise figure via only one stage. This was the driving motivation factor behind implementing a multi stage (two stages) design which incorporates the design techniques (gain peaking, CPGS, etc...) discussed earlier in this dissertation. The multi stage LNA essentially cascades the single stage LNA design illustrated in Figure

4-15. The matching network was then retuned for optimal performance. The cascode transistor devices, bias networks, bias levels are identical to the single stage design. As in the single stage version, the DC nodes are decoupled with many MIM and MOS bypass capacitors. The bias circuitry is isolated from the input of the gain stages through $\lambda/4$ -wave transformations. A micrograph of the fabricated chip is shown in Figure 4-20.

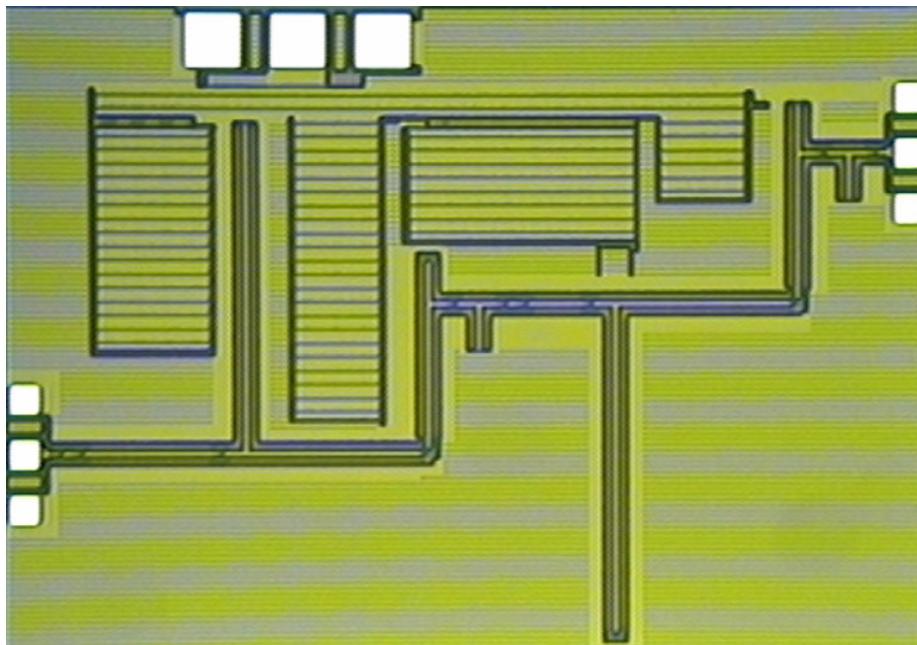


Figure 4-20: Multi (Two) Stage 60 GHz LNA Die Photo

The two stage LNA has yet to be characterized, however, based on the fact that the Model-to-Hardware correlation of the single stage design was very good, the simulation results offered for the two stage design indicate record setting world class performance by setting the highest figure of merit by far for a mmWave LNA. The Noise Figure is 6 dB at 65 GHz. A very broad peak Gain of 35 dB is observed

between 62 and 66 GHz and the amplifier provides a minimum of 30 dB from 60 – 68 GHz with an average NF of 6.5 dB. The LNA is able to deliver this performance while consuming only 16.2mW. The results are shown in Figures 4-21 and 4-22.

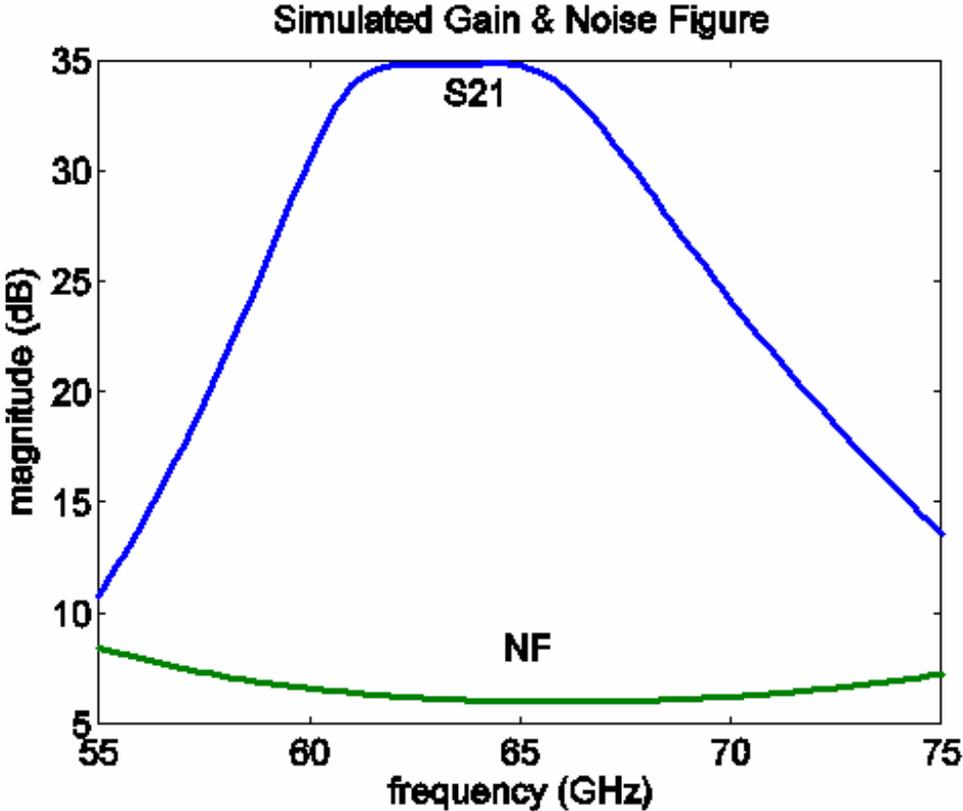


Figure 4-21: Two Stage 60 GHz LNA Gain and Noise Figure Data

At 65 GHz the simulated IIP3 with 50 MHz tone spacing varies from -8 dBm to +1 dBm. Using the FOM described (4.5.1) and the worst case IIP3 simulated, the Two Stage LNA exhibits a figure of merit of over 670. This result is more than a factor of 8x better than the highest known reported figure of merit from Table 4-1.

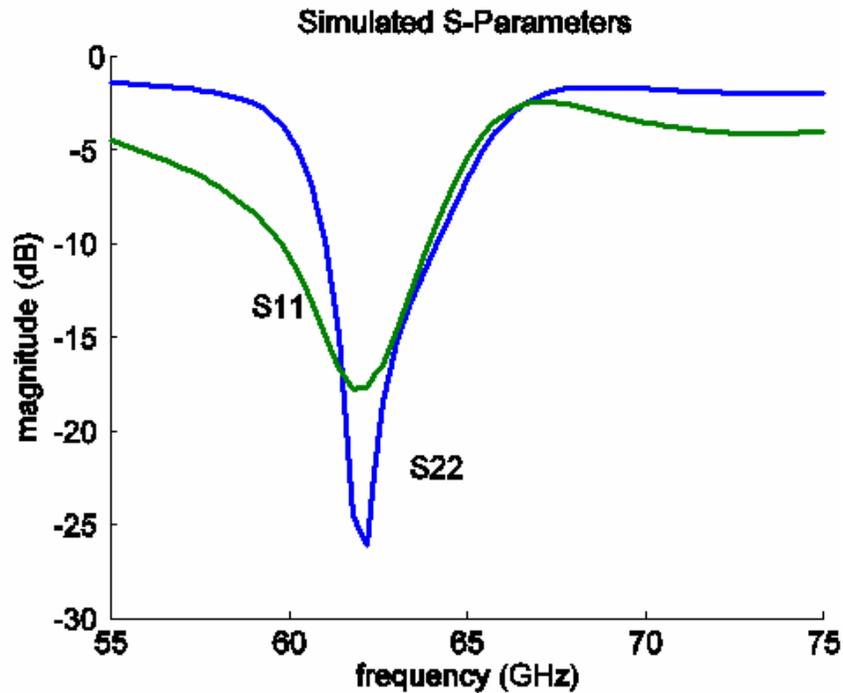


Figure 4-22: Two Stage 60 GHz LNA Input and Output Return Loss

4.6 W-band LNA Designs

4.6.1 Single Stage 90 GHz LNA

The design and characterization of a fully integrated W-band (90 GHz) LNA designed with an enhanced Hybrid Transmission Line and a CPGS (a conductive path to ground a P- substrate) is now presented. The LNA was developed in IBM's 8HP 0.12 μm , 200 GHz f_T , SiGe technology. The measured results demonstrate a peak gain of 13 dB, a Noise Figure of 5.1 dB with a DC power consumption of only 8.1 mW. The amplifier exhibits a 3-dB Gain Bandwidth of 16 GHz from 84 - 100 GHz with a minimum Gain of 10 dB and an average NF of only 5.5 dB. This device has the highest known reported figure of merit for a silicon based W-band LNA at the time of

completion of this dissertation. As in the previously described 60 GHz LNAs the CPGS passive noise suppression technique along with the enhanced Hybrid T-line are incorporated, resulting in outstanding circuit performance. The schematic used in the single stage design is shown in Figure 4-23.

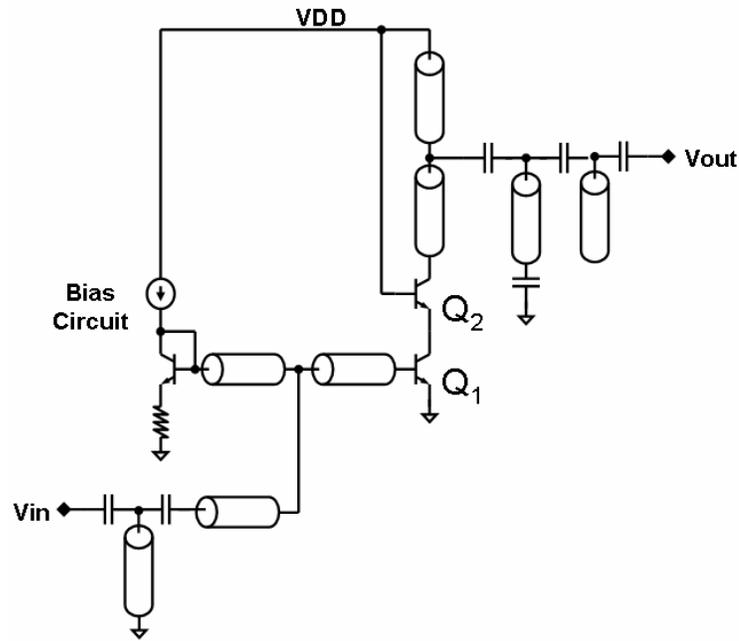


Figure 4-23: Simplified Single Stage 90 GHz LNA Schematic

The DC nodes are decoupled with many MIM and MOS bypass capacitors. The bias circuitry is isolated from the input of the gain stage through a $\lambda/4$ -wave transformation. Each element in the circuit, including interconnect, was extracted in order to carefully examine and minimize parasitic effects. A micrograph of the fabricated chip is shown in Figure 4-24. Total chip area, including bond pads, is less than 0.6mm^2 for the LNA.

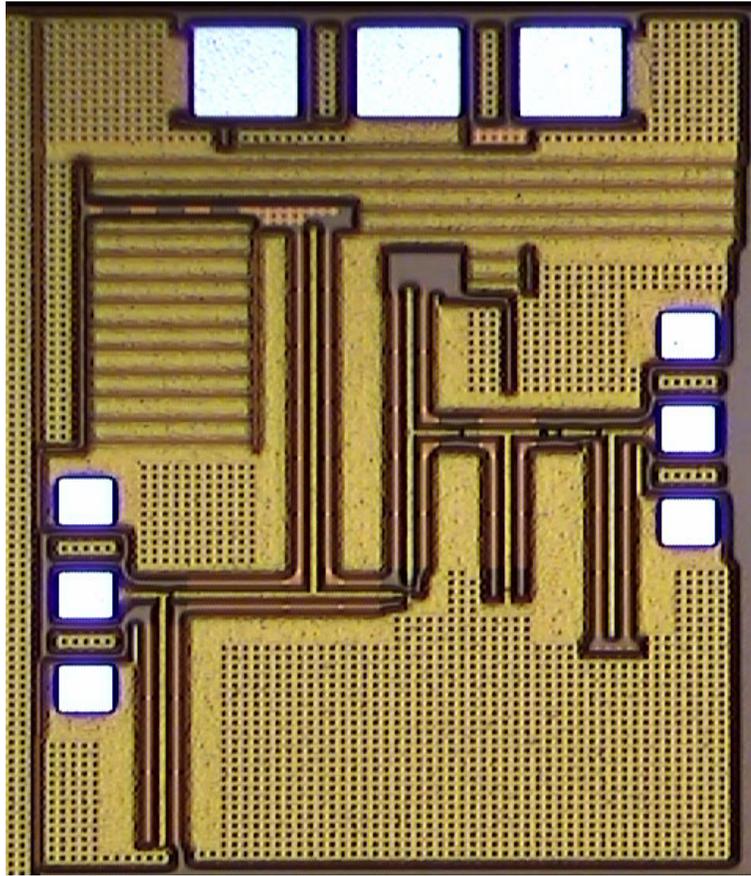


Figure 4-24: Single Stage 90 GHz LNA Die Photo $0.9 \times 0.65 \text{ mm}^2$

The fabricated LNA was characterized using test equipment and components from Agilent, Cascade, Quinstar, and Anritsu. The Noise Figure was measured to be 5.1 dB at 91 GHz using the down conversion mixing technique described earlier. As of June 2007, this LNA has the lowest known reported Noise Figure for a W-band silicon amplifier. The Gain and Noise Figure are illustrated together in Figure 4-25. The S-Parameters were measured directly (without conversion) and are shown in Figure 4-26. A measured input 1-dB compression point of -12.5 dBm is shown in

Figure 4-27. Finally, the measured input Third-Order-Intercept (TOI) or IIP3 using 100 MHz tone spacing is -5.4 dBm, is illustrated in Figure 4-28.

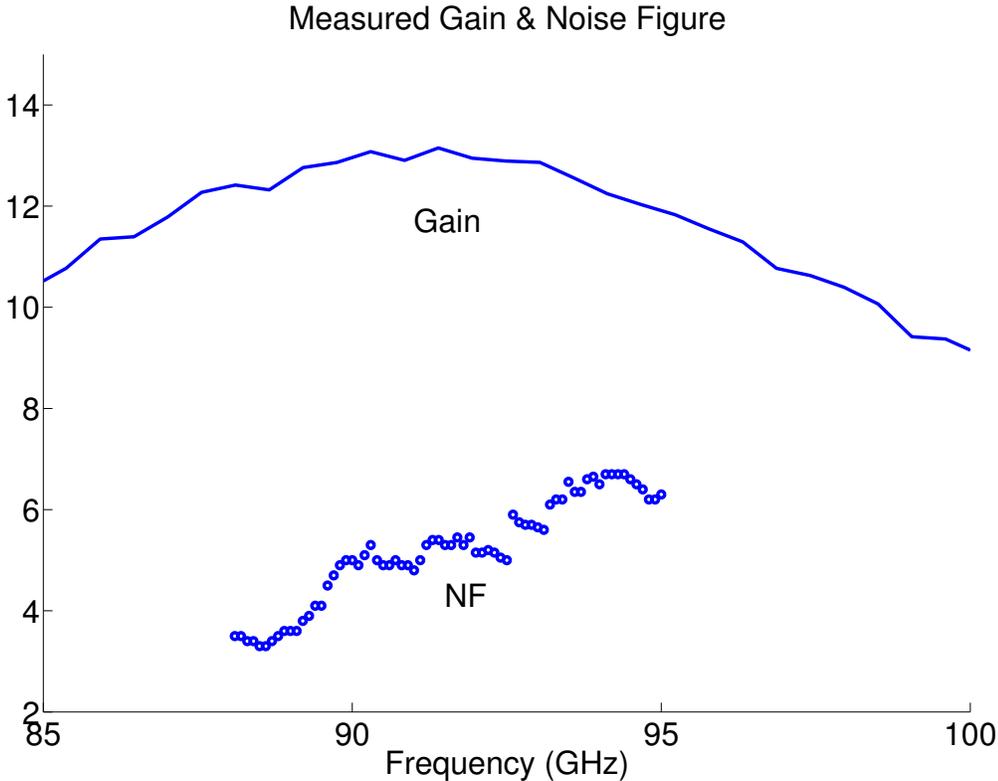


Figure 4-25: Measured Gain and Noise Figure data of the Single Stage 90 GHz LNA

The performance results for the single stage 90 GHz LNA are summarized in Table 4-2. This device has the highest known reported figure of merit for a 90 GHz silicon based LNA at a value of 28.9. The figure of merit (FOM) used in Table 4-2 was described earlier in this dissertation by (4.5.1).

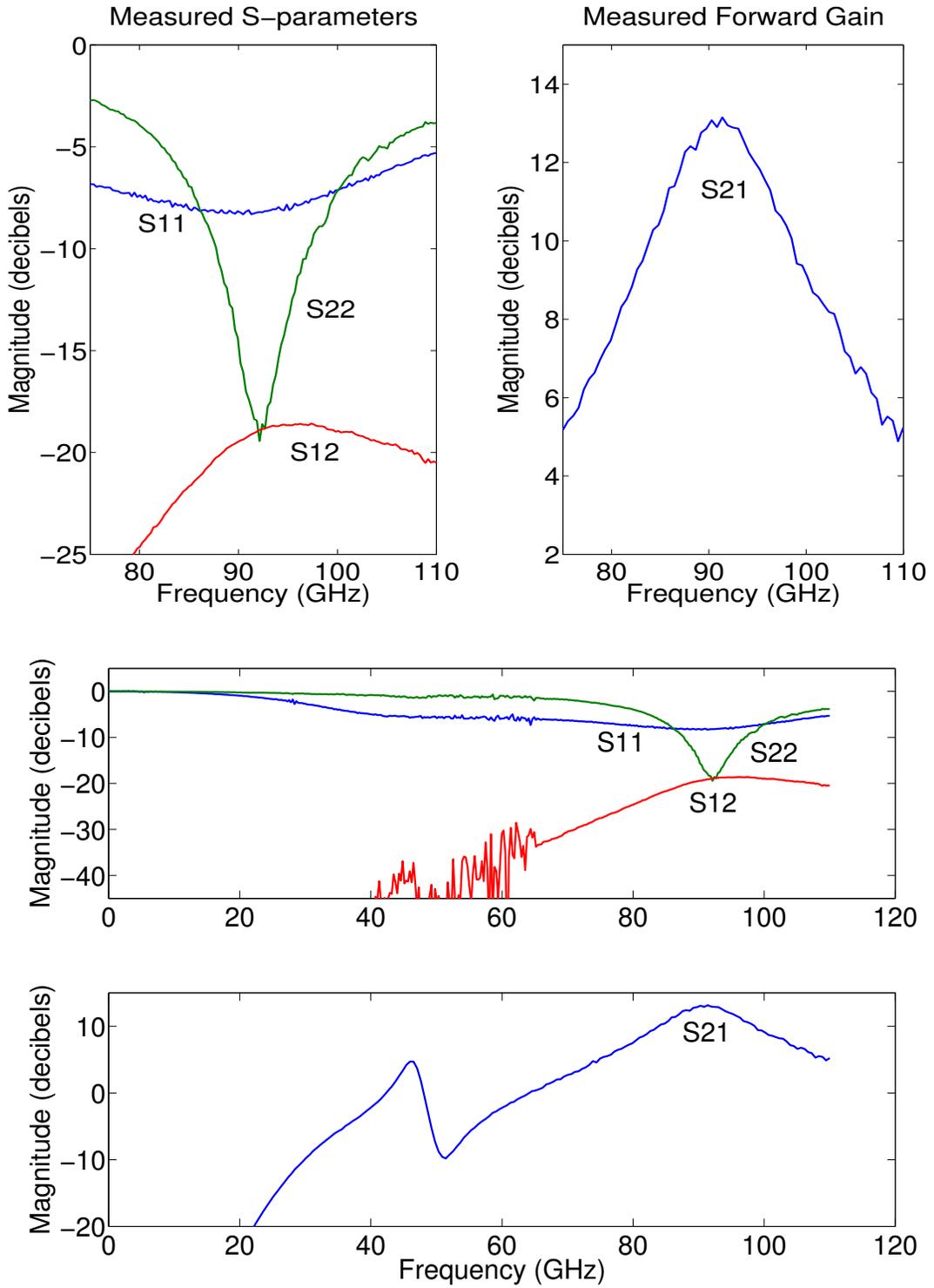


Figure 4-26: Measured S-Parameter data of the Single Stage 90 GHz LNA

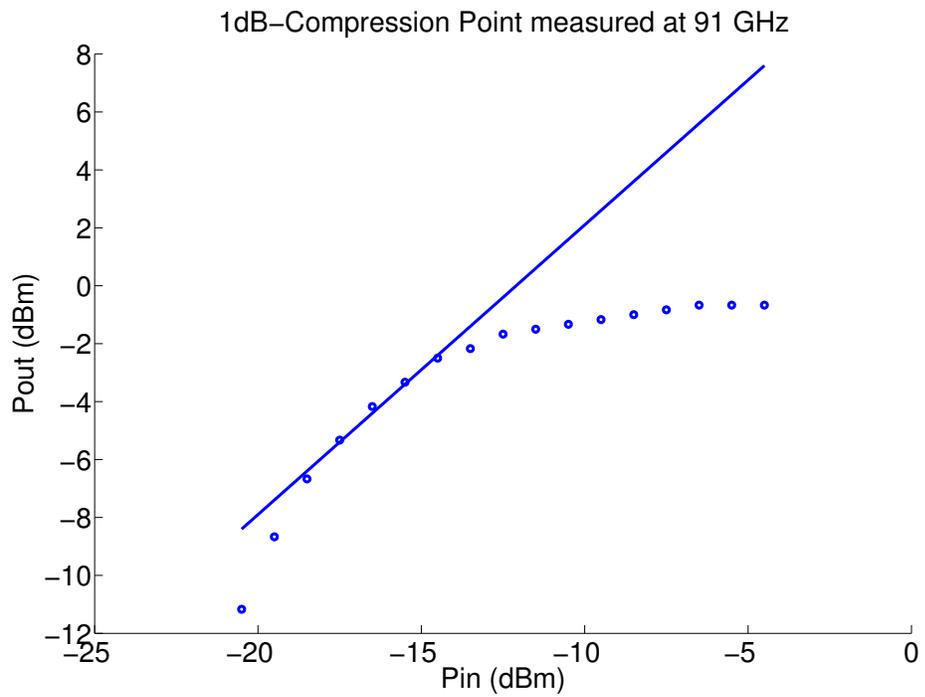


Figure 4-27: 1dB-Compression Point of Single Stage 90 GHz LNA

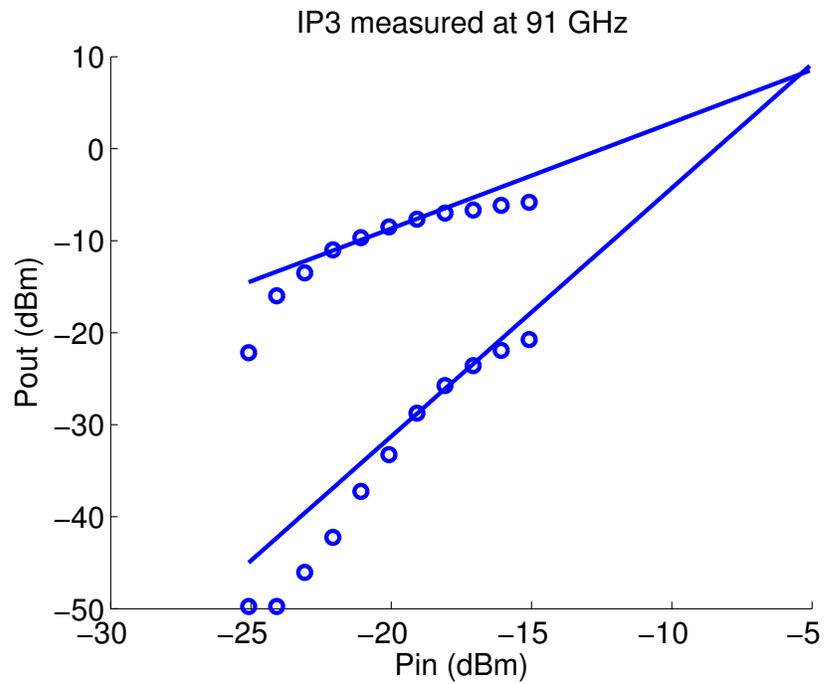


Figure 4-28: Third Order Intercept of Single Stage 90 GHz LNA

Table 4-2: Single Stage 90 GHz LNA Performance Summary

Frequency (GHz)	Bandwidth (GHz)	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)
91	16	13	5.1	-5.4
Gain Stages	Area (mm ²)	Technology	DC Power (mW)	FOM (mW ⁻¹)
1	0.9 x 0.65	200/290 GHz f_T / f_{max} SiGe HBT	8.1	28.9

4.6.2 Multi Stage W-band LNA

The multi (two) stage W-band LNA essentially cascades two identical profile reduced, gain peaked cascode transistor stages with a custom matching network. The schematic design is illustrated in Figure 4-29. The cascode transistor devices, bias networks, bias levels are identical to the single stage design. As in the single stage 90 GHz design, the DC nodes are decoupled with many MIM and MOS bypass capacitors, the enhanced Hybrid Transmission Line and CPGS techniques are employed. The bias circuitry is isolated from the input of the gain stages through $\lambda/4$ -wave transformations. A micrograph of the fabricated chip is shown in Figure 4-30.

The simulation results demonstrate a peak gain of 32 dB, a Noise Figure of 9 dB with a DC power consumption of only 16.2 mW. The Gain, Noise Figure, along with the input and output return losses are illustrated together in Figure 4-31. Though measured results are not presented directly for this device, its simulated performance

has been proven in the Direct Down Converter experiment which is discussed in chapter 5.

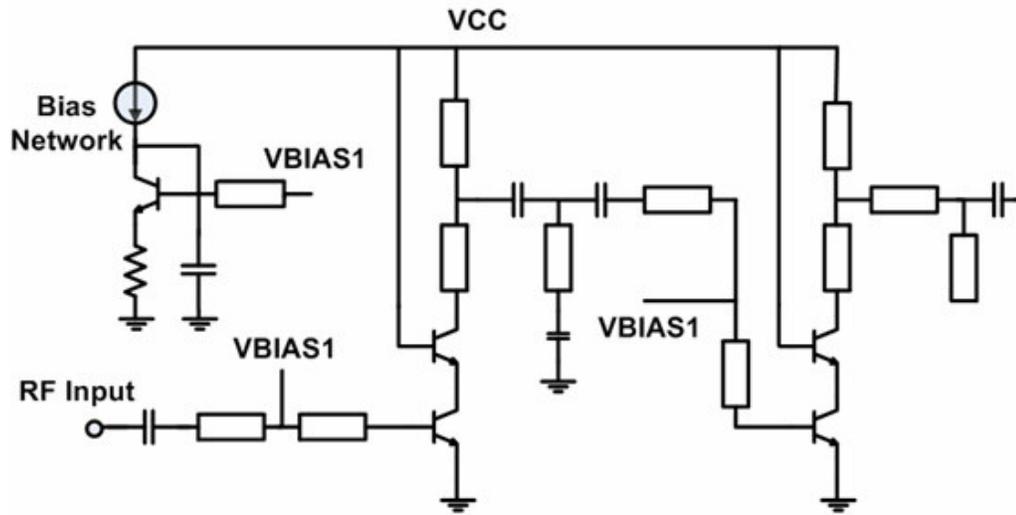


Figure 4-29: Schematic of Two Stage W-band LNA

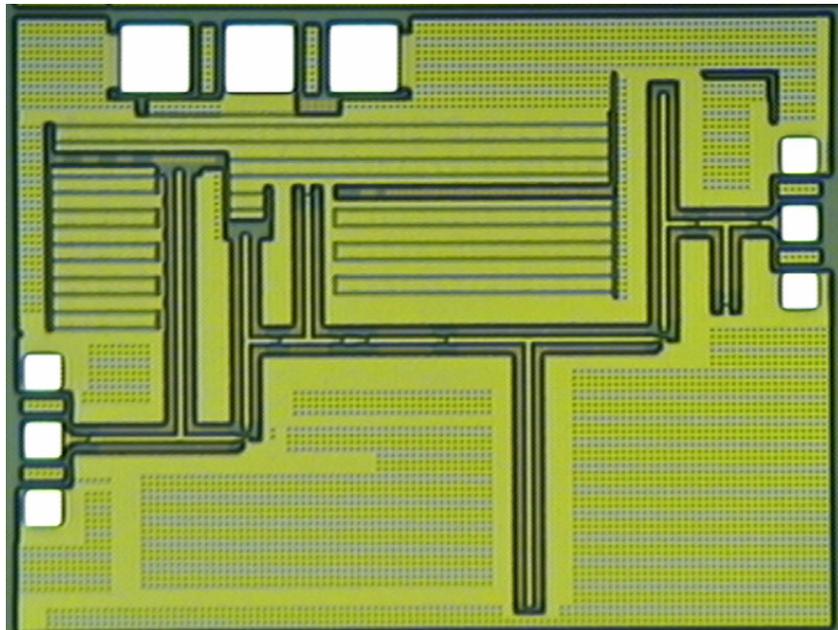


Figure 4-30: Two Stage W-band LNA Die Photo

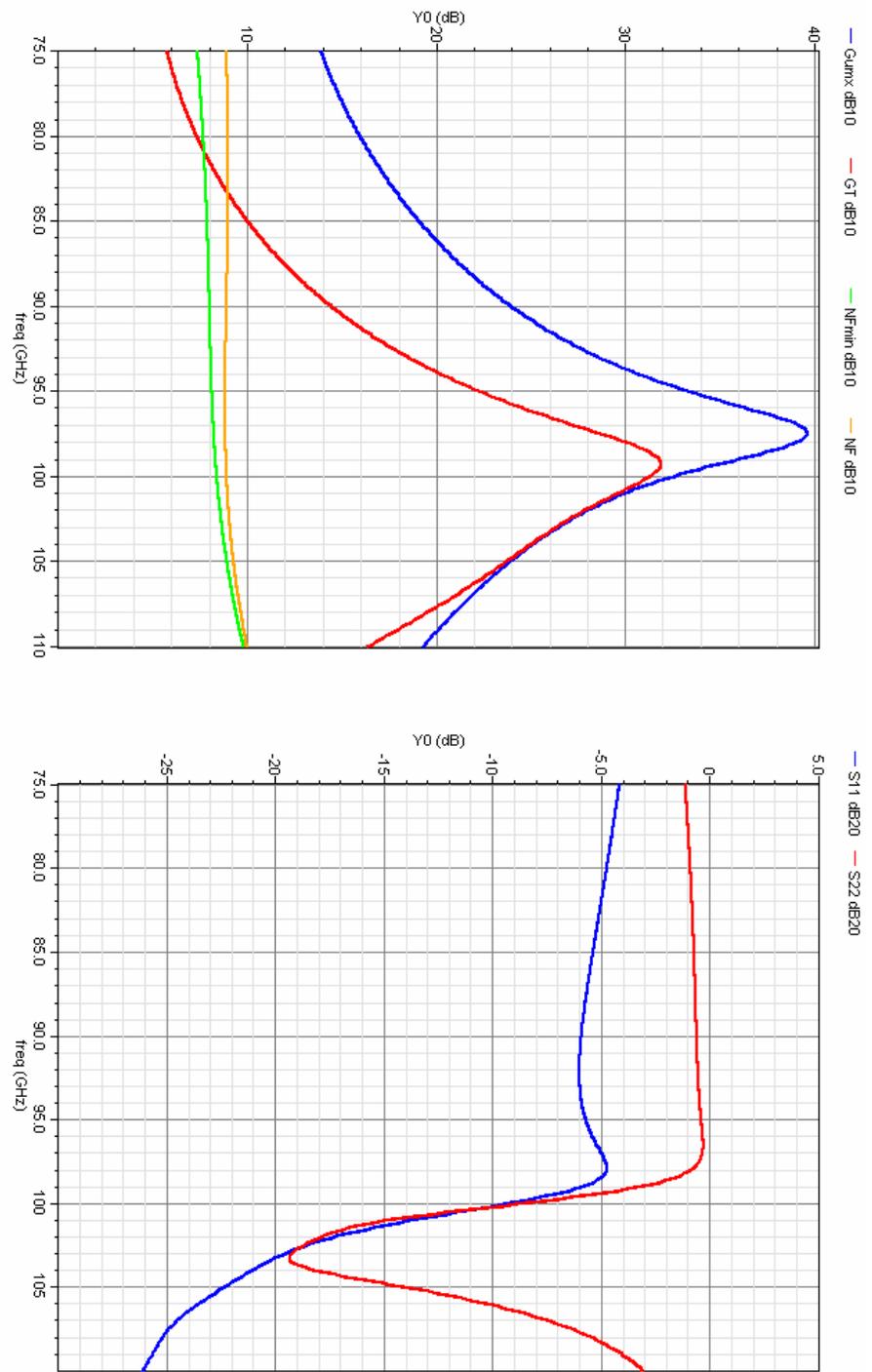


Figure 4-31: Two Stage W-band LNA Performance Data

4.7 Proposed Figure of Merit for LNAs

Several, if not all, of the simulated and measured hardware demonstrations in the previous sections of this chapter achieve the best known reported LNA performance metrics. These metrics include lowest Noise Figure, DC Power, highest Transducer Gain and figure-of-merit FOM, recalling (4.5.1):

$$FOM_{LNA} = \frac{G \cdot IIP3 \cdot f}{(NF - 1) \cdot P_{DC}} \quad (4.7.1)$$

Though (4.7.1) attempts fairly to consider as many different performance metrics as possible, it must be modified somewhat to give credit to designs with large bandwidths especially with the emergence of several wide-band standards and several frequency nodes. Hence the following equation is proposed which considers all the metrics of (4.7.1) as well as the 3-dB gain bandwidth of an amplifier:

$$FOM_{LNA} = \sqrt{f_o \cdot \Delta f} \frac{G \cdot IIP3}{(NF - 1) \cdot P_{DC}} \quad (4.7.2)$$

This new FOM will hopefully promote more thorough reporting of results throughout the field and should be considered as the new standard of ranking and rating all LNAs independent of process technology.

Table 4-1, which summarized and benched marked the state-of-the-art for 60 GHz LNAs, is now recalled and modified in Table 4-3 using the new FOM in (4.7.2). This clearly details the superior performance (in Silicon) achieved using the techniques developed throughout this dissertation. Table 4-4 all summarizes the performance of each LNA described in this chapter.

Table 4-3: Comparison of State-of-the-Art 60 GHz LNAs

LNA Metric	Floyd [30]	Gordon [31]	This Work	Heydari [32]	Yoa[33]
Frequency (GHz)	61.5	65	59	62	58
Bandwidth (GHz)	8	5 (est)	10	5	5 (est)
Gain (dB)	14.7	14	14.5	12.2	14.6
Noise Figure (dB)	4.5	10.5 (sim)	4.1	6 (sim)	4.5 (sim)
IIP3 (dBm)	-8.5	-6	-2	+2	-6.8
DC Power (mW)	10.8	34	8.1	10.4	24
Technology	200/290 GHz f_T / f_{max} SiGe HBT	160/160 GHz f_T / f_{max} SiGe HBT	200/290 GHz f_T / f_{max} SiGe HBT	140/200 GHz f_T / f_{max} 90nm CMOS	140/170GHz f_T / f_{max} 90nm CMOS
Gain Stages	2	2	1	2	2
Area	0.6 x 0.9 mm ²	0.3 x 0.4 mm ²	0.9x1.0mm ²	0.38x1.27mm ²	0.35x0.4mm ²
FOM (mW ⁻¹)	4.7	0.3	34.0	14.9	2.4

Table 4-4: Summary of mm-Wave SiGe LNAs in this Dissertation

Frequency (GHz)	59	91	65	99
3-dB Bandwidth (GHz)	10	16	8	5
Gain (dB)	14.5	13	35	32
Noise Figure (dB)	4.1	5.1	6	9
IIP3 (dBm)	-2	-5.4	-8	-8
DC Power (mW)	8.1	8.1	16.2	16.2

Table 4-4 (Continued)

Gain Stages	1	1	2	2
Area (mm ²)	0.9 x 1.0	0.65 x 0.9	1.0 x 1.2	0.9 x 1.0
FOM (mW ⁻¹)	34.0	12.1	236.7	49.7

4.8 Summary

This chapter described the design techniques employed in mm-Wave Low Noise Amplifiers in Silicon Germanium. Advances in the speed of the silicon transistor and increased complexity of the integrated circuit metallization stack; along with sophisticated Electro-Magnetic (EM) simulation software has fortified design capability. A comprehensive design approach for implementing micro and millimeter wave wireless transceiver front-end circuits was proposed. In this chapter the LNA was the focus because of its vital role in the receiver and the techniques developed can be applied to a myriad of other circuits where the operating frequency is high, noise must be curtailed and the dimensions of passive structures are comparable to the signal wavelength.

An enhanced Hybrid Transmission Line was developed to mitigate the implementation of the passive noise reduction layout technique developed in the previous chapter. Also, a new concept in SiGe device sizing using Mason's Unilateral Gain and Current Gain peaking, which essentially exploits parasitic capacitances in order to tune unilateral and current gain peaking for operation frequencies upwards of 100 GHz, was discussed. Simulation and measured hardware demonstrations confirm the validity of the proposed design techniques and methodology. Several best known reported LNA performance metrics were achieved and described in this chapter. A new figure-of-merit (FOM) equation for amplifiers was also proposed.

Chapter 5: 94 GHz Direct Down Converter²

5.1 Motivation and Challenges

With emerging demand on many applications in millimeter-wave transceiver systems, Silicon-Germanium (SiGe) technology has been widely utilized to implement circuits operating at V-band and W-band frequency range. Recent SiGe technologies provide sufficiently high speed active devices with maximum transition frequency (f_t) of 200 GHz or higher and well-modeled passive components including microstrip transmission lines. Due to its high integration level and cost effectiveness in comparison to other compound technologies, SiGe HBT technology has been proven to be a very attractive solution for millimeter-wave integrated circuit applications. In terms of the high gain and low noise performance SiGe is also more competitive alternative than sub-micron CMOS technology thus far [36], [37], [38].

In the frequency range of 57-64 GHz, a receiver developed in 200 GHz- f_t SiGe process demonstrated 38-40 dB of conversion gain, a 5-6.7 dB noise figure and a -36 dBm input 1-dB compression point [36]. That receiver, features a LNA, RF mixer, IF VGA, IF mixer and a PLL, is known as the most successful demonstration of a WPAN receiver. Other receivers in SiGe technology for 77 GHz applications, such as automotive radar or passive imaging, have been reported in [37] and [38]. In [37] the receiver includes a LNA, an active balun and a double balanced mixer with an LO balun and achieves 30 dB of conversion gain, an 11.5 dB noise figure and a -26 dBm input 1-dB compression point. The receiver presented in [38] is composed of a two-stage differential LNA, a double balanced mixer and a voltage-controlled

² The results in this section are part of a collaborative effort with Jihwan Kim of the Georgia Institute of Technology and the results had been submitted to [35]; notification of acceptance will be announced by early March 2008.

oscillator (VCO) and exhibits 40-46 dB of conversion gain and a -38 dBm input 1-dB compression point.

5.2 Overall System Design

This work features a receiver front-end implemented on a single-chip operating from 87-94 GHz with more than 36 dB of peak conversion gain and a noise figure of only 10 dB. This W-band receiver, composed of a two-stage cascode LNA, a coupled-wire Marchand balun and a Gilbert cell double balanced mixer, could potentially be utilized in low cost frequency modulated continuous wave (FMCW) radar applications in the 94 GHz frequency range. The receiver front-end was fabricated using IBM's 0.12 μm SiGe BiCMOS technology (SiGe8HP) with a f_i/f_{max} of 200/290 GHz. Conveniently, SiGe8HP also features 0.13 μm CMOS devices. For multi-leveled passive structures and ease of signal routing, seven metal layers are available consisting of two thick aluminum layers at the top and five thin copper layers. Metal-insulator-metal (MIM) capacitors and metal-film resistors are also available in this technology. As in the mm-Wave designs of the previous chapters, each transmission line section utilized in the matching networks and in the Marchand balun, implements the enhanced hybrid transmission line structure with 4 μm thick aluminum signal lines with coplanar-style ground shields along the sides and a microstrip-style lower ground bottom plane [35].

The comprehensive design flow proposed in chapter 4 was utilized in this work, which provides a process in which a designer will make well informed and/or even innovative design choices. As a design progresses through the flow, the circuit becomes a hybrid blend of schematic, layout and custom model blocks. Electro-magnetic (EM) modeling of interconnect, parasitic effects on circuit performance, as

well as substrate conditioning via the conductive path to ground the substrate (CPGS) technique, were all taken into consideration in this experiment [35].

5.2.1 Marchand Balun

From the single-ended output of the LNA to differential input of the mixer, the Marchand balun was used to generate differential signals with 180° phase difference. The Marchand balun is known as the most popular structure for splitting signals because of its wide bandwidth and ease of implementation [39]. In the W-band frequency range, a $\lambda/4$ -wave length of the carrier signal is only about 300-400 μm , which makes it very feasible and practical to be utilized in a single-ship application. The optimum coupling factor can be achieved by adjusting the width of the signal path and distance between two signal paths in coupled-wire transmission lines, which were chosen to be 5 μm and 20 μm , respectively in this design. The stand-alone Marchand balun was also fabricated in order to characterize its transmission loss. The schematic model and measured data for insertion loss are shown in Figure 5-1. In the frequency range of 87-94 GHz the single-ended loss is about 7.8 dB which converts to a differential loss of about 4.8 dB [35].

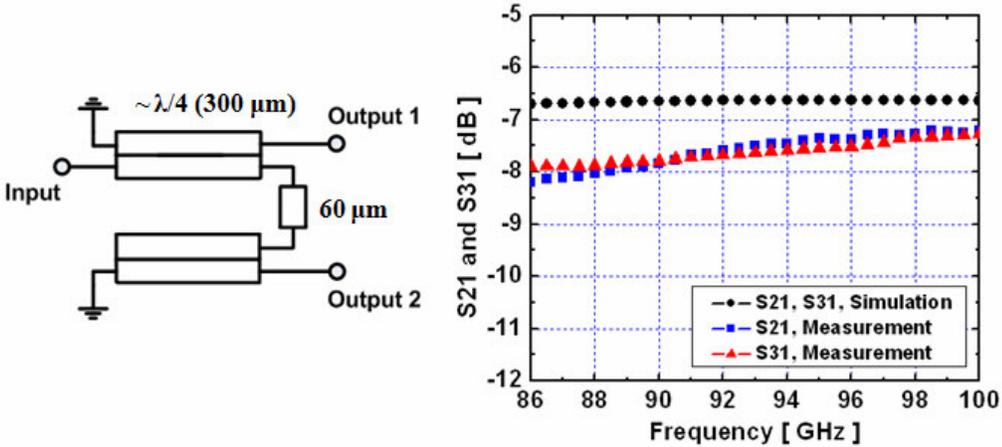


Figure 5-1: Schematic Model and Measurement of Coupled-Wire Marchand Balun

5.2.2 Active Balun

A two-stage W-band Low-Noise Amplifier (LNA) using the unilateral gain peaking design technique with profile reduction from chapter 4 was implemented. A schematic of the amplifier and combined balun is shown in Figure 5-2. Parasitic capacitances from the layout of the cascode transistors are exploited in order to frequency shift the peak of Mason's Unilateral Gain to the desired operating range. This methodology enhances overall amplifier (circuit) gain performance tremendously without additional dc power consumption or penalty in Noise Figure. A cascode amplifier topology was used because it provides high gain and good isolation. The advantages are immunity from Miller effect, and it allows for semi-unilateral matching networks. The dc nodes are decoupled with many MIM and MOS bypass capacitors. The bias circuitry is isolated from the input of the gain stages through a $\lambda/4$ -wave transformation. Each element in the LNA, including interconnect to the balun, was extracted in order to carefully examine and exploit parasitic effects. All of the T-junctions were realized using the same structure which was modeled with an EM simulator.

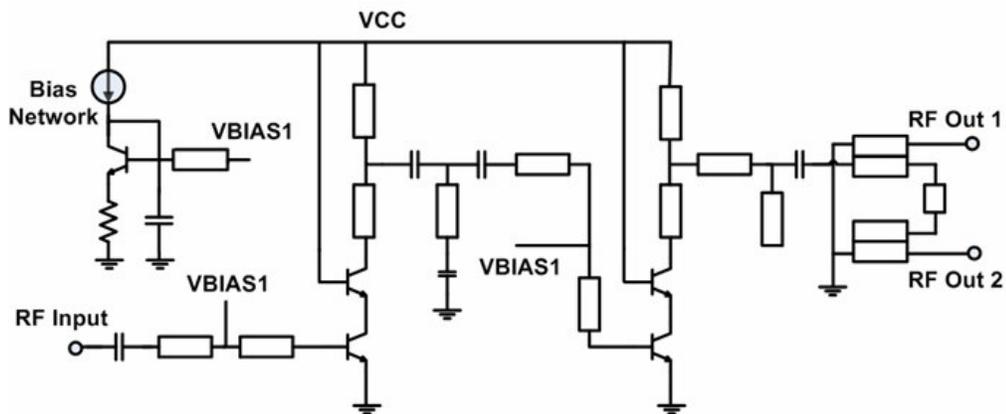


Figure 5-2: Schematic of Active Balun (LNA and Marchand Balun Combination)

The Active-Balun (LNA with Marchand balun) featured here provides a tremendous amount of gain and maintains a 180° phase difference. Some simulated performance metrics of the active balun, which does not consider the excess capacitance of the anticipated Mixer load causing a small shift in operating frequency, are offered in Figure 5-3. Since the LNA is the first gain stage in the receiver path, its' noise figure dominates that of the overall system. Afterwards the subsequent receiver components add noise to an already amplified signal, leading to a much better signal-to-noise ratio than an un-amplified signal.

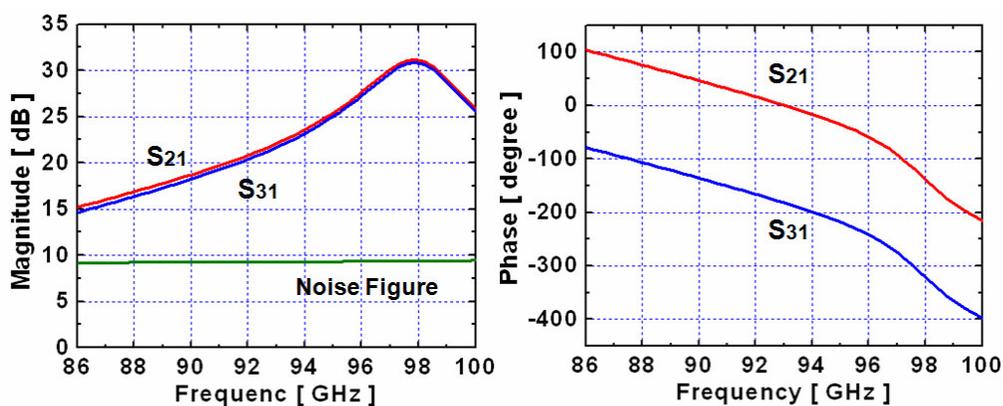


Figure 5-3: Simulated S21, S31, NF and Phase Difference of the Active-Balun

5.2.3 Mixer³

A Gilbert cell double balanced topology was chosen due to its superior performance in terms of high Conversion Gain and high linearity while effectively suppressing feed-through between LO, RF and IF ports in comparison to other configurations. The Mixer down-converts RF signal at 87-94 GHz to the low IF frequency of 500 MHz. Avoiding DC offset problems the selected low IF frequency makes design of whole down-conversion receiver system simple. The

³ The circuit in this section was developed by Jihwan Kim of the Georgia Institute of Technology

transconductance portion of the Mixer interfaces with RF matching network, and is optimized to achieve the highest power gain and the lowest Noise Figure simultaneously. The bias current density and transistor size of the switching part were chosen for the highest operating speed to maximize the Conversion Gain. The designed RF and LO input matching network were implemented using hybrid transmission lines and MIM capacitors. The on-chip coupled-wire Marchand balun was also used to generate differential LO signal from an external signal source. In order to shift down the voltage level at the output node of the Mixer core the emitter follower was used. This emitter follower drives the IF signal to the output buffer which is a conventional differential amplifier having a 50Ω output impedance. A simplified circuit schematic of the designed Mixer, including matching networks and the LO balun is shown in Figure 5-4. Thorough consideration was taken into account in the layout to minimize the signal coupling through the substrate. The technique of conductive path to ground the substrate was used to improve the port-to-port isolation [35].

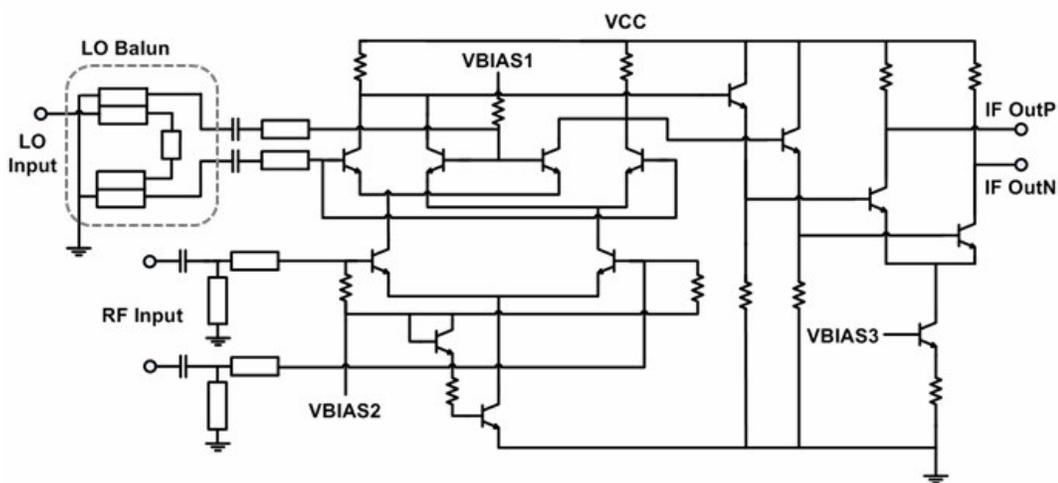


Figure 5-4: Simplified Schematic of Mixer and LO Balun

5.3 Measured Results

On-wafer measurement using Cascade Microtech's 110 GHz GSG probes for RF and LO input was performed. GSSG probe was used for the IF output. To generate 85-100 GHz external signal two millimeter-wave source modules, OML's S10MS and Agilent's 83558A, were used in combination with Hewlett Packard's 20 GHz signal generators (83622B). Using the Agilent's W-band power sensor (W8486A) and power meter (E4419B) reference power level table was made through the frequency range of interest de-embedding all the possible losses due to RF cables and wave-guide adapters, etc. The minimum power level that was able to be generated was around -60 dBm. RF power level of -50 dBm was chosen to observe variation of Conversion Gain with sweeping RF input frequency or applied LO power level. In all cases, IF output frequency was fixed at 500 MHz. Single-Side-Band (SSB) Noise Figure was measured using Quinstar Technology's W-band noise source (QNS-FB12LW) and Agilent's Noise Figure analyzer (N8972A). Careful calibration was performed with the W-band noise source in combination with the Wave-Guide Mixer (QMB-FBFBWS), LNA (QLW-75B05015-I1) and PA (QPW-75B01315-I1) before measuring the actual Noise Figure [35].

Measured conversion gain and SSB noise figure versus RF input frequency and LO input power levels are presented in Figure 5-5 and Figure 5-6 respectively. A maximum conversion gain of 36.3 dB was achieved at a 2 dBm LO power level at 91 GHz. In the frequency range of 87-93 GHz, the conversion gain is at least 32 dB. Measured minimum SSB noise figure was 10 dB at 92 GHz. From 85 to 96 GHz, SSB noise figure was less than 15 dB. RF input power level was swept from -58 dBm to -30 dBm to measure the input 1dB compression point of -36 dBm. RF frequency and LO power were fixed at 91 GHz and 2 dBm respectively, this result is shown in

Figure 5-7. S-parameters were measured from 20 GHz to 110 GHz using Agilent's 8510C VNA. Measured results are presented in Figure 5-8.

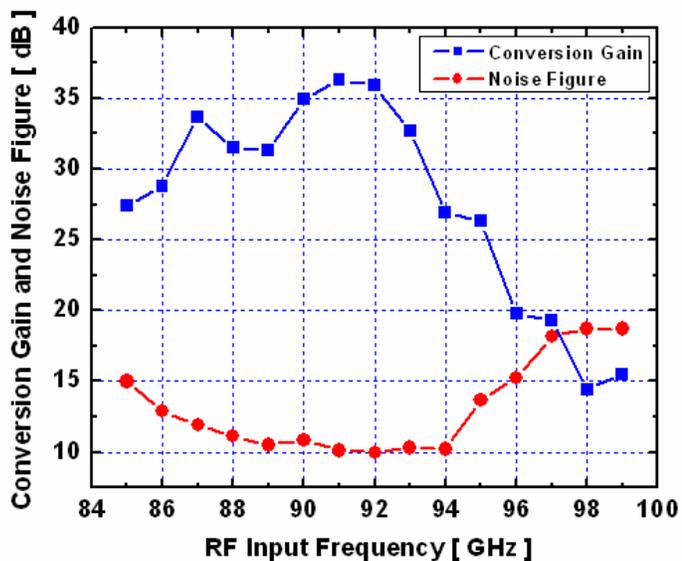


Figure 5-5: Measured Conversion Gain and SSB Noise Figure vs. RF frequency (LO Power is 2 dBm, IF Frequency is 500 MHz)

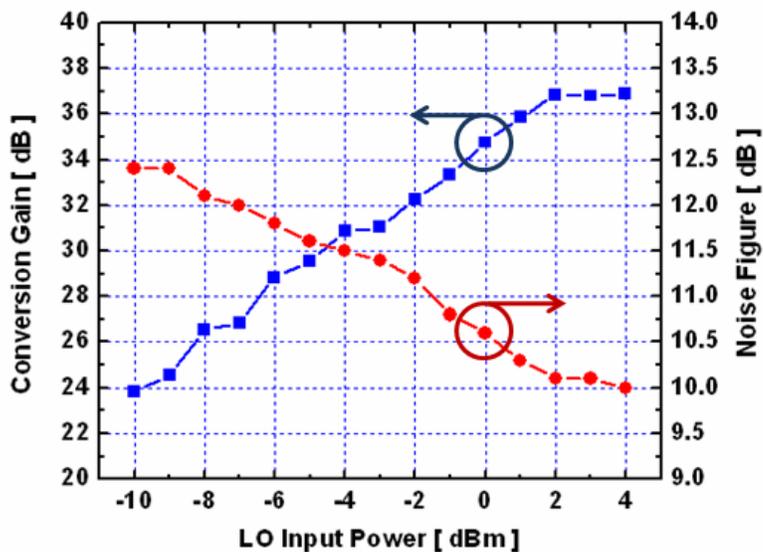


Figure 5-6: Measured Conversion Gain and SSB Noise Figure vs. LO power (RF Frequency is 91 GHz, IF Frequency is 500 MHz)

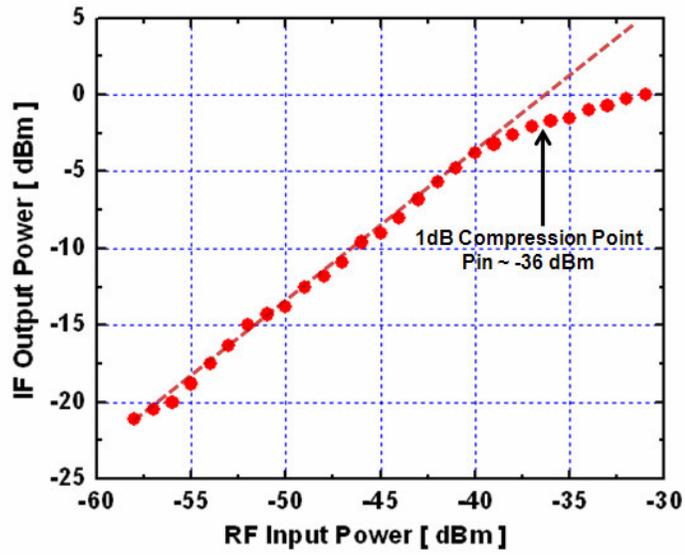


Figure 5-7: Measured IF Output Power vs. RF Input Power at 91 GHz (LO Power is 2 dBm, IF Frequency is 500 MHz)

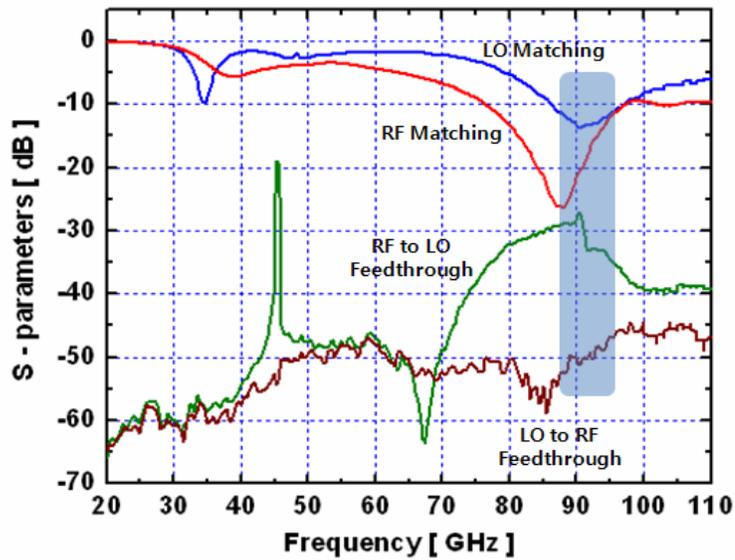


Figure 5-8: Measured Conversion Gain and SSB Noise Figure vs. RF Frequency (LO Power is 2 dBm, IF Frequency is 500 MHz)

5.4 Summary

This chapter described the design of a W-band receiver front-end consisting of a LNA, coupled-wire Marchand balun and Gilbert cell double balance mixer with LO balun. This receiver front-end employed the same techniques utilized in the mm-Wave Low Noise Amplifiers designed in chapter 4. The fabricated receiver consumes 109.7 mW and demonstrates a measured a minimum SSB noise figure of 10 dB at 92 GHz, a peak conversion gain of 36.3 dB and a 1dB compression point of -36 dBm at 91 GHz with good RF and LO port matching and isolation. This circuit is suitable for use in low cost FMCW applications in the 94 GHz range. A die photo of the designed receiver front-end is shown in Figure 5-9.

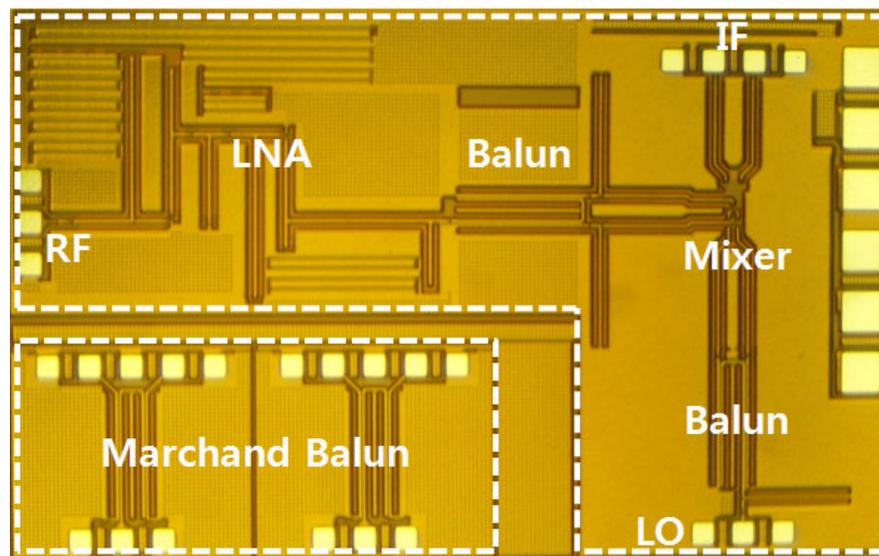


Figure 5-9: Die Photo of Fabricated Receiver, 1.82 mm² Including Pads

Chapter 6: mm-Wave RFID for Biomedical Applications

6.1 Motivation and Challenges⁴

Radio frequency identification (RFID) is becoming more and more popular in areas as purchasing, distribution logistics and manufacturing. Biomedical applications also do a widespread use of RFID as under-skin implants for identification and non-invasive diagnosis. Key factors of RFID are size and cost. Passive RFIDs harvest energy from the incoming RF radiation, without the need of a battery, thus reducing their cost. The antenna is nowadays the only external component required. This chapter proposes an invention of a RFID architecture, circuit design and modulation scheme that allows operation in the license-free millimeter-wave band around 60GHz on a low-cost deeply scaled (90 or 65 nm) CMOS process. At these frequencies (24 or 60 GHz) the physical size of a high-efficiency antenna can be shrunk to a few millimeters. The antenna can now be integrated with the whole RFID (or on silicon backplane), further reducing its size. Cost is also reduced due to no assembly required.

A passive RFID tag has no self-contained power source, but rather harvests its operating power from the RF signal received from the wireless device (typically called an RFID reader) that is interrogating it. Since the harvested power is usually very low (e.g., a few microwatts), passive RFID tags typically operate by simply modulating antenna impedance, so that the signal that is backscattered (i.e., reflected), from the antenna is a modulated version of the signal that was received. Since the RFID reader is receiving a very weak signal while transmitting a much stronger signal on the same frequency, high isolation between the transmitter and receiver sections is required,

⁴ This work in its entirety was performed at Intel Corporation. Stefano Pellerano, J. Alvarado Jr., Yorgos Palaskas, "Non-Backscatter Passive RFID," Docket 42P23608, May, 2006

thus increasing the complexity and cost of the RFID reader. An additional problem with a conventional passive RFID tag is that the size of the antenna, which is dictated by the frequency being used and is typically many times larger than the rest of the RFID tag, creates a minimum size for the RFID tag that makes the tag unfeasible for many applications [40].

6.2 Overall System Topology

At 60GHz the wavelength is only 5mm. Doppler effect and multi-path in indoor environment prevent the use of a coherent modulation scheme (as phase-modulation). An amplitude-shift-keying (ASK) is more suitable for this application. A passive RFID can respond when interrogated using backscattering modulation. The impedance of the receiving antenna is modulated so that the incoming RF carrier is reflected back according to the modulation. The interrogator has to detect the reflected and modulated signal while it is transmitting the RF carrier to power-up the RFID. High isolation between the TX and RX part and a low phase noise oscillator are required for the interrogator, thus increasing its complexity and overall cost. Proposed here is a different modulation scheme that allows the interrogator to switch off its TX section before receiving the RFID data, relaxing the requirements and complexity of its RX section. In the power-up phase, the interrogator is transmitting the RF carrier and the RFID harvests and stores this energy on a storage capacitor. In the transmit phase, the interrogator stops transmitting the carrier and the RFID sends back the data using the energy previously stored into the capacitor. In order to reduce the size of the capacitor so that it can also be integrated with the tag, one bit at a time is transmitted. Each bit consists of a short or long (about twice) pulse of a 60GHz sinusoidal signal generated by an integrated free-running oscillator. Figure 6-1 shows the system block diagram. A voltage multiplier based on [41] harvests the RF energy and stores it into

capacitor C_{STORAGE} . A voltage limiter keeps the multiplier output voltage below the maximum tolerable value. A sensor circuit monitors the voltage on the storage capacitor. When the proper operating voltage is reached (V_{HIGH}) and the end-of-burst (EOB) detector senses that the RF carrier is no longer transmitted by the interrogator, the 60GHz oscillator is turned on for τ or 2τ , depending on the bit to be transmitted. The sensor circuit switches the system back to charging mode when the voltage on C_{STORAGE} has dropped below a certain threshold (V_{LOW}) [40].

6.2.1 Voltage Multiplier and End-of-Burst Detector

An end-of-burst detector is essential for this architecture, since the RFID has to respond back only when the interrogator is not transmitting the RF carrier anymore. Figure 6-2 shows the simplified schematic of the EOB detector. It is embedded into the voltage multiplier (a two-stage multiplier is assumed here for simplicity). The circuit operation is based on the fact that when the input RF carrier is no longer provided, the internal node A of the multiplier will discharge much faster than the output node B, where the storage capacitance is connected. This will turn on both devices M1 and M2, raising EOB.

6.2.2 Short or Long Pulse Generation

A short or a long 60GHz sinusoidal pulse is generated by the embedded VCO depending on the bit to be transmitted. The time duration of the long pulse is about twice that of the short one. This ratio is well-defined over PVT (process and temperature variations) using the scheme illustrated in Figure 6-3. During transmission, most of the current consumption is due to the VCO and its buffer. The long pulse in Figure 6-3a, is defined by the time (2τ) required by the current drawn by the VCO and its buffer to discharge from V_{HIGH} to V_{LOW} . To generate the short pulse in Figure 6-3b, the bias current of the VCO and the buffer are mirrored into two

dummy cells. The doubled current will now discharge the storage capacitor in half the time (τ).

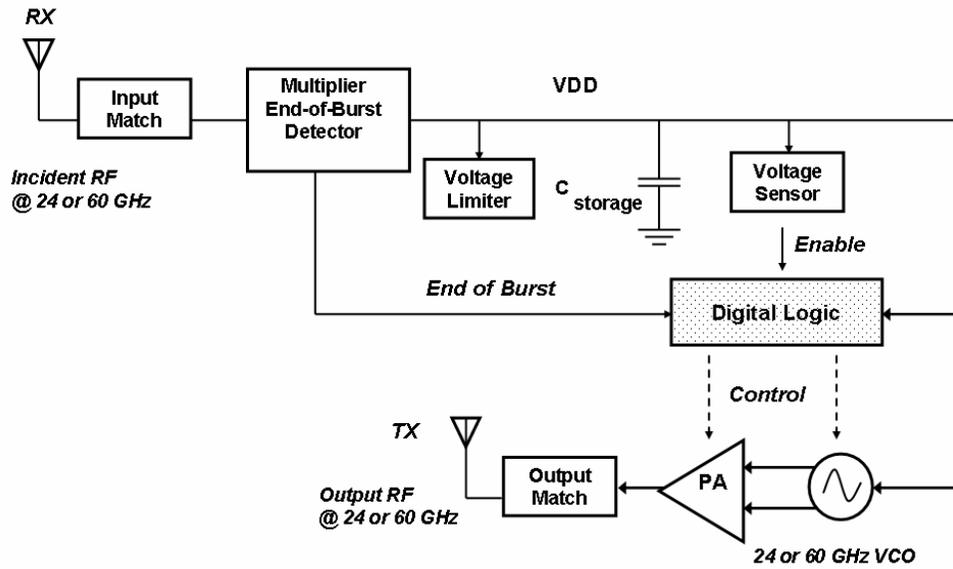


Figure 6-1: Block Diagram of the RFID System Architecture

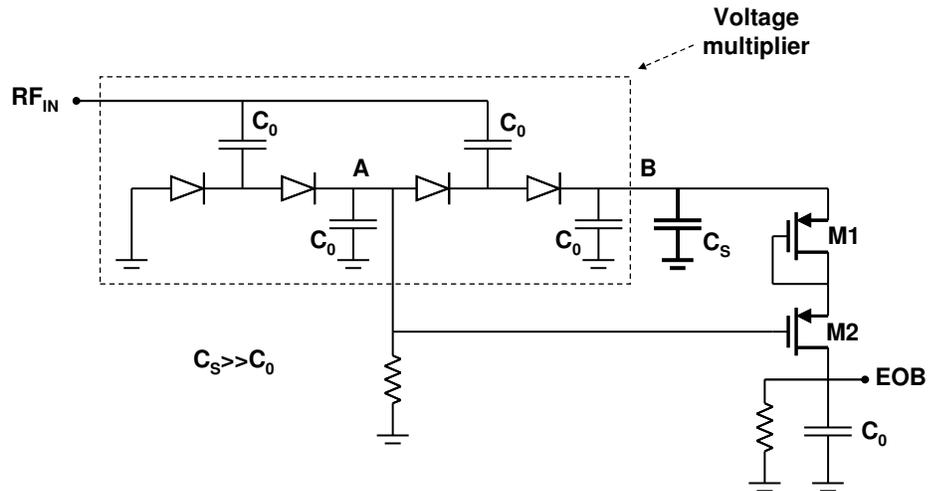


Figure 6-2: End-of-Burst Detector Embedded in the Voltage Multiplier

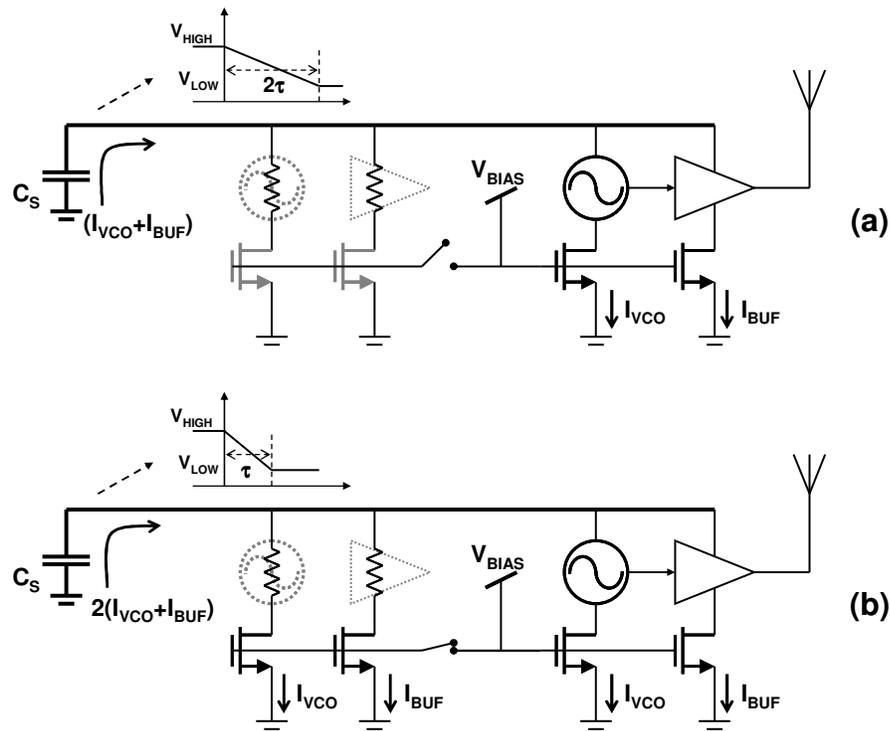


Figure 6-3: Long (a) and Short (b) Pulse Transmission Configuration

6.2.3 Novelty and Contributions to the Field

The integration of the RFID together with the antenna (on the same die or on a silicon backplane) and the storage capacitance is a new accomplishment. The use of mm-wave frequencies allows integrating the antenna, thus reducing the cost and the size of the RFID. The general architecture, including the modulation scheme (pulse-width modulation with bit-by-bit transmission) is novel. The use of a modulation scheme not based on back-scattering relaxes the requirements of the RX section of the interrogator, thus simplifying its architecture and reducing its cost. The EOB detector circuit and the short/long pulse width generation scheme are new. The voltage multiplier uses a novel “floating” bulk-potential diode connected PMOS device architecture, shown in Figure 6-4, to efficiently charge the storage capacitor [43]. The

us of bit-by-bit transmission reduces the size of the storage capacitance, thus allowing its complete integration on the die. The use of a non-coherent pulse-width modulation together with time-division access between the interrogator and the RFID makes the system more insensitive to Doppler effect and multi-path fading. The proposed end-of-burst detector circuit embedded in the voltage multiplier represents almost no area overhead and operates at a very low power, a key-factor in order to maximize the RFID read range. The pulse-width generation scheme is insensitive to PVT, making the system very robust and appropriate for large volume production. As in chapters 4 and 5 the CPGS (conductive path to ground the substrate) techniques was heavily employed to ensure optimal circuit performance by minimizing noise and cross-talk between different functional blocks of the system.

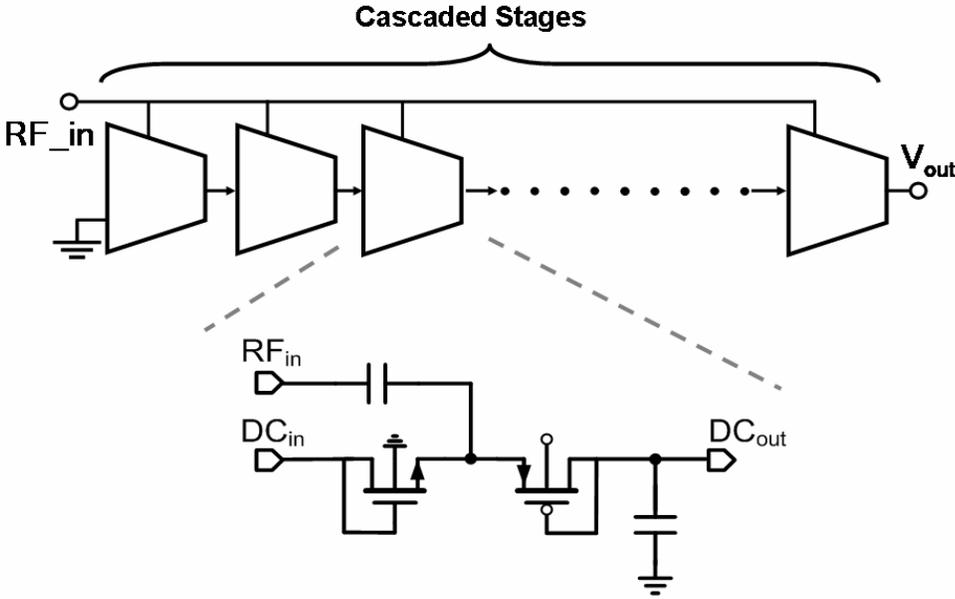


Figure 6-4: Voltage Multiplier with Diode Connected Floating Bulk PMOS

6.3 Design and Layout Details

6.3.1 Storage Capacitor and Coplanar Waveguide Ground Plane

On chip passives generally consume the largest area in micro and mm-Wave designs. Efforts to reduce the size of passives and efficiently use the area they demand are critical. As described in chapter 2, the substrate and bulk potential must be controlled between different functional blocks so that active devices do not experience the ill-effects of noise, cross talk and substrate bounce. The storage capacitor and coplanar waveguide (CPW) ground plane in this application are exceptionally larger than any other component in this RFID Tag. Figure 6-5 is a die photo of the 24 GHz Tag which shows the majority of the chip area covered by the storage capacitor and the ground plane in between signal lines.

In order to obtain a very high density capacitor, a multilayered design was employed which stacked and combined MOS (metal oxide semiconductor), Metal Finger, and MIM (metal insulator metal) capacitors. The capacitor is able to achieve a density of over $2 \text{ fF}/\mu^2$, with an overall storage capacitance of more than 500 pF. The ground side of the storage capacitor contains the base layers and substrate contacts needed to control the bulk potential. The CPW ground plane is employed by simply shorting both sides of the storage capacitor to ground and removing the insulator layer. This ensures that the overall design would be uniform in density and maximize yields. The CPW traces were EM simulated with the grounded storage cap style ground plane to ensure performance quality of the transmission line structures.

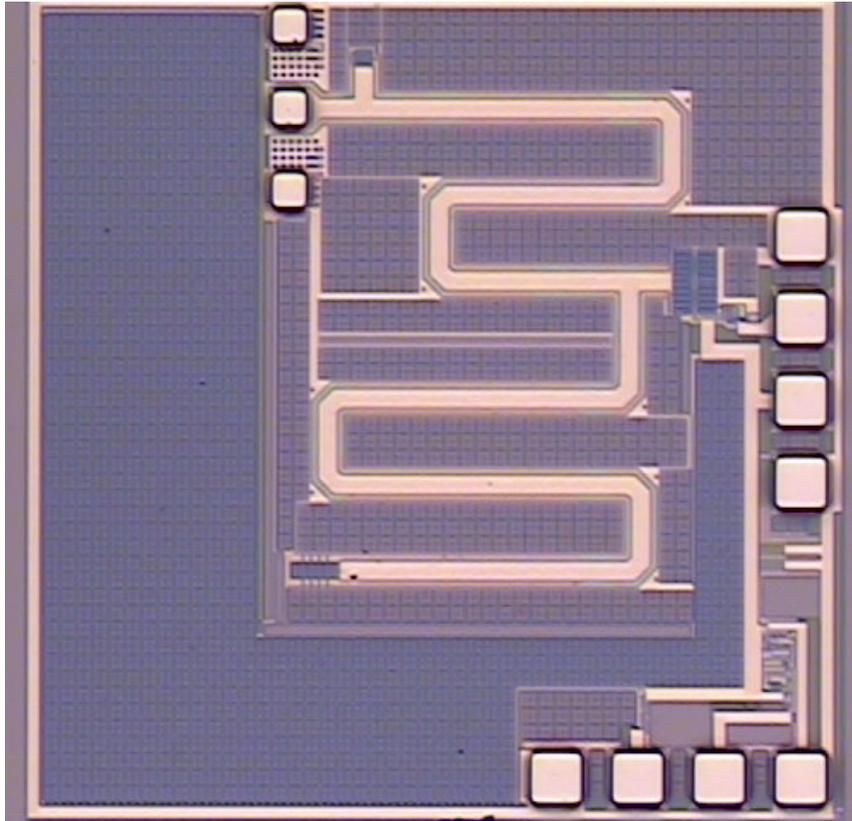


Figure 6-5: 24 GHz RFID Receiver Tag Die Photo

6.3.2 Analog Control Logic

In order for the RFID Tag to function properly a few control logic signals had to be implemented. The Tag must be able to discern when it is or isn't receiving RF energy, when it has received enough energy to transmit a message, when it must cease transmission and the difference between harvesting energy for the first time or not; all while consuming very little (micro watts) to no power at all. This is a difficult task that becomes increasingly complex with added features/functionality of the Tag. Hysteresis and volatile memory effect techniques must be employed to in order to implement some of the required analog control logic. Figures 6-6, 6-7 and 6-8 illustrate some of the measured analog control logic signals.

6.4 Experimental Results

At the time of completion of this dissertation, measurements were only taken for the receiver portion of the RFID Tag. This is the more significant portion of the overall system because it contains all of the novel circuits and design techniques, while the transmitter portion “safely” utilizes circuits (i.e. VCO, PA and matching network) and proven methodologies commonly known in RF circuit design.

Figure 6-6 illustrates the charging (energy harvesting with incoming RF signal) mode control signals of the Tag. The Enable signal triggers high when enough energy is gathered on the storage cap and the EOB (end-of-burst) signal remains low.

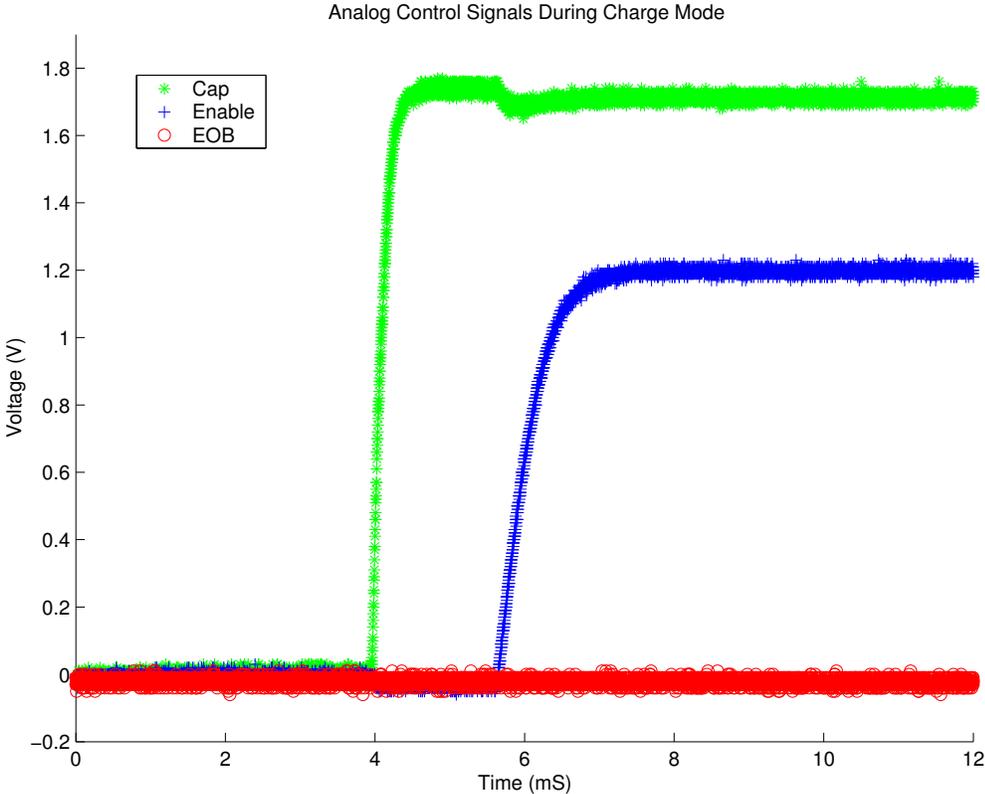


Figure 6-6: Charging Mode Control Signals

Figure 6-7 illustrates the control signals as the Tag transitions into the discharging (transmitter enabled with no incoming RF signal) mode. The Enable signal triggers low when the voltage on the storage cap falls to 1 volt. As the incoming RF signal ceases, the EOB (end-of-burst) signal remains triggers high.

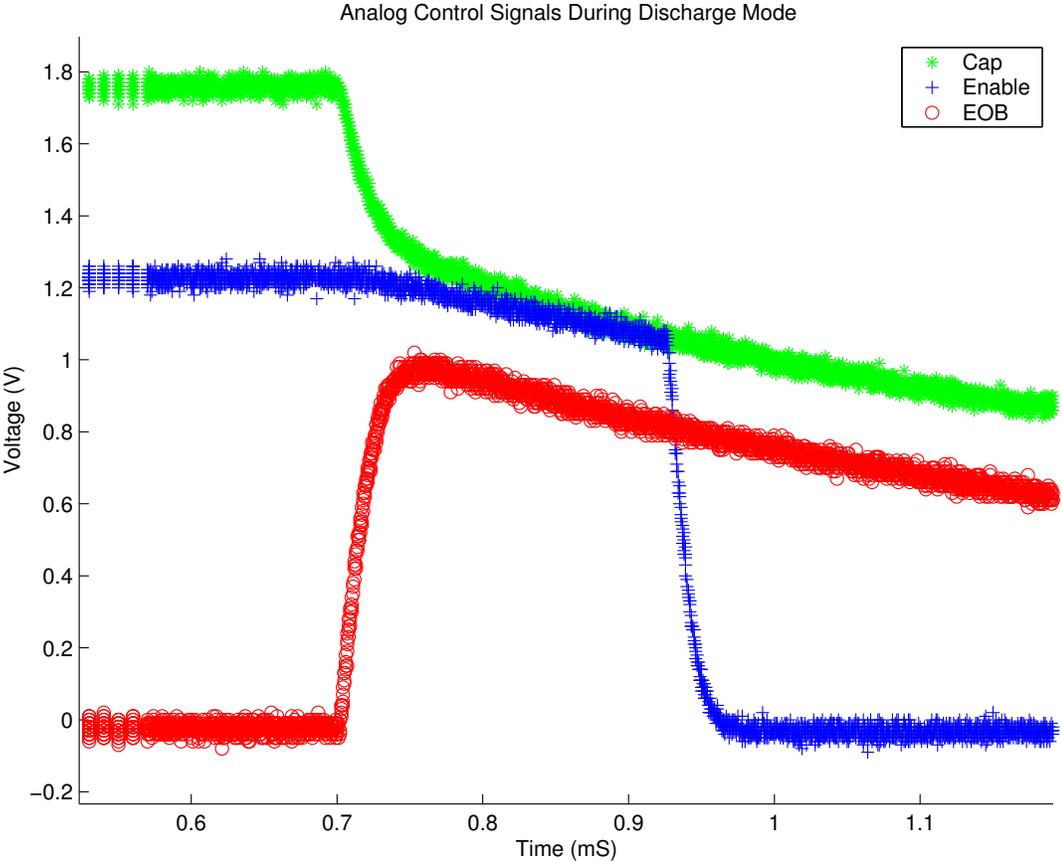


Figure 6-7: Charging Mode Control Signals

Figure 6-8 illustrates the hysteresis effect on the Enable control signal as the Tag transitions back and forth from the charging mode into the mode. The Enable signal triggers high once 1.8 volts is stored and triggers low when the voltage on the storage cap falls to 1 volt.

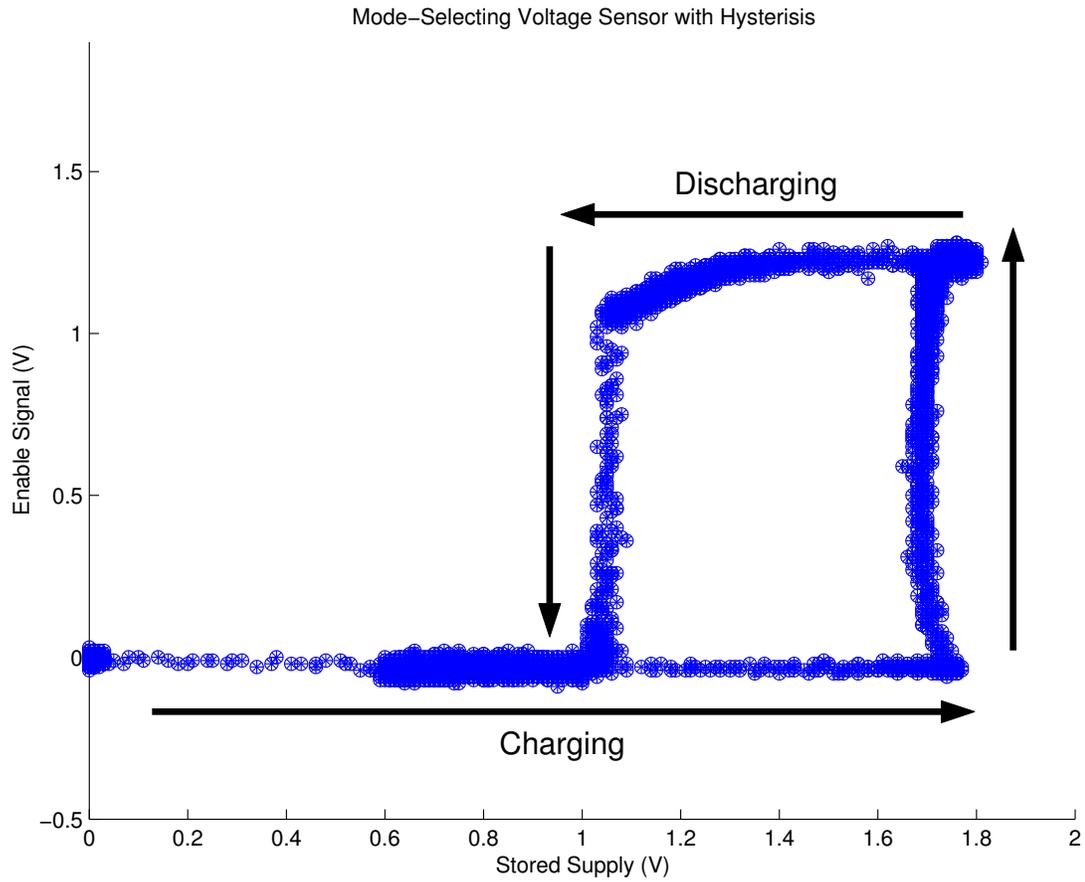


Figure 6-8: Hysteresis on Enable Control Signal

Figure 6-9 illustrates the required RF input power to reach 1.8 volts on the storage capacitor using different output loads. This gives a measure of the sensitivity of the RFID Tag at 24 GHz. Figure 6-10 illustrates the harvested energy at different output loads as a function of frequency.

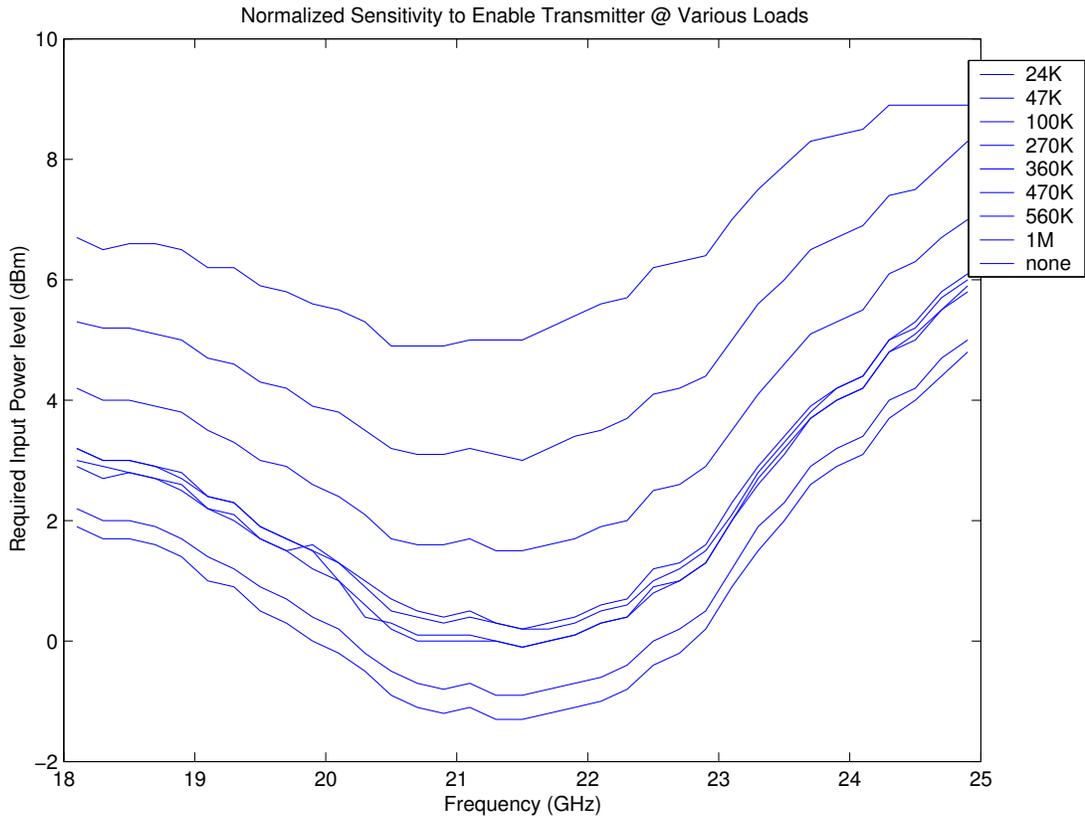


Figure 6-9: Required RF Input Power to Trigger Transmission From Tag

6.5 Summary

This chapter proposed an invention of a RFID architecture, circuit design and modulation scheme that allows operation in the license-free millimeter-wave band around 60GHz on a low-cost deeply scaled (90 or 65 nm) CMOS process. At these frequencies (24 or 60 GHz) the physical size of a high-efficiency antenna can be shrunk to a few millimeters. The antenna can now be integrated with the whole RFID (or on silicon backplane), further reducing its size. Cost is also reduced due to no assembly required. The proposed architecture can be used to build fully-integrated RFID at mm-wave frequencies (e.g. 60GHz or 24GHz) using low-cost deeply scaled

CMOS process. The integration of the antenna further reduces the cost and the overall size of the RFID. The adopted modulation scheme simplifies the interrogator architecture, reducing the cost of the overall system (RFID + interrogator).

The invention can also be used in biomedical applications, e.g. communication between an implanted sensor and an external interrogator. Very high frequency (e.g. 60GHz) would reduce the size of the implanted device which is a key requirement in this application. This is an area where the world might have a lot of interest in this work in the immediate future due to increased involvement in digital health [40].

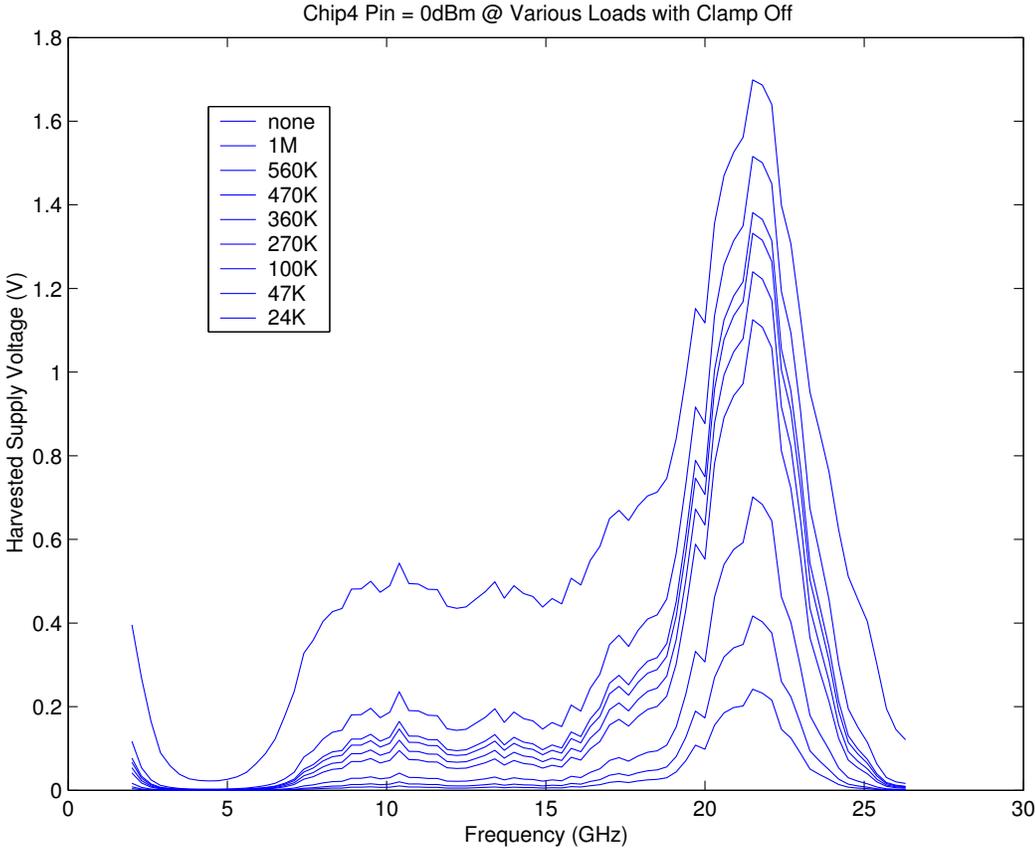


Figure 6-10: harvested energy at different output loads

Chapter 7: Conclusion

7.1 Summary of this Work

A comprehensive design approach for implementing micro & millimeter wave wireless transceiver front-end circuits was proposed. It encompasses a wide range of issues related to active and passive elements in silicon based circuits. All design aspects including modeling and simulation were considered for maximum accuracy and reliability. The new design approach promotes circuit optimization and results in very robust and reliable radio frequency design applications on silicon.

Many of the techniques employed are intended to combat the limitations of the silicon substrate; even beyond the frequency limitations of the devices, and towards overcoming and in some cases exploiting the parasitic effects of interconnect wiring at increased frequencies. In this discussion the most substantial work was performed on the design and characterization of a variety of low noise amplifiers (LNAs). Due to the outstanding performance compared with other state-of-the-art implementations, a new figure-of-merit (FOM) equation was proposed. Other successful demonstrations of transceiver circuits are also covered such as a direct down converter featuring an active balun at 94 GHz, and radio frequency identification (RFID) tags with an active transmitter at 24 GHz and 60 GHz.

7.2 Future Work

The main purpose of this work was to demonstrate an effective integrated approach to designing micro and millimeter wave range transceiver front-end circuits in CMOS SiGe BiCMOS technology. In developing the work covered in this dissertation certain innovations were discovered (i.e. unilateral and current gain

peaking in SiGe, and floating bulk MOS properties). Future effort should be devoted into exploring the maximum potential of these discoveries. Also, efforts should be and are currently being made into more fully integrated wireless systems in the mm-Wave range. A complete transceiver system designed under the same philosophy that interfaces with digital blocks on or off-chip and transmits and receives information would be the ultimate goal of this research and will undoubtedly demonstrate the validity of the novel design techniques discussed in this dissertation.

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