Sputtered AlN
as Hard Mask for GaN Etching and Selective Area Regrowth
and as High-k Gate Dielectric for MOS Devices

A Thesis

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Master of Science

by

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ABSTRACT

AlN recently gained much attention for its potential applications in semiconductor power devices. Sputtered AlN can be an alternative to the conventional SiO_2 hard mask. For GaN etching and regrowth, the use of AlN hard mask can eliminate the possibility of Si and O elements acting as shallow donors to the regrown GaN. In this work, deposition, patterning and etching of AlN are explored to examine its potential as a good hard mask that has near-vertical and smooth sidewall profiles. In addition, AlN with wide energy bandgap of 6.2 eV confers its electrical isolation properties for high breakdown field; combined with its high dielectric constant up to 8.5, AlN can be used as a high-k dielectric material for MOS device applications. In this work, metal-insulator-semiconductor (MIS) capacitors are fabricated, the dielectric constant and breakdown field of sputtered AlN are determined as ~6.7 and ~4.3 MV/cm by C-V and I-V measurements. Time-dependent dielectric breakdown (TDDB) behaviors of sputtered AlN in MIS capacitors are also evaluated for understanding the dielectric breakdown mechanism and reliability under long-term electrical stress.

BIOGRAPHICAL SKETCH

Anni Wu studied Materials Science and Engineering at University of Washington in Seattle for her undergraduate degree. During her senior year of undergraduate, she was working at Siemens Healthineer. She worked on material processing and acoustic properties characterization for Ultrasound Transducer materials, including RTV silicone lens material, polyurethane matching layer material and AlN composite backing material.

After finishing her Bachelor's degree, Anni came to Cornell University to continue her study in Materials Science and Engineering for a Master of Science degree. She worked under Professor Debdeep Jena and Professor Grace Xing on GaN based power devices. Anni will finish her Master thesis by August 2019.

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CHAPTER 1

Introduction

Semiconductor technology plays an important role in many electronics that support our social infrastructure and everyday life. Semiconductors become essential for innumerable digital consumer products to produce, store, and transform information. Semiconductors were discovered back in the 19th century; starting with Si and Ge as the most commonly known semiconductor elemental materials, the technology was expended into a variety of compound semiconductors such as GaAs, InP, GaN, Ga_2O_3 among many others[1,2]. In 1947, the developments in quantum physics led to the invention of semiconductor transistors, which had become the fundamental building block of modern electronic devices and integrated cirtuit[3]. Along with the rapid development of semiconductor technology, Moore's law solidifies as the golden rule for the electronics industry, stating that the number of transistors in an integrated circuits doubles every two years[4]. Moore's prediction describes a driving force for our "information age", and that data are produced in phenomenally growing volumes and transported at ultra-high speeds.

One of the most important demands of scaling resulting from Moore's law is the advancement in nanofabrication technology. For many device fabrication processes, the conventional polymeric photoresist mask is not suitable, primarily due to its low etching selectivity to poly-Si and the ease of degradation during plasma etching[5]. Therefore, a hard mask such as oxide or nitride is urgently required to overcome these challenges. In addition, as the scaling of the device approaches its limitation caused by the high tunneling leakage current at dielectric

thicknesses below 1 nm, alternative high dielectric constant (high-k) materials are pursued in the need to replace conventional poly-Si or SiO_2 as the gate dielectric[6]. Aluminum Nitride (AlN) is a III-V semiconductor with a high dielectric constant up to 8.5, which makes it attractive for high-k dielectric application[7]. Also, for GaN-based power devices, AlN can be a favorable material in terms of better control at the interface between nitrides. This work will focus on this material for its potential usage as a hard mask as well as a high-k gate dielectric for power electronic devices.

1.1 Sputtered AlN

Aluminum nitride (AlN) is an III-nitride compound that has been investigated for many microelectronic applications due to its unique physical properties. AlN has hexagonal closed packed wurtzite structure[8]; therefore, its piezoelectric and dielectric properties due to the non-centrosymmetric crystal structure has been widely utilized in micro-electromechanical systems (MEMS) such as ultrasound transducers, resonators, and energy harvesting devices[9-12]. The wide bandgap energy (6.2 eV) and good compatibility with designs on semiconductor materials of AlN also enable applications in high-frequency communications and power semiconductor devices[13,14]. AlN thin films can be produced via various deposition methods, including molecular beam epitaxy (MBE)[15], metal organic chemical vapor deposition (MOCVD)[16], pulsed laser deposition (PLD)[17], atomic layer deposition (ALD)[18], and reactive sputtering[19,20]. Among these deposition methods, sputtered AlN has attracted attention due to its simplicity, ease of parameter control, low deposition temperature, and cost-effectiveness[21].

In addition to the applications of AlN in MEMS and high-frequency devices as mentioned above, AlN also has several important properties that allow its potential usage in power electronics processing and structures. As GaN-based power devices are greatly explored for its potential to

exceed Si, GaAs, and SiC[22], the compatibility of materials that are involved with the device construction with GaN is also a determining factor for successful integration into advanced devices. First of all, as a nitride compound, AlN is able to provide a stable interface with the GaN substrate. Secondly, AlN displays excellent thermal stability, which enables thermal processing steps up to its melting point (~ 2100 °C) in device fabrication[23]. Also, the large energy band gap (6.2eV) of AlN confers excellent electrical isolation properties of this material` for a high breakdown field needed to reduce the tunneling current flowing through the gate insulator[23]. Combined with its high dielectric constant up to 8.5, AlN becomes an excellent material for high-k dielectric power devices while overcoming the challenges associated with high gate oxide leakage current due to scaling[7].

1.2 This work

Silicon dioxide (SiO_2) has been widely utilized as hard masks for patterning semiconductor devices. However, during the fabrication process of GaN epitaxial regrowth, the Si or O element from the SiO_2 may contaminate the GaN regrowth junction interface and subsequent regrown GaN by acting as shallow donors. In this work, novel nitride masks for GaN etching and selective regrowth have been investigated to eliminate the above issue. It is highly desired in many processes that the hard mask can be completely removed in a later processing step. For this reason, amorphous AlN is preferred over crystalline or polycrystalline AlN since amorphous AlN can be readily etched in base solutions. AlN deposited by reactive sputtering with Al target source and N_2 gas can be a good candidate for this application. The deposition condition of sputtered AlN is studied and the potential of AlN film to act as a good etch or regrowth mask is explored in Chapter 2.

Responding to the rapid growth of semiconductor technology towards higher device densities and faster speed, the transistor dimensions in integrated circuits are scaling down. In order to achieve high transistor speed with minimum power consumption, the transistor drive current can be raised by increasing the amount of charge in the transistor channel, which is controlled by the gate capacitance[24]. A high gate capacitance can be achieved by decreasing the gate oxide thickness t or having high-k dielectric materials ($C_{ox} \propto k/t$). As the gate oxide scaling has been considered a limiter for thickness below 2 nm[25], where further reduction in gate oxide thickness results in high leakage current leading to high power consumption, high-k dielectrics are extensively studied to increase the gate capacitance and hereby the drive current[26,27]. In this work, the dielectric constant, as well as electrical breakdown field, are evaluated for sputtered AlN through measuring the C-V and I-V characteristics of the metal-insulator-semiconductor (MIS) capacitors. The properties are also compared with PECVD SiN_x and ALD Al_2O_3 in MIS structures, which will be discussed in Chapter 3.

Time-dependent dielectric breakdown (TDDB) is one of the most important reliability concerns in MOS integrated circuits[28-30]. In Chapter 4, the TDDB behaviors are evaluated for sputtered AlN in MIS capacitors, and also compared with ALD Al_2O_3. The devices are stressed under constant voltage (i.e. electric field E) below the critical breakdown potential and the times to failure (t_{BD}) are recorded, which can be described in a Weibull statistical distribution. According to the thermodynamic model, where $\log(t_{BD})$ is proportional to E, the device lifetime under low stressing voltage can be extrapolated from this relationship[31,32].

1.3 Related research

Reactive sputtering of AlN has been extensively researched for microelectronic applications. Many works published the effect of sputtering parameters such as power, substrate temperature, pressure, and nitrogen gas flow on AlN film quality. Among many research studies, Ohtsuka et al. investigated the effect of sputtering pressure from 3 to 11 Torr on AlN crystalline quality and residual stress, using pulsed DC magnetron sputtering on sapphire substrate under the conditions of 800 W, 550°C, 50% N_2 gas concentration, and reported the crystalline quality of AlN films was improved by deposition with lower sputtering pressure[33]. Wang et al. studied on the effects of substrate temperature and bias voltage on crystal orientation, using DC magnetron sputtering under 170 W, 9 mTorr, and 15% N_2 gas concentration of total 35 sccm flow, and found that the crystalline quality of the films improves to be highly c-axis oriented as the substrate temperature increased to 300°C, and the deposition rate enhances when the negative bias voltage was applied[34]. Jiao et al. investigated the effect of RF power and gas flow on residual stress and film quality, using RF magnetron sputtering under 25°C, 5 mTorr with varied power and N_2 gas concentration, and reported that [5] Stan et al. investigated electric and pyroelectric properties of deposited films, using RF magnetron sputtering on Si substrate at 50°C, 1.5 mTorr, and 25% N_2 gas concentration of total 40 sccm flow[36]. Sputtered AlN hard mask has been investigated for selectivity etching of materials such as SiO_2 and SiC, but not yet for GaN[37,38]. Professor Grace Xing has used sputtered AlN as a regrowth hard mask in her PhD work to fabricate GaN HBTs, though this process is not published. Studies have shown that AlN thin films deposited by sputtering can be etched in hot phosphoric acid at 60°C, and other etchants such as hot HF/H_2O, HF/HNO_3, NaOH, KOH, and AZ 400K photoresist developer[39-44]. The wet etching studies with ensure good removal of the AlN mask.

As sputtered AlN appears favorable as a potential replacement for SiO_2 as a high-k gate dielectric material, the dielectric permittivity and breakdown potential of sputtered AlN are extensively studied. These properties are reported to be closely related to the film quality of the film, which is affected by deposition conditions. Adam et al. studied on the electrical properties of MIS capacitors with AlN gate dielectrics using reactive magnetron sputtering under the conditions of room-temperature using powers of 50 and 100 W with 5 mT of 15% argon and 85% nitrogen. Adam reported that the dielectric permittivity varies between 4-11 and breakdown field is between 4-12 MV/cm, which AlN film sputtered at lower powers has higher dielectric constant and breakdown field, and thermal annealing can further increase the values[45]. Ramadan et. al reported the dielectric constant of c-axis oriented AlN to be 8.7-8.9 using reactive DC sputtering at room temperature at 200–300 W, 1 mTorr, and under 2:1 Ar/N_2 flow ratio, which indicates a higher dielectric constant value for high-quality film[46]. The time-dependent dielectric breakdown behavior of sputtered AlN has not yet been studied, but it shares a very similar breakdown mechanism with dielectric materials such as SiO_2. McPherson reported a comprehensive review of time-dependent dielectric breakdown (TDDB) physics and models based on SiO_2[47]. Many other researchers also investigated the TDDB behavior of SiO_2 and provided plots of Weibull statistical distribution in a wide electric field range[48-51].

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CHAPTER 2

Sputtered AlN as Hard Mask for GaN Etching and Selective Area Regrowth

The rapid progress in high drive current and high-speed field-effect transistors has been driven by many research studies. Among different device structures, junction gate field-effect transistor (JFET) has brought great attention due to its unique advantages in many aspects, such as low noise, high input impedance, low power consumption, small cell pitch that creates low specific on-state resistance and high saturation current densities, and the elimination of threshold instability due to the traps at the oxide interface[1-3]. This also requires development in device patterning technology to fulfill the processing needs. For many device fabrication processes, the conventional polymeric photoresist mask is not suitable because of its ease of degradation during fluorine or chlorine-based plasma etching[4]. Therefore, a hard mask is required to overcome the challenge. Silicon dioxide (SiO_2) is considered as one of the most commonly used hard mask for fabrication; however, it has its limitation of containing elements that can act as shallow donor to GaN-based devices. In this study, the development of a novel nitride mask is motivated to support the fabrication need of GaN channel etching and regrowth for a vertical junction gate field-effect transistor design.

JFET is one of the most mature switch concepts in SiC[3,5,6]. In comparison, GaN also hold great promises as a semiconductor material for JFET structure due to its superior material properties. In terms of the basic material requirement for power devices, it is desirable for the semiconductor to have high charge, breakdown field, electron or hole velocity, and thermal conductivity. With a wide bandgap of 3.4 eV, GaN promises power transistors with excellent

characteristics of dielectric constant of 9.0, intrinsic electron mobility of 1200 cm^2/Vs, and a breakdown electric field of 3.3 MV/cm, which provides much greater Baliga's figure of merit (BFOM) than many other semiconductors[7,8]. High drive current can be achieved by limiting the on-resistance (R_{ON}), which is inversely proportional to the relative dielectric constant, electron mobility, breakdown field. The theoretical limits of on-resistances as a function of breakdown voltage for GaN and comparative semiconductors in Fig. 2.1 suggests that the on-resistance of GaN devices can be much lower than those of Si, GaAs, SiC devices at the same breakdown voltage[9].

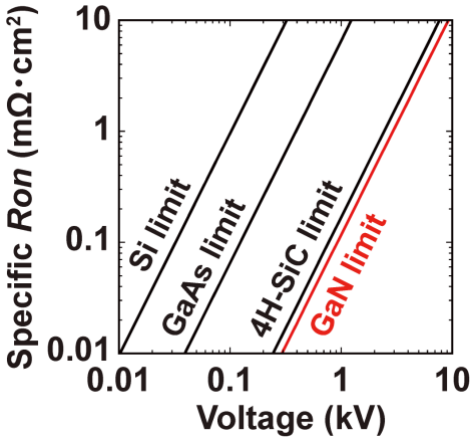

Figure 2.1: Benchmarking the theoretical ideal performance limits of GaN power devices against other semiconductors [ref.9]

With these attractive attributes in terms of the performance prospect of GaN power devices, GaN-based VJFET has been designed and explored in the Jena-Xing group. (Figure 2.2) In this device, heavily doped p-GaN is used to create a large depletion region in the n-GaN channel, therefore to achieve normally-off. Since GaN has a wide band gap, the large intrinsic build-in potential further assists the normally-off attribute. By applying the negative gate bias, the device can be turned on for carriers transporting through the channel region.

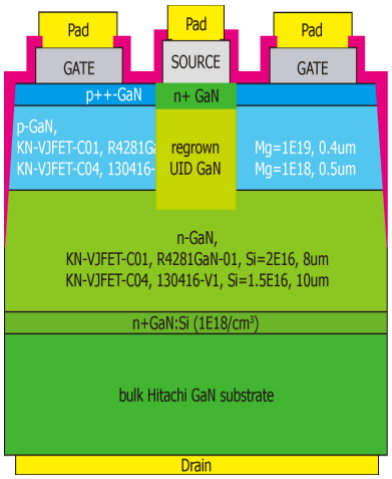

Figure 2.2: Schematic cross-section of GaN VJFET device (by Dr. K Nomoto, Jena-Xing group)

One fabrication challenge is the selective area doping in the lateral and buried p-n junctions. Due to immature implantation technology in GaN, regrowth is often employed to realize ohmic contact or lateral junctions. For selective area regrowth, GaN can be regrown in the interested area, and the rest of the area should be covered by the mask.

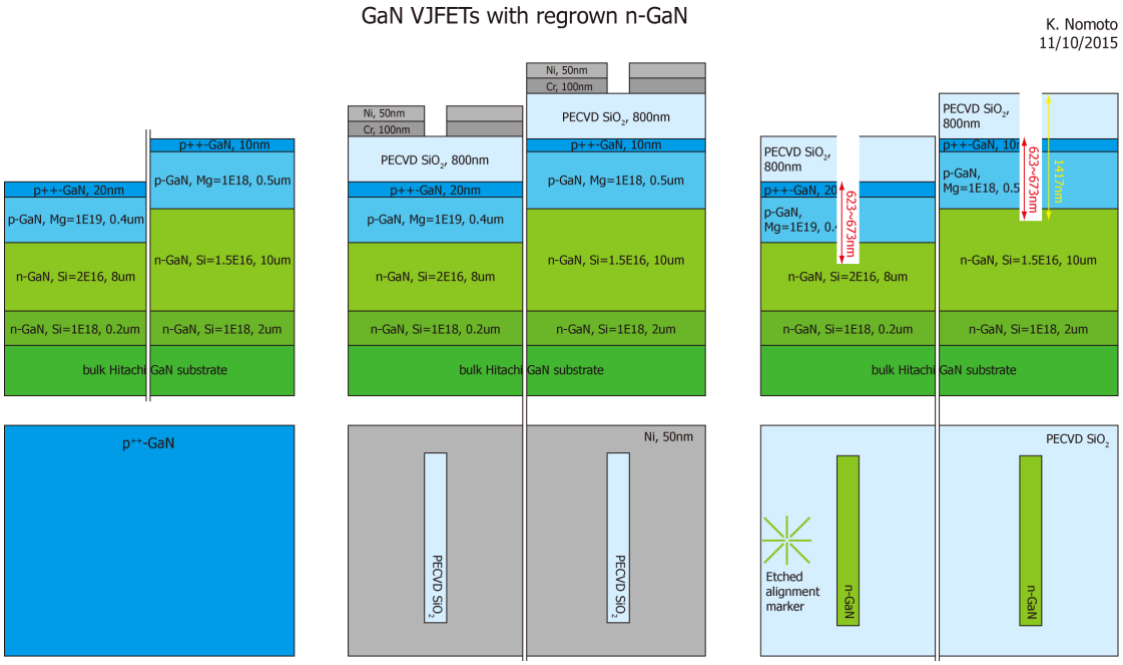

Figure 2.3: Process flow of GaN VJFET (by Dr. K Nomoto, Jena-Xing group)

The device fabrication process flow is described as Figure 2.3 shown above. N-GaN and p-GaN are grown by molecular beam epitaxy (MBE). PECVD SiO_2 and Cr-Ni hard masks are used for GaN etching and regrowth. For GaN-based electronic devices, SiO_2 is commonly used as the hard mask for GaN etching and regrowth. However, for this fabrication design of GaN VJFET, it is preferable that the hard mask does not contain Si and O, which may contaminate the regrowth junction interface by acting as shallow donors. Therefore, nitride mask such as AlN is considered as a candidate for GaN etching and selective area regrowth. The expected features of hard mask for the above GaN VJFET fabrication are 1) near-vertical edge profile 2) smooth sidewall and grass-free 3) easy to remove after regrowth 4) good thermal stability to withstand the high temperature during epitaxial regrowth. In this project, deposition, patterning, and etching of AlN, and the potential for material to act as good etch or regrowth mask are explored.

2.1 AlN Reactive Sputtering Deposition Conditions

AlN thin films deposition can be done by numbers of chemical vapor depositions (CVD) physical vapor depositions (PVD) techniques, including molecular beam epitaxy (MBE), metal organic chemical vapor deposition (MOCVD), pulsed laser deposition (PLD), atomic layer deposition (ALD), and DC or RF reactive sputtering.10) For GaN electronic devices, the electrical performance is very sensitive to surface damage. For hard masks deposited by plasma-based deposition techniques, it is important to lower the plasma power to ensure low damage to the GaN epitaxial surface. Atomic layer deposition (ALD) is another interesting choice – AlN can be deposited at low temperatures using a N-plasma source. However, the ALD deposition rate is too low to be economical for our purpose (200 nm of regrowth mask will require 20+ hours). Currently

at Cornell, there is no other CVD system suitable to deposit AlN. Therefore, sputtered AlN is explored as a choice of hard mask material.

Sputtering is a technique used to deposit thin film by plasma bombardment. The system consists of a chamber, gas inlets, vacuum pumps, plasma sources and power supply. The energetic particles (Ar+) bombard off the target material into the plasma region that is maintained by DC or RF electromagnetic field, and the ejected ions will travel through the plasma region to be deposited onto the wafer substrate. The AlN film is deposited by the AJA Sputter Deposition tool at CNF, which is a cryo-pumped sputtering system allowing deposition of a variety of metals and dielectrics. A cryopump traps gases and vapors by condensing them on a cold surface and maintains the high vacuum condition of 3 mTorr in the chamber. The power supply provides a DC power of 400 W. Higher sputtering power indicates higher kinetic energy being supplied to the ions; therefore, this study employs a fairly low deposition power to achieve amorphous AlN film. The substrate chuck is maintained at a consistent temperature of 300^{o}C. The inlet feeds Ar and N_2 gasses and subsequently excited into plasma; by reacting with the Al ions ejected from the target source, the Al and N ions merge to create an AlN compound. CNF AJA operating menu suggested a plot of deposition rate with respect to the Ar and N_2 flow ratio. (Figure 2.4) The total gas flow is kept at 30 sccm. There is an inverse relationship between the deposition rate and N_2 flow, which is due to a lower momentum transferred to the target atoms with a decreasing amount of the Ar flow, and also partly due to AlN formation on the Al target. High Ar flow ratio (N_2 less than 8 ccm) can sputter higher amount of Al, and result in Al-rich AlNx film. Therefore, 15 sccm:15sccm N_2 to Ar ratio is used for the deposition in this study. The deposition rate is around 2.2 nm/min. The deposited film is characterized by X-ray diffraction (XRD) to determine the thin film orientation and film structure.

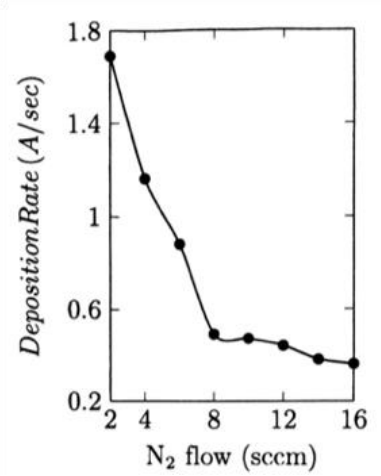

Figure 2.4: Sputtered AlN deposition rate vs. N_2 flow with a fixed total gas flow of 30 sccm (CNF AJA Sputtering Tool)

2.2 Sputtered AlN Film Structure Characterization

X-ray diffraction (XRD) is used to characterize the film structure of the sputtered AlN. Figure 2.5 shows the XRD pattern of 530 nm AlN film deposited on (001) Si substrate, and the film thickness is measured by ellipsometry. The diffraction peaks are observed at 2θ=32.96 and 68.15, which corresponds to (002) Si and (004) Si. The presence of broad hump at low diffraction angles indicates an amorphous crystalline feature of the sputtered AlN. The AlN film is annealed in the furnace at 800°C for 30 min to simulate GaN MBE regrowth condition. Figure 2.6 shows that the (002) Si and (004) Si peaks at 2θ=32.96 and 68.15 are observed again, while no sharp diffraction peaks correspond to AlN crystal planes. After annealing, some small peaks appear at the low angle hump region, which can be an indication of that the amorphous film quality has been improved by forming crystal domains. In future study, pole figure XRD need to be measured for more accurate analysis and explanation of the film structure. XRD phi scan of four peaks separated by 90 degrees confirms that the peaks at 69 degrees belong to the cubic structure of Si substrate. (Figure 2.7)

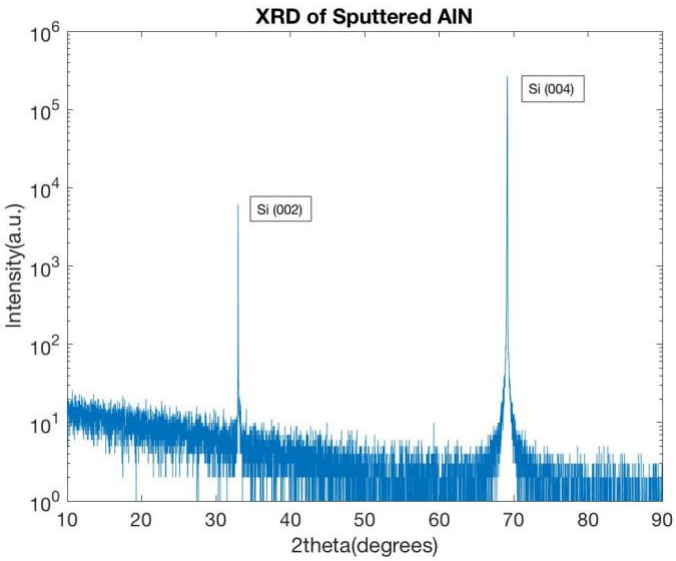

Figure 2.5: 2theta-omega XRD scan of sputtered AlN

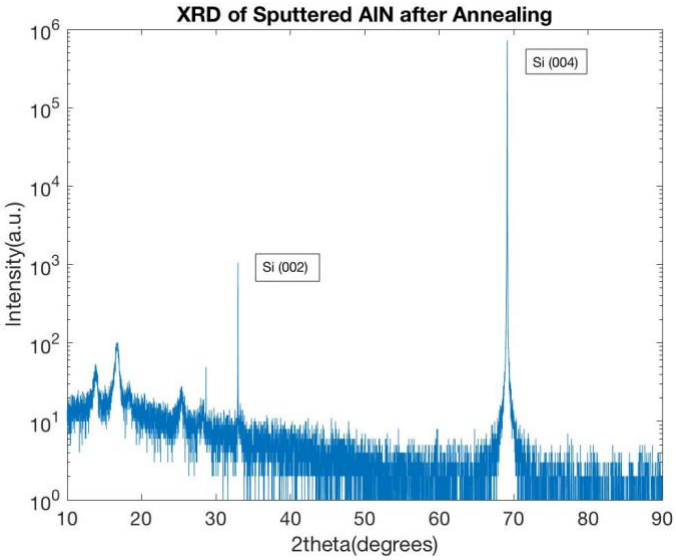

Figure 2.6: 2theta-omega XRD scan of sputtered AlN after annealing

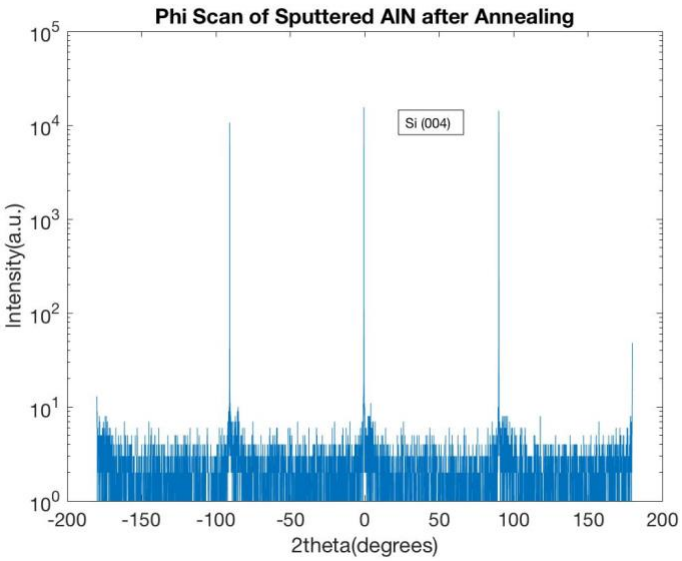

Figure 2.7: Phi XRD scan of sputtered AlN after annealing

In this study, amorphous AlN film is preferred because the hard mask is expected to be easily removed by etching after the GaN regrowth processes. For future study, the AlN film quality can be improved for other application by manipulating the sputtering parameters such as sputtering pressure, power, substrate temperature, and N_2 to Ar ratio. According to the kinetic theory, lower pressure can promote adatoms with faster mobility, and hereby to induce high growth of crystalline material. Many research reported the formation of c-axis sputtered AlN films by lowering the process pressure[11-13]. A higher sputtering power ranges from 100 W to 2000 W can also enhance the kinetic energies being supplied to the ions. Research demonstrated high crystal-quality sputtered AlN film by using high deposition power at low deposition pressure[12, 14, 15]. However, high power can also have a destructive effect on the film quality by creating secondary atoms due to the increase in the kinetic energy. In addition, the high substrate temperature can also increase the energy, which helps in depositing the highly c-axis oriented AlN films[16]. Such considerations can be taken into the future experiments to study the effect of sputtering parameters on the AlN

film quality, which can be beneficial for enhancing the dielectric, piezoelectric, and other electrical properties of the material.

2.3 Sputtered AlN Hard Mask Process Flow and SEM Inspection for Sidewall Profile

The fabrication process of GaN VJFET described in Figure 2.8 a,b used SiO_2 as the etching and regrowth hard mask. In this project, sputter AlN is explored for its feasibility to replace SiO_2 as the hard mask. The structure is designed to have a comparable process flow with GaN VJFET. The AlN is sputtered onto the Si substrate using the parameters described in section 2.1. Negative photoresist SPR2020 is spin-coated on the AlN film to pattern the Cr-Ni metal mask at 6000 rpm for 60 seconds. The sample is baked for 1 minute at 100^{o}C before the exposure. The photoresist is exposed under ABM contact aligner for 4.2 seconds using a photomask with 0.5-20 um features (Figure 2.8c). The sample is post-baked for 1 minute at 110^{o}C. The photoresist is then developed using AZ 726 developer for 70 seconds at room temperature, followed by DI water rinse and nitrogen blow. The sample is descumed by a Gen-1000 oxygen plasma source to strip off the residual photoresist material at the conditions of O_2=42 sccm, 20 mTorr, RIE = 100 W for 2 minutes. After photolithography, Cr and Ni are deposited by E-Beam evaporation. Cr and Ni are patterned by the lift-off process using Microposit Remover 1165 for 5 minutes with sonication at room temperature. The photoresist is removed by hot Microposit Remover 1165 at 80^{o}C for 20 minutes. For an anisotropic etch, it is preferred to use dry plasma etching, which creates straight sidewalls in the vertical direction. To pattern the AlN as hard mask, AlN is dry etched by ICP-RIE plasma etching (PT-770), under the conditions of BCl3/Ar/Cl2=10/10/20 sccm, 6 mTorr, RIE/ICP=20/250 W, DC=90 V. The detailed step-by-step fabrication process is listed in the process sheet 1 in the appendix.

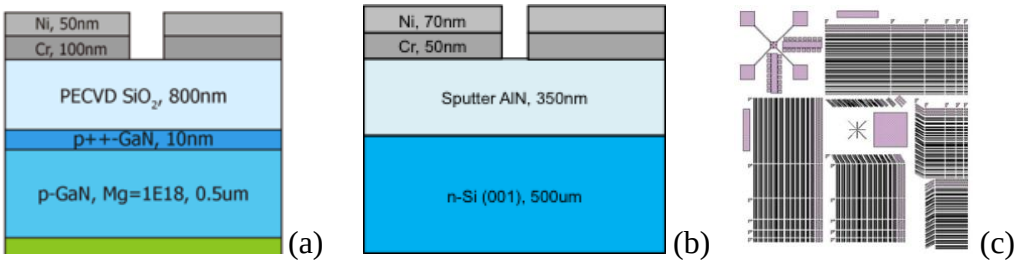

Figure 2.8: (a) Cross section of SiO_2 hard mask on GaN (b) Cross section of AlN hard mask on Si (c) Design of photomask used to pattern Ni/Cr and AlN hard mask for this experiment

Scanning electron microscope (SEM) images are taken to inspect the edge profile of patterned AlN. The sample is cleaved to reveal the cross section and it is observed on the 70-degree tiled sample stage. SEM images in Figure 2.9 indicate near-vertical edge profile and smooth sidewalls of AlN are obtained from ICP dry etching, which are desirable features for etching and regrowth hard mask.

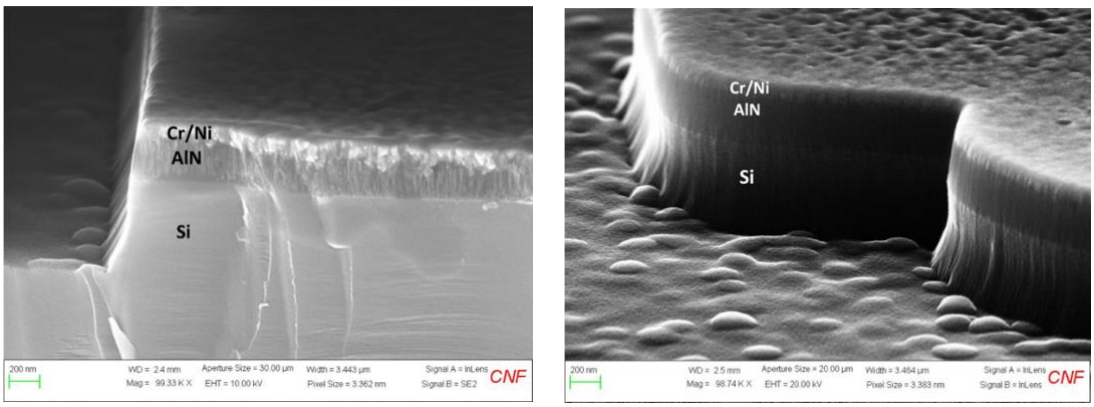

Figure 2.9: SEM images of patterned AlN hard mask on Si

2.4 Sputter AlN Wet Etching for Hard Mask Removal

Wet etching study of the sputtered AlN is performed to ensure mask removal after the GaN regrowth process. The wet etching of AlN involves oxidation of the film surface and subsequent dissolution of the oxides. Wet etching process of AlN contains several chemical and physical steps. First, the etchant is transported towards the AlN for adsorption at the active sites on the surface.

Second, the chemical reaction happens between the oxidizing agent in the etchant and the exposed AlN surface, which produces soluble by-products. Finally, the by-products desorb from the surface and can be dissolved in the solvent such as water. Although the chemical wet etching mechanism of AlN is similar to GaN, low quality amorphous AlN films are more vulnerable to wet etches comparing to MBE epitaxial-grown AlN or GaN; therefore, decent etching selectivity can be achieved during the AlN hard mask removal process. Studies have shown that AlN thin films deposited by sputtering can be etched in hot phosphoric acid at 60°C, and other etchants such as hot HF/H_2O, HF/HNO_3, NaOH, KOH, and AZ 400K photoresist developer[17-22]. In this work, wet etching of sputtered AlN is studied is hot phosphoric acid and KOH.

The experiment setup consists of a beaker with a solution that is submerged in the water bath, a magnetic bar inside the beaker, a hot plate, and a thermometer. The water bath is used for better temperature stabilization. In order to make sure that the chemical reaction is reaction-limited, a magnetic stirrer is used to assist with the diffusion of the reaction products, eliminating the local "loading effect" of the etchant. Incorporating agitation helps with the movement of etchants onto the surface; therefore, uniform and well-controlled etch rate can be determined based on the reaction-limited process. The temperature is controlled using a hot plate, and the temperature is monitored using a thermometer. By having the above setup, the temperature of the chemical solution can be controlled with fluctuation of ± 2°C. The etch rate of sputtered AlN is tested by tracking the etch time and the film thickness using Filmetric. In a fixed composition of etchants, the etch rate is expected to be linear with time if agitation is used. Figure 2.10 shows the plot of AlN film thickness versus wet etching time in KOH and H_3PO_4. The etching rate of sputtered AlN in 50% concentration KOH at room temperature is 33 nm/s, and the etching rate in 80% concentration H_3PO_4 at room temperature is 13 nm/s.

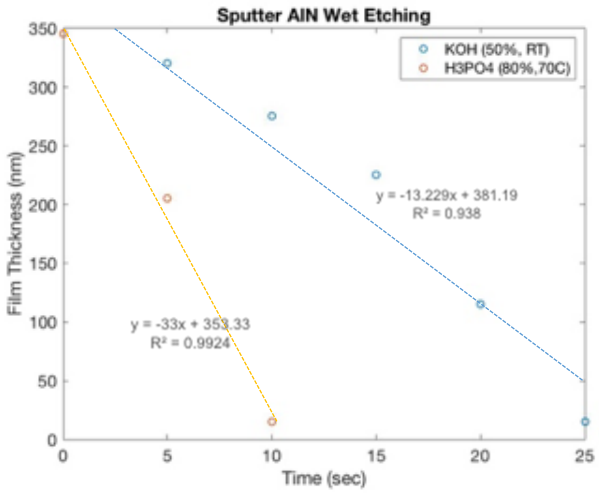

Figure 2.10: Wet etching for sputtered AlN in KOH and H_3PO_4

Wet etching of annealed sputter AlN (800°C for 30 min) is also studied since the AlN hard mask will be removed after the regrowth process. The annealed AlN film is etched in 70°C hot phosphoric acid, and the etch rate drops significantly, indicating a higher crystal quality after a high temperature anneal. Figure 2.11 shows the plot of annealed AlN film thickness versus wet etching time in H_3PO_4 at 70°C and 80°C. The etching rate of annealed AlN in 70°C H_3PO_4 has reduced to 0.69 nm/s. Increasing the H_3PO_4 solution temperature to 80°C improves the etching rate to 5.81 nm/s.

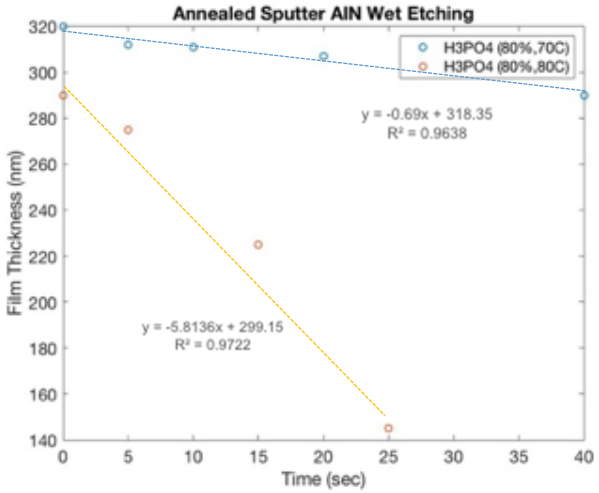

Figure 2.11: Wet etching for sputtered AlN in KOH and H_3PO_4

The grain sizes of as-deposited AlN and annealed AlN are compared using AFM as shown in the Figure 2.12. Both XRD and AFM measurements suggest that the grain size of AlN increases after annealing, which explains that the decrease in etch rate is caused by the change in crystal quality.

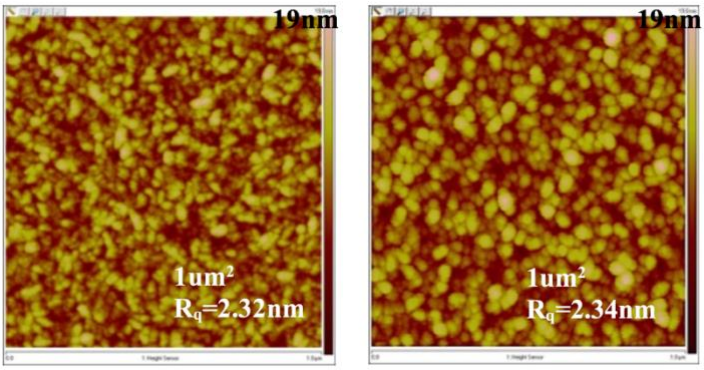

Figure 2.12 AFM image of as-deposited sputtered AlN (left) and annealed AlN (right)

The wet etching rate for both as-deposited sputtered AlN and annealed AlN are summarized in the table below. Although the etch rate is a relatively rough estimate, the study promises decent etching for the AlN hard mask removal.

Wet Etching	**KOH (50%, RT)**	**H_3PO_4 (80%,70C)**	**H_3PO_4 (80%,80C)**
Sputter AlN	**33nm/s**	**13nm/s**	**/**
Sputter AlN after annealing	**/**	**0.69nm/s**	**5.81nm/s**

As discussed at the beginning of the section, the requirements of a good hard mask for GaN etching and regrowth are 1) near-vertical edge profile 2) smooth sidewall and grass-free 3) easy to remove after regrowth 4) good thermal stability. The SEM images present satisfaction of the first two requirements, where sputtered AlN mask enables close-to-vertical edge profile and smooth sidewalls. The wet etching study indicates the removal feasibility of the mask. For future work,

the same process should be performed on GaN to observe the surface morphology of GaN after the mask removal. Based on this work, sputtered AlN hard mask can be implemented into the fabrication processes of GaN VJFET and many other GaN-based devices.

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CHAPTER 3

Sputtered AlN as High-k Dielectric

High-k dielectrics are nowadays extensively studied as a replacement of silicon dioxide in various transistor devices as gate oxide. Therefore, developing an understanding of the dielectric and electrical properties of high-k dielectric material plays a key role in designing high-performance transistors. Steady advances in manufacturing technology have allowed for a steady reduction in transistor size[1)]. One of the major benefits can be acquired from the scaling is the reduction in channel length to achieve high drive current. The drive current I_D for a field effect transistor can be written as the equation below[2)],

$$I_{D,Sat} = \frac{W}{L}\mu C\frac{(V_G - V_{th})^2}{2} \tag{3.1}$$

where W is the width of the transistor channel, L is the channel length, μ is the channel carrier mobility, and C is the gate capacitance. An increase in drive current requires a reduction in channel length or an increase in the gate oxide capacitance. However, channel length scaling comes with the issue associated with short channel effect such as drain-induced barrier lowering (DIBL), where the drain voltage widens the drain depletion region to a point that reduces the potential barrier, causing higher leakage current at subthreshold gate voltage[3)]. (Figure 3.1)

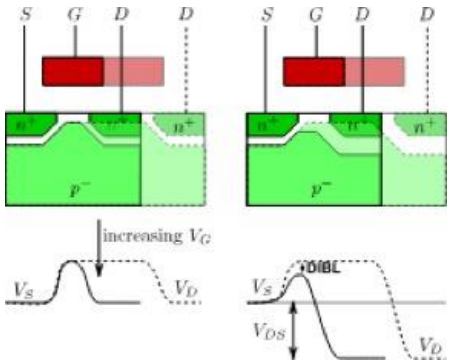


Figure 3.1: Drain induced barrier lowering of short channel transistor[4)]

An alternative method to achieve high drive currents and controllable short channel effects is to increase gate oxide capacitance. Regardless of the quantum mechanical and depletion effect from the device body and gate, the capacitance can be modeled as a parallel plate capacitor. The gate oxide capacitance in a MOSFET can be described as the equation[5)],

$$C = \frac{\kappa \varepsilon_0 A}{t} \tag{3.2}$$

where A is the capacitor area, κ is the relative dielectric constant, ε_0 is the vacuum permittivity, t is the thickness of the capacitor oxide insulator. The gate oxide scaling has been considered a limiter for thickness below 2 nm, where a further decrease in oxide thickness would cause dramatic increase in leakage currents due to tunneling, leading to high power consumption and reduced device performance[6)], Silicon Dioxide (SiO_2) has been used as the gate material for MOSFET for decades[7)]. An approach to increase gate capacitance without the associated leakage effect is to replace SiO_2 with a high-k dielectric material. A high-k dielectric material has a much smaller equivalent oxide thickness (EOT) than SiO_2, which the EOT is the thickness of SiO_2 of a transistor that would be required to achieve same capacitance as the high-k material is used. As indicated in Figure 3.2, for the equivalent gate oxide thickness, high-k dielectric has significant orders of magnitude less gate leakage than SiO_2 since the actual material thickness is thicker[8)].

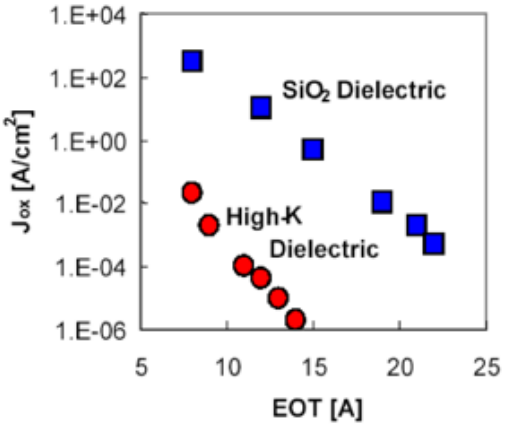


Figure 3.2: Comparison of gate oxide leakage of SiO_2 and high-k dielectric[8)]

Study on high-k dielectrics for MOSFET has become an area of active research, such as Al_2O_3 and HfO_2[9,10)]. For GaN-based power devices, there are challenges in controlling the interface between the nitride and the gate oxide, therefore, developing a nitride-based gate dielectric material becomes an urgent need. AlN with a large energy band gap (6.2 eV) promises excellent electrical isolation properties for a high breakdown field; combining with its high dielectric constant up to 8.5, AlN can be a favorable gate dielectric in the application of GaN-based power transistors[11,12)]. Shih et al. have studied on sputtered amorphous AlN gate dielectric for AlGaN/GaN MIS-HFET, indicating good insulating properties of the AlN, and reduced gate leakage currents. In this work, the dielectric property and breakdown field of sputtered AlN will be studied and discussed, for evaluating its feasibility as a good alternative gate dielectric for MOS devices.

3.1 MIM/MIS Capacitors Process Flows

3.1.1 MIM Capacitors, Gen-1

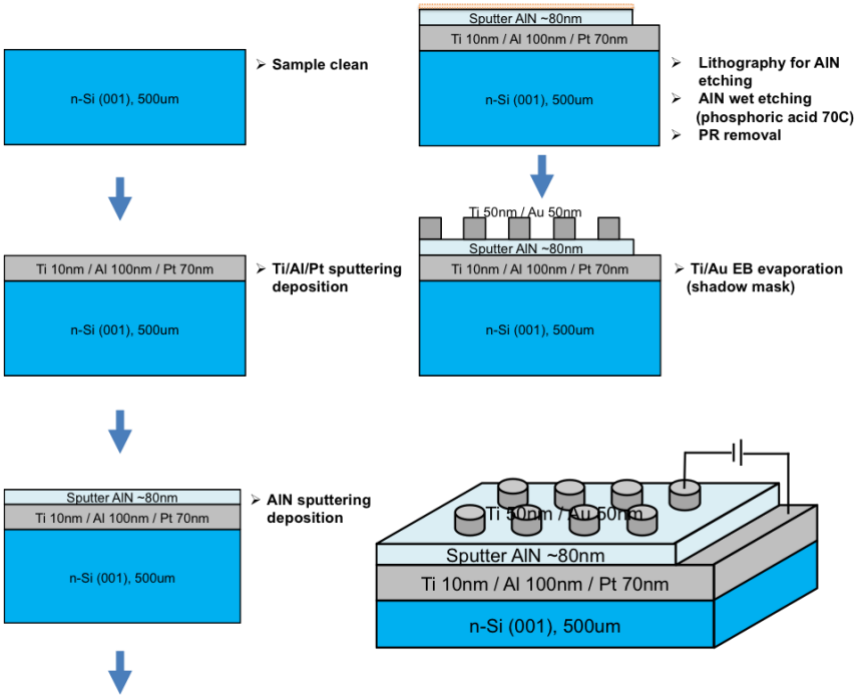


Figure 3.3: Process flow of MIM Capacitors, Gen-1

Figure 3.3 shows the test structure of metal-insulator-metal (MIM) Capacitors. The MIM Capacitor includes a bottom layer of metal plate, a dielectric insulating layer disposed on the metal plate, and metal anodes stacked on the capacitor dielectric layer. Pieces of 1 cm^2 n-type (001) Si wafers are used in this device as the substrate. The bottom layer of the metal plate is deposited by sputtering that consists of 10nm Ti / 100nm Al / 70nm Pt from the bottom to top. Ti is used for adhesion, and Pt is used as the oxidation protection layer due to its inert property. The metal layers are sputtered under the condition of 300^{o}C, 3 mTorr, 30 sccm Ar flow, 400 W, and each layer is sputtered sequentially with the samples inside the chamber. The dielectric layer AlN is then sputtered on the metal plate using the deposition conditions described in section 2.1. The dielectric material is etched to expose some area of the metal layer along the edge. Positive photoresist S1813 is spin coated for wet etching at 4000 rpm and 1000 ramp for 60 seconds. Some area of the

photoresist is removed by acetone with the swab. The photoresist is then soft baked at 90°C for 1 minute and developed with AZ-726 for 40 seconds. The sputtered AlN is wet etched by hot phosphoric acid at 70°C. The photoresist is removed by hot Microposit Remover 1165 at 80°C for 20 minutes. The top metal anodes are deposited by E-beam evaporation of 50 nm Ti / 50 nm Au using shadow mask. In addition to AlN, MIM Capacitors are also fabricated with three other dielectric materials for comparative study, including PECVD SiO_2, PECVD SiN_x, and ALD Al_2O_3. PECVD SiO_2 is deposited under the conditions of 350°C, 1500 mTorr, 50/900 sccm Silane/N_2O flow at 10 W. PECVD SiN_x is deposited under the conditions of 300°C, 1600 mTorr, Silane/NH_3/N_2=20/30/1425 sccm at 160 W. Plasma ALD Al_2O_3 is deposited at 300°C. PECVD SiO_2, PECVD SiNx, are wet etch by BOE 6:1, and ALD Al_2O_3 is dry etched by ICP plasma dry etching under the conditions of BCl_3/Ar=40/10 sccm, 5 mTorr, RF1 40 W, and RF2 600 W. More detailed step-by-step fabrication processes are listed in the process sheet 2 in the appendix.

The MIM Capacitors are measured; however, the devices are leaky with a low yield <10% for about 40 devices measured total. The reason could be caused by nanoparticle-like features on the devices as shown in Figure 3.4. Step-by-step control samples are inspected, and no nanoparticle features are observed on the Pt metal layer prior to the AlN deposition. After the AlN deposition, nanoparticle features appeared due to the inert characteristics of Pt that inhibits the growth. Similar features are also observed on MIM Capacitors with other dielectric materials.

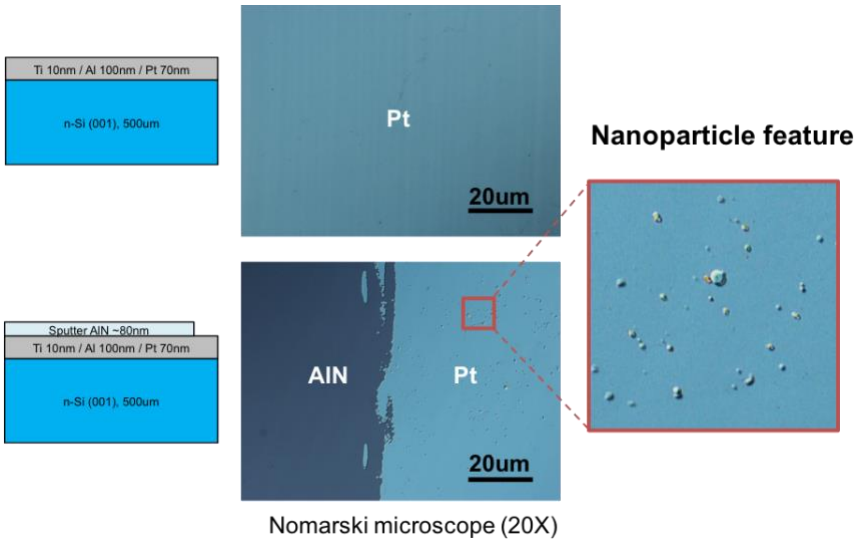


Figure 3.4: Nanoparticle features on sputtered AlN MIM Capacitor device, Gen-1

Another issue associated with this generation of MIM Capacitors is that the uncertainty about the anode size. Figure 3.5 shows that the anode patterns are enlarged due to deposition under mask under the microscope, which can cause inaccuracy for the dielectric constant characterization for this study. Therefore, a second generation MIM Capacitor structure is designed and fabricated to resolve the above issues.

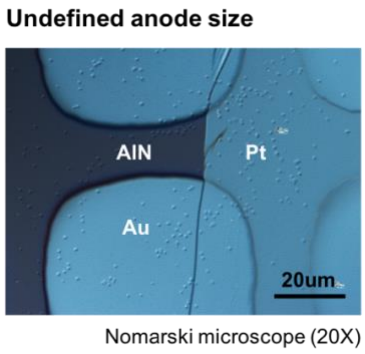


Figure 3.4: Undefined anode size on sputtered AlN MIM Capacitor device, Gen-1

3.1.2 MIM Capacitors, Gen-2

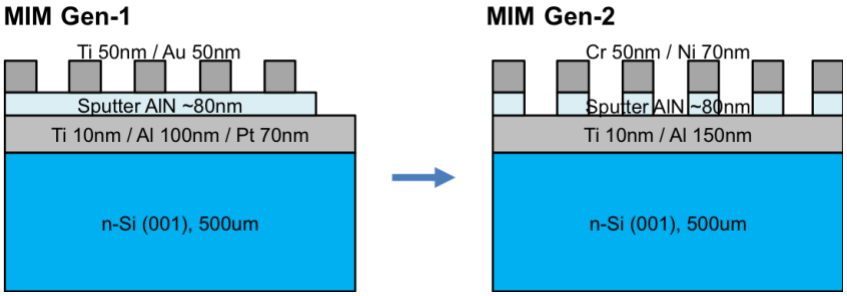


Figure 3.5: Process flow of MIM Capacitors, Gen-2

Figure 3.5 shows the device structural design of MIM Capacitors, Gen-2. Similar to many steps of MIM Capacitors, Gen-2. The bottom metal plate is deposited using sputtering of 10 nm Ti / 150 nm Al, but without the Pt layer to eliminate the nanoparticle features problem. For a more defined shape of metal anodes, they are patterned into circular shapes using stepper. Negative photoresist AZ2020 is spin coated at 6000 rpm 6000 ramp for 60 seconds. The photoresist is soft baked at 115^{o}C for 1 minute. The stepper exposure time is 0.2 second using a photomask that has circular patterns. A post-exposure bake is used to reduce standing waves in resist exposed on the stepper. The sample is then post-baked at 115^{o}C for 1 minute, and developed in MIF 726 at room temperature for 100 sec. The sample is descumed by Gen-1000 oxygen plasma source to strip off the residual photoresist material at the conditions of O_2=42 sccm, 20 mTorr, RIE = 100 W for 2 minutes. After photolithography, 50 nm Cr / 70 nm Ni are deposited by E-Beam evaporation. Cr and Ni are patterned by the lift-off process using Microposit Remover 1165 for 5 minutes with sonication at room temperature, followed by a descum process using oxygen plasma source of O_2=42 sccm, 20 mTorr, RIE = 500 W for 2 minutes. The Cr/Ni anodes can serve as a hard mask to pattern the dielectric materials. More detailed step-by-step fabrication processes are listed in the process sheet 3 in the appendix. The removal of Pt intern metal layer has resolved the issue of nanoparticle feature. By using the stepper, more defined anode sizes are achieved in 80, 180, 380

um diameter circular shapes. However, the device yield is still very low <20% for about 30 devices measured in total. Some issues related to the metal and dielectric insulating layer is suspected, but the reason is still not clear. To proceed with this study, MIS Capacitor structure is designed to ideally generate high yield devices.

3.1.3 MIS Capacitors

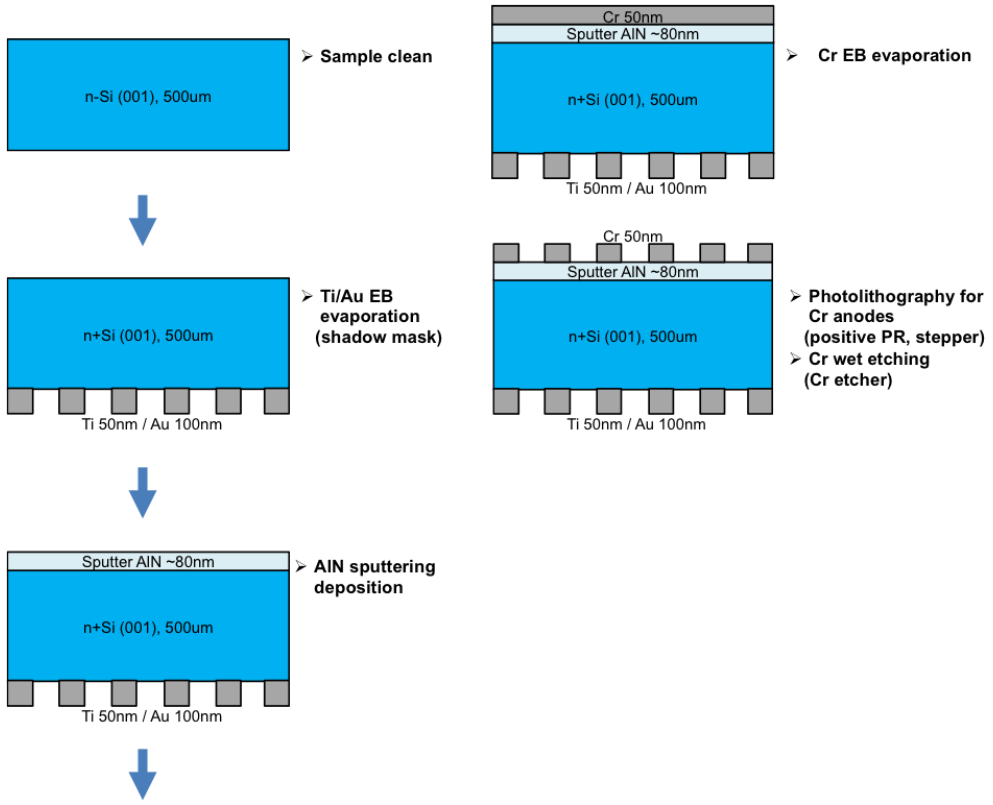


Figure 3.6: Process flow of MIS Capacitors

Figure 3.6 shows the process flow of MIS Capacitors. Highly doped n-Si is used in this device. Metal back contact of 50 nm Ti / 100 nm Au is deposited using E-beam evaporation with shadow mask. The AlN is sputtered on Si using the same deposition conditions described in section 2.1. Cr is then deposited on AlN using E-beam evaporation. The Cr anodes are patterned by photolithography using stepper. Positive photoresist SPR700 is spin coated at 6000 rpm for 45

seconds. The photoresist is soft baked at 95°C for 1 minute. The stepper exposure time is 0.2 second using a photomask that has circular patterns. The sample is post-baked at 115°C for 1 minute and developed in MIF 726 at room temperature for 60 sec. The sample is descumed by Gen-1000 oxygen plasma source to strip off the residual photoresist material at the conditions of O_2=42 sccm, 20 mTorr, RIE = 100 W for 2 minutes. Cr is ICP plasma dry-etched under the conditions of Cl_2/O_2=36/4 sccm, 4 mTorr, 15/300 W, DC:90 V. The photoresist is removed by hot Microposit Remover 1165 at 80°C for 20 minutes. More detailed step-by-step fabrication processes are listed in the process sheet 4 in the appendix. The Back contact of metal on Si is confirmed to be ohmic contact by I-V measurement that consists a linear behavior. MIS capacitors are also fabricated with PECVD SiO_2, PECVD SiN_x, and ALD Al_2O_3 under the same deposition conditions as mentioned above. Ohmic contact can be further improved to reduce the contact resistance by rapid thermal annealing (RTA) 500°C for 30 seconds as shown in Figure 3.7.

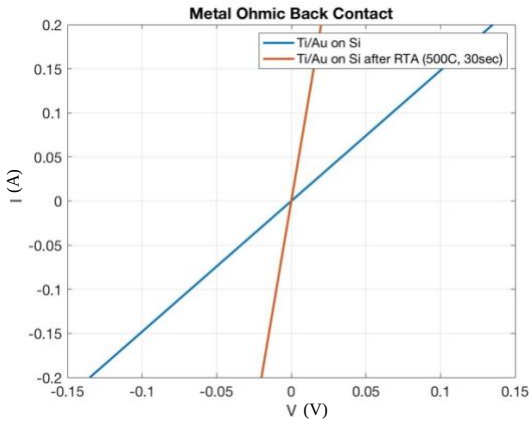


Figure 3.7: Metal ohmic back contact before and after RTA

For the dielectric constant of the deposited dielectric materials, the accuracy of thickness measurement becomes very important. The film thicknesses of sputtered AlN, PECVD SiO_2, PECVD SiN_x, and ALD Al_2O_3 are measured as 83 nm, 47 nm, 68 nm, 47 nm using ellipsometry. During the fabrication process of MIM Capacitors, Gen 1, the thickness of sputtered AlN film is also measurement by atomic force microscopy (AFM) as shown in Figure 3.8. The AlN film

thickness measured by AFM as 61.3 nm shows good agreement with the ellipsometry measurement (59.7 nm) with an offset of 1.5 nm.

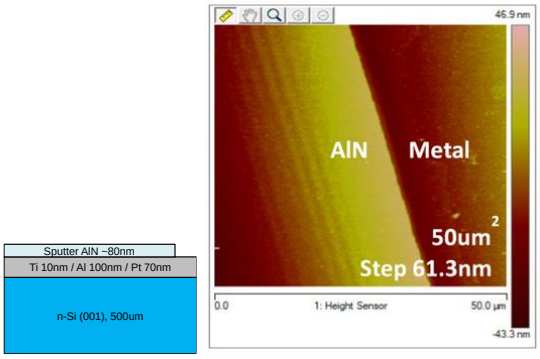


Figure 3.8 AFM thickness measurement of sputtered AlN on metal (MIM, Gen1)

3.2 C-V Characteristic of Sputtered AlN MIS Capacitors

Figure 3.9 shows the C-V characteristic of sputtered AlN MIS Capacitors in order to evaluate the dielectric constant of the material. The AlN dielectric insulator layer has a thickness of 83 nm, and the capacitors are in circular shape with diameters of 180 um, 380 um. Under the gate voltage sweep of -10 to +10 V at 500 Hz, a nearly linear C-V relationship is observed. Repeated measurements under identical conditions gave the same capacitance linearity, showing that no substantial wear out takes place during the measurements.

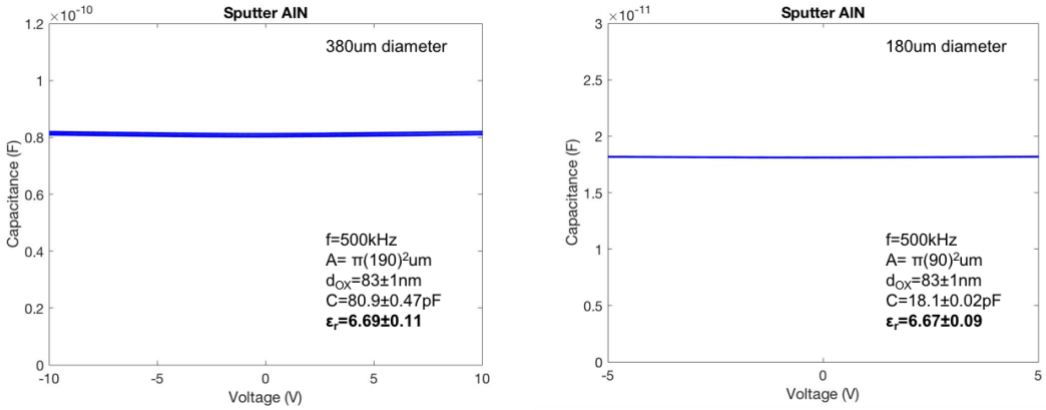


Figure 3.9: C-V characteristic of sputtered AlN MIS Capacitors

The dielectric constant is calculated using the equation,

$$\varepsilon_r = \frac{Ct}{\varepsilon_o A} \tag{3.3}$$

where C is the capacitance extrapolated from the C-V curve, t is the sputtered AlN film thickness measured by Ellipsometry, ε_0 is the vacuum permittivity (8.854×10^{-12} F·m^{-1}), and A is the device area. For devices in both sizes, the dielectric constant is calculated to be around 6.7.

For general C-V behavior of MIS capacitors, a capacitance drop would be expected in the depletion region as the gate voltage increases beyond the flat band voltage, where the MIS capacitor consists of two capacitors in series: the oxide capacitor, and the depletion-layer capacitor. The obtained results show that the device follows the character of the MIM Capacitor, indicating high doping of the Si substrate. To confirm the device behavior, the doping concentration of Si is determined by Hall-Effect, and 1D Poisson simulation is performed to model the C-V curve with measured doping concentration. The sheet concentration of 500 um Si substrate is measured as $(1.97 \pm 0.60) \times 10^{18}$ cm^{-2}; therefore, the doping concentration is calculated as $N_d = (3.93 \pm 1) \times 10^{19}$ cm^{-3}. Figure 3.10 shows simulated C-V characteristics of SiO_2 (from the material database) using measured doping concentration $N_d = (3.93 \pm 1) \times 10^{19}$ cm^{-3}, and a low input doping concentration $Nd = 4 \times 10^{15}$ cm^{-3}. The simulation confirmed the MIM Capacitor-like behavior with high Si doping concentration.

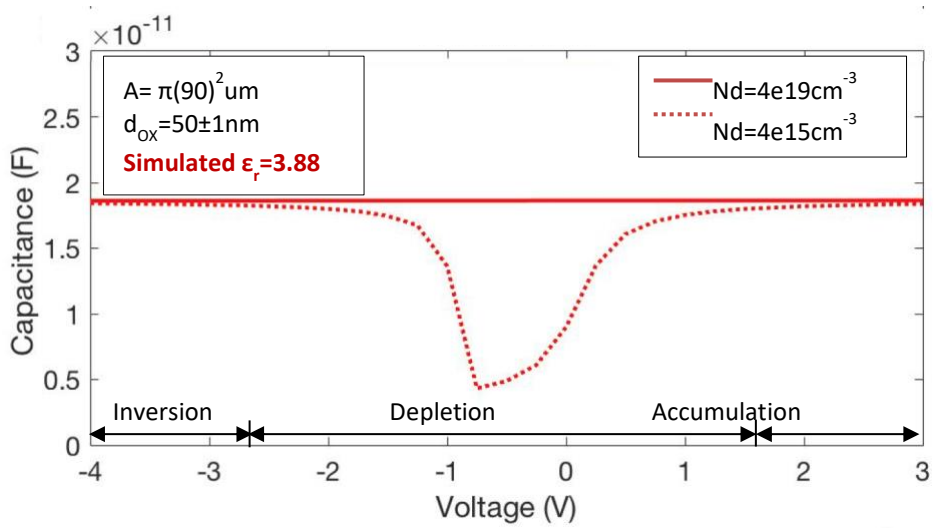


Figure 3.10 1D Poisson simulation of the C-V characteristics of SiO_2

The capacitance of the MIM Capacitors is measured at different frequencies ranging from 200 kHz to 1 MHz with a bias swept from -10 to 10 V and the capacitance shows little variation between the considered frequency range. (Figure 3.11)

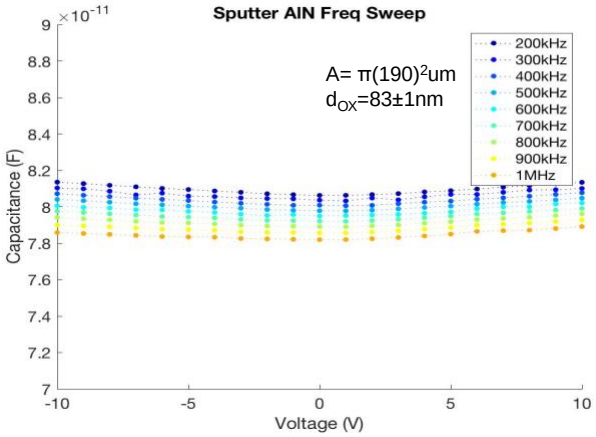


Figure 3.11: C-V characteristic of sputtered AlN MIS Capacitors with frequency sweep

From the above discussion, the dielectric constant of sputtered AlN is measured to be 6.7 in this work, and researchers reported different values depending on the film quality. Gould et al. reported the dielectric properties of AlN deposited by RF magnetron sputtering that the relative permittivity is approximately 9.1; the film structure is not discussed in this study[14]. Adam et al. studied on the electrical properties of MIS capacitors with AlN gate dielectrics using reactive magnetron sputtering, indicating the dielectric permittivity is between 4 and 11[15]. The amorphous AlN film is sputtered at room-temperature using powers of 50 and 100 W with 5 mT of 15% argon and 85% nitrogen. Figure 3.12 shows that AlN film sputtered at 50 W have higher dielectric permittivity; thermal annealing of dielectric in N_2 at 750°C or oxidizing in dry O_2 at 800°C can further increase the dielectric constant.

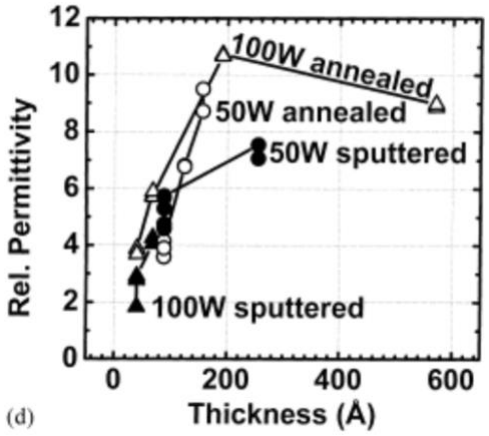


Figure 3.12 Effect of sputtering power and thermal annealing on the AlN dielectric constant[15)]

Ramadan et. al reported the dielectric constant of c-axis oriented AlN to be 8.7-8.9. The film is deposited using reactive DC sputtering at room temperature at 200–300 W powers, 1 mTorr pressure, and under 2:1 Ar/N_2 flow ratio[16)]. Since the sputtered AlN film has a highly-crystalline structure in Ramadan's work, a higher dielectric constant is expected.

3.3 I-V characteristic of sputtered AlN MIS Capacitors

The I-V characteristics of MIS Capacitors are measured to evaluate the breakdown field of sputtered AlN at both forward and reverse bias. Devices are measured through breakdown and then remeasured to confirm the permeant failure. Figure 3.13 shows the current density versus voltage sweeps, where the breakdown field is measured to be ~4.2-4.3 MV/cm at forward bias and ~6.0-6.6 MV/cm at reverse bias.

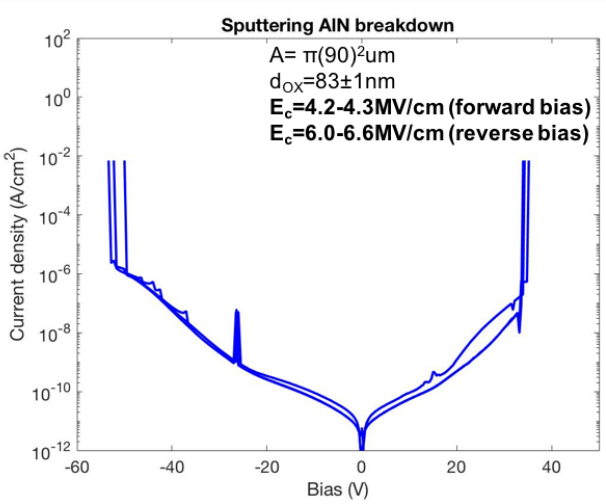


Figure 3.12: I-V characteristic of sputtered AlN MIS Capacitors

The breakdown field at forward bias is measured to be lower than that at the reverse bias. One reason is that the barrier height between the anode metal and AlN and that between the Si conduction band edge and AlN are different. Another reason can be that the formation of the depletion region under the reverse bias adds up to the insulating layer thickness resulting in higher breakdown voltage. As shown in the Figure 3.13, under reverse bias, if a more negative bias than flat band voltage is applied, the band diagram on the gate side will be pulled upward and a depletion region at the Si surface appears. Although the n+Si is heavily doped with a high doping concentration of (4±1)x10^{19} cm^{-3}, the depletion region is calculated to take into consideration. To calculate the maximum possible depletion width under the applied voltage before breakdown (~55 V), the electric field across the oxide and in the Si at the insulator-semiconductor interface is calculated to be 55.4 V.

$$V_{Total} = V_{app} + V_{FB} \tag{3.4}$$

$$V_{Total} = 55V + (\Phi_{Cr} - \Phi_{Si}) \tag{3.5}$$

$$V_{Total} = 55V + \left(\Phi_{Cr} - (X_{Si} + (E_{c\_Si} - E_{F\_Si}))\right) \tag{3.6}$$

$$V_{Total} = 55V + \left(\Phi_{Cr} - (X_{Si} + kTln\frac{N_{c\_Si}}{N_{d\_Si}})\right) \tag{3.7}$$

$$V_{Total} = 55V + \left(4.5eV - (4.05eV + 0.26ln\frac{2.8e19}{3.93e19}\right) = 55.4V \quad (3.8)$$

The depletion width (W_s) in the Si is calculated using the equation,

$$\frac{q*N_d*W_s}{\varepsilon_{ox}} * t_{ox} + \frac{1}{2}\frac{q*N_d*{W_s}^2}{\varepsilon_{Si}} = 55.4V \quad (3.10)$$

Where q = 1.6x10^{-19} C, Nd = 3.93x10^{19} cm^{-3}, ϵ_{Si} = 11.9*8.85x10^{-14} F·cm^{-1}, $\epsilon_{ox\ (assumed)}$= 9*8.85x10^{-14} F·cm^{-1}, t_{ox}=80x10^{-7} cm. The depletion width (W_s) in Si is calculated to be 8.29 nm. Although the depletion width is relatively small comparing to the dielectric layer thickness, it can attribute to higher breakdown voltage at the reverse bias.

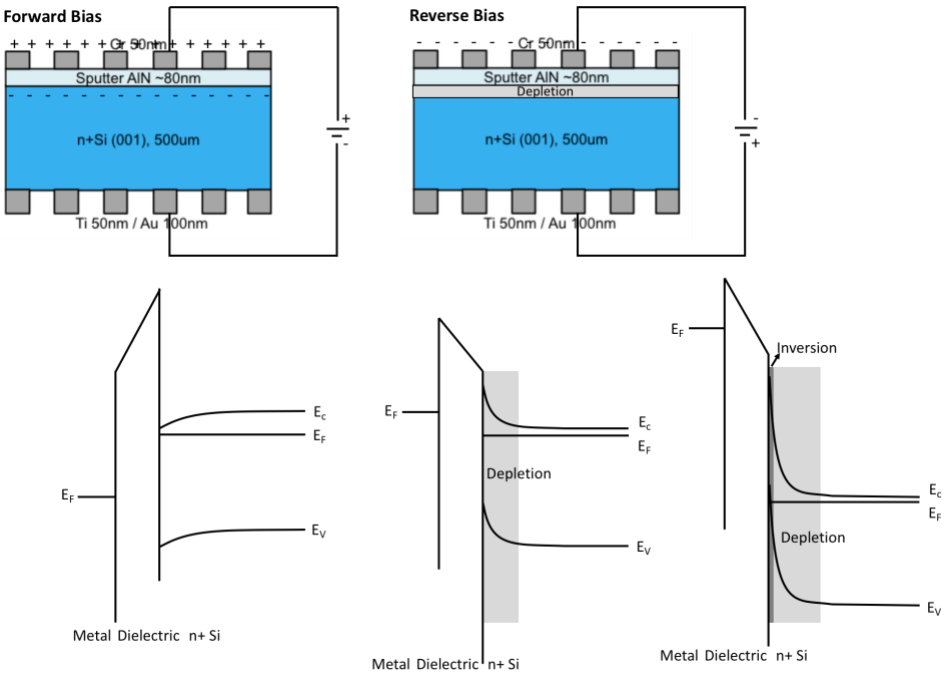


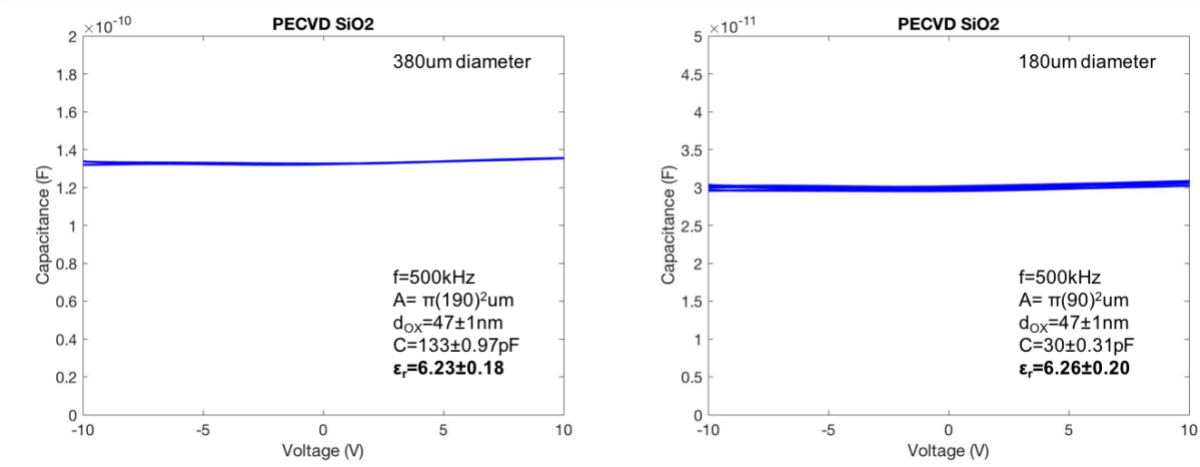
Figure 3.13: Band diagrams of sputtered AlN MIS Capacitors

Sputtered AlN can become an attractive alternative high-k dielectric material if the breakdown fields can be further improved. Adam et al. reported breakdown field around 4 MV/cm

for MIS capacitors fabricated with sputtered AlN using the conditions mentioned previously, and the breakdown field can be increased up to 12 MV/cm by lowering the sputtering power and thermal annealing[15]. For the future work of this project, improvements in the high-k performance of sputtered AlN can be made by lowering the sputtering power and thermal annealing to improve its film quality. As discussed in section 2.4, annealed AlN shows a significant reduction in the etch rate and enlargement in grain size, which indicative of higher film quality. Such considerations can be incorporated into the future study for evaluating the dielectric properties of sputtered AlN.

3.4 C-V and I-V characteristics of PECVD SiO_2, PECVD SiN_x, and ALD Al_2O_3 MIS Capacitors

The C-V characteristic of PECVD SiO_2, PECVD SiNx, and ALD Al_2O_3 MIS capacitors are measured as shown in Figures 3.14-3.16.



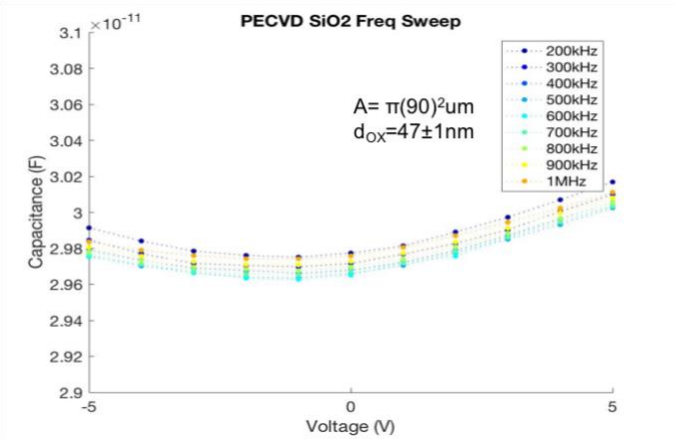


Figure 3.14: C-V characteristic of PECVD SiO_2 MIS capacitors

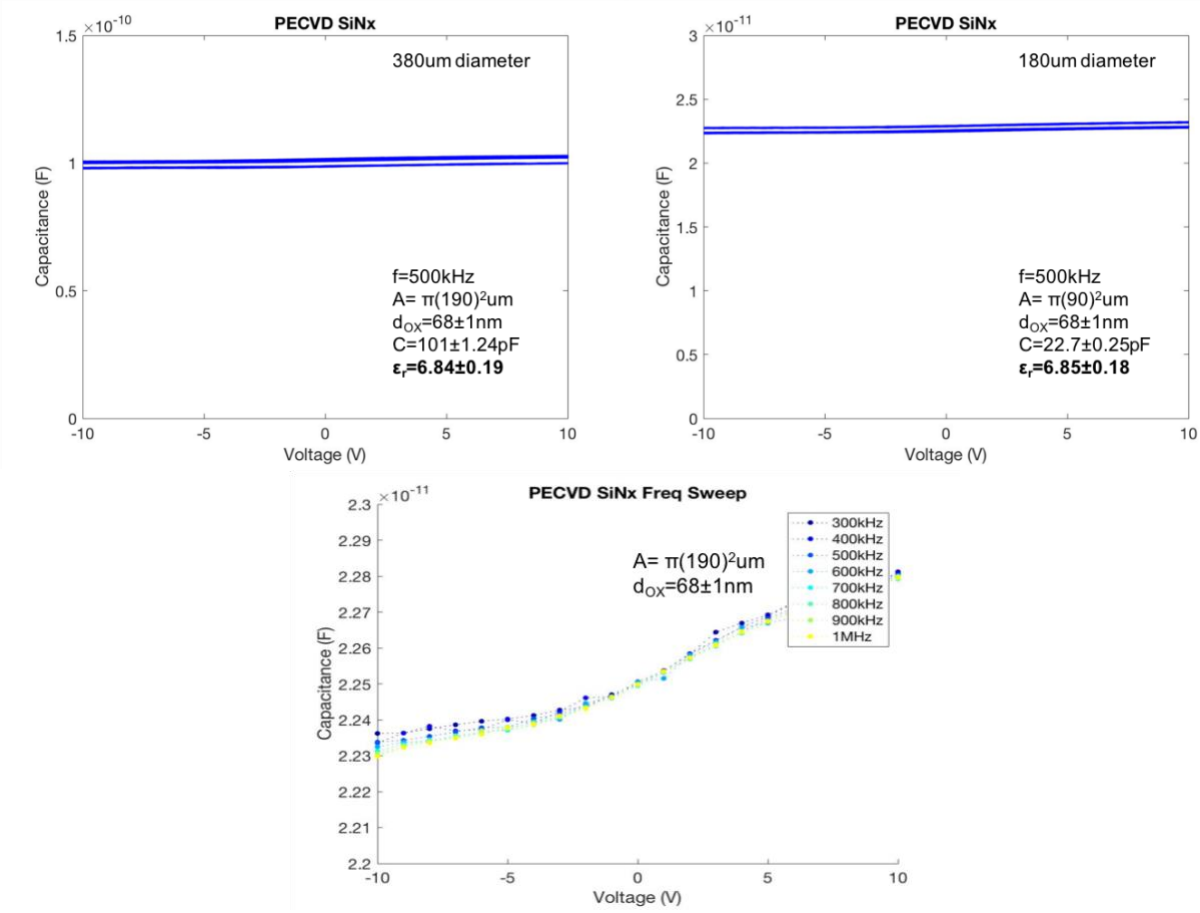


Figure 3.15: C-V characteristic of PECVD SiN_x MIS Capacitors

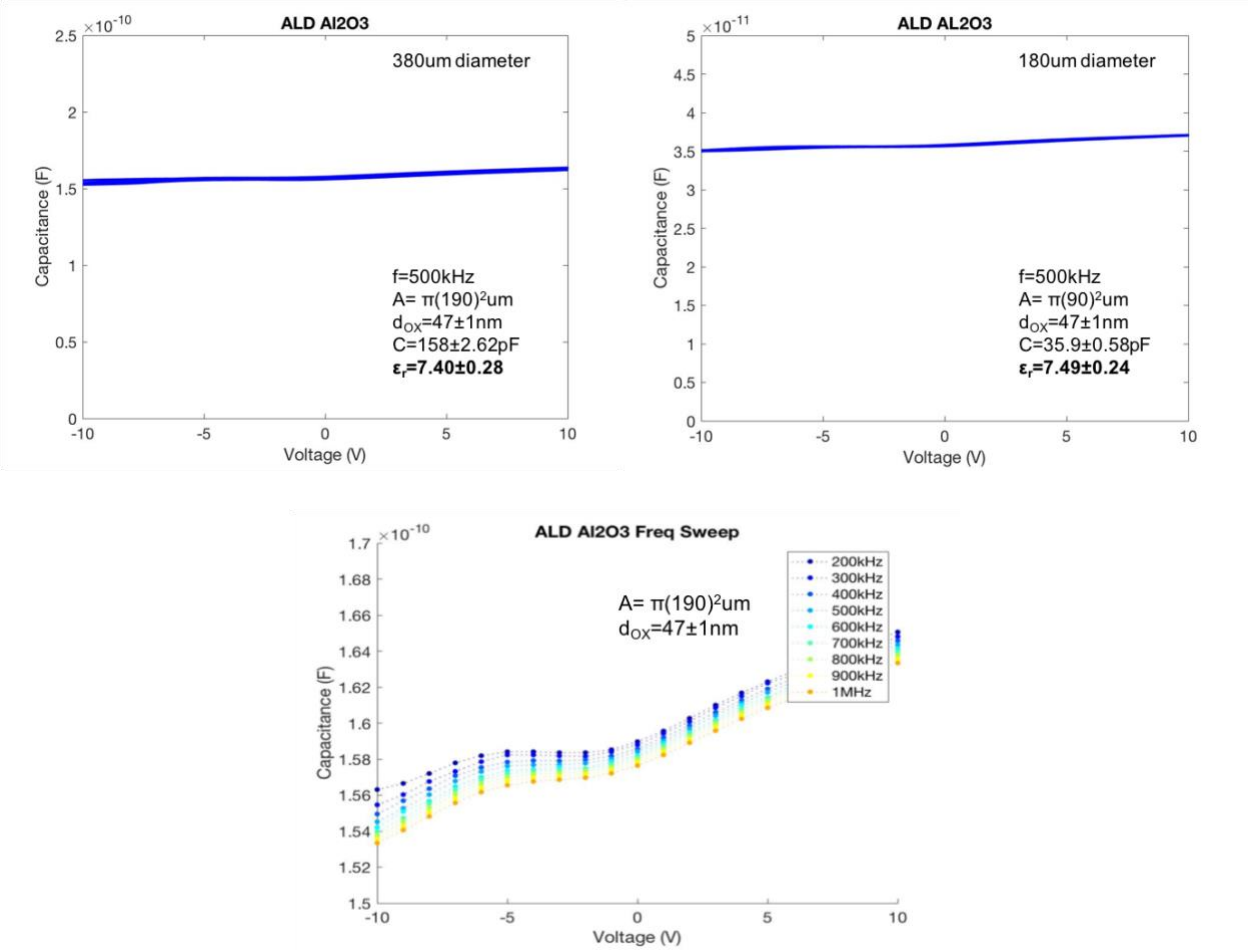


Figure 3.16: C-V characteristic of ALD Al_2O_3 MIS capacitors

The dielectric constant of PECVD SiO_2, PECVD SiNx, and ALD Al_2O_3 are each calculated to be 6.2, 6.8, 7.4, and the capacitance shows little frequency dependence. The measured dielectric constant of PECVD SiO_2 is much higher than the expected value (~3.8). The refractive index of deposited PECVD SiO_2 is evaluated at wavelengths from 380 to 1000 nm using spectroscopic ellipsometry in order to determine the stoichiometry of the film. Figure 3.17 shows the ellipsometry measurement of PECVD SiO_2 using Cauchy model, where the three terms A, B, C are adjusted to match the refractive index for the material. The refractive index is measured to be 1.58, which is high than the reference value of the refractive index for pure SiO_2 (1.46-1.47). This SiO_2 film is deposited under the conditions of 350°C, 1500 mTorr, 50/900 sccm Silane/N_2O flow, 10 W. One reason can be that the low power and high Silane ratio caused Silane self-reaction with

deficiency of oxygen gas from the N_2O flow, creating Si-rich SiO_x film. The reflective index of PECVD SiO_2 is re-evaluated using the deposition conditions of 350°C, 1800 mTorr, 20/2500 sccm Silane/N_2O flow, 30 W and 140W, and it is measured to be 1.48, and 1.46. Therefore, the MIS Capacitors that are made of PECVD Si-rich SiO_x film should not be used as a representation for characterizing the dielectric properties of SiO_2.

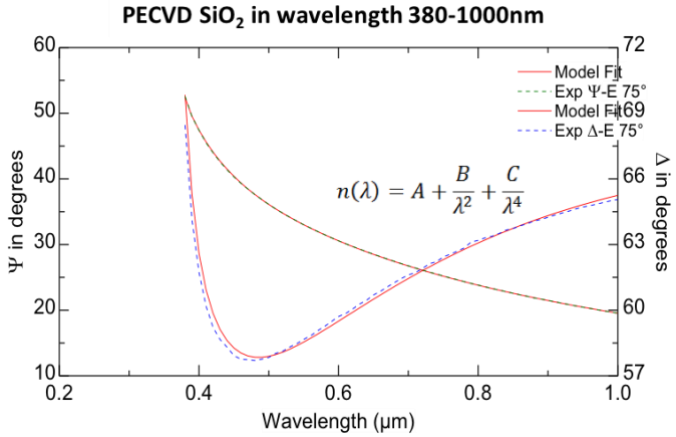


Figure 3.17: Ellipsometry measurement of PECVD SiO_2

Figure 3.18 shows the I-V characteristics of PECVD SiNx, and ALD Al_2O_3 MIM Capacitors, where the breakdown field of PECVD SiNx is measured to be ~4.3-5.2 MV/cm at forward bias and ~10-10.7 MV/cm at reverse bias, and the breakdown field of ALD Al_2O_3 is measured to be ~6.4-6.5 MV/cm at forward bias and ~7.4-8.3 MV/cm at reverse bias.

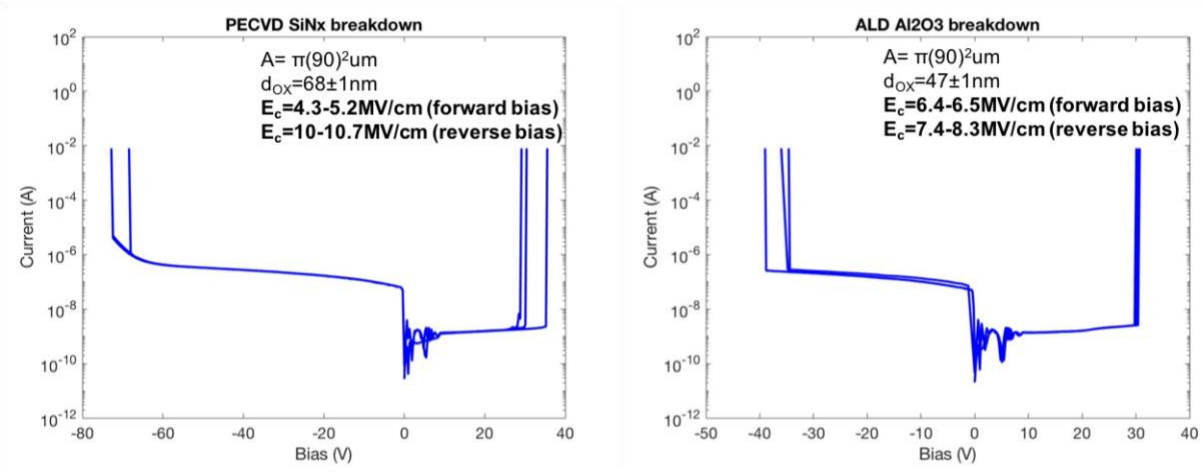


Figure 3.18: I-V characteristic of PECVD SiNx and ALD Al_2O_3 MIS capacitors

Comparing with sputtered AlN that has a measured dielectric constant of 6.7 and breakdown field of ~4.2-4.3 MV/cm at forward bias and ~6.0-6.6 MV/cm at reverse bias. ALD Al_2O_3 can be a better candidate as high-k gate dielectric for high voltage power devices. For future study, more systematic considerations of the required properties of gate dielectric should be taken, not only the dielectric constant and breakdown field, but also including band alignment, thermostability, interface quality, and compatibility with the semiconductor materials that are used in processing for MOS devices. Much research is still required to make high-k dielectrics show promise with respect to all of these expectations toward successful integration into future MOS technologies.

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CHAPTER 4

Time-Dependent Dielectric Breakdown of Sputtered AlN

As transistors are scaling down for higher speed and increased functionality, gate oxide reliability becomes one of the principal concerns of MOS integrated circuits. To evaluate whether the gate dielectric satisfies the prospective reliability under working condition, it is important to understand the electric field dependence of time to breakdown. Time-dependent dielectric breakdown (TDDB) describes the destruction of the gate dielectric layer caused by defect accumulation under the stress of constant electric field over time that is lower than the dielectric strength of the material. Irreversible traps, broken bonds, or defects can often be generated under long-term electrical stress. So far, SiO_2, the most commonly used gate oxide material, has been studied under many research for evaluating its TDDB behaviors[1-4]. In this study, the TDDB focuses on sputtered AlN for understanding its reliability as high-k gate dielectric material for its potential in advanced MOS technologies.

4.1 TDDB Physics and Mechanisms

The most frequently used TDDB model for MIS capacitors is based on field-induced degradation[5]. According to thermochemical theory, the bond breakage for a molecule depends on its interaction frequency with the lattice times the Boltzmann probabilit[6]. The breakage rate constant k can be described as

$$k = v_0 e^{-\frac{\Delta H}{K_B T}} \tag{4.1}$$

where v_0 is vibration frequency, ΔH is the activation enthalpy to break the bond.

Since the external electrical field weakens the bonds, ΔH decreases with the applied field,

$$\Delta H = \Delta H_0 - p_{eff}(m,n)E_{ox} \tag{4.2}$$

where p is the effective dipole moment, m, n are based on the Mie-Grüneisen bonding parameters[7]. The time-to-failure (TF) is inversely proportional to k;

$$TF = A_0 e^{\left[\frac{\Delta H_0}{K_B T} - \frac{p_{eff}(m,n)E_{ox}}{K_B T}\right]} \tag{4.3}$$

therefore, TF in log scale is proportional to E_{ox}.

This TDDB model will not be expected if the molecular bond has no dipole moment. The major drawback of Thermochemical Model is its deficiency in polarity dependence, which the model does not explain the TDDB difference when the cathode and anode are reversed.

4.2 Weibull Statistical Distribution and Testing Method

Weibull and log-normal distributions both have been widely used for time-dependent dielectric breakdown statistics[8]. Generally, the Weibull distribution is preferred because it can incorporate measurements in various device areas with Poisson statistics[9]. It is reported that the discrepancy between the Weibull and log-normal distributions is negligible when the sample size is smaller than 100[10].

The Weibull distribution can be described in the equation,

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{4.4}$$

where F is the cumulative failure probability, η is the characteristic time-to-breakdown at the failure percentage of 63.2%, β is the shape factor of Weibull distribution, also known as Weibull slope, and t is breakdown time[1].

This equation can be linearized into,

$$\ln[-\ln(1- F(t))] = \beta\ln(t) - \beta\ln(\eta) \tag{4.5}$$

where ln[-ln(1- F(t))] yields a straight line with a slope of β; therefore, β and η values can be extrapolated from this linear relationship. The model extracted from the data can indicate the predicted time-to-failure for various testing voltage. For example, 50% of the devices fail when time t, satisfies the following equation:

$$0.5 = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{4.6}$$

The testing process involves biasing MIS test structures at a constant electric field that is lower than the critical field and measuring the leakage current until a drastic increase in current that signals the dielectric breakdown. For plotting the Weibull distribution, a number of identical devices are measured under the same biasing condition. The breakdown times are recorded and are arranged in ascending order. Median ranks can be obtained by Benard's approximation to estimate the unreliability for each failure,

$$F(t) = \frac{j-0.3}{n+0.4} \tag{4.7}$$

where j is the failure order, n is the sample size.

For example, if 20 devices are tested and the breakdown times are recorded. The Median rank $F(t)$ for the device that breaks the fasted can be calculated as $F(t) = \frac{1-0.3}{20+0.4}$

Therefore, Weibull statistical distribution can be plotted using the above approximation.

4.3 TDDB Measurement of Sputtered AlN and ALD Al_2O_3

Figure 3.6 in section 3.1.3 shows the test structures of MIS capacitor. Highly doped n-type (001) Si substrate with a doping concentration of ~4x10^{19} cm^{-3} is used in the device structure. Sputtered AlN with a thickness of 83 nm is deposited using the conditions described in section 2.1. The device areas are π(90um)^2. The breakdown field of sputtered AlN is measured to be ~4.3 MV/cm as discussed in section 3.3. The sputtered AlN MIS capacitors are stressed in the electric

field range 3.61-4.22 MV/cm at room temperature for a time-dependent dielectric breakdown study as shown in Figure 4.1.

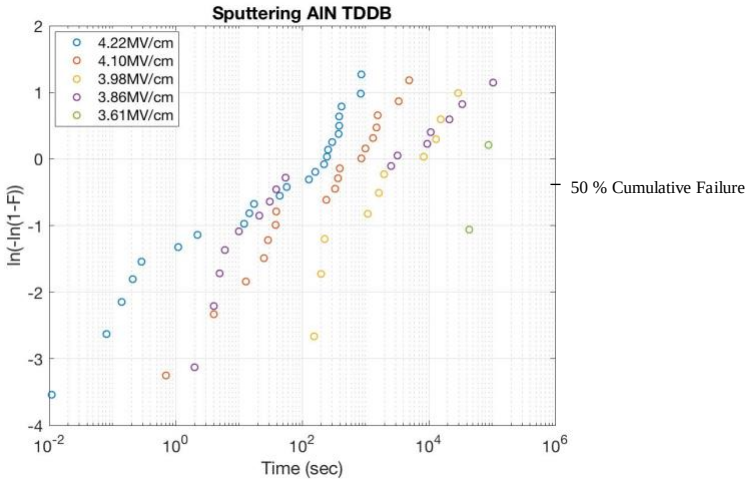

Figure 4.1: Weibull plots of sputtered AlN in the electric field range 3.61-4.22 MV/cm at room temperature

The electric field dependence of the intrinsic lifetime for positive gate bias of sputtered AlN is shown in Figure 4.2. The log (time to 50% failure) is proportional to E_{OX} according to the thermochemical theory, except that the point at breakdown field of 3.86 MV/cm is off the trend. Since the sample size (70 devices) is small, more data are needed to discuss the breakdown mechanism. From this trend line, the intrinsic lifetime at the low electric fields can be extrapolated from the model.

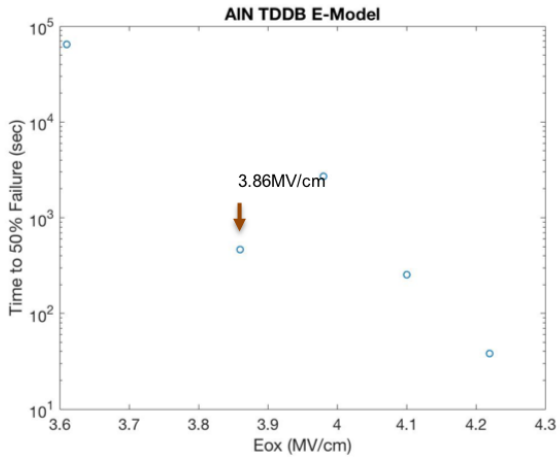

Figure 4.2: Time to 50% failure of 83 nm sputtered AlN as a function of electric field log(t_{BD})-E_{OX} plot

Figure 4.3 shows the time-dependent dielectric breakdown measurement of ALD Al_2O_3 to compare its behavior with sputtered AlN. ALD Al_2O_3 is deposited under the conditions as described in section 3.1.1. The film thickness is 47 nm and the device areas are $\pi(90um)^2$. The breakdown field of ALD Al_2O_3 was measured as ~6.5 MV/cm in section 3.4. Since the critical field of ALD Al_2O_3 is larger than sputtered AlN, it is expected that the time-to-failure of Al_2O_3 takes longer than sputtered AlN as the same constant biasing voltage, which makes it a better candidate as high-k gate dielectric material for high voltage power devices.

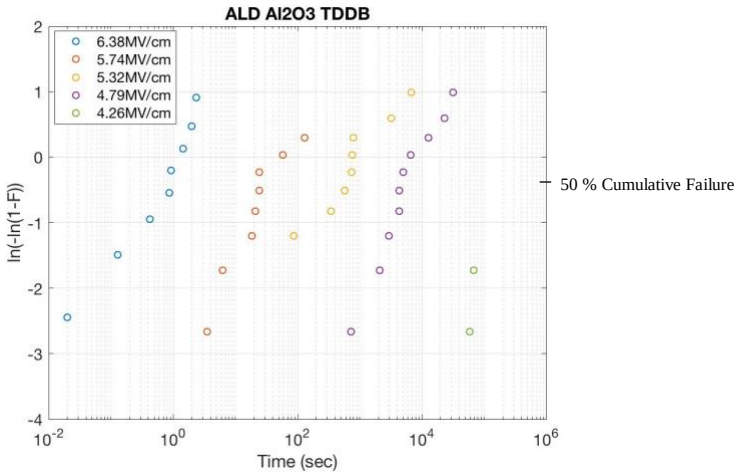

Figure 4.3: Weibull plots of ALD Al_2O_3 *in the electric field range 4.26-6.38 MV/cm at room temperature*

A relationship can be established to determine the failure rate for test devices in different areas. The final irreversible breakdown is transformed by many soft breakdowns. As shown in Figure 4.4, a larger device tends to have more soft breakdowns, so that it is expected to have a higher probability that one of the soft breakdowns turns into a final irreversible breakdown, resulting in a lower failure time[12)].

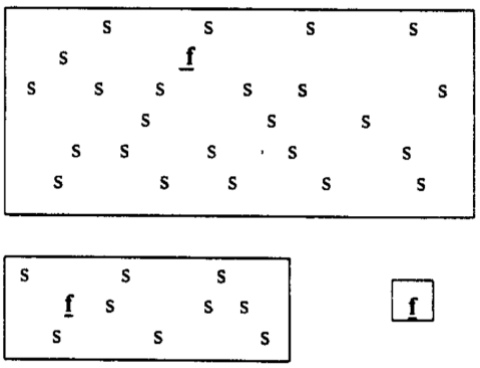

Figure 4.4: Breakdown failure probability in area dependence[12)]

Devices with different areas can be normalized based upon the Poisson model defect distribution, which has been widely used to derive area-scaling formulas for thin oxides[11, 13)]. The Poisson model assumes a random distribution of defects in the dielectric layer. The probability that a vulnerable area contains no defects can be expressed as[8)],

$$Y = e^{-\lambda(t)A} \tag{4.8}$$

where λ(t) is the average defect density that has been activated as a function of time, and A is the area. The cumulated failure rate is related to this yield:

$$F(t) = 1 - Y \tag{4.9}$$

$$F(t) = 1 - e^{-\lambda(t)A} \tag{4.10}$$

The Weibull distribution failure function is described as in (4.1):

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{4.4}$$

By setting the failure functions equal from equation (4.1) and (4.6), Weibull plot can be normalized with the area dependence relationship.

$$\lambda\,(t) = \left(\frac{t}{\eta}\right)^{\beta} \frac{1}{A} \tag{4.11}$$

$$F_2(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta} \frac{A2}{A1}} \tag{4.12}$$

The cumulative distribution function can then be normalized by the following equation,

$$1-F_1(t) = [1 - F_2(t)]^{\frac{A1}{A2}} \quad (4.13)$$

where A_1 and A_2 are device areas, and F_1 and F_2 are the cumulative distribution functions at a stress time t for A_1 and A_2.

Figure 4.5 shows the Weibull cumulative distribution versus the stress time for 47 nm ALD Al_2O_3 capacitors measured at 5.32 MV/cm at 40°C with different device areas of $\pi(40um)^2$ and $\pi(90um)^2$. Figure 4.6 shows the Weibull plots after area normalization, where the failure distribution calculated from $\pi(40um)^2$ devices using Eq. (4.8) shows good agreement with the distribution measured by $\pi(90um)^2$ devices, proving that the lifetime can be estimated for various device areas by using Eq. (4.8) for statistical normalization.

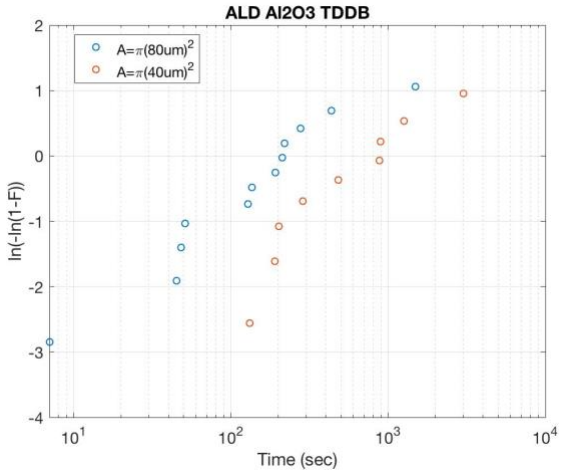

Figure 4.5: Weibull plots of ALD Al_2O_3 in different device areas of $\pi(40um)^2$ and $\pi(90um)^2$ at 5.32 MV/cm, 40°C

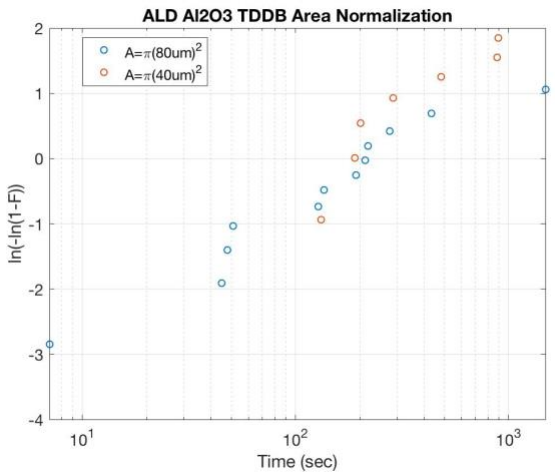

Figure 4.5: Weibull plots of ALD Al_2O_3 in different device areas of $\pi(40um)^2$ and $\pi(90um)^2$ at 5.32 MV/cm, 40°C after Poisson area normalization

Over the past years, significant amount of research and development efforts has been dedicated to investigating the breakdown models of gate dielectrics in order to understand the reliability of the materials. The Weibull function has been experimentally demonstrated by this work and many other studies to be the correct choice for describing the breakdown distribution. Recently, more concerns about Weibull shape factors are carried out for its dependency on thickness, voltage, temperature, and material polarity[14]. Therefore, further research is certainly needed to be able to describe the breakdown behaviors at a higher confidence level.

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[14] Wu, E.Y. and Vollertsen, R.P., 2002. On the Weibull shape factor of intrinsic breakdown of dielectric films and its accurate experimental determination. Part I: theory, methodology, experimental techniques. IEEE Transactions on Electron Devices, 49(12), pp.2131-2140.

CHAPTER 5

Conclusion

This work shows the development of aluminum nitride (AlN) as a hard mask material for GaN etching and regrowth. The fabrication technique enables the use of a III-nitride mask to eliminate the possibility of contamination in the GaN regrown junction interface by Si and O elements acting as shallow donors. Using reactive sputtering, AlN is deposited under the conditions of 300^{o}C, 3 m Torr, DC 400 W, and gas mixture of 15 sccm Ar and 15 sccm N_2, with a deposition rate of ~2.2 nm/min. XRD is performed indicating that the sputtered AlN film is an amorphous structure, which is desirable for selective wet etching over high-quality MBE-grown GaN during the process of mask removal. Sputtered AlN film is patterned under Cr/Ni metal mask using ICP dry etching under the conditions of BCl_3/Ar/Cl_2=10/10/20 sccm, 6 mTorr, RIE/ICP=20/250 W, DC=90 V. The dry etching rate is not yet determined but the lower bound is 20 nm/sec under this condition. SEM images are taken to inspect the sidewall profile, indicating near-vertical edge profile and smooth sidewalls. Wet etching study of as-sputtered AlN is performed to ensure the hard mask removal, which the AlN film can be wet etched in RT 50% KOH at 33 nm/s, and in 70C 80% H_3PO_4 at 16 nm/s. Sputtered AlN is annealed at 800^{o}C for 30 minutes to simulate the regrowth condition. XRD indicates the AlN film quality has been improved by forming crystal domains, and AFM shows that the grain size of the film has been enlarged after annealing. The wet etching rate has been greatly reduced due to the improved crystal quality, which the etching rate of annealed AlN in 70^{o}C H_3PO_4 has reduced to 0.6 nm/s. An increase in the H_3PO_4 solution temperature to 80^{o}C is used to achieve decent etching rate of

6.5 nm/s. Sputtered AlN shows great potential as a hard mask that has desirable features such as near-vertical edge profile, smooth sidewall, grass-free, easy to remove after regrowth, and good thermal stability, which can be implemented into fabricating GaN-based devices.

This work has also reported the characteristics of metal insulator semiconductor (MIS) capacitors with sputtered AlN as the dielectric material. Two generations of metal insulator metal (MIS) capacitors are also fabricated; however, the device yield is low due to some issues related to the metal-dielectric layer interface. Capacitance-voltage (C-V) and Current-voltage (I-V) measurements revealed a dielectric constant of 6.7, breakdown fields of 4.2-4.3 MV/cm at forward bias, and 6-6.6 MV/cm at reverse bias. For the future work of this project, improvements in the high-k performance of sputtered AlN can be made by lowering the sputtering power and thermal annealing to improve its film quality and thereby the dielectric constant and breakdown field. The C-V and I-V characteristics of PECVD SiO_2, PECVD SiNx, and ALD Al_2O_3 MIS capacitors are also tested for comparative study. PECVD SiO_2 is deposited under the conditions of 350^{o}C, 1500 mTorr, 50/900 sccm Silane/N_2O flow, 10 W. PECVD SiN_x is deposited under the conditions of 300^{o}C, 1600 mTorr, Silane/NH_3/N_2=20/30/1425 sccm, 160 W. Plasma ALD Al_2O_3 is deposited at 300^{o}C. The dielectric constant of PECVD SiO_2, PECVD SiN_x, and ALD Al_2O_3 are each measured to be 6.2, 6.8, 7.4. The high dielectric constant of PECVD SiO_2 is caused by incorrect stoichiometry of Si-rich SiO_x film due to low deposition power and high Silane ratio; therefore, it cannot be used as a representation for characterizing the dielectric properties of SiO_2. The breakdown field of PECVD SiNx is measured to be ~4.3-5.2 MV/cm at forward bias and ~10-10.7 MV/cm at reverse bias, and the breakdown field of ALD Al_2O_3 is measured to be ~6.4-6.5 MV/cm at forward bias and ~7.4-8.3 MV/cm at reverse bias. Cooperating with the properties above, ALD Al_2O_3 can also be a good candidate as high-k gate dielectric for high voltage power

devices. Time-dependent dielectric breakdown (TDDB) behaviors of sputtered AlN and ALD Al_2O_3 is also investigated in this work. A detailed procedure of TDDB analysis is discussed, including the breakdown physics and mechanisms, testing methods, and Weibull statistical distribution. Overall, sputtered AlN can be pursued as an alternative high-k gate dielectric material for MOS technology. Properties such as dielectric constant and breakdown field can be further improved by adjusting the deposition condition or thermal annealing. While work is ongoing, much research is still required for achieving the material's best capability for future electronics.

APPENDIX

Process Sheet 1 **Substrate: n+Si**
Purpose: Study of sputter AlN hard mask

#	Process	Process	Conditions
1	Si Substrate Cleaning	Solvent clean	Acetone and methanol with sonication, DI rinse+N2 blow
2	Optical Microscope	Check profile	
3	Sputter AlN deposition	Deposition	Al target with Ar/N2 =15/15sccm, 300C, 3m Torr, DC 400W
4	Lithography for 'source region' trenches	Spin resist (SPR2020)	6000 rpm, 2000 ramp, 60s
5		Soft bake	100C, 60 sec
6		ABM contact aligner	Exposure time 4.2 s
7		PEB	110C, 60 sec
8		Development	AZ-726 MIF, 70 sec, RT
9		Rinse	DI 30 sec+N2 blow
10			check patterns
11		Descum	O_2=42 sccm, 20mTorr, RIE = 100W, 3 mins (mode 3)
12	Cr/Ni EB evaporation	Cr (50nm)	Density: 7.2, Z-Ratio:0.305, Tooling Factor:72
13		Ni (70nm)	Density: 8.91, Z-Ratio:0.331, Tooling Factor:66
14	Cr/Ni Lift off	Lift off	Remover 1165, 5mins sonication, DI rinse
15		Solvent clean	Acetone and methanol with sonication, DI rinse+N2 blow
16			check patterns
17		Descum	O_2=42 sccm, 20mTorr, RIE = 500W, 2 mins (mode 3)
18	Dry etching for AlN	ICP-RIE etching (PT-770)	Xing1, BCl_3/Ar/Cl_2=10/10/20 sccm, 6 mTorr, RIE/ICP = 20/250 W, DC: 90 V

Process Sheet 2 **Substrate: n+Si**
Purpose: MIM Capacitor Gen-1

#	Process	Process	Conditions
1	Si Substrate Cleaning	Solvent clean	Acetone and methanol with sonication, DI rinse+N2 blow
2	Optical Microscope	Check profile	
3	Metal sputter deposition	Ti(10nm)	Ti target, Ar flow 30sccm, 300C, 3m Torr, DC 400W, presputter 20seconds
4		Al (100nm)	Al target, Ar flow 30sccm, 300C, 3m Torr, DC 400W, presputter 20seconds
5		Pt (70nm)	Pt target, Ar flow 30sccm, 300C, 20m Torr, DC 400W, presputter 20seconds
6	Dielectric layer deposition (for different devices)	Sputter AlN	Al target with Ar/N2 =15/15sccm, 300C, 3m Torr, DC 400W
7		PECVD SiO2	SiH4/N2O=50/900sccm, 350C, 10 W, 1500 mTorr, season 2min
8		PECVD SiNx	LF SiNx, 300C, 1600mTorr, Silane/NH3/N2=20/30/1425sccm, 160W, season 2min, first step 5min for temperature stabilizat
9		ALD Al2O3	Plasma Al2O3 300C, Season 2min
10	Lithography for dielectric etching	Spin resist (S1813)	4000 rmp, 1000 ramp rate, 60s
11		Remove edge resist	Acetone with swab
12		Soft bake	90C, 1min
13		Development	AZ-726 MIF, 40 sec, RT
14		Rinse	DI 30 sec+N2 blow
15		Descum	O_2=42 sccm, 20mTorr, RIE = 100W, 3 mins (mode 3)
16	Dielectric etching (for different devices)	Sputter AlN etching	Hot phosphoric acid (80%), 70C, 20% over etch
17		PECVD SiO2 etching	6:1 BOE, 20% over etch
18		PECVD SiNx etching	6:1 BOE, 20% over etch
19		ALD Al2O3 etching	Pt770, Bsong2, BCl3/Ar=40/10sccm, 5mTorr,RF1 40W, RF2 600W, 20% over etch
20	PR removal	Remove photoresist	Hot 1165, 80C, 20 mins
21		Cleaning	Acetone and methanol with sonication, DI rinse+N2 blow
22	Metal anode EB evapoatation	Ti (50nm)	Shadow mask
23		Au (50nm)	Shadow mask

Process Sheet 3 **Substrate: n+Si**
Purpose: MIM Capacitor Gen-2

#	Process	Process	Conditions
1	Si Substrate Cleaning	Solvent clean	Acetone and methanol with sonication, DI rinse+N2 blow
2	Optical Microscope	Check profile	
3	Metal sputter deposition	Ti(10nm)	Ti target, Ar flow 30sccm, 300C, 3m Torr, DC 400W, presputter 20seconds
4		Al (150nm)	Al target, Ar flow 30sccm, 300C, 3m Torr, DC 400W, presputter 20seconds
5	Dielectric deposition	PECVD SiO2	SiH4/N2O=50/900sccm, 350C, 10 W, 1500 mTorr, season 2min
6		PECVD SiNx	LF SiNx, 300C, 1600mTorr, Silane/NH3/N2=20/30/1425sccm, 160W, season 2min, first step 5min for temperature stabilizat
7	Lithography for anodes	spin resist (AZ 2020)	6000 rpm 6000 ramp rate, 60s
8		soft bake	115 °C, 60 sec
9		exposure(AS200)	exposure time: 0.2
10		PEB	115 °C, 60 sec
11		development	MIF 726 RT, 100 sec
12		rinse	DI 30 sec+N_2 blow
13			check patterns
14		descum	O2=42 sccm, 20mTorr, RIE = 100W, 2 mins (mode 3)
15	Metal anode EB evaporation	Cr (50nm)	Density: 7.2, Z-Ratio:0.305, Tooling Factor:72
16		Ni (70nm)	Density: 8.91, Z-Ratio:0.331, Tooling Factor:66
17	Metal anode Lift off	Lift off	Remover 1165, 5mins sonication, DI rinse
18		Solvent clean	Acetone and methanol with sonication, DI rinse+N2 blow
19			check patterns
20		Descum	O_2=42 sccm, 20mTorr, RIE = 500W, 2 mins (mode 3)
21	Etching for dielectric	PECVD SiO2 etching	6:1 BOE, 20% over etch
22		PECVD SiNx etching	6:1 BOE, 20% over etch

Process Sheet 4 **Substrate: n+Si**
Purpose: MIS Capacitor Gen-1

#	Process	Process	Conditions
1	Si Substrate Cleaning	Solvent clean	Acetone and methanol with sonication, DI rinse+N2 blow
2	Optical Microscope	Check profile	
3	Metal back contact EB evaporation	Ti (50nm)	
4		Au (100nm)	
5	Dielectric layer deposition (for different devices)	Sputter AlN	Al target with Ar/N2 =15/15sccm, 300C, 3m Torr, DC 400W
6		PECVD SiO2	SiH4/N2O=50/900sccm, 350C, 10 W, 1500 mTorr, season 2min
7		PECVD SiNx	LF SiNx, 300C, 1600mTorr, Silane/NH3/N2=20/30/1425sccm, 160W, season 2min, first step 5min for temperature stabilizat
8		ALD Al2O3	Plasma Al2O3 300C, Season 2min
9	Cr EB evaporation	Cr (50nm)	Density: 7.2, Z-Ratio:0.305, Tooling Factor:72
10	Lithography for Cr anode	spin resist(SPR700)	6000 rpm, 45s
11		pre baking	95C, 60 sec
12		exposure(AS200)	exposure time 0.2 sec
13		PEB	115 °C, 60 sec
14		development	726 MIF (TMAH 2.38 %): 60 sec@RT
15		rinse	DI 30 sec+N_2 blow
16			check patterns
17		descum	O2=42 sccm, 20mTorr, RIE = 100W, 2 mins (mode 3)
18	Cr dry etching	Cr etch	Xing 6, Cl2/O2=36/4sccm, 4mTorr, 15/300W, DC:90V
19	PR removal	Remove photoresist	Hot 1165, 80C, 20 mins
20		Cleaning	Acetone and methanol with sonication, DI rinse+N2 blow