Advancements in Design and Application of Microfluidic Devices to Study Cell Migration in Confined Environments

A Thesis

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Biomedical Engineering

by

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ABSTRACT

For multicellular organisms, cell migration can act as a double-edged sword. While being vital for wound repair, immune responses and embryonic development, wayward cells may also disrupt essential biological processes that may detrimentally affect the long-term survival of a life form. This is particularly true for the ability of metastatic cancer cells to translocate from the primary tumor and colonize into surrounding distant tissues and organs. Metastatic cancer cells are able to force themselves through tight interstitial spaces of only 1-30 μm in diameter. This squeezing through such confined spaces can induce an enormous amount of physical stress upon the nucleus of a cell, leading to nuclear envelope ruptures, chromatin herniation, and significant DNA damage. To study these processes in more detail, we created a microfluidic device that modeled the tight three-dimensional constrictions that metastatic cancer cells may encounter during local and distant invasion. The device gave researchers a high-throughput method for observing what short and longer-term effects mechanically induced nuclear deformation had on the cell's nucleus. Originally, we constructed our intricate PDMS microfluidic devices from SU-8 molds, which lacked reliability and inconsistently reproduced the most critical features of our designs. To improve our yield, I shifted our nanofabrication process to the deep-reactive-ion etching (DRIE) and reactive-ion etching (RIE) of silicon. This revised approach has enabled us to improve the fidelity of our critical features, while also reducing the fabrication time and costs. The precision of silicon etching has opened doors for creating more complex microfluidic designs and other novel ideas. For example, we recently created a set of five devices that mimic different densities of the extracellular collagen fiber networks that form in many tissues. These devices are now finding use in the study of cancer cell migration and immune cell motility in confined spaces.

Developing work has involved the use of etched transparent substrates in hopes of creating a reusable device. Instead of holes for PDMS, an inverse design of etched standing pillars in fused silica could become the second generation of our migration devices. We also have explored the use of fluorinated ethylene propylene FEP Teflon as a substitute for PDMS molded devices. Nanoimprinted FEP has a reflective index near that of water and could give our devices the capability of super-resolution microscopy. Over the past three years, I have improved and expanded the fabrication of these novel cell migration devices and left future group members a reliable template for furthering their research.

BIOGRAPHICAL SKETCH

The author was born in Norwich, New York on June 19, 1973 and obtained a BS degree in Biology in 1995 at the State University of New York at Oneonta. After working eight years as an analytical chemist in the environmental and material science fields, Aaron started working at Cornell University in 2004. He is currently a Thin-film Process Engineer at the Cornell NanoScale Facility (CNF). After seven years of taking classes extramurally, he decided to pursue a Master in Science degree in Biomedical Engineering through Cornell's Employee Degree Program.

ACKNOWLEDGEMENTS

I wish to express my appreciation to Don Tennant, Dan Ralph, Chris Ober and the current and former staff at the Cornell NanoScale Facility for giving me the opportunity to pursue a degree while working full-time, along with Jan Lammerding, and Chris Schaffer for taking a chance on me. I would like to thank my wife and kids for putting up with nine years of late nights and missed dinners. Thanks also go to Maureen Brull and Belinda Ann Floyd for handling all the confusing paperwork that this degree involved and for Mingming Wu for being on my special committee.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

For decades, cell biologists have relied on two-dimensional (2D) migration assays for their convenience and seamless integration with many common imaging tools (Wu, Gilkes and Wirtz, 2018). While being impactful in the field of cell biology, 2D studies are limiting for studying cancer cell migration (Van Horssen et al., 2010). These assays only accounted for the frictional forces between the cell and the substrate, which does not accurately depict how a cancer cell moves *in vivo* (Lautscham et al., 2015). In order for cells to move throughout the body, they must overcome ever-changing three-dimensional (3D) matrixes of different compositions, pore sizes and stiffnesses. This desire to replicate cell motility was the driving force for creating 3D cell migration platforms. Many porous *in vitro* 3D environments are constructed from cell-derived matrixes or semisolid biocompatible materials such as collagen or hydrogels. Boyden chambers and other transwell migration/invasion assays influence migration by using chemical attractant to lure cells across membranes or extracellular matrices (ECM) of specific pore sizes. Although effective, the optical interference created by ECM combined with the frequent perpendicular nature of cell migration made time-lapse and live cell imaging problematic and complex (Justus et al., 2014). In hopes of improving imaging quality along with throughput, many researchers started utilizing the tools from the microelectronics industry in order to create confined microfluidic migration devices. Some groups combined microfluidic channels with ECM scaffolding while others chose to forgo the biological component altogether and mimic pores and constrictions with biocompatible materials (Anguiano et al., 2017). One such collection of devices developed by the Lammerding group (Davidson et al., 2015) were able to precisely reproduce 3D narrow

constrictions from polydimethylsiloxane (PDMS) to observe the mechanical affects migrating has on cells and their organelles and more specifically nucleus and its nuclear envelope. Not only do these novel devices support a wide range of cell lines, but they also have provided high-quality fluorescence imaging of nuclear lamina bucking, chromatin strain, DNA damage and nuclear rupture/blebbing and repair (Davidson et al., 2015).

What soon happens after any successful publication are new ideas, applications and demands from other collaborators using the technology. From the fabrication standpoint, this should include an honest assessment of performance to benefit future work. This may involve correcting nagging flaws, increasing the yield of successful devices and developing newer innovative designs. This paper will demonstrate the fabrication improvements made on the original cell migration devices by switching design software and utilizing different nanofabrication capabilities. In particular, I developed a “Top-Down” approach for reliably fabricating the 1-3µm constrictions throughout not only a single migration device, but across a full wafer of devices. From this approach came the ability to fabricate a new set of cell migration devices that mimic different densities of collagen. Other work highlighted in this thesis will involve the use of different substrate platforms, methods for cleaning/reusing devices, nanoimprinting and what may be the next generation of our migration devices.

1.2 Background

Cells migrate in response to events and signaling (Vicente-Manzanares, 2005). Some responses are beneficial such as the formation of layers in an embryo for future tissue and organ development or the migratory response to environmental cues neutrophils take for wound healing. Sometimes these pathways falter and signaling may become abnormal or misinterpreted in a way that can be detrimental to the organism. Rheumatoid arthritis and other autoimmune diseases are immune cells homing in on the wrong locations (Luan et al., 2017). The prime example of detrimental cell migration is cancer metastasis or the movement of cancer cells from the primary tumor to generate distant secondary tumors. Cancer metastasis is the leading cause of cancer deaths, but many details about cancer cell survival and colonization are still widely misunderstood (Chaffer & Weinberg, 2011). One area of research on this subject focuses on the mechanics of how these tumor cells can migrate through these extremely tight interstitial spaces without suffering significant damage or apoptosis. For a cell, the nucleus is the limiting factor for passing through a small constriction. The nucleus is the stiffest and largest organelle (Mcgregor et al., 2016) and has to withstand a remarkable amount of deformation to pass through tight 3D spaces. The nuclear envelope encases and separates all the genetic material from the surrounding cytoplasm. The nuclear envelope (Figure 1-1) consists of two lipid bilayers; an outer nuclear membrane (ONM) faces the cytoplasm and the cytoskeletal filaments and an inner nuclear membrane (INM) that surrounds the chromatin. Both membranes are joined at nuclear pore complexes creating 30-50nm of perinuclear space between the bilayers. The outer surface of the INM is covered with a crowded meshwork of different lamin proteins called the nuclear lamina which interacts with the chromatin and plays a significant role in the structural strength and deformability of the nucleus (Davidson & Lammerding, 2014). Recent studies

have brought to light the importance that chromatin condensation has on the mechanical properties of the nucleus (Gerlitz & Bustin, 2011). Two proteins form the LINC complex that links or tethers the nucleoskeleton to the cytoskeleton elements are across the nuclear membrane. The SUN (Sad1p and UNC-84) domain proteins interact with lamin proteins through the INM and binds with KASH (Klarsicht, Anc-1, Syne-1 homology) domain proteins within the perinuclear space. KASH interacts through the ONM with actin filaments, cytoskeletal crosslinker protein plectin and microtubules motor proteins dynein and kinesin in the cytoplasmic region.

Previous work examining the mechanical effects that varying collagen pore sizes had on different migrating cell lines (Wolf et al., 2013) inspired this novel 3D cell migration device. As mentioned in the motivation section, fabricating these migration devices features gives the researcher greater command and experimental control of their work. Precise and reproducible PDMS molded constrictions in the horizontal plane would supplant collagen pore size variability and drastically improve our imaging capabilities. Figure 1-2 illustrates the four essential components of our cell migration devices; 1) reservoirs for cell culture media, 2) wells for loading cells into the device, 3) a constriction channel between two chambers for imaging our cell assays and 4) the bypass channel for equalizing the chemotactic gradient.

Each migration device consists of two reservoirs that overlap opposite chambers for loading cell culture media. Different concentrations of a chemical attractant will initiate cell movement from the sink reservoir, through the constriction pathway and towards the source reservoir on the other side (Figure 1-3). We used a 6 mm diameter Harris Uni-Core Biopsy punch (Harris Uni-core, Ted Pella, Inc.) and fabricated 200-250 μm tall alignment marks to accurately reproduce the diameter and location of each reservoir. Cell-loading ports located

on the sink reservoir side also used specific punch sizes (0.75 & 1.25 mm) and location parameters. One of the attributes of this design is the accessibility of loading cells into and recovering cells after they passed through the channel. The bypass channel helps establish the chemotactic gradient between the sink and source reservoirs by quickly equilibrating the fluid levels. This in turn, controls the flow of fluid through the constriction channel. Engineering this fluid balance reduced the gradient equilibrium times and opened up the possibilities for long term imaging (Davidson et al., 2015).

The criteria for the constriction channel were to engineer (1-3 μm) interstitial spaces in a clear imaging area for observing cell migration and its mechanical effects on the cell's nucleus. After many tests and iterations (Davidson et al., 2015), the group decided on a design of three rows of PDMS pillars (Figure 1-4). A row consists of thirteen closely packed circular pillars of the same diameter. Each vertical pillar is separated by 30 μm from center-to-center. By varying the pillar diameters from 27-29 μm, gaps or constrictions 1-3 μm apart were created. Two rows of rectangular blocks sandwiched the center circular constriction row. From edge-to-edge, the vertical gap between blocks is 15 μm, which is too large to constrict the cell's nuclei, but wide enough to encourage linear cell movement and recovery. The whole channel is divided by horizontal walls into six segments, with each segment containing constrictions of a specific size (Figure 1-5).

Fluorescence reporters were used to visualize cellular events as they happened in real time. Nuclear localization signal sequences tagged with a green fluorescence protein (NLS-GFP) were used in Figure 1-6 to visualize rupturing/blebing of the nuclear envelope and the subsequent leaking of nuclear material into the cytoplasm as breast cancer cell passes through a 2 μm constriction (Denais et al., 2016). Figure 1-7 demonstrates the effects that

low lamin levels have on the nuclear envelope flexibility (Mekhdjian et al., 2017). Low lamin expression in some types of cancer may influence the deformability of their nuclear envelopes, giving these cells a possible migration advantage (Lammerding et al., 2006) and has also been linked to poor cancer patient prognosis (McGregor et al., 2016). In Figure 1-8, red fluorescent protein RFP-53BP1 was used to detect double stranded DNA breaks as an indicator for possible DNA damage. Fluorescence reporters have been used for labeling many other factors and proteins involved nuclear envelope damage.

The actual nanofabrication comes from creating a PDMS mold for the migration devices. The device consists of two fabricated layers of different heights; a 5 µm layer with the constrictions and a 250 µm layer for the rest of the device (cell chambers, bypass channels and alignment marks for the reservoirs and ports). The mold is an inverse of the actual PDMS device, so patterned 27-29 µm diameter holes were fabricated in order to cast pillars. Other than the punched reservoirs and ports, all the other features are molded from PDMS. The original molds were composed of two layers of SU-8 with the 5 µm layer spun before the 250 µm layer. The migration devices were made in pairs with twelve device pairs patterned on a 4" silicon wafer (Figure 1-9). These pairs are cut out of the PDMS, cleaned and plasma treated to produce a permanent covalent bond with a glass cover slip (Figure 1-10). Prior to seeding cells and filling cell media reservoirs, the device is functionalized with ECM proteins before incubation and later live-cell analysis and florescence imaging (Keys et al., 2018).

These cell migration devices are heavily used in Lammerding Lab which involves repeated PDMS molding from the same SU-8 master wafer. The group was having difficulties accurately fabricating the SU-8 5µm constriction channel dimensions. Poor fabrication yield

combined with SU-8 adhesions issues were starting to hold up research efforts. The group wisely resorted to creating plastic molds of successful SU-8 master wafers for PDMS molding (Figure 1-10), but this was not a solution to the fabrication issues. This thesis will illustrate the use of reactive-ion etching and other fabrications changes made in order to significantly increase the yield and fidelity of PDMS master wafers. These improvements also opened doors to newer designs and devices currently used in the lab.

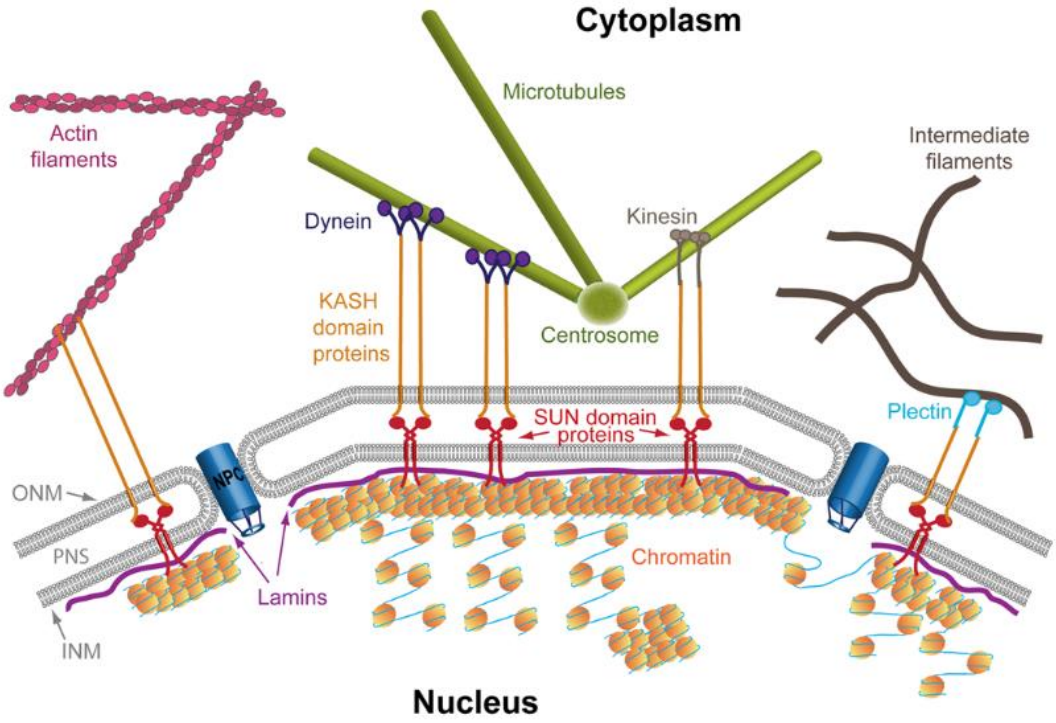


Figure 1-1: Cross-section of the nuclear envelope and its related components (Gerlitz & Bustin, 2011). The nuclear membrane is composed of an outer nuclear membrane (ONM) and an inner nuclear membrane (INM). They connect at the nuclear pore complexes (NPC) forming a perinuclear space (PNS) in-between. INM is lined with the lamina, which interacts with the SUN domain proteins embedded in the PNS. KASH domain proteins combine with the SUN proteins to form the LINC complex, a link between the nucleoskeleton and cytoskeleton.

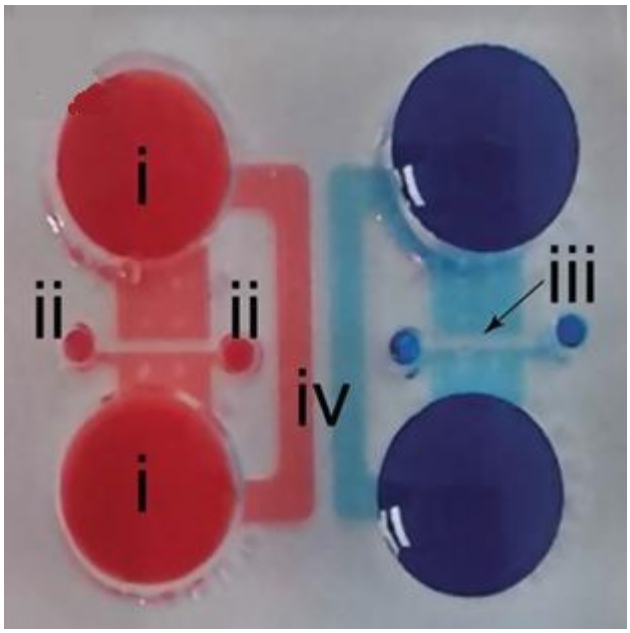


Figure 1-2: Overview of the migration device. Top-down view of migration device, with food coloring added to enhance details. Cell culture media is added into the media reservoirs (i). Cells are seeded into the devices through seeding ports (ii) that lead to the 5-µm-tall area with the constrictions (iii). Larger bypass channels (iv) allow rapid equilibration of media reservoir levels to prevent flow through constrictions, facilitating formation of a chemotactic gradient by diffusion if serum or growth factors are added to one of the reservoirs (Keys et al.,2018).

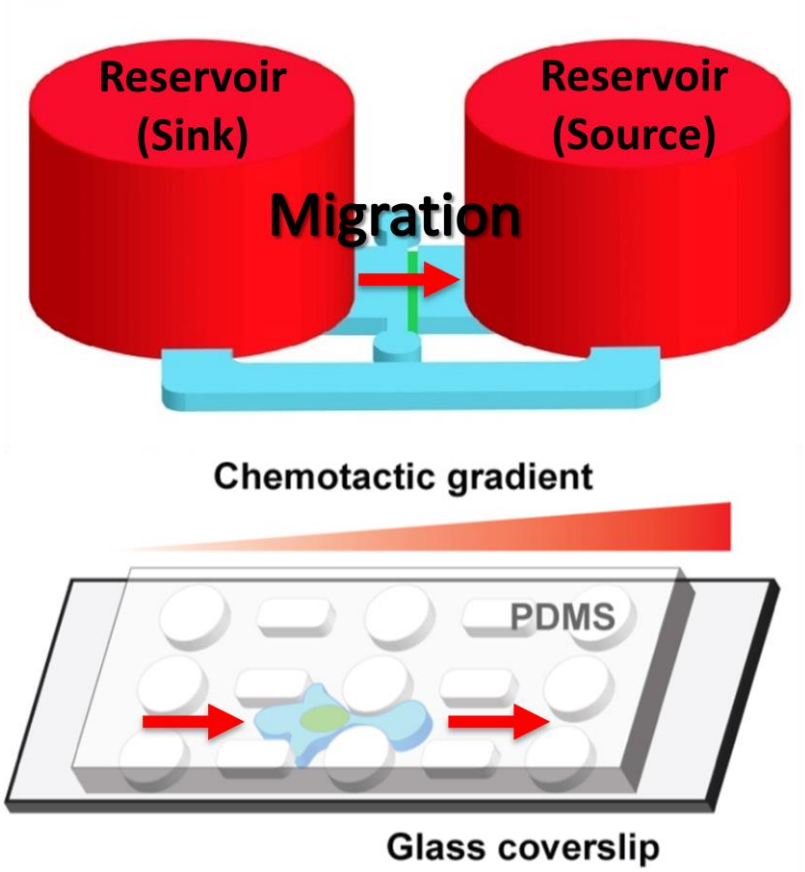


Figure 1-3: Side View of migration device. Top image: Red indicates the PDMS media reservoirs ≈5mm in height. The blue regions are the 200-250 µm tall seeding ports and chambers while the green is the 5 µm constriction channel. Bottom image: An expanded view of the cell constriction channel (Davidson et al, 2015).

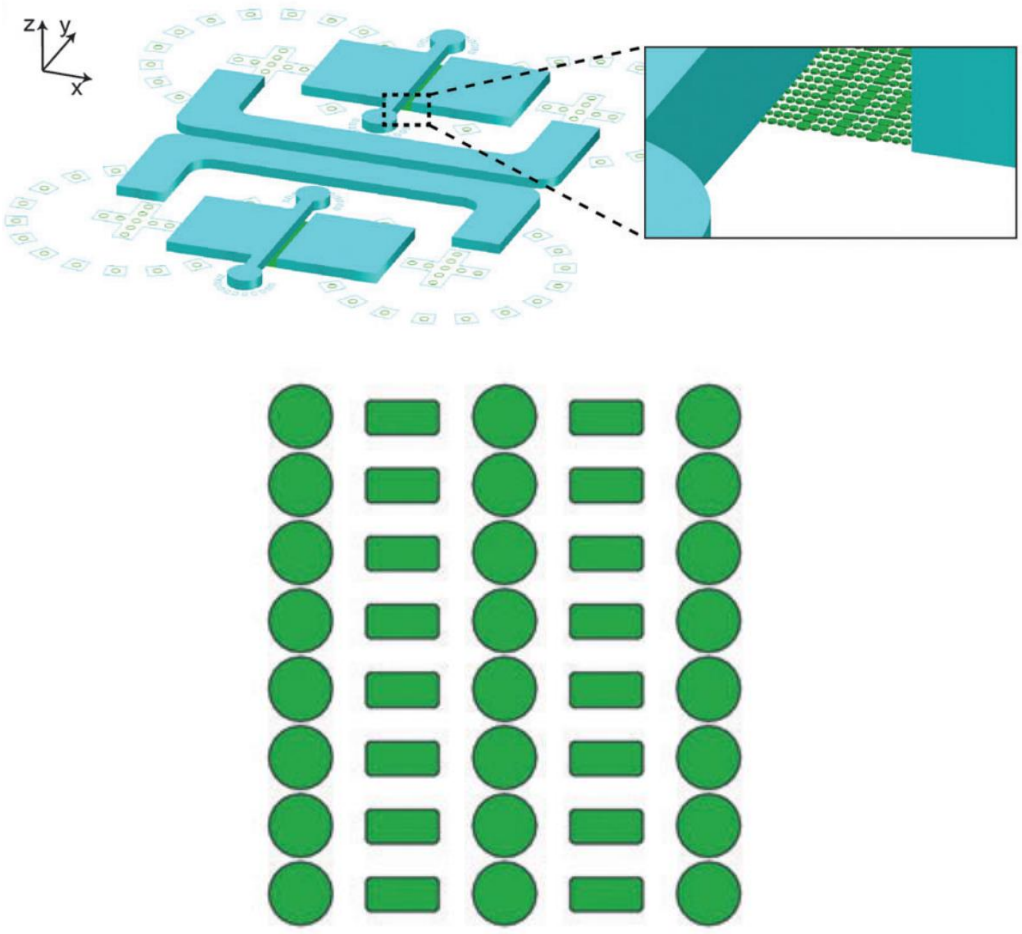


Figure 1-4: The constriction pathway.

Top: The placement of the constriction pathway in our cell migration device.

Bottom: A top down image of the three rows 1-3 µm pillar constrictions and two 15µm rectangular rows between (Davidson et al, 2015).

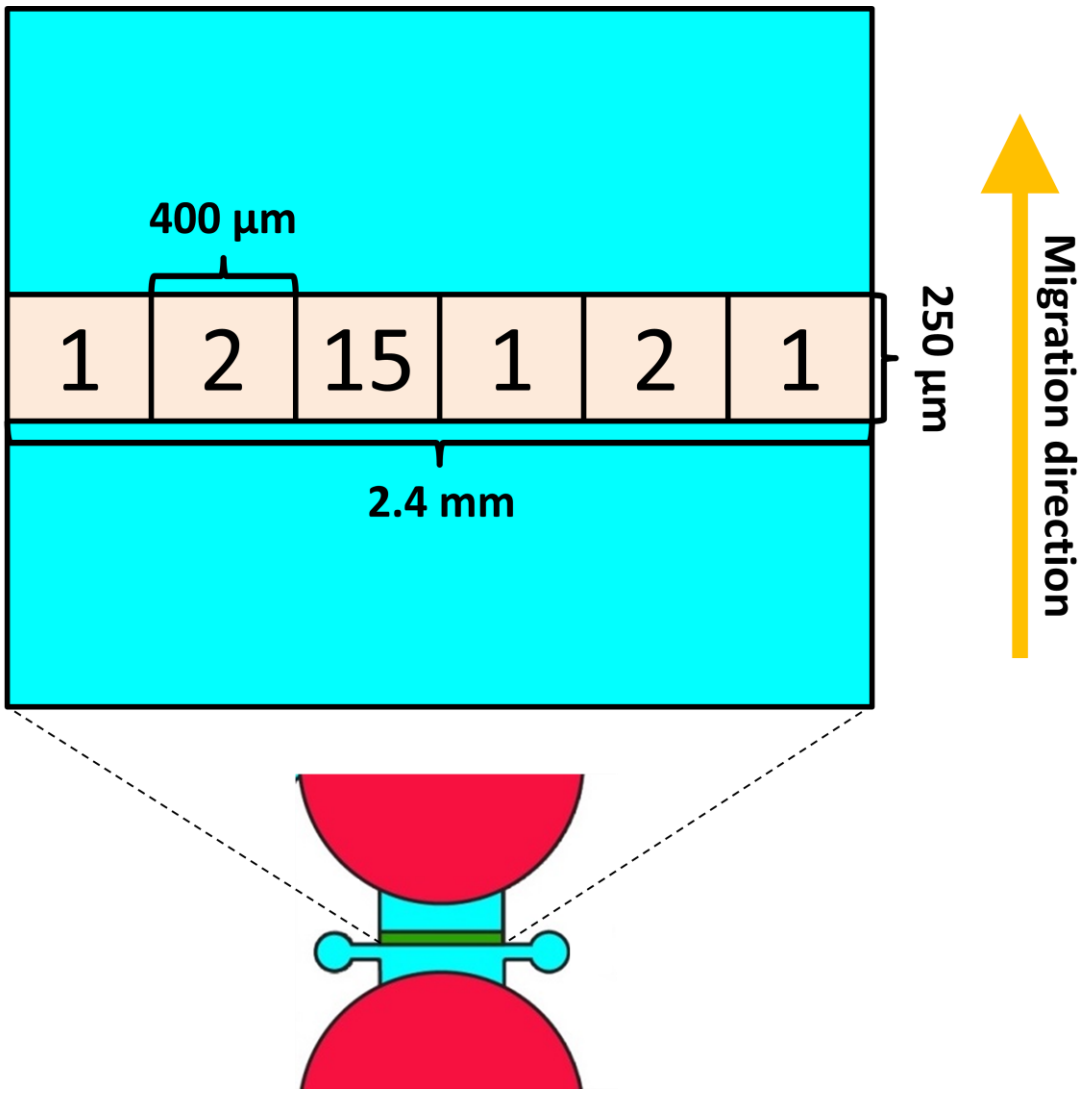


Figure 1-5: An expanded top down image of the seeding ports and constriction channel layout and dimensions (Courtesy of the Lammerding Group).

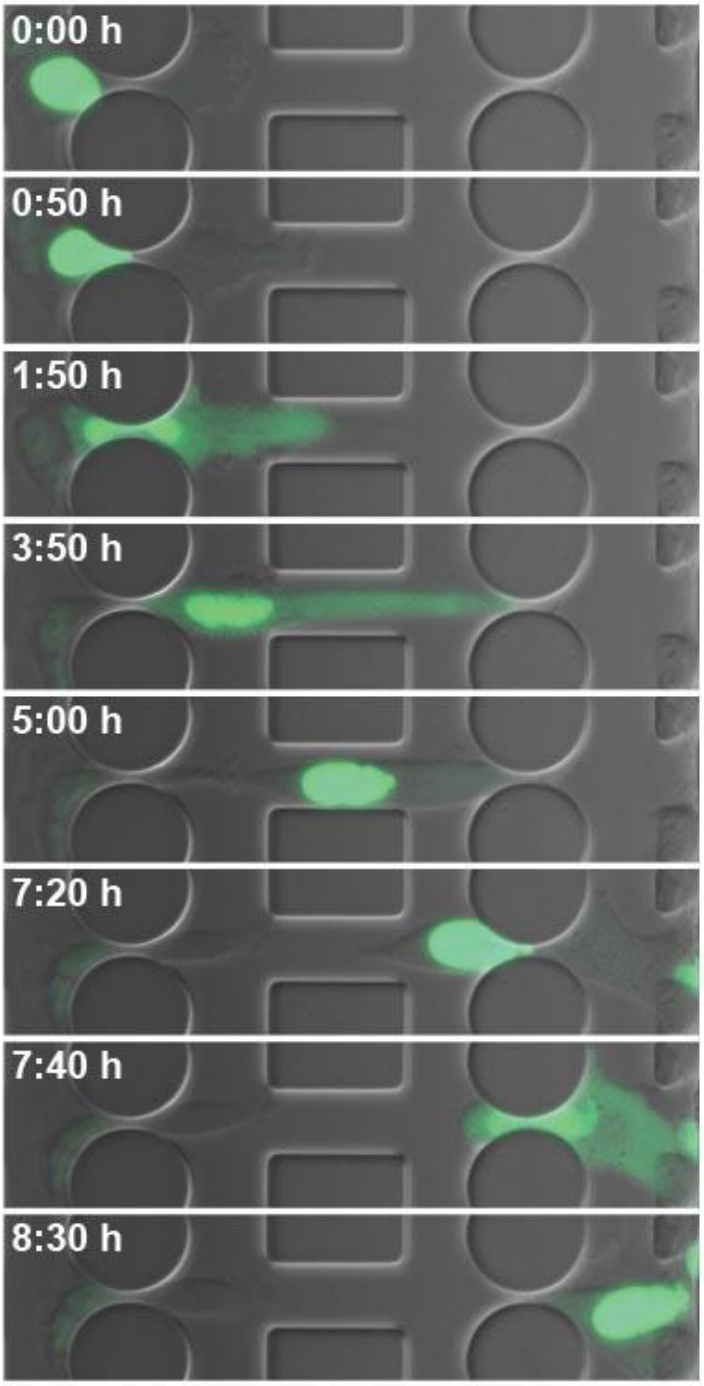


Figure 1-6: A time-lapse sequence of multiple nuclear envelope ruptures as a MDA-MB-231 breast cancer cell moves through 2 x 5 μm^2 microfluidic constrictions. The fluorescent reporter NLS-GFP indicates nuclear envelope blebing and a loss of nuclear material into the cytoplasm (Courtesy of the Lammerding Group).

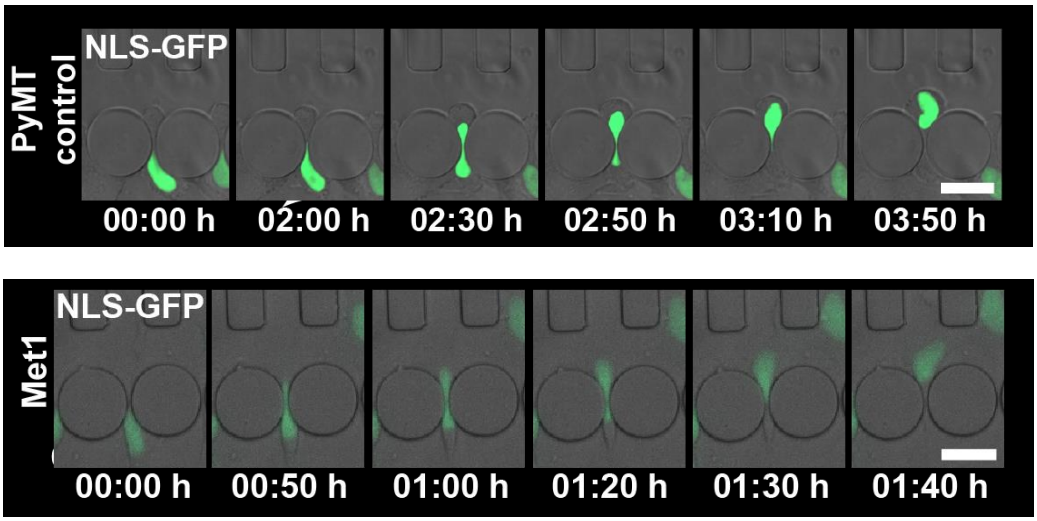


Figure 1-7: A comparison between a control with normal lamin levels (top) metastatic cell with low lamin levels (bottom) as migrate through a 1 x 5 µm^2 confined space constriction (Mekhdjian et al., 2017).

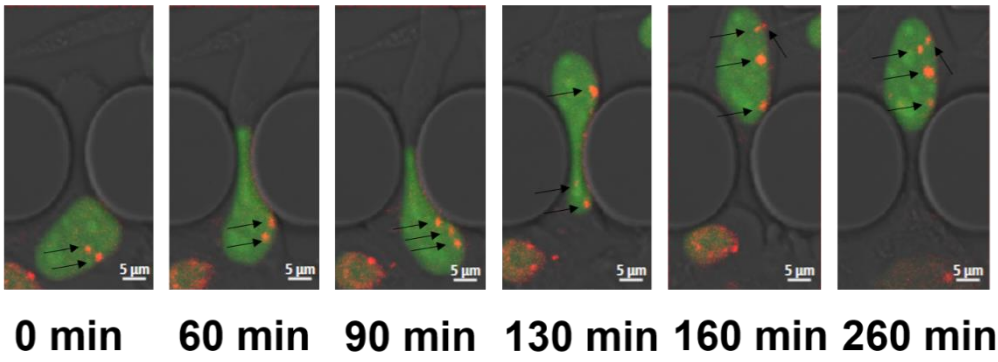


Figure 1-8: An increase in DNA damage (red 53BP1-mCherry) caused by mechanical deformation of the nucleus (green NLScopGFP) in MDA-MB-231 cell after passing through a 2 x 5µm2 confined space constriction (Courtesy of Prayga Singh and the Lammerding Group).

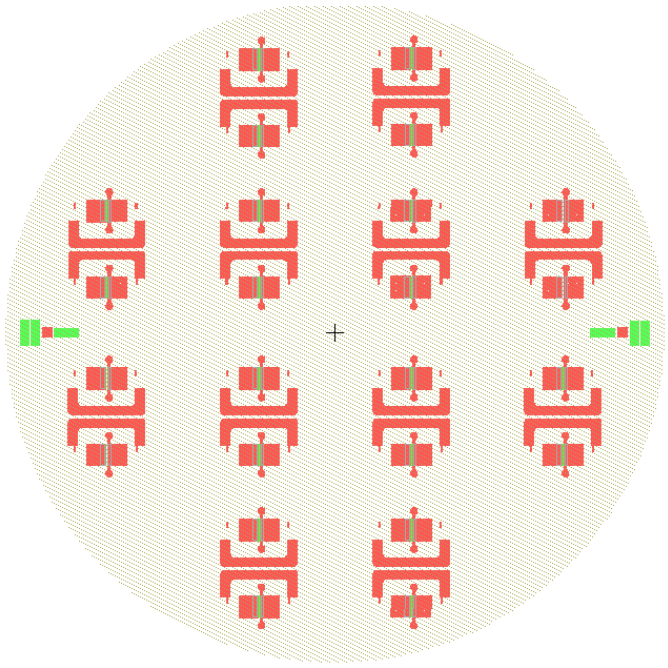


Figure 1- 9: Full four-inch wafer map of twelve pairs of cell migration devices.

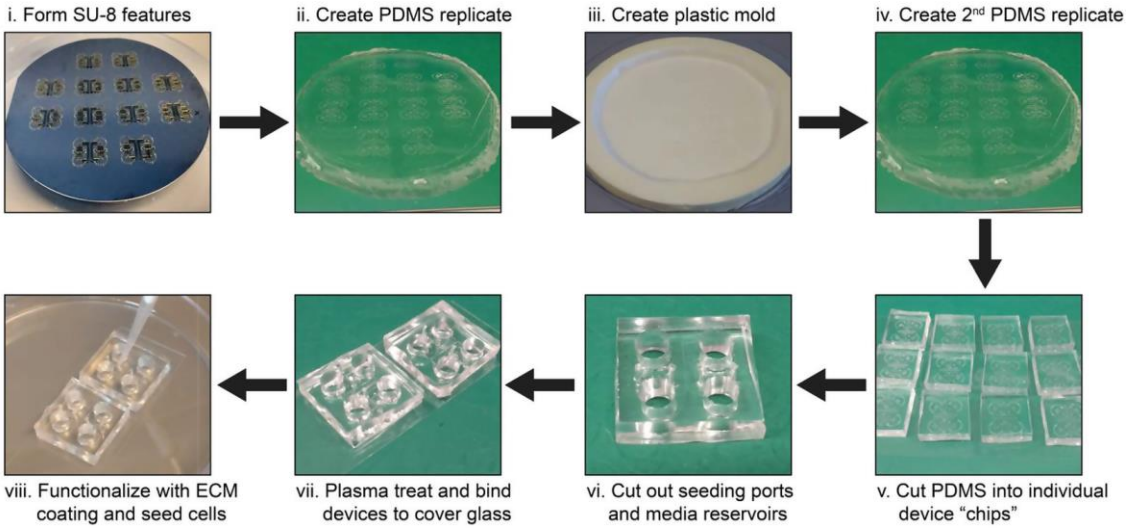


Figure 1-10: An overview of the PDMS molding and migration device preparation after the fabrication of the SU-8 master (Keys et al., 2018).

CHAPTER 2

ADVANCES IN CONSTRICTION CHANNEL DESIGN

2.1 First Round of New Constriction Designs

Although the original migration device design worked well (Denais et al., 2016), we wanted to implement some additional designs with the goal to add more constrictions to increase the frequency of nuclear ruptures.

2.2 Design # 1, # 2 and # 3

As shown in Figures 2-1 - 2-5, these three designs were very similar and were intended to present cells with constriction in every direction. Each device had a 1, 2, 3 and 10 µm version. From our early testing, Design # 3 appeared to be the best option (Figure 2-6 & 2.-7), but we soon learned that nine levels of tight constrictions damaged the cells beyond repair. Cells that migrated through the 3 µm constrictions died soon afterwards while cells through the 1 µm constrictions died in the middle of the device. These findings point to the importance that the 15 µm areas served in the original devices for cell recovery and repair.

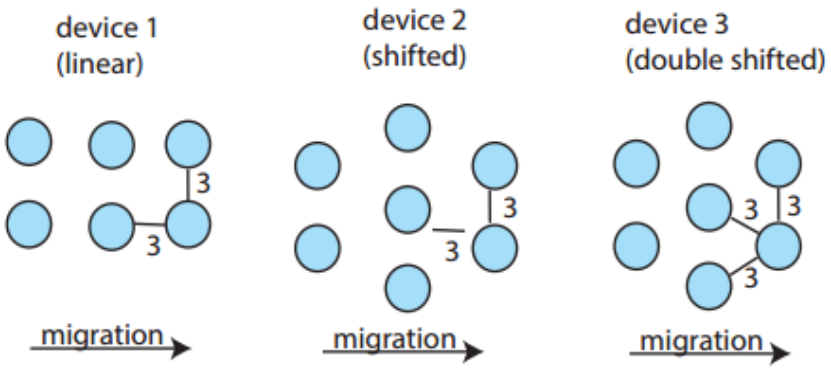
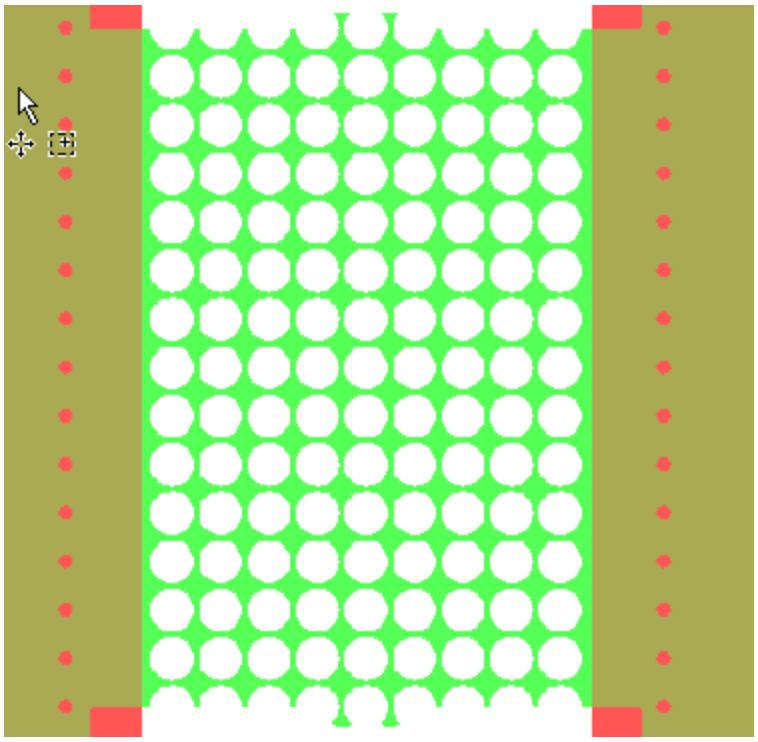
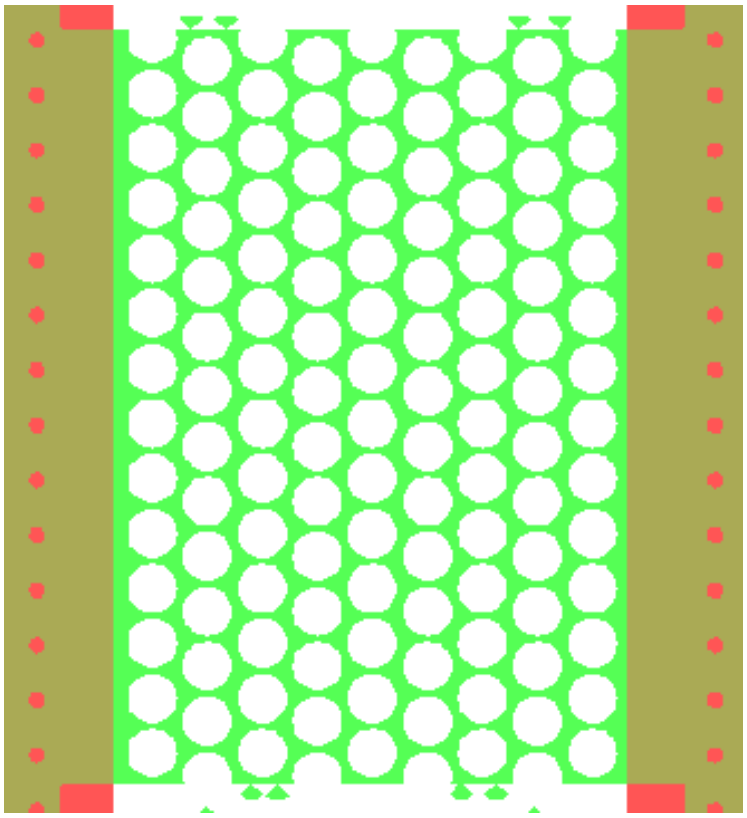


Figure 2-1: Diagrams for the proposed constriction gaps for Devices # 1, # 2 & # 3. Units are in micrometers



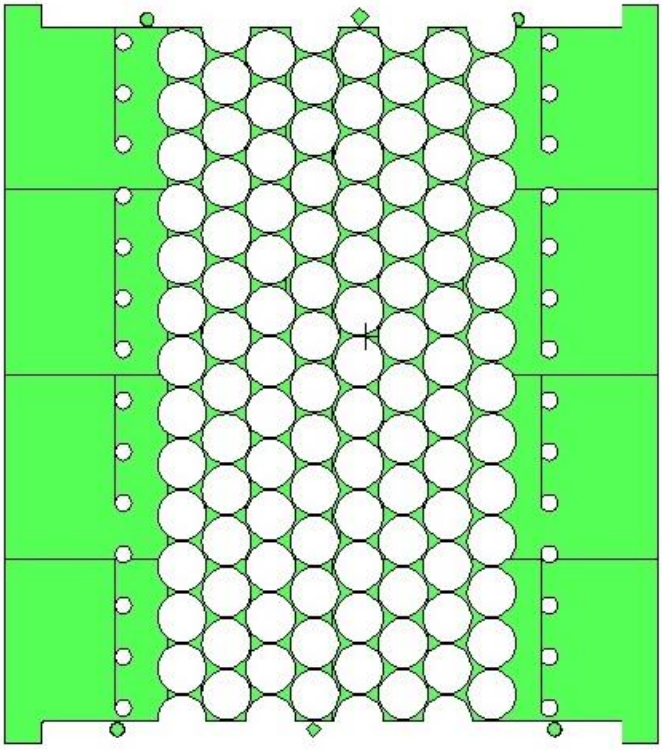
Parameters	X	Y
Delta	30	30
Array	9	14
Translation	30	0

Figure 2-2: CAD layout Design # 1 after boolean subtraction (green) in migration device (red) and L-Edit Coordinates (Parameters explained in Appendix A, section 3.2).



Parameters Left	X	Y
Delta	60	30
Array	5	14
Translation	-120.000	-210.000
Parameters Right	**X**	**Y**
Delta	60	30
Array	4	14
Translation	-90.000	-222.500

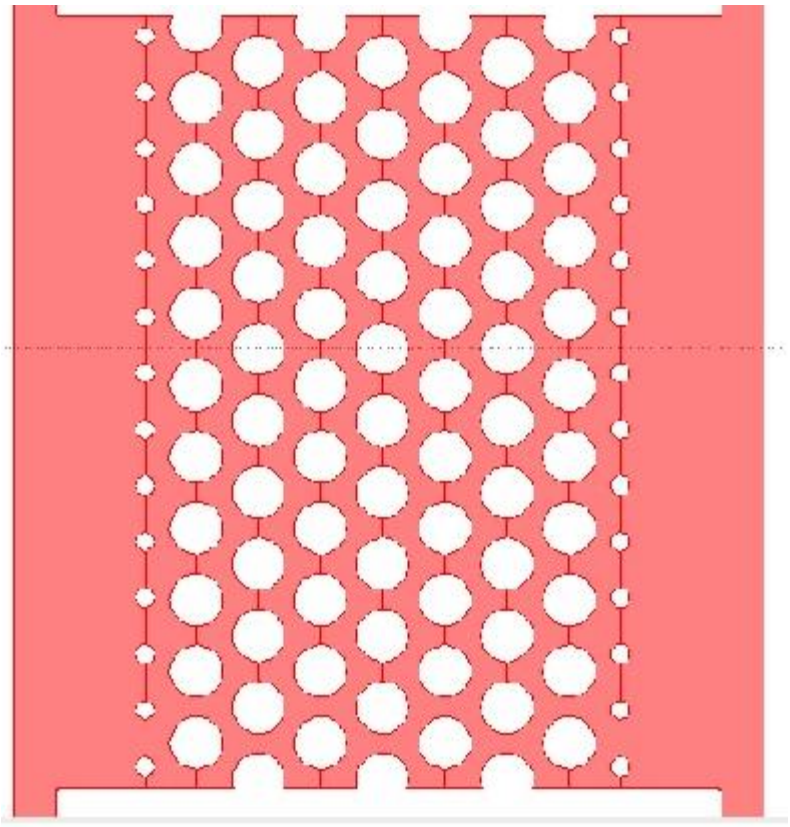
Figure 2-3: CAD layout of Design # 2 after boolean subtraction (green) in migration device (red) and L-Edit Coordinates (Parameters explained in Appendix A, section 3.2). .



Row #1

Parameters Left	X	Y
Delta	52	30
Array	4	14
Translation	-111.000	-224.925
Parameters Right	**X**	**Y**
Delta	52	-224.925
Array	4	14
Translation	-85.000	-210.000

Figure 2-4: Design # 3 CAD after Boolean subtraction on mask # 1 and L-Edit coordinates (Parameters explained in Appendix A, section 3.2).



Parameters Left	X	Y
Delta	-150	-222.500
Array	5	11
Translation	64	37
Parameters Right	**X**	**Y**
Delta	-118	-204.000
Array	4	10
Translation	64	37

Figure 2-5: The control for Design # 3 after LayoutBEAMER Boolean subtraction and L-Edit coordinates (Parameters explained in Appendix A, section 3.2). .

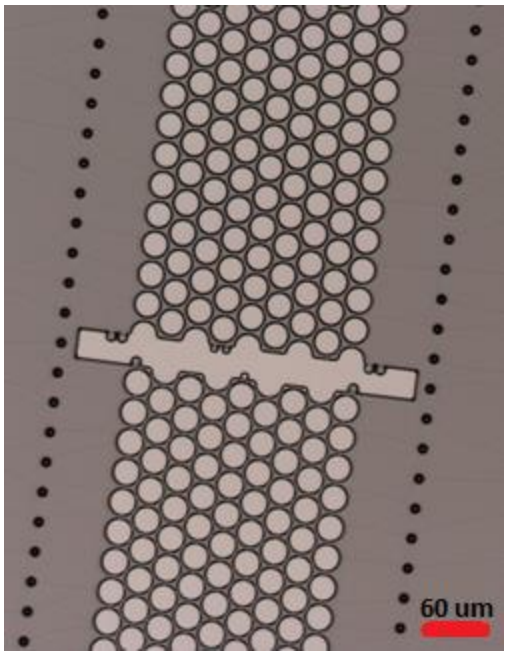


Figure 2-6: Design # 3 composed of 5 µm of SU-8.

Upper 2 µm gaps. Lower 1 µm gaps. (10x).

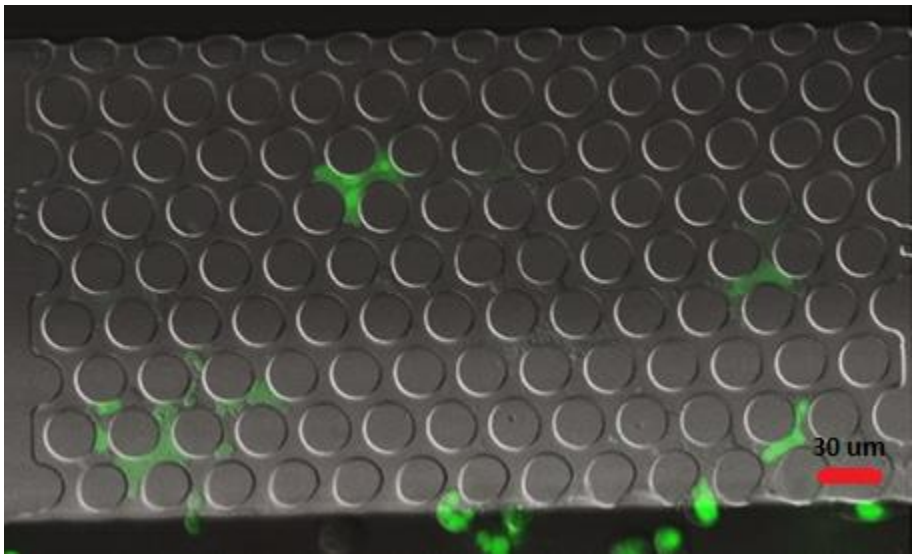


Figure 2-7: Cell moving through a PDMS molded Design # 3 cell migration device.

2.3 Design # 4

Ten rows of constrictions were tapered from 5 µm to 1 µm. The layout was similar to Design #1 (Figure 2-2) with the exception of the pillar diameters increasing from right to left (Figure 2-8). Pillars arranged in this fashion can be used to measure migration speed and presents an effective tool for comparing how different cell lines travel through narrower constrictions (Davidson et al., 2015).

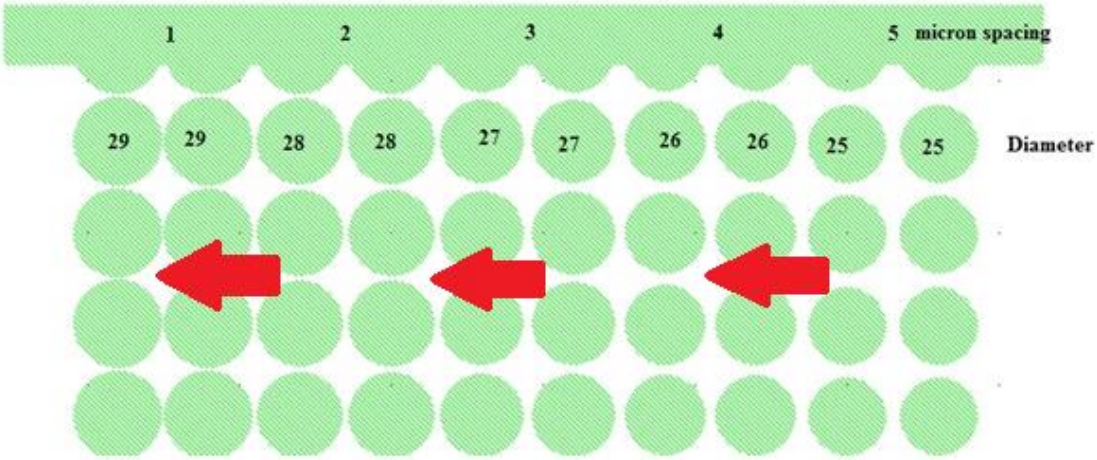


Figure 2-8: CAD layout for Design # 4 before Layout BEAMER Boolean subtraction. Red arrows indicates the migration direction.

2.4 Design # 5

This device has longer constriction channels to study nucleus changes during confined migration. Three different lengths of (10, 15 & 20 µm), 2 µm wide versions were generated along with a 10 µm wide control (Figure 2-9).

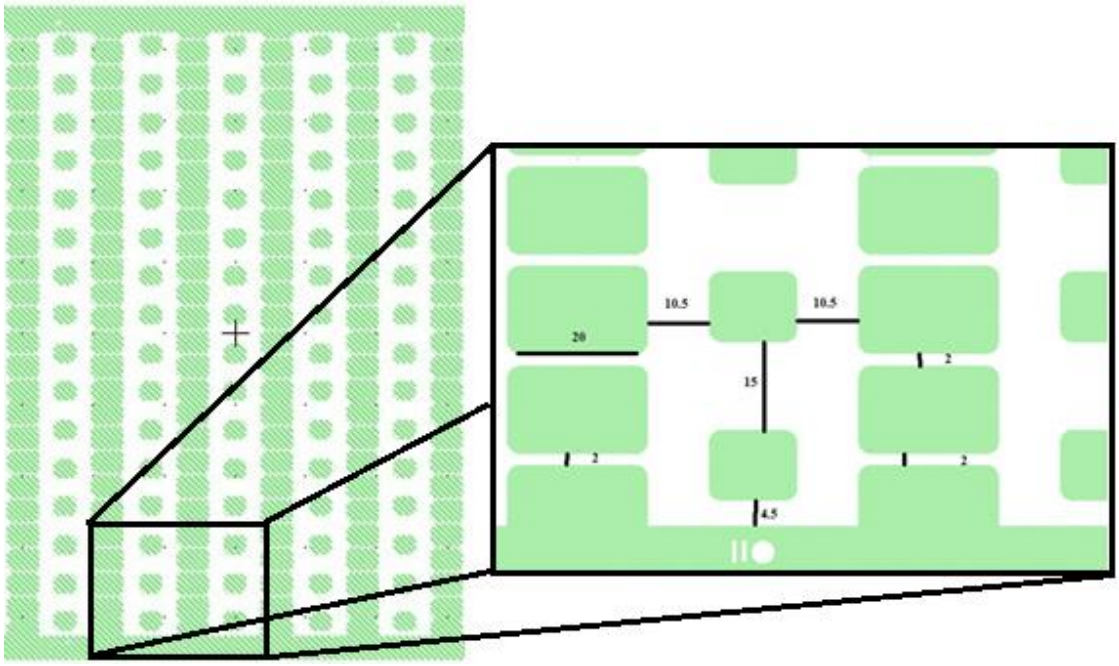


Figure 2-9: CAD layout and blown-up 20 µm version of Design # 5 before the Boolean subtraction. The 2 µm wide channel is 20 µm long with 1 µm chamfers at each end.

2.5 Design # 6

The inspiration for this design came from the structure of collagen matrix. Collagen is fibrous protein that is found in connective tissue, muscle and skin and is the most abundant protein found in the ECM. Researchers have using different densities of collagen for their 3D cell migration and cancer metastasis research for decades (Wolf et al., 2013). While being effective, using collagen for migration studies does have its limitations such as temperature instability and microstructural variability of pore sizes. Collagen/ECM can also be challenging to image in high resolution. Ideally, we desired to create a reproducible microfabricated "field of pillars" of varying gaps for the cells to maneuver through. By doing so, we creating a platform for improved real-time imaging of multiple nuclear rupture events.

To create our collagen mimic device, holes 5 µm in diameter x 5 µm in depth needed to be patterned and replicated in or on top of the substrate. SU-8 2005 was originally used, but the very nature of SU-8 made its use for this application very difficult. Unlike photoresist, that when an under exposure results in an ineffective pattern transfer, underexposed SU-8 will not adhere to the substrate due to a lack of photoacid activation which diminishes post exposure baked crosslinking (Microchem, n.d). This became an issue when replicating this field of closely packed pillars because the shortest possible exposures times produced accurate lithography, but resulted in poor adhesion. Any increase in the length of the exposure improved adhesion, but resulted in constricting the diameter of our holes. We could have designed larger diameter pillars for our array which may have shrunk to 5 µm when over exposed, but this would have only been effective for our "loose" and maybe "midrange" designs where gaps were over 3 µm. A densely packed array of larger pillars or

other close proximity designs would never shrink without creating larger gaps or merging pillars into each other.

We decided that continuing SU-8 fabrication was not suitable to bring these "field of pillars" designs to life and we needed to explore some alternative fabrication processes. As mentioned in the SU-8 and plasma etching sections, better lithography and smaller features can be achieved by using a thinner photoresist. The 1.7 μm thickness of AZ nLof 2020 was thin enough to replicate the 5μm diameter pillars easily while also being thick enough to act as an etch mask for both deep and reactive-ion etching 5μm into silicon. The fact that we could simply use photoresist for pattern transfer and not depend on it as a structural entity was extremely beneficial to our new process.

We considered developing a computer program to generate these fields of pillars, but because this was originally a prototype, a simpler approach was used. Using the criteria for each design (Table 2-1 and Figure 2-10) groups of varying size and shape 5 μm pillar clusters were developed into L-Edit cells and instanced into the ≈342 μm x 400 μm constriction areas (Figure 2-11). As shown in Figures 2-12 & 2-13, five different cells and some individual pillars resemble the layout of a patchwork quilt. The cells were varied so that they could fit well into the design as a whole. Some clusters had only three or four pillars (Figure 2-14) while others had many more (Figures 2-15 & 2-16). Different shaped groupings along with enabling the mirror and rotation features in L-Edit (Figure 2-17) helped to fit the cells within the criteria and further the appearance of randomness. Extra pillars were added into open spaces as needed.

The original Design # 6 consisted of a loose, midrange and dense versions of the field of pillars concept (Table 2-1 and Figures 2-18 – 2-20). All three versions were laid out twice in

each Design # 6 migration device (Figures 2-21 & 2-22) on the original Design # 1-6 prototype wafer (Figure 2-23). What we learned from the early trials was that cells migrated too quickly through the loose version and could not make it through the device in the dense version. The midrange seemed ideal for travel time and for the frequency of nuclear ruptures recorded. We decided to forgo the loose and dense versions and looser and denser versions of the midrange CAD would be created (Figures 2-24 & 2-25). Pillars were removed from the five-midrange clusters for the loose midrange (LM) cell while pillars were added to the clusters for the dense-midrange (DM) cell. For the next wafer, the LM and DM cells replaced the loose and dense cells for the right half of the wafer (six pairs of migration devices) (Figure 2-26). The three pairs of migration devices in the bottom-left corner of the wafer had a different layout. All six segments of each pair were dedicated to only one midrange type. In other words, one device of all LM sections, DM sections and midrange sections. These midrange designs of all the same densities were incorporated on their own wafer (Figure 2-27). We again used the midrange design to fabricate a 1"x 1" square field of pillars (see Appendix J).

After the initial run, we noticed that some of the holes used for molding the 5 µm pillars still contained remnants of the PDMS pillars. We determined that the scalloped-sidewalls from the DRIE etch probably contributed to the broken and missing pillars and smoother sidewalls were needed. From that point on, reactive-ion etching was used for all future constriction fabrication.

Figure 2-28 demonstrates heterochromatin condensation from nuclear confinement detected in cells migrating through this new migration design. Heterochromatin is transcriptionally silent DNA that remains tightly wound around histones. Mechanical forces

on the nucleus increase the trimethylation of lysine 9 on the histone H3 protein sub unit (H3K9me3) (Unpublished work, 2019) which is an indicator for mammalian heterochromatin and gene silencing (Lehnertz et al., 2003). The acetylation of histone H3K9 (H3K9ac) can indicate transcriptionally active euchromatin (Karmodiya et al., 2012). These hallmarks are important because chromatin organization does affect the stiffness and deformability of the nucleus (Tyler & Lammerding, 2018).

Versions of Design # 6	Spacing Between Pillars
Loose	**10-15 µm**
Midrange	**3-10 µm**
Dense	**1-4 µm**

Table 2-1: The criteria for the initial Design # 6

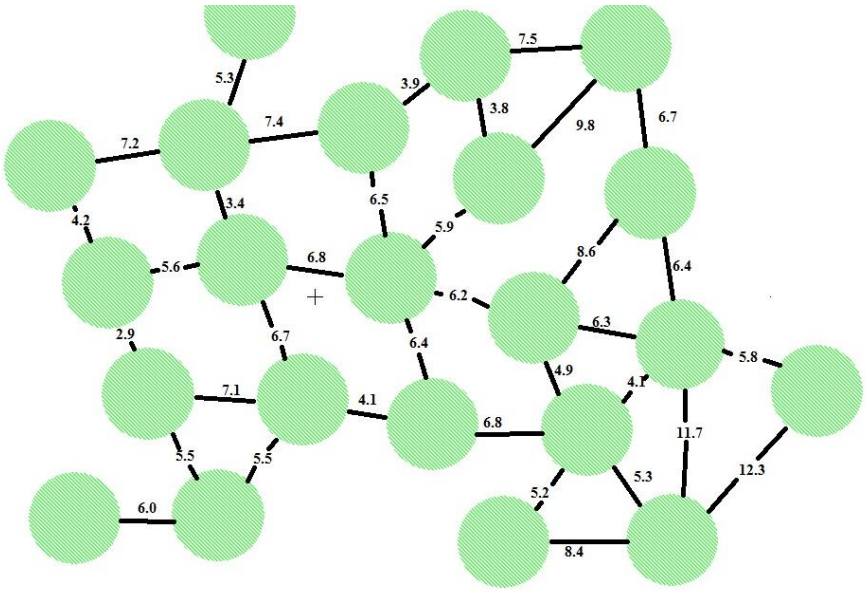


Figure 2-10: An example of the spacing between 5 µm pillars for the Midrange version of design # 6. Values are in micrometers.

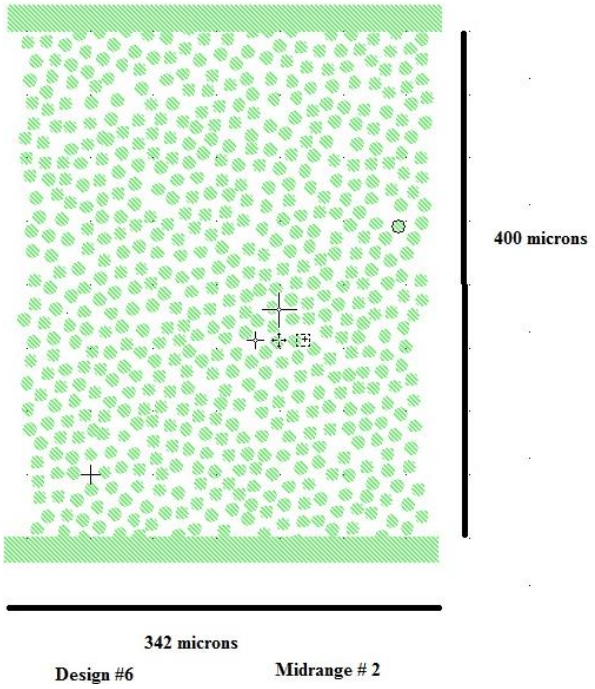


Figure 2-11: The original Midrange Design # 6 CAD with 10 µm instead of 5 µm pillars.

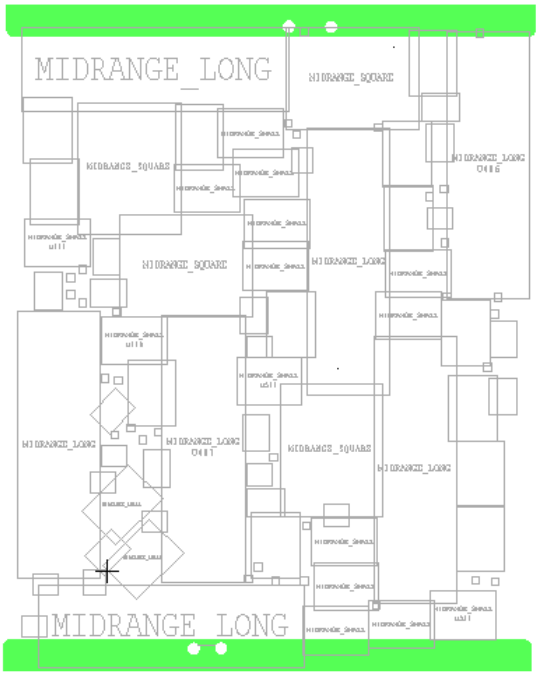


Figure 2-12: The "patchwork" layout for the Midrange version field of Design # 6

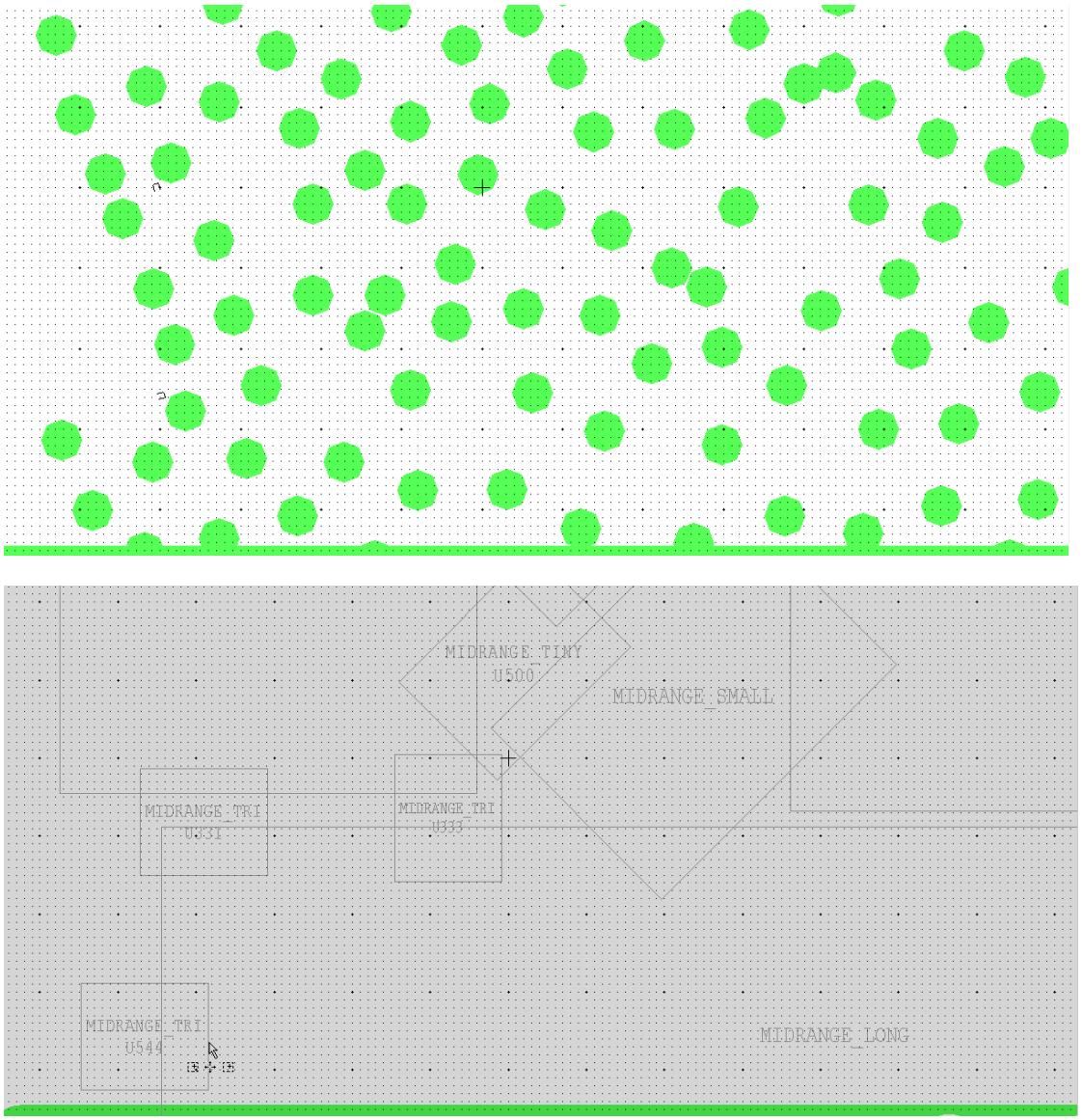


Figure 2-13: An example of the "patchwork" layout. Top: The pillars as seen in L-edit.

Bottom: The pillars hidden with only the instanced cells area shown.

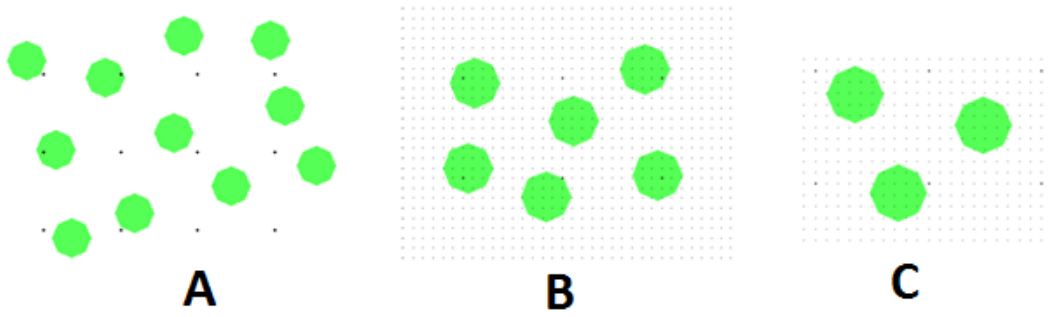


Figure 2-14: Pillar clusters: A) Small, B) Tiny and C) Triangle

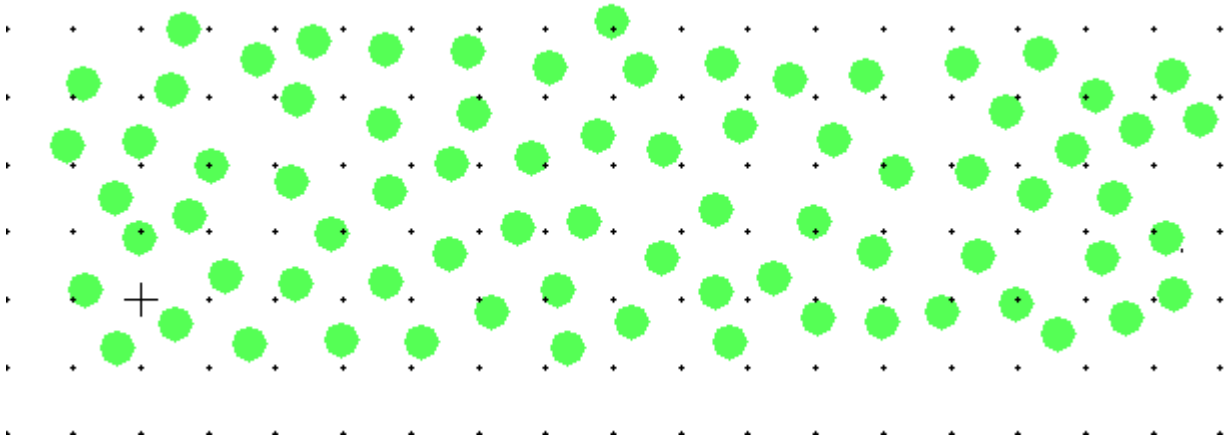


Figure 2-15: Midrange Long Cluster

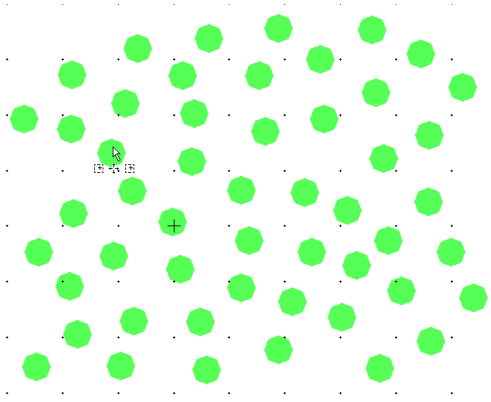


Figure 2-16: Midrange Square Cluster

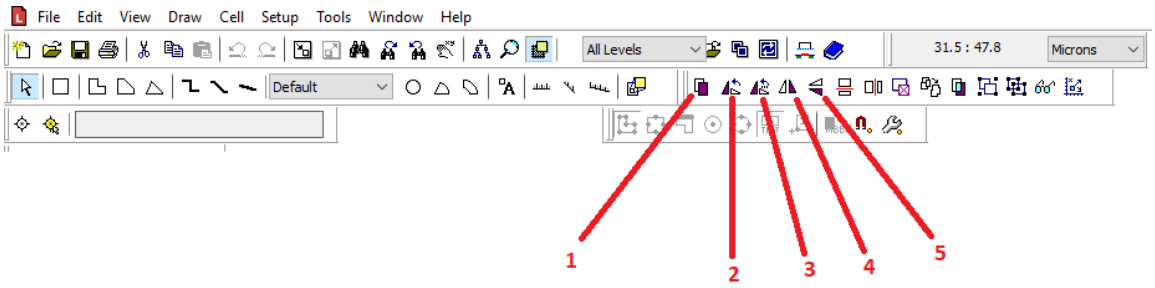


Figure 2-17: The L-Edit features for duplication, rotation and mirroring.

1) Duplication, 2) Rotate selected object 90^{o} CCW, 3) Rotate at any angle, 4) Mirror vertically, 5) Mirror Horizontally

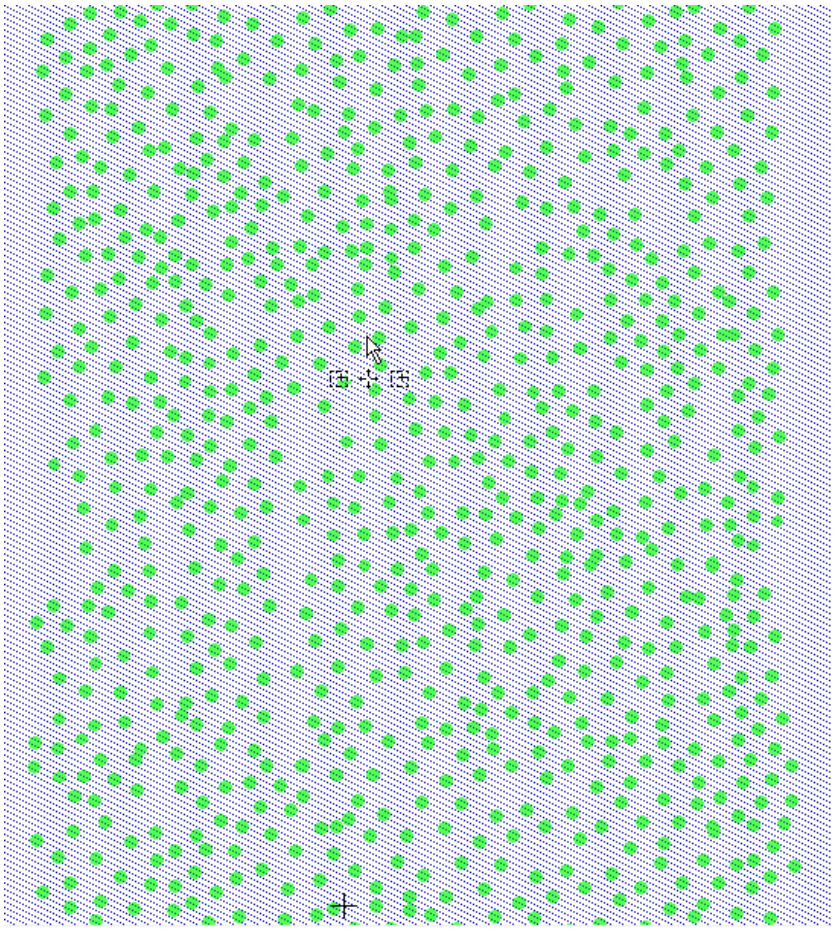


Figure 2-18: The loose CAD version of Design # 6 before Boolean subtraction.

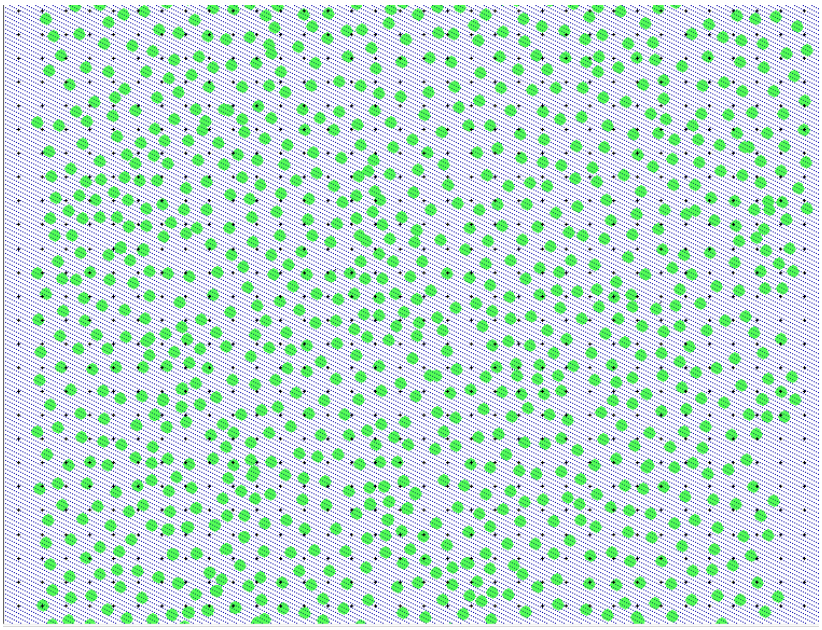


Figure 2-19: The Midrange CAD version of Design # 6 before Boolean subtraction.

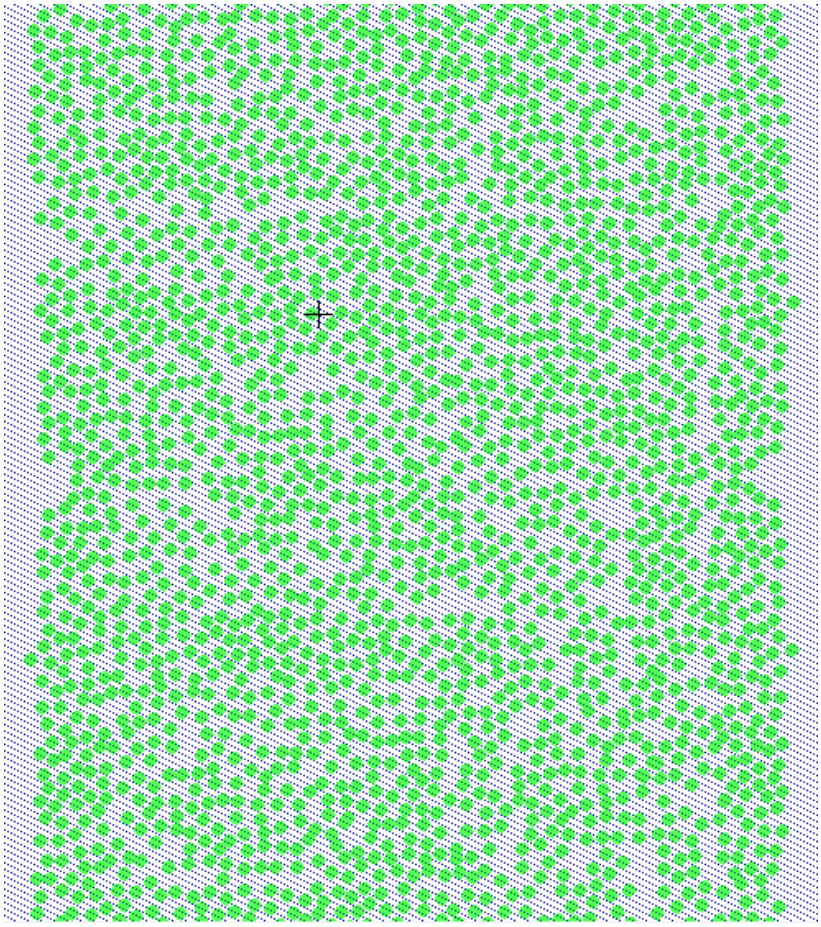


Figure 2-20: The dense CAD version of Design # 6 before Boolean subtraction.

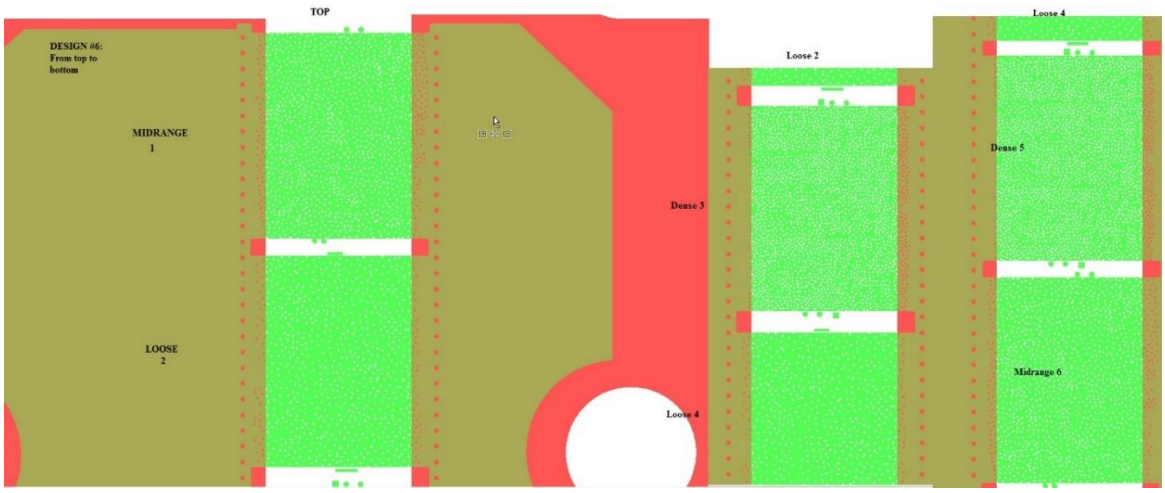


Figure 2-21: Sections of the migration device layout for Design # 6

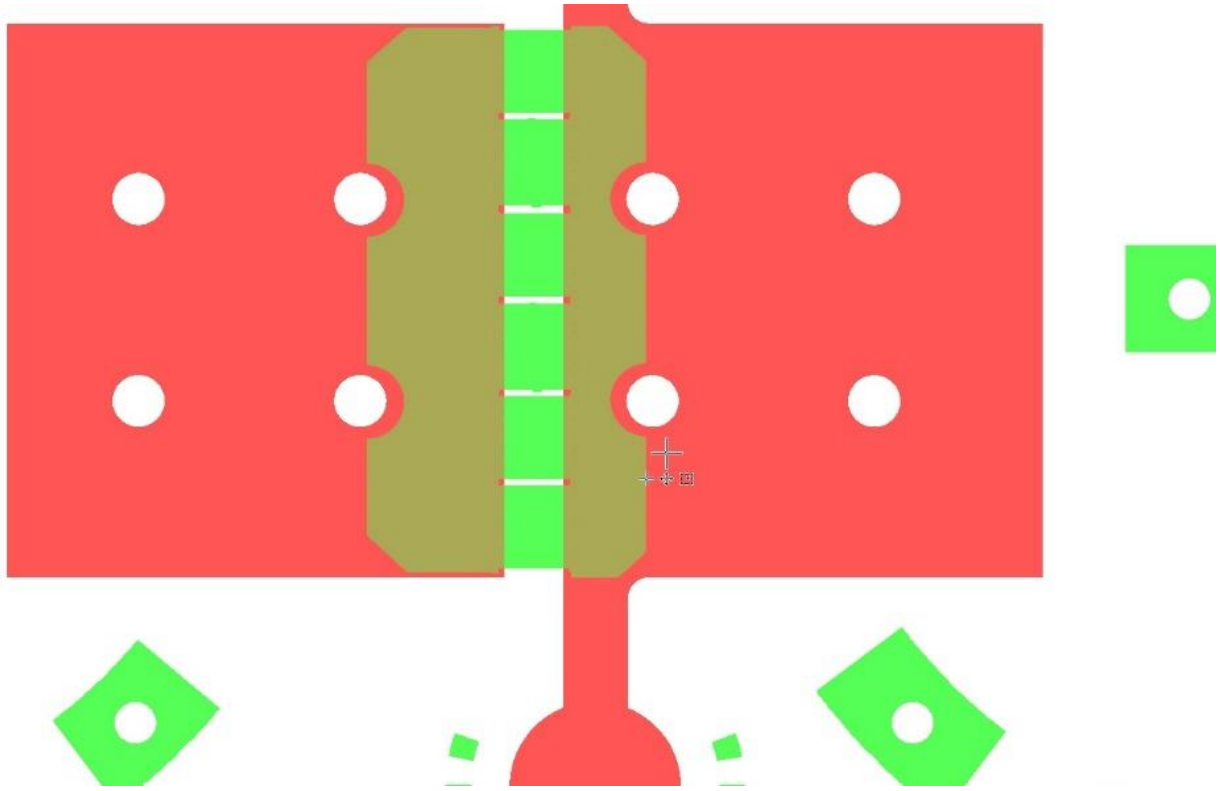


Figure 2-22: All six segments of the Design # 6 migration device.

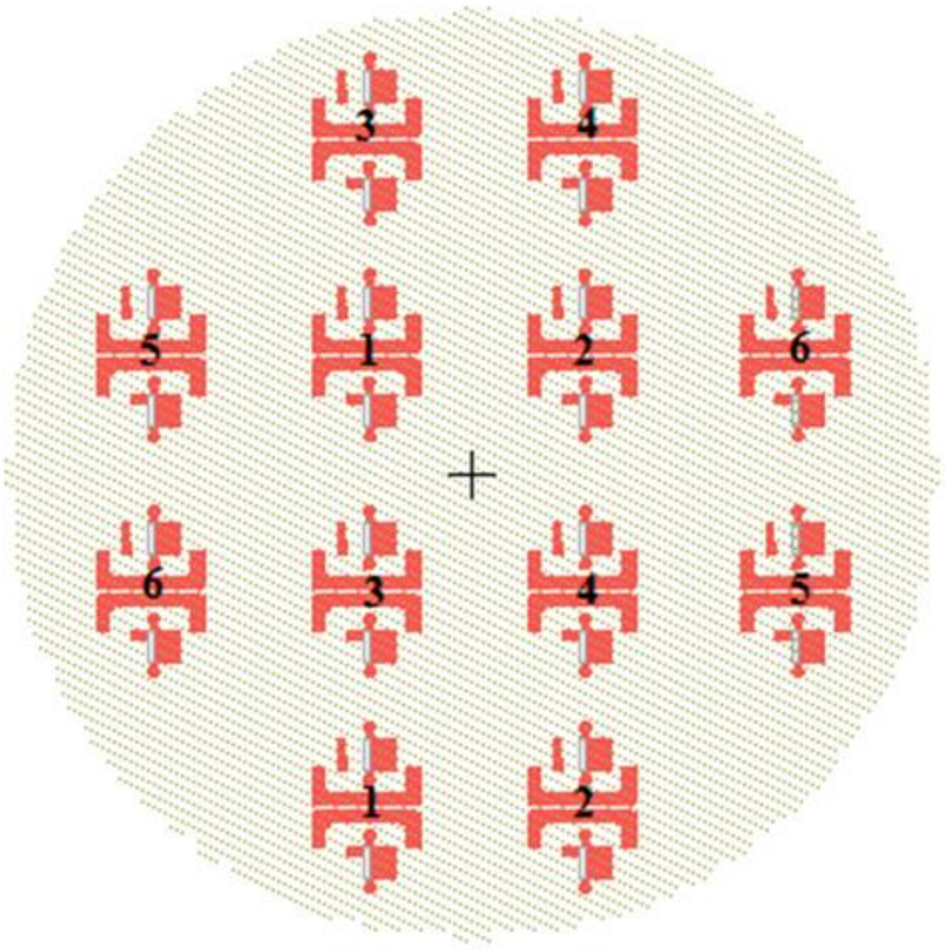


Figure 2-23: The layout of the original Design # 1-6 wafer. A number represents the location of the specific design.

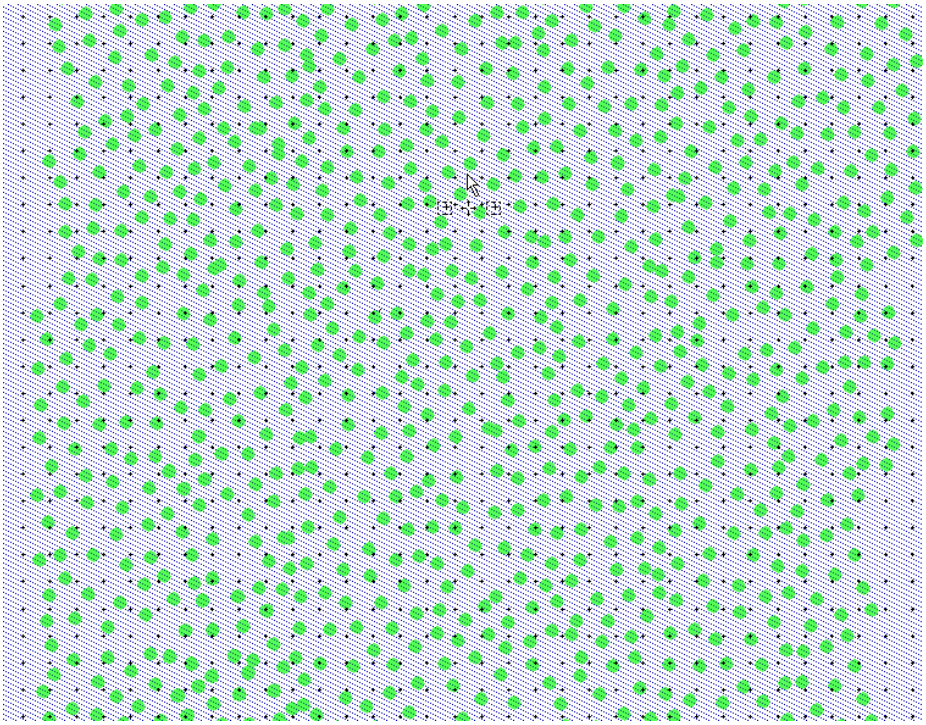


Figure 2-24: The loose-midrange CAD version of Design # 6 before Boolean subtraction.

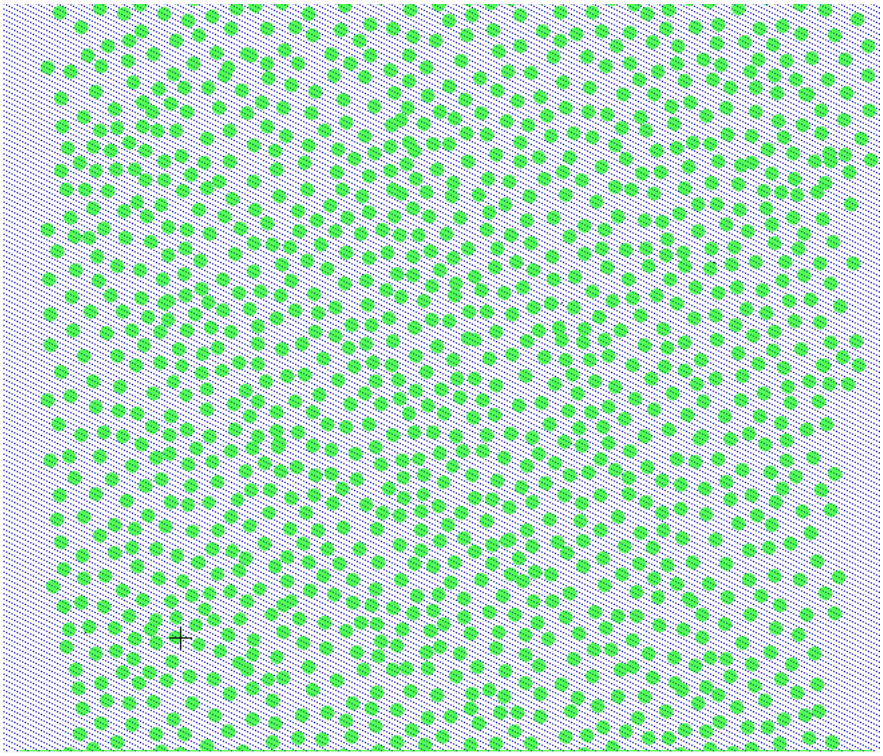


Figure 2-25: The dense-midrange CAD version of Design # 6 before Boolean subtraction.

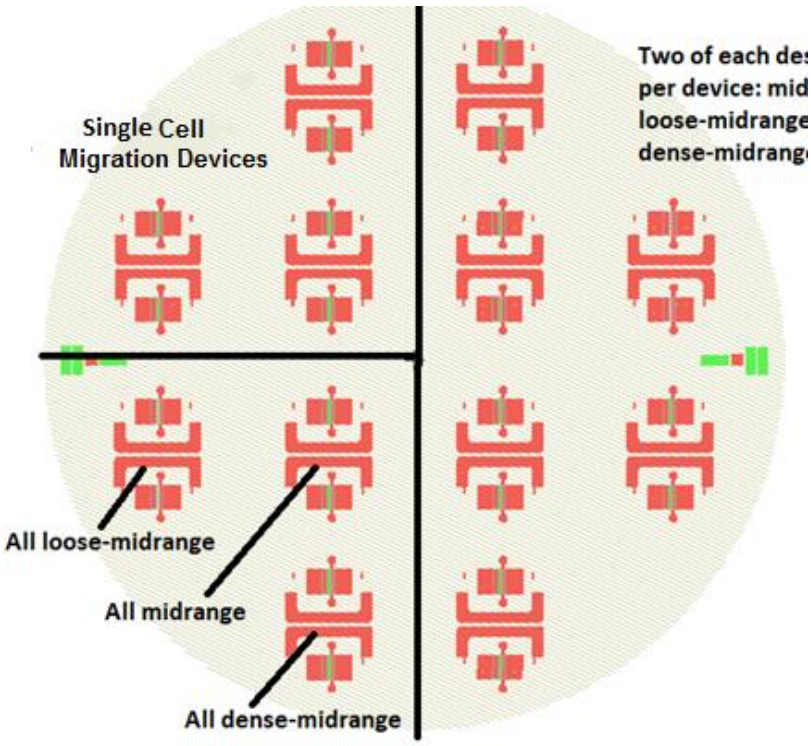


Figure 2-26: Full wafer map of Design # 6/single cell migration devices.

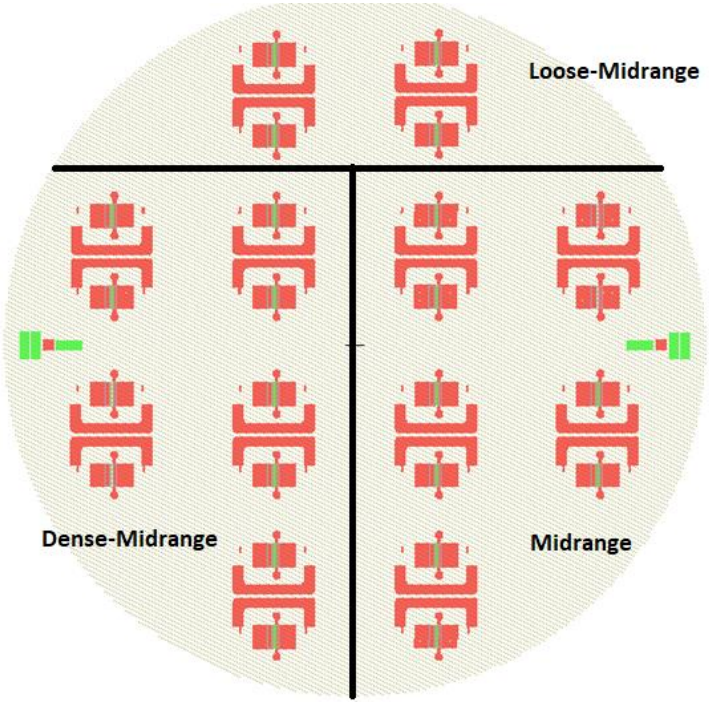


Figure 2-27: Full wafer map of Design # 6 wafer with all midrange designs

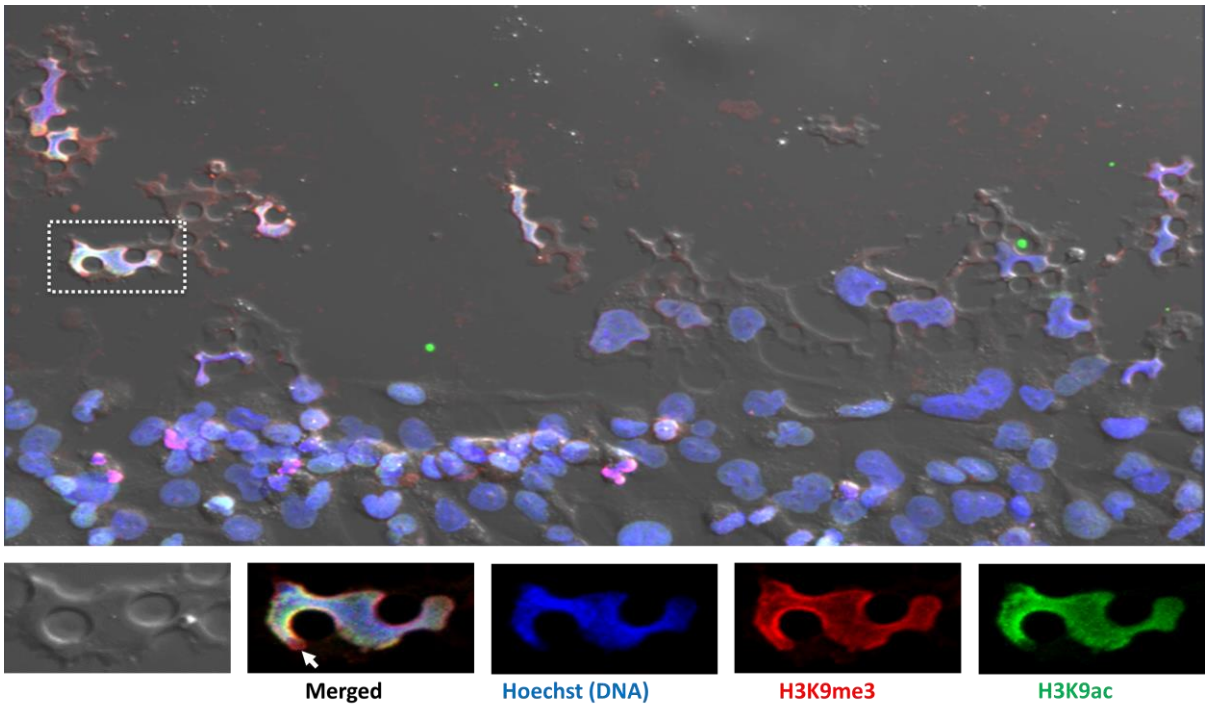
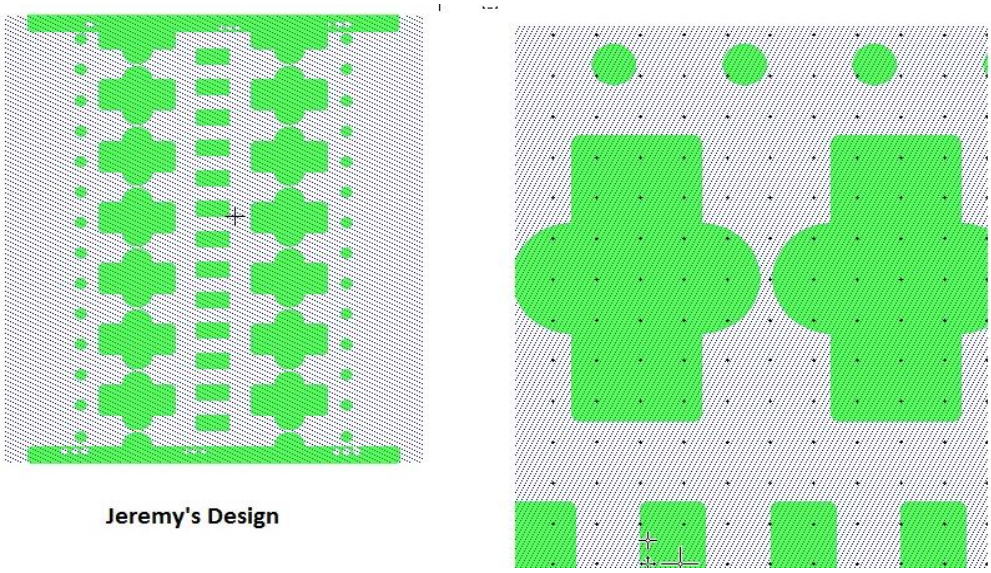


Figure 2-28: An example of heterochromatin condensation using the Design # 6 migration device. The arrow on the merged bracketed cell indicates an increase of trimetylation on histone H3 (H3K9me3) due to nuclear confinement.

2.6 Single Cell Migration Device

The concept for this device came from Jeremy Keys, a BME graduate student in the Lammerding Lab who is studying single cell migration. When cells come in contact with one another, they create a collective or cooperative migration, which is very different than single cell migration (Friedl et al., 2011). To encourage single cell migration, we surrounded the constrictions with rectangular abutments to isolate or herd individual cells into the constrictions (Figure 2.6.1). The rectangles are 70 µm x 30 µm with 2 µm chamfers (see the section on how to create chamfered rectangles). Versions of this device have 1, 2, 3 and 10 µm constrictions. This design was implemented on the second round of Design # 6 wafers.



27µm-30µm Diameter Parameters	X	Y
Delta	140	30
Array	2	14
Translation	-90.200	-221.000
Upper Rectangle Parameters	X	Y
Delta	140	60
Array	2	7
Translation	-90.400	-178.000
Lower Rectangle Parameters	X	Y
Delta	140	30
Array	2	1
Translation	-90.400	-236.000
10µm Pillars Parameters	X	Y
Delta	245	30
Array	2	14
Translation	-148.250	-210.000

Figure 2-29: CAD layout and L-Edit parameters for the single cell migration device before Layout BEAMER Boolean subtraction (Parameters explained in Appendix A, section 3.2).

2.7 Migration devices with all the same constriction

We returned to our original migration device design (Figure 1.2.4) for studying the effects of nuclear deformation over time by collecting cells that had migrated through a specific constriction size. This was accomplished by replacing our standard constriction channel layout (Figure 1-4), with six segments of all the same constrictions (Figure 2-29). A wafer was created with six migration devices with only 1 µm gaps, three with all 2 µm gaps and the remaining three all 15 µm (Figure 2-30 – 2-34). Our motivation for designing these migration devices was to explore the long-term effects and consequences nuclear deformation, fragmentation and nuclear envelope rupture. Clonal cells were seeded and removed after migration through the constrictions. The capture cell lines were expanded for two to four weeks and reseeded back into the constrictions. The cell lines would eventually migrate three times through the devices.

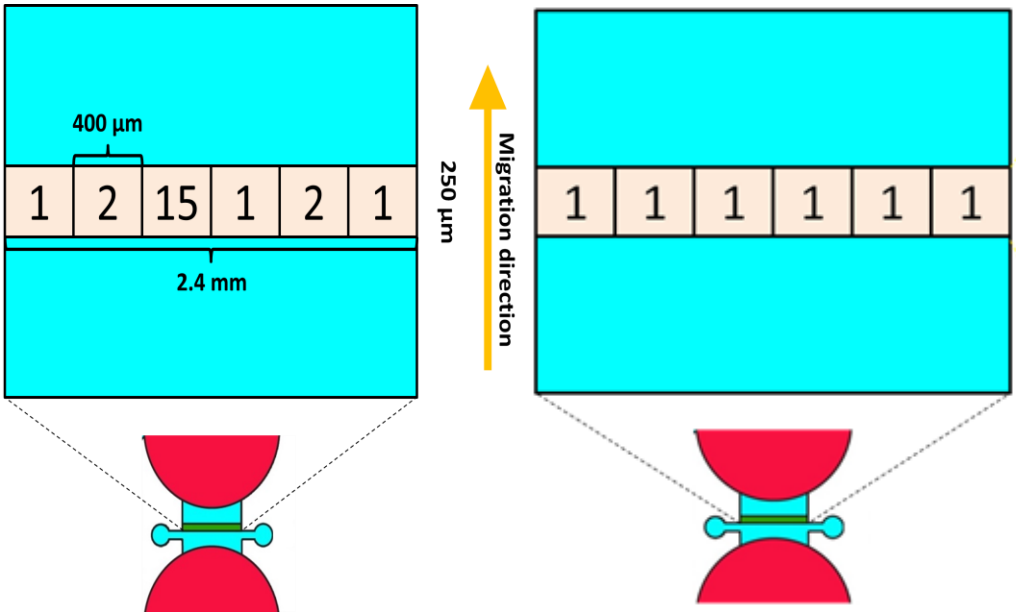


Figure 2-30: A comparison between the layout of our standard migration device (left) and a device with all the same 1 µm constrictions (right).

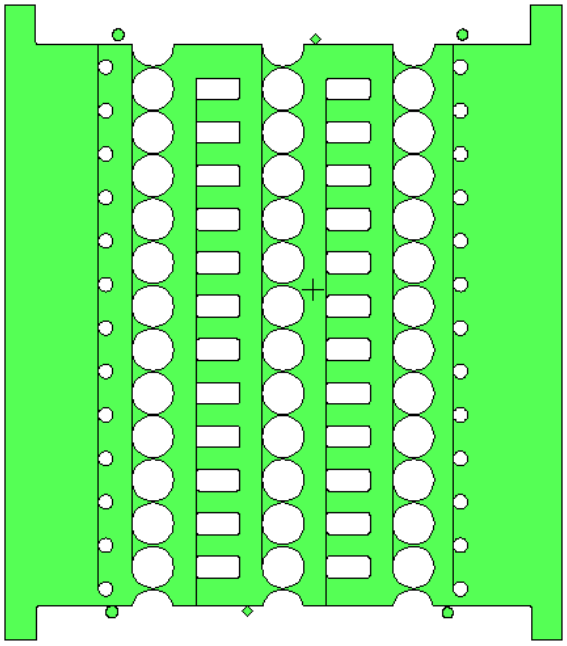


Figure 2-31: Layout for all 1 µm constriction migration device after Boolean subtraction.

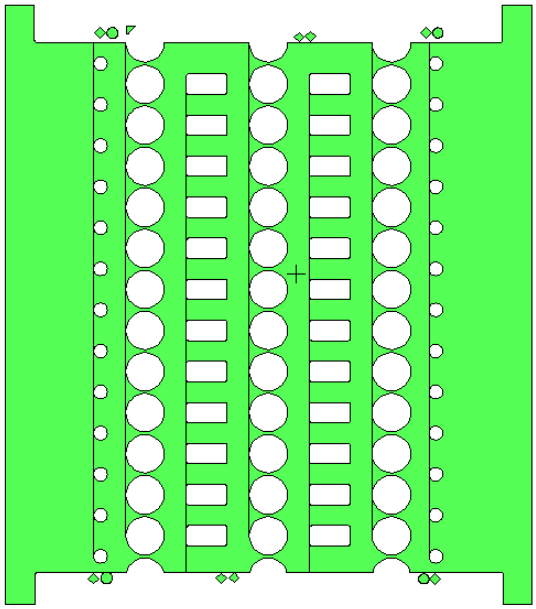


Figure 2-32: Layout for all 2 µm constriction migration device after Boolean subtraction.

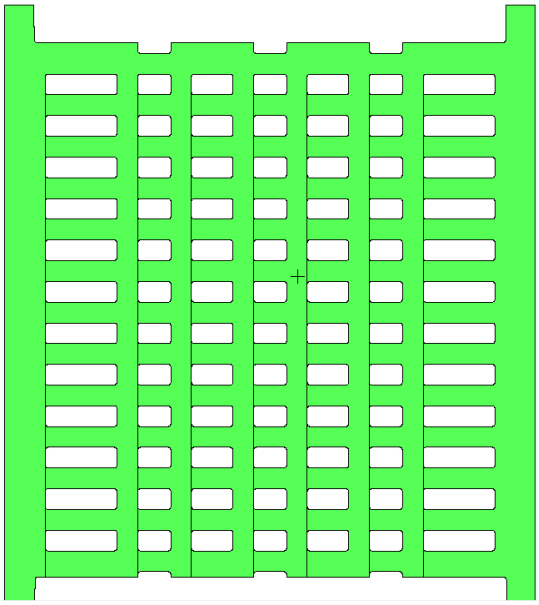


Figure 2-33: Layout for all 15 µm constriction migration device after Boolean subtraction.

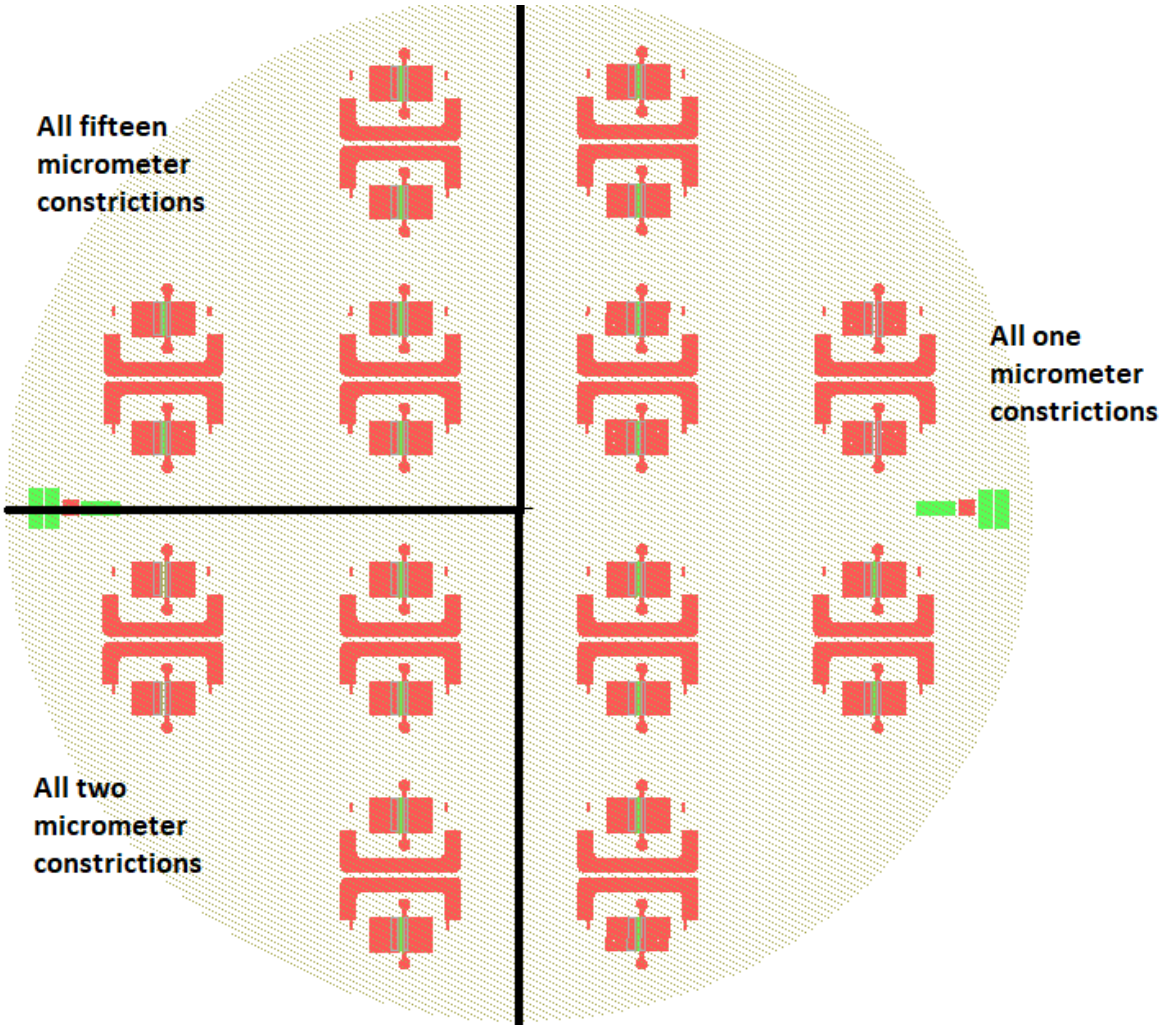


Figure 2-34: Full wafer layout for the all 1, 2 and 15 µm constrictions.

CHAPTER 3

ADVANCES IN FABRICATION

3.1 Introduction

Many obstacles emerged when attempting the repeat the fabrication process for these migration devices. After months of issues, it was best to examine alternative methods for reproducing these devices. The main source of problems revolved around accurately replicating the 1-3 µm constrictions with SU-8. We finally found that etching these fine features into the silicon substrate gave us a much better yield and opened the door for the creation of the newer designs with greater precision (see designs chapter of thesis). The following sections will discuss the evolution of this work from spinning layers of SU-8 into the reactive-ion etching (RIE) of hard materials.

3.2 SU-8 Fabricated Constriction Channels

SU-8 is a negative photosensitive epoxy manufactured by the MicroChem Corporation. The photosensitive compounds forms a strong acid when exposured to light in the recommended i-line (365 nm) or conventional UV (365-400 nm) spectrum. A post exposure bake (PEB) catalyzes the photoacid and initiates epoxy crosslinking at the exposed areas. This crosslinking is capable of creating insoluble high aspect ratio features imaged upon a substrate. With minimal nanofabrication equipment and at a relatively low cost, SU-8 has become an effective tool for creating “Bottom-Up” micron size structures for PDMS molding and microfluidic applications. With all the promise that SU-8 processing can offer to the biological research community, it does have its drawbacks. First, any researcher who has ever worked with SU-8 will quickly convey their struggles fabricating devices from it. SU-8 is notorious for having short and long-term adhesion issues to the underlying silicon wafer

along with high film stress that leads to cracking, buckling and delamination (Figure 3-1 & 3-2). Substrates must be properly cleaned, dehydrated and heat-treated beforehand for any chance of a successful outcome. Even with FOTS treatments, repeated PDMS molding will eventually pull the SU-8 features off the wafer. Spinning the highly viscous epoxy has its own challenges such as poor full wafer uniformity and significant edge bead thicknesses when not spun or baked correctly. These high/low spots or uneven surface topography can create gaps between the photomask and the wafer resulting in proximity lithography and distorted feature geometrics (Chuang et al., 2002).

The migration devices were originally fabricated with a two-step SU-8 process consisting of thin layer that represented the pillars constrictions, and a thicker 200-250 µm layer for the cell chambers, bypass channels and alignment marks for punched PDMS wells (Davidson et al., 2015). Designs for both layers were transferred from a computer assisted design (CAD) program, to a mask writer and on to an opaque photoresist/chromium over glass photomask. The mask writer exposes the photoresist above the chromium on desired areas of the photomask, which are later developed leaving exposed chromium to be wet etched later. The removal of the exposed chromium allows light to pass directly through the photomask and on to a SU-8 wafer placed directly underneath. As light passes through a photomask, it bends outwards around the corners of the etched chromium, which will enlarge the image dimensions underneath. The larger the gap between the mask and the SU-8 wafer, the larger the distortion. To minimize diffraction or the spreading of light through small apertures, the photomask is pressed against wafer in close contact. This contact lithography is an inexpensive and effective means of transferring features as small as ≈ 1-2 µm onto a wafer. The main issue we had in fabrication was creating the 1 & 2 µm gaps through 5 µm thick SU-8. Thicker resist and photosensitive compounds require a larger optical dose and tend to

suffer from the effects of diffraction (Williams, 2004). The combination of these factors raises the minimum feature sizes achievable using contact lithography, leading to our 1 μm constriction gaps ending up around 2-3 μm in size after SU-8 development. Reduction steppers are able to reproduce smaller features by optically reducing the image 4x or 5x and exposing with short wavelength of light (Sheats et al, 1998), but these tools take some dose time characterization and are expensive. Quite often, lithographers implement different contact lithography techniques to attain smaller feature sizes. Applying vacuum and forcing the wafer and mask together can minimize the gap between both surfaces. Smaller features (<1 μm) can be achieved with contact lithography by using hard vacuum contact and photoresist <2 μm thick or SU-8 2002 (if SU-8 is desired, one thought to consider in the future is to spin two layers of 2 μm SU-8 on top of one another to achieve a 4 μm tall gap). SU-8 tends to be thicker on the outer edge of the wafer due to the centrifugal forces involved in spin-coating the epoxy. Removing the SU-8 edge bead from the wafer is essential and improves contact lithography and the overall uniformity of the film. For our devices, 5-10 mm of SU-8 can be removed from around the edge of the wafer, just be careful not to remove or damage the alignment marks. Utilizing the air bearing while bring the substrate in contact may also balance out any surface irregularities.

We were able to create ≈1μm gaps by slightly under exposing the SU-8 and then performing a long bake to complete the cross linking (See Appendix C). Under-exposed SU-8 tended to buckle and delaminate off the wafer after development. The hard bake relaxes the SU-8 at the gaps, which sometimes conform to the sizes desired. This is a creative solution for attaining smaller feature sizes, but the yield for successful devices was poor. More often than not, the SU-8 would either break or tear at the gaps. Even the gaps that were successful

display signs of tearing at the thinnest sections (Figures 3-3 & 3-4). Gap sizes varied from wafer to wafer and from constrictions on the same device and/or harden wider than desired. Overtime, it was becoming difficult to reproduce device wafers, leaving the good wafers highly coveted. In efforts to preserve them from SU-8 delamination and failure, the group started to create plastic molds of successful wafers. More specifically, a plastic positive mold was made in order to later make another plastic mold from that to replicate and make a durable copy of the SU-8 mold for their PDMS migration work (Keys et al., 2018). Not only does this seem to be a lot of work, but may compromise the final product's fidelity. Even with this safeguard, it was only a matter of time before the SU-8 would break and a new wafer would need to be made.

Eventually, the most critical component of the device should not depend on a photosensitive epoxy and an unreliable lithography trick. We needed to replicate our lithography reliably into a material not prone to breakage and delamination. The most straightforward solution was to etch the 5µm features directly into the silicon substrate instead of depositing or spinning on another material. The microelectronics industry and the nanofabrication community has been etching silicon for decades for the development of Micro-Electro-Mechanical Systems (MEMS) (Qu, 2016) and more recently microfluidic devices (Iliescu et al., 2012).

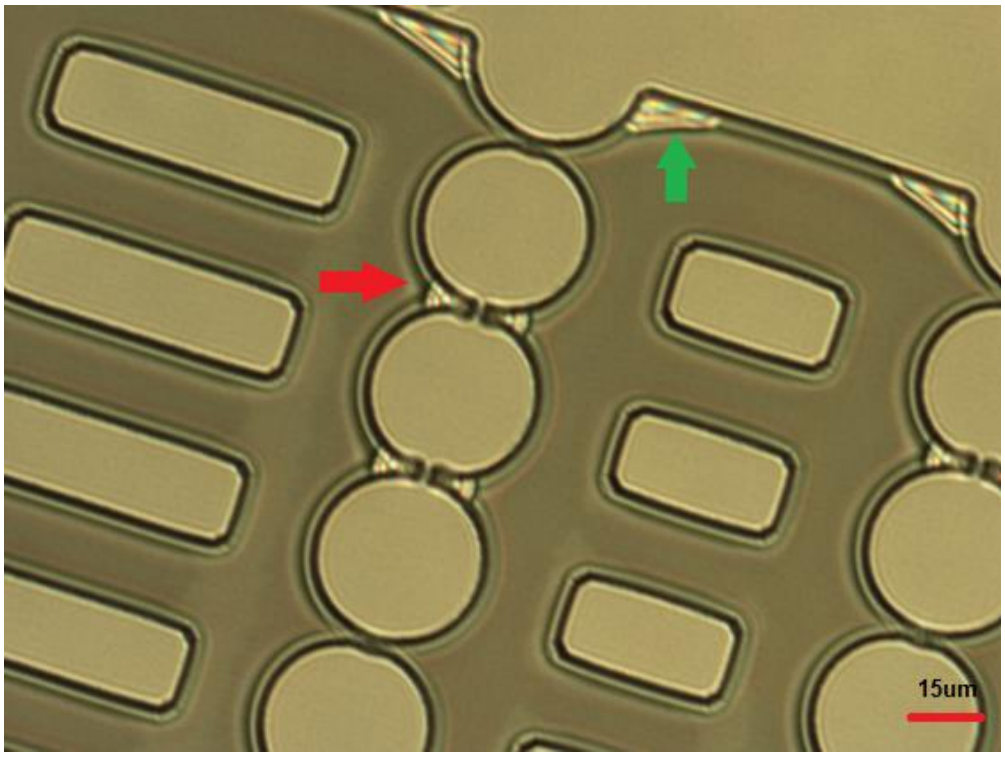


Figure 3-1: Intermittent SU-8 breakage (red arrow) at the 1 µm gaps and delamination (green arrow) at the edges of the device (50x).

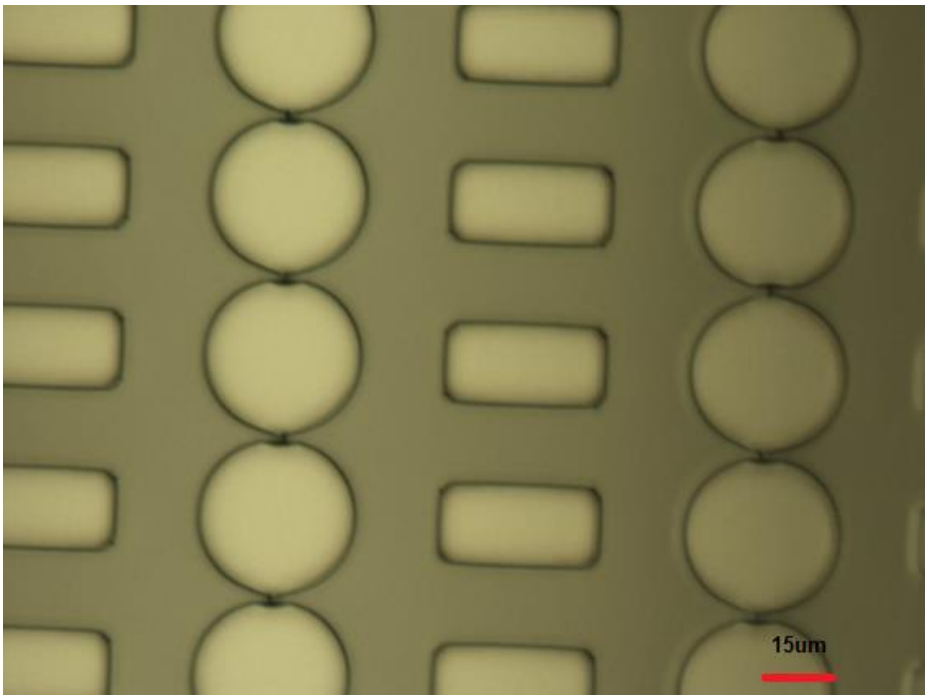


Figure 3-2: SU-8 cracking throughout all the 1 µm gaps in this device (50x).

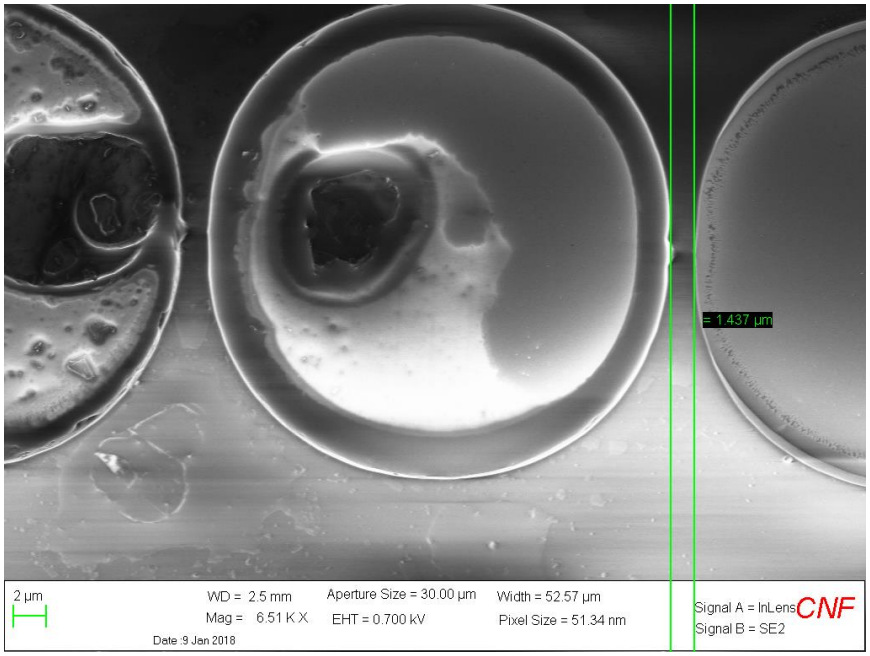


Figure 3-3: A Scanning electron microscope image and measurement of an attempted 1 µm gap constructed between two 29 µm diameter holes made with SU-8 2005.

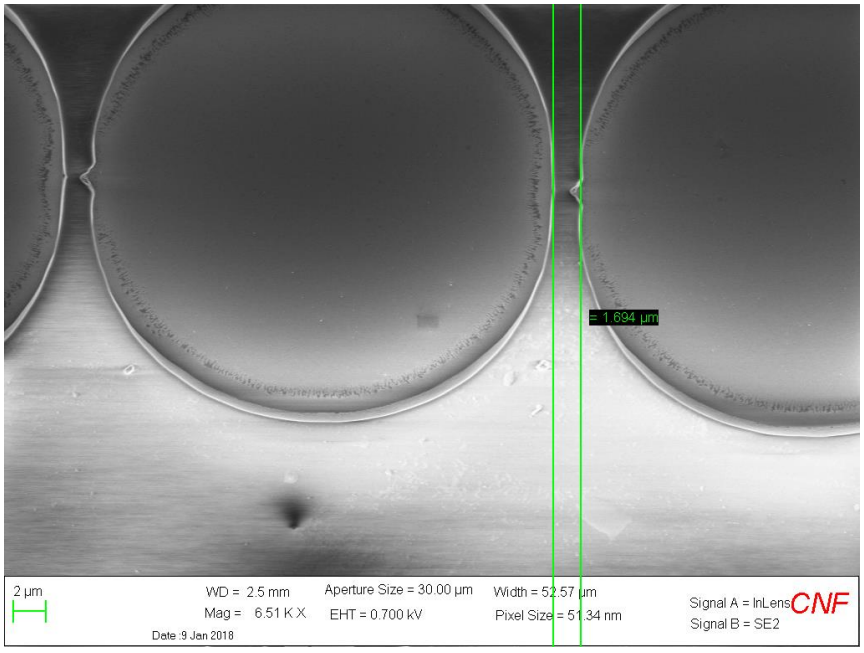


Figure 3-4: A Scanning electron microscope image and measurement of an attempted 1 µm gap constructed between two 29 µm diameter holes made with SU-8 2005.

3.3 Plasma Etching and Deep Reactive Ion Etching

We decided that the best course of action for improving the yield of these devices was to forgo the thin SU-8 process and etch all the critical features directly into the silicon substrate. Not only is etching more precise, controllable and a permanent fabrication solution, but silicon adds strength and eliminates adhesion issues. Etching will occur on exposed surfaces and areas, so lithography is required to cover or mask the areas that should not be etched. Patterning with a thinner photoresist instead of fighting diffraction through 5 µm of SU-8 would also remedy the lithography issues. A thin negative resist can easily resolve the 1 µm gaps while also serving as an etch mask. As mentioned before, 1µm features can effortlessly be reproduced with 2 µm thick SU-8 2002. We discovered that spinning a 1.7 µm thick layer of negative AZ nLof 2020 resist was adequate for both replicating critical features and standing up to the rigors of plasma etching.

The term plasma refers to a partially ionized gas composed of ions, free electrons and inert gas neutrals. For the etching applications, argon gas was bled into a vacuum chamber to be ionized between two parallel plates. The gas normally behaves as an insulator, but if the voltage increases high enough between the plates, the insulator break downs, resulting in an electrical arc. This initial spark generates a large number of excited argon ions and free electrons that are drawn instantly to the positive and negative sides of the plates (Figures 3-5 & 3-6). These particles collide with other neutral gas molecules to created more electrons and ions. Electrons are able to move much faster than the ions due to their smaller mass and are more likely to collide with other particles (Campbell, 2008). More secondary electrons are released when the ions strike the cathode, which are then immediately accelerated towards the anode. These collisions eventually increase and this

mixture of excited gas fragments can be sustained as long as the voltage remains high enough to created high energy particles. For etching, not all the neutral atoms are needed to be ionized and can coexist with an equal number of electrons and ions in what is termed a low temperature or weakly ionized plasma.

Electron and ions collisions can fracture or dissociate other gases molecules introduced to the plasma resulting in gas particles with incomplete bonding states called reactive plasma neutrals or free radicals. Fluorine radicals are extremely reactive to silicon while other radicals may be reactive to different exposed surfaces. With the proper etch chemistry, these radicals adsorb onto a surface they have an affinity for, react and form a volatile byproducts (Figure 3-7). These byproducts will desorb from the exposed surfaces and leave the chamber through the vacuum pump exhaust.

What determines how these high-energy particles will etch is their organization and directionality as they make contact with the substrate. Etch chamber's using only a parallel plate configuration will scatter the high-energy particles in many directions. As free radicals randomly impact the substrate, etching will occur in both the vertical and horizontal directions resulting in isotropic etching (Nojiri, 2015). A plasma dominated by free radicals will easily etch underneath and undercut an etch mask (Figure 3-8). Isotropic etching may appear detrimental, but is a vital step for fabricating cantilevers (Davis & Boisen, 2005) and other micromechanical suspended structures (Qu, 2016).

One can directly etch straight sidewalls into a material or anisotropic etch by creating an electric field that influences the directionality of these energetic particles. One method for achieving this is ion milling or ion-beam etching. Ion milling achieves anisotropic etching by vertically bombarding the surface with only excited positive argon ions. Without any reactive

gases, the etching is purely physical in nature and can indiscriminately etch almost any alloy, compound or metals that lack any volatile etch products (Campbell, 2008). Etch depth is directly dependent on etch mask durability due to the low etch selectivity of ion milling. Therefore, a thick hard mask is necessary to withstand the ion bombardment and combat mask erosion. This style of etching is a destructive process; it leaves damage to the substrate and etch debris on the surface.

Researchers later discovered that combining the directionality of ions with isotropic chemical etching improved the effectiveness of the free radicals. Coburn and Winters' landmark paper in the late seventies revealed the value of etching with both techniques simultaneously (Coburn & Winters, 1979). As demonstrated in Figure 3-9, the poly-silicon etch rates were significantly higher for the tandem argon ion and xenon difluoride (XeF_2) processes than either the fluorine radical or the ion beam alone. It is believed that because these horizontal surfaces are exposed to both the ions and radicals, they etch at a higher etch rate than the vertical sidewalls, which are only exposed to only free radicals (Kessels, 2017). The energetic bombardment of ions is also constantly exposing new horizontal surfaces to free radical absorption, which increases etch rates and minimizes bombardment damage (Coburn & Winters, 1979). This work initiated researchers to develop similar anisotropic processes for etching specific materials with high selectivity and was the beginning of ion-assisted or reactive-ion etching (RIE). Later, it was discovered that a plasma powered by a radio frequency (RF) source within a magnetic field or an inductively coupled plasma (ICP) would increase the ion density. This combined with the parallel plate configured RIE increase the etch rates even more (Campbell, 2008).

Another path for plasma etching silicon at the CNF was developed from the desire to etch high aspect features at greater depths. All ICP-RIE processes are limited by their aspect ratios (etch depth/feature width). Smaller holes will etch at slower rates than larger holes and eventually, the rates will slow or stop when the holes becomes too deep for the ions/radicals to complete their chemical reactions (Campbell, 2008). Deep reactive-ion etching (DRIE) by the Bosch process (Bosch, 1994) is an alternating three-step etch recipe that is capable of anisotropically etching holes through a wafer. The Bosch process begins with a short isotropic sulfur hexafluoride (SF_6) ICP etch. The SF_6 in a plasma dissociates into six fluoride radicals that bind with silicon to form the volatile silicon tetrachloride and silicon fluoride compounds (SiF_4 & SiF_x). The etch step is followed by the deposition of octofluorocyclobutane (C_4F_8) on the sidewalls and base of the etched trench. This fluorocarbon is critical for maintaining the anisotropic contours by inhibiting horizontally etching of the sidewalls. The SF_6 and directional ions are used again to break through the fluorocarbon base before etching another short isotropic etch, leaving the passivation layer on the previous sidewalls. Every completion of these successive steps will leave small isotropic scallops in the sidewalls. By repeating these three steps or loops, vertical high aspect ratio silicon features can be created independent of geometric planes. For our first trial, I chose to DRIE the 5 µm constrictions (Appendix C) of our Designs # 1-6 wafer (Figure 2-22). Our decision was motivated by the speed of DRIE compared to RIE which would later translate to lower tool time and costs.

Our initial DRIE results were very promising. For the first time, we were able to faithfully reproduce our 1 µm features throughout the wafer (Figures 3-10 & 3-11). Even with the complexity of design #3, the gaps appeared to be uniform and precise (Figures 3-12 - 3-14). Our original 2.5 second exposure was effective for design # 1-5 (Chapter 2.2-2.4), but was too

long for Design # 6 (Chapter 2.5), resulting in holes ≈ 3 µm in diameter (Figures 3-15 & 3-16). We were able to accurately replicate the 5µm hole sizes by decreasing the exposure time to 1.7 seconds (Figure 3-17) and finally make PDMS molds for Design # 6. The optimum exposure dose for a pattern is a complex function with many variables, which is why some characterization is important for every exposure. With the newfound success, I later started etching newer Design # 6 layouts that included devices with all the same pillar densities (Figure 3-18) and the single cell migration device (Figure 3-19). This DRIE process was not only reproducible, but was efficient and required less than two hours of clean room time.

I later optimized the exposure time to 3.0 seconds for the migration devices with all the same size constrictions designs (Figures 3-20 – 3-25). Images and measurements from the scanning electron microscope revealed the fidelity and accuracy of the etching compared to using SU-8. Gaps precisely 1.0 µm could be achieved by slightly lowering the exposure time by tenths of a second. There was also a cleanliness to etching, which should transfer to the final PDMS product.

With all the promise of DRIE, the method had one major downside, as the scalloping of the sidewalls sometimes caused PDMS to tear and remain in the holes. This was especially prominent with the 5 µm pillars for design # 6 (Chapter 2.5). Over time, we were concerned that PDMS may clogged most of the pillars, compromising the mold. Removing the PDMS from the 5 µm holes seemed challenging and spawned the SU-8 removal work later in the thesis. The easiest solution for this situation was to move the process to a unique ICP-RIE recipe specifically developed to obtain smoother sidewalls. This approach increases process time and costs, but the smoother sidewalls give a better product and possibly a more permanent solution for fabricating the fine migration device features.

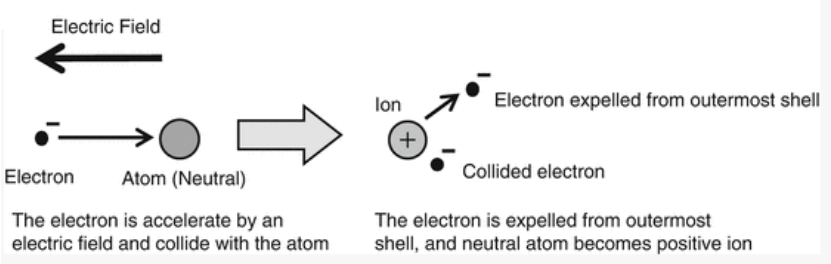


Figure 3-5: An Example of Plasma Initiation: An electrons colliding into a gas neutral result in the generation of an ion and an expelled electron (Nojiri, 2015).

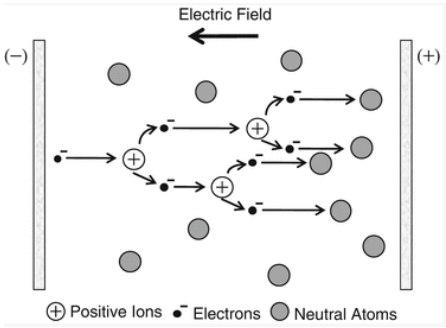
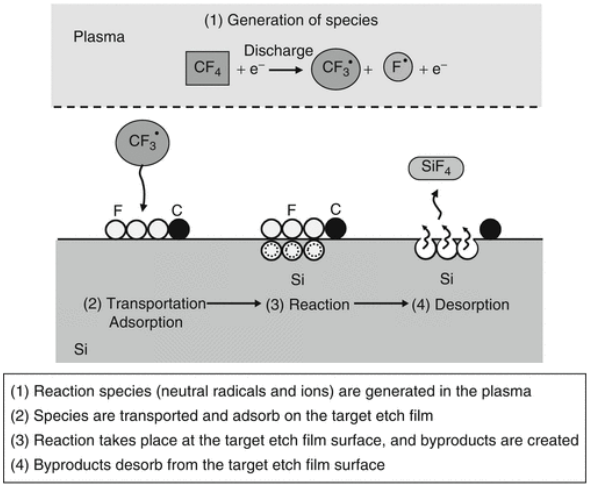


Figure 3-6: Electron avalanche in-between parallel plates during the early stages of an inert gas plasma (Nojiri, 2015).



Figures 3-7: The stages of gas neutrals becoming free radicals and reactively etching a substrate (Nojiri, 2015).

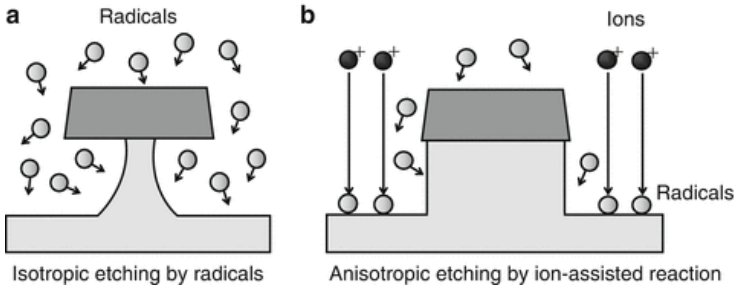


Figure 3-8: Two types of plasma etching:

a) Isotropic etching

b) Anisotropic ion-assisted or reactive-ion etching (Nojiri, 2015).

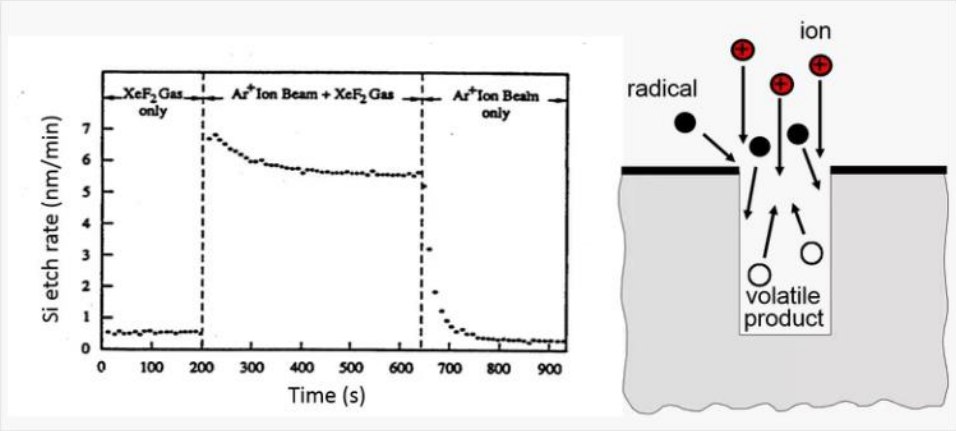


Figure 3-9: An overview of reactive-ion etching:

Left: The pivotal diagram from Coburn and Winters' paper: *Ion- and electron-assisted gas-surface chemistry—An important effect in plasma etching* (Coburn & Winters, 1979) illustrating the effect that combining ion bombardment with reactive gas chemistry had on etching poly-silicon.

Right: A simple illustration of the mechanics of reactive-ion etching (Kessel, 2017).

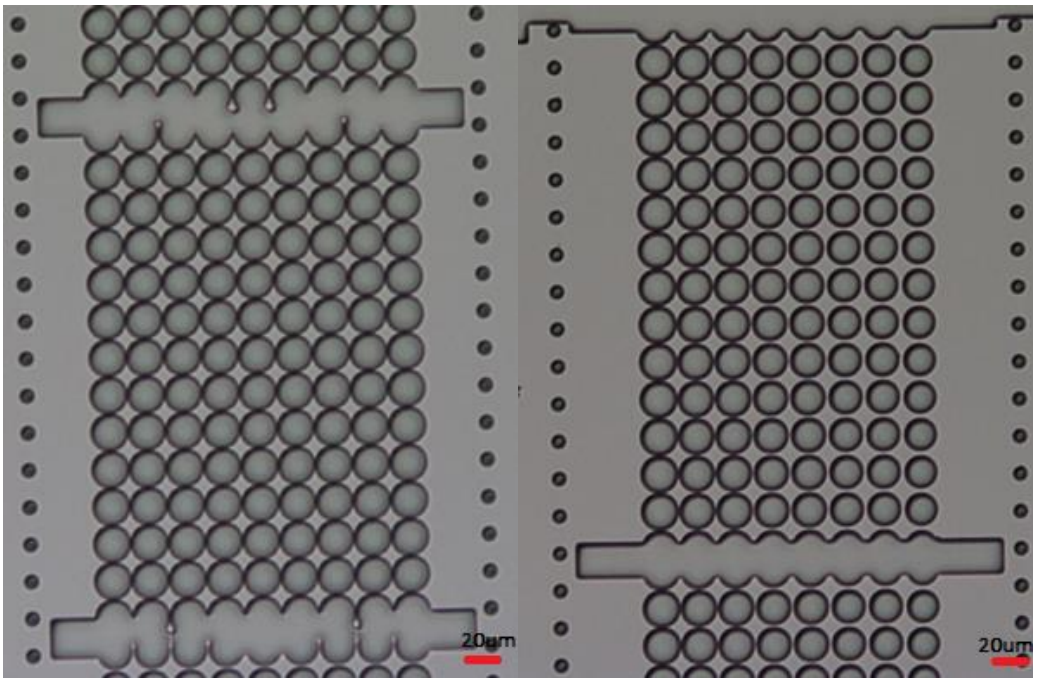


Figure 3-10: DRIE molds in silicon. Left: Design #1 with 1 µm gaps.

Right: Design #4 with descending constriction gaps from 5 µm to 1µm (10x).

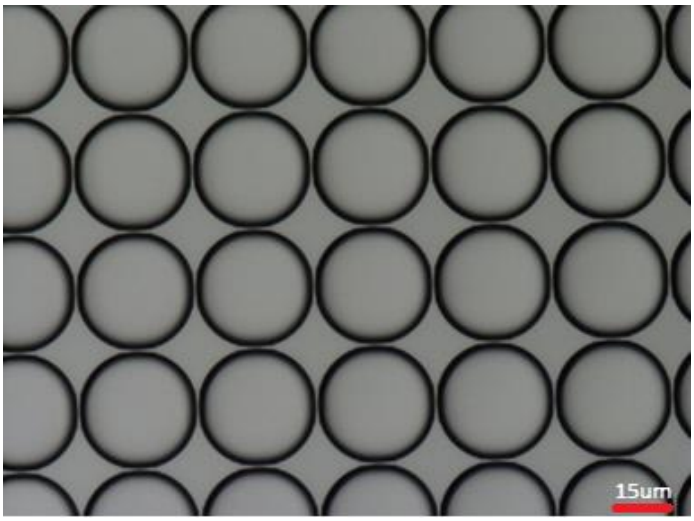


Figure 3-11: Design # 1 constriction channel. A linear lattice of 1 µm gaps between 29 µm holes DRIE etched 5 µm into silicon (50x).

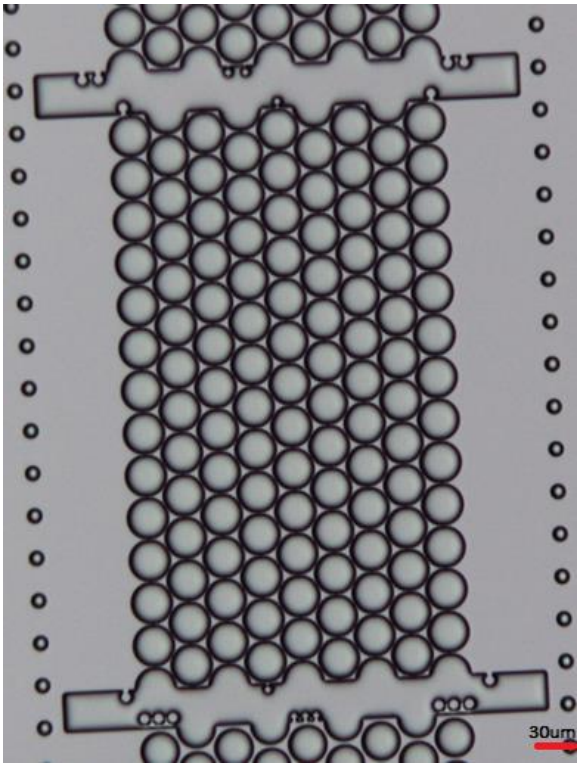


Figure 3-12: Design # 3 double-shifted holes DRIE in silicon.

From top to bottom: 2 µm, 1 µm and 3 µm constrictions gaps. (10x).

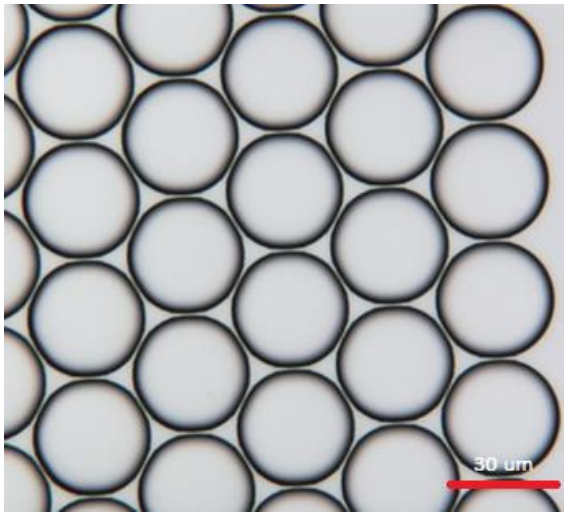


Figure 3-13: DRIE Design # 3 mold in silicon. Etched 29 µm diameter holes surrounded by

1 µm gaps in all directions (50x).

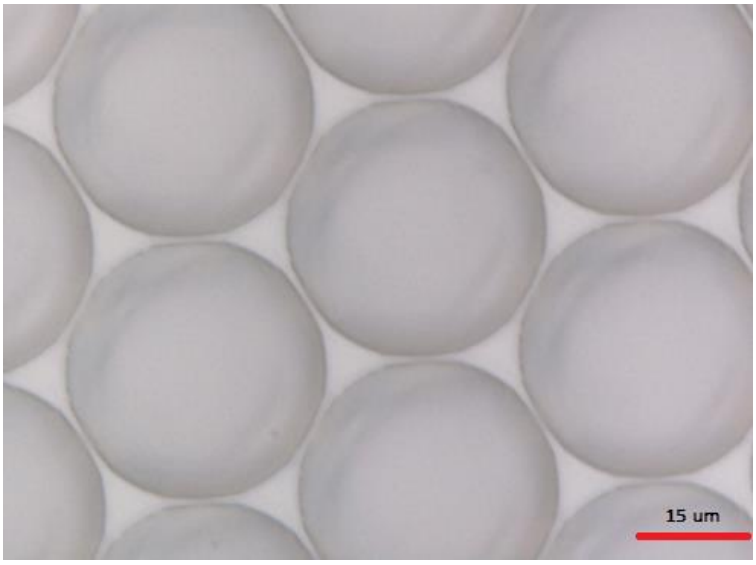


Figure 3-14: DRIE Design # 3 mold in silicon. Etched 29 µm diameter holes surrounded by 1 µm gaps in all directions (100x).

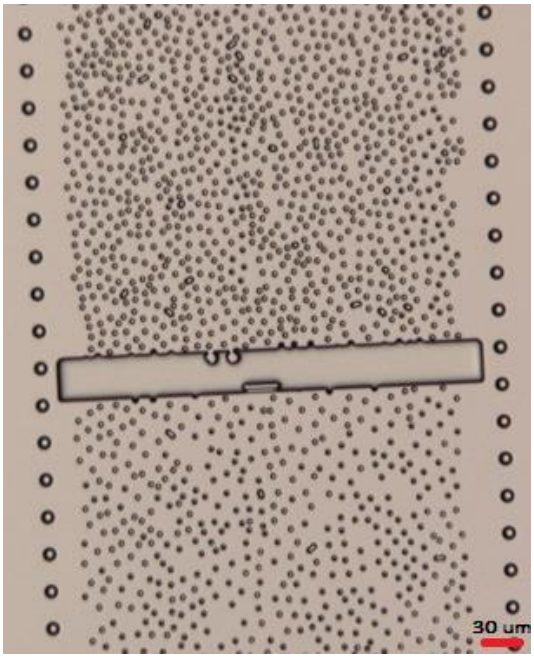


Figure 3-15: The reduction in pillars diameters of a Design #6 PDMS mold after exposing AZ nLof 2020 for 2.5 seconds (10x).

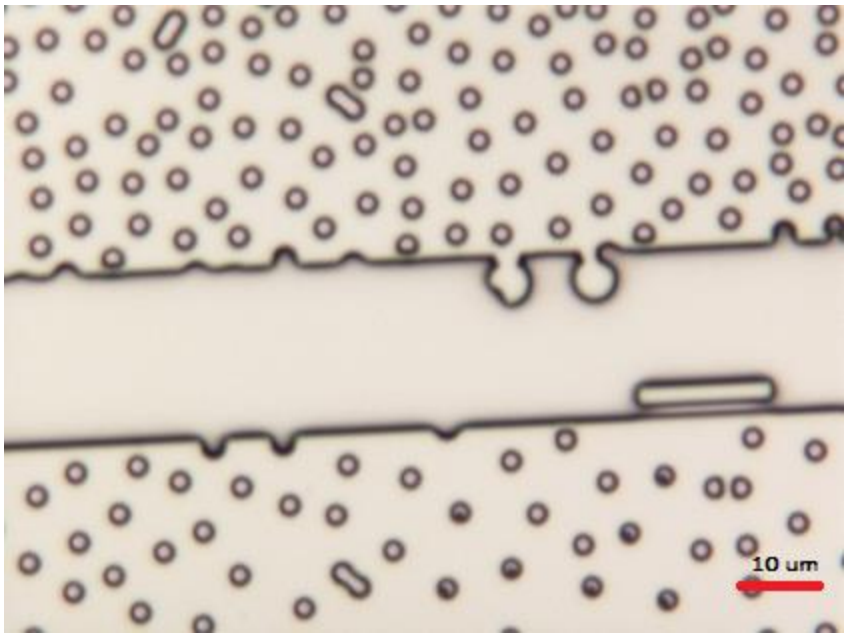


Figure 3-16: The reduction in pillars diameters of a Design #6 PDMS mold after exposing AZ nLof 2020 for 2.5 seconds. Pillars actual 3 µm in diameter instead of the desired 5 µm (50x).

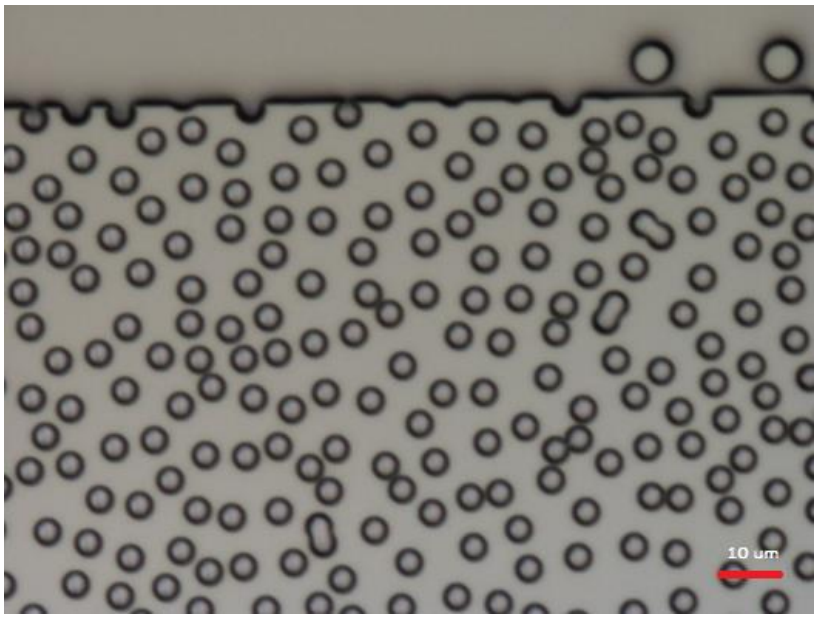


Figure 3-17: 5 µm holes were DRIE etched for Design #6 after reducing the exposure time of AZ nLof 2020 to 1.7 seconds (50x).

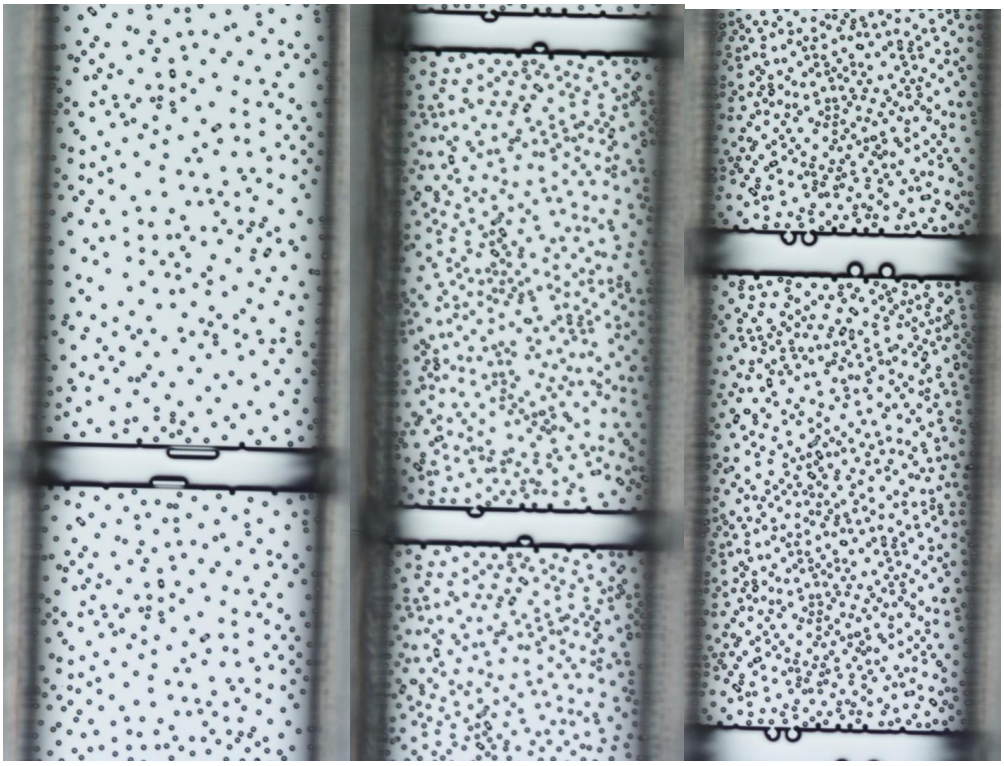


Figure 3-18: Different densities of our Design # 6 designs in DRIE silicon (10x).

Left: midrange loose designs, Center: midrange designs, Right: midrange dense.

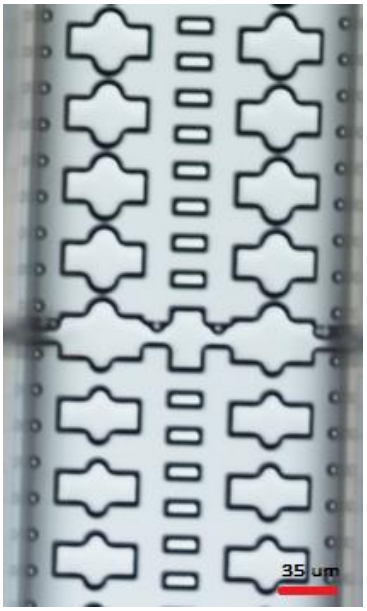


Figure 3-19: DRIE silicon mold of the single cell migration device after exposing AZ nLof 2020 for 1.7 seconds (10x).

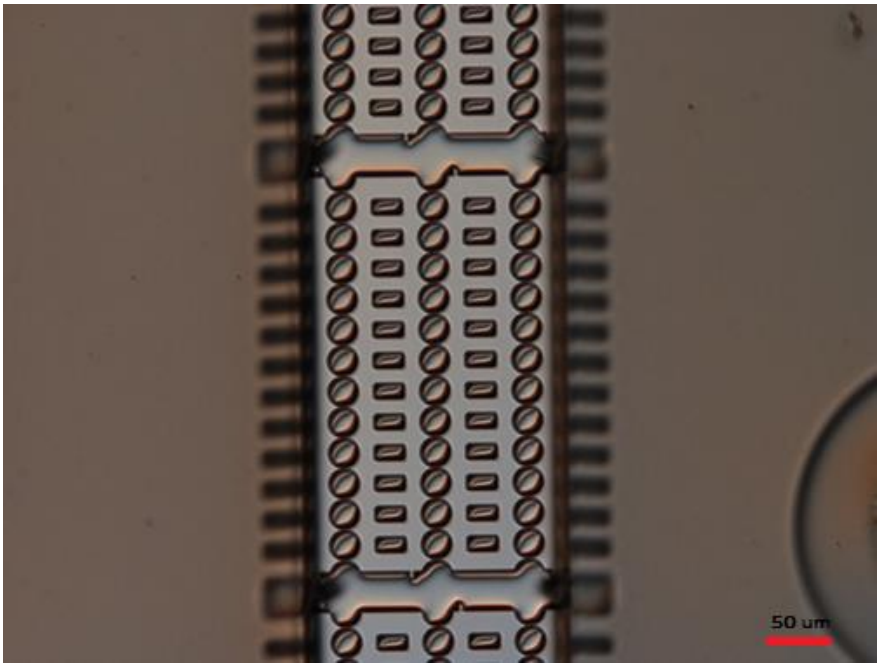


Figure 3-20: A completed migration device mold with all DRIE silicon 1µm constrictions in the center and surrounded by the upper 200 µm SU-8 cell chambers (10x).

Figure 3-21: 1 µm constrictions gaps between 29 µm holes deep reactive ion etched into a silicon substrate (50x).

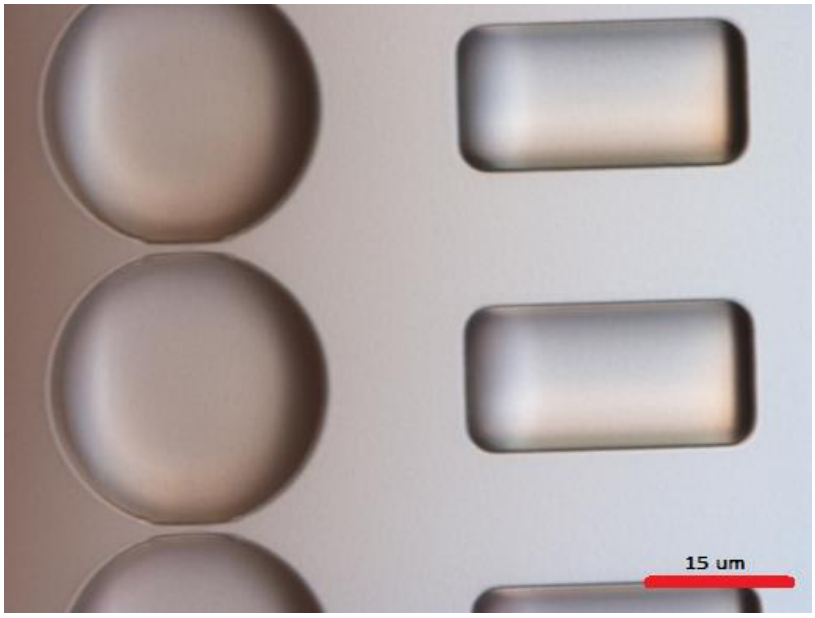


Figure 3-22: 1 µm constrictions gaps between 29 µm holes deep reactive ion etched into a silicon substrate (100x).

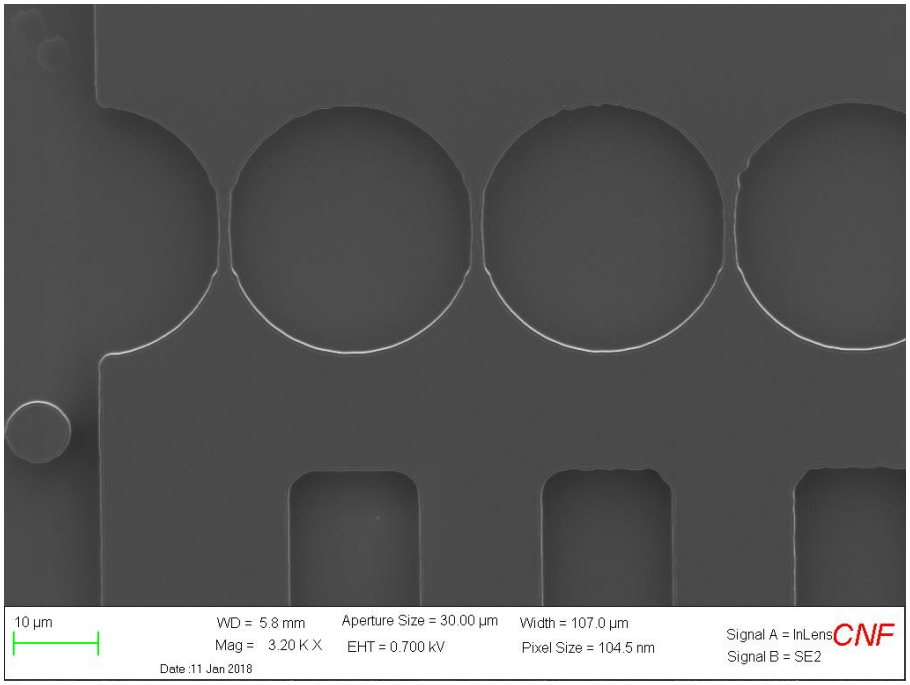


Figure 3-23: Scanning electron microscope image of a row of 1µm constrictions between 29 µm etched holes into silicon.

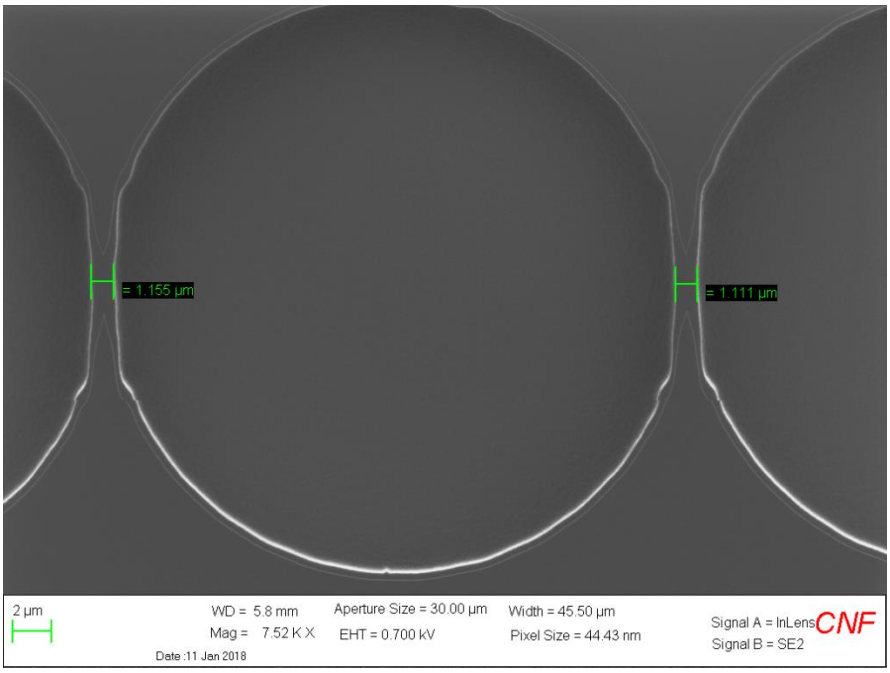


Figure 3-24: A pair of measurements from a scanning electron microscope of 1µm constrictions gaps created from etching 29 µm holes into silicon.

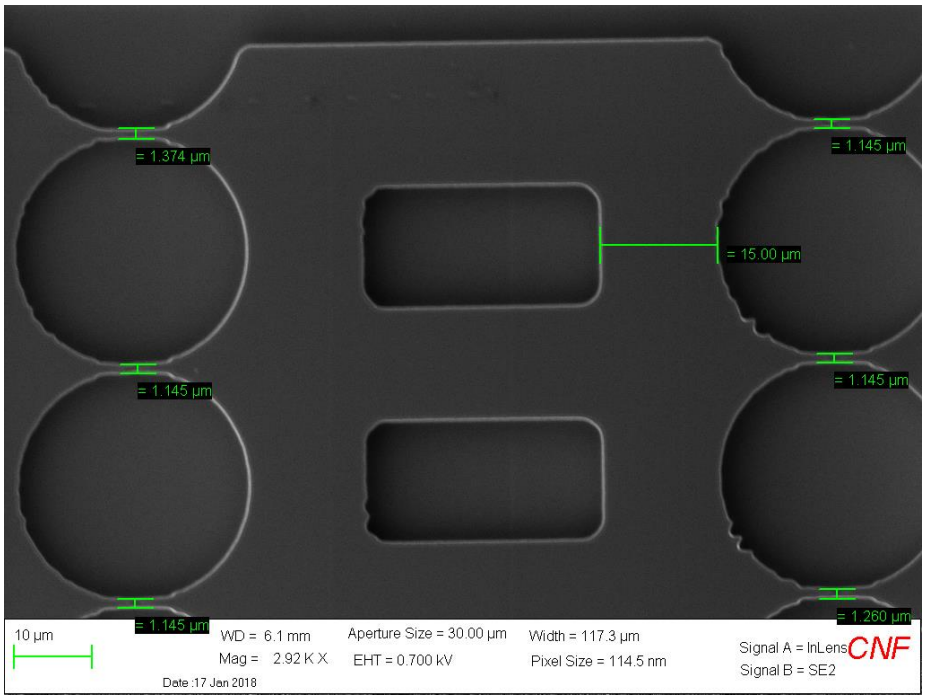


Figure 3-25: Multiple measurements from a scanning electron microscope of 1µm constrictions gaps created from etching 29 µm holes into silicon.

3.4 Reactive Ion Etching

ICP-RIE is a combination of the high selectivity and enhanced chemical reactivity of free radicals with the vertical directionality of concentrated ion bombardment (Nojiri, 2015). Because ICP-RIE is a completely different etch process than DRIE, photolithography optimized for other approaches may not give the same results. Unlike DRIE, the etch rates are much lower for ICP-RIE silicon, which translates into a slower etch. The ICP-RIE process is straight etching and lacks any other deposition or breakthrough steps, so the dimensions of our etch mask must be able to hold up to thirty-five minutes of intense plasma etching. Any mask erosion or undercutting may impact the critical feature sizes in ways that were not observed with DRIE.

The photonics etch (Table 3-1) on the Plasmatherm Unaxis SLR 770 was chosen due to its unique capability to produce smooth anisotropic sidewalls in silicon. For photonics applications, the reduction of etched sidewall surface roughness and defects are extremely important for minimize optical losses (Feng, 2009). This etch recipe was also compatible with our current AZ nLof 2020 lithography for etching 5 μm into silicon. As with the DRIE, SF_6 disassociates into fluorine radials when infused into an argon plasma. These fluorine atoms bind with any exposed silicon to produce volatile silicon tetrafluoride and other silicon-fluorine compounds (SiF_4 & SiF_x). Fluorine radicals tend to undercut the mask, which is why increasing the ion density with ICP-RIE is critical for maintaining vertical sidewalls (Shul & Pearton, 2012). The C_4F_8 inhibits isotropic etching while oxygen free radicals scavenge any free carbon atoms to produce volatile carbon monoxide (CO), carbon dioxide (CO_2) (Ji et al., 2017) and carbonyl fluoride (COF_2) (Mohamed & Alkaisi, 2013).

Photonics Recipe (sccm)	C_4F_8	SF_6	Ar	O_2
Light Plasma	2	2	40	10
Etch	56	24	40	10

Table 3-1: The Photonics Etch Gas Recipe

For our first trial (Appendix D), I patterned a Design # 6/single cell migration device wafer (Figure 2-26) and used the same 1.7 seconds exposure time needed for replicating DRIE Design # 6 (Chapter 2.5) in AZ nLof 2020 photoresist. It is important to mention that varying the exposure dose and increasing post exposure bake time and temperature undercuts the resist profile (AZ nLOF 2000 Serie, 2016), so keeping consistent baking times and temperature are vital for reproducible results. This first trial wafer was etched for half of the estimated etch time and measured on a profilometer in order to establish an etch rate. After twenty-four minutes of RIE, 3.1-3.2 µm of silicon was etched with 1µm of resist remaining, which corresponds to a 0.13 µm/minute etch rate. The wafer was etched for another fourteen minutes to a measured depth of ≈5.0µm with 0.5-0.6 µm of resist remaining.

The final step for DRIE and RIE was removing the photoresist off the wafer. Photoresist can be stripped by using either solvents or subjecting the wafer to an oxygen plasma. Soaking in acetone will remove most resists in five to sixty minutes (depending on the resist chemistry and any possible polymerization created from plasma etching). The concerning aspect of solvents are the organic residues that they leave after drying. Residues may lead too poor SU-8 adhesion and defective migration devices. If solvents are the only option, it would be advised to never let them dry on the wafer and rinse twice with IPA and water afterwards.

The semiconductor industry was also concerned about solvent use in their facilities and was searching for other means to remove photoresist while maximizing throughput. They found that a small amount of oxygen mixed within an argon plasma would burn off or ash almost all organic compounds off a wafer's surface with little to no effect to the silicon. Oxygen plasma stripping became an industry standard and was one of the earliest applications of plasma etching in microfabrication (Donnally and Kornbilt, 2013). Before parallel plate etching, argon plasmas were generated in a quartz barrel type chamber wrapped with an external coil. As RF power increases around the argon-injected environment, a plasma is generated. The excited ions and electrons reduce double bonded oxygen molecules into free oxygen radicals, which in turn attack and break down the hydrocarbon chains of photoresist into volatile products such as CO and CO_2. What is unique about these barrel ashing tools are their capabilities of simultaneously stripping resist off both sides of wafers in large volumes. For comparison, parallel plate etch chambers can usually only uniformly stripping resist off the exposed side of one single wafer at a time. For our applications, either was found to be adequate.

The RIE holes appeared to have the correct dimensions, but after stripping the photoresist, the final silicon hole were etched much too wide. The diameters of the holes were measuring 7 µm instead of the intended 5µm (Figure 3-26). This was anticipated with running a new process for the first time and it eventually took many trials to nail down the best exposure times (Figure 3-27) for each type of device (Table 3-2 & 3-3). The 5 µm pillars of Design # 6 required a 3.5 second exposure time (Figure 3-28) while 4.0 seconds produces good resolution of the 1 µm gaps (Figure 3-29). Once we secured the exposures times for each design type, fabricating these devices became fairly routine and the results were far superior to both the SU-8 and DRIE versions. Not only did the holes have smooth sidewalls

for PDMS molding, but we were still able to reduce time and cost by creating a high yield fabrication process. Utilizing plasma etching will open doors for future microfluidics devices and intricate PDMS molds.

Wafer	Exposure Time (seconds)	Design # 6 Pillar Diameter (µm)
1st Photonics test wafer	1.8	7
Fused Silica Test	3.0	6
2nd Photonics wafer	4.0	4 on "all" devices, 3-3.5 on design 6 devices
3rd Photonics wafer	3.5	4.8

Table 3-2: Exposures Times with correlating measurements for 5 µm pillars.

Wafer	Exposure Time (seconds)	1 µm Gap Measured(µm)	10 µm Gap Measured (µm)
1st Photonics test wafer	1.8	Etched Through	7
Fused Silica Test	3.0	Etched Through	9
2nd Photonics wafer	4.0	1	10
3rd Photonics wafer	3.5	Etched Through	9

Table 3-3: Exposures Times with correlating measurements for 1 & 10 µm gaps.

This feature size/exposure time information may be helpful future researchers if they desire to create larger pillars or different gaps with the same photomask. Future researchers should also consider moving the ICP-RIE process to a different etcher. The Plasmatherm Unaxis SLR 770 is primarily a DRIE etch tool and the chamber needs to be coated or seasoned with the byproducts of that etch or irregularities and inconsistent will add variability to other projects. In order to RIE etch in that chamber, all the polymer byproducts from DRIE needs to be removed with a ten minute photonics etch on a dummy wafer before etching our device work. After our thirty-five minute etch is completed, the RIE byproduct must be remove with SF_6 with the 0Release recipe for forty minutes or the Photonics etch time + five minutes. A logical alternative would be etching our devices with hydrogen bromide (HBr) on the Oxford Instruments' Cobra ICP Etcher at the CNF. Bromide will etch silicon at a slower rate than fluorine (Donnelly & Kornblit, 2013), but less likely to undercut the mask and capable of producing flat trench bottoms with fewer etch defects (Wagner & Nine, 2013).

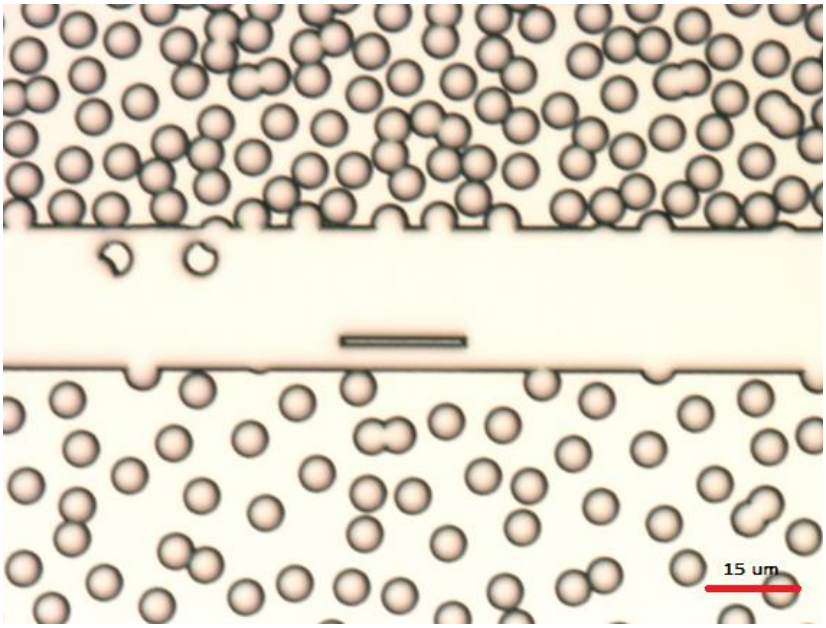


Figure 3-26: First trial run using the Photonics etch for replicating Design # 6. Holes for PDMS pillars were ≈ 7 µm in diameter after using AZ nLOF 2020 with an exposure time to 1.8 seconds as a etch mask (50x).

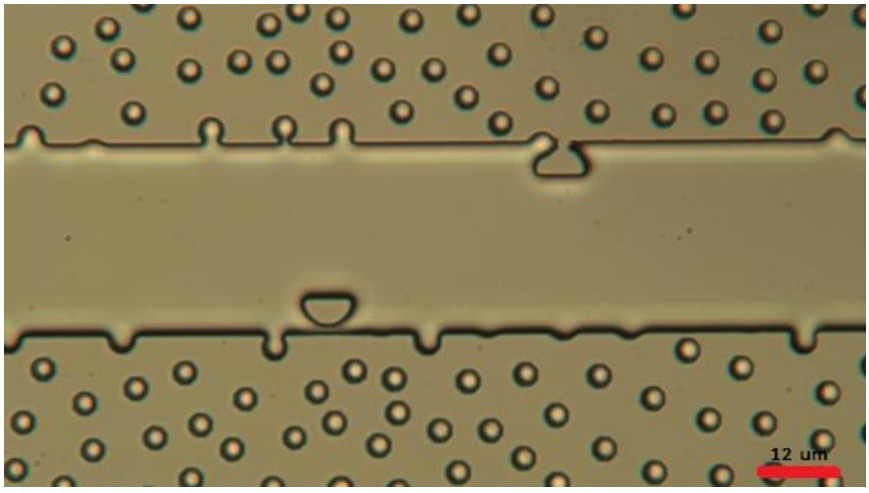


Figure 3-27: Second trial run using the Photonics etch for replicating Design # 6. Holes for PDMS pillars were ≈ 3-4 µm in diameter after increasing the AZ nLOF 2020 exposure time to 4.0 seconds (50x).

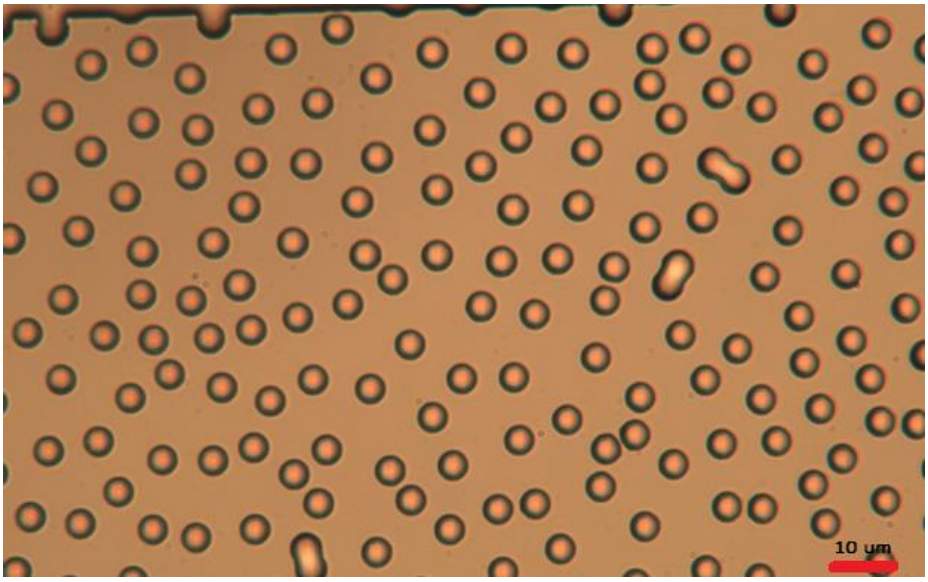


Figure 3-28: Third trial run of using the Photonics etch for replicating Design # 6. Holes for PDMS pillars were ≈ 5 µm in diameter after reducing the AZ nLOF 2020 exposure time to 3.5 seconds (50x).

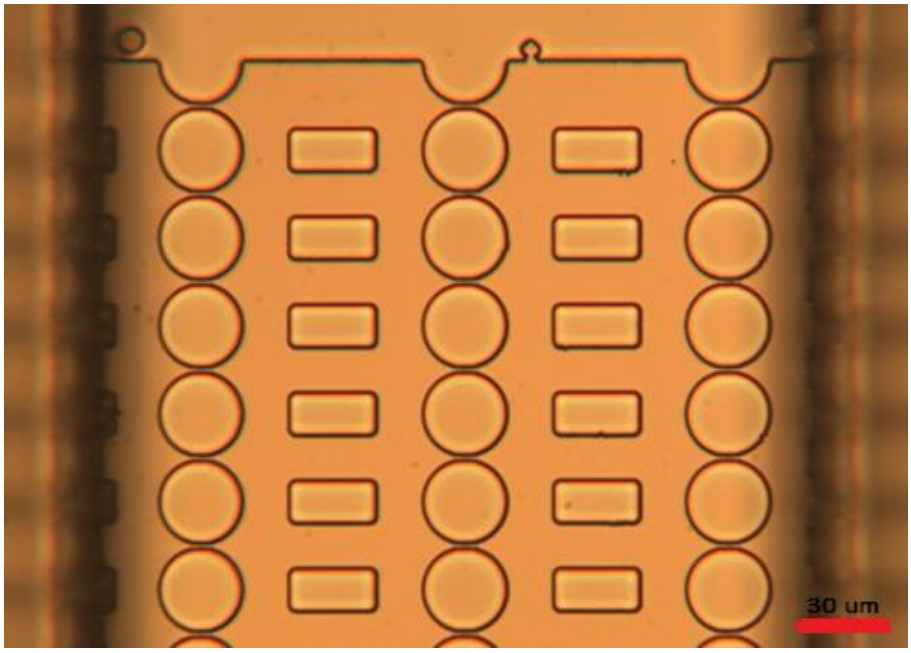


Figure 3-29: 1 µm gaps created by etching 29 µm holes with the Photonics RIE process. The 200 µm SU-8 layer is surrounding the constriction channel (20x).

3.5 Upper SU-8 Layer

With all the emphasis on the 5 µm critical features, it is important to optimize the fabrication of the bypass channels, cell chambers and alignment marks. While the top layer design has not changed from previous work (Davidson, et al., 2015), I was able to improve the process flow have been and the fabrication steps.

First, previous researchers reported issue with adhesion between the first SU-8 layer and the second. SU-8 developer is a noxious solvent and extremely difficult to remove off glassware and wafers. The best solution we found was to rinse the SU-8 developer with 2-propanol (IPA) and gently with DI water twice before drying with low pressure nitrogen and an overnight dehydration bake @ 90^{o}C. For the silicon work, an oxygen plasma to remove any remaining photoresist followed by a hot piranha etch and an overnight dehydration bake @ 90^{o}C was effective.

We recognized that the heights of the bypass channels and chambers could be lower and decided to reduce the SU-8 thickness from 250 µm to 200 µm, which required new spin curves. Previous work used SU-8 2075 with the spin recipe in Table 3-4. Microchem designates numbers for their SU-8 formulations based on their expected thicknesses at 3000 RPM (the thickness of SU-8 2002 should be 2 µm @ 3000 RPM, SU-8 2005 is 5 µm and SU-8 2075 is 75 µm). Reducing the spin speed lowers the centrifugal force, leaving more SU-8 on the wafer. This translates into a thicker film, but there is a limit on how slow the speed should go before a lack of uniformity becomes an issue. At the CNF, the rule of thumb is not to reduce the spinner bowl speeds below 1500-2000 RPM. For better uniformity, I needed to find a SU-8 formulation that was closer to our target thickness. After some testing, spinning SU-8 100 @ 1500 RPM worked the best (Table 3-5).

Spin Curve for 250 µm of SU-8 2075	RPM	R/S	Seconds
Ramp Up	**500**	**100**	**10**
Spin	**1000**	**100**	**60**
Ramp Down	**100**	**100**	**15**

Table 3-4: Original 250 µm SU-8 Spin Curves

Spin Curve for 200 µm of SU-8 100	RPM	R/S	Seconds
Ramp Up	**500**	**100**	**10**
Spin	**1500**	**100**	**60**
Ramp Down	**100**	**100**	**15**

Table 3-5: 200 µm SU-8 Spin Curves

Spin speeds are not the only factor affecting SU-8 uniformity. The original pre-exposure and post–exposure bakes would often cause the SU-8 films to crater or pit during baking. If theses recessions or low points are involved in our photolithography, the developed features in these lower areas will be further away from the photomask resulting in diffraction and wider features. From experimentation, these craters were more likely to form during the pre-exposure bake when the temperature was too high or the ramping rate was too fast. The best pre-exposure recipe for preventing film deformation was to initial ramp the SU-8 from room temperature (RT) to 62.5-63.5^{o}C for seven or eight hours at a ramp rate of 1.5^{o}C/second and then increasing to 67.5^{o}C for fourteen hours or overnight. This same recipe @ 68.5^{o}C did produce craters.

Finally, the original exposures times were much too long and needed to be shortened in order to retain the true dimensions of the photomask. Contact lithography exposures were originally done on the ABM contact aligner for six cycles of 60 seconds, which was excessive even for the 250 µm thickness. Time was slowly removed from the exposure over the course of two years (Table 3-6) until it was determined that six cycles of 36 seconds was suitable.

Wafer Number	Pre-Exposure Temperature & Time	Exposure Times
1	55 ^{o}C for 22 hours	50.0 Seconds x 6
2	56.5 ^{o}C for 22 hours	45.0 Seconds x 6
3	57.5 ^{o}C for 22 hours	40.0 Seconds x 6
4	60 ^{o}C for 7 hours & 62.5 ^{o}C for 18 hours	37.0 Seconds x 6
5	60 ^{o}C for 7 hours & 62.5 ^{o}C for 17 hours	36.5 Seconds x 6
6	60 ^{o}C for 8 hours & 63.5 ^{o}C for 16 hours	36.2 Seconds x 6
7	61 ^{o}C for 7 hours & 63.5 ^{o}C for 16 hours	52.5 Seconds x 4
8	62 ^{o}C for 6.5 hours & 66 ^{o}C for 17.5 hours	35.0 Seconds x 6
1st DRIE Test	62.5 ^{o}C for 7 hours & 67 ^{o}C for 16 hours	34.5 Seconds x 6
1st Photonics Test	62.5 ^{o}C for 6 hours & 68 ^{o}C for 17 hours	34.1 Seconds x 6
1st Fused Silica Test	63 ^{o}C for 9.5 hours & 68 ^{o}C for 13.5 hours	33.8 Seconds x 6
2nd Photonics Test	63.5 ^{o}C for 6 hours & 68 ^{o}C for 17 hours	33.5 Seconds x 6
3rd Photonics Test	63.5 ^{o}C for 6 hours & 68 ^{o}C for 20 hours	33.2 Seconds x 6
4th Photonics Test	64 ^{o}C for 7 hours & 68.5 ^{o}C for 17 hours	33.0 Seconds x 6

Table 3-6: Exposure times for upper SU-8 layer

3.6 Removing SU-8

From a fabrication standpoint, one of the most important aspects of this RIE silicon/thick SU-8 stack is the ability to liftoff the SU-8 layer and re-use the etched constrictions. The weakest point to any SU-8 device is its substrate adhesion and for our devices, when a bypass channel come off after repeated PDMS molding, the researcher usually discarded the device and fabricates a new one. We discovered that a long-term detergent soak could remove all the remaining SU-8 giving us the opportunity to spin on another layer of SU-8 and save the silicon etched devices.

The CNF recently approved a proprietary chemical stripper referred to as Techistrip P1316. Supposedly, this chemical when heated to 70^{o} C is able to remove SU-8 off silicon substrates without damaging the surface. The ability to remove SU-8 could be beneficial to our research. Not only could we reuse damaged devices, but this also opens up the possibilities of using oxygen plasma for etching residual PDMS from the collagen mimic devices. The initial drawbacks of J1316 are the chemical costs and it contains some hazardous chemicals such as TMAH (tetramethylammonium hydroxide) and DMSO (dimethyl sulfoxide).

The initial trial of heated P1316 removed a full wafer of 20 µm thick SU-8 features after sixty minutes along with one of our 5 µm SU-8 constriction layer wafers. Under a microscope, all traces of the previously deposited SU-8 had vanished. The same solution had no effect after 72 hours @ room temperature on another 5 µm SU-8 constriction layer wafer. I achieved some success by heating another recently cross-contaminated 200 µm SU-8/RIE wafer in the same solution issue for one hour. While most of the larger 200 µm features remained, some of the smaller features and bypass channels came off. Under the microscope, it appears that the P1316 is not dissolving the SU-8, but actually undercutting the SU-8/silicon substrate interface (Figures 3-30 & 3-31). Strangely, the P1316 still has little effect on the

second 5 µm wafer. I later determined that P1316 lost its potency after heating and solution could not be reused more than twice. This could be due to the volatility of DMSO.

After the same P1316 trials, the same SU-8/RIE wafer was soaked in a DI water/dawn detergent solution over the weekend. I discovered that a long surfactant soak, loosen up the bonds between the SU-8 and the silicon substrate. After ≈ 72 hours in the detergent solution, most of the features came off easily when massaged gently with a gloved thumb (Figures 3-32 & 3-33). Using a new detergent bath helped remove all the remaining features 24 hours later.

In order to use the wafer again, all traces of the detergent have to be removed. The wafer was first soaked overnight in DI water and then rinsed three times using the Hammatech's "Rinse & Dry" recipe (figures 3 -34 & 3-35). A hot piranha etch (three parts concentrated sulfuric acid and one part 30% hydrogen peroxide) was done to strip away the remaining organic residues off the substrate (Figures 3-36 & 3-37) and baked overnight @ 90^{o}C. I was able to successfully re-applied 200 µm SU-8 on the stripped substrate later that week.

Further work explored the reproducibility and limitations of this process. First, it had to be determined if detergent and water alone could liftoff all the SU-8. I spun and removed 200 µm of SU-8 on a previously unused DRIE etched wafer after fifteen days. Next, as a good test of reproducibility, SU-8 was spun and removed multiple times off the same wafer with detergent solution. Again, a previously unused 5 µm DRIE etched wafer was water rinsed, hot piranha cleaned and baked overnight before spinning SU-8. As a way to offer possible scenarios for using this technique, wafer was purposely slightly misaligned with the photomask. After five days in the solution, SU-8 undercutting was pronounced (Figure 3-38) and some of the smaller alignment marks and bypass channels had completely detached (Figures 3-39 & 3-40). About half of the smaller alignment marks and all the bypass channels detached after twelve days in solution (Figures 3-41 & 3-42) and most of the cell chambers by nineteen days

(Figures 3-43 & 3-44). All the SU-8 features came off in thirty-one days. I conducted the test again, but this time without direct physical contact to the features. With the absence of physical force, it took fifty-one days to strip the wafer of SU-8. The detergent solution stripped 160 µm of SU-8 off another wafer (Figure 3-45), but seems to have little effect on the thinner 5 µm layer of SU-8. It may be safe to assume that the film stress of the SU-8 combined with the surfactant undercutting action may instigate the delamination. Future research should investigate how film stress and thickness affect this process.

Most recently, a heated surfactant bath successfully removed 200 µm hard baked SU-8 features off a device wafer is less than thirty-six hours. This SU-8 layer suffered from undercutting due to magnetic stirring during development. The experiment initially submerged the wafer in a 95^{o}C bath of deionzied water with two drops of Triton X-100 for two hours resulting in the removal of most of the bypass channels and alignment marks. The remaining features were removed after sitting in the bath overnight and heating for another hour the next day. Unlike the removal with Dawn detergent, the heated Triton X-100 left traces of the SU-8 features outlines and surface staining upon the wafer that could not be removed by oxygen plasma stripping or multiple hot piranha etches (Figure 3-46).

Figure 3-30: Undercutting of SU-8 under the 200 µm cell chamber after 60 minutes in J1316 @ 70^{o}C (2.5X)

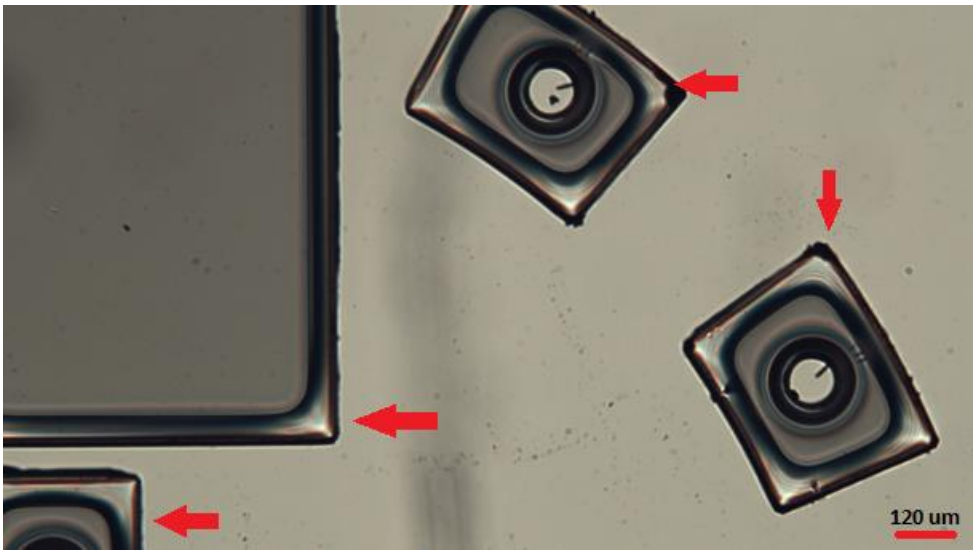


Figure 3-31: Undercutting of SU-8 features at all the corners and edges after 60 minutes in J1316 @ 70^{o}C (2.5X)

Figure 3-32: Missing 200 µm features on RIE migration device wafer. The upper left-hand corner of the wafer still has the remaining 200 µm features after soaking for ≈ 72 hours in a Dawn Detergent/deionized water bath. The red circle highlights the reflection of the RIE 5 µm constrictions.

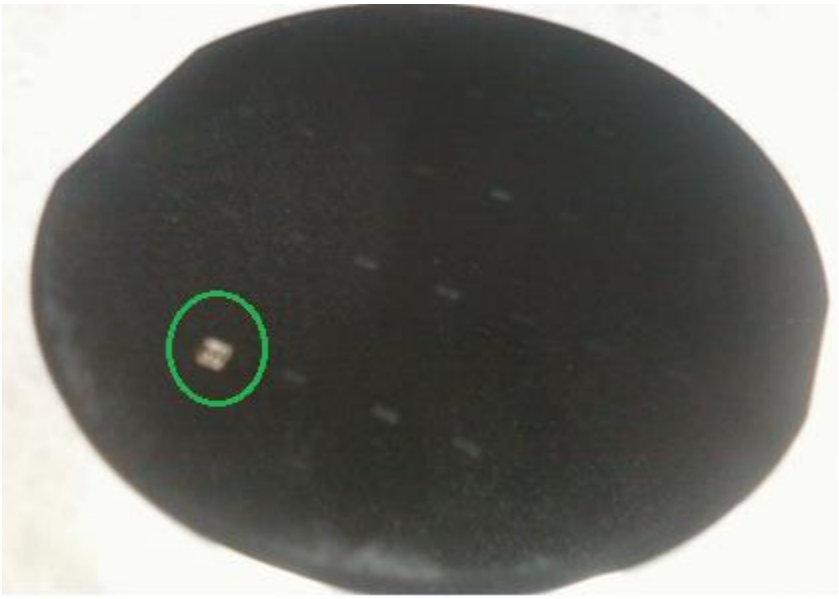


Figure 3-33: The final 200 µm feature (circled in green) on RIE migration device wafer after soaking for ≈ 96 hours in Dawn Detergent/deionized water bath. The reflection of the Reactive-ion etched 5 µm constrictions can be seen on the wafer.

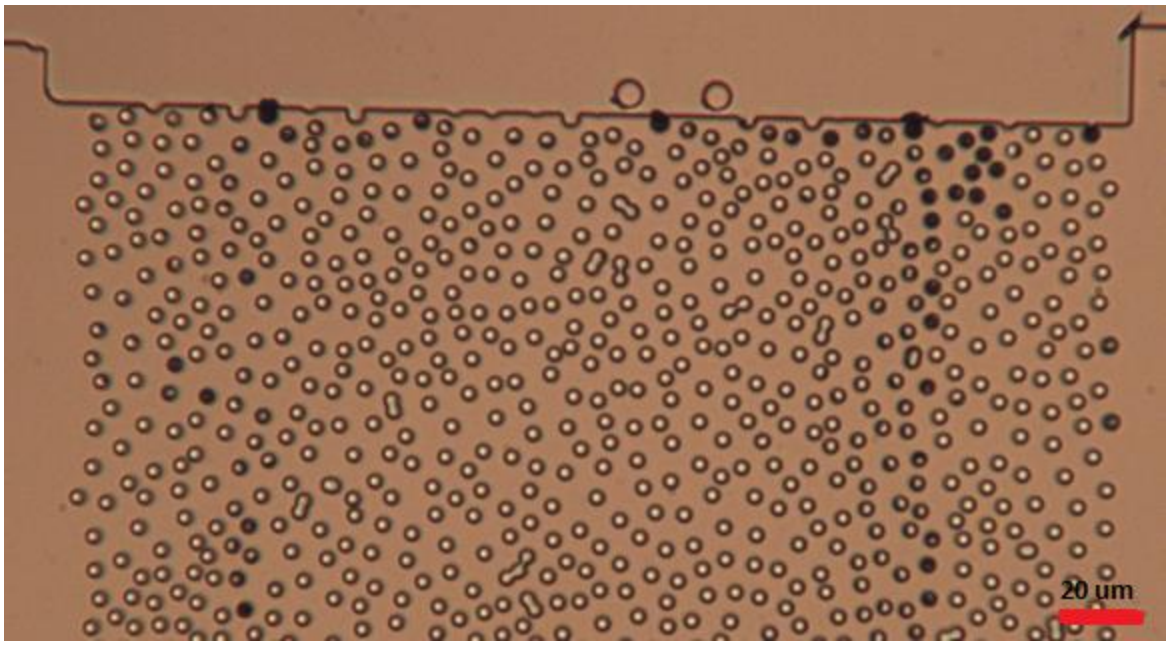


Figure 3-34: Silicon etched 5 µm holes after Dawn detergent bath SU-8 removal and multiple rinses in deionized water (20x).

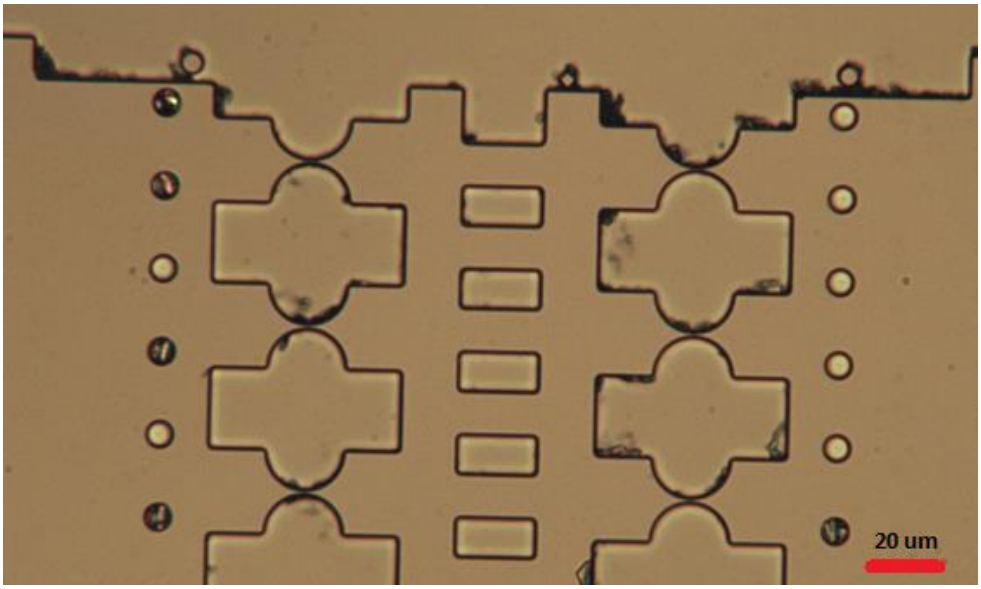


Figure 3-35: RIE Migration device constriction channels after DI after detergent SU-8 removal and multiple DI water rinses (20x).

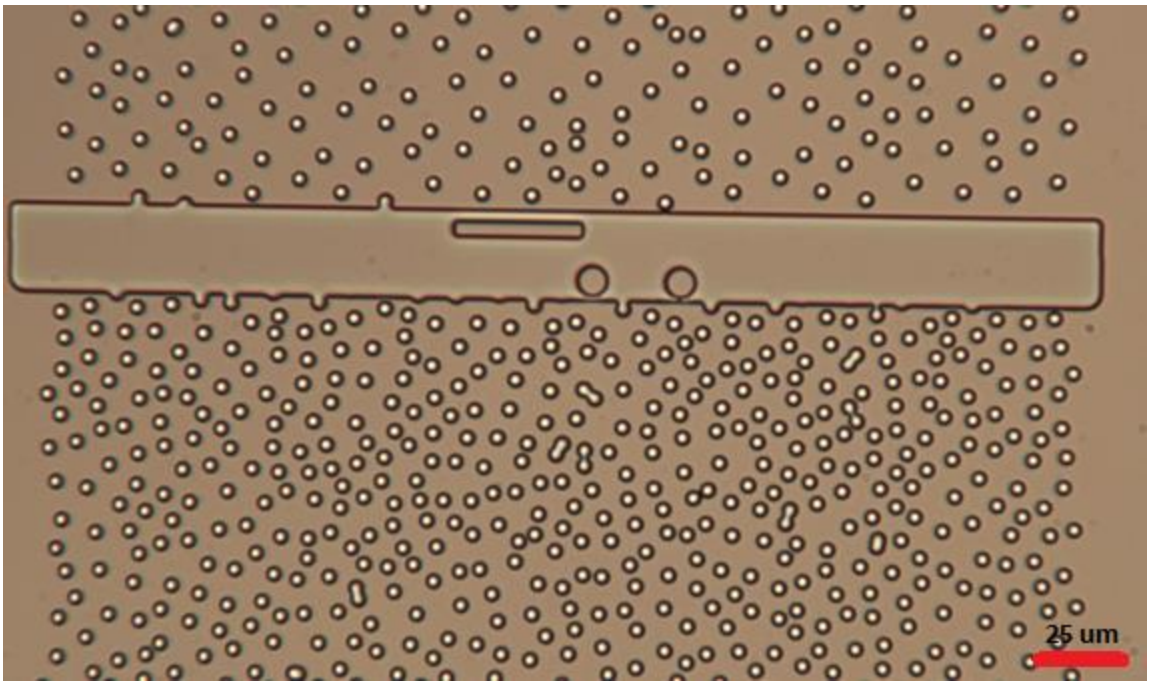


Figure 3-36: Silicon etched 5 μm holes after hot piranha etch removed all the organic debris (20x)

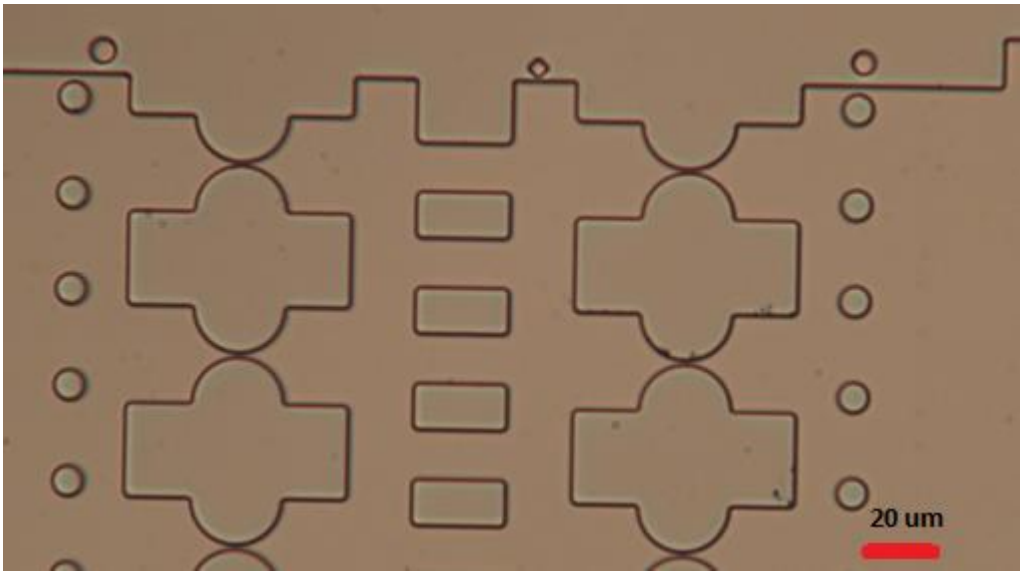


Figure 3-37: RIE migration device constriction channels after hot piranha etch removed most of the organic debris (20x).

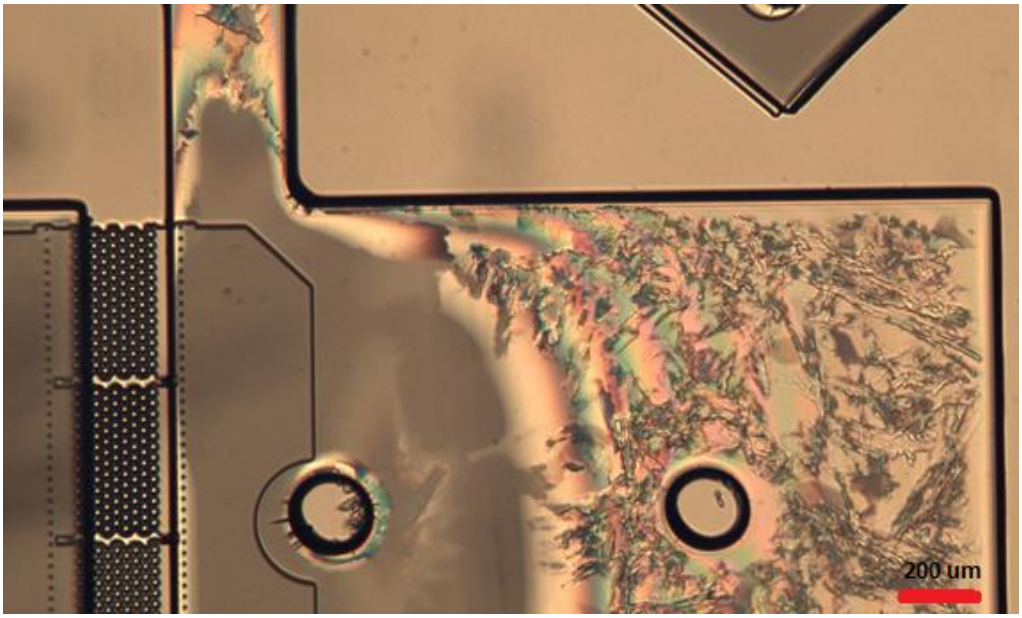


Figure 3-38: Misaligned 200 µm SU-8 features undercut after five days in Dawn detergent solution (2.5x)

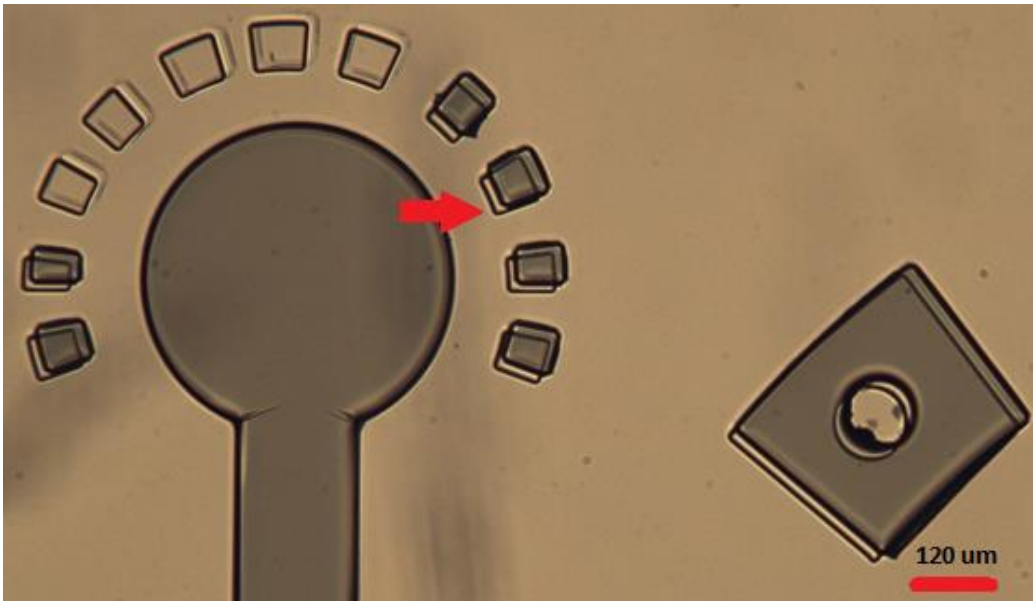


Figure 3-39: Misaligned 200 µm SU-8 features removed after five days in detergent solution (2.5x). The outlines underneath the SU-8 features (indicated with the red arrow) are actually etched into the silicon as a result of an older mask that had the alignment marks on the 5 µm mask.

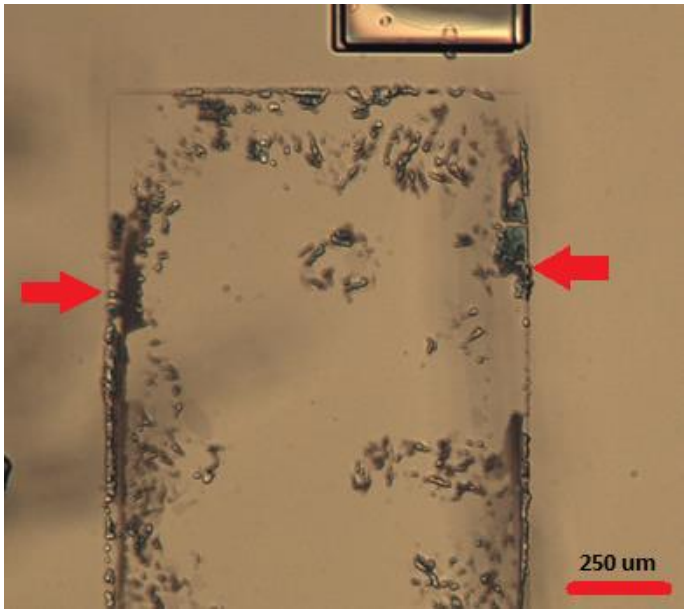


Figure 3-40: Red arrows mark the SU-8 outline of a detached bypass channel left behind on the wafer after five days submerged in a Dawn detergent solution (2.5x).

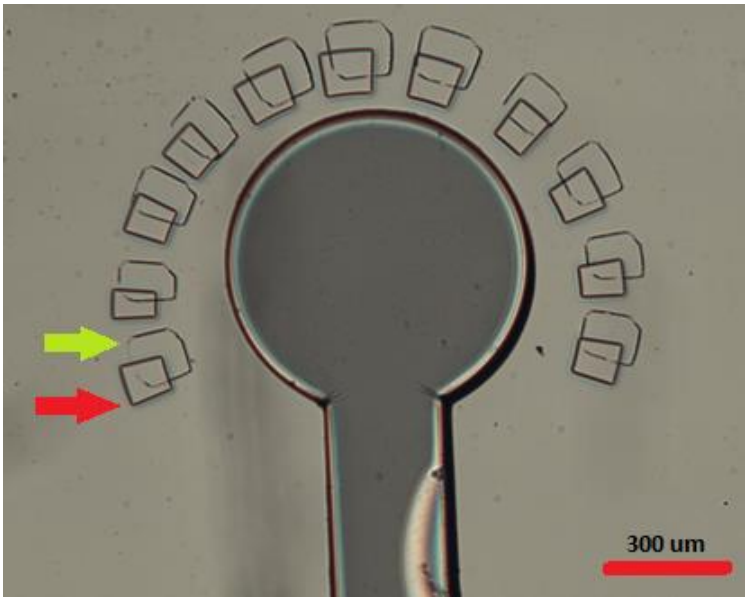


Figure 3-41: SU-8 alignment marks completely removed around the cell seeding port after twelve days in Dawn detergent solution (2.5x). Green arrow points to the SU-8 outline that remains after the bulk SU-8 detached from the wafer. The red arrow is the etched silicon alignment marks from an older the 5 µm layer mask design.

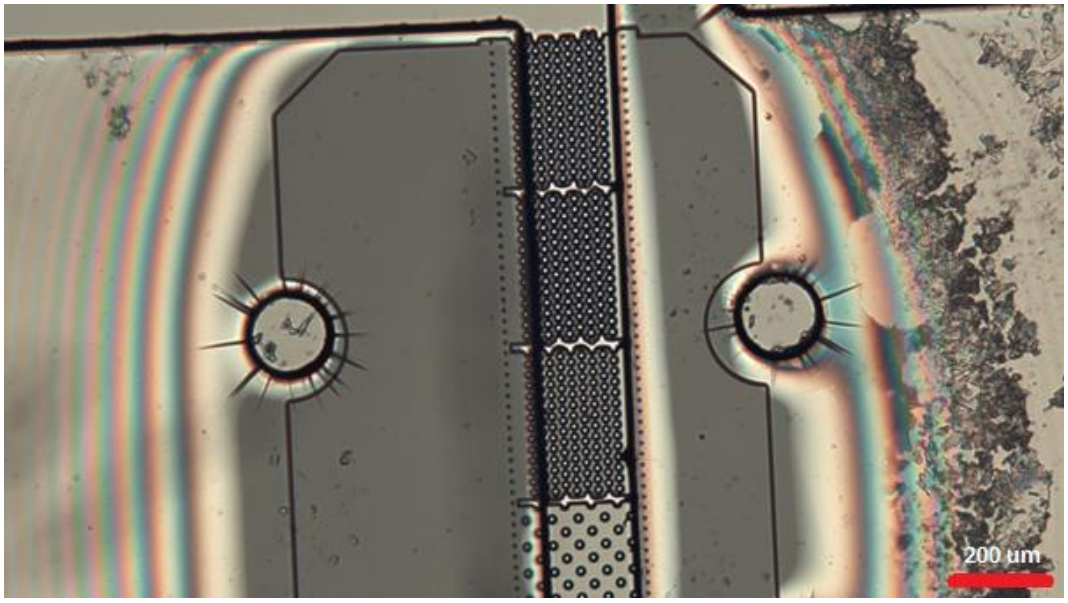


Figure 3-42: Further undercutting of the SU-8 cell chambers after twelve days submerged in a Dawn detergent solution (2.5x).

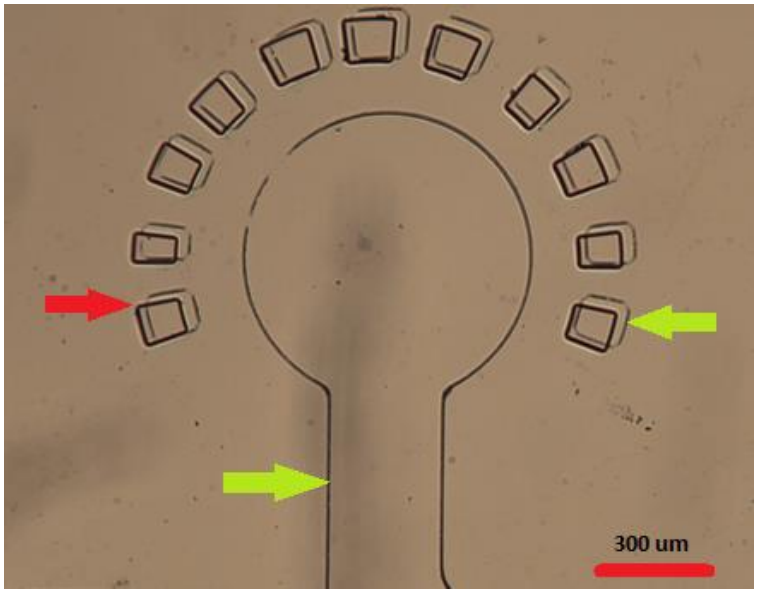


Figure 3-43: Complete removal of SU-8 cell seeding port and alignments marks after nineteen days submerged in Dawn detergent solution (2.5x). Green arrows points to the SU-8 outlines that remains after the bulk SU-8 detached from the wafer. The red arrow is the etched silicon alignment marks from an older the 5 µm layer mask design.

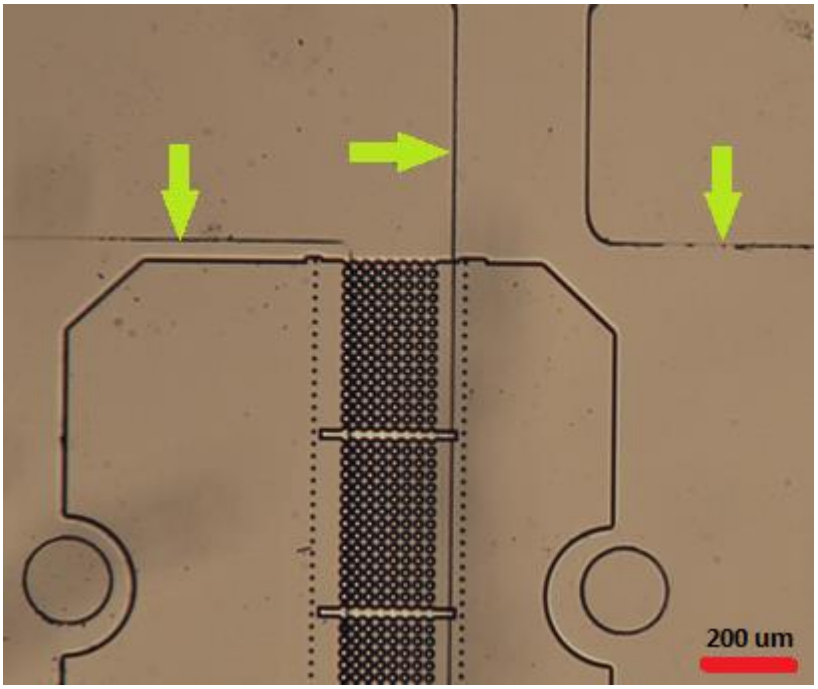


Figure 3-44: Misaligned SU-8 feature removed after nineteen days in detergent solution (2.5x). Green arrows points to the SU-8 outlines that remains after the bulk SU-8 detached from the wafer.

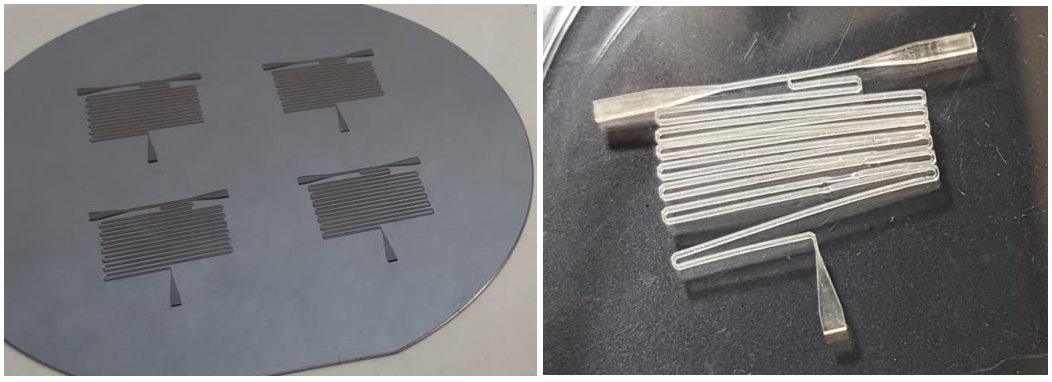


Figure 3-45: A complete SU-8 microfluidic device mold released from a silicon wafer. Left: Four, 160 µm thick SU-8 devices patterned on a four-inch wafer. Right: Released device after submerged in heated Triton X-100 detergent solution for three hours.

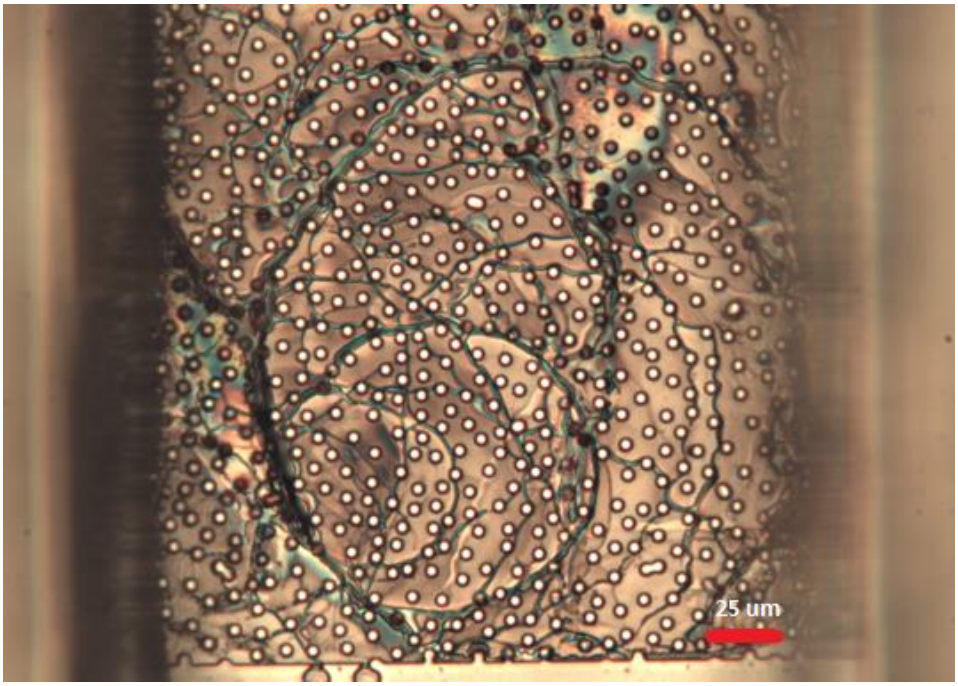


Figure 3-46: Surface staining after submerged in heated Triton X-100 detergent solution for three hours (20x). The constriction channel is surrounded by 200 µm SU-8 cell chambers.

3.7 Inverted Migration Device Design

We recently began the initial work on inverted cell migration device which would eliminate the use of PDMS for our constrictions. This thesis has demonstrated the capabilities of plasma etching for fabricating closely packed holes in silicon. This same technology can also be configured for etching alternate substrates. One concept we have discussed was fabricating a transparent device with etched pillars array instead of holes for PDMS molding. The PDMS molded cell chambers, bypass channels and ports from the original device would remain (Figures 1-2 – 1-4) except from the constriction channel. The 5 μm pillars would be etched into the "cover glass" base (Figure 1-10) of the device with the rest of the PDMS molded device located on top (Figure 3-47). Etched pillars provides a permanent and reusable solution for our constriction needs. No longer would our most critical feature be dependent on PDMS molding which sometimes resulting in torn or missing pillars, damaged SU-8 and constriction/chamber collapsing. The transparency would also open up these devices to different microscopy and imaging methods.

Microscope slides may be the biologist material of choice, but are high discouraged in the nanofabrication community as a suitable substrate. Microscope slides are usually made of poor quality soda lime glass which is banned in all of the etch tools at the CNF due to its high concentration of sodium, calcium and magnesium. Fused silica (also called fused quartz) with its chemical purity, ultraviolet transparency and wealth of etch history at the CNF made it the obvious choice for this application.

Before spending the time and resources on etching the standing pillars into fused silica, we needed to determine whenever fluid would flow through this design and whenever we could etch smooth side-walled, single micron features into the transparent substrate. As a proof of concept, we

decided to DRIE the inverse design into silicon. In nanofabrication, simple experimental trials can be very useful for discovering design flaws before spending a lot time and effort on the final process.

3.8 Creating Silicon Pillars

The first step for our next generation device was to see if we could create pillars in the substrate instead of holes with the same photomask. This "top-down" approach to fabricating these devices was quite different than using SU-8 to build our devices, so some new tooling and reagents would need to be utilizes. As mention, to reduce cost and because this initial attempt was a proof-of -concept experiment, an N-type silicon wafer was used instead of fused silica. Similar to the previous work, AZ nLof 2020 was spun and exposed with hard vacuum contact lithography for 1.6 seconds. This was one tenth lower than the previous work (it is important not to get too comfortable with a process; there is always room for improvement.) Next, we used lithography technique known as "lift-off" to reverse the negative image from the AZ nLof 2020 into a positive hard etch mask. For lift-off, the negative resist is not an etch mask, but a sacrificial layer for patterning the inverse or positive tone design on to the wafer. This was done by electron-beam evaporating a small thickness (50 nm) of aluminum oxide (Al_2O_3) on the exposed silicon and patterned photoresist surfaces. Evaporation is a physical vapor deposition method for perpendicularly depositing metals, oxides or other materials on to a substrate. By only depositing on the horizontal surfaces and not the sidewalls, solvents such as acetone can penetrate, swell and float or lift off the Al_2O_3 coated negative photoresist, leaving a positive hard mask of our image on the wafer (Figures 3-47 & 3-48).

Significantly less area was needed to be etched in the positive tone compared to the negative tone design, so the loop count required was estimated to be half of what was used previously. After a 35 loop warm-up on a dummy wafer, 10 loops were etched using the Plasmatherm Uniaxis SLR 770. The

measured step height was ≈7.2 µm; giving us a 720 nm etch/per loop for this positive tone design (compared to the 310 nm/per loop etched for the negative tone). After etching has been completed, Al_2O_3 was removed with a 20 second hydrofluoric acid dip and then rinsed repeatedly with DI water.

Overall the deep reactive-ion etched pillar devices exceeded expectations. The pillars were the correct diameter without any sign of distortion or breakage (Figures 3-50 & 3-51). I am slightly concerned about residual etch scalloping and some lower level bridging between pillars in close proximity, but this should not be an issue when we reactive-ion etch the features into fused silica. Any issues that do arise with pillar wall angles can later be optimized by adjusting the etch recipe parameters. As observed in the initial DRIE test on design # 1 -6 (Chapter 3.3), the standard migration style devices will require a longer exposure time to accurately create the correct feature sizes (Figure 3-52).

It is important to note that a visual inspection of the wafer is always important before continuing to the etch step. Often in liftoff, some the Al_2O_3/resist mask remains on the wafer or is held by stiction to another location (Figures 3-53 & 3-54). To remove the undesired remnants, first, try sonicate the wafer in acetone for 5-10 minutes. If that is not effective, heat the wafer on a hotplate set @ 110^{o}C for 60 seconds and immediately continue to sonicate in acetone. Lightly scrubbing the wafer with an Alpha Swab soaked in acetone also works, but may damage the desire areas of the mask.

Slabs of PDMS were initially used to cap the device. Each piece was functionalize in a plasma for 30 seconds and laid upon one of the pillars migration devices for a good seal. Holes were punched on either side of the device for dye (food coloring) to track if liquid and later cells could possible move through the pillars (Figure 3-55). Punching the two ports was much more difficult than anticipated. Ports made with smaller hole punches kept missing the target area giving validation for the use of alignment marks. Eventually, larger punches were used, but the results were inconclusive (Figure 3-56); it appears

that dye had passed through the pillar array, but it may have also travelled over the pillars and not through the constrictions. The next iteration should have a much wider area for holes or ports so that adding dye or seeding cells would be much easier. In addition, too much force may have been used to push down the functionalized PDMS, which could have restricted the flow through the constrictions.

Adding or extending the etched area around the standing pillars may make loading dye or cells much easier. Plus, the importance of the bypass channels was illustrated by the lack of fluid movement in the initial test. The easiest way to test this was to overlap the 200 μm mask with the 5μm pillars designs and etch them both to the same depth. The challenge was finding a way to use a positive and negative tone image together which requires spinning two different photoresist at some point on the same wafer so that the same Al_2O_3 mask could be used for the whole design. This was important because all the features would have the same etched depth if both images were etched at the same time. My first attempt was spinning and exposing the pillars design using AZ nLOF 2020 first with hopes that the double baking steps would solidify the AZ nLOF resist enough to spin and expose the Shipley 1813 on top of it. The AZ nLOF 2020 turned out to be soluble in Shipley 1813 resist resulting in only an exposure of the 200 μm layer without any trace of the pillar designs. With some experimentation, a pair of resists may be found to work in tandem for this process, but for the time being, the new plan was to etch the critical pillar designs first then etch the bypass channels and migration device afterwards (Figure 3-57).

It is important to point out that spinning photoresist with any uniformity on a deep etched wafer is difficult. The surface irregularities interfere with the ability of the photoresist to evenly spread outwards during spinning. Large amounts of resist ends up collecting against the high points and pooling in the recessed areas. This pooling of resist may help mask and protect the pillars from the second etch (Figures 3-58 & 3-59), but after going through this process, the second resist cycle covered only the base

and not the tips of the standing pillars. This lack of coverage resulted in pillars narrowing from the top to the base (Figure 3-60). Using spray resists or depositing a larger puddle of resist before spinning may change this, but reversing the order and etching the chambers and bypass channels first may be what is best for the geometry of the pillars. Still, etching the device in this order should still work as good proof-of-concept test.

Because PDMS was difficult to remove of off the test wafer after the first round, we opted to use microscope slides for the second round of testing. The slides were taped at the edge of the device with dye applied at the slide/etched cell chamber interface. Dye does appear to be wetting over the pillars, but this could be due to the cell adhesion agents used to coat the slides (Figure 3-61). Using an FOTS treated slide, the dye does appear to wetting between and not over the pillars (Figure 3-62).

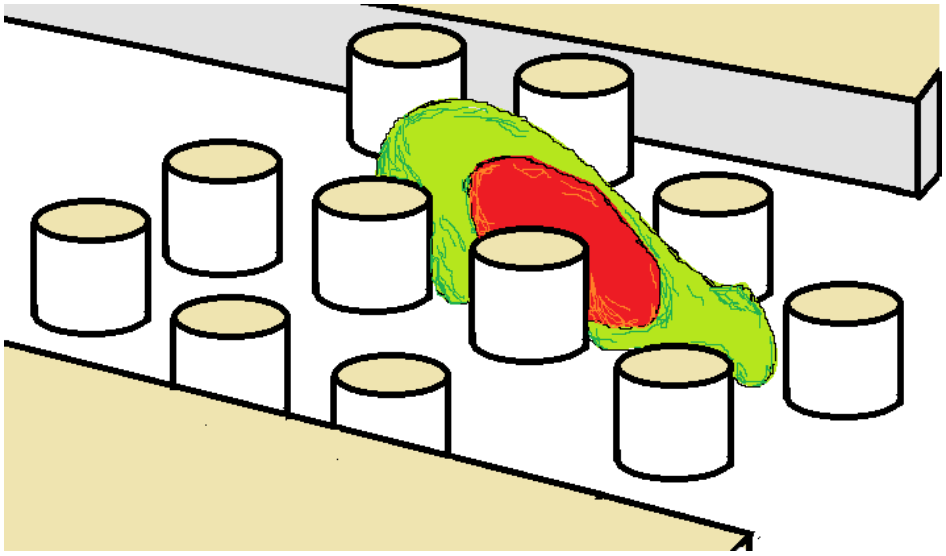


Figure 3-47: A diagram of the inverted pillar design with a cell migrating. Pillars are etched into the device substrate and capped with a PDMS mold of the remaining device components. Everything colored tan represents the surface that is in contact with the upper PDMS layer.

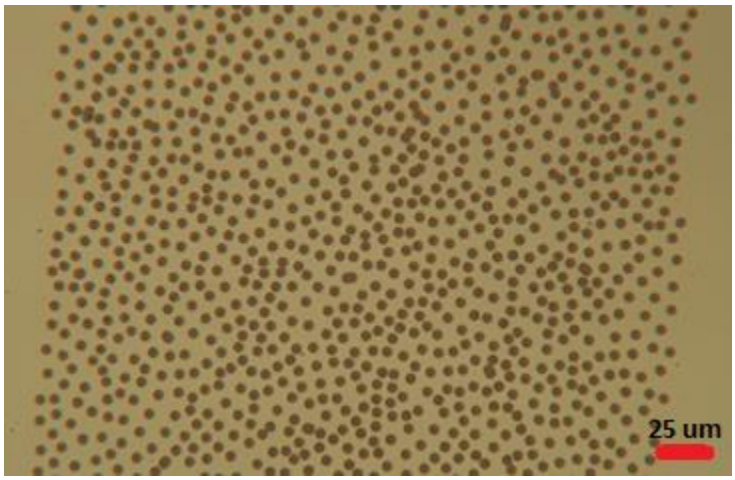


Figure 3-48: A positive-tone aluminum oxide (Al_2O_3) hard mask created using the photolithography lift-off technique before deep reactive-ion etching (20x).

Figure 3-49: A positive-tone aluminum oxide (Al_2O_3) hard mask created using the photolithography lift-off technique before deep reactive-ion etching (50x).

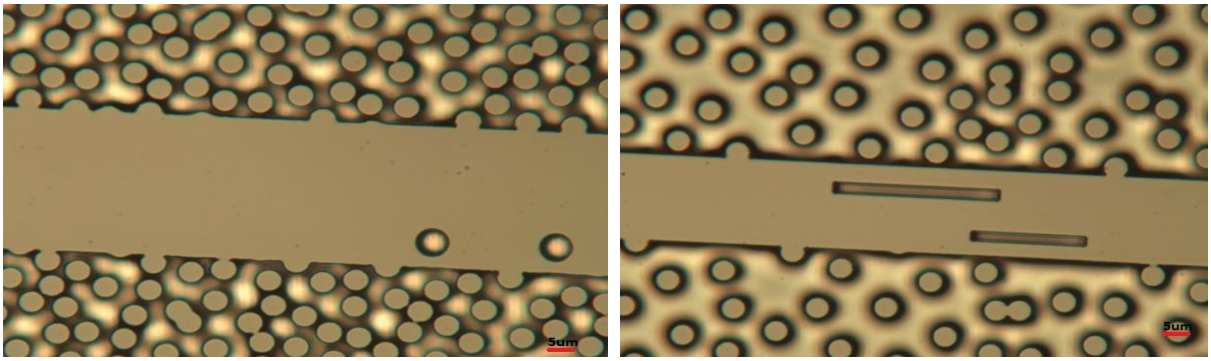


Figure 3-50: Standing pillar array deep reactive-ion etched ≈7.2 µm into a silicon wafer (50x).

Left: Consecutive "Mid-Dense" density devices. Right: Consecutive "Mid-Loose" density devices.

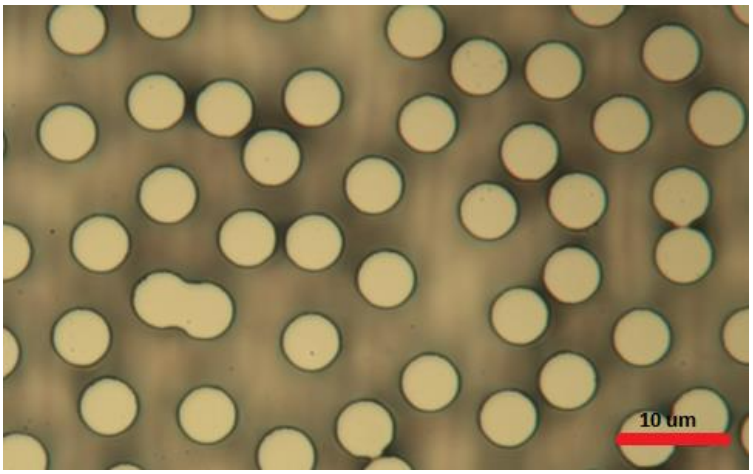


Figure 3-51: Standing silicon pillar array (100X). The space between the silicon pillars was deep reactive-ion etched ≈7.2 µm into the wafer.

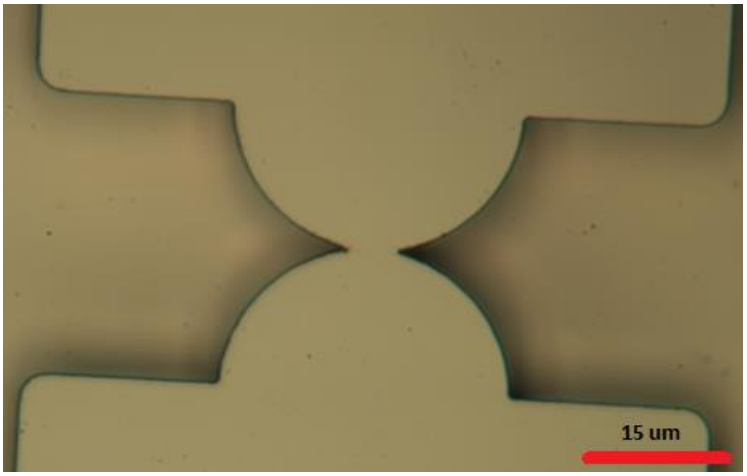


Figure 3-52: A broken 1 µm feature from the same wafer as the standing pillar array. 1.6 second exposure using an aluminum oxide etch mask for DRIE (100x).

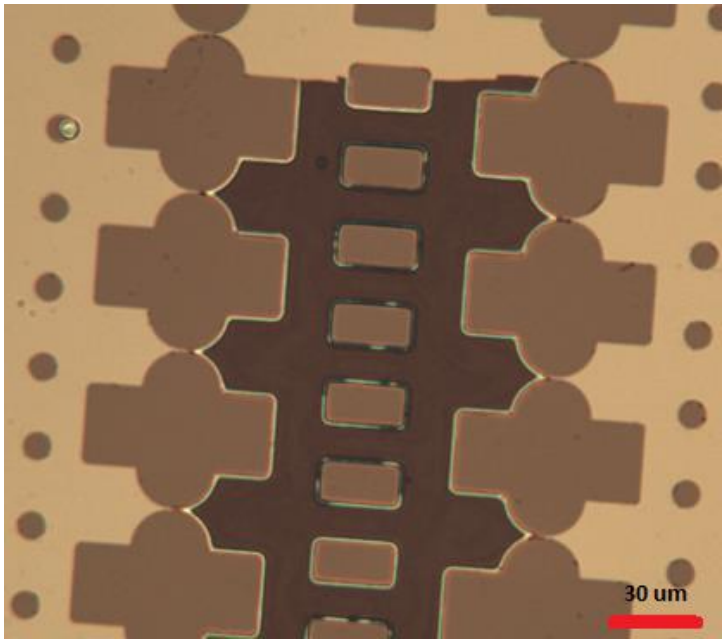


Figure 3-53 Remaining aluminum oxide etch mask that never lifted off after an acetone soak (20x)

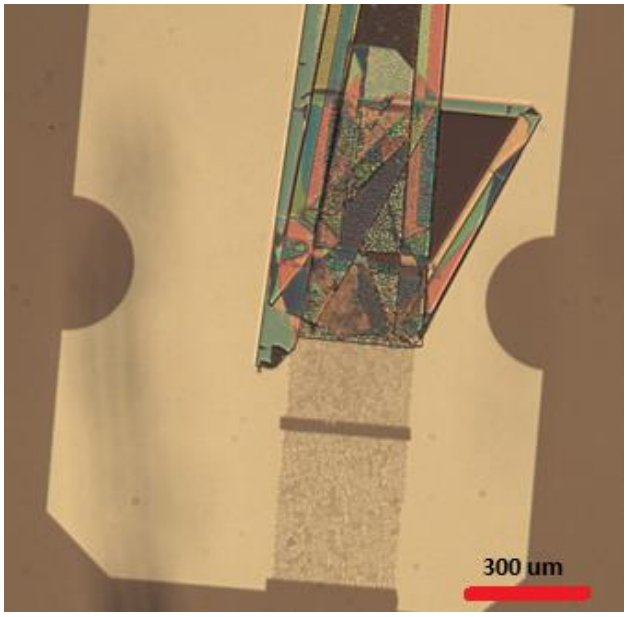


Figure 3-54: Lifted off evaporated aluminum oxide folded over itself and the desired cleared area (2.5x)

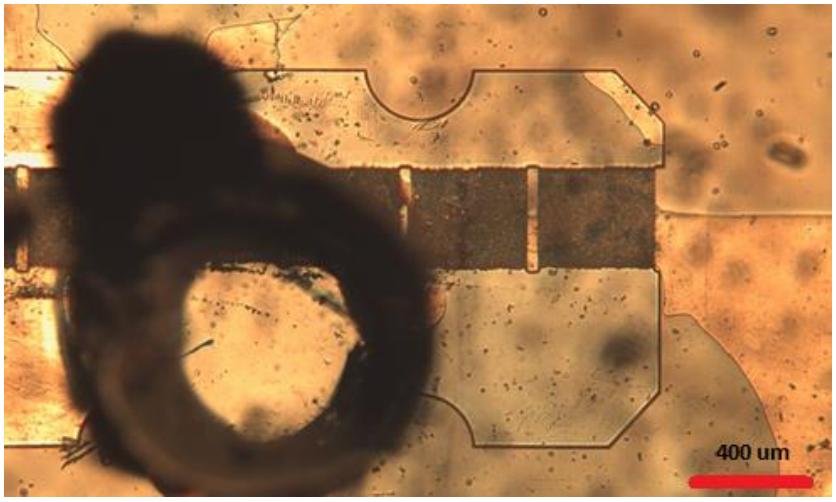


Figure 3-55: First attempt of flowing dye though the etched pillar design: Green food coloring injected with a syringe into the standing pillar array through PDMS hole (2.5x).

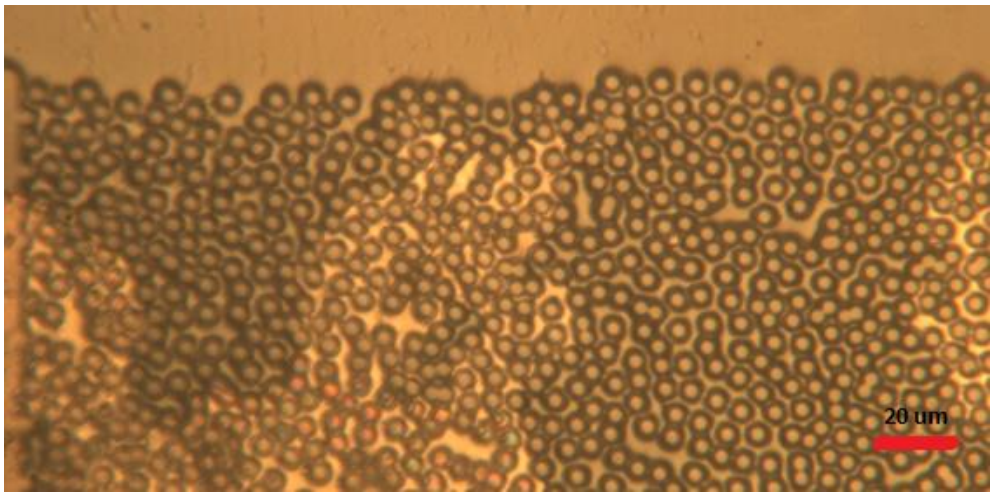


Figure 3-56: First attempt of flowing dye though the etched pillar design: Green food coloring injected into standing pillar array (20x).

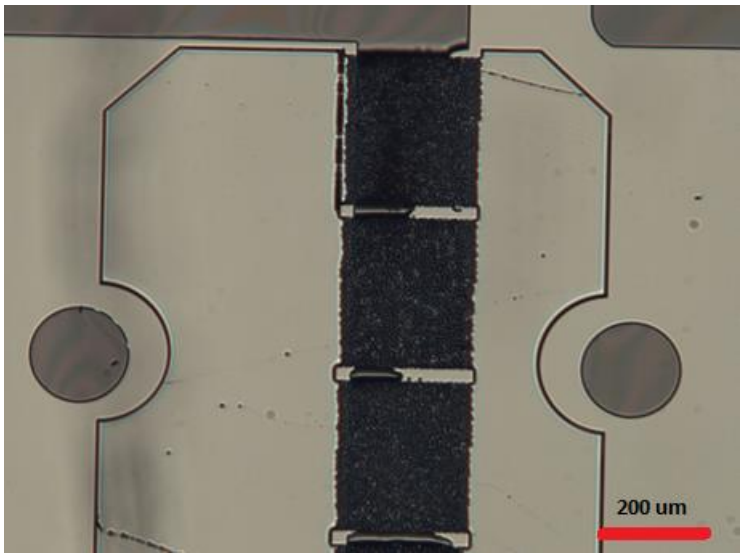


Figure 3-57: Standing pillar design with second layer of photoresist for etching the cell chambers. Shipley 1813 (grey) photoresist spun on top (2.5x).

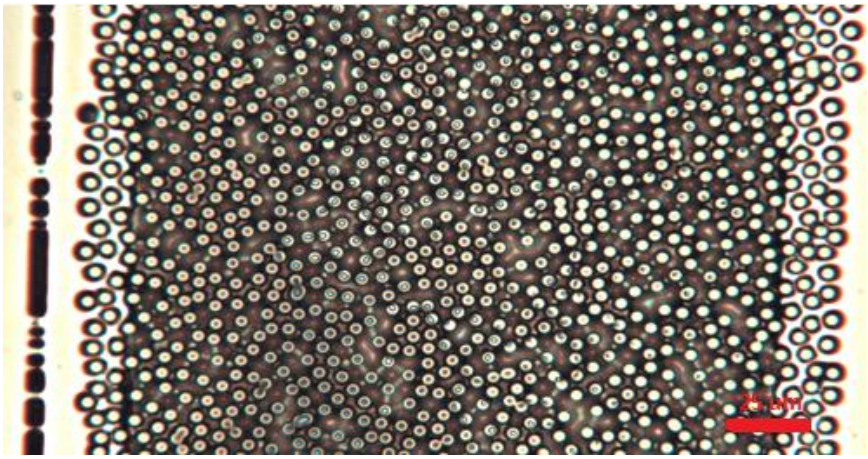


Figure 3-58: Standing pillar design with second layer of photoresist for etching the cell chambers. Shipley 1813 (grey) photoresist spun in-between the pillars and on some of the tops (20x).

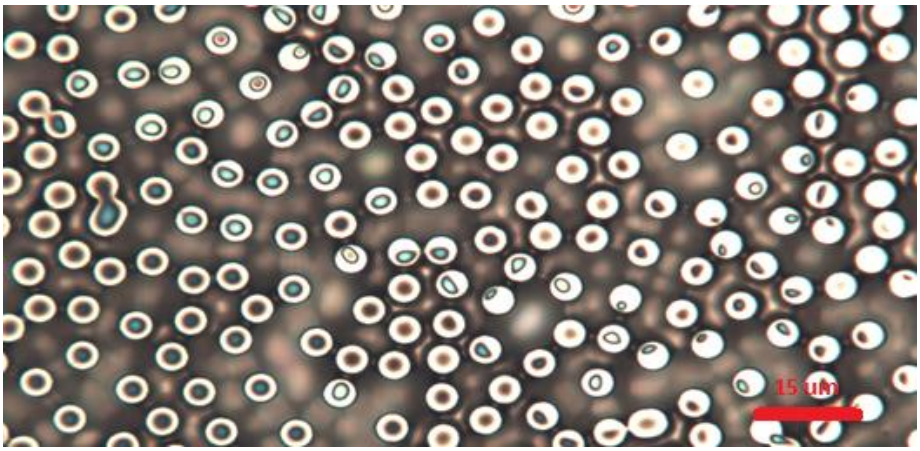


Figure 3-59: Standing pillar design with second layer of photoresist for etching the cell chambers. Shipley 1813 (grey) photoresist spun in-between the pillars and on some of the tops (50x).

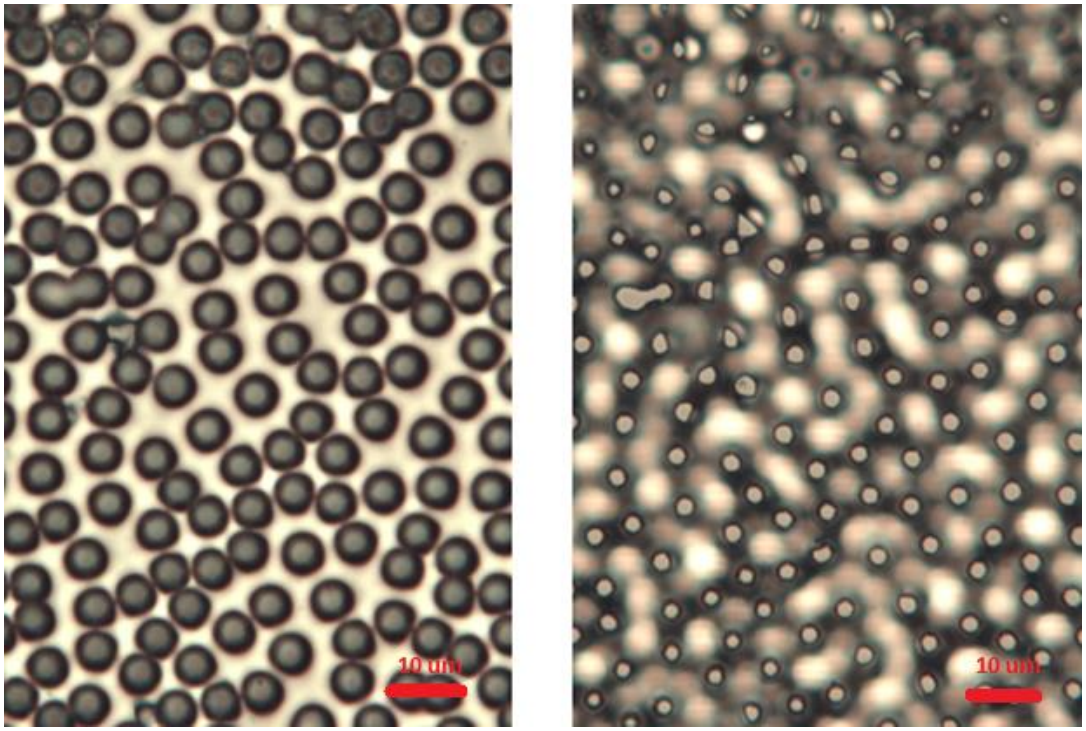


Figure 3-60: Images of narrowed silicon pillars after the cell chambers and bypass channels were DRIE. Left: the base of the pillars. Right: the top of the pillars (50X).

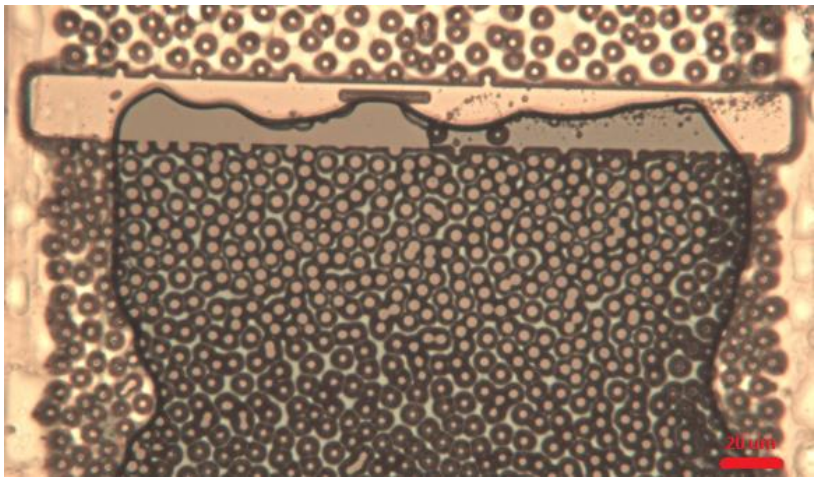


Figure 3-61: Second dye test with glass microscope slide as a capping layer (20X).

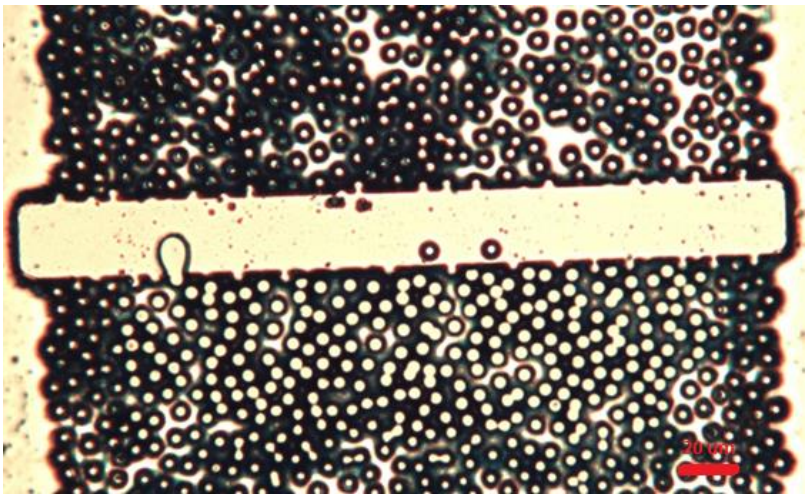


Figure 3-62: Second dye test of our etched pillars design. An FOTS coated glass microscope slide was used as a capping layer for this iteration (20X).

3.9 Creating the Ports and Bypass Channels

We also investigated a PDMS mold to replace the upper layer of SU-8. PDMS cell chambers, bypass channels and alignment marks for ports would be laid upon a larger field of fused silica pillars constrictions to complete the second generation cell migration assay. In order to fabricate a 200 µm deep silicon mold, a much more robust etch mask than photoresist would be required to withstand the lengthened DRIE. As a rule, the selectivity for silicon to photoresist for the Bosch DRIE etch process is 50:1. AZ nLof 2020 used previously was only 1.7 µm thick and would not hold up to the DRIE etch process for that length of time, but an Aluminum oxide mask with its etch selectivity of 500:1 would. The only difference is the lithographic tone would need to be reversed in order to produce an etched mold instead of an SU-8 structure. Using the same lift-off techniques as before, but with a positive photoresist would result in a negative tone Al_2O_3 hard mask.

A confocal inspection performed before the DRIE revealed particles and some pin holes in the alumina mask. Attempts to wash the particles off actually created more particles and holes in the mask (Figure 3-64). Pin holes can be caused by localized film stress, remaining chemical residues or outgassing solvents, but the more likely culprit is the presence of very thin spots of residual photoresist before evaporating the alumina. Instead of evaporating on the intended silicon, alumina is deposited on these resist spots and is lifted off when submerged in solvent. The solution for removing areas of resist is to de-scum on the wafers. A de-scum is a light oxygen plasma done before any physical vapor deposition that had been exposed to photoresist. The goal is to remove the Angstrom-thick spots of resist while preserving the integrity of the photomask.

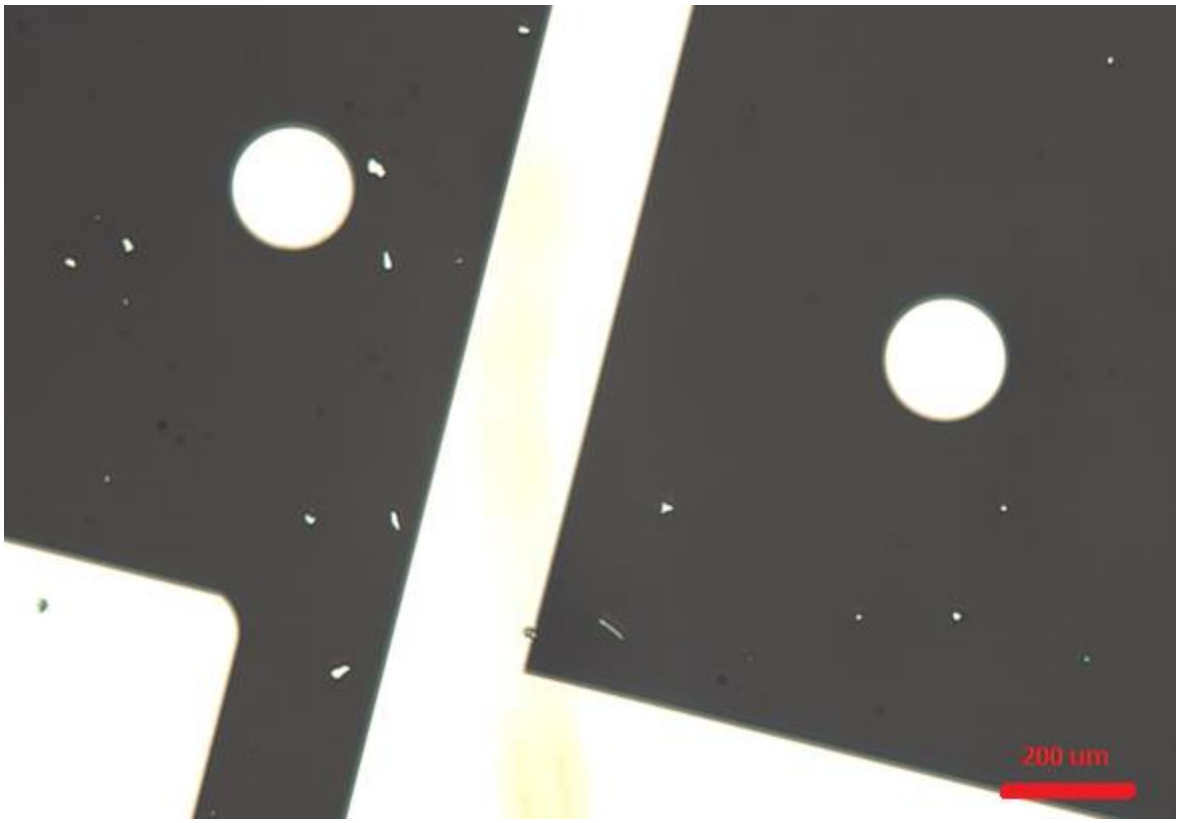


Figure 3-63: Pinholes and delamination off an evaporated aluminum oxide etch mask (20x)

3.10 Etching Fused Silica Holes

Fused silica (FS) is a common platform for fabricating microfluidics optics and other transparent components (He et al., 2010). The method for anisotropic etching of FS is unique and more involved than the previous silicon etching examples. The main difference is etching FS requires a sputtered chromium hard mask. The concept of a hard mask was discussed in the plasma etching section as a photoresist alternative for withstanding ion bombardment. For our applications, we will need a chromium mask to be resistant to prolonged plasma etching and sidewall erosion (Aydinoglu et al., 2017). When using a hard mask, there is a fine line for determining the proper etch mask thicknesses; a mask too thin will suffer from vertical mask erosion while a mask too thick will distort fine feature resolution. From previous experience, 300 nm of sputtered chromium was determine to be sufficient for etching 5 μm.

Sputtering is another physical vapor deposition technique for depositing metals. Similar to RIE, a weakly ionized plasma accelerates excited argon ions towards a deposition material target. The ions impact and dislodge atoms from the target, redepositing them upon a parallel substrate. Sputtered films are usually denser than evaporated films, which is why they are often used for hard masks (Franssila, 2010).

We turned to the negative AZ nLof 2020 photoresist again to patterned our Design # 6/single cell migration device wafer (Figure 2-26) on to the chromium. At the CNF, there are three RIE tools that are capable of etching chromium, but because two of them were down for repairs at the time, we chose to use the Trion Minilock III ICP-RIE etcher for our work. The Trion uses chlorine and oxygen gases to selectively and controllably etch chromium without burning the photoresist. After etching seven minutes, a 23 nm/minute etch rate for was determined for our design using the Tencor p-10 profilometer. An additional six more minutes completed etch. The results were promising; from an

optical inspection, all the 1 µm and 2 µm gaps measured correctly, the 5µm pillars measured ≈ 4.75 µm and the mask had ≈0.7-0.8 µm photoresist remaining. After the inspection, I stripped the residual photoresist off the wafer with a four-minute oxygen plasma etch on the Oxford 81 RIE tool. Over etched photoresist may create hard polymers that may be difficult to remove after the FS etch.

The FS etch was performed on the Oxford 100 ICP RIE tool using trifluoromethane (CHF_3) as the main etch gas (Table 3-7). Similar to the previous RIE examples, the combination of argon ion bombardment breaking the Si-O bonds and the plasma cracking the CHF_3 gas into fluorine and other carbon-fluorine free radicals (CF_x) etch the exposed FS into the volatile products of silicon tetrafluoride and other silicon-fluorine compounds (SiF_4 & SiF_x) along with tetrafluoromethane (CF_4). Too many fluorine radicals will form CF_4 resulting in isotropic etching, it is essential to keep the concentration of fluorine radicals low enough in order that some CF_x polymerization can form on the sidewalls and anisotropic etching can occur (Mohamed & Alkaisi, 2013). Oxygen is added once again to control polymerization by scavenging any free carbon atoms into volatile byproducts (CO, CO_2, & COF_2). Once etched, the final step is to remove the mask with chromium etchant and rinse repeatedly with DI water.

Fused Silica Etch with Chromium Mask	
CHF_3	**20 SCCM**
Argon	**30 SCCM**
ICP Power	**2500 Watts**
RIE Power	**60 Watts**
Pressure	**4 mTorr**
Temperature	**50 °C**

Table 3-7: Fused Silica Etch Recipe

The results were very encouraging; we actually etched ≈ 6 µm into the FS which was a little too deep, but established an etch rate of 188 nm/minute. As for horizontal geometries, the Design # 6 holes were 6 µm instead of the desired 5 µm in diameter (Figure 3-64) while the 2 µm and 10 µm gaps of the single cell migration design measure ≈ 0.8 µm and 9 µm (Figures 3-65 & 3-66). The 1 µm gaps were

etched through (Figure 3-67). The FS etch appear clean and without a brown silicon nitride wafer behind the FS for contrast, completely transparent. These photos show that we are able to fabricate a < 1 µm gap in FS. Future work will have to adjust the lithography and the etch parameters as we did for ICP-RIE silicon, but overall this etch process appears viable for creating the standing pillars design.

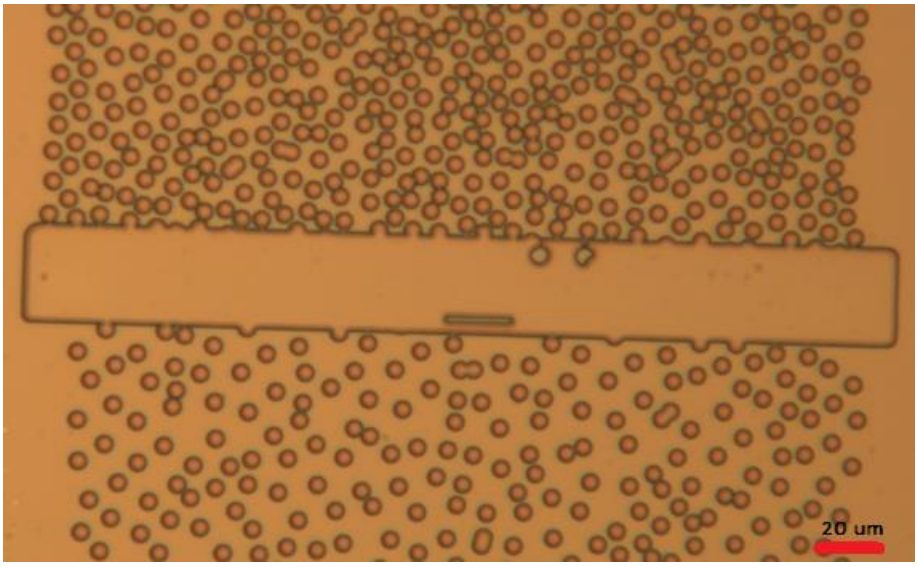


Figure 3.9.1: Loose and dense versions of Design # 6 in fused silica (with a brown silicon nitride wafer behind for contrast). Pillars are 6 µm in diameter (20x).

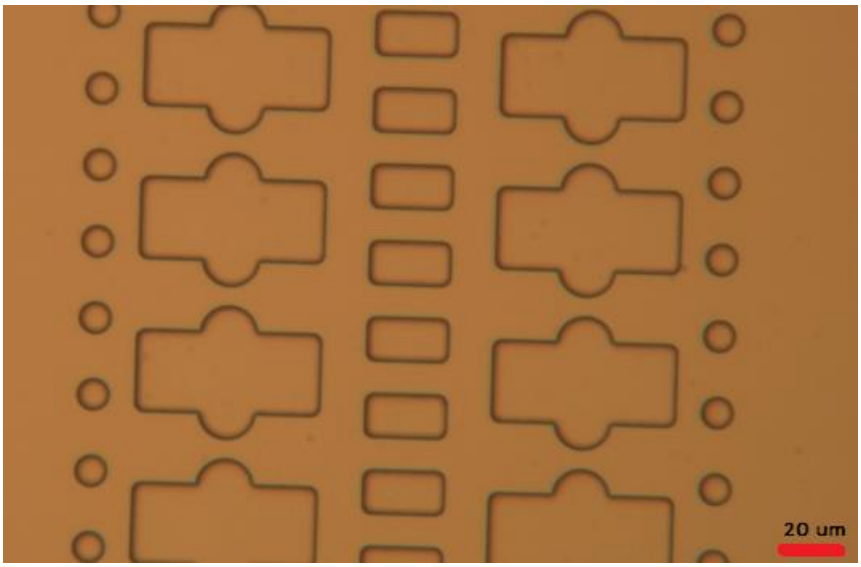


Figure 3.9.2: Isolated cell migration device in fused silica (with a brown silicon nitride wafer behind for contrast). 10 µm gaps actually measured 9 µm (20x).

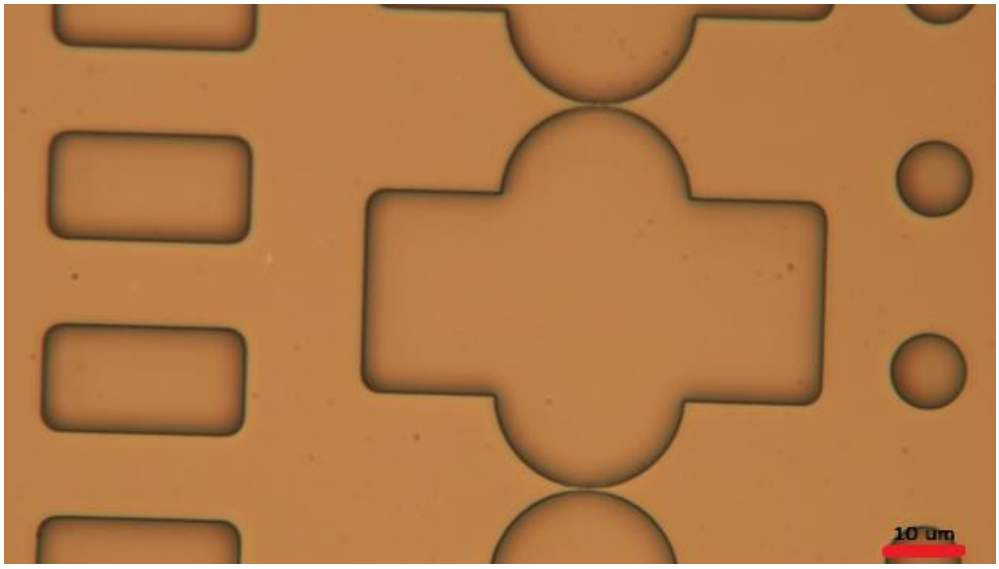


Figure 3: Isolated cell migration device in fused silica (with a brown silicon nitride wafer behind for contrast). 2 µm gaps actually measured ≈ 0.8 µm (50x).

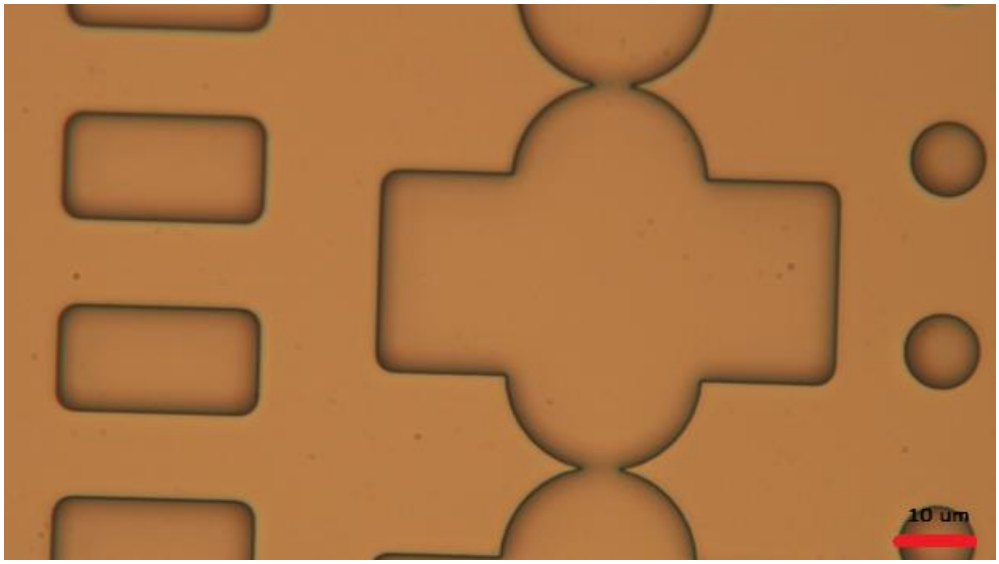


Figure 3.9.4: Isolated cell migration device in fused silica (with a brown silicon nitride wafer behind for contrast). The broken areas were intended to be 1 µm gaps (50x).

3.11 Nanoimprinting Migration Devices

We were investigating PDMS substitutes for molding our microfluidic devices for super-resolution applications that require imaging through media that matches the refractory index of water, n = 1.33 (Bashkatov & Genina, 2013). The cured PDMS we used currently has a refractive index of 1.41 (Dow Corning, 2017) which is too distant for these applications. After consideration, we eventually chose fluorinated ethylene propylene (FEP) as our super-resolution material. FEP is a highly transparent copolymer of hexafluoropropylene and tetrafluoroethylene with a refractive index of 1.334 near that of water (FEP, n.d.). The difficulty lies in how to use FEP for replicating our migration devices. Currently, FEP cannot be poured or spun, but the surface of thin sheets exposed to enough heat and pressure could produce an identical raised image off a hard master. This embossing process would require a SU-8 or silicon master of our migration device heated near the glass transition temperature or melting point (253-282^{o}C) of FEP (FEP, n.d.). Originally, we intended to use a hotplate or a heated pneumatic press for our embossing, but we did not have access to any equipment that could heat above 200^{o}C. The Nanonex 2500 nanoimprint tool's capability of heating to 300^{o}C made it the logical choice for embossing FEP. Instead of using two parallel plates, the Nanonex applies force uniformly between two flexible membranes. This air cushion press is capable of sub-micrometer resolution with minimum damage to the mold or substrate (Tan et al., 2004).

Nanoimprint lithography was driven by the semiconductor industry's need for a cost-effective, high-throughput method of pattern transfer. More specifically, the ability to mass produce nanometer-size features patterned by electron-beam lithography (Beck et al., 2002). In 1975, Gordon Moore revised his prediction he made ten years earlier that the number of components on a circuit would double every two years (Brock and Moore, 2006). The only

way that integrated circuit designers could keep up with Moore's Law and pattern smaller features closer together was to push the capabilities of lithography. Photolithography was fast, but was soon limited by diffraction and the wavelength of light. The current deep-ultraviolent light stepper using at the CNF is only capable of feature ≈ 200 nm in size (Gruhle et al., 1991). Electron-beam lithography (EBL) manipulates a focused beam of electrons to direct-write line widths of a few nanometers (Cummings et al., 2015), but this technology was not suitable for a manufacturing setting due to its high cost, environmental requirements and sluggish writing speeds (Whitesides and Love, 2001). Knowing these limitations, some researchers that were able to use of polymers or flexible substrates for their devices turned to nanoimprinting as a solution. Similar to assembly line metal stamping, an intricate three-dimensional hard master is used for thermally embossing into softer substrates. Now many devices could be generated from one EBL master.

For our first trials (Table 3-9), a 5 µm tall SU8 master from our migration devices of all the same constrictions design (Chapter 2.7) was used. The wafer was preheated overnight @ 200^{o}C and the actual gaps sizes were 2, 3 and 15 µm. All FEP sheets were washed with IPA/water and dried with nitrogen beforehand.

Steps	Imprint First Trial	Imprint Second Trial
Pre-Imprint	**200 ^{o}C/120 psi**	**180 ^{o}C/120 psi**
Imprint	**215 ^{o}C/200 psi for 2 minutes**	**190 ^{o}C/300 psi for 30 seconds**
Vent	**55 ^{o}C**	**55 ^{o}C**

Table 3-9: Parameters for the first and second nanoimprint trials

The first imprint trial was only capable of accurately replicating the 15µm gaps. The 3µm gaps measured 2µm in width (Figure 3-68) while all the 2µm gaps were broken. The depths of the imprinted sidewall measured on the P-10 Tencor profiliometer were an average of 4.34 µm. A Large bubble also formed around the outside perimeter of the

imprinted features (Figure 3-69). By increasing the pressure for the second trial, 1 µm gaps were achieved on the edges of our devices but the inner gaps were broken (Figure 3-70). All the other gaps were smaller than the master (Figure 3-71) and the bubbles that formed around the outside of the imprinted features were significantly smaller. After these initial tests, I increased the imprinting temperature to 265^{o}C (Table 3-10), which resulted in greater feature fidelity.

Steps	Imprint # 3
Pre-Imprint	220 ^{o}C/120 psi
Imprint	255-265 ^{o}C/200 psi for 30 seconds
Vent	55 ^{o}C

Table 3-9: Parameters for the third nanoimprint trial

The imprints done at 260^{o}C - 265^{o}C were accurate representations of the master wafer (Figure 3-72) and even smaller gaps were created at 255 ^{o}C. The Nanonex did have trouble maintaining the desired temperatures, which led to inconsistent results. Imprinting with the upper and lower SU-8 layers was attempted next. This wafer was from the original design #1-6 deep reactive ion etched (DRIE) test (Figure 2-23). Even at a lower temperature, most of the 250 µm SU-8 layer peeled off the devices after imprinting. The remaining 250 µm layer was removed, exposing the 5µm DRIE etched layer to a second round of imprinting. The imprinted 1µm gaps using a DRIE master appeared clean and consistent (Figures 3-73 – 3-76). This is important because creating a DRIE master is a faster and more cost effective alternative to a RIE master. Another key observation was to cut the FEP pieces smaller than the wafer. Without cutting the piece out, the edges burn and create hot spots on the FEP.

The next step was to bond another flat FEP sheet under the imprinted device layer in order to complete the confined space prototype. The first tests done with the Nanonex failed when only two FEP sheets were loaded into the diaphragm. It was apparent that some hard

backing layer was required for bonding. Initially, two ≈ 1 inch strips of silicon were laid vertically across two rows of imprinted features and bonded for 30 seconds at 275^{o}C. This bonded well, but separation was forming only around the pillars and not the whole device (Figure 3-77). In addition, it appeared that the temperature was too high after all but one of the imprinted devices melted into the base FEP layer (Figure 3-78). The temperature was lowered to 265 ^{o}C for the next test along with the inclusion of a 4" silicon wafer for backing the imprint. This worked much better, but eventually the backing wafer bonded with the FEP and shattered when removing the device (Figure 3-79). Remnant FEP residue on the backing wafer probably caused this adhesion and was not seen again after replacing with a new backing wafer. After this change, I was able to bond the layer with the desired gaps between the pillars (Figure 3-80).

We were unable to use the first batch of bonded FEP imprinted devices for multiple reasons. Once bonded, the FEP became hard and stiff, making it difficult to successfully load cells into the devices. This may be alleviated by redesigning the 5 µm layer to accommodate the cell chambers or larger areas for loading cells (which may benefit the next generation fused silicon pillar device prototype). Future designs may also include a bypass channel to control fluid flow through the chamber. We could add a syringe ports into the device while bonding which may guarantee an inward path as long as bonding doesn't happen to block or isolate the syringe tip. We may also look into chemical bonding as an alternative to thermal bonding. Loctite's Plastic Bonding System is an example of a two-part epoxy used for joining polymers such as Teflon and FEP. These systems use an activator solution to prime the surfaces for bonding. From Loctite's description (Loctite Adhesives, 2018), the bonding is fast, transparent and recommended for flexible and gas filling applications, but nothing is mentioned about liquid applications or biocompatibility.

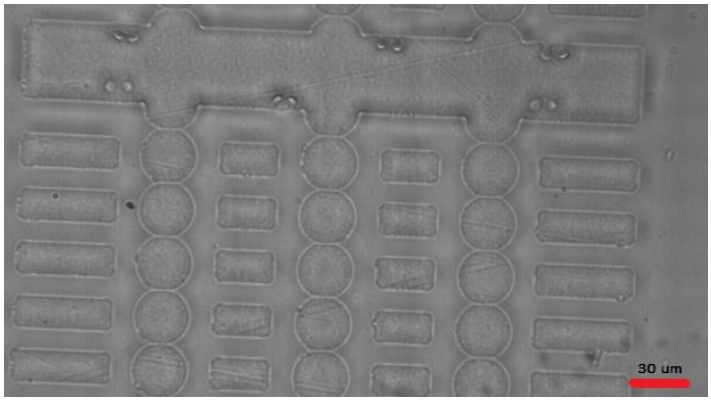


Figure 3-68: Nanoimprinted FEP from SU-8 Master from the first trial (20 x).

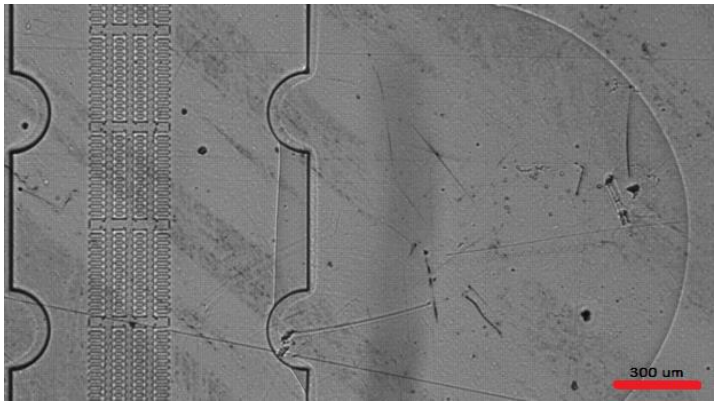


Figure 3-69: Bubble formation from nanoimprinting FEP using the parameters from Trial # 1 (2.5 x).

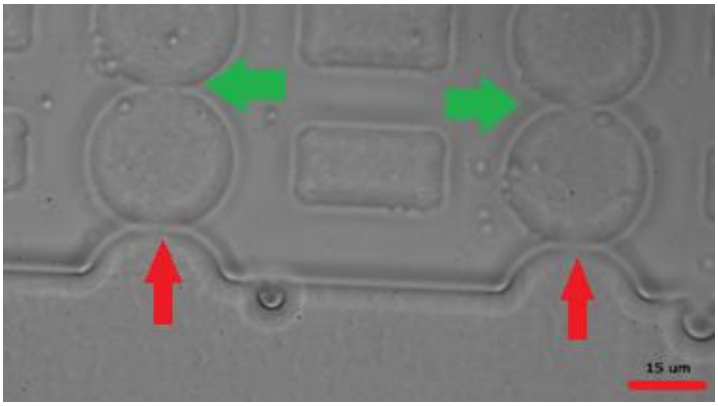


Figure 3-70: Nanoimprinted FEP from SU-8 Master from the second trial (50 x). Note that the top gaps (green arrows) are broken while the bottom two gaps (red arrows) are intact.

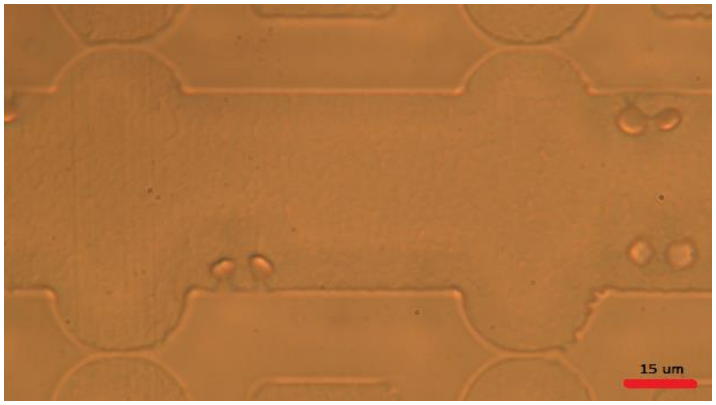


Figure 3-71: Nanoimprinted FEP from SU-8 Master from the second trial (50x). Note than 2 µm gaps are much smaller using this recipe.

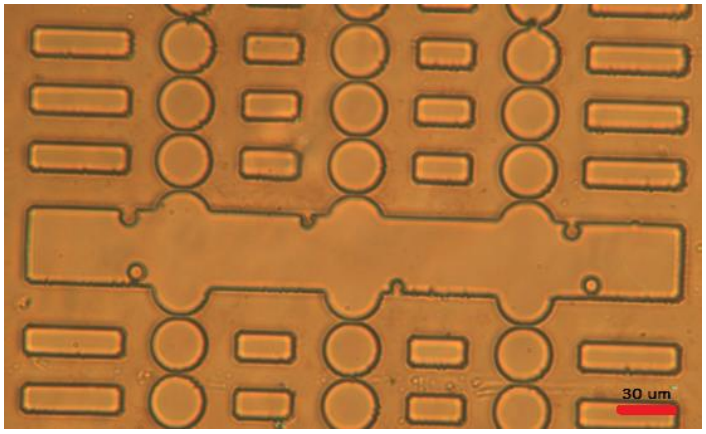


Figure 3-72: Nanoimprinted FEP from SU-8 Master from third imprint trial (20 x).

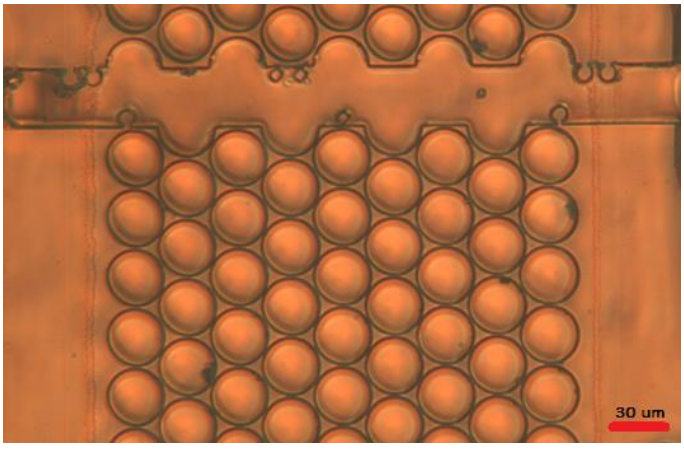


Figure 3-73: Imprinted FEP with 5 µm DRIE Master of Design # 3 @ 265^{o}C (20x).

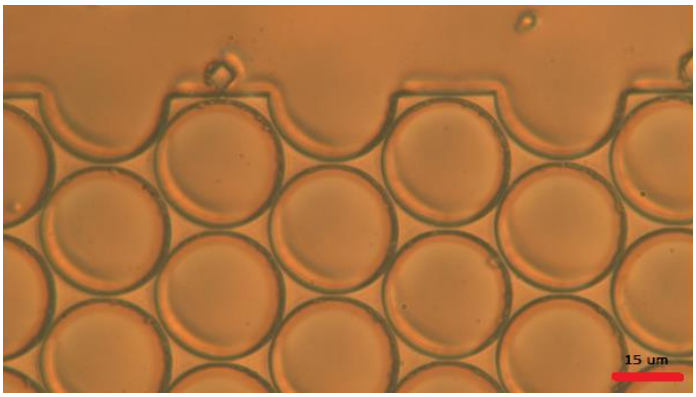


Figure 3-74: Imprinted FEP with 5 µm DRIE Master of Design #3 @ 265^{o}C (50 x).

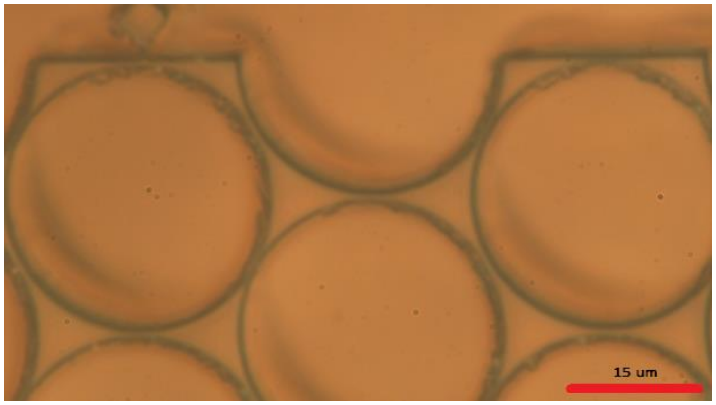


Figure 3-75: Imprinted FEP with 5 µm DRIE Master of Design #3 @ 265^{o}C (100x).

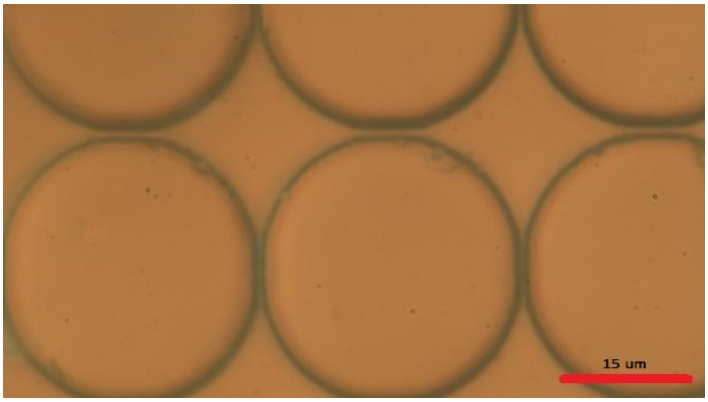


Figure 3-76: Imprinted FEP with 5 µm DRIE Master of Design # 1 @ 265^{o}C (100 x).

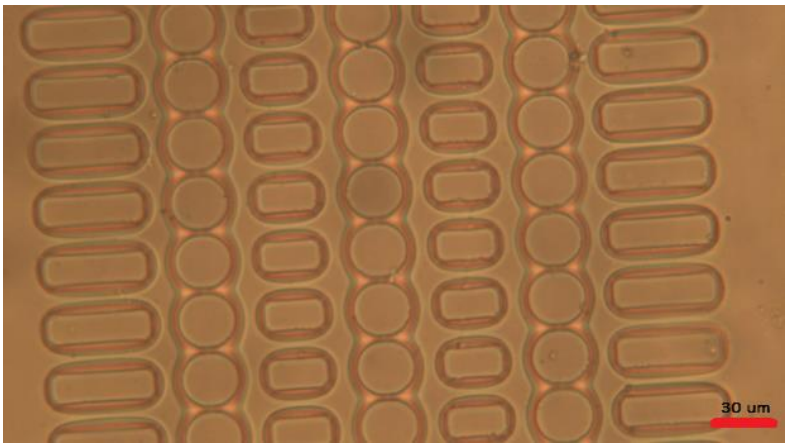


Figure 3-77: Imprinted FEP bonded to flat FEP sheet@ 275^{o}C. The device was bracketed with two cleaved silicon wafer strips (20 x).

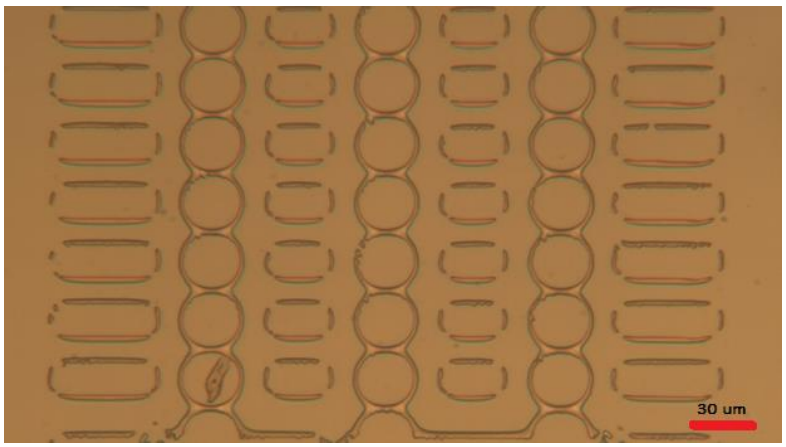


Figure 3-78: Imprinted FEP bonded to flat FEP sheet@ 275^{o}C. The imprinted layer appears melted. The device was bracketed with two cleaved silicon wafer strips (20x).

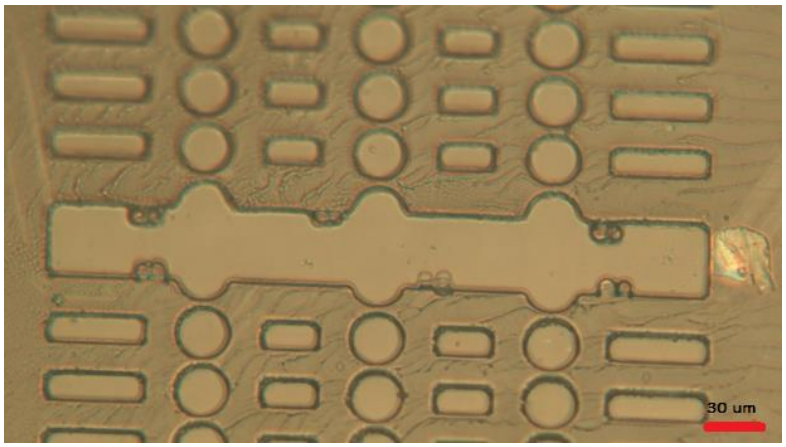


Figure 3-79: Imprinted FEP bonded to flat FEP sheet@ 265^{o}C and backed with a full silicon wafer. The FEP adhered and broke the wafer when it was removed (20x).

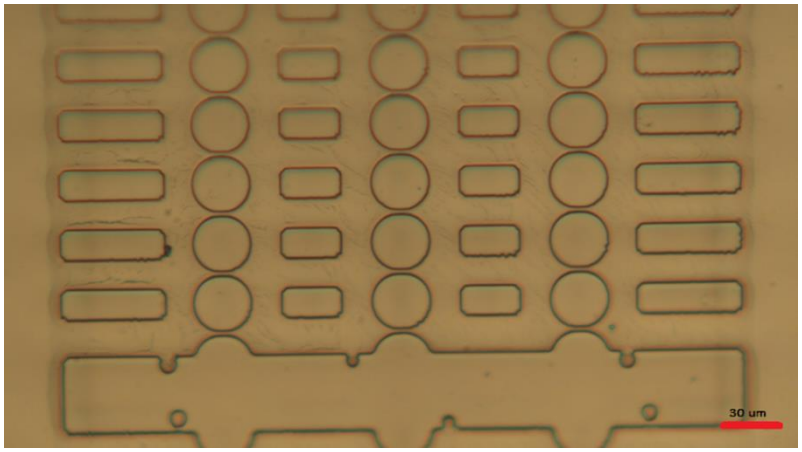


Figure 3-80: Imprinted FEP bonded to flat FEP sheet@ 265^{o}C and backed with a full silicon wafer.

3.12 Summary & Conclusions

The implementation of reactive-ion etching has drastically changed an inconsistent process into a reliable and reproducible protocol for fabricating our cell migration devices. Etching our constriction channels into the silicon substrate has given us the capability of producing complex geometries and has expanded our catalog of devices. Removing and reapplying SU-8 to what was once considered damaged master wafers I feel is the biggest breakthrough. Not only does this give our etched wafers a longer lifespan, but we now have the ability to mechanically and chemically clean out PDMS from our intricate holes and microfluidic gaps. Finally, the groundwork has been made for etching pillars into fused silicon and nanoimprinting our cell migration devices into FEP. These process have the potential to further advance the usability of the devices, enabling their broader distribution to other research groups.

APPENDIX A

TANNER L-EDIT TUTORIAL

A.1 Introduction

For this thesis work, we used Tanner L-Edit CAD software. AutoCAD is an industry staple for 3D drafting, but the software does not work well in a 2D format and is strongly discouraged at the Cornell NanoScale Facility for photomask writing. The main issues involve the conversion of a CAD drawing into a GDS (Gerber Data Stream) file that the Heidelberg mask writing software can interpret. Designed for photomask production for the microelectronic industry, Tanner L-Edit (and similar software such as Cadence and K-Layout) are better suited for large data files and repeating shapes that our design work requires.

Transferring work involved measuring the dimensions of each feature and the spaces between features from early AutoCAD files and recreating the designs on L-edit. Though time consuming, this work was beneficial for my understanding of how the device works and the significant of certain features. An example was the issue created by moving the alignment marks for the reservoirs to the 5μm layer instead of 200-250 μm layer (Figure A-1). The change made it difficult for other group members to see the shorter alignment marks through the thick PDMS polymer.

The layout work presented an opportunity to learn L-Edit's unique layout capabilities. The most important software tool for our work was the doughnut generator, which enables the user to create circles with a reduced number of vertices. This is extremely critical because each polygon vertices equals multiple data points and we are using a large number of polygons for some of our devices. Lowering the number of vertices for the repeated polygons designs will make the GDS file conversion much easier. Another L-Edit tool worth pointing out was the ability to repeat or array these polygons in the desired patterns.

Performing these array functions on AutoCAD was nearly impossible, leaving users with drawing or copying features individually.

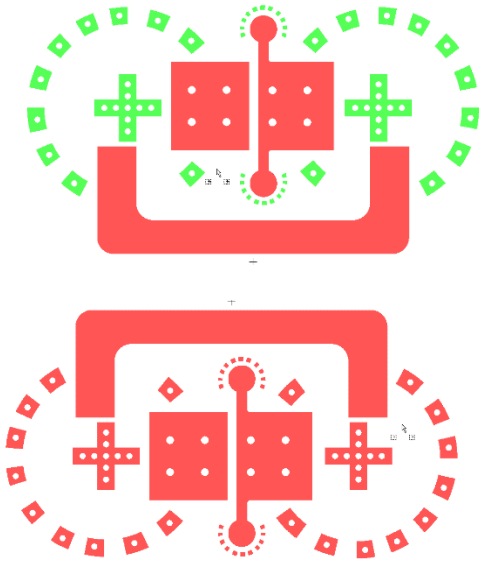


Figure A-1: Left: Earlier migration CAD revisions with the alignment marks on the 5 µm layer (green) instead of the 200-250 µm layer (red). Right: Final CAD version with alignment marks on the 200-250 µm layer.

A.2 L-Edit Tutorial

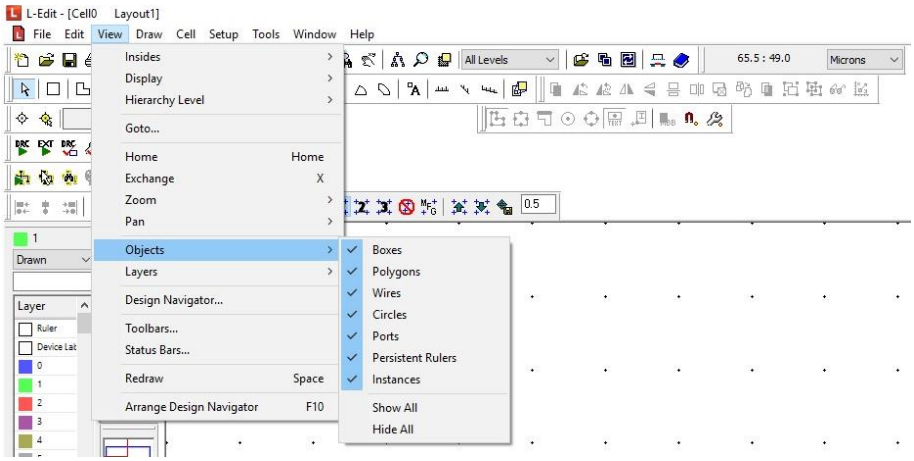
The following sections will illustrate the steps and skills required to create our cell migration devices using L-Edit version 15.0, 64-bit.

A.2.1 Creating Circles

The icon for circles in the toolbar is hidden for initial L-Edit users. To open this on your toolbar:

1) Left-click **View→Objects**

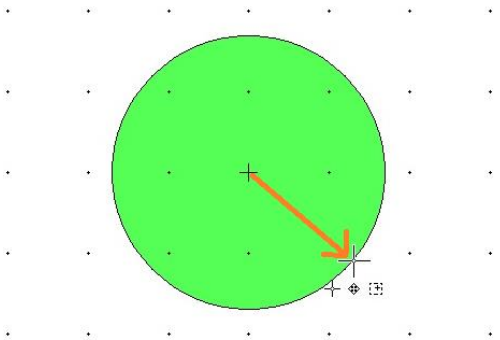
2) Click **Circles**



3) Click on the Circle icon in the tool bar.

4) Hold down the left button on your mouse and pull away from the center the desired circle radius.

5) Release the left mouse button to end.

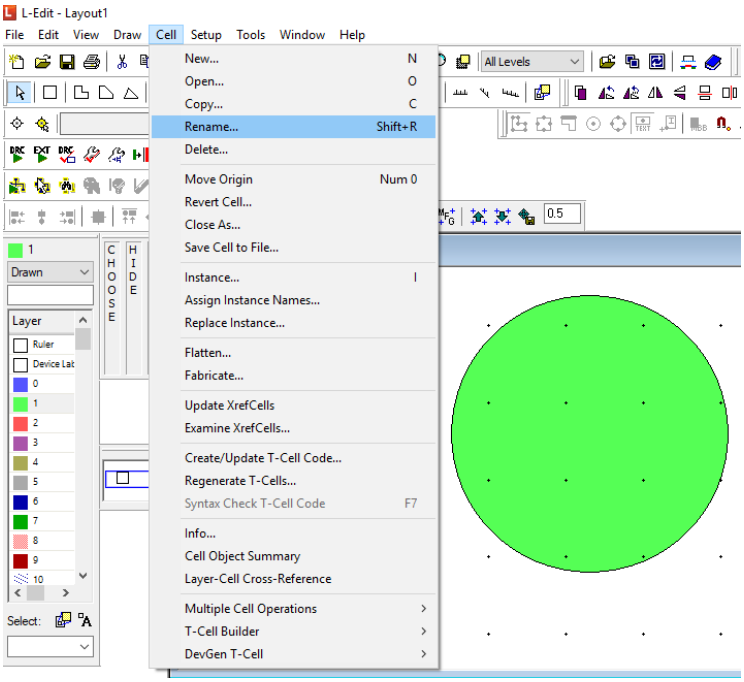


A.2.2 Creating and Instancing Cells

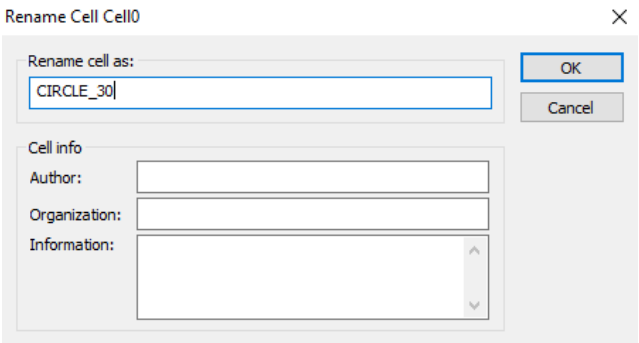
Once a shape or a group of shapes is created, it can be saved in L-Edit as a cell. Any cell can be instanced or pasted into another cell. Multiple cells can be combined to create the final design. Instanced cells can also be repeated into arrays.

1) After a shape is made, pull down the Cell menu.

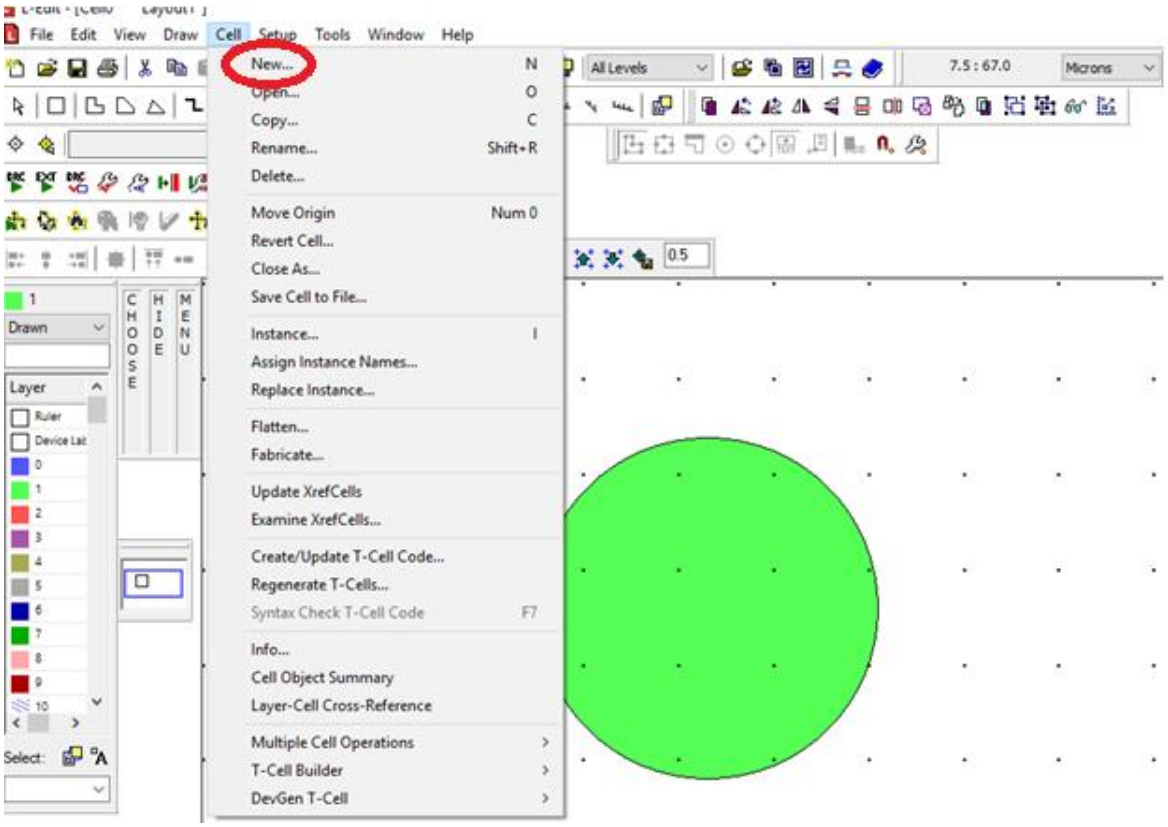
2) Highlight and left-click Rename.



3) Name the cell with all capital letters and numbers only. Use an Underscore (_) instead of a space if needed. Click OK when finished.



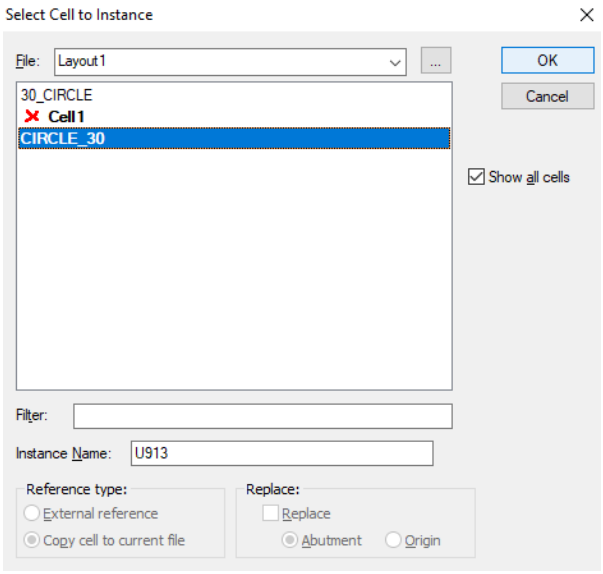
4) To make a new cell, pull down the Cell menu and click New.



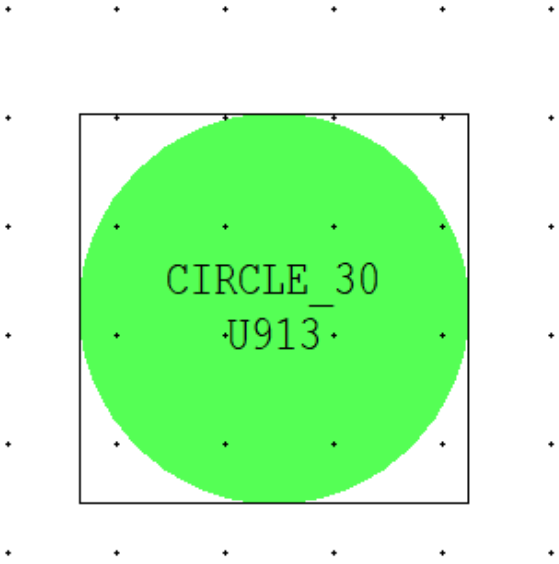
5) Name the cell as stated in step #3.

6) Press the **I** key to instance the cell.

7) Highlight the cell to be instanced and click OK.



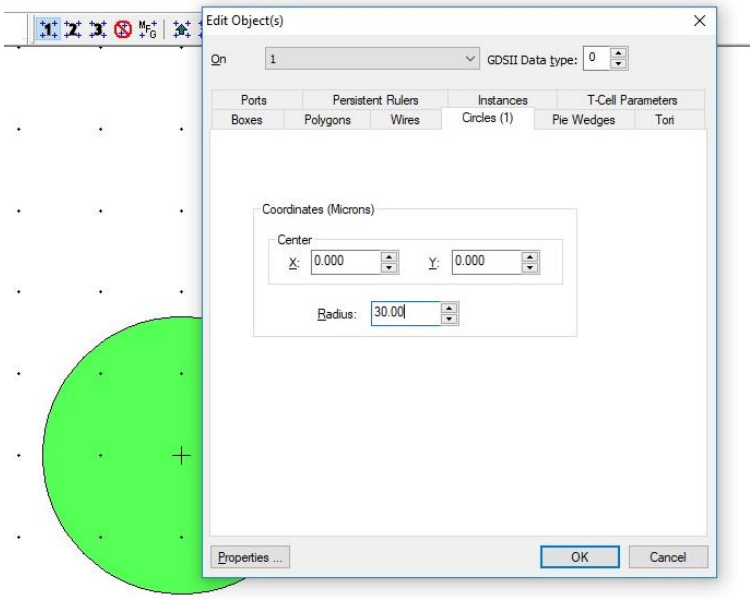
8) The instanced cell should appear in a square bracket.



A.2.3 Editing Shapes

L-Edit offers the user the ability to edit the dimensions and locations of previously designed shapes. The following section will discuss how to edit a circle.

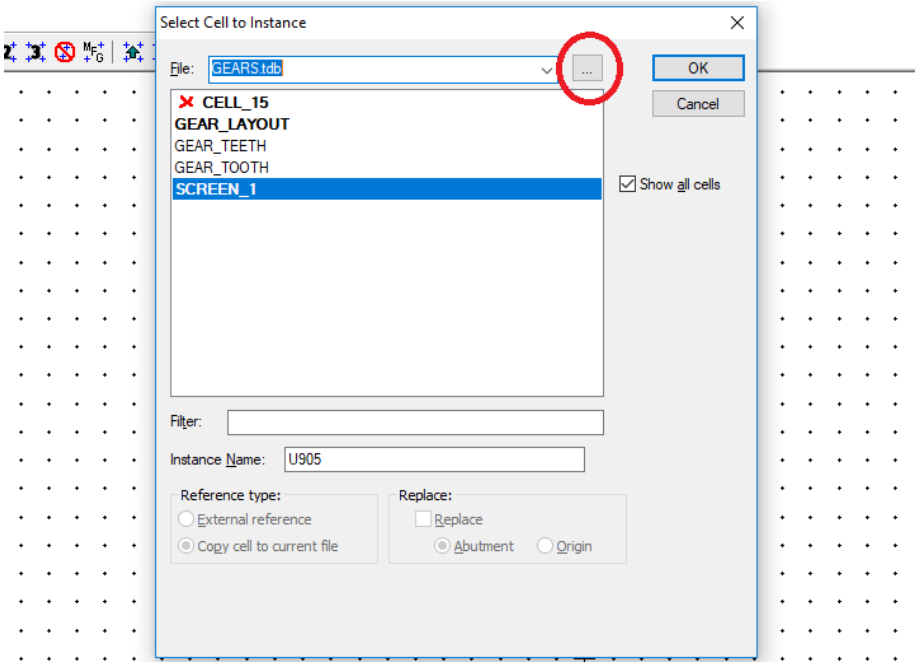
Use **CTRL-E** to edit a highlighted circle's radius and X/Y center coordinates.



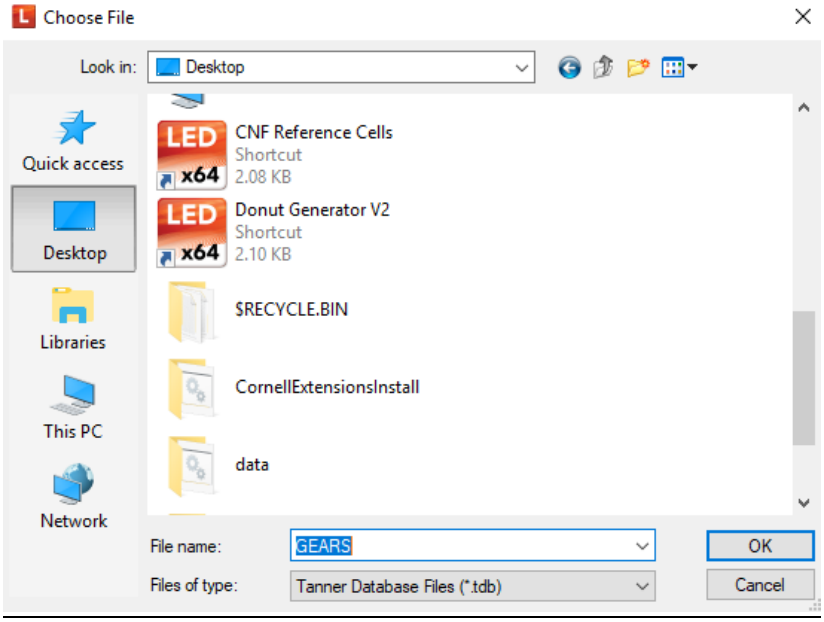
A.2.4 Donut Generator

The Cornell NanoScale Facility created the Donut Generator in order to draw circular polygons that would be able to convert much easier into a GDS format. In L-Edit, polygons can be kept under 200 sides or vertices, but the some Boolean processes and GDS conversion may fail when the number of polygons becomes too many. This was evident when the denser versions of Design # 6 (Chapter 2.5) crashed and the reason we used LayoutBEAMER for the Boolean subtraction (Refer to Design # 6 section for more information). In the case of the migration devices, the pillars were kept at thirty-two vertices, the border posts at sixteen and the smaller 5µm pillars of design # 6 at eight. Because the donut generator is not a standard program for L-Edit, the following is a tutorial on how to use and install the file:

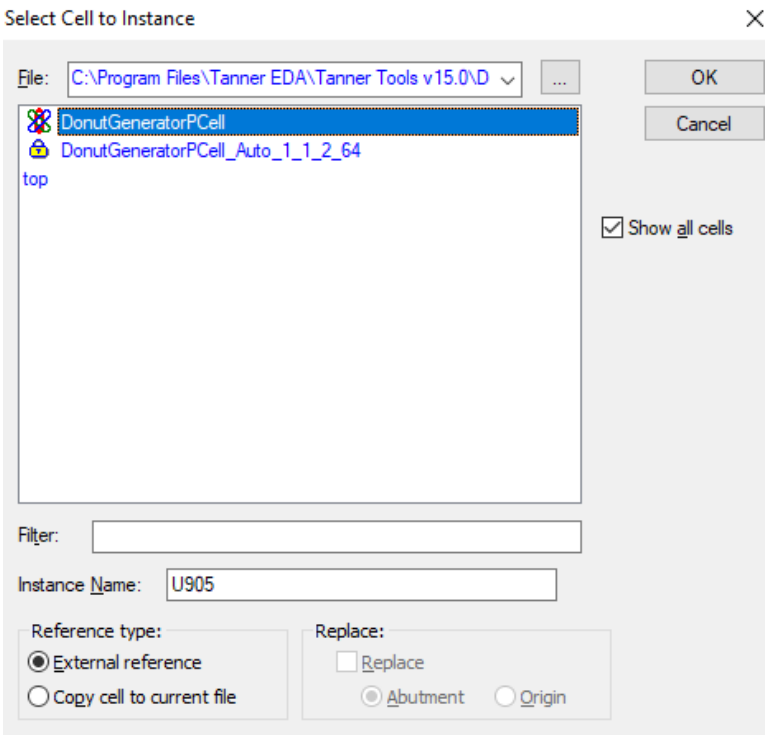
1) Click **I** for Instance.
2) Click on Browser icon circled in red.



3) Click Desktop icon on the left and open the DONUT GENERATOR V2 shortcut

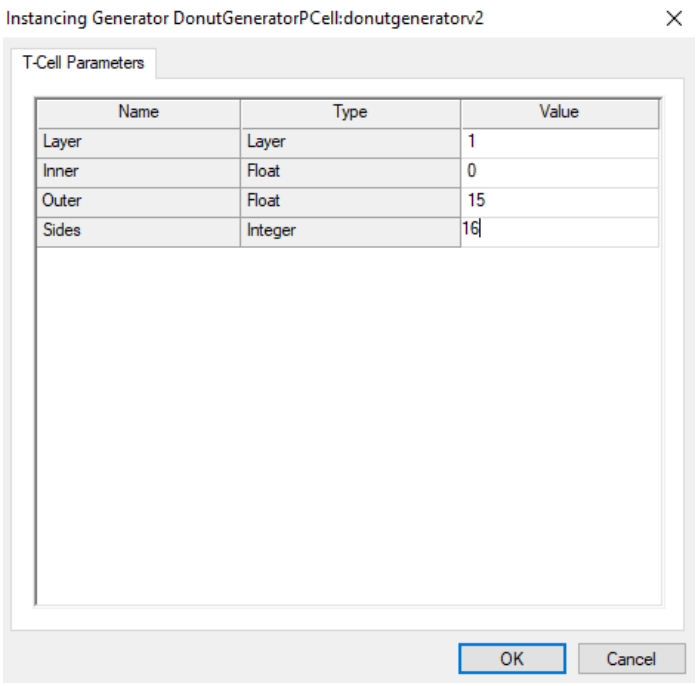


4) Select the **DonutGeneratorPCell** to instance and click OK.

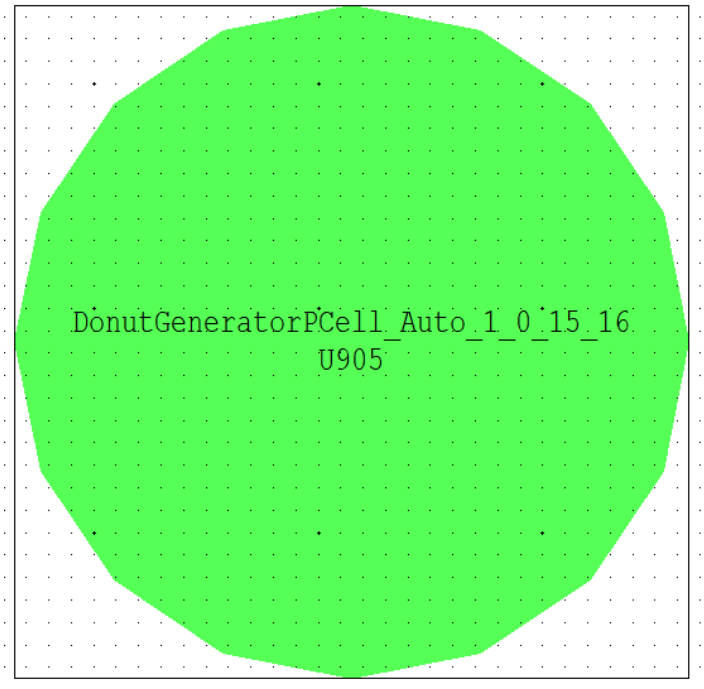


5) The software will ask you the parameters of the circular polygon. Create the polygon on layer one. The inner and outer refers to the inner and outer radius of the polygon.

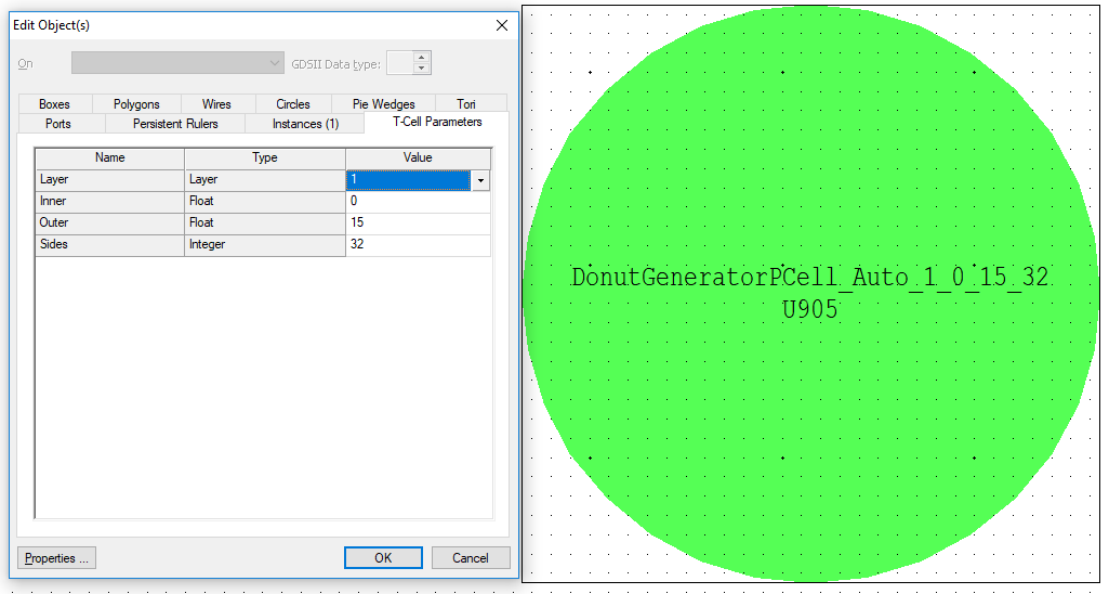
The inner should remain zero for a filled circle. The sides is the number of polygon vertices.



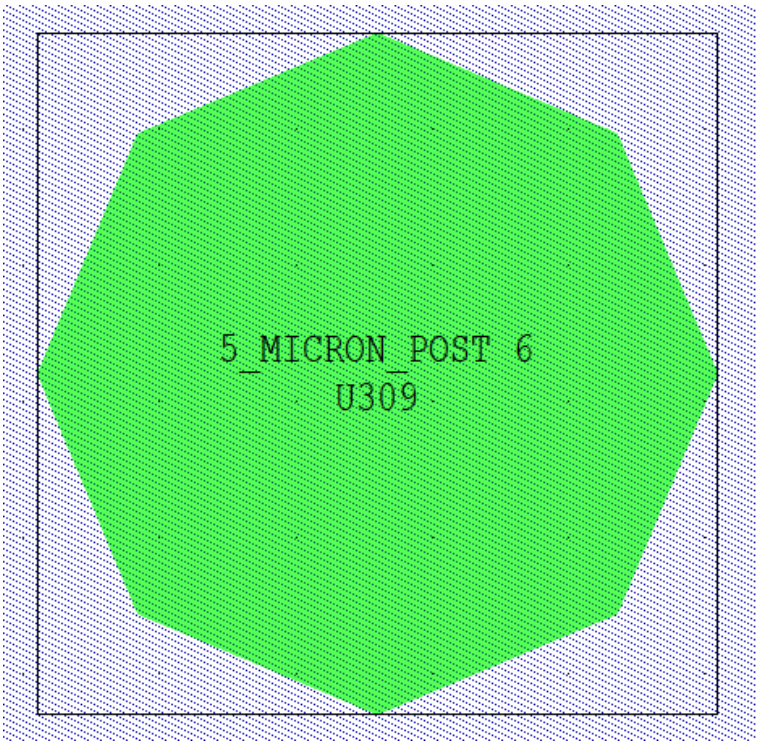
6) Here is an example of a 30 µm, sixteen sided polygon.



7) Press **Ctrl-E** to edit the polygons. Here is an example of a 30 µm, thirty-two sided polygon. Note the rounder form by doubling the vertices.



8) Here is an example of a 5 µm, eight-sided pillar used for Design # 6.



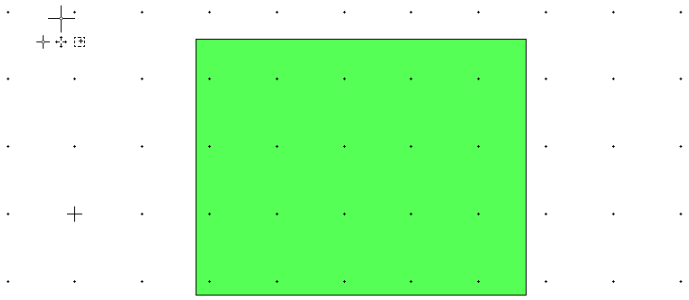
9) Open up a new cell and instance the new polygon.

A.2.5 Creating Chamfered Rectangles

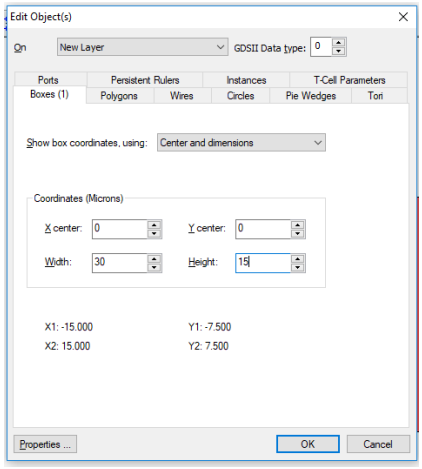
All of our devices use rectangles with rounded or chamfered corners. The following is a tutorial on how to create these shapes.

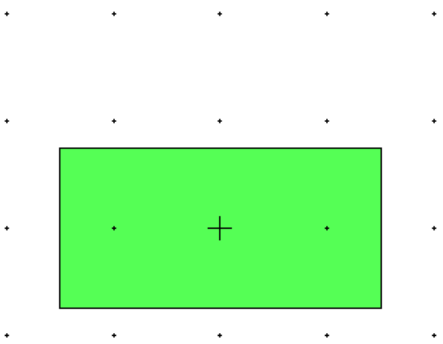
1) Enable the square icon on the tool bar menu.

2) Click and hold the scroll wheel while moving the mouse to create a rectangle.

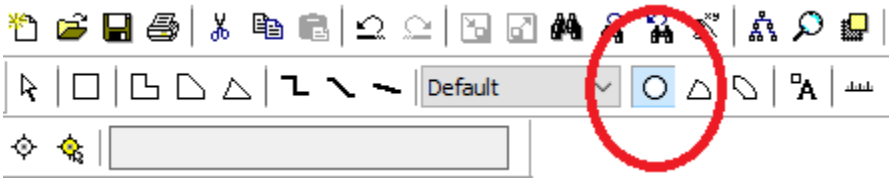


3) CTRL-E to open edit object screen. Center the rectangle by changing both X-Center and Y-Center to zero. Change the width to 30 and the height to 15.



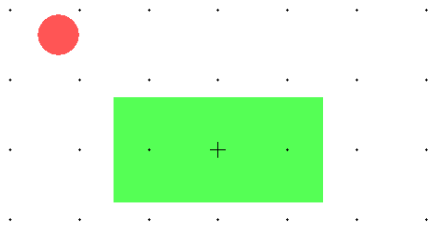


4) Enable the circle icon on the tool bar menu.



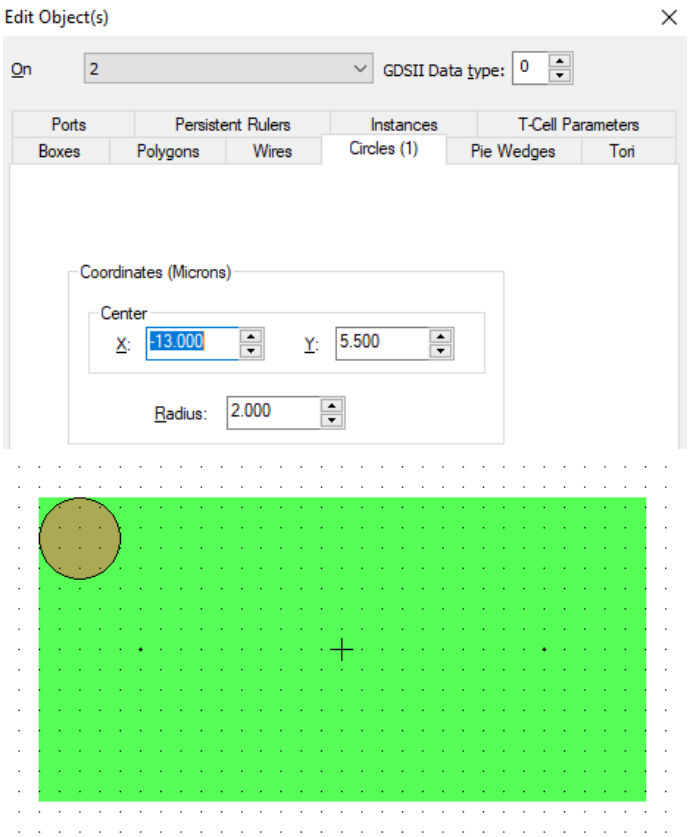
5) Select Layer 2.

6) Left click and pull the mouse to expand circle.



7) Right click to highlight the circle and press CTRL-E to open the edit object window.

8) Change the rectangle coordinates to (-13, 5.5) and the radius to 2µm.

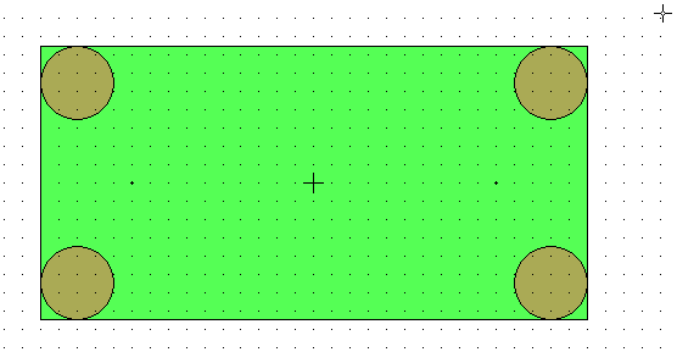


9) Highlight and press CTRL-C to copy the circle.

10) Press CTRL-V to paste the copied circle.

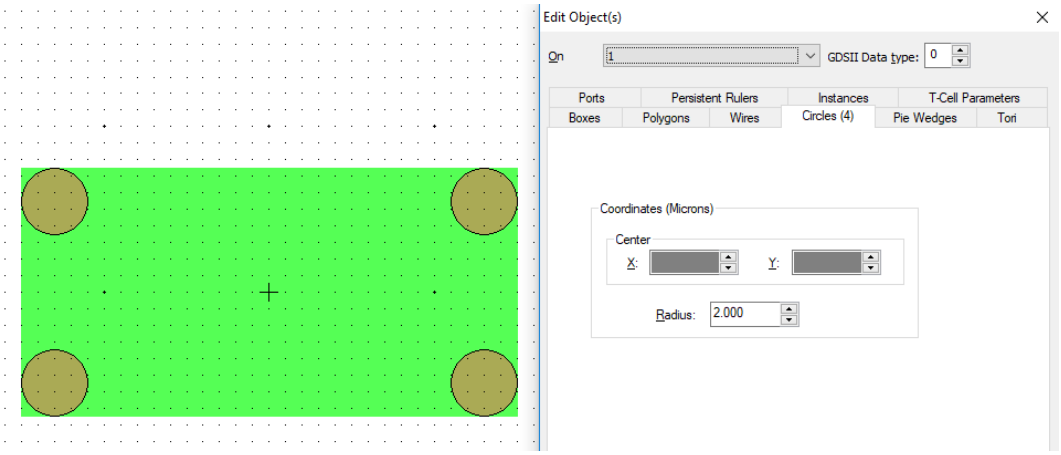
11) Change the circle coordinates to (13, 5.5) and the radius to 2µm.

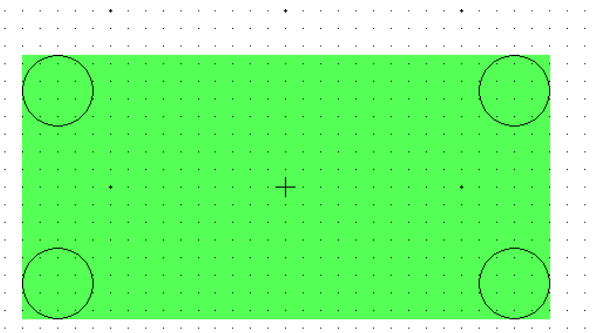
12) Repeat steps 9-10 two more times with circles in the coordinates of (-13, -5.5) and (13, -5.5).



13) Hold shift and right-click all four circles.

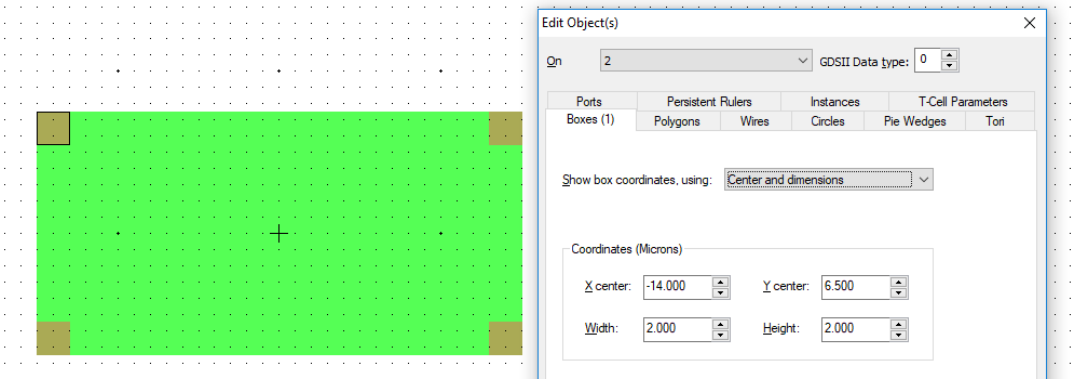
14) CTRL-E and at the top-right of On, change the circles from layer 2 to layer 1.



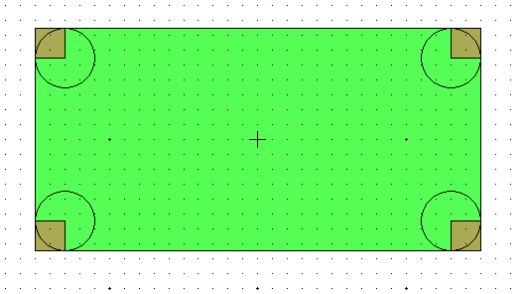


15) Using Layer 2, click the square icon on the tool bar and create a square. Press CTRL-E and change the X-Center to -14.0µm and the Y-Center to 6.5 µm. Change both the width and height to 2 µm.

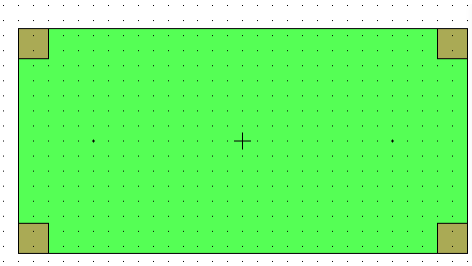
16) Highlight the new square and repeat steps 9-10 three times to create three more squares. Their coordinates should be (14, 6.5), (14, -6.5) and (-14, -6.5). The square can also be dragged to these locations by holding the scroll wheel and moving the mouse.



17) This is the design so far:

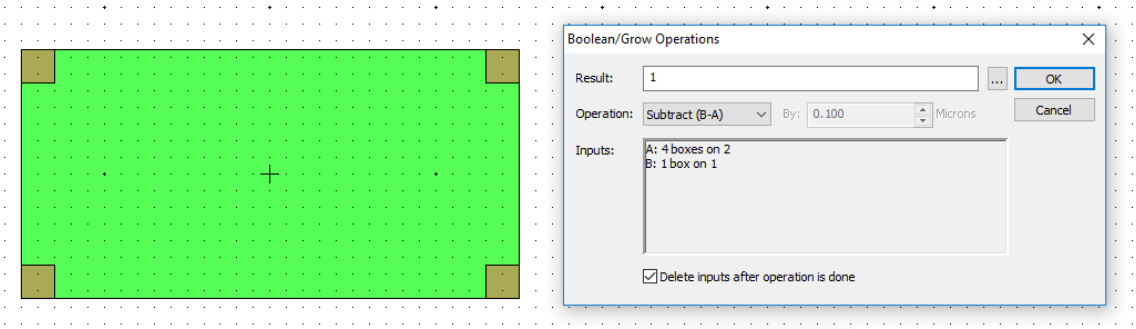


18) Highlight only the large rectangle and the four squares

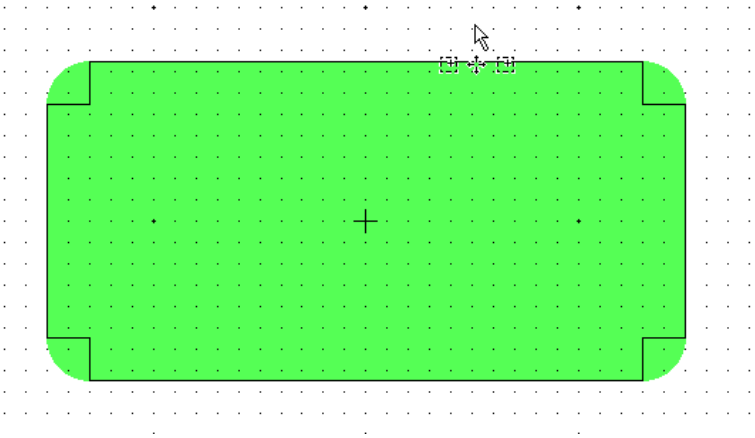


19) Click on the Boolean/Grow Operation icon on the tool bar

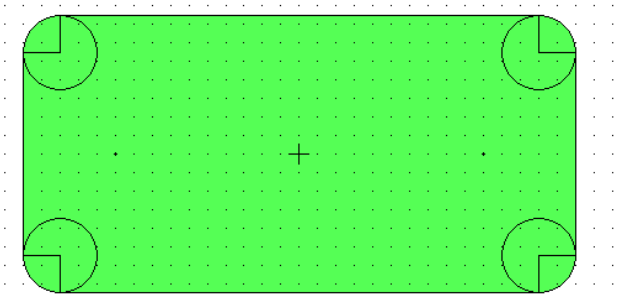
20) Perform a Boolean (B-A) Subtraction. Remember to check the box for deleting inputs.



21) The result should be as seen below. If not, try subtracting (A-B).

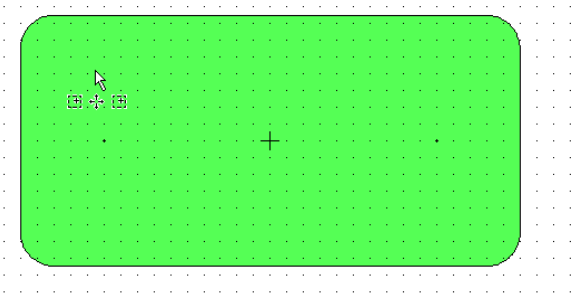


22) Highlight all the remaining shapes.



23) Click on the Merge icon on the tool bar.

24) The final shape should appear as below:



25) Save as a new cell to instance later into the device. Remember to use all capital letters and underscores instead of space.

A.3 L-Edit Example: 2 µm Migration Device

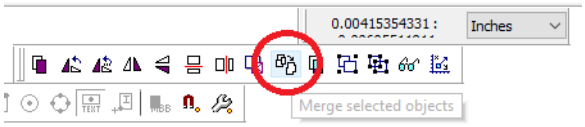
This is a breakdown of how we developed one of our standard or migration devices of all the same constriction sizes (Chapter 2.7) using L-edit software. These steps will give the reader a good template for how to modify and create future devices.

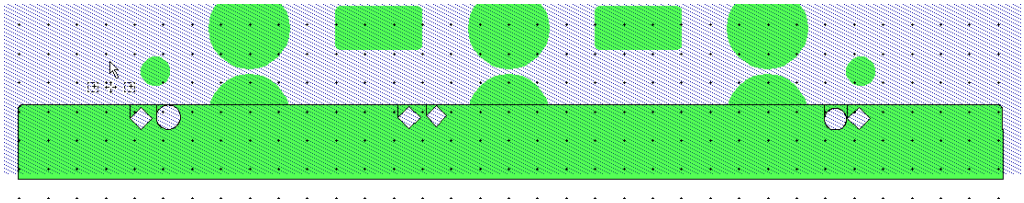
A.3.1 Boarder Walls

Walls are needed to prevent the cells from leaving the designated restriction and the time-lapse imaging area. It is an important reminder that the green areas (Layer 1) will be subtracted from the blue field (Layer # 10) when the design work is finished. Layer # 10 will be switched to Layer # 1 in order to create "holes" for PDMS pillars.

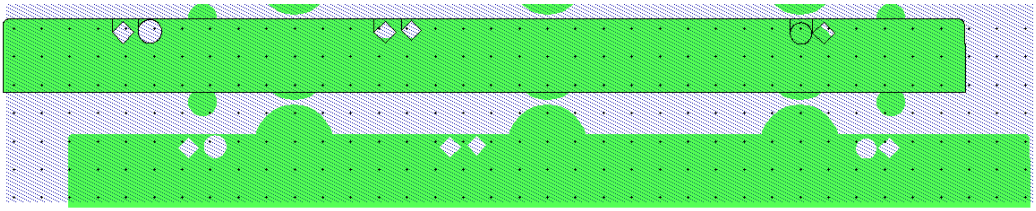
1) Click on the **Square** icon.
2) Right-click and drag the mouse to the right to create a rough rectangle.
3) Hold **CTRL-E** and under Center and Dimensions change the height to ≈26 µm and the width to ≈342 µm.
4) Add rounded chamfers if desired (see the section on creating the rectangular blocks for how to create chamfers).
5) A marking system should be used to indicate the type of device. Two shapes were Boolean subtracted from the wall to indicate that the device has 2 µm constrictions. Refer to the Boolean Subtraction section for help.
6) Merging these shapes together may help lower the polygon count for an easier final Boolean subtraction and latter mask writter conversion. This can be done by

highlighting the intended features and using the merge icon.

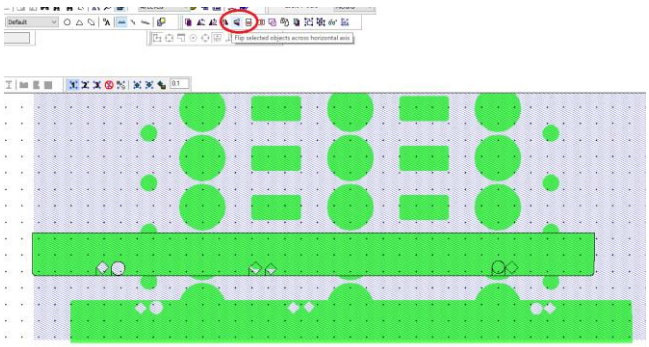




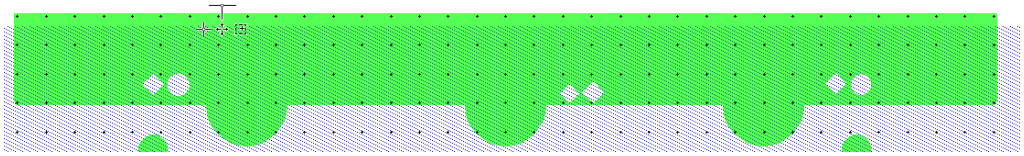
7) To create the top boarder, right-click the wall (the edges will become outline in black) and Press **CTRL-V**. This will duplicate the wall.



8) While highlighted, click on the **Horizontal-Axis Mirror** Icon in the toolbar to invert the wall.



9) Drag the inverted boarder wall to represent the top of the device. The innerfaces of both walls should be ≈ 410 µm apart.



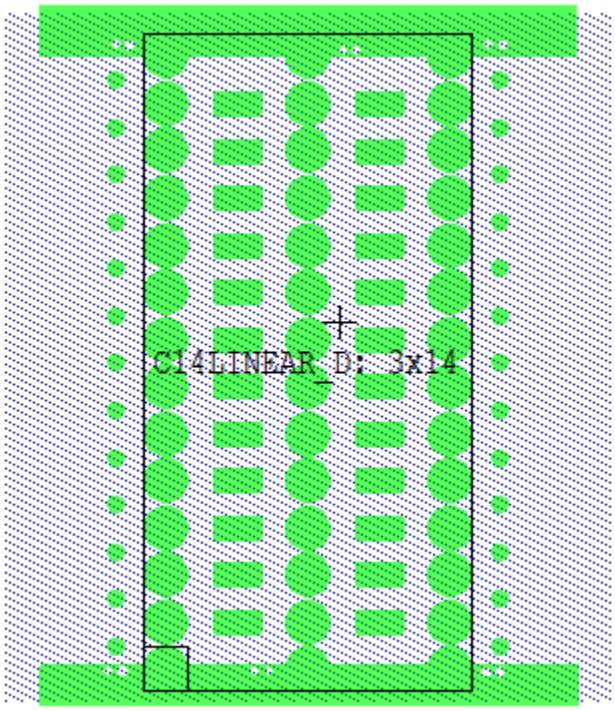
A.3.2 Constrictions

Laying out closely packed columns of circles across the constriction channel creates the constrictions.

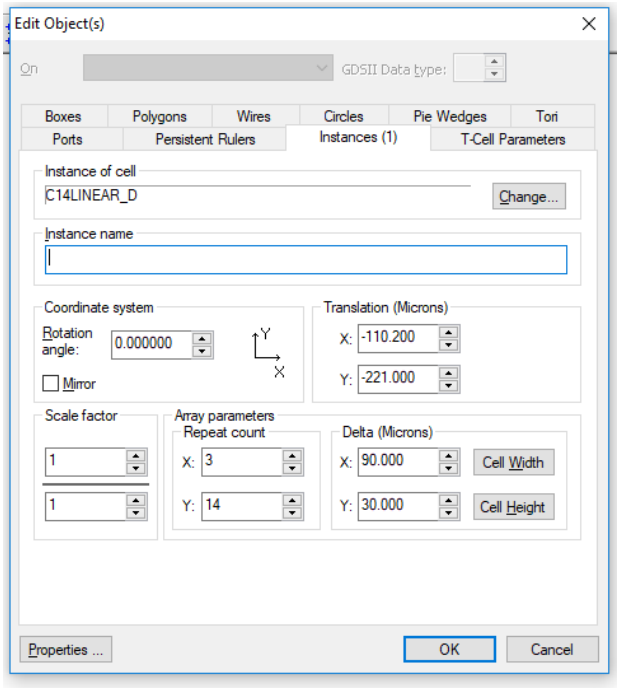
1) Start by performing an Instance (**CTRL-I**) on the shape of the first circle (outlined in black square in the lower left-hand corner). If you are concerned with the amount of polygons, use the **Donut Generator** software to draw the first circle (see Donut Generator section for help). The proper pillar sizes for certain constriction dimensions are as followed:

Constriction Size (µm)	Pillar Radius (µm)
1	14.5
2	14.0
3	13.5

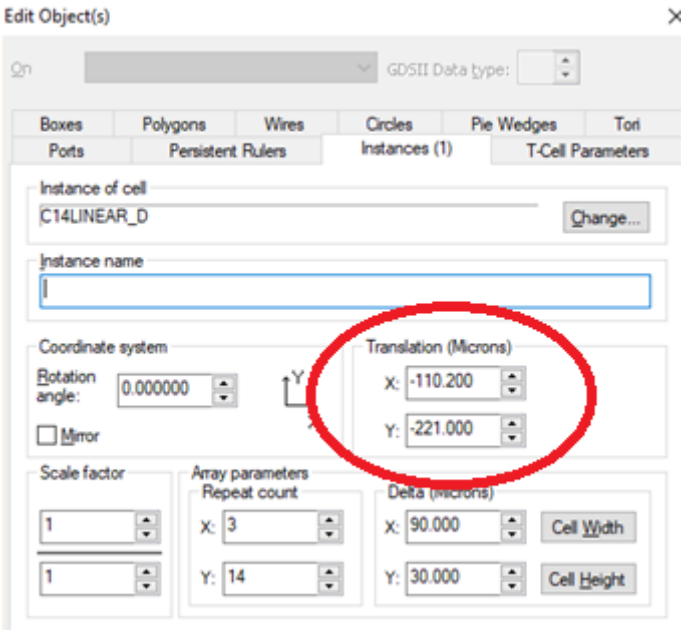
For this example, we instanced a 14 µm radius circle.



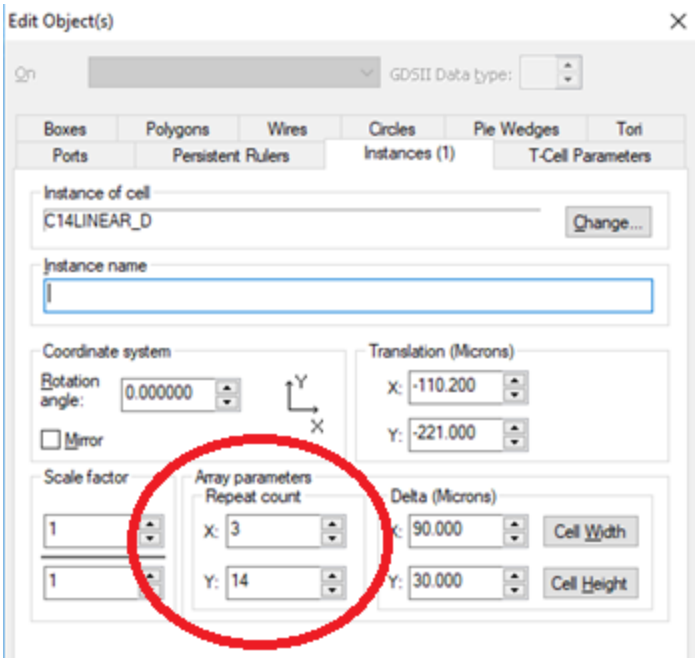
2) Hold **CTRL-E** to open the Edit Objects window.

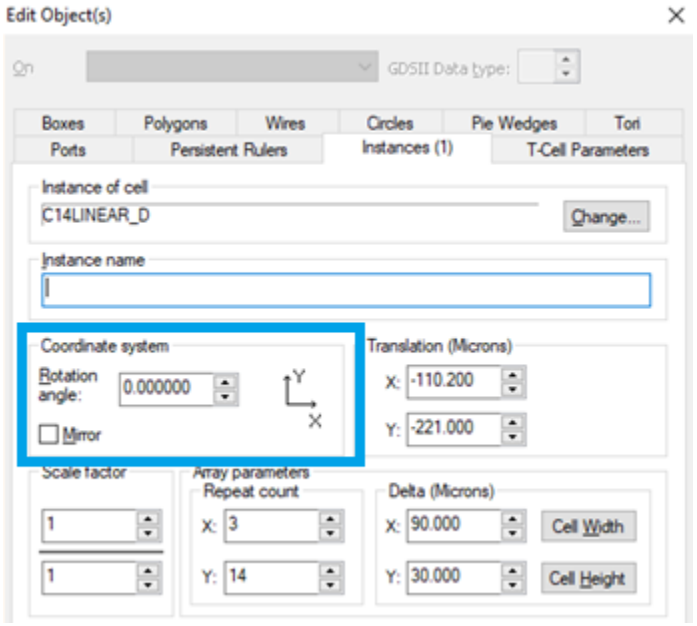


3) Change the Translation (Red Circle): The translation is the location of the original instanced circle. A good strategy is to keep the center of your design around (0, 0) coordinates. For this example, The X: -110.00 and the Y:-221.00.

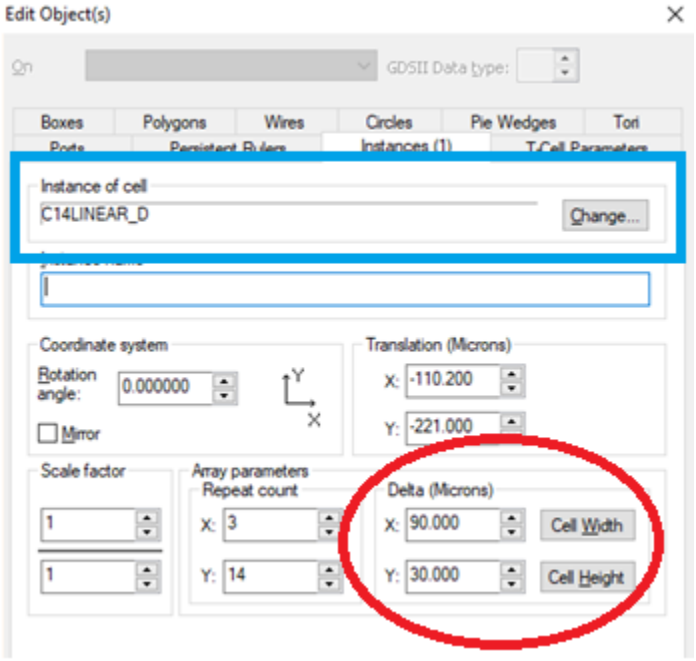


4) Change the Array Parameters Repeat Count (Red Circle) to the number of circle that are desired for a column and the number of columns in a row. For this example, there are 3 rows of columns with 14 circles. It should be noted that the direction the circles are arrayed is defined by the Coordinate system box (Blue Square).



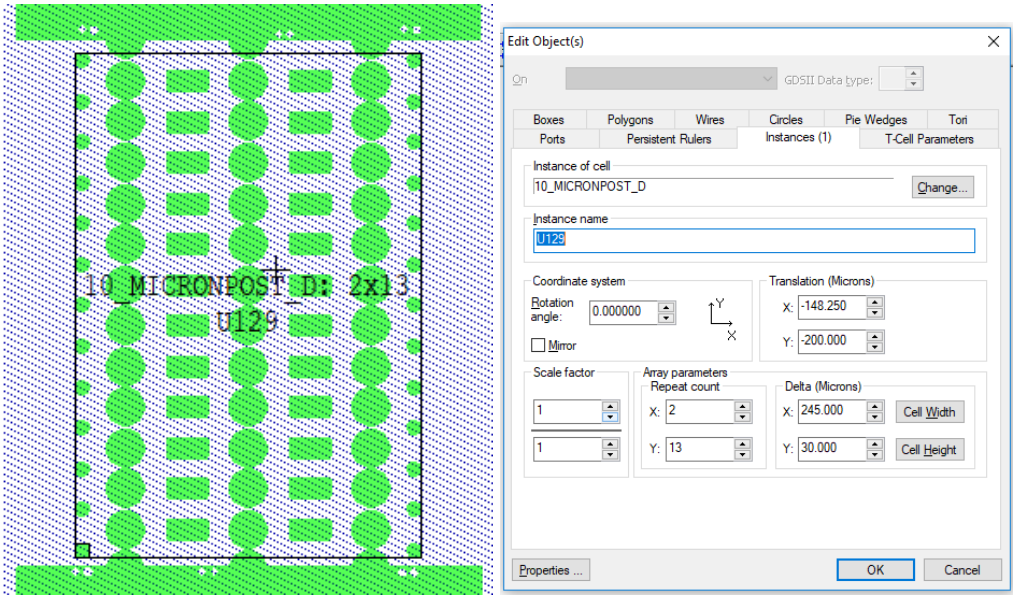


5) Change the Delta Coordinates (Red Circle): These parameters control the distance from center-to-center of the repeated circles in the X, Y directions. For our migration devices, the 14 µm radius circles are 30 µm apart in the Y-direction which results in a 2 µm constriction gap. It is important to note that with this formula, the constriction sizes are dependent on the radius of the circles and not changing the Delta Y-coordinate. Changing the Instance of Cell (Blue Square) to a circle with a 14.5 µm radius will create 1 µm gaps. For this example, the columns are 90 µm apart.



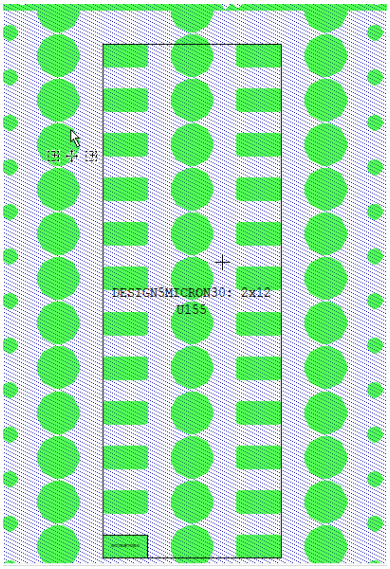
A.3.3 Boarder Pillars

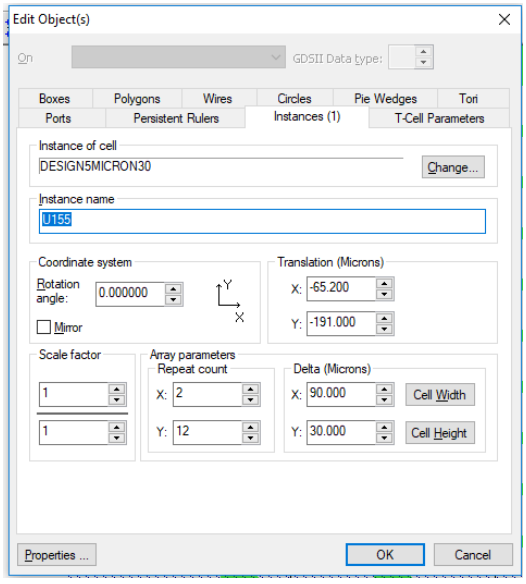
These pillars are much smaller and assist in guiding cells into the constriction channels. Create the boarder pillar array exactly the same way as constriction array discussed previously other than using a 5 µm radius circle. The Edit Objects parameters are shown below.



A.3.4 15 µm Constrictions:

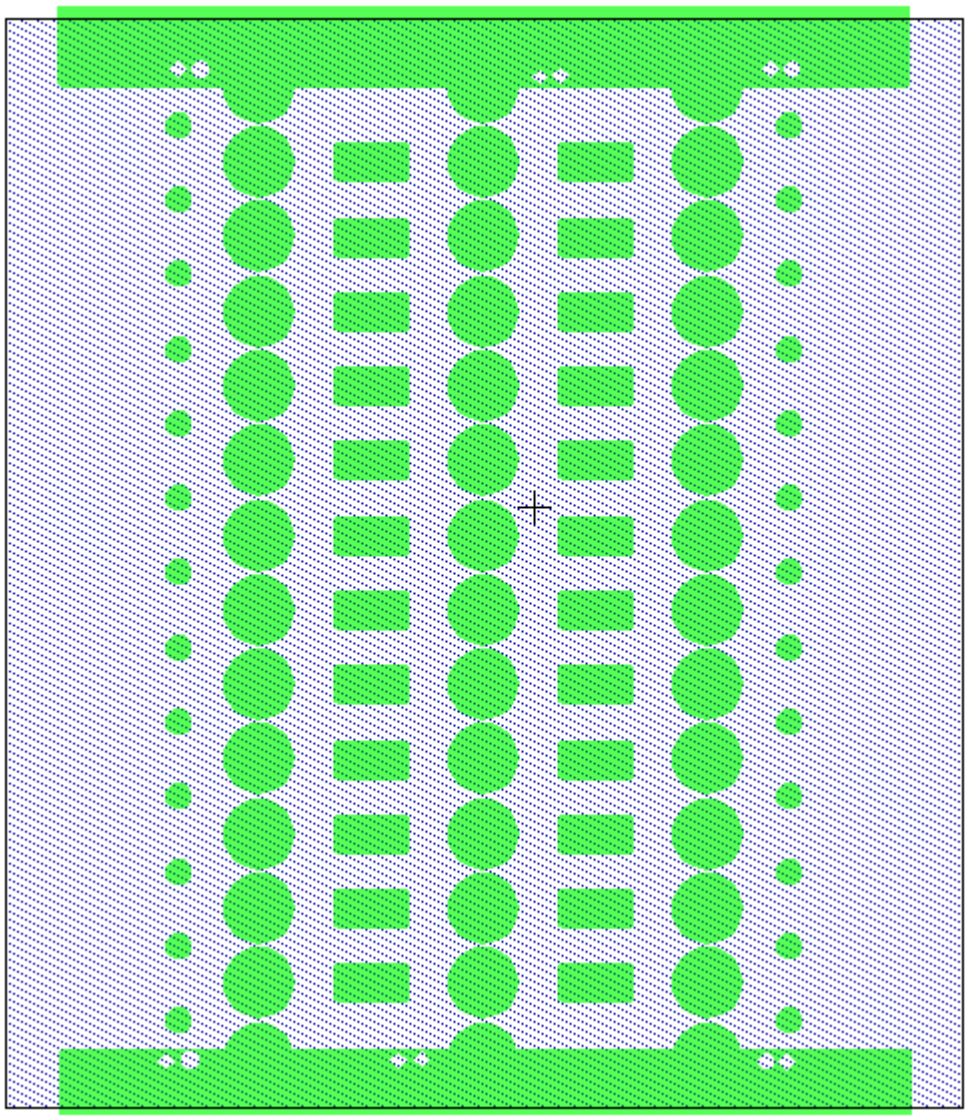
These chamfered rectangles to act help guide the cells without deforming their nuclei and parallel to the centers of the adjacent circles. Read the section on creating these rounded rectangles in the previous sections. This area also gives the cells some time for recovery and repair. This array is developed with the same Edit Objects parameters listed below.





A.3.5 Drawing the Bounding Box

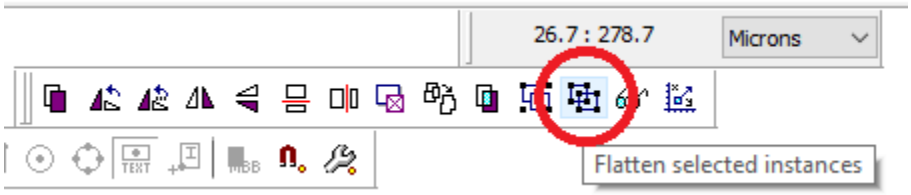
A bounding box is created on another layer that encompasses your device. It is advantageous to choose a layer that is not a solid fill so that you can visualize the feature layer # 1. Layer # 10 was chosen for this example.



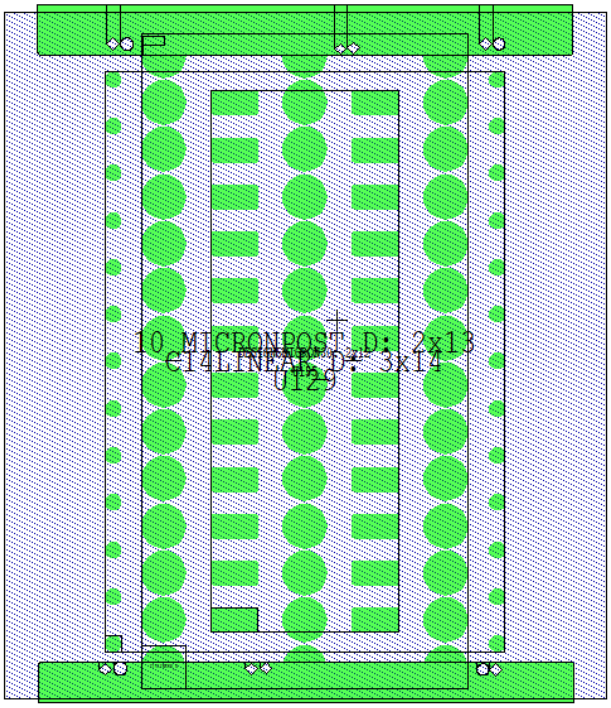
A.3.6 Tone Reversal

To create a negative image of the constrictions, we are going to subtract the green layer #1 from the blue, bounding layer # 10. Using L-Edit is much easier if the layers are kept sequential.

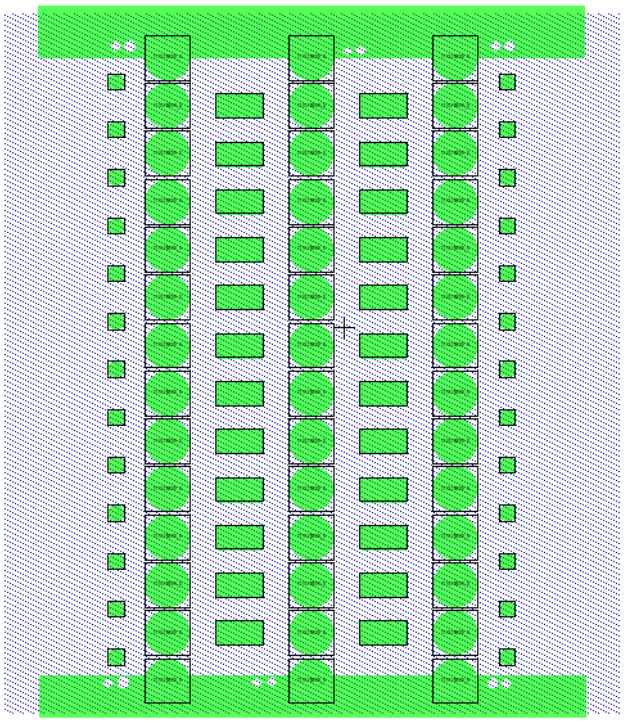
1) Right click while holding **SHIFT** to highlight (black outline) all the polygons to be subtracted. Make sure that all the edges are highlighted. If not, layer # 1 may need to be Flatten before proceeding. Flattening can be done with the toolbar icon.



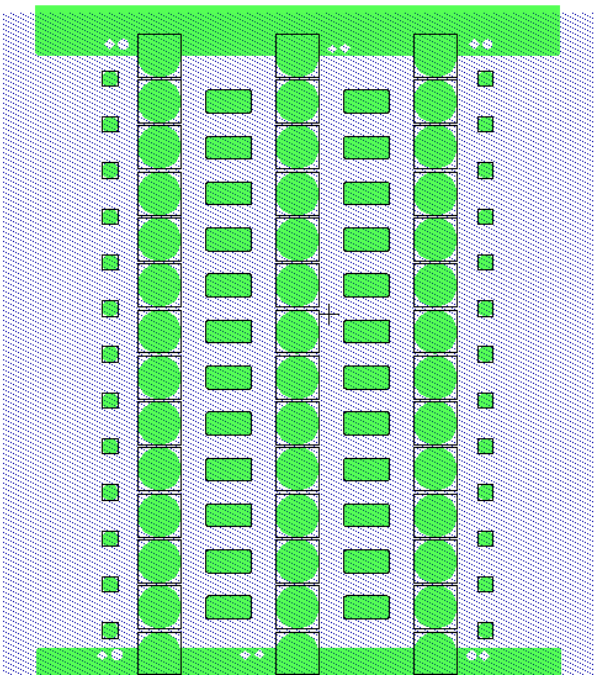
2) Flattening will have to be done three times in order to lose the instanced array status and revert back to singular shapes.



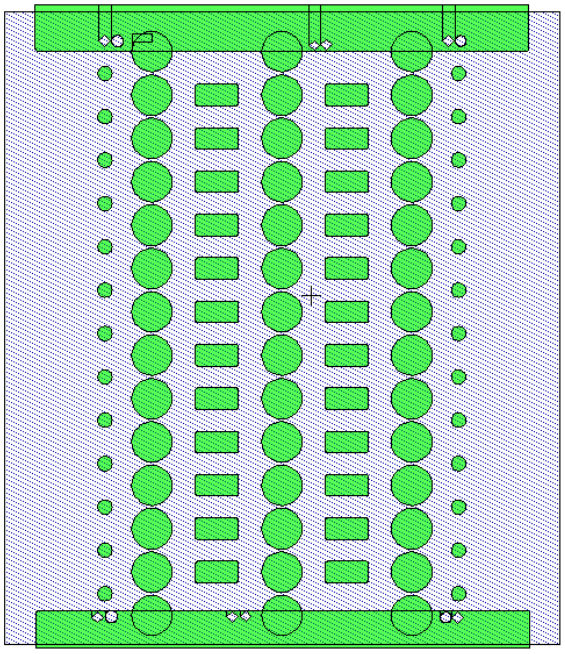
Hold **SHIFT** and Highlight all the components



After first flattened

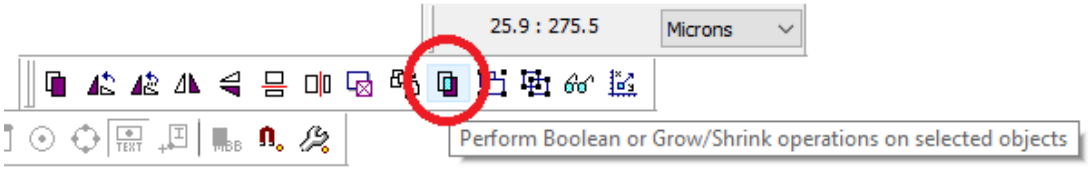


After second flattened



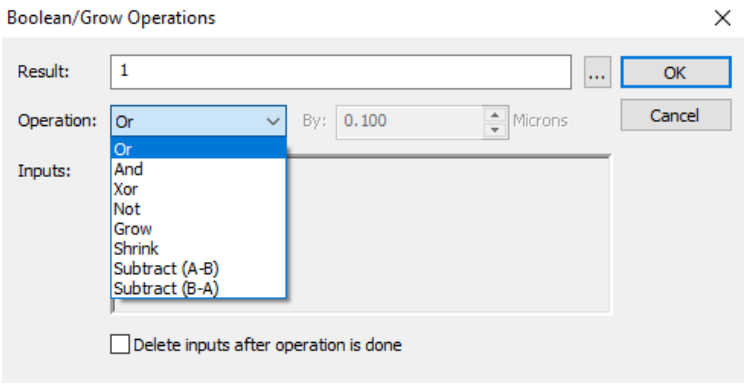
After third flattening.

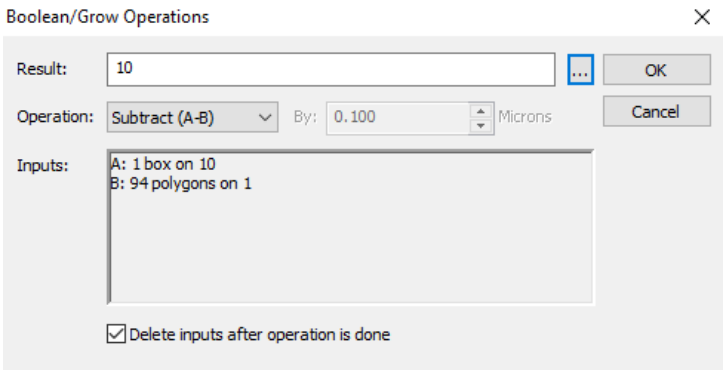
3) Make sure all shapes are still selected and click on the Boolean operation icon on the tool bar

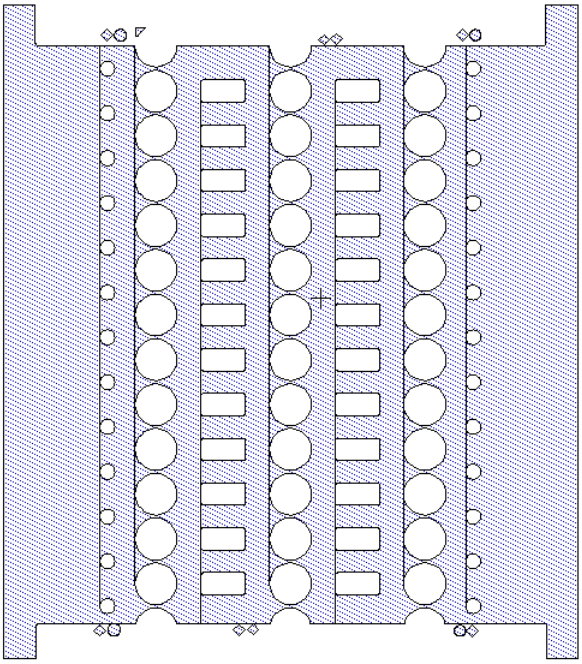


4) Scroll down the operation menu and choose Subtract (A-B). Change the result to Layer # 10 or the bounding box layer. Remember to check the box for deleting all inputs after the operation is done and click OK. This will subtract Green Layer # 1

from Layer # 10, creating an inverse image of the original design which is suitable for molding PDMS pillars.

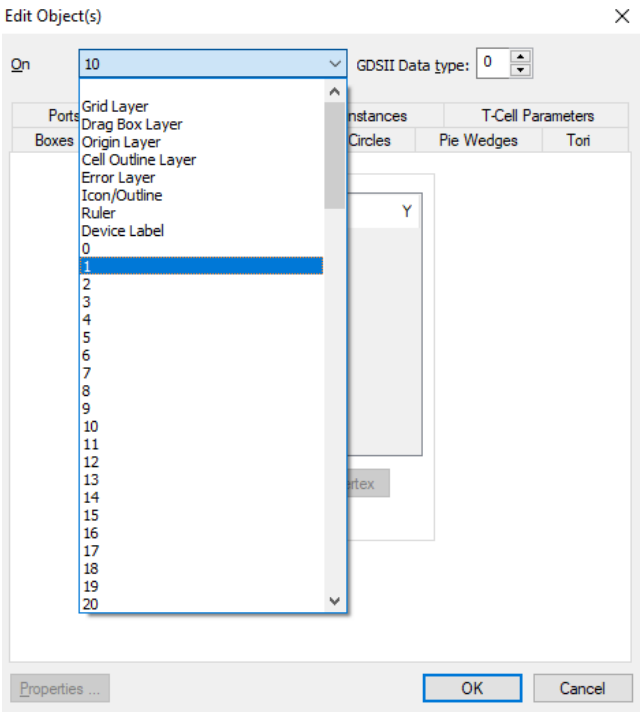




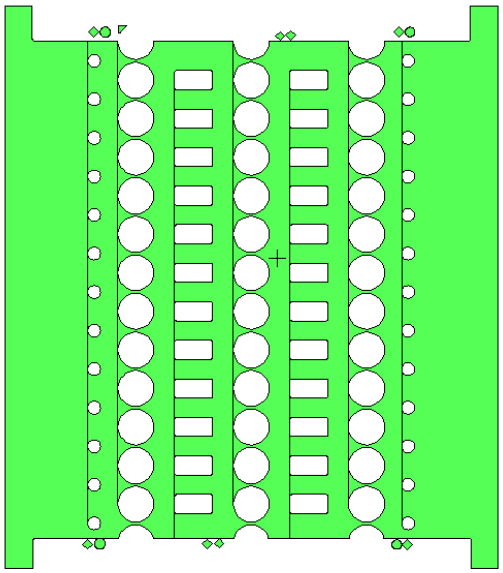


After Boolean subtraction, Design is on Layer # 10

5) With all the shapes highlighted, Use CTRL-E to change the Layer # 10 to Layer # 1 and click OK.



6) The final design should appear in green. Make sure all shapes are on the same layer.



A.3.7 Using LayoutBEAMER:

"BEAMER" or Layout BEAMER is a pattern fracturing software designed to efficiently convert complex patterns and shapes. Originally intended for electron beam lithography, BEAMER has found a niche at the CNF for converting complex L-Edit or CAD files into more manageable formats. L-edit can easily export and perform the Boolean subtraction for most of the migration design work done in the lab, but it became necessary to use BEAMER when we developed the Design # 6/Field of Pillars (FOP)/collagen mimic devices (Chapter 2.5). When I initially attempted to perform the Boolean subtraction or tone reversal on the early FOP Designs, the "loose" collagen model was the only design that was successful. The "midrange" model reversal was distorted and the tone reversal of the "dense" model would cause the software to crash. L-edit was unable to perform the binary subtraction and create the polygonal negative needed for an increased pillar density and number. This tone reversal was easily done using BEAMER which the CNF has a license for.

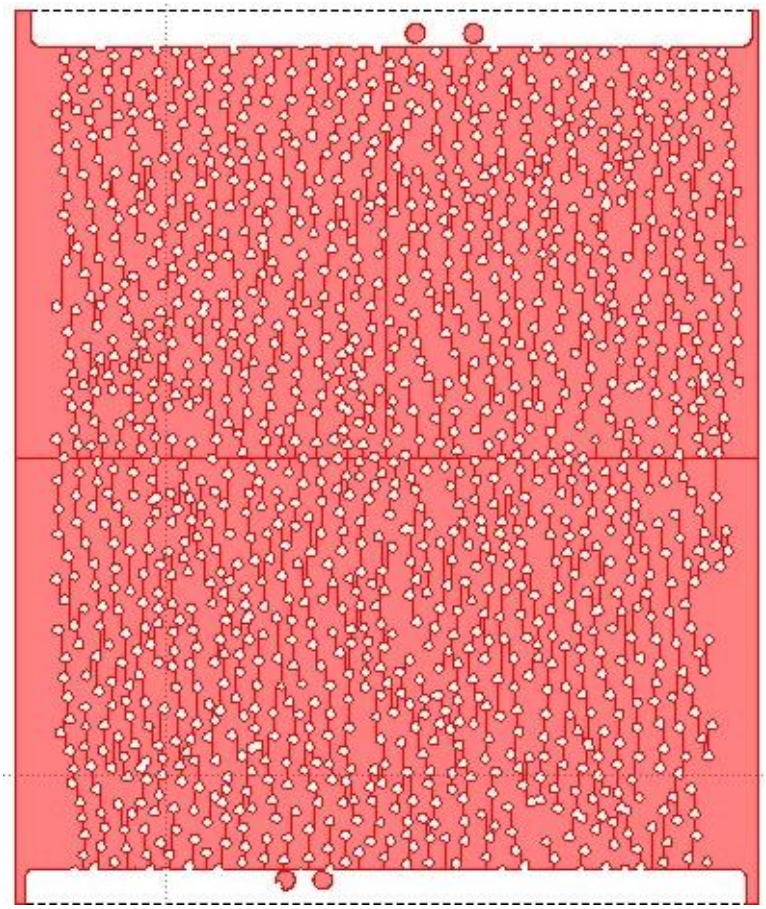
To access BEAMER on Windows at the CNF:

1) Enable the XMing server
2) Enable X11 forwarding and hit APPLY
3) Log into Korat with your Netid and CNF password
4) At the promt, type **LayoutBEAMER**

To perform a tone reversal:

1) Drag and drop two IMPORT modules into the process flow area
2) Choose the same GDS file for each
3) Right-click IMPORT and select RUN TO for each

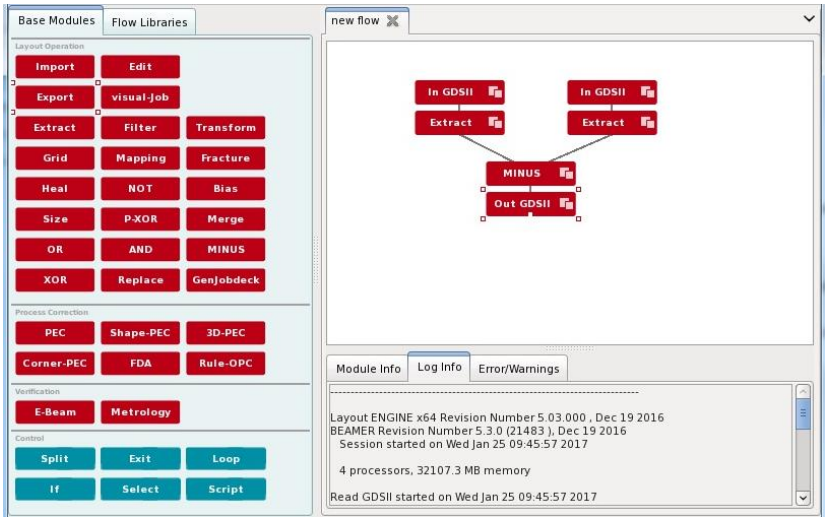
4) Drag and drop EXTRACT module over the existing IMPORT Modules. This is done by dragging the small white connection ports over one another until a connecting black line appears
5) An Extract box will appear. Choose the left-hand side as the Bounding layer #10 and the right-hand side as the constriction layer #1
6) Right-click EXTRACT and select RUN TO for each
7) Drag the MINUS module over the left and right extract so that all three are connected
8) Right-click MINUS and select RUN TO
9) Right-click MINUS and select VIEW LAYOUT, then VIEW-FILL SHAPES



10) Drag the EXPORT module over the MINUS

11) Choose the GDS file format

12) Right-click EXPORT and RUN TO



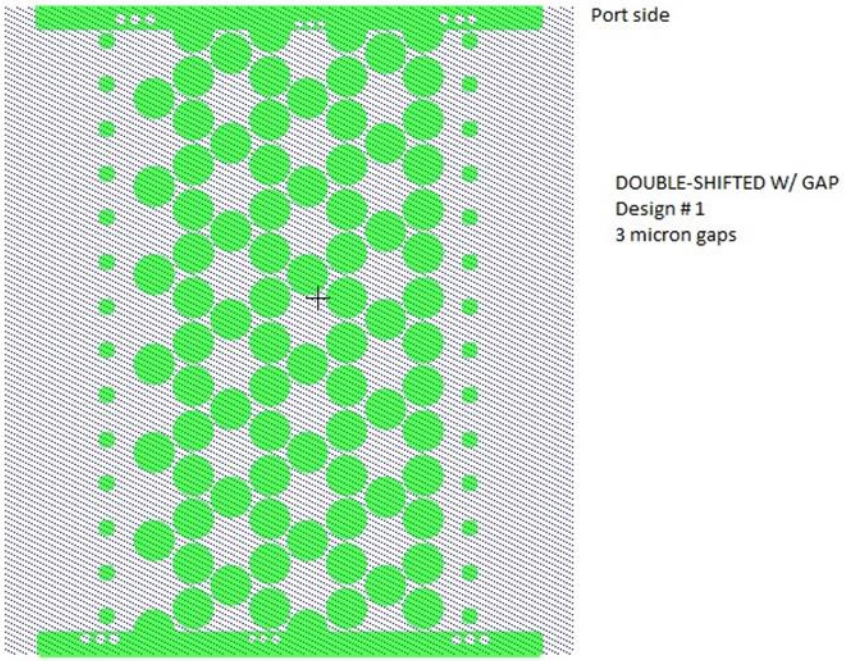
13) Save this file and Import it back into L-EDIT for your Migration Device. The imported design will be on Layer #10. Refer to Step # 6 from the previous “Tone Reversal” section on how to change back to Layer #1.

APPENDIX B

UNUSED CONSTRICTION CHANNEL DESIGNS

The following are designs created in L-Edit, but never made on to a photomask for nanofabrication. The motivation for these designs were similar to the previous round, but we wanted to add some open spaces in order to give the cells a chance to recover before entering another constriction. As mentioned previously, we learned from the first round, Design # 3 that the cells would die if they went through too many constricions without relief. L-Edit parameters are explained in Appendix A, section 3.2.

Second Round Design #1: Double-shifted with gaps



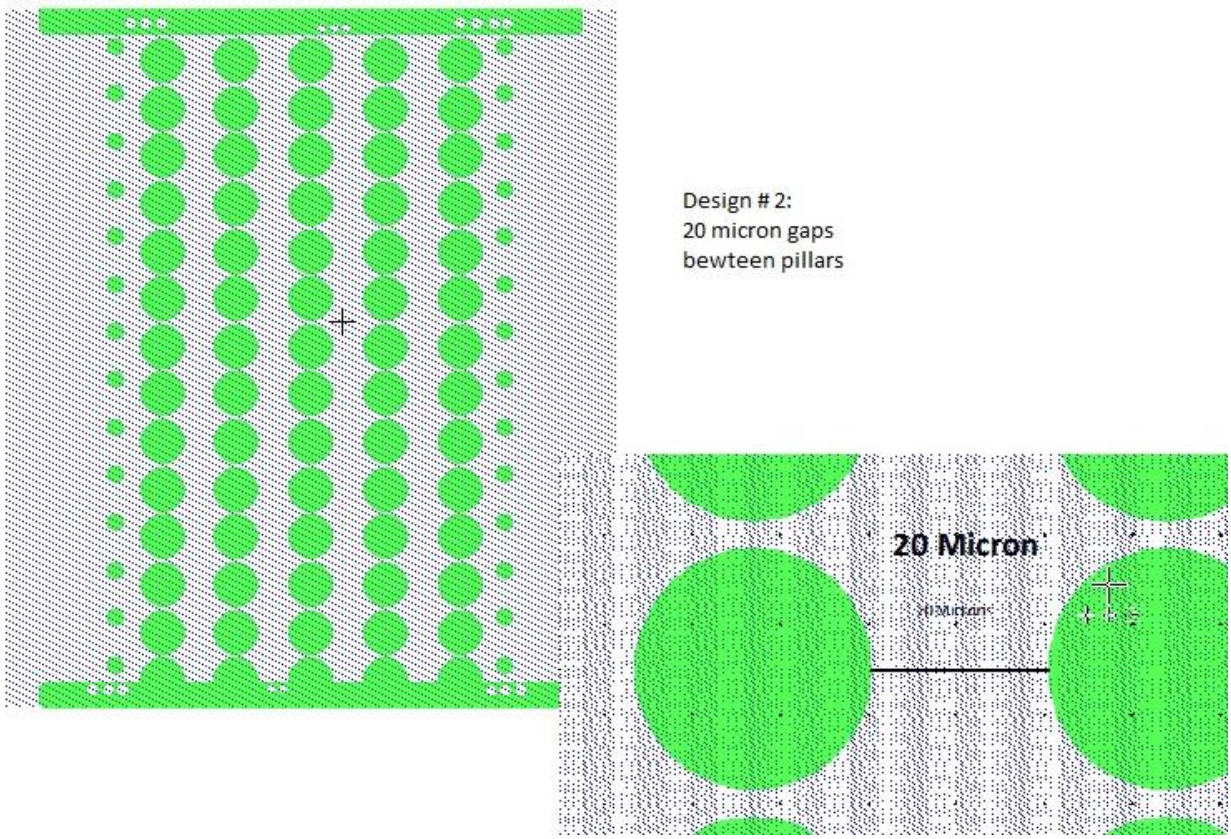
This was very similar to the first round Design # 3 double shifted model, but instead of two arrays of circles, I created three. The second column on the left has the same parameters as design # 3 and is repeated three times in the X-direction, ending on the

farthest column on the right (column eight). Column three has the same parameters as column one. Only first circle starts one row higher in the Y-axis. The row starting on the far left (column one) differs from Design # 3 in the following ways:

Far Left Parameters	X	Y
Delta	52	60
Array	1	7
Translation	-111.000	-224.925
Mid Left Parameters	**X**	**Y**
Delta	52	60
Array	1	7
Translation	-59.000	-195.000
Center Parameters	**X**	**Y**
Delta	52	60
Array	1	7
Translation	-7.000	-224.925
Far Right Parameters	**X**	**Y**
Delta	52	60
Array	1	7
Translation	45.000	-195.000

Other Parameters	X	Y
Delta	52	30
Array	4	14
Translation	-85.000	-210.000

Second Round Design # 2: One Row Gap:

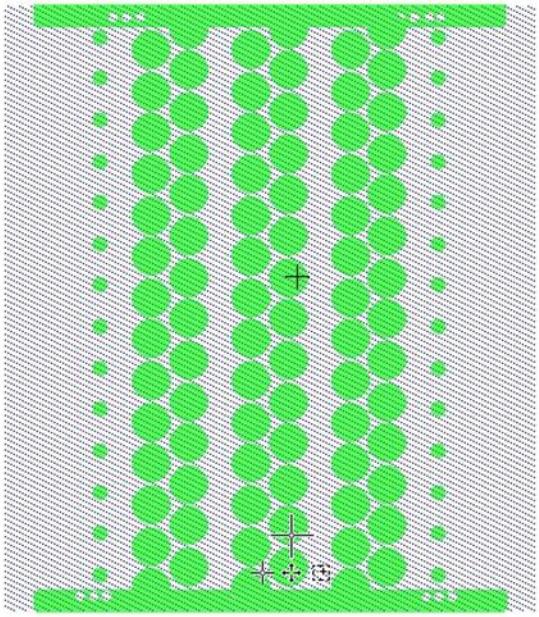


This design was developed from one circle repeated fourteen times to created a column which was repeated into five rows from left to right.

The parameters were:

Parameters	X	Y
Delta	47	30
Array	5	14
Translation	-114.000	-224.925

Second Round Design # 3: Double Shifted with 20 µm Gaps



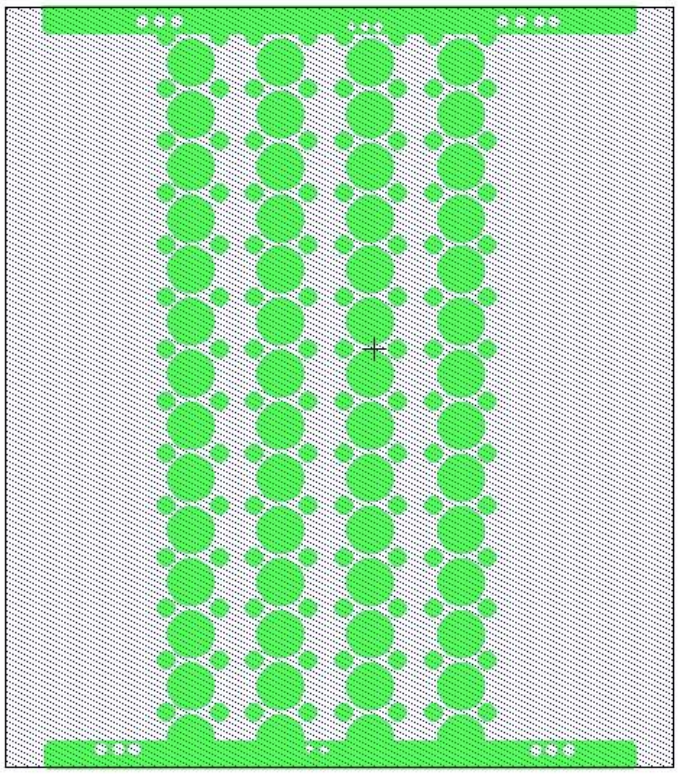
Design # 3:
Double-Shifted with
20 micron gaps

Two double-shifted columns only repeated three times and further apart.

The parameters for the far left column:

Parameters Left	X	Y
Delta	72	30
Array	3	14
Translation	-106.000	-224.925
Parameters Right	**X**	**Y**
Delta	72	30
Array	3	14
Translation	-79.000	-210.000

Second Round Design # 5a:

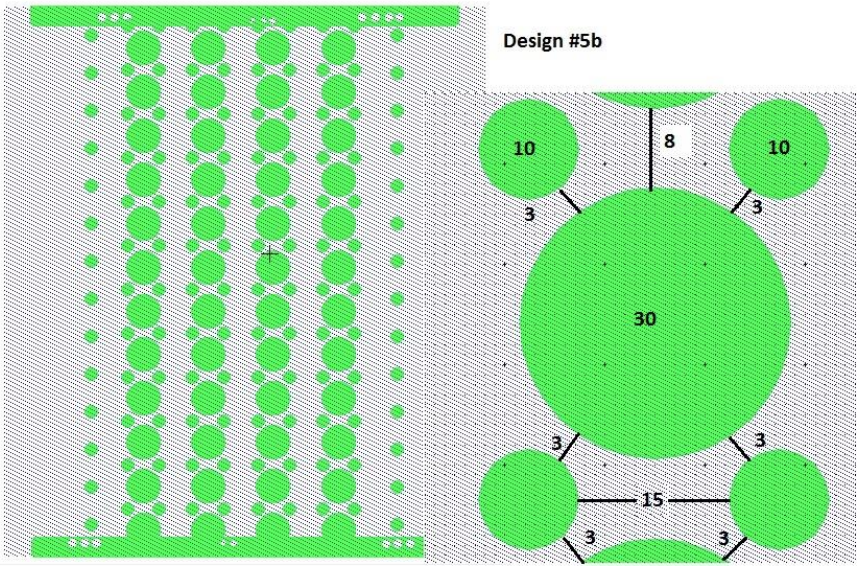


Design #5a
Larger post = 30 Micron
Small Posts = 10 Micron
All gaps = 3 Micron

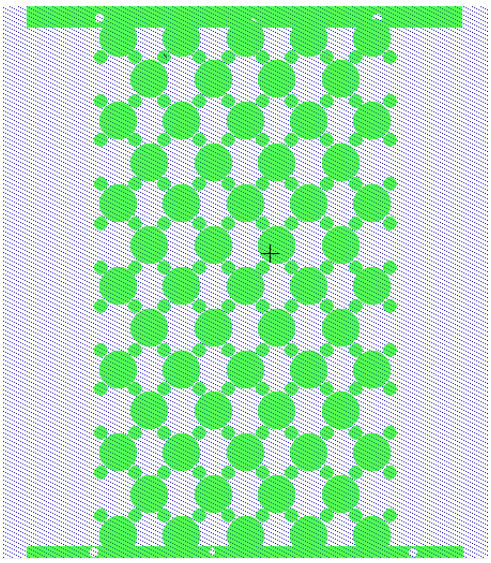
30µm Features Parameters	X	Y
Delta	52	35
Array	4	12
Translation	-101.000	-220.925

10µm Features Parameters	X	Y
Delta	72	30
Array	3	14
Translation	-79.000	-210.000

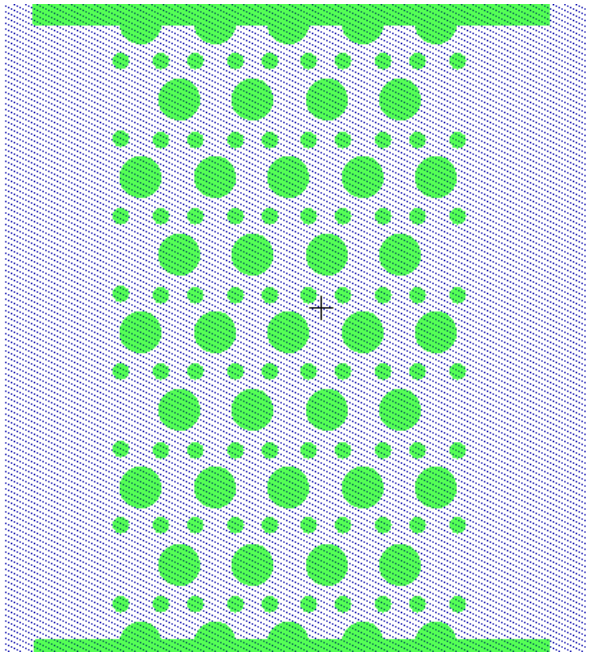
Second Round Design # 5b:



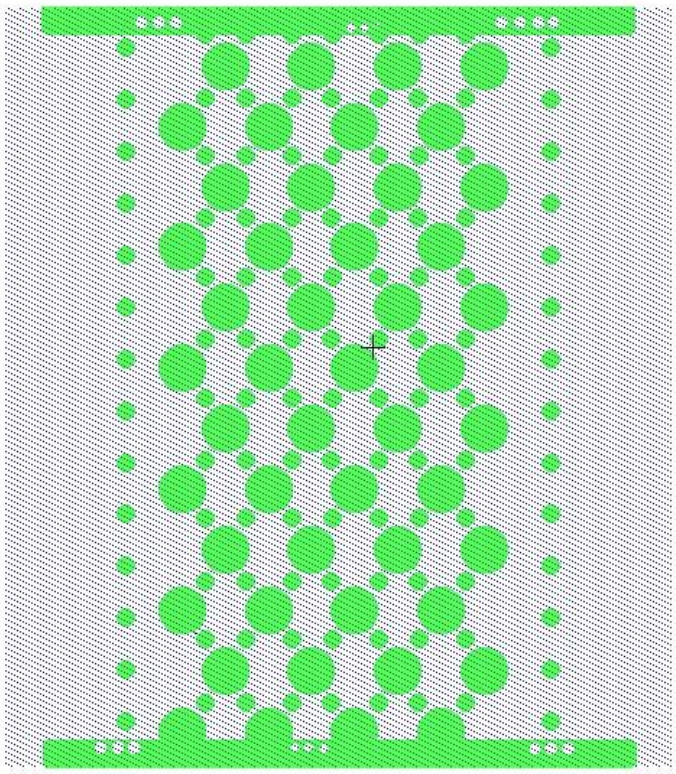
Outer 27µm Diameter Parameters	X	Y
Delta	50	70
Array	5	6
Translation	-119.400	-221.700
Inner 27µm Diameter Parameters	X	Y
Delta	50	70
Array	4	6
Translation	-94.600	-186.700
Outer 10µm Diameter Parameters	X	Y
Delta	10	70
Array	1	6
Translation	-140.600	-198.900
Lower Left 10µm Diameter Parameters	X	Y
Delta	50	70
Array	5	6
Translation	-111.600	-198.900
Lower Right 10µm Diameter Parameters	X	Y
Delta	50	70
Array	4	6
Translation	-88.600	-199.900
Upper Left 10µm Diameter Parameters	X	Y
Delta	50	70
Array	5	6
Translation	-111.600	-162.450
Upper Right 10µm Diameter Parameters	X	Y
Delta	50	70
Array	4	6
Translation	-88.200	-162.450



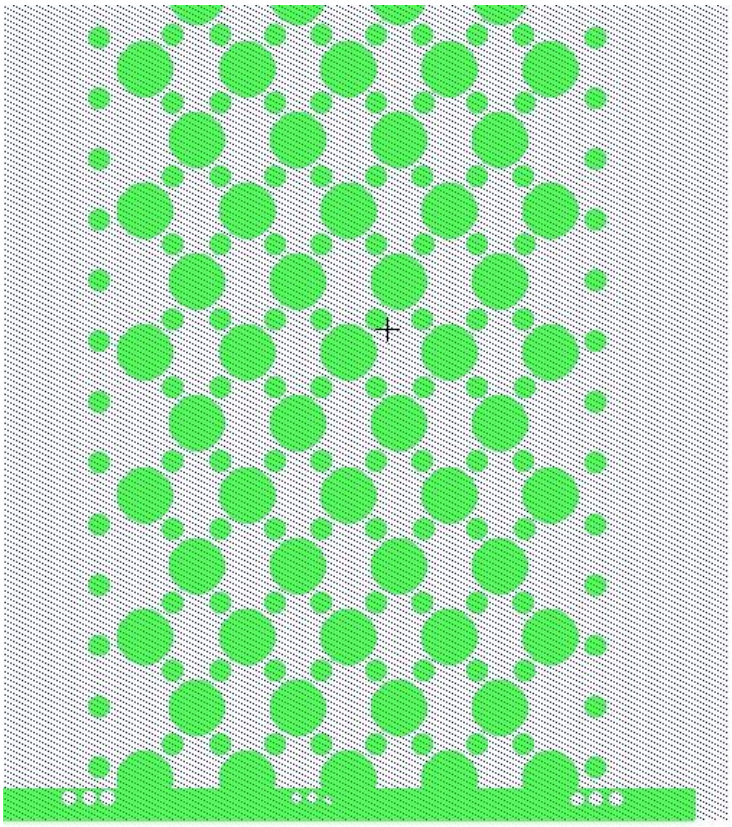
Outer 29µm Diameter Parameters	X	Y
Delta	50	65
Array	5	7
Translation	-119.400	-220.900
Inner 29µm Diameter Parameters	X	Y
Delta	50	65
Array	4	6
Translation	-94.450	-188.500
Outer 10µm Diameter Parameters	X	Y
Delta	50	65
Array	1	6
Translation	-138.400	-199.650
Lower Left 10µm Diameter Parameters	X	Y
Delta	50	65
Array	5	6
Translation	-111.200	-199.650
Lower Right 10µm Diameter Parameters	X	Y
Delta	50	65
Array	4	6
Translation	-88.600	-199.650
Upper Left 10µm Diameter Parameters	X	Y
Delta	50	65
Array	5	6
Translation	-111.200	-165.300
Upper Right 10µm Diameter Parameters	X	Y
Delta	50	65
Array	4	6
Translation	-88.600	-165.300



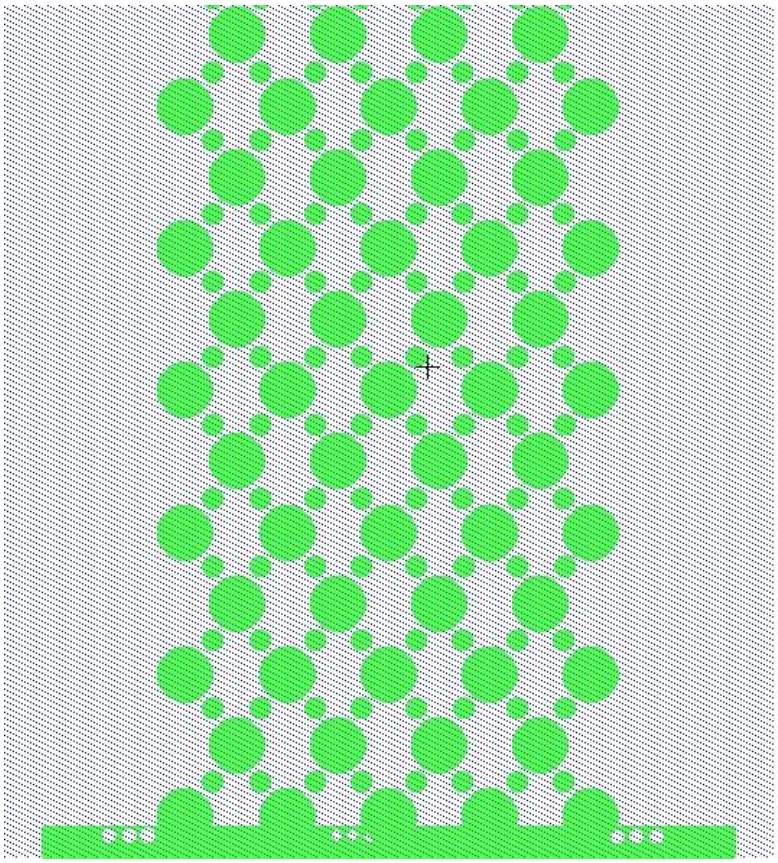
Outer 30µm Diameter Parameters	X	Y
Delta	49	102.5
Array	5	5
Translation	-119.600	-221.700
Inner 30µm Diameter Parameters	X	Y
Delta	49	102.65
Array	4	4
Translation	-94.600	-170.700
Outer 10µm Diameter Parameters	X	Y
Delta	10	103
Array	1	4
Translation	-139.000	-190.900
Lower Left 10µm Diameter Parameters	X	Y
Delta	49	102.600
Array	5	4
Translation	-111.500	-190.900
Lower Right 10µm Diameter Parameters	X	Y
Delta	49	102.600
Array	4	4
Translation	-88.700	-190.900
Upper Left 10µm Diameter Parameters	X	Y
Delta	49	102.600
Array	5	4
Translation	-111.500	-138.500
Upper Right 10µm Diameter Parameters	X	Y
Delta	49	102.600
Array	4	4
Translation	-88.700	-138.500



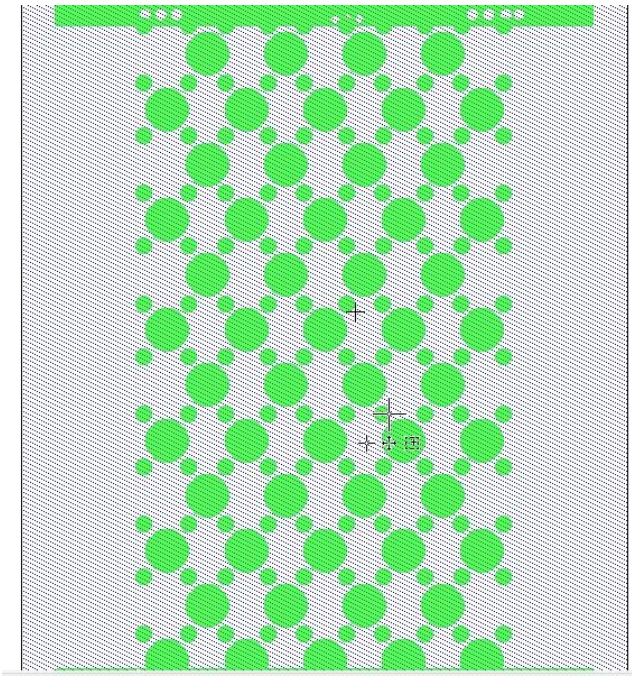
Design 5C
3 micron gaps
10 and 27 micron pillars



Design 5
with original 10 micron boarder



Design 5
Original boarder removed



Design # 5E

APPENDIX C

FABRICATING CONSTRICTION CHANNELS WITH SU-8

1) **Clean the wafers**: Clean silicon wafers using a standard hot piranha etch or MOS procedures [1] and bake overnight at 90 °C to dehydrate.

2) Spinning SU-8: Apply ~2 mL of SU-8 2005 (MicroChem) to the center of the wafer and spin at 3000 RPM for 30 seconds to obtain a 5 µm layer (see table below for the full spin curve). Allow the SU-8 to relax for 10 minutes**.**

Spin Curve for 5µm of SU-8 2005	RPM	R/S	Seconds
Ramp Up	**500**	**100**	**10**
Spin	**3000**	**300**	**30**
Ramp Down	**100**	**100**	**30**

3) Remove the Edge Bead: Remove ≈ 5 mm of excess SU-8 from the wafer perimeter using a cleanroom swab soaked in acetone.

4) **Pre-exposure bake:** Bake the wafer on a hot plate without a lid @ 95˚C for 2 ½ minutes, then remove from plate and allow to cool back to RT. This pre-exposure baking step removes the excess solvents, improves the photoresistive profile of the SU-8, and prevents adhesion to the contact mask.

5) **Expose the wafer:** Use the Karl Suss MA-6 contact aligner with hard vacuum contact settings and the long pass filter for 13.1 seconds. The hard vacuum contact settings used were pre-vacuum for 4 seconds, hard contact for 10 seconds and post-vacuum for 4 seconds.

6) **Post-exposure Bake**: Bake the wafer on a hot plate without a lid for 3 ½ minutes @ 95˚C. then remove from plate and allow to cool back to RT.

7) **Develop the Resist:** Leave wafers in SU-8 developer overnight to remove any unexposed SU-8.

8) Rinse the wafers: Rinse wafers with fresh SU-8 developer and then rinse twice with isopropyl alcohol and then deionized water.

9) Hard Bake: Bake wafers on a hot plate from RT to 160^0C for a couple of hours with a ramp rate of 1.5°C per minute. Then shut off hot plate off and allow the wafer to cool to room temperature. This hard bake step will solidifies the SU-8, relieve stress and prevents unwanted merging with the second layer. This step may relax and solidify the arched, underexposed SU-8 gaps on our devices into the relative desired widths.

[1] *MOS Cleaning is a 10 minute base dip in 1 part NH_4OH, 1 part H_2O_2 and 6 parts DI water for ten minutes, DI water rinse and an acid dip in 1 part HCl, 1 part H_2O_2 and 6 parts water for another ten minutes with a final DI water rinse.*

APPENDIX D

FABRICATING CONSTRICTION CHANNELS BY DEEP REACTIVE-ION ETCHING

1) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 2. P-20 removes any dangling water bonds from the silicon surface for better photoresist adhesion.

2) **Spinning AZ nLof 2020:** Pipette ≈2 ml of AZ nLof 2020 in the center of the wafer and spin at 3000 RPM/500/45 seconds. The resist thickness measured ≈1.7 μm.

3) **Pre-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature.

4) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer with a swab soaked in acetone.

5) **Expose of Resist:** Using the Karl Suss MA-6 contact aligner with hard vacuum contact. Expose the resist for 1.7 seconds for the Design # 6 type designs and 2.5 seconds for all other designs. Longer exposure times will create smaller pillars wider gaps. The hard vacuum contact settings used were, pre-vacuum for 4 seconds, hard contact for 10 seconds and post-vacuum for 4 seconds. Measuring the diameter of the pillars to make sure the exposure was not too long. The pillars should measure 5μm in diameter. Longer exposure times will create smaller pillars/larger gaps.

6) **Post-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature. Longer bakes will distort the sidewalls of the resist (AZ® nLOF 2000, 2016).

7) **Develop the Resist:** Place the wafer in the Hammatech's four-inch wafer holder and develop with MIF 726 developer for 120 seconds.

8) **Examine the Wafer:** Developing sometimes leaves artifacts and areas of incomplete development. It is also important to look for other lithography issues before wasting time etching. Remove poor lithography with step # 11 and reuse the wafer.

9) **Perform a De-scum:** This will remove any unseen nanometer areas of resist with a low power oxygen plasma. There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers.

10) **DRIE Etching:** If no one has ran the Unaxis 770 before this step, run 35 loops of the **0Trench** recipe on a dummy wafer to warm up the tool. The etch rate for this design is 280 nm etch/per loop, so eighteen loops should etch 5 µm into the silicon.

11) **Remove the Photoresist:** Used the Anatech asher "O2 Stripping" recipe for 5-10 minutes.

APPENDIX D

FABRICATING CONSTRICTION CHANNELS BY REACTIVE-ION ETCHING

1) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 2. P-20 removes any dangling water bonds from the silicon surface for better photoresist adhesion.
2) **Spinning AZ nLof 2020:** Pipette ≈2ml of AZ nLof 2020 in the center of the wafer and spin at 3000 RPM/500/45 seconds. The resist thickness should measure ≈1.7 µm.
3) **Pre-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature.
4) **Remove the Edge Bead:** Remove 5mm of resist from the edge of the wafer with a swab soaked in acetone.
5) **Expose of Resist**: Use the Karl Suss MA-6 contact aligner with hard vacuum contact settings. Expose the resist for 3.4 seconds for the Design # 6 type designs and 4.0 seconds for all other designs. The hard vacuum contact settings used were pre-vacuum for 4 seconds, hard contact for 10 seconds and post-vacuum for 4 seconds. Measuring the diameter of the pillars to make sure the exposure was not too long. The pillars measure 5 µm in diameter. Longer exposure times will create smaller pillars/larger gaps.
6) **Post-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature. Longer bakes will distort the sidewalls of the resist (AZ® nLOF 2000, 2016).
7) **Develop the Resist:** Place the wafer in the Hammatech's four inch wafer holder and develop with MIF 726 developer for 120 seconds.

8) **Examine the Wafer:** Developing sometimes leaves artifacts and areas of incomplete development. This step is critical because any problems or irregularities with the lithography will transfer to the silicon etch. If observed, rerun step # 5. If the lithography is still compromised, remove the photoresist with step # 12 and rerun the process starting at step #1.

9) **Perform a De-scum:** This will remove any nanometer thick areas of resist that remained after development. Use a low power oxygen plasma. There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers.

10) **RIE Etching, Season the Chamber:** On a dummy wafer, run the **NICKZOR1** (photonics etch) recipe for five minutes to season the chamber. This will remove any residual DRIE polymers and contaminates from the chamber that may be detrimental to the RIE etch.

11) **RIE Etching:** Load the wafer and etch with the **NICKZOR1** (photonics etch) recipe for thirty-five minutes (etch rate ≈ 130 nm/minute for the cell migration devices).

12) **RIE Etching, Release:** Unload the etched wafer and reload the dummy wafer. Etch for forty minutes with the **0RELEASE** recipe (or the Photonics etch time + five minutes). This will remove the photonics etch polymers and contaminates from the chamber.

13) **DRIE Etching:** Run forty loops of **0trench** to return the chamber to a suitable environment for DRIE etching.

14) **Remove the Photoresist:** Used the Anatech asher “O2 Stripping” recipe for 5-10 minutes.

APPENDIX F

FABRICATING THE UPPER SU-8 LAYER OF CELL MIGRATION DEVICES

1) **For silicon etched features only:** Strip the photoresist in an oxygen plasma tool. Clean the wafers with a hot piranha etch.
2) **For silicon and SU-8 wafers:** dehydrate the wafers overnight in a 90°C oven.
3) **Cover alignment marks:** Remove the wafers from the oven and quickly conceal the 5 µm layer alignment marks with a piece of Kapton (polyamide) tape. Cut the tape to a point in the center so that it does not interfere with any migration devices nearby. If Kapton tape is unavailable, used a cleanroom alpha swab with acetone to remove the freshly spun SU-8 from the alignment marks during step #5.
4) **Spinning SU-8:** For a thickness of 200 µm, pour out an inch size puddle of SU-8 100 on the center of the wafer and spin at 1500 RPM for 60 seconds (see table below for the full spin curve). Allow the SU-8 to relax for 10 minutes.

Spin Curve for 200µm of SU-8 100	RPM	R/S	Seconds
Ramp Up	**500**	**100**	**10**
Spin	**1500**	**100**	**60**
Ramp Down	**100**	**100**	**15**

5) **Remove the Edge Bead:** Remove ≈ 5 mm of excess SU-8 from the wafer perimeter using a cleanroom swab soaked in acetone.
6) **Pre-exposure bake:** Bake the wafer on a hot plate with a lid propped up with two microscope slides. Increase the temperature from RT to 62.5°C at a rate of 1.5 °C per minute for ≈8 hours. Increase again to 67.5 °C at a rate of 1.5°C per minute for ≈14 hours (or overnight) and leave to cool back to RT on the hot plate.

7) **Remove the tape:** Score the edges of the Kapton tape with a razor and gently remove the tape from the wafer. Use a nitrogen gun to remove any SU-8 particles off the wafer.

8) **Expose the wafer**: Expose the wafer on the ABM contact aligner with a Long pass filter for 36 seconds, six times with 36 seconds of rest in-between. The UV lamp intensity can decrease over its lifetime, and therefore the optimal exposure time for this step may vary.

9) **Post-exposure Bake**: Soon after the exposure, bake the wafer on a hot plate with a lid propped up with two microscope slides. Increase the temperature from RT to 95 °C at a rate of 1.5 °C per minute and hold at 95°C for 1 minute. Turn off the hot plate and leave the wafer to cool back to RT.

10) **Develop the Resist:** Leave wafers upside down in SU-8 developer overnight to remove any unexposed SU-8.

11) **Rinse the wafers:** Rinse wafers with fresh SU-8 developer and then rinse with isopropyl alcohol and deionized water two times each. Leave the wafers in a fume hood for two hours or in an oven @ 30 °C on an aluminum plate to remove moisture and leave to cool in the oven to RT.

12) **Deposit FOTS**: Use the Molecular Vapor Deposition tool to deposit the anti-stiction coating fluroctatriclorosilane (FOTS).

APPENDIX G

FABRICATING SILICON PILLARS BY DEEP REACTIVE-ION ETCHING

1) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 2. P-20 is used to remove any dangling water bonds of the silicon surface for better photoresist adhesion.
2) **Spinning AZ nLof 2020:** Pipette ≈2 ml of AZ nLof 2020 in the center of the wafer and spin at 3000 RPM/500/45 seconds. The resist thickness measured ≈1.7 µm.
3) **Pre-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature.
4) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer with a swab soaked in acetone.
5) **Expose of Resist:** Using the Karl Suss MA-6 contact aligner, expose the resist for 1.6 seconds with Hard Vacuum Contact for all Design #6 work. The hard vacuum contact settings used were: pre-vacuum for 4 seconds, hard contact for 10 seconds and post-vacuum for 4 seconds. Measuring the diameter of the pillars to test if the exposure was not too long. The pillars should measure 5 µm in diameter. Longer exposure times will create smaller pillars.
6) **Post-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature. Longer bakes will distort the sidewalls of the resist (AZ nLof, 2016).
7) **Develop the Resist:** Place the wafer in the Hammatech's four-inch holder and develop with MIF 726 developer for 120 seconds.

8) **Examine the Wafer:** Liftoff sometimes leaves artifacts and areas that haven't lifted off. If this is observed, try to sonicate the wafer in acetone. If that isn't effective, heat the wafer on a hotplate set @ 110^{o}C for 60 seconds and continue sonication. Lightly scrubbing the wafer with an Alpha Swab soaked in acetone or 1165 developer may also work.

9) **Perform a De-scum:** There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers.

10) **Evaporate Al_2O_3:** Place the wafer either in the center of a flat platen or in a tapered, four-inch wafer lift-off platen. Using the Even-Hour evaporator, deposit 50nm of Al_2O_3 at a rate ≈ 1.8-2.0 Angstroms/seconds. Let cool in bell jar for 10 minutes before venting.

11) **Lift-off the Resist:** Soak the wafer in acetone for 30 minutes. You may want to sonicate the wafer if needed. Rinse wafer with IPA and water.

12) **DRIE Etching:** If the Unaxis 770 has not been run before, run 35 loops of the **0Trench** recipe on a dummy wafer to warm up the tool. The etch rate for this design is 720 nm etch/per loop, so eight loops should etch 5 μm into the silicon.

13) **Remove the Al_2O_3:** With metal wafer tweezers, submerge the wafer in ≈ 30 ml of hydrofluoric acid (HF) for 30 seconds. Remove the wafer and rinse multiple times in DI water.

APPENDIX H

FABRICATING THE BYPASS CHANNELS AND CELL CHAMBERS WITH SILICON PILLARS BY DRIE

A method was created by following the standing pillar and ports/bypass processes flows:

1) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 2. P-20 is used to remove any dangling water bonds of the silicon surface for better photoresist adhesion.
2) **Spinning AZ nLof 2020:** Pipette ≈2 ml of AZ nLof 2020 in the center of the wafer and spin at 3000 RPM/500/45 seconds. The resist thickness measured ≈1.7 µm.
3) **Pre-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature.
4) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer with a swab soaked in acetone.
5) **Expose of Resist:** Using the Karl Suss MA-6 contact aligner, expose the resist for 1.6 seconds with Hard Vacuum Contact. The hard vacuum contact settings used were: pre-vacuum for 4 seconds, hard contact for 10 seconds and post-vacuum for 4 seconds. Measuring the diameter of the pillars to test if the exposure was not too long. The pillars should measure 5 µm in diameter. Longer exposure times will create smaller pillars.
6) **Post-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature. Longer bakes will distort the sidewalls of the resist (see AZ nLof, 2016).

7) **Develop the Resist:** Place the wafer in the Hammatech's a four inch holder wafer holder and develop with MIF 726 developer for 120 seconds.

8) **Examine the Wafer:** Liftoff sometimes leaves artifacts and areas that haven't lifted off. If this is observed, try to sonicate the wafer in acetone. If that isn't effective, heat the wafer on a hotplate set @ 110^{o}C for 60 seconds and continue sonication. Lightly scrubbing the wafer with an Alpha Swab soaked in acetone also works.

9) **Perform a De-scum:** There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers.

10) **Evaporate Al_2O_3:** Place the wafer either in the center of a flat platen or in a tapered, four-inch wafer lift-off platen. Using the Even-Hour evaporator, deposit 50 nm of Al_2O_3 at a rate ≈ 1.8-2.0 Angstroms/seconds. Let cool in bell jar for 10 minutes before venting.

11) **Lift-off the Resist:** Soak the wafer in acetone for 30 minutes. You may want to sonicate the wafer if needed. Rinse wafer with IPA and water.

12) **DRIE Etching:** If the Unaxis 770 has not been run before, run 35 loops of the **0Trench** recipe on a dummy wafer to warm up the tool. The etch rate for this design is 720 nm etch/per loop, so eight loops should etch 5 µm into the silicon.

13) **Remove the Al_2O_3:** With metal wafer tweezers, submerge the wafer in ≈ 30 ml of hydrofluoric acid (HF) for 30 seconds. Remove the wafer and rinse multiple times in DI water and dry.

14) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 15. P-20 is used to remove any dangling water bonds of the silicon surface for better photoresist adhesion.

15) **Spinning Shipley 1813:** Pipette ≈2 ml of Shipley 1813 in the center of the wafer and spin at 4000 RPM/1000/30 seconds. Because of the etched features on the wafer, you may want to create a larger resist puddle before spinning.

16) **Pre-exposure Bake:** Bake the wafer on a preheated 90^{o}C hot plate for 60 seconds and let cool to room temperature.

17) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer and over the alignment marks with a swab soaked in acetone.

18) **Expose of Resist:** Using the ABM contact aligner, expose the resist for 19 seconds for the original and 17.5 seconds for the etched version. Measuring the constriction channel was a good way to test if the exposure was too long. The constriction channel off the photomask measured ≈ 280 µm and this exposure measured 275 µm. Future runs may use a lower exposure time.

19) **Develop the Resist:** Place the wafer in the Hammatech's a four inch holder wafer holder and develop with MIF 726 developer for 60 seconds.

20) **Perform a De-scum:** There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers. The PT 72 "O2 clean" program was used.

21) **DRIE Etching:** If the Unaxis 770 has not been run before you, run 35 loops of the **0Trench** recipe on a dummy wafer to warm up the tool. Five loops etched 2.8-2.9 µm deep on the first attempt, establishing an etch rate of ≈570 nm etch/per loop, for this design.

22) **Removing the Resist:** Used either the Anatech asher "O2 Stripping" recipe for 5-10 minutes or soak in acetone and clean with IPA and water.

APPENDIX I

FABRICATING PDMS MOLDS FOR UPPER LAYER OF CELL MIGRATION DEVICE

1) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 2. P-20 is used to remove any dangling water bonds of the silicon surface for better photoresist adhesion.
2) **Spinning Shipley 1813:** Pipette ≈2 ml of Shipley 1813 in the center of the wafer and spin at 4000 RPM/1000/30 seconds. The resist thickness measured 1.369 µm.
3) **Pre-exposure Bake:** Bake the wafer on a preheated 90^{o}C hot plate for 60 seconds and let cool to room temperature.
4) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer with a swab soaked in acetone.
5) **Expose of Resist:** Using the ABM contact aligner, expose the resist for 19 seconds for the original and 18 seconds for the etched version. Measuring the constriction channel was a good way to test if the exposure was not too long. The constriction channel off the photomask measured ≈ 280 µm and this exposure measured 275 µm. Future runs may use a lower exposure time.
6) **Develop the Resist:** Place the wafer in the Hammatech's four-inch holder and develop with MIF 726 developer for 60 seconds.
7) **Examine the Wafer:** Liftoff sometimes leaves artifacts and areas that haven't lifted off. If this is observed, try to sonicate the wafer in acetone. If that isn't effective, heat the wafer on a hotplate set @ 110^{o}C for 60 seconds and continue sonication. Lightly scrubbing the wafer with an Alpha Swab soaked in acetone also works.

8) **<u>Perform a De-scum</u>:** There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers. The Anatech de-scum program for 90 seconds was used.

9) **<u>Evaporate Al_2O_3</u>:** Place the wafer either in the center of a flat platen or in a tapered, four-inch wafer lift-off platen. Using the Even-Hour evaporator, deposit 100nm of Al_2O_3 at a rate ≈ 1.8-2.0 Angstroms/seconds. Let cool in bell jar for 10 minutes before venting.

10) **<u>Lift-off the Resist</u>:** Soak the wafer in acetone for 30 minutes. You may want to sonicate the wafer if needed. Rinse wafer with IPA and water.

APPENDIX J

FABRICATING CONSTRICTION GEOMETERIES IN FUSED SILICA

1) **Sputtering Chromium**: 300 nm of chromium was sputtered on four fused silica wafers as a hard mask for etching fused silica. This work was orginially done using a CVC 601 sputtering tool, but that tool was recently decommissioned by the CNF. Possible alternatives for any future chromium depositions at the CNF would be either AJA sputtering tools or the CHA Mark 50 E-beam Evaporator set up for conformal deposition.
2) **Spinning P-10**: Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 2. P-20 removes any dangling water bonds from the silicon surface for better photoresist adhesion.
3) **Spinning AZ nLof 2020:** Pipette ≈2 ml of AZ nLof 2020 in the center of the wafer and spin at 3000 RPM/500/45 seconds. The resist thickness should measure ≈1.7 µm.
4) **Pre-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature.
5) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer with a swab soaked in acetone.
6) **Expose of Resist**: Use the Karl Suss MA-6 contact aligner with hard vacuum contact settings. For this initial test, we exposed for 3.0 seconds. The hard vacuum contact settings used were pre-vacuum for 4 seconds, hard contact for 10 seconds and post-vacuum for 4 seconds. Measuring the diameter of the pillars to make sure, the exposure wasn't too long. The pillars should measure 5 µm in diameter. Longer exposure times will create smaller pillars/larger gaps.

7) **Post-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature. Longer bakes will distort the sidewalls of the resist (AZ® nLOF 2000, 2016).

8) **Develop the Resist:** Place the wafer in the Hammatech's four-inch wafer holder and develop with MIF 726 developer for 120 seconds.

9) **Examine the Wafer:** Developing sometimes leaves artifacts and areas of incomplete development. This step is critical because any problems or irregularities with the lithography will transfer to the silicon etch. If observed, rerun step # 8. If the lithography still has issues, remove the photoresist with step # 12 and rerun the process starting at step #1.

10) **Perform a De-scum:** This will remove any nanometer thick areas of resist that remained after development. Use a low power oxygen plasma. There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers.

11) **Etching Chromium, O2 Clean:** Using the Trion Minilock III ICP-RIE tool, load a sapphire wafer and run the **"O2 Clean"** recipe for 600 seconds.

12) **Etching Chromium, Cl2/N2 Clean:** Run the **"Cl2/N2 Clean"** recipe for 600 seconds.

13) **Etching Chromium, Seasoning the Chamber:** For more consistent etch results, unload the sapphire wafer and load a chromium sputter target. Etch the target with the **"CR STANDARD ETCH"** recipe for 600 seconds before loading your wafers into the Trion.

14) **Etching Chromium, Etch your Wafer:** Unload the sputter target and load your wafer into the tool. It may be advantageous to split the calculated etch time into two shorter etches. This will avoid overheating the fused silica wafer and drastically

increase the etch rate. Our test etch was split into two, seven and six minute etches. In addition, this break will provide an opportunity to measure the etch depth and rate on the profilometer.

15) **Remove the Photoresist**: Using the oxygen etch recipe on the Oxford 81 to remove the photoresist. The etch rate of photoresit with this recipe is 200 nm/minute. This step is important because the photoresist may become an insoluble polymer after fused silica etching.

16) **Fused Silica Etching, Pre-Heat/Pre-clean the Chamber:** Load the wafer and run the **"Oxygen Preheat Preclean"** recipe for 10 minutes before and in-between newly loaded wafers. This step will pre-heat the chamber to 50^{o}C.

17) **Etching Fused Silica:** Run the **"CHF3/Ar Fused Silica"** recipe. The etch rate is 190-200 nm/minute. We etched for thirty-two minutes to a depth of ≈ 6.0 µm deep holes with ≈ 200 nm of chromium remaining.

18) **Fused Silica Etching**: Remove the wafer and run the **"Oxygen Clean"** recipe for the amount of time as the etch (in our case, thirty-two minutes).

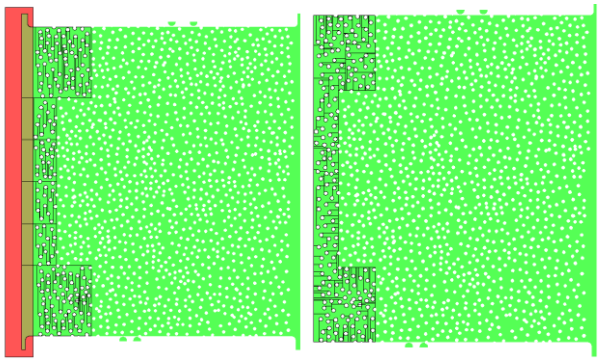
19) **Etch away the Chormium Mask**: Removed the mask in Cyantek CR-14 chromium etchant solution. The etch rate @ RT is 80 nm/minute. After etching, rinse throughly with DI water.

APPENDIX K

FABRICATING ONE SQUARE INCH FIELD OF PILLARS

As a spinoff of Design # 6 (Chapter 2.5), we were interested in producing larger sections of PDMS 5 µm pillars for cell migration experiments. Absent of cell ports, bypass channels or chambers, only cell media reservoirs would be punched in the PDMS where needed, As a proof of concept, the midrange design # 6 constrictions CAD was trimmed and modified to create a ≈320 µm x 400 µm rectangle that was arrayed into an one inch by one inch field of pillars (Figures 1 & 2). The following are the L-Edit steps for making a contact mask.

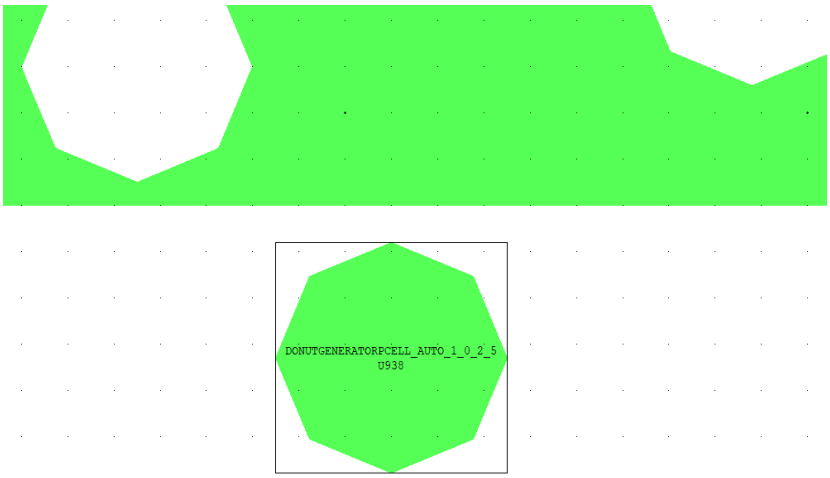
1) Open or import the MID_BOOL.GDS file.
2) If needed, use **CTRL-E** to change the Layer # 10 to Layer # 1.
3) Create a 100 µm x 500 µm rectangle on Layer # 2.
4) Line up the rectangle vertically over the vertical edge of the field of pillars. The goal is to create a rectangle by cover up and subtracting the sides of the migration walls and any empty space before the pillars start.
5) Once the layer # 2 rectangle is lined up. Select both layers and perform the Boolean subtraction.



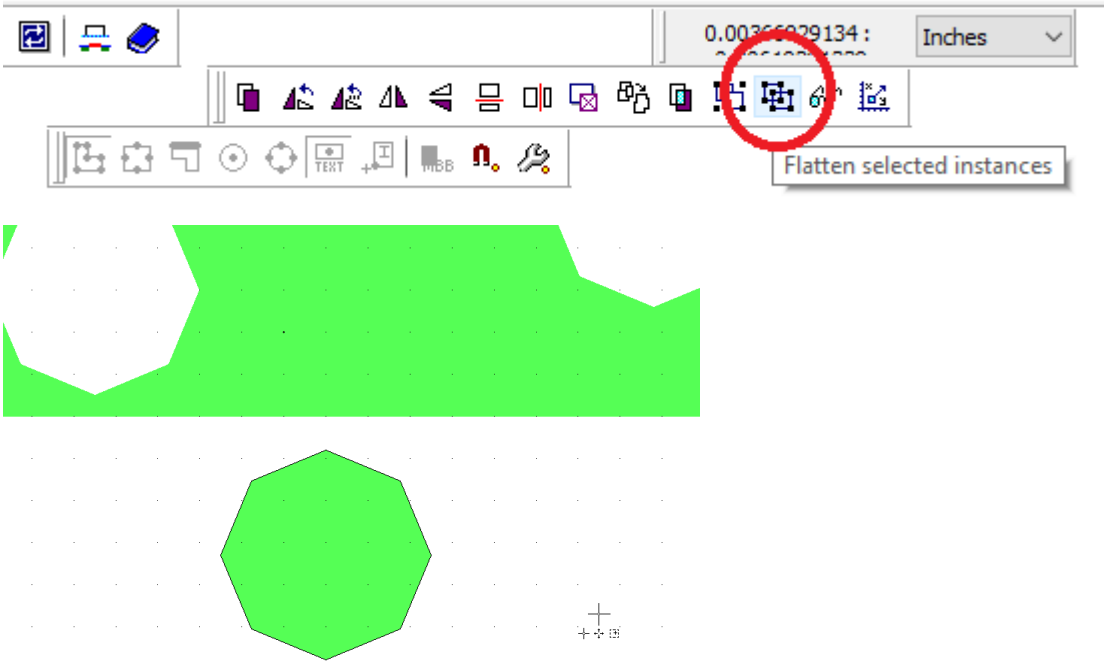
6) Repeat steps 3-5 on the other vertical side.

If any gaps or empty spaces along the vertical edges need more pillars:

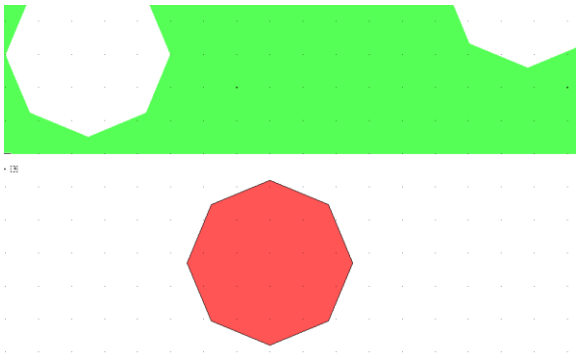
7) Import and instance the 5_MICRON.GDS file.



8) Flatten the 5 µm circle once.



9) Use **CTRL-E** to change the flattened circle from layer # 1 to layer # 2.



10) Highlight the layer # 2 circle and use **CTRL-C** to copy it.

11) Center click and hold the mouse to drag the circle where it is needed.

12) Use **CRTL-V** to add more circles.

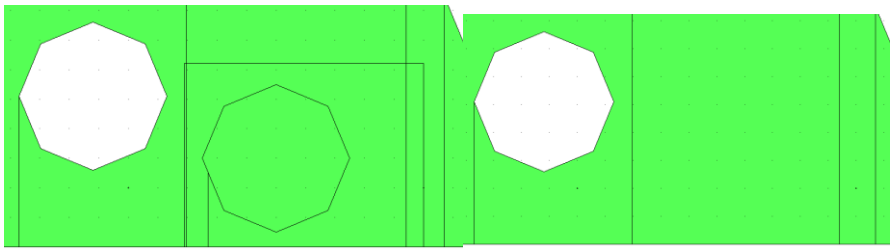
13) Repeat steps # 11 and # 12 as needed.

If any half or cutoff circles need to be covered up:

14) Click on the rectangle icon in the toolbar.

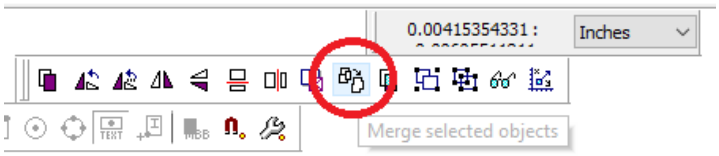
15) Click on layer # 1

16) Draw an appropriate size rectangle over the cover up area.



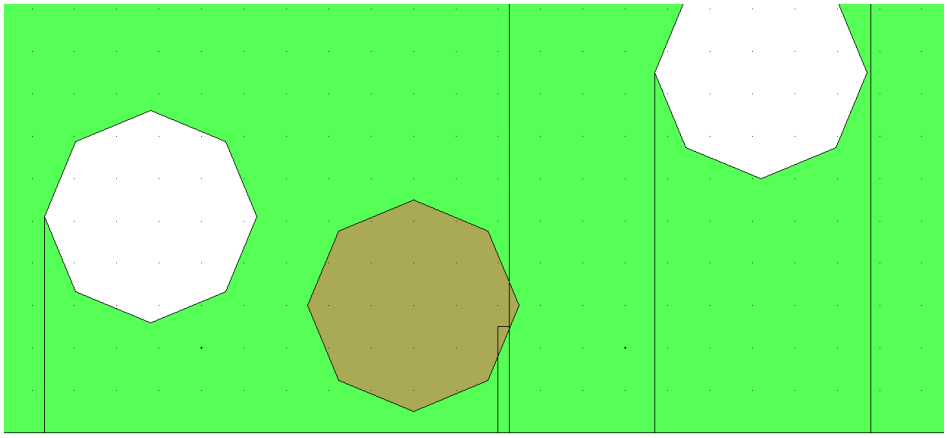
17) Hold **SHIFT** and highlight the rectangle and surrounding space.

18) Click on the merge icon in the toolbar.

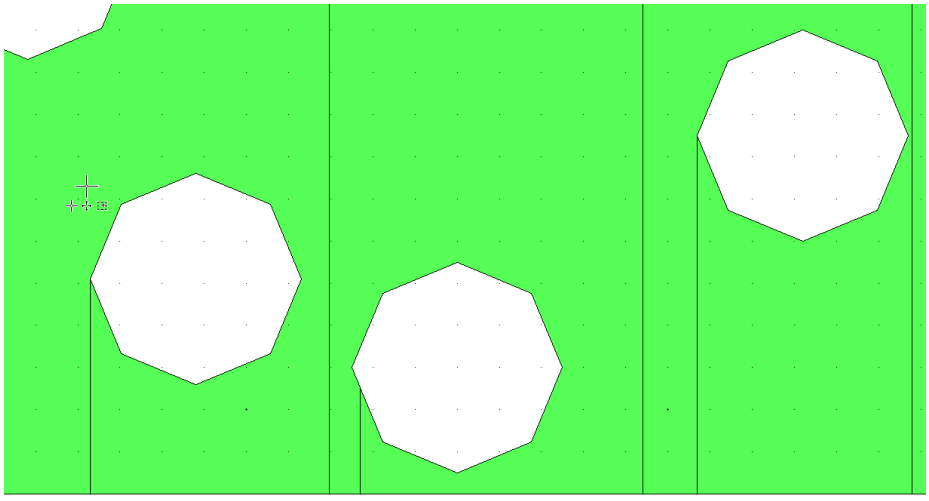


19) Repeat steps 7 through 12 if more circles are needed.

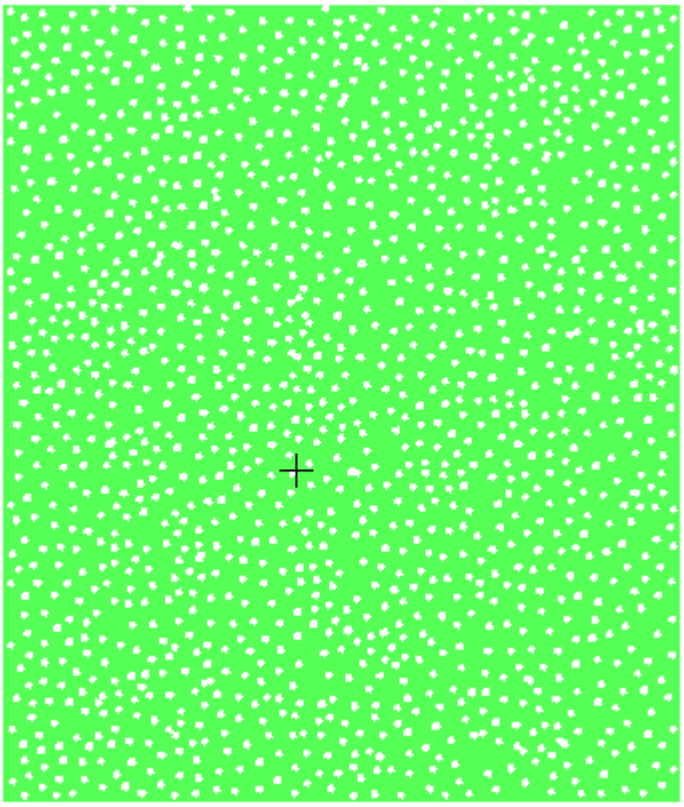
20) When all the layer # 2 circles are added. Hold **SHIFT** and highlight the circles and surrounding spaces.



21) Click on the Boolean subtraction icon to subtract the layer # 2 circles from Layer # 1 background.



22) The final design should look like this:



23) Open a new cell and instance this design. Use **CTRL-E** to create the array. A 40 x 40 array created a 0.5” x 0.5” field of pillars. An 80 x 80 grid created a 1” x 1” grid.

We used the 80 x 80 array for our test contact photomask. Ideally, ASML deep ultraviolet stepper at the CNF would have been the optimal solution if we decide in the future to expand this project. The stepper would give us the means of patterning different pillar densities, sizes and composites of different designs. On the other hand, factoring in the ease and minimal expense of contact lithography along with the fact that the 1” x 1” contact mask took less than twenty-three minutes to write, staying with the contact aligners may be the best solution.

The same 5 µm lithography and photonics/reactive-ion etch recipes for the cell migration devices were also used for this application.

1) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist. P-20 removes any dangling water bonds from the silicon surface for better photoresist adhesion.
2) **Spinning AZ nLof 2020:** Pipette ≈2 ml of nLof 2020 in the center of the wafer and spin at 3000 RPM/500/45 seconds. The resist thickness measured ≈1.7 µm.
3) **Pre-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature.
4) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer with a swab soaked in acetone.
5) **Expose of Resist:** Use the Karl Suss MA-6 contact aligner with hard vacuum contact settings. Expose the resist for 3.4 seconds for the 5µm pillar array. The hard vacuum contact settings used were pre-vacuum for 4 seconds, hard contact for 10 seconds and post-vacuum for 4 seconds. Measuring the diameter of the pillars to test if the exposure was too long. The pillars should be off the photomask measured 5µm in diameter. Longer exposure times will create smaller pillars.
6) **Post-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature. Longer bakes will distort the sidewalls of the resist (AZ® nLOF 2000, 2016).
7) **Develop the Resist:** Place the wafer in the Hammatech's four-inch wafer holder and develop with MIF 726 developer for 120 seconds.

8) **Examine the Wafer:** Developing sometimes leaves artifacts and areas of uncompleted development. If this is observed, rerun step # 5. If the lithography is still compromised, remove the photoresist with step # 12 and rerun the process starting at step # 1.

9) **Perform a De-scum:** This will remove any nanometer areas of resist that remained after development. This is done with low power oxygen plasma. There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers. This De-scum was done for this wafer using the Oxford 81's mild descum recipe for 30 seconds.

10) **RIE Etching, Season the Chamber:** On a dummy wafer, run the **NICKZOR1** or photonics etch recipe for five minutes to season the chamber. This will remove any residual DRIE polymers and contaminates that may be detrimental to the RIE etch.

11) **RIE Etching:** Load the wafer and etch with the **NICKZOR1**/photonics etch recipe for thirty-five minutes (etch rate ≈ 133 nm/minute for the cell migration devices).

12) **RIE Etching, Release:** Unload the etched wafer and reload the dummy wafer. Etch for forty minutes with the **0RELEASE** recipe (or the Photonics etch time). This will remove the photonics etch polymers and contaminates from the chamber.

13) **DRIE Etching:** Run forty loops of **0trench** to return the chamber to DRIE etching.

14) **Remove the Photoresist:** Used either the Anatech asher "O2 Stripping" recipe for 10 minutes.

15) **Deposit FOTS:** Use the Molecular Vapor Deposition (MVD) tool to deposit the anti-stiction coating fluroctatriclorosilane (FOTS).

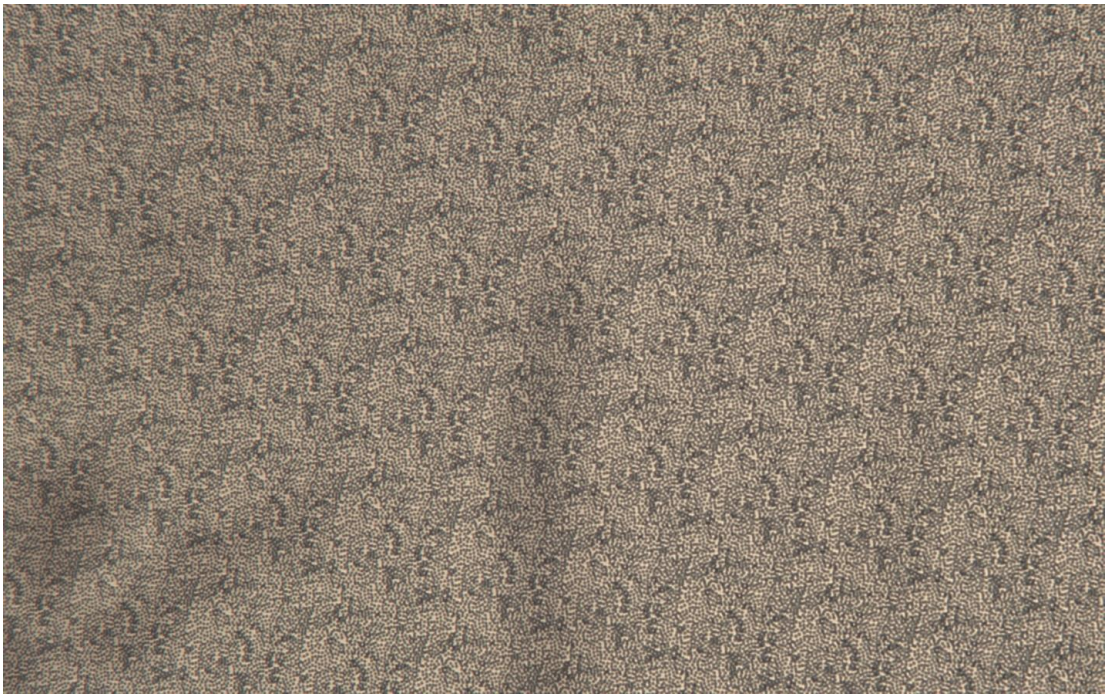


Figure J-1: Midrange array of 5 µm holes for molding PDMS pillars (2.5x).

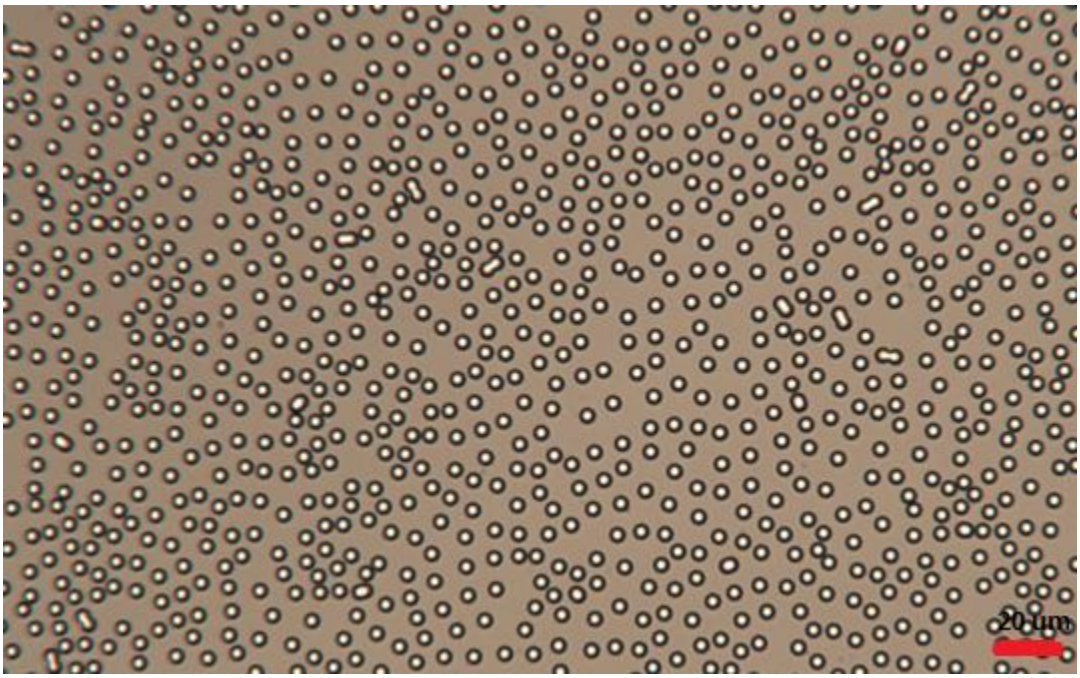


Figure 2: Midrange array of 5 µm holes for molding PDMS pillars (20x).

APPENDIX L

FABRICATING LONG TRENCHES BY DRIE

The "Muscle" sub-group of the Lammerding lab requested a PDMS mold of larger and longer channels for loading cells. The first draft of the design had twelve, 5µm channels and thirteen, 15 µm channels running 200 µm in length (Figure 1). The channels lengths were later revised to be one centimeter in length with one-hundred sixty-five, 5 µm channels and one-hundred sixty-six 15 µm channels spaced 20 µm apart in a 1 x 1 cm field (Figure 2 &3). Each wafer would have eighteen devices (Figure 4). The design was revised again to split the trench lengths on the bottom nine devices in half, creating two rows of 500 mm long trenches. Two wafers etched with trenches 18 µm and 41 µm deep were fabricated (Figure 5).

1) **Spinning P-20:** Pipette enough P-20 to cover an N-type wafer and spin with the same parameters as you would spin the photoresist in step # 2. P-20 removes any dangling water bonds from the silicon surface for better photoresist adhesion.

2) **Spinning AZ nLof 2020:** Pipette ≈2 ml of AZ nLof 2020 in the center of the wafer and spin at 3000 RPM/500/45 seconds. The resist thickness measured ≈1.7 µm.

3) **Pre-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature.

4) **Remove the Edge Bead:** Remove 5 mm of resist from the edge of the wafer with a swab soaked in acetone.

5) **Expose of Resist:** Using the ABM contact aligner, expose the resist for 2.3 seconds with Hard Contact. Measuring the diameter of the trenches to test if the exposure was not too long. Longer exposure times will create wider trenches.

6) **Post-exposure Bake:** Bake the wafer on a preheated 110^{o}C hot plate for 60 seconds and let cool to room temperature. Longer bakes will distort the sidewalls of the resist (AZ® nLOF 2000, 2016).

7) **Develop the Resist:** Place the wafer in the Hammatech's four-inch wafer holder and develop with MIF 726 developer for 120 seconds.

8) **Examine the Wafer:** Developing sometimes leaves artifacts and areas of incomplete development. It is also important to look for other lithography issues before wasting time etching. Remove poor lithography with step # 11 and reuse the wafer.

9) **Perform a De-scum:** This will remove any unseen nanometer areas of resist with a low power oxygen plasma. There are four plasma tools at the CNF that have de-scum recipes: Plasmatherm PT72, Anatech asher and both Oxford 80 RIE etchers.

10) **DRIE Etching:** If no one has ran the Unaxis 770 before this step, run 35 loops of the **0Trench** recipe on a dummy wafer to warm up the tool. The etch rate for this design was ≈460 nm/per loop, so forty loops etched 18 µm and ninety loops etched 41 µm into the silicon.

11) **Remove the Photoresist:** Used the Anatech asher "O2 Stripping" recipe for 5-10 minutes.

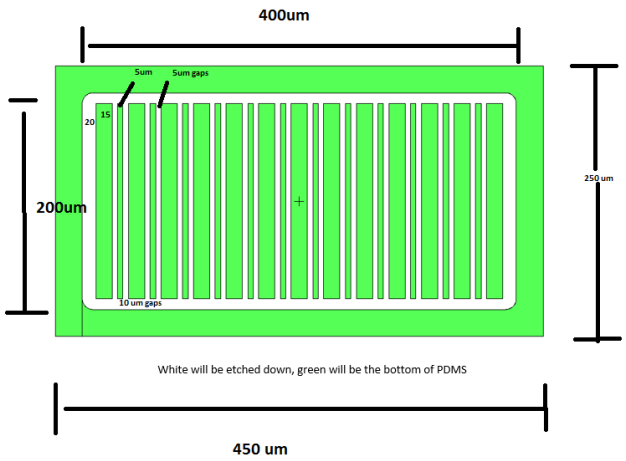


Figure L-1: First-draft of micropatterned channel design.

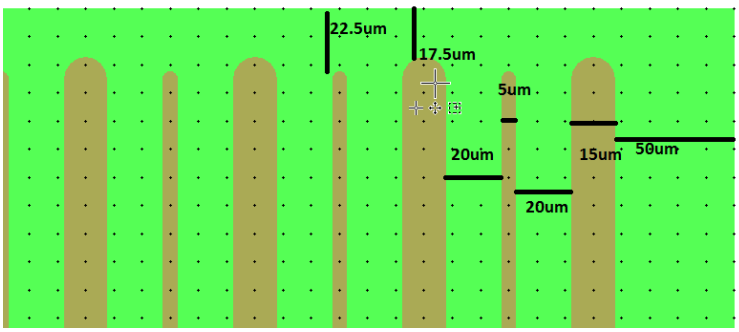


Figure L-2: Revised design with rounded ends and increased spacing between channels.

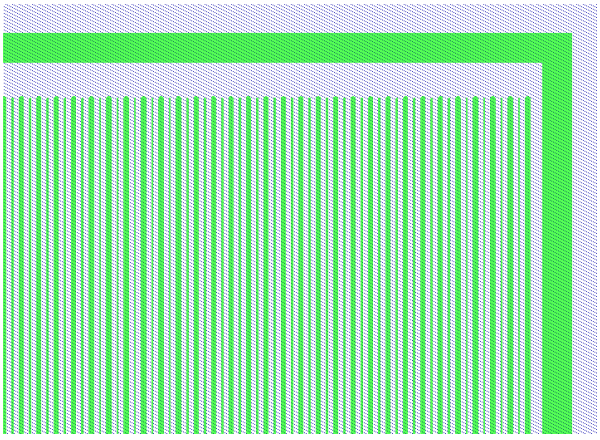


Figure L-3: A section of the 1 cm x 1 cm micropatterned groove CAD before performing the Boolean subtraction.

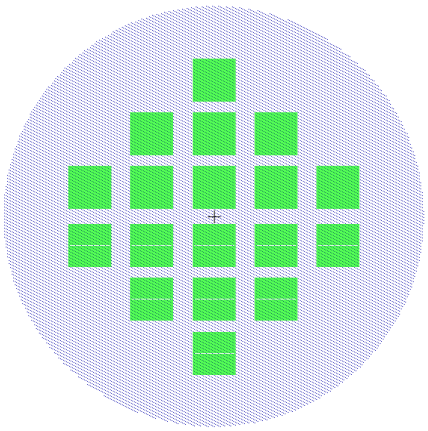


Figure L-4: The layout for the 1 cm x 1 cm channel arrays on a four inch wafer. Note the trenches for the bottom nine arrays are split in half.

Figure L-5: A section of the deep reactive-ion etched mold for PDMS casting of 1 cm long channels.

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