EXPLORING POLARIZATION DOPING IN GAN FOR POWER APPLICATIONS

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GaN has made tremendous progress in photonic and radio frequency applications, largely thanks to its wide band gap (3.4 eV), the high electron mobility (up to 2200 $cm^2/V \cdot s$) and saturation velocity ($>10^7$ cm/s). With the wide band gap and high electron mobility, GaN also possesses great potential in power applications. Unlike the traditional wide-band-gap material (SiC) used in power applications, GaN has a strong polarization effect, which enables dopant-free doping techniques that can realize two dimensional electron gas (2DEG) as well as three-dimensional (3D) bulk doping. This work focuses on exploring polarization doping for power applications.

GaN high electron mobility transistors (HEMTs), which are based on the polarization-induced 2DEG, have already been well researched for power applications. The highest reported breakdown voltage of GaN HEMTs is as high as ~3000 V. However, the performance of 2DEG based diodes are lagging behind. A GaN 2DEG based Schottky barrier diode with a record-breaking breakdown voltage of 1.9 kV is developed and described in this work. The fabrication process of this diode is fully compatible with GaN HEMT fabrication. Thus the diode can be readily integrated with GaN HEMTs.

In contrast to the polarization-induced 2DEG, the polarization-induced 3D bulk doping is rarely studied for power applications. Here we start by studying the electron mobility in polarization-doped $Al_xGa_{1-x}N$ with a low doping concentration of $\sim 1 \times 10^{17}$ cm^{-3}. The electron mobility is first experimentally extracted. Then a theoretical model of the electron mobility is built based on the experimental data. The theoretical model reveals that as the doping concentration is further reduced, it is crucial to reduce dislo-

cation density and thus its adverse effect on the electron mobility.

Both polarization-induced 2DEG and bulk doping are then applied to a GaN metal-oxide-semiconductor HEMT (MOSHEMT) with a polarization-doped p-type back barrier. This device, referred to as PolarMOSH is an integral component for the power transistor, referred to as PolarMOS. The successful demonstration of PolarMOSH paves the way towards realizing PolarMOS and eventually taking full advantage of polarization doping in power applications.

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CHAPTER 1

INTRODUCTION

1.1 Material Properties of GaN

GaN is a wide-band-gap semiconductor that has attracted intense research for decades and found its way to applications in various fields, including light emitting diodes (LEDs) [7, 8], laser diodes [9, 10] and radio frequency (RF) power circuits [11, 12, 13]. The most well known success of GaN comes from its enabling the invention of blue LEDs [14]. The key properties of GaN that leads to its indispensable role in the creation of blue LEDs are its wide band gap and direct band gap. The direct band gap allows electron-hole pairs to recombine efficiently and thus emit photons, while the wide band gap ensures that the emitted photons are within or close to the blue light spectrum. In additional to its wide band gap, GaN also has good electron transport properties, especially in the two-dimensional electron gas (2DEG) formed at the heterostructure between III-Nitride materials. In 2DEGs, the reported electron mobilities are as high as 2200 $cm^2/V \cdot s$ [15] and the saturation velocity exceeds 1×10^7 cm/s [11]. Although these values are not as high as those in narrower-gap III-V semiconductors [16], its combination with the wide band gap of GaN have enabled the high operating frequency and high power density [17, 18, 19] of GaN high electron mobility transistors (HEMTs). With a reported breakdown electric field of >4 MV/cm [20], GaN based devices can operate at a high voltage with a high power-added-efficiency. Utilizing SiC substrates with a high thermal conductivity, GaN HEMTs also greatly reduce the burden of device cooling [21, 22]. These advantages have pushed GaN devices into various high frequency application, including base stations, wireless communication and defense systems. One of the drawbacks of GaN HEMTs has been its cost [23]. Both of the commonly adopted

Table 1.1: Material properties of various semiconductors

Material Property	Si	GaAs	4H-SiC	GaN	β-Ga_2O_3	Diamond	AlN
Bandgap(eV)	1.1	1.4	3.3	3.4	4.9	5.5	6
$\mu(\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s})$	1400	8000	1000	1200	300	2000	500
E_{Cr}(MV/cm)	0.3	0.4	2.5	3.4	8.0	10	15
ε_{r}	11.8	12.9	9.7	9	10	5.5	8.5
BFOM(over Si)	1	15	340	870	3444	24664	32158

substrates for epitaxy, sapphire and SiC, have a substantially higher cost than Si. Combine the substrate cost with the additional processing cost caused by the lack of large wafers (> 4 inch in diameter), GaN has not seen its wide adoption in commercial market. However, thanks to the rapid advancement in GaN-on-Si technology [24, 25, 26], GaN HEMTs are more and more seriously being considered for commercial RF applications.

Besides its success in photonics and RF electronics applications, GaN also possesses great potential in power electronics. In Table 1.1, some key material properties of GaN is compared to traditional semiconductors and other wide-band-gap materials. In the context of power applications, the most important material properties include carrier mobility and breakdown electric field. The strength of a material's potential in power applications is often benchmarked by the Baliga's figure-of-merit (BFOM) [27], which takes both electron mobility and breakdown electric field into consideration. The BFOMs, calculated by $\varepsilon\mu_n E_{Cr}^3$, are compared in Table 1.1 [28]. The high electron mobility and breakdown field of GaN renders a BFOM value 870 times as high as that of Si and more than two times higher than that of SiC. Some more advanced wide-band-gap materials, including β-Ga_2O_3, diamond and AlN, have even higher BFOM values and will likely be the focus of future research interest beyond GaN. Another widely used method for benchmarking the potentials of semiconductors for power applications is by plotting its ideal one-dimensional on-resistance versus breakdown voltage [27], where

the on-resistance ($R_{on,sp}$) and breakdown voltage (BV) is related by:

$$R_{on,sp} = \frac{4\mathrm{BV}^2}{\varepsilon \mu_n E_\mathrm{C}^3}. \tag{1.1}$$

The calculated $R_{on,sp}$ vs BV for various semiconductors are compared in Fig. 1.1. These lines in Fig. 1.1 represents the ideal performance of a unipolar device for each material. They are often referred to as material limits and are used to benchmark device performance. From Fig. 1.1, GaN has a clear advantage over Si and GaAs in the intrinsic performance limit, while more advanced materials like AlN promises a further performance boost.

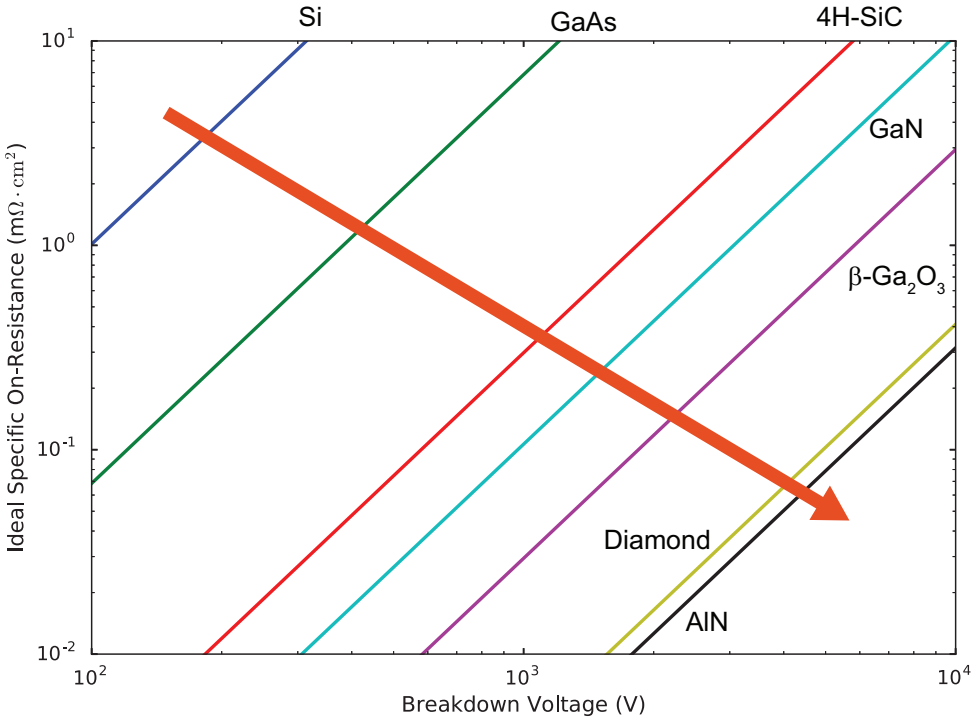

Figure 1.1: Benchmark of ideal specific on-resistance vs. breakdown voltage among various semiconductors. The calculation is based on the material properties listed in Table 1.1

Despite the great potentials of GaN in power applications illustrated in both Table 1.1 and Fig. 1.1, the development of GaN power devices have been hindered by the high dislocation densities in the epitaxial layers grown on foreign substrates. Owing to

recent improvements in epitaxy and the availability of high quality free-standing GaN substrates [29, 30, 31], much research efforts have been put into the development of GaN power devices.

1.2 Polarization Doping in III-Nitride Materials

In addition to the high electron mobility, high breakdown field and wide band gap, wurtzite GaN also exhibits a strong spontaneous polarization effect along the c-axis and piezoelectric effect, as observed in III-Nitride materials (AlN, InN and GaN) and their alloys. Although all III-V and II-VI compound semiconductors are polar materials due to the difference in ionicity of their component atoms, spontaneous polarization is only present in materials of an asymmetric crystal structure, such as wurtzite structure (Fig. 1.2 [1]). All the discussions on III-Nitride materials in this work are limited to III-Nitride materials of wurtzite structure. In relaxed wurtzite III-Nitride materials, the atom locations often deviate from the ideal wurtzite crystal structure, resulting in a dipole forming in each unit cell. As the in-plane symmetry remains intact, the direction of the formed dipole is along the c-axis. The amount the atom location deviation from the wurtzite structure of tetrahedral coordinates is measured by the ratio between the lattice constants in the [0001] (c) direction and within the c-plane (a) in comparison to the ideal ratio of $c/a = \sqrt{8/3} = 1.633$. The lattice constants, spontaneous polarization and dielectric constant of GaN, AlN and InN in wurtzite phase are listed in Table 1.2 [32]. The formation of spontaneous polarization in wurtzite GaN is illustrated as a microscopic picture in Fig. 1.3 [1].

Also listed in table 1.2 are the piezoelectric constants of III-Nitride materials. For a III-Nitride material layer subject to a small strain, the piezoelectric polarization can be

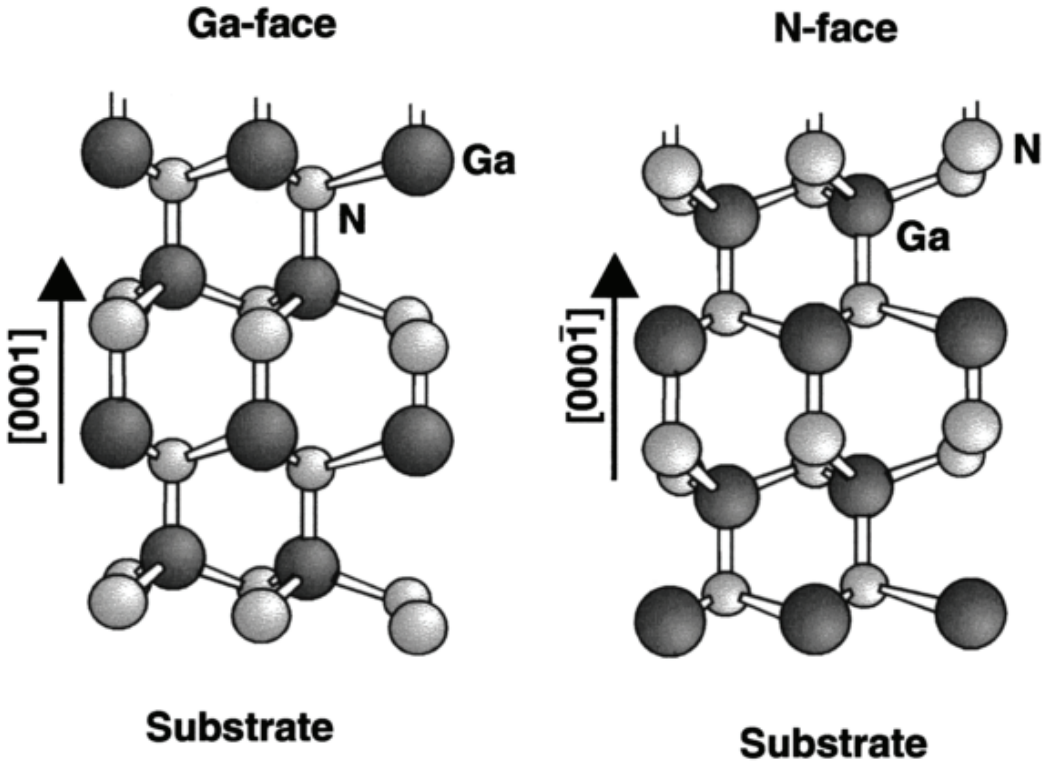

Figure 1.2: Schematic illustration of the crystal structure of wurtzite GaN in Ga-face and N-face polarity. (Reproduced from Reference [3], Ambacher *et al.* 1999)

Table 1.2: Lattice constants, spontaneous polarization, and piezoelectric of wurtzite phase GaN, AlN and InN.

Wurtzite	GaN	AlN	InN
a_0 (Å)	3.189	3.112	3.54
c_0 (Å)	5.185	4.982	5.705
u	0.376	0.380	0.377
c_0/a_0	1.627	1.601	1.612
$\Delta c_0/a_0$	-0.006	-0.032	-0.021
P_{SP} (C/m^2)	-0.029	-0.081	-0.032
e_{33} (C/m^2)	0.73	1.46	0.97
e_{31} (C/m^2)	-0.49	-0.60	-0.57

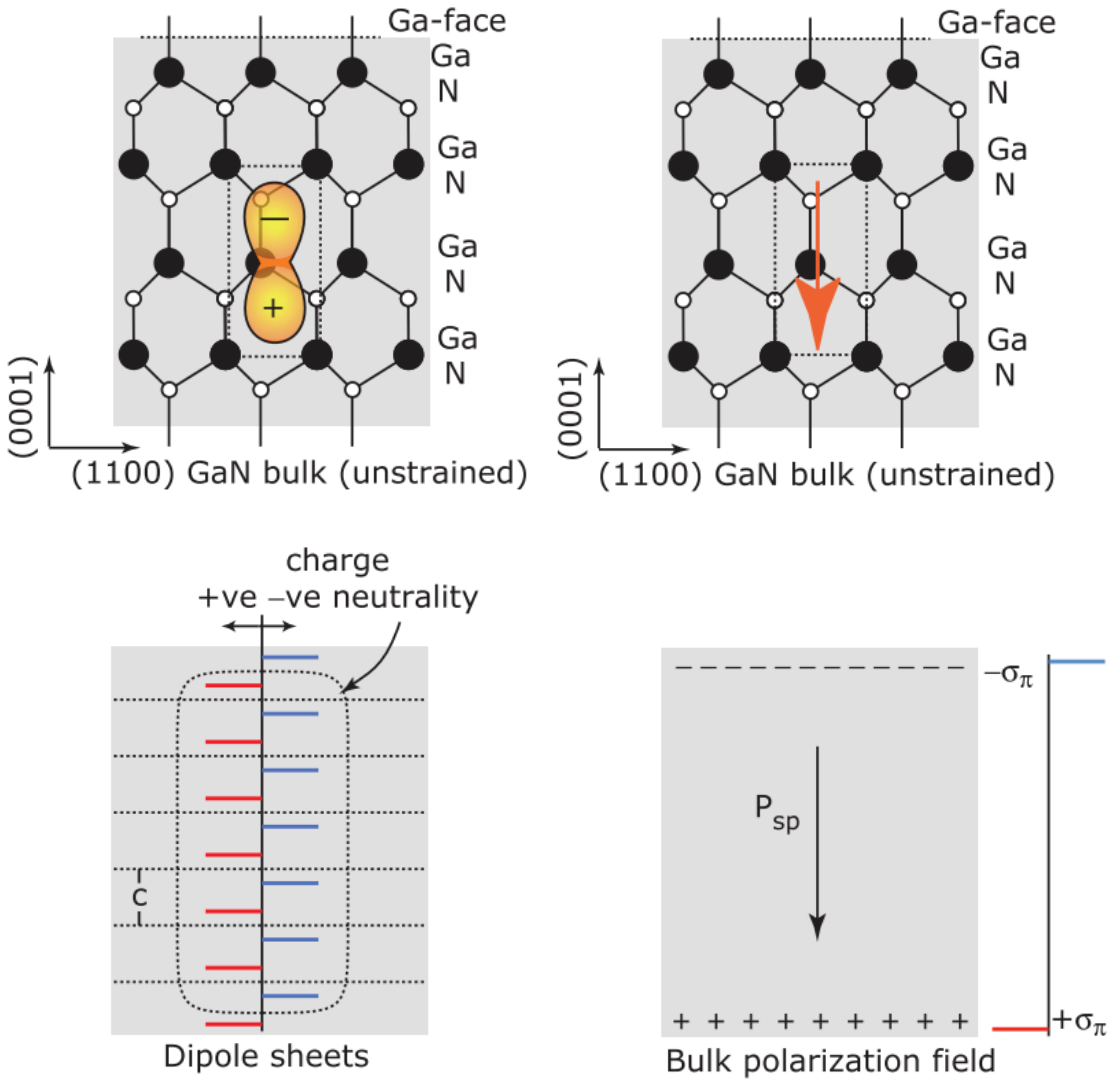

Figure 1.3: Microscopic picture of spontaneous polarization in a free-standing wurtzite GaN slab. (Reproduced from Reference [1], Wood *et al.* 2008)

expressed as [32]:

$$P_{\mathrm{PE}} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y), \tag{1.2}$$

where $\epsilon_z = (c - c_0)/c_0$ is the strain along the c axis, $\epsilon_x = \epsilon_y = (a - a_0)/a_0$ is the in-plane strain which is assumed to be isotropic, e_{33}, e_{13} are the piezoelectric constants, and a and c are the lattice constant of the strained material. For hexagonal III-Nitride materials,

the lattice constants c and a are related by the following equation:

$$\frac{c - c_0}{c_0} = -2\frac{C_{13}}{C_{33}}\frac{a - a_0}{a_0}, \tag{1.3}$$

where C_{13} and C_{33} are the elastic constants. Combining Eq. 1.2 and Eq. 1.3, the piezoelectric polarization in a material layer strained to a in-plane lattice constant of a_0 can be calculated by:

$$P_{\mathrm{PE}} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}). \tag{1.4}$$

Equation 1.4 is often used to evaluate the polarization charge in heterostructure where a thin material layer is strained to have the same in-plane lattice constant as the bulk material.

The total polarization (P_{Total}) in a III-Nitride layer is then obtained by summing the spontaneous ($P_{mathrmSP}$) and piezoelectric ($P_{mathrmPZ}$) polarization:

$$P_{\mathrm{Total}} = P_{\mathrm{SP}} + P_{\mathrm{PZ}}. \tag{1.5}$$

The crystal structure and polarization fields in AlN on GaN and InN on GaN heterostructure are illustrated in Fig. 1.4 [1]. In a AlGaN/GaN heterostructure, due to the polarization field discontinuity at the interface, an equivalent fixed sheet charge is formed at the interface and hence the formation of a two-dimensional electron gas (2DEG) in the GaN. Since the 2DEG is formed as a result of the polarization doping, with no impurity doping required, the electron mobility is not affected by impurity scattering by dopant and the 2DEG concentration is mostly free of freeze-out effect.

As GaN HEMTs have been under extensive research for more than a decade, the theoretical model for the 2DEG concentration at a GaN based heterostructure has been well studied and documented [33, 28]. The high electron concentration and mobility/velocity of 2DEGs have been key to GaN's success in RF power applications.

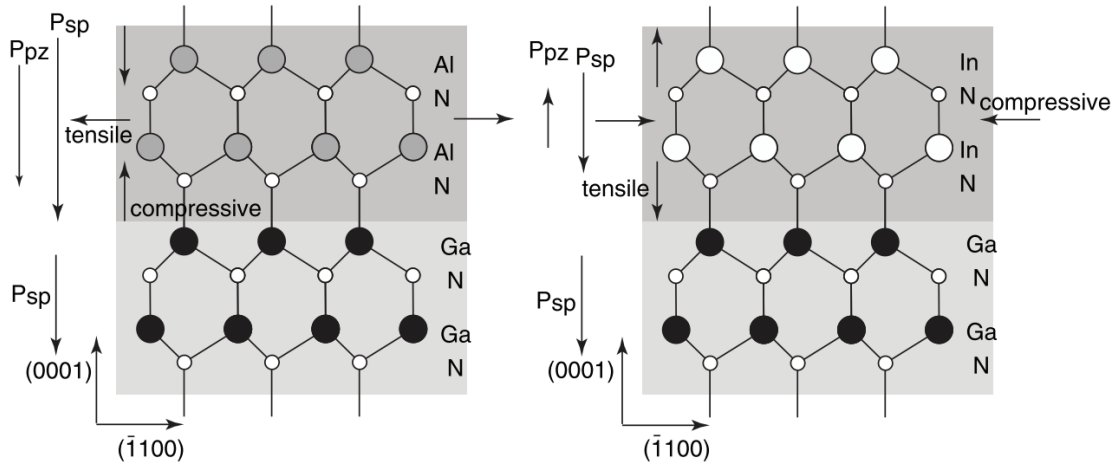

Figure 1.4: Crystal structure and polarization fields in AlN on GaN and InN on GaN materials. The GaN layer is assumed to be thick enough to relax the strain, while AlN and InN are strained to have the same in-plane lattice constant as GaN. (Reproduced from Reference [1], Wood *et al.* 2008)

Another unique property of the GaN material system is its capability of realizing bulk 3-dimensional doping purely through polarization engineering, free of impurity doping [34, 35]. Similar to the polarization-induced 2DEG, the bulk, polarization induced (Pi-induced) doping relies on the discontinuity of polarization field in the material. In 3D Pi-induced doping, the polarization discontinuity is intentionally spread across the material along the direction of the polarization field. As a consequence of this spread polarization discontinuity, fixed charge is brought into the material. The polarity and concentration profile of this fixed charge depend on the divergence of the polarization discontinuity. To satisfy Poisson equation and charge neutrality at equilibrium condition, free carriers (electrons or holes) are attracted by the fixed charge and thus the achievement of bulk doping. A $Al_xGa_{1-x}N$ layer with Pi-induced doping is used as an example to further explain the technique.

For a $Al_xGa_{1-x}N$ layer where the Al composition is linearly increased along the *c*-axis towards the Ga-face, given that the maximum Al composition is small, a mostly constant n-type doping profile can be realized as the gradient of the polarization field is

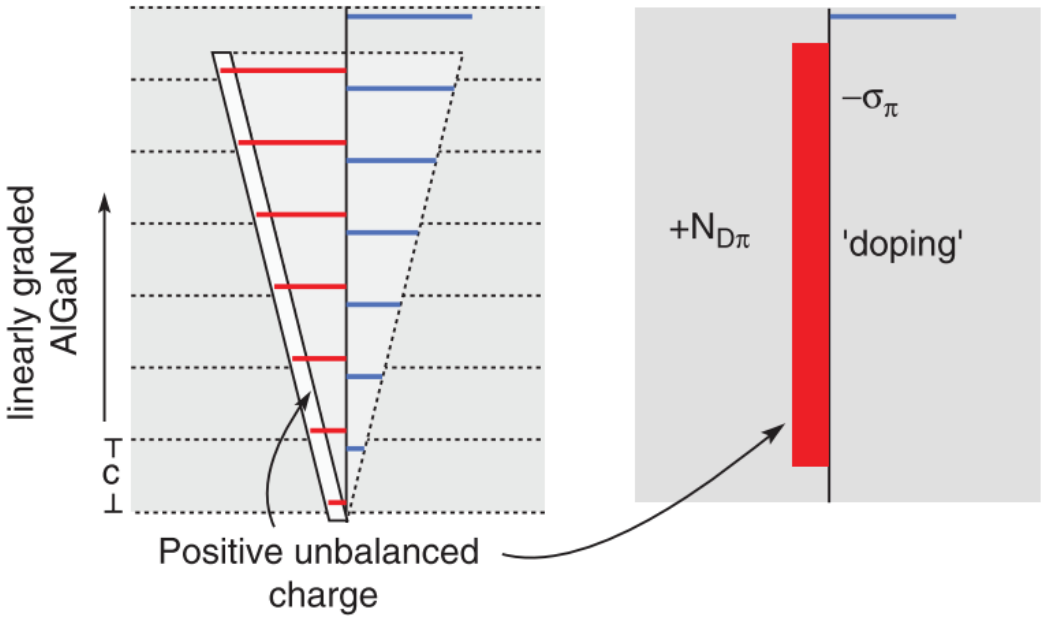

Figure 1.5: Illustration of of formation of net bulk charge in a layer by polarization grading. (Reproduced from Reference [1], Wood *et al*. 2008)

largely constant. This doping technique is illustrated in Fig. 1.5 [1]. Similar techniques can be applied to achieve p-type doping or with N-face III-Nitride materials [35].

The doping concentration of a Pi-doped $Al_xGa_{1-x}N$ layer can be calculated based on its Al composition profile [36]. Given a Ga-face $Al_xGa_{1-x}N$ layer of a thickness of z_0 and a Al composition linearly graded along the *c*-axis from 0 at its bottom to x_0 at the surface, the polarization-induced doping concentration is

$$\rho_\pi = \frac{\partial P[x(z)]}{\partial z}, \tag{1.6}$$

where $P[x(z)]$ is the polarization at the depth z. As the polarization (in cm^{-2}) of $Al_xGa_{1-x}N$ coherently strained on GaN is

$$P[x] = [2x + 1.1875x^2 + 3.25x] \times 10^{13}. \tag{1.7}$$

The doping profile in the $Al_xGa_{1-x}N$ is then given (in cm^{-3}) by [37]:

$$\rho_\pi(z) = \frac{x_0}{z_0}(5.25 + 2.375x_0\frac{z}{z_0}) \times 10^{21}, \tag{1.8}$$

where z and z_0 are expressed in Å. Notice that even for a perfectly linear Al composition grading, the Pi-induced doping concentration ρ_π is not independent of the depth z. However, when $x_0 \ll 5.25/2.375 \approx 2.2$, the z dependence is negligible and the doping concentration is largely constant. Another feature observed from Eq. 1.8 is that the Pi-induced doping concentration can be tuned by the maximum Al composition $x0$ and the layer thickness z_0. This is important as different applications require materials of different doping concentration ranges.

1.3 Polarization Doping in GaN for Power Applications

The 2DEG in GaN heterostructures have been heavily exploited for RF applications [38, 39], where its high electron mobility and saturation velocity, in combination with the high breakdown electric field, has enabled tremendous improvements in the RF power density and efficiency over their GaAs based counterparts. Enormous efforts have also been put into utilizing the GaN 2DEG for power applications, yielding serious advancements in the power performance of GaN devices, especially for GaN HEMTs and MOSHEMTS [40, 41]. Fig. 1.6 [40] shows the benchmark of the performance of reported GaN HEMTs, SiC MOSFETs and GaN vertical devices. GaN HEMTs with breakdown voltages exceeding 2000 V [42, 43] have been reported, with a much lower on-resistance compared to the SiC MOSFETs of a similar breakdown voltage.

Although GaN 2DEG has clearly shown its potential in power applications through the state-of-the-art power performance of the power HEMTs, the development of GaN 2DEG based diodes has been lagging behind, with a maximum breakdown voltage around 1.6 kV [44, 45] and often accompanied by a large reverse leakage current. For GaN HEMT to be a true platform for power applications, it is vital to realize a matching

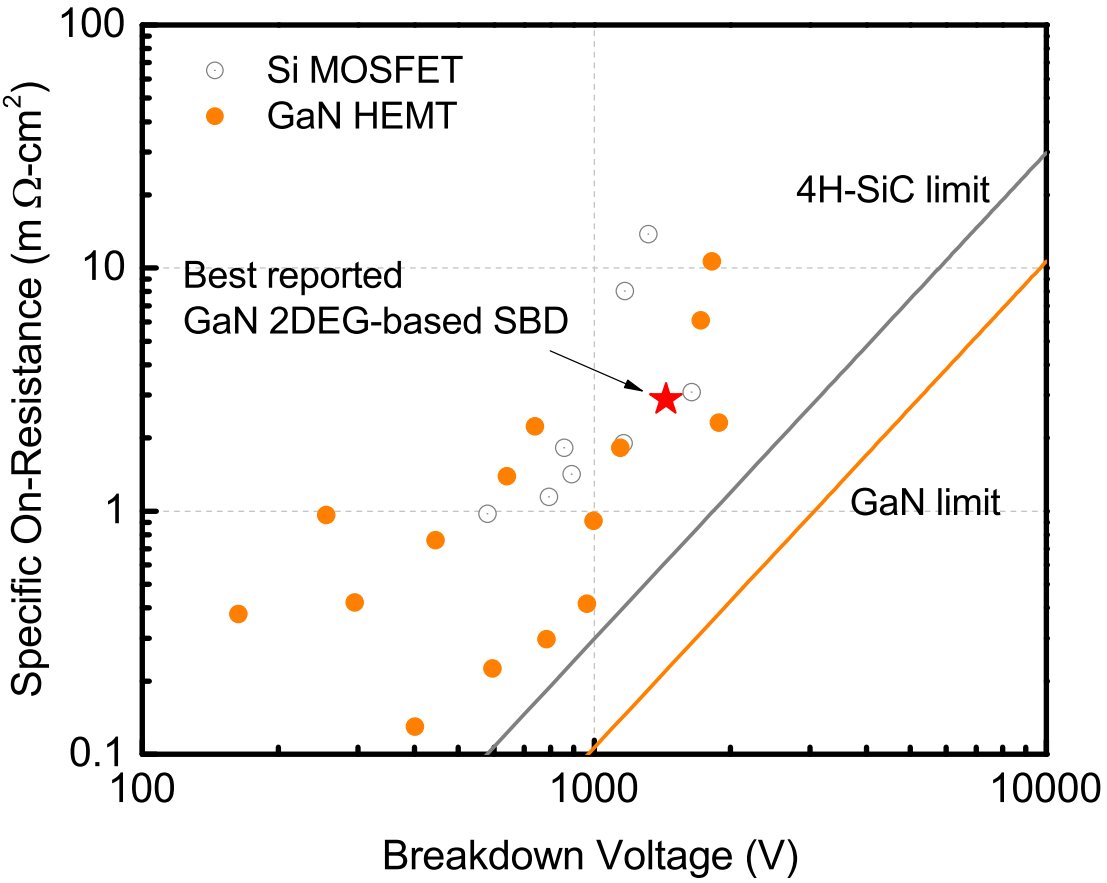

Figure 1.6: Benchmark of the performance of reported SiC and GaN power transistors. The theoretical performance limits for various materials and device types are also plotted.

diode performance. The lagging diode performance is largely due to the high dislocation density associated with GaN materials grown on foreign substrates, causing a large reverse leakage current and a early device breakdown [46]. While GaN HEMTs with Schottky gate suffer from the same problems caused by the high dislocation density, they can be largely avoided by introducing the metal-insulator-semiconductor (MIS) gate [47, 33]. The gate dielectric in the MIS gate passivates the leakage paths caused by the dislocations, greatly reduces the leakage and hence the leakage-related early breakdown problem. For GaN 2DEG based diodes (mostly Schottky barrier diodes), however, introducing a MIS structure would also block the forward conduction of the device. In

this work, the development of a lateral AlGaN/GaN Schottky barrier diode, featuring a record breaking breakdown voltage of 1.9 kV, is described. This state-of-the-art diode performance is achieved through careful device design and fabrication process optimization.

In comparison to the polarization-induced 2DEG in GaN, the Pi-induced bulk doping had not been researched for power applications until Xing's proposal on PolarMOS [2]. This is in part due to challenges in growing $Al_xGa_{1-x}N$ layers with a low Pi-induced doping concentration. Earlier studies focused on growth of $Al_xGa_{1-x}N$ materials of a high doping concentration ($>1 \times 10^{18}$ cm^{-3}) [48, 49, 50], where the total thickness of the Pi-doped layer is within 100 nm. Although such materials is suitable for RF applications and has been utilized to show good RF performance [49] in GaN metal-semiconductor field effect transistors (MESFETs), they are of too high a doping concentration to be used in power applications. In power applications, a doping concentration $<1 \times 10^{17}$ cm^{-3} [2, 51] in the drift region is required to achieve a high breakdown voltage.

Thanks to the progress made in GaN epitaxy and the availability of high quality free-standing GaN substrates [52, 53, 54], Pi-induced doping can now be applied to a much lower concentration ($<1 \times 10^{17}$ cm^{-3}), making it possibly a viable option for power applications. However, more research is needed to understand the advantages and disadvantages of Pi-induced doping at low doping concentrations. To compare Pi-induced doping to the traditional impurity doping in the context of power applications, one must study the electron mobility in Pi-doped materials at doping concentrations $<1 \times 10^{17}$ cm^{-3}. In this study, the electron mobility in Pi-doped $Al_xGa_{1-x}N$ with a doping concentrations $\sim 1 \times 10^{17}$ cm^{-3} is obtained by experiments and compared to its impurity-doped counterpart. A theoretical model for electron mobility in Pi-doped $Al_xGa_{1-x}N$ and impurity-doped GaN is then developed based on the experimental data.

The development of a novel transistor utilizing the Pi-induced bulk doping is also described in this study. This transistor, referred to as PolarMOSH, is a GaN MOSHEMT with a Pi-doped p-type $Al_xGa_{1-x}N$ back barrier. It is an integral component of the vertical power transistor referred to as PolarMOS [2], which takes advantage of both n-type and p-type Pi-induced doping to achieve high power performance. The demonstration of PolarMOSH presented in this work paves the way to the realization of PolarMOS and hence eventually taking Pi-induced bulk doping into power applications.

1.4 Outline of This Work

In this work, polarization-induced doping including 2DEG and bulk doping are studied in the context of power applications.

In chapter 2, the focus is on developing a GaN 2DEG based Schottky barrier diodes with a breakdown voltage that matches that of GaN power HEMTs and thus make GaN 2DEG a more viable platform for power applications. Through careful device design and fabrication process optimization, a lateral AlGaN/GaN Schottky barrier diode with a breakdown voltage of 1.9 kV is achieved, representing a record breakdown voltage among GaN SBDs at the time of reporting. The development process and device characterization are described in detail. And the device performance is benchmarked among other Schottky barrier diodes reported in the literature to highlight the advancement brought by the device presented in this work.

In chapter 3, the Pi-induced n-type doping at a concentration $\sim 1 \times 10^{17}$ cm^{-3} is experimentally demonstrated. This is the lowest Pi-induced doping concentration at the time of reporting and signals the advancement of Pi-induce bulk doping towards power applications. The electron mobility in this Pi-doped GaN is then characterized

through a combination of *I-V* and *C-V* measurement. Based on this experimental data, a theoretical model for electron mobility in Pi-doped $Al_xGa_{1-x}N$ and impurity-doped GaN is developed. This theoretical model provides insights regarding the optimal application scenarios for Pi-induced bulk doping and impurity doping in GaN. This model also reveals the direction to be taken to further improve the electron mobility in Pi-doped $Al_xGa_{1-x}N$ as the doping concentration is reduced below 1×10^{17} cm^{-3}.

In chapter 4, the development process of a GaN MOSHEMT with Pi-doped p-$Al_xGa_{1-x}N$ back barrier, referred to as PolarMOSH, is described. This PolarMOSH is an integral component of the GaN vertical power transistor referred to as PolarMOS. As PolarMOS takes advantage of both n-type and p-type Pi-induced Pi-doping to achieve high power performance, the demonstration of PolarMOSH in this work shows the advancement towards achieving PolarMOS and eventually materializing the potentials of P-induced bulk doping in power applications.

In chapter 5, conclusions of this work are drawn and future work is suggested.

CHAPTER 2

DEVELOPMENT OF HIGH VOLTAGE LATERAL AlGaN/GaN SCHOTTKY BARRIER DIODES

2.1 Introduction

Diode based rectifiers is an indispensable element in electronic circuit design. The operation of a rectifier includes three conditions: forward bias, reverse bias and switching in-between. In the context of high voltage, high power applications, the performance of a rectifier is benchmarked by its forward current capability, reverse-voltage blocking capability and power loss during operation.

The forward current capability is the maximum current the device can handle under forward bias. This maximum current scales with device size (anode area for vertical diodes and anode width for lateral diodes) and forward bias voltage. As the small device footprint is desired for system miniaturization and cost reduction, the forward current capabilities of rectifiers are compared in current density rather than the absolute current. A rectifier typically has a linear current-voltage characteristics when the forward bias voltage is larger than its turn-on voltage, which can be characterized by its differential resistance. Although in theory, the forward current can always be increased by increasing the forward bias voltage, it is often the generated heat due to power loss that limits its maximum forward current. The excessive heat generated increases the device temperature and hence the device resistance. In continuous operations, the power loss of the rectifier should not exceed the power dissipation capability of the cooling system to prevent build up of heat and eventual thermal runaway. The generated heat under forward bias has two contributors: the existence of a barrier (characterized by the turn-on voltage) and the on-resistance (characterized by the differential resistance). Thus to achieve

a high forward current, it is important to minimize the turn-on voltage and on-resistance.

The reverse-voltage blocking capability of a rectifier is characterized by its breakdown voltage under reverse bias. The breakdown voltage of a diode is often defined as the reverse bias voltage at which the reverse current exceeds a certain current density. The reverse breakdown voltage characterized the diode's capability in operating under high voltages.

AlGaN/GaN based Schottky barrier diodes have shown great performances in terms of breakdown voltage [55]. However, they are still not up to the level of GaN HEMTs' [40, 42]. This is due to the high leakage current through the metal-AlGaN/GaN Schottky junction causing an early breakdown. Numerous studies have linked this leakage current with surface defects [56, 57], bulk defects [58, 59] and the dislocations in the epitaxial AlGaN/GaN [60, 61]. While this leakage current through the metal-AlGaN/GaN Schottky junction is effectively curbed in power HEMTs by employing metal-insulator-semiconductor (MIS) gate structure [62, 33, 63, 64], the solution is more complicated for AlGaN/GaN SBDs as MIS structure would affect the forward conduction capability of SBDs. To make GaN power HEMTs a truly competitive platform for power electronics, AlGaN/GaN based diodes with fully compatible fabrication process and matching breakdown voltages are required. In this chapter, the development of a high voltage, lateral AlGaN/GaN Schottky barrier diode is described in detail.

2.2 Planar AlGaN/GaN SBDs vs. Recessed AlGaN/GaN SBDs

Traditionally, to make a SBD on a AlGaN/GaN epitaxial wafer grown for HEMTs fabrication, anode metal with large work function (Ni, Pt or Pd) is deposited directly on the wafer surface. The fabrication process is identical to the HEMT fabrication process,

thus these SBDs can be easily integrated with HEMT fabrication. In these conventional SBDs, the metal-semiconductor junction is then formed between the deposited metal and AlGaN on the surface. The Schottky barrier height is then determined by the metal work function and the electron affinity of AlGaN. The cross-section schematic and the electron energy band diagram at the Schottky junction of planar AlGaN/GaN SBDs is illustrated in Fig. 2.1(a). As the electron affinity of AlGaN decreases with increasing Al composition, with the same metal, the Schottky barrier height of metal/AlGaN is larger than that of metal/GaN. For the typical Al composition of 20 $\sim$ 30% in epitaxial layers for HEMT fabrication, the Schottky barrier height is $\sim$ 1.3 V, which is already undesirably larger than the turn-on voltage of a Si p-n diode. It is also worth pointing out that, unlike a regular Schottky junction where the metal is in direct contact with the conducting semiconductor, the metal and the conducting two-dimensional electron gas is separated by the semi-insulating AlGaN. This separation requires electrons to transport through the AlGaN under both forward and reverse bias condition. Since AlGaN is susceptible to the generation of defects during its epitaxial growth, more defect related conduction (defect-assisted tunneling [59, 65, 66] and Poole-Frenkel conduction [67, 68, 60]) are involved in under both forward and reverse bias.

Based on the fabrication process of the conventional AlGaN/GaN SBDs, a recessed AlGaN/GaN SBD can be readily fabricated with one extra dry etching process before the anode metal deposition. The cross-section schematics and electron energy band diagram is illustrated in Fig. 2.1(b). Compared to conventional SBDs, the Schottky barrier height is smaller, as it is determined by the electron affinity of GaN rather than AlGaN. The metal in a recessed AlGaN/GaN SBD is in direct contact with the two-dimensional electron gas, rather than indirect contact with AlGaN separation. Thus a recessed AlGaN/GaN SBD is expected to have superior forward bias characteristics to those of conventional AlGaN/GaN SBDs. The reverse bias characteristics of the

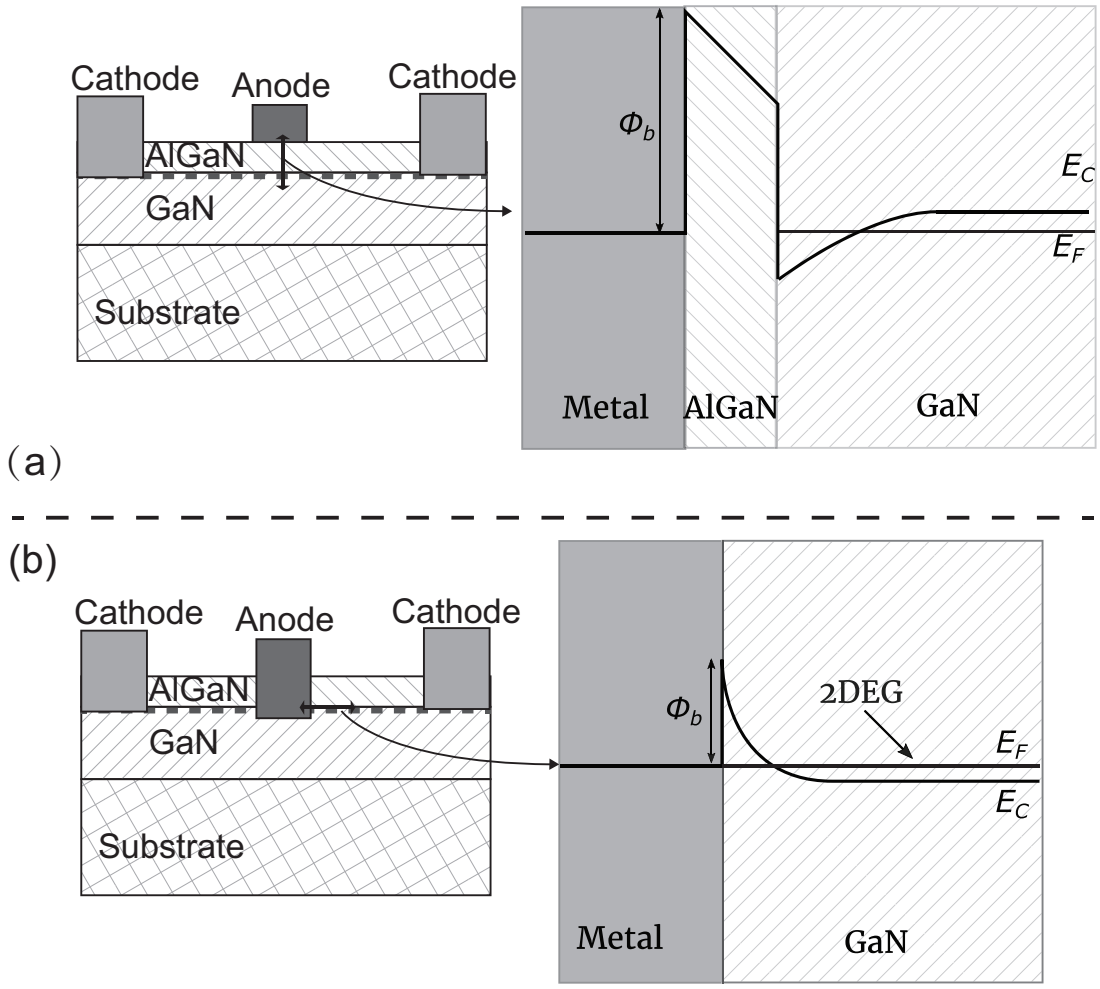

Figure 2.1: Illustration of the cross-section schematics (left) and electron energy band diagram at the Schottky junction (right) of planar (a) and recessed (b) AlGaN/GaN SBDs.

recessed AlGaN/GaN SBDs is susceptible to leakage current increase as the local 3-D effective doping concentration within the 2DEG is quite high ($> 10^{19}$ cm^{-3}).

To experimentally compare the DC characteristics of conventional and recessed AlGaN/GaN SBDs, they are fabricated on the same sample with epitaxial layers grown for HEMT fabrication. The epitaxial layers are grown by Metal-Organic Chemical Vapor Deposition along metal-face (c plane) on a sapphire substrate. The growth started with buffer layer, followed by UID GaN, 19 nm $Al_{0.19}GaN$ and 3 nm GaN. Hall effect measurement of the as-grown wafer shows that the 2DEG at the AlGaN/GaN interface has

an electron density of 9.6×10^{12} cm^{-2} and an electron mobility of 1400 $cm^2/V\cdot s$, resulting in a sheet resistance of 465 Ω/square.The fabrication process is commenced with ohmic contact formation through metal alloying. The sample is patterned through photolithography and a metal stack consisting of 20/100/40/40 nm Ti/Al/Ni/Au is deposited and then annealed at 890 °C for 18 s. All the SBDs are designed in a circular layout, making them self-isolated. A dry etching process is nevertheless carried out to isolate the test structures (TLM and van der Pauw patterns) fabricated along with the SBDs. The dry etching is based on Cl_2 and performed in a reactive ion etching (RIE) system. The anodes are then patterned and the recess is realized through Cl_2 based dry etching by an inductively coupled plasma (ICP) etching system. The ICP etching instead of RIE is used to reduce the amount of physical bombardment and hence damage to the material during the etching process. The anode recess etch depth is measured by profilometer to be 50 nm, which is larger than the total thickness of the top barriers, ensuring that the subsequently deposited anode metal will be in direct contact with the 2DEG through the etched sidewall. During the anode recess etching process, the conventional SBDs are protected by photoresist. A gate metal stack consisting of 200/40 nm Ni/Au is then deposited as anode metal for both conventional and recessed SBDs.

The current-voltage characteristics of the fabricated SBDs are measured by Keithley 4200 Semiconductor Characterization system (4200-SCS). The comparison of the forward bias characteristics of the fabricated planar and recessed AlGaN/GaN SBDs is plotted in Fig. 2.2. In the linear scale plot of Fig. 2.2, the turn-on voltage of the recessed SBD, extracted through linear extrapolation, is around 0.5 V while it is 1.3 V for the planar SBD - a 61% reduction. This observation is consistent with previous reports, where a reduction in turn-on voltage is also observed with partial or complete top barrier removal at the anode of SBDs. The differential on-resistance R_{ON} for both SBDs are calculated and plotted in Fig. 2.2(a). The two types of SBDs have similar

R_{ON} value when the forward bias voltage is larger than their turn-on voltages, which is expected since the current-voltage characteristics is determined by the series resistance. In this case, the series resistance include the contact resistance of the cathode and the resistance of the 2DEG between the anode and cathode. In the semi-logarithmic plot shown in Fig. 2.2(b), an obvious difference between the planar and recessed SBDs is seen when the bias voltage is below the turn-on voltages. While the *I*-*V* curve recessed SBD shows a linear behavior before the increased current level makes the effect of series resistance more significant, the *I*-*V* of the recessed SBD shows a large deviation from the expected linear behavior. This difference is also reflected in the calculated ideality factor. To calculate the ideality factor, the measured anode current is modeled by the following equation,

$$I = I_0 e^{\frac{qV_F}{nkT}}. \tag{2.1}$$

I is the measured anode current, I_0 is the saturation current, V_F is the applied forward bias voltage, n is the ideality factor, k is the Boltzmann constant and T is the temperature. Thus the ideality factor as a function of forward bias voltage can be written as

$$n(V_F) = \frac{q}{kT\frac{dln(I)}{dV_F}}. \tag{2.2}$$

For an ideal Schottky barrier diode with not leakage path or recombination current under forward bias, the ideality factor is 1. The more leakage and recombination current there is, the larger the ideality factor gets. A fluctuation in values between 1 and 4.5 in the calculated ideality factor can be seen for the planar SBD, indicating the existence of trap-assisted tunneling. On the contrary, the calculated ideality factor for the recessed SBD shows no fluctuation as it gradually increases as the current level increase and stays between 1 and 3 before the turn-on voltage. The fitted ideality factor is calculated to be 1.67 for the recessed SBD. The closer to 1 ideality factor of the recessed SBD compared

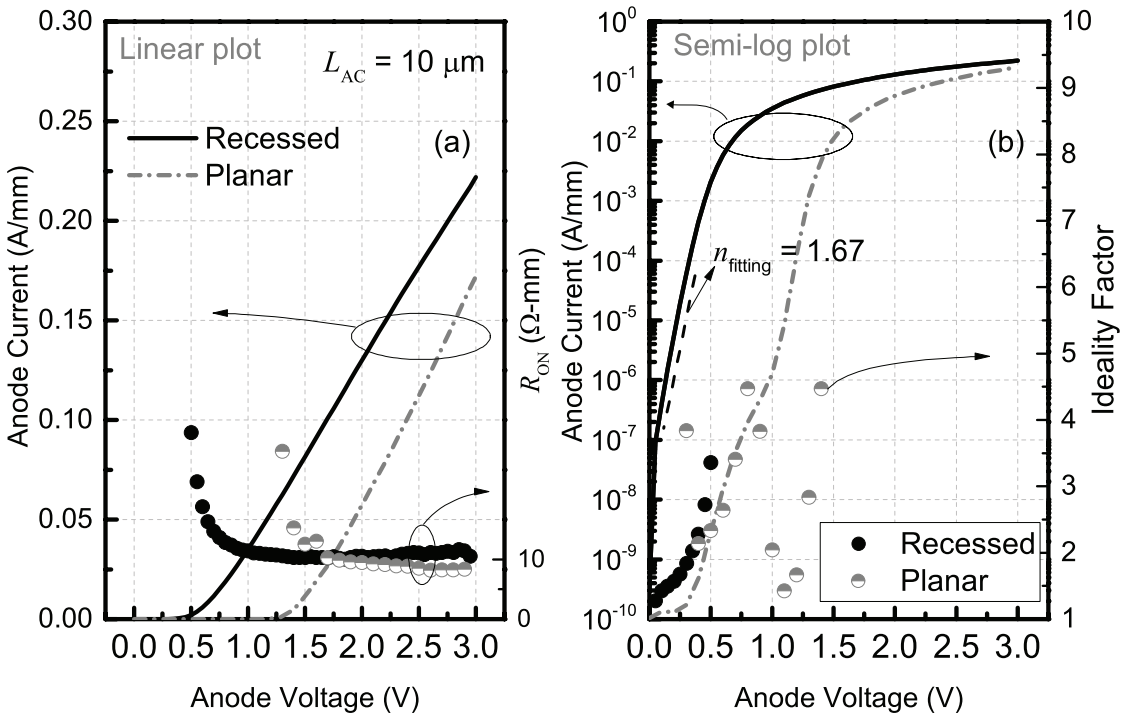

Figure 2.2: Comparison of the forward bias characteristics of fabricated planar and recessed SBDs (No field plate). The current-voltage characteristics are plotted in linear scale (a) and semi-logarithmic scale (b). The differential on-resistance and ideality factors are calculated and plotted. Both devices have an anode-cathode separation of 10 μm.

to the planar SBD shows a reduction in non-ideal current transport by making the direct contact between the anode metal and the 2DEG. The comparison of forward bias characteristics shows that the recessed AlGaN/GaN SBDs indeed have munch improved performance in turn-on voltage and ideality factor.

The comparison of the reverse bias characteristics of the fabricated planar and recessed SBDs is plotted in Fig. 2.3 along with the buffer leakage current. The buffer leakage current is measured between a pair of ohmic contact pads isolated by the aforementioned dry etching process. The separation distance between these two pads is 10 μm. The measured buffer leakage current is at least 100X smaller than either the planar and recessed SBDs. This shows that the buffer leakage current has negligible effects on the reverse bias characteristics of the fabricated SBDs.

Both planar and recessed SBD show a reverse leakage saturation when the reverse bias voltage is larger than 30 V. The saturated reverse current of the recessed SBDs is higher than that of the planar SBDs. The increase of reverse leakage current is not surprising and often seen as the Schottky barrier height is reduced in a regular SBD, due to increased amount of electrons available for thermionic or field emission. However, the reverse leakage current of the recessed SBDs is as high as 0.1 mA/mm, which is very close to the often adopted breakdown criteria of leakage current level of 1 mA/mm. This high leakage current inhibits the development of recessed SBDs with high reverse breakdown voltage and is to be addressed in the next section.

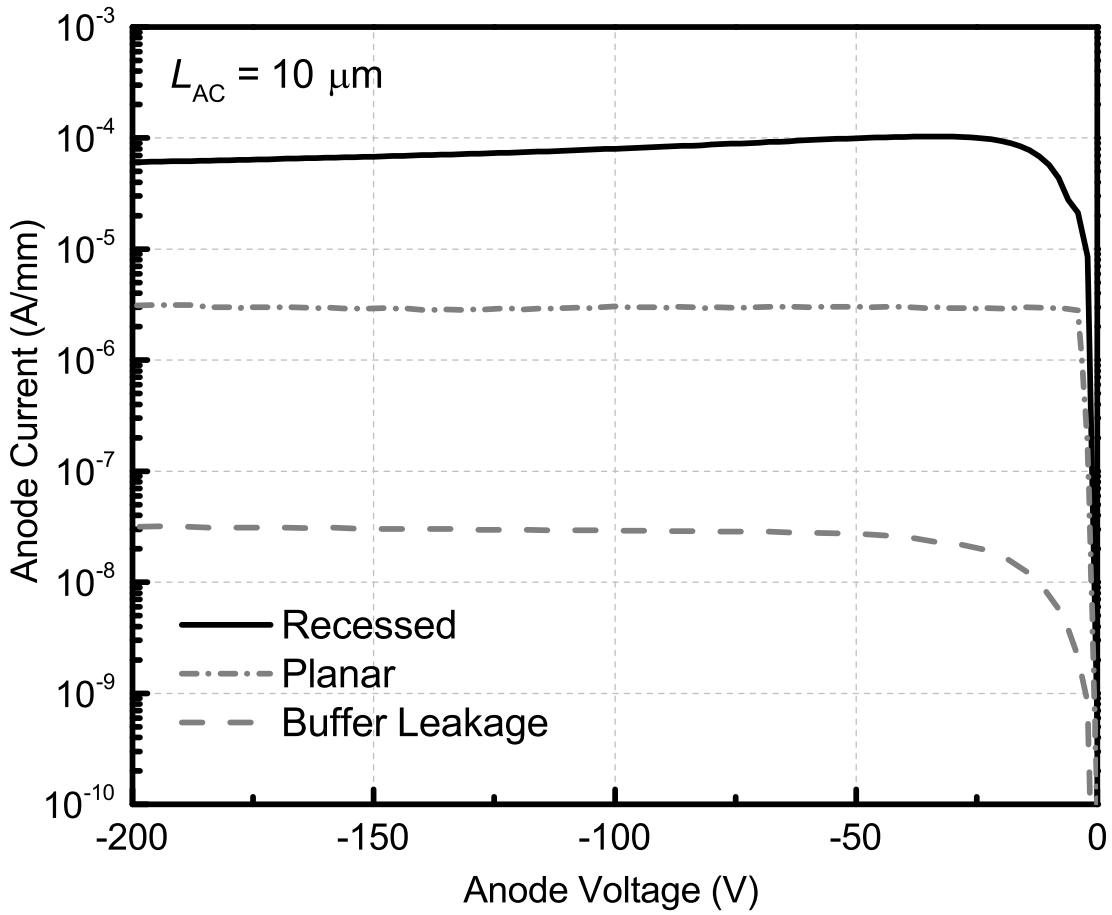

Figure 2.3: Comparison of the reverse bias characteristics of fabricated planar and recessed SBDs (No field plate). The buffer leakage current, measured on a pair of mesa-isolated ohmic contacts separated by a distance of 10 μm, is also plotted for comparison.

2.3 Recessed AlGaN/GaN SBDs with Field Plate

To address the reverse leakage current issue in the recessed SBDs described in the previous section, a new device structure is designed to combine the merits of both planar and recessed SBDs. The device cross-section schematic is shown in Fig. 2.4. The revised AlGaN/GaN SBD design features a recessed anode as well as a planar anode as field plate (FP). This recessed AlGaN/GaN SBD with FP is equivalent to a planar SBD and a recessed SBD in parallel connection.

Under an increasing forward bias voltage, the recessed SBD within the recessed SBD with FP is expected to turn on before the planar SBD as the recessed SBD has a much smaller turn-on voltage. So the turn-on voltage of the recessed SBDs with FP is only determined by the recessed SBD. When the recessed SBD with FP is under an increasing reverse bias voltage, the field plate gradually depletes the 2DEG underneath it. When the reverse bias voltage is larger than the pinch-off voltage of the planar SBD, the 2DEG underneath the FP is completely depleted, shielding the recessed SBD from further increase of bias voltage. The reverse bias characteristics of the recessed AlGaN/GaN SBDs is determined by the planar AlGaN/GaN SBD. Therefore, the recessed AlGaN/GaN SBDs are expected to have the reverse bias characteristics of the planar SBDs while retaining the forward bias characteristics of the recessed SBDs, effectively combining the merits of two types of SBDs.

The fabrication process for the recessed AlGaN/GaN SBDs is based on the recessed SBDs. The fabrication process is started with patterning the field plates by photolithography on the recessed SBDs. A metal stack of 40/100 nm Ni/Au is then deposited by E-beam evaporation, followed by lift-off process to remove the photoresist. Note that the anode is realized with two metal depositions to strictly study the effects of the field

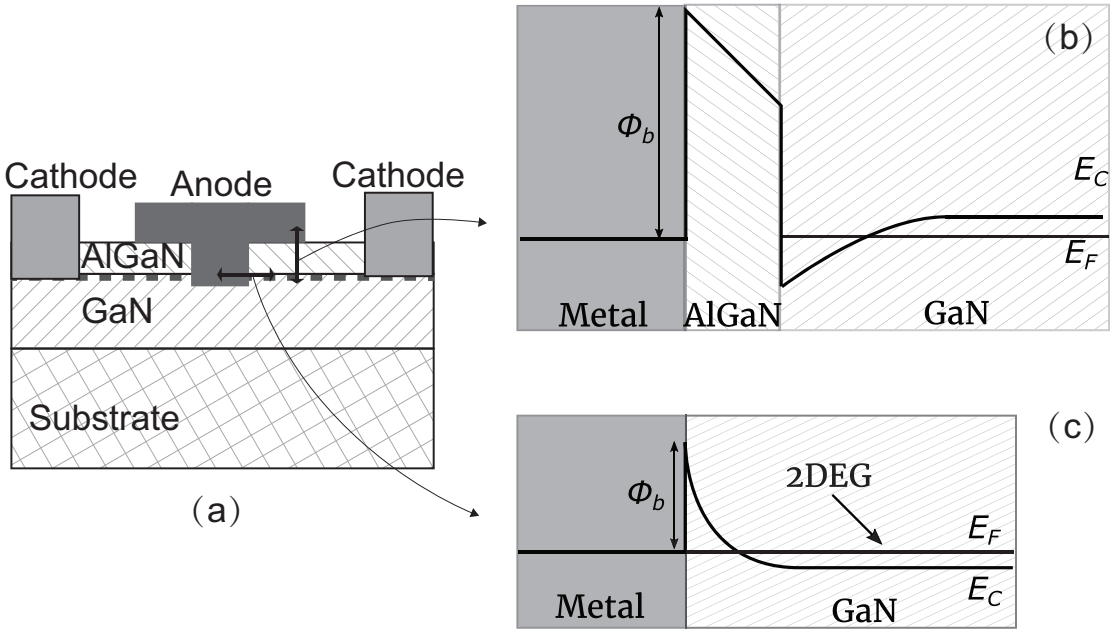

Figure 2.4: Device cross-section schematic of recessed AlGaN/GaN SBDs with field plate (a) and the electron energy band diagrams of the planar (b) and the recessed (c) Schottky junction. (d) The equivalent circuit under forward and reverse bias

plate, which is not necessary in a stand-alone fabrication process. The length of the anode field plate is 2 μm. This field plate length is adopted in the rest of this chapter unless specified otherwise. The comparison of the forward bias characteristics of the fabricated recessed SBDs with and without FP, and planar SBDs is plotted in Fig. 2.5.

Fig. 2.5 shows that the recessed SBD with FP indeed has similar forward bias characteristics with the recessed SBD, shown by the nearly overlapping *I*-*V*s of the two types of SBDs and identical ideality factors. This confirms that the recessed SBDs with FP retain the superior forward bias characteristics, validating previous analysis in designing the recessed SBDs with FP. Interestingly, the measured forward bias *I*-*V* shows no turning-on of the planar SBD even when the forward bias voltage is larger than its turn-on voltage. In junction barrier Schottky diodes, which is also equivalent to two diodes of different turn-on voltages in parallel connection, an decrease of on-resistance is often seen in the forward *I*-*V* when the voltage reaches the larger of the two turn-on voltages.

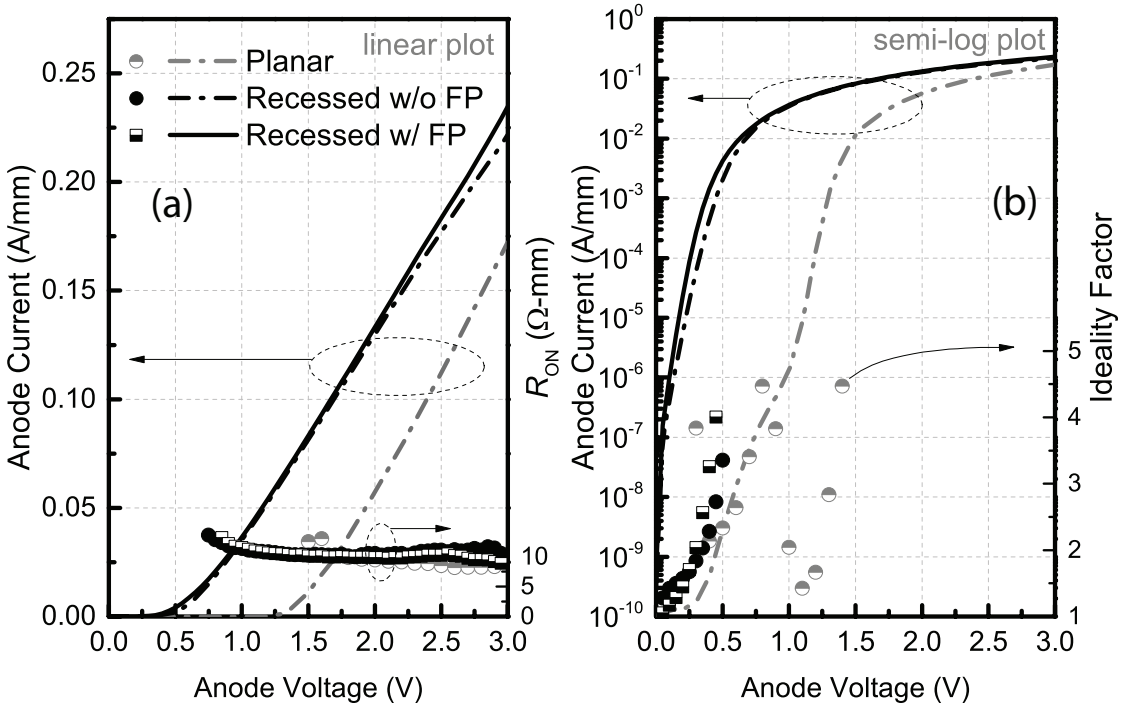

Figure 2.5: Comparison of the forward bias characteristics of the fabricated recessed SBD with FP, recessed SBD without FP and planar SBD. (a) Forward bias *I*-*V*s in linear plot and the differential on-resistance. (b) Forward bias *I*-*V*s in semi-logarithmic plot and ideality factor.

The absence of a turn-on of the planar SBD will be explained later.

The comparison of the reverse bias characteristics of the fabricated recessed SBDs with and without FP, and planar SBDs is shown in Fig. 2.6. It is shown that the recessed SBD with FP has similar reverse characteristics as that of the planar SBD, having a leakage current around 10X smaller than that of the recessed SBD without FP. This close match of reverse bias characteristics of the recessed SBD with a 2 μm FP and planar SBD suggests that the planar Schottky junction determines the reverse bias characteristics, regardless of the existence of the recessed Schottky junction.

Fig. 2.5 and 2.6 together shows that the recessed SBDs with FP indeed combines the merits of recessed AlGaN/GaN SBDs and planar AlGaN/GaN SBDs, having the low turn-on voltage of the recessed SBDs while retaining the relatively low reverse leakage

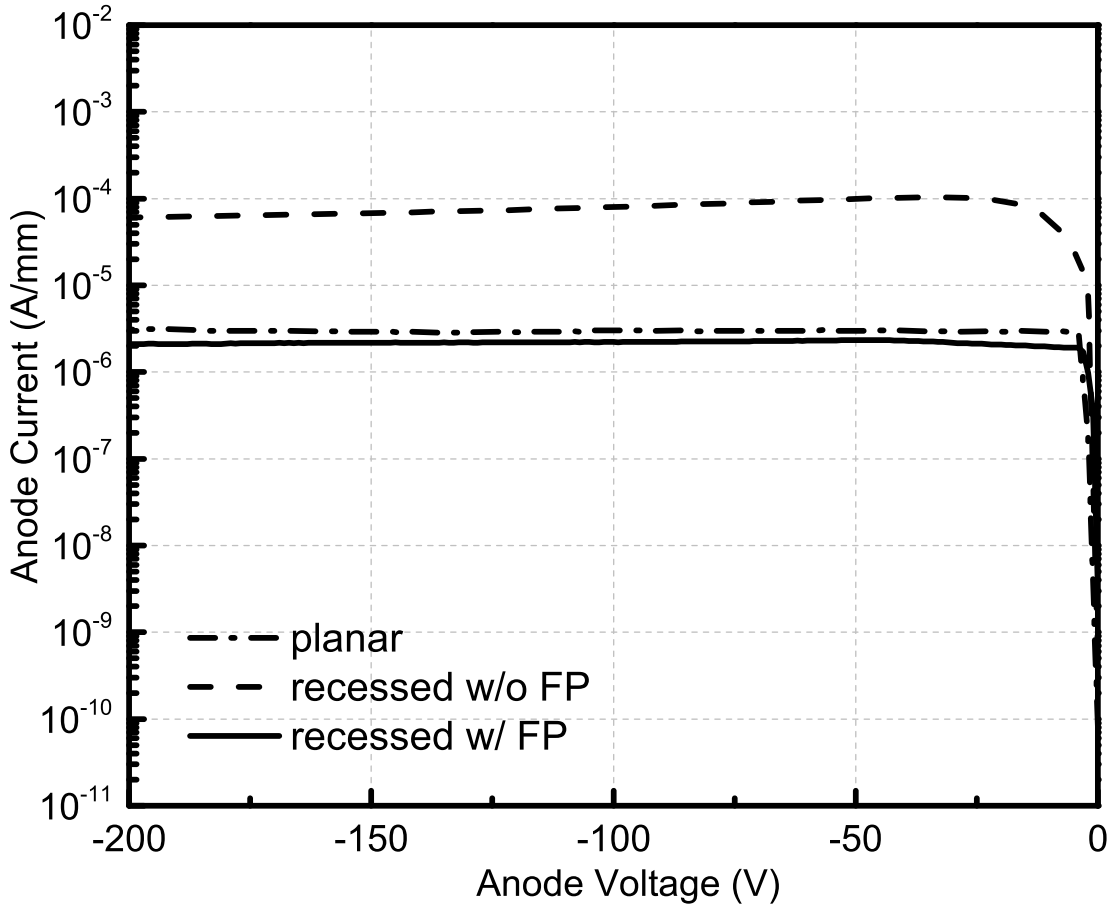

Figure 2.6: Comparison of the reverse bias characteristics of the fabricated recessed SBD with FP, recessed SBD without FP and planar SBD. The length of the anode field plate is 2 μm.

current of planar SBDs.

The statistical comparison of the turn-on voltages and leakage currents is plotted in Fig. 2.7 and 2.8. The forward turn-on voltage is extracted at a current level of 1 mA/mm, while the reverse leakage current is extracted at −100 V anode-cathode bias.

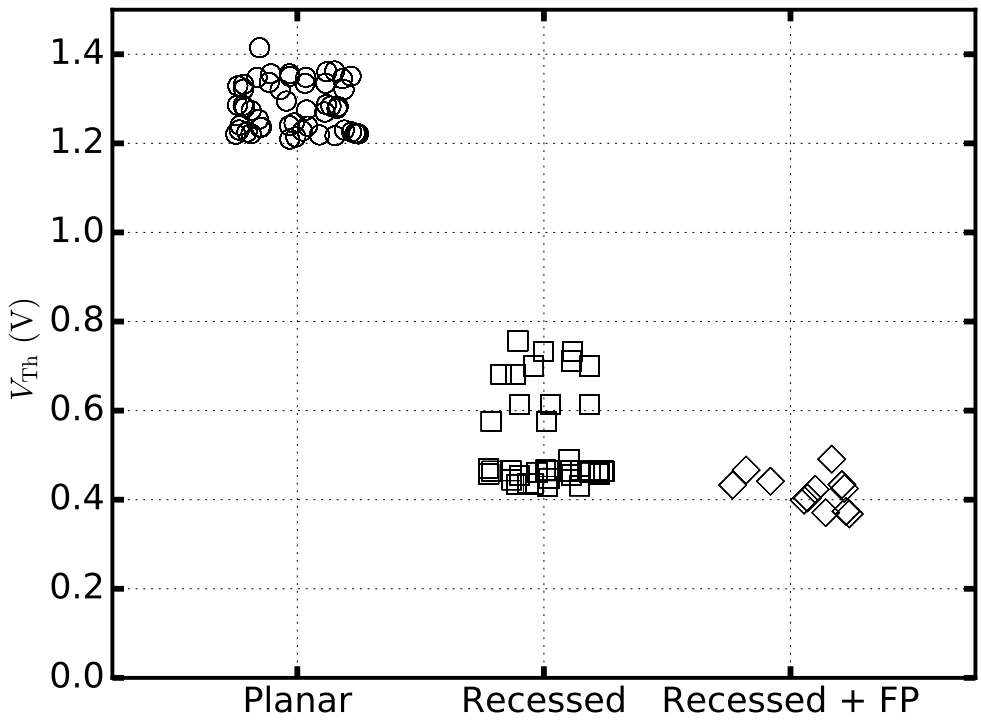

Figure 2.7: Statistical comparison of the turn-on voltages of planar AlGaN/GaN SBDs, recessed AlGaN/GaN SBDs with and without field plates. The turn-on voltage is extracted at a anode current level of 1 mA.

2.4 Controlling the Leakage Current

Although the recessed SBD with FP is shown to combine low turn-on voltage of recessed SBDs and low leakage current of planar SBDs, further reduction of leakage current is required to achieve a high breakdown voltage and be suitable for high voltage operations. As analyzed in prior sections, the leakage current of recessed SBDs with FP is dominated by the planar field plate. This leakage current has been extensively investigated in studying the gate leakage current of GaN HEMTs. It has been found that Poole-Frenkel conduction [67, 69] and current through dislocations result in the often observed large leakage current [61, 68]. Two techniques have been proven effective

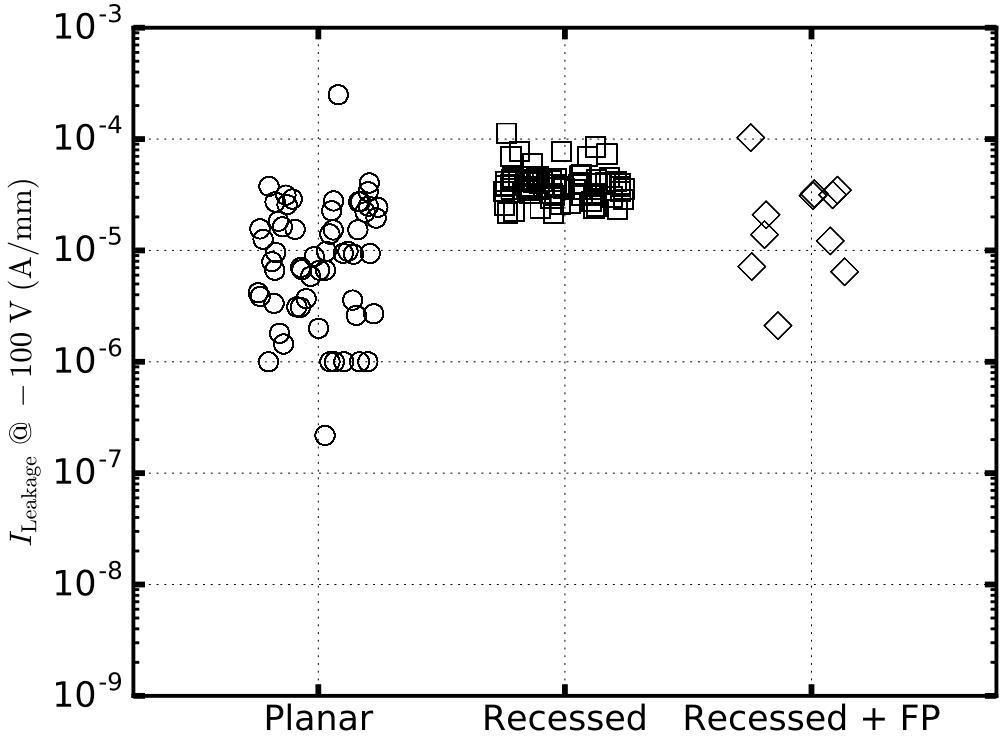

Figure 2.8: Comparison of the reverse leakage current of planar AlGaN/GaN SBDs, recessed AlGaN/GaN SBDs with and without field plates. The reverse leakage current is extracted at a reverse bias voltage of 100 V.

in reducing gate leakage current: inclusion of gate dielectric and O_2 plasma treatment. For GaN HEMTs with a gate dielectric, often referred to as MOSHEMT or MISHEMT, gate leakage current is often too low to be a concerning issue, as the presence of a gate dielectric can effectively eliminate the leakage current between the gate metal and the 2DEG channel. O_2 plasma treatment prior to gate metal deposition is found to reduce the leakage current by forming a thin layer of oxide at the surface. In this section, both techniques are explored for reduction of leakage current in recessed SBDs with FP.

2.4.1 Effect of SiNx

SiNx is the preferred dielectric for passivation of GaN HEMTs as it results in a low current collapse. It has recently been under intense research as a candidate for gate dielectric. Although SiNx has a band gap smaller than that of SiO_2 or Al_2O_3, it has a conduction band offset around 1 eV, which is sufficient to suppress the electron current by thermionic emission. The SiNx investigated here is deposited through atomic layer deposition.

The fabrication process of recessed SBDs with FP is modified to incorporate SiNx. A 20 nm thick SiNx layer is deposited after ohmic contact formation and mesa isolation etching. A CF_4 based dry etching of the deposited SiNx and BCl_3 based dry etching of AlGaN/GaN are carried out following the photolithography to expose the anode areas. The anode along with FP is then patterned through another photolithography and metal deposition by E-beam evaporation. The experiments in the rest of this chapter is performed with samples from a GaN-on-Si wafer grown by metal-organic chemical vapor phase deposition. The epitaxial layers consist of 1 nm GaN, 20 nm $Al_{0.26}Ga_{0.74}N$, 1 nm AlN, 200 nm GaN, and 4 μm buffer layer. All the epitaxial layers are grown along the metal face crystal orientation, i.e. [0001]. Hall effect measurement on samples diced from the wafer shows a 2DEG concentration of 7.5×10^{12} cm^{-2} with an electron mobility of 1800 cm^{-2}/Vs, resulting in a sheet resistance of 462 Ω/□.

The comparison of reverse bias *I-V* characteristics of recessed SBDs with and without SiNx under the FP is shown in Fig. 2.9, where the reverse leakage current of the recessed SBD with SiNx underneath FP has a larger leakage current compared to that without SiNx. The observed higher leakage current in recessed SBDs after incorporating SiNx underneath the FP is surprising, since the leakage current between the FP and 2DEG channel is expected to be largely suppressed by the insertion of SiNx. To find

out the cause of the increased leakage current, the forward *I*-*V* needs to be compared to monitor any change in the vertical Schottky junction. Fig. 2.10 shows the comparison

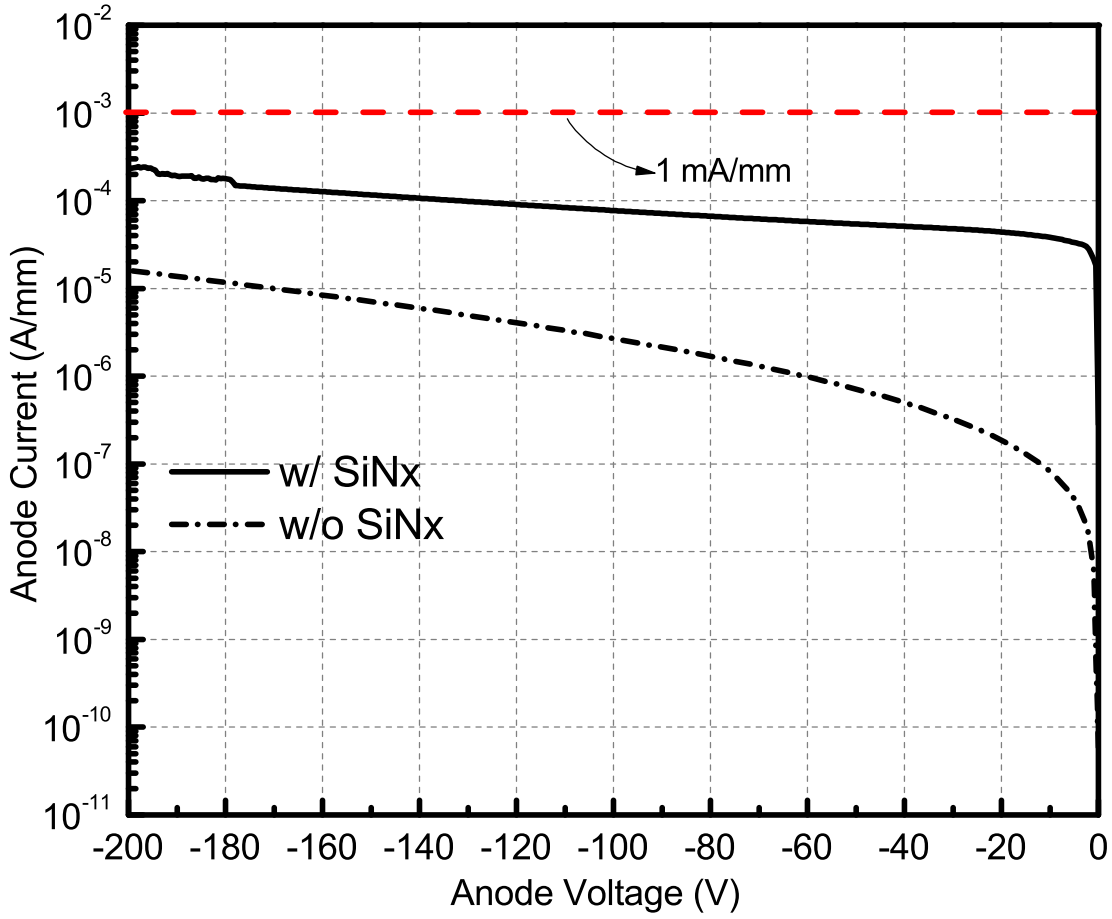

Figure 2.9: Comparison of reverse *I*-*V* characteristics of recessed SBDs with and without SiNx. Both SBDs have anode field plates integrated.

of forward bias *I*-*V* characteristics of recessed SBDs with and without SiNx underneath FP. The forward turn-on voltage is seen to be reduced from 0.66 V to 0.35 V after incorporation of SiNx underneath FP, a reduction close to 50%. A reduction in forward turn-on voltage is a result of the decrease of the Schottky barrier height, which in turn results in an increase in leakage current through the Schottky barrier. The decrease of Schottky barrier height is likely due to the increase of 2DEG concentration induced by the positive charge in the deposited SiNx. This increase of 2DEG density caused by SiNx deposition is routinely observed with GaN HEMT wafers, with either AlGaN or

InAlN top-barriers [33].

Notice that the reverse leakage currents in Fig. 2.9 is higher than the recessed SBDs with FP shown in prior sections. This is likely due to the higher dislocation density in epitaxial layers grown on Si substrates than sapphire substrates. This leakage current caused by the decrease of Schottky barrier height and dislocation will be addressed with O_2 plasma treatment as described in the next section.

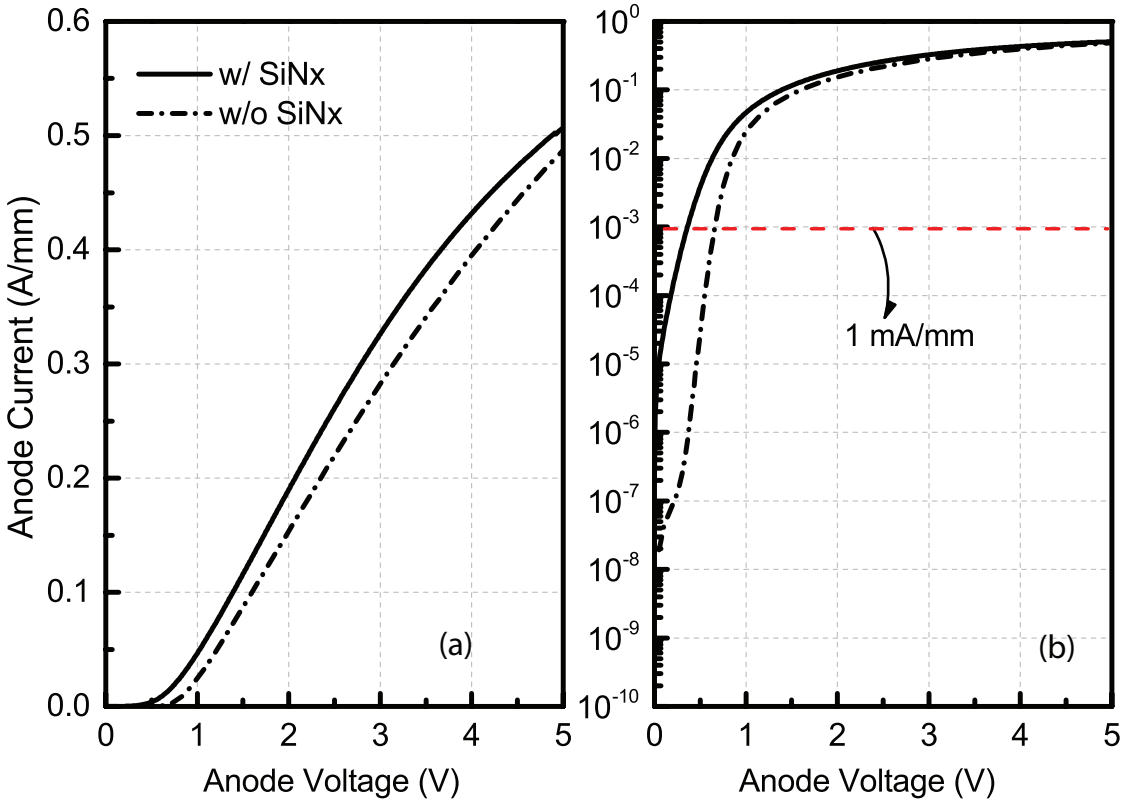

Figure 2.10: Comparison of forward *I-V* characteristics of recessed SBDs with and without SiNx. Both SBDs have a 2 μm-long anode field plate integrated.

2.4.2 Effect of O_2 Plasma Treatment

As has been shown in the previous section, an increase in reverse leakage current is observed when SiNx is incorporated underneath the FP in recessed SBDs, caused by the

reduction in Schottky barrier height. To increase the Schottky barrier height and thus curb the leakage current, O_2 plasma treatment is explored. Oxygen plasma treatment has been reported to effective in increasing Schottky barrier height and reducing leakage current in GaN HEMTs[70]. Here the O_2 plasma treatment is carried out right before anode metal deposition, so that the entire etched anode area, including the sidewall and planar area are exposed to O_2 plasma treatment. O_2 plasma treatment was carried out in RIE using a 30 sccm O_2 flow at 20 mTorr and a RF power of 30 W and a 75 V self bias.

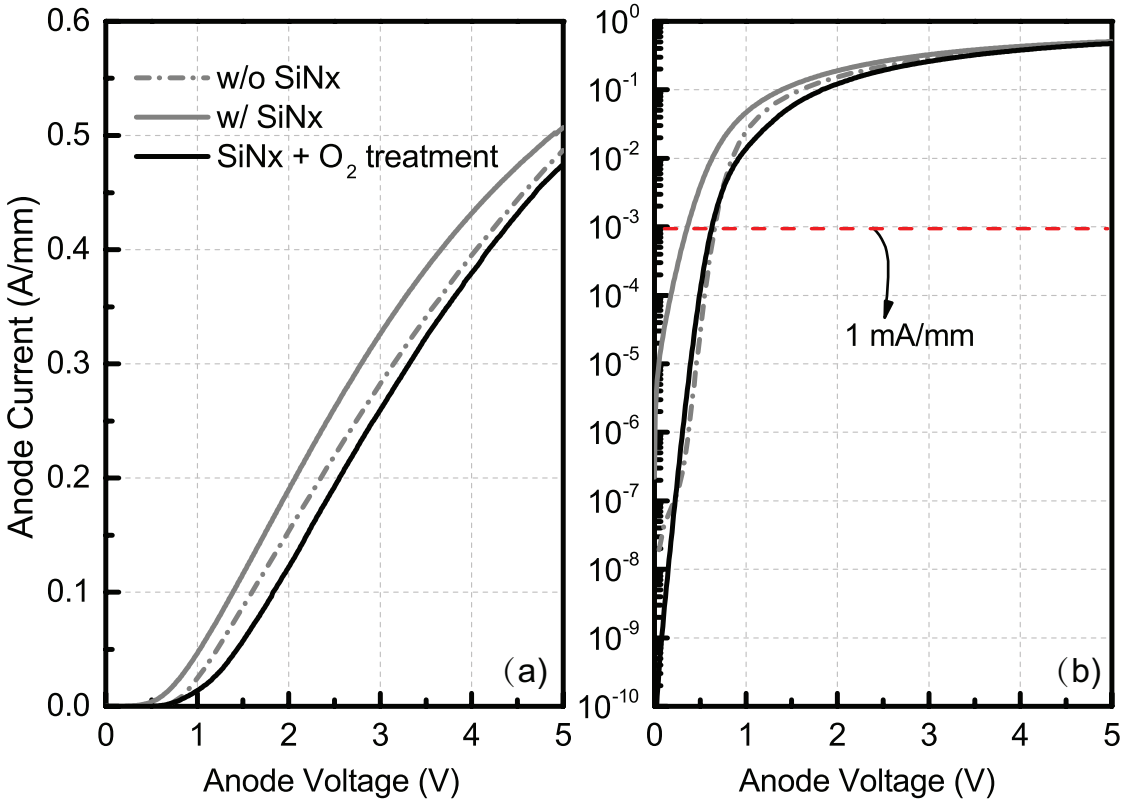

Figure 2.11: Effect of O_2 plasma treatment at the recessed anode on the forward *I-V* characteristic of the recessed SBDs. All SBDs have a 2 μm-long anode field plate integrated.

The effect of O_2 plasma treatment on the *I-V* characteristics of recessed SBDs is shown in Fig. 2.11, along with the *I-V* characteristics of recessed SBDs without SiNx underneath FP. Oxygen plasma treatment is shown to be effective in increasing the Schottky barrier height and hence the turn-on voltage. The decrease of turn-on volt-

age brought by the incorporation of SiNx is completely offset by O_2 plasma treatment. This almost identical turn-on voltage between recessed SBDs without SiNx and with SiNx as well as O_2 treatment allows an accurate assessment of the efficacy of SiNx in suppressing the leakage current through the field plate.

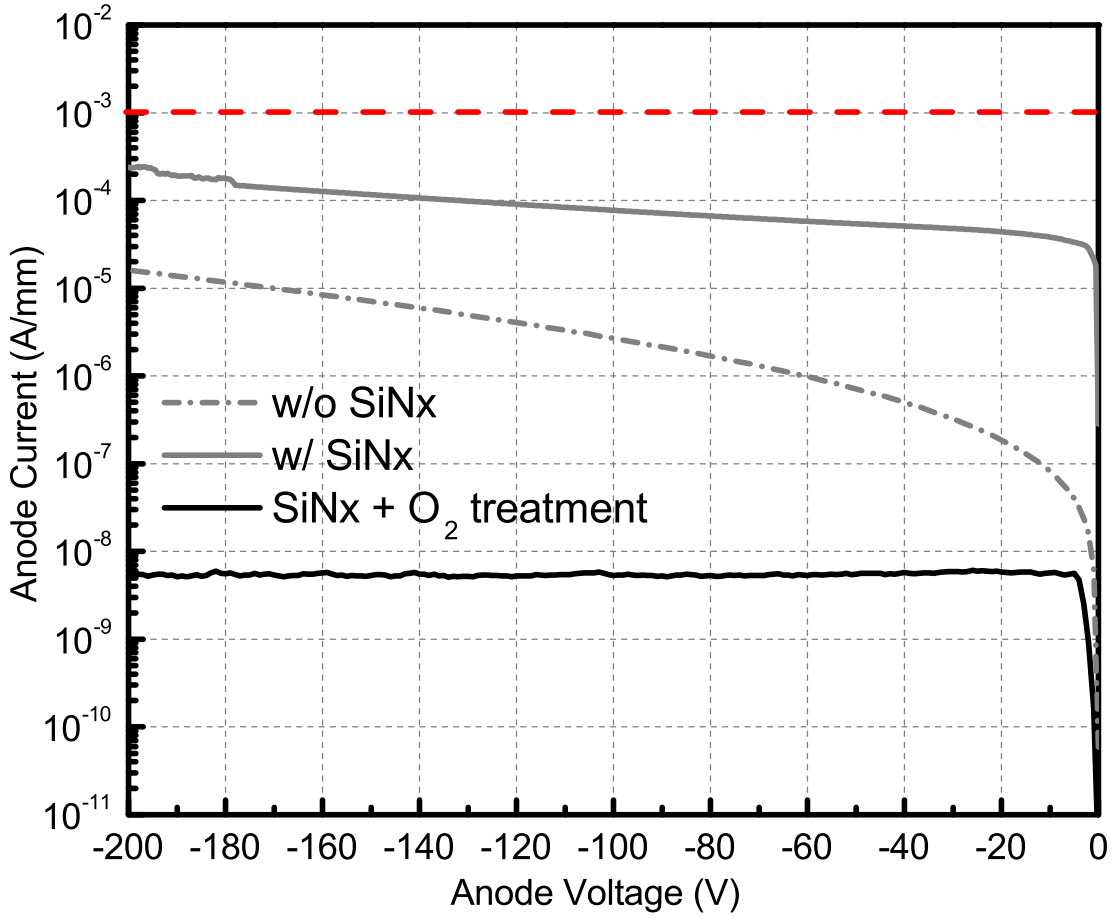

Figure 2.12: Effect of O_2 plasma treatment at the recessed anode on the reverse *I-V* characteristic of the recessed SBDs.

Fig. 2.12 shows the effect of O_2 plasma treatment on the reverse *I-V* characteristics of recessed SBDs with SiNx underneath FP. The IV characteristics of recessed SBDs without incorporating SiNx is also shown for comparison. It is seen in Fig. 2.9 that O_2 plasma treatment results in a leakage current reduction as large as 10^4 times. Compared to recessed SBDs without SiNx underneath FP, recessed SBDs with SiNx as well as O_2 plasma treatment show a reverse leakage current about 1000 times smaller. Considering

that the SBDs without SiNx and SBDs with SiNx as well as O_2 plasma treatment have similar Schottky barrier heights and forward turn-on voltages, properties determined by the direct Schottky contact between the anode metal and 2DEG, the incorporation of SiNx is indeed effective in suppressing the leakage current between FP and 2DEG. Incorporating SiN underneath the FP in recessed SBDs has different effects on the leakage current through the FP and the leakage current through the metal/2DEG Schottky contact. The SiNx layer decreases the leakage current through the FP by passivating the leakage path and increasing the barrier height, but also increase the leakage current through the metal/2DEG Schottky junction by increasing the 2DEG density hence reduce the Schottky barrier height. O_2 plasma treatment can effectively increase the Schottky barrier height and suppress the leakage current through metal/2DEG Schottky junction. As a result, by employing both SiNx and O_2 plasma treatment, the reverse leakage current of recessed SBDs is successfully controlled.

2.5 1.9 kV Lateral AlGaN/GaN SBDs

Having designed the device structure and fabrication processes to achieve SBDs featuring low forward turn-on voltage and low reverse leakage current, we further revise the device design to realize SBDs with high breakdown voltages.

2.5.1 Device Design

In designing semiconductor devices for high voltage applications, multiple field plates is a proven effective technique in managing the maximum electric field and boosting breakdown voltages [71, 72, 25, 73]. The ideal case for electric field management to

maximize the breakdown voltage is to create a constant electric field profile across the voltage bearing region, which renders the largest breakdown voltage for a given electric field maximum. In the case of managing electric field using multiple field plates, the electric field in the voltage bearing region is shaped into multiple peaks, with one peak at the end of each field plate plus one at the edge of the protected electrode. In this manner, the breakdown voltage is increased provided that the device breaks down at the same electric field maximum.

To employ the multiple field plate technique to boost the breakdown voltage of the recessed SBDs, a second anode field plate is incorporated. The cross section schematic of the recessed SBD with double field plate is shown in Fig. 2.13 along with the GaN wafer epitaxial layer structure. The first and second field plates are 2 and 3 μm long, respectively. To ensure the efficacy of the field plates, the pinch-off voltages by the field plates should be sufficiently separated [74]. So in the designed device structure, the 100 nm thick SiO_2 layer underneath the second field plate has an effective oxide thickness (EOT) > 10 times larger than the SiNx underneath the first field plate. SiO_2 is chosen as the dielectric underneath the second field plate because of its large band gap and thus breakdown electric field, as the electric field is expected to peak at the corner of the second field plate.

It is worth pointing out the first field plate is deliberately designed to feature a small pinch-off voltage in absolute value so that it can effectively curb the reverse leakage current as described in previous sections. As a result, the first field plate serve a purpose more of restricting the reverse leakage current than boosting the breakdown voltages.

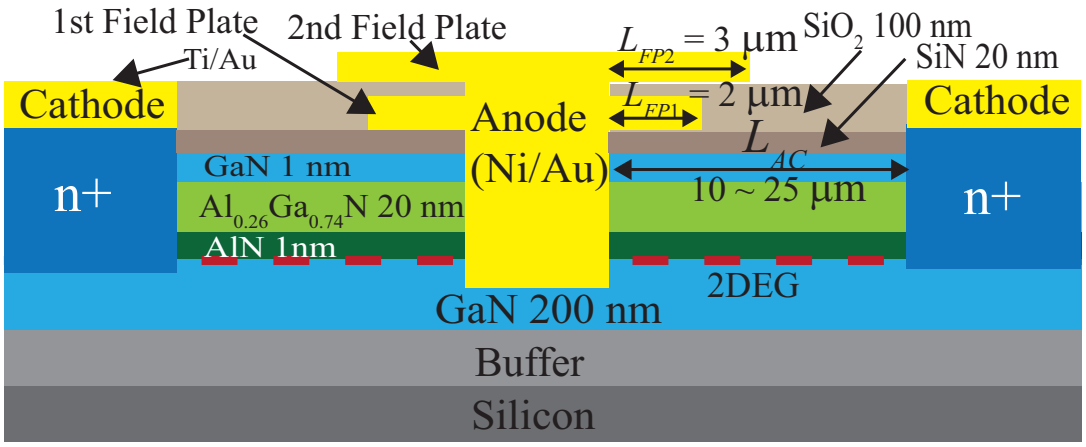

Figure 2.13: Cross-section schematic of the lateral AlGaN/GaN SBD with recessed anode and double field plate.

2.5.2 Device Fabrication

The fabrication process for the recessed SBDs with double FP is developed based on the previously described processes. The fabrication starts with ohmic contact formation by MBE regrowth and Ti/Au deposition [75, 5]. The selectively regrown n^+ GaN has a thickness of 100 nm and a Si doping concentration of 1×10^{20} cm^{-3}. Cl_2 based reactive ion etch is then carried out to isolate the testing structures fabricated along with the SBDs. All diodes are self-isolated, as they are designed in a circular layout with cathodes surrounding anodes. A 20 nm SiNx layer is then deposited by atomic layer deposition as the dielectric for the first field plate. The anode is then defined by optical lithography and selective etching to remove the SiNx layer and 50nm of AlGaN/GaN using CF_4 and BCl_3 plasma, respectively. The anode contact along with the first field plate with a length (L_{FP1}) of 2 μm is then patterned by photolithography. The sample is then subject to a O_2 plasma treatment performed on a RIE system. The anode metal stack consisting of Ni/Au is then deposited by E-beam evaporation. The thickness of the deposited Ni is 100 nm, larger than the anode etch depth, to ensure a good adhesivity between the anode metal and the anode side wall. A SiO_2 layer of 100 nm is subsequently

deposited as the dielectric for the second field plate, followed by contact via patterning with optical lithography and wet etch by buffered oxide etchant (BOE). Finally, the second field plate with a length of 3 μm is formed through optical lithography and Ni/Au deposition by E-beam evaporation.

After the completion of the fabrication process, Hall effect measurement using the square van der Pauw structure shows a 2DEG concentration of 9.8×10^{12} cm^{-2} and an electron mobility of 1490 cm^2/Vs, resulting in a sheet resistance of 428 Ω/□. Notice that the 2DEG concentration is increased from 7.5×10^{12} cm^{-2}, a 30% increase, due to the deposition of SiNx. Owing to the degradation of electron mobility during fabrication processes, the sheet resistance of the 2DEG after the complete fabrication processes remains similar to that of the as-grown 2DEG.

2.5.3 Device Characteristics

The DC characteristics of the fabricated SBDs are measured using a Keithley 4200 semiconductor characterization system. The measured forward bias *I*-*V* characteristics of the SBDs with various anode/cathode separations are plotted in Fig. 2.14. The ideality factor n and the forward turn-on voltage voltage $V_{\text{turn-on}}$ are extracted to be 1.22 ± 0.05 and 0.67 ± 0.02 V, respectively. The forward turn-on voltage is consistent with the previously described recessed SBDs with SiNx and O_2 plasma treatment (Fig. 2.11). Notice that the *I*-*V* characteristics of SBDs with different anode/cathode separations overlap over 9 orders of magnitude in the linear region of the semi-logarithmic plot (Fig. 2.14 left). Since the forward *I*-*V* characteristics are dominated by the Schottky junction rather than the series resistance for $V < V_{\text{turn-on}}$, this overlapping *I*-*V* curves, together with the aforementioned small variations of ideality factors and turn-on voltages show that the

fabricated SBDs have an excellent uniformity.

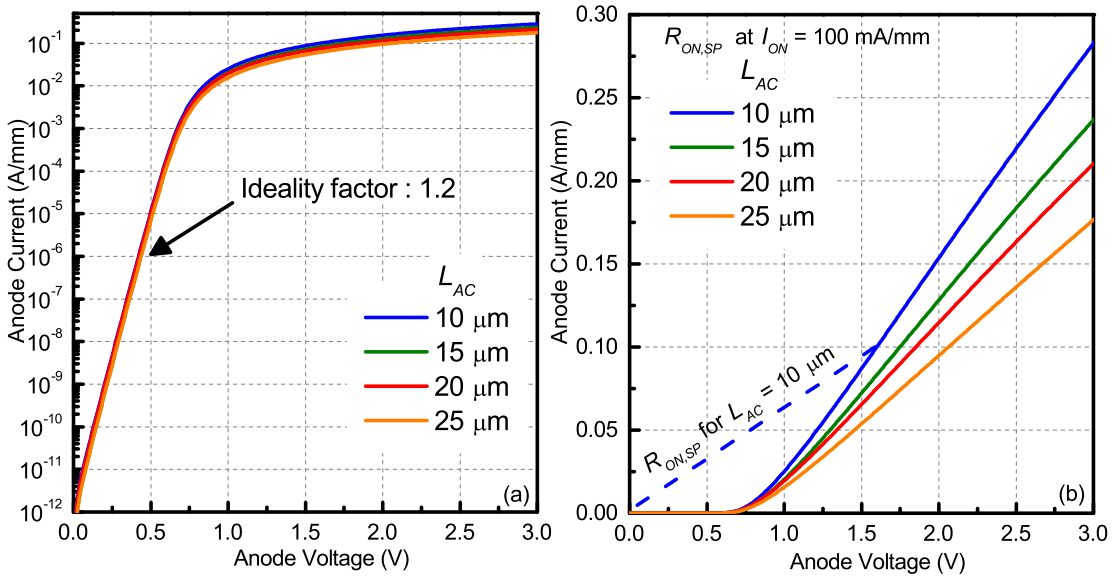

Figure 2.14: Forward *I-V* characteristics of the fabricated SBDs with recessed anode and double field plate, plotted in semi-logarithmic (left) and linear scale (right). The dashed line in the right denotes the method for extraction of $R_{\mathrm{ON,SP}}$. (This figure is reproduced from Zhu et al, IEEE EDL 2015.)

The on-resistance of the SBDs can be extracted using the linear plot of the forward *I-V* characteristics, as shown in Fig. 2.14 (right). The on-resistance can be calculated either as an absolute resistance ($R_{\mathrm{ON}} = V_{\mathrm{AC}}/I_{\mathrm{AC}}$) or a differential resistance ($R_{\mathrm{ON}} = \frac{dV_{\mathrm{AC}}}{dI_{\mathrm{AC}}}$).The absolute on-resistance is accounts for the voltage drop and power loss on the junction (Schottky or p-n) and thus is often used in the context of DC and power efficiency. The differential on-resistance excludes the static voltage drop on the junction and emphasize on the response of voltage/current as a result of the change in the applied current/voltage. Consequently, the differential on-resistance is more suitable parameter for AC related applications. For the purpose of fairly benchmarking the performance of diodes, the on-resistance should be calculated with the same method.

One of the key merits of SBDs is the junction barrier height, which leads to a low voltage drop on the junction when $V_{\mathrm{AC}} > V_{\mathrm{turn-on}}$ and thus a low forward power loss. As

a result, it is more meaningful to focus on the absolute on-resistance to highlight SBDs' advantage of low turn-on voltage. This is especially true in diodes fabricated with wide-bandgap materials, where turn-on voltage of p-n diodes can be > 5 times larger than that of SBDs. The dashed line in Fig. 2.14(right) depicts how the absolute on-resistance is calculated for the SBD with a L_{AC} of 10 μm. The calculated absolute $R_{ON,SP}$ for SBDs with a L_{AC} of 10 μm and 25 μm is 1.6 and 5.12 $m\Omega \cdot cm^{-2}$, respectively.

Since the recessed SBDs have 2D-3D contacts between the 2DEG and the anode metal, one may ask whether this transition of dimensionality could result in a significant impact on the on-resistance. To answer this question, the differential on-resistance is broken down to each contributing components. As the SBDs are in a circular layout illustrated in the inset plot of Fig. 2.15, the differential on-resistance R_{On} can be modeled as:

$$R_{On,diff} = \frac{R_{sh}}{2\pi}(lnR_2 - lnR_1) + \frac{R_C}{2\pi R_2} + R_0 \tag{2.3}$$

where R_1 and R_2 are the cathode and anode radius, R_C is the contact resistance and R_0 is the rest of $R_{On,diff}$, including the contribution from the 2D-3D junction. As the contact resistance can be obtained through TLM measurement, R_{SH} and R_0 can be extracted by measuring SBDs with different cathode radius, as shown in Fig. 2.15(left). A good linear fitting of $R_{On} - R_C$ over $lnR_2$is observed in Fig. 2.15(left), showing a good agreement between the experimental data and model. Based on the extracted R_{SH} and R_0, a detailed breakdown of the on-resistance can be obtained, as shown in Fig. 2.15(right).

The on-resistance component (R_0) which includes the contribution from the 2D-3D contact, accounts for about 33% of the total on-resistance for SBDs with a L_{AC} of 5 μm. As R_0 is constant as long as the anode perimeter remains the same, the percentage of R_0's contribution to the total R_{On} decreases as L_{AC} increases. In general, the 2D-3D nature of the Schottky contact does not result in a significant increase in differential on-

resistance. This is consistent with the comparison of on-resistance between the planar and recessed SBDs shown in previous sections, where the two types of SBDs show similar differential on-resistance. Given that the 2D-3D Schottky contact brings a > 50% decrease of forward turn-on voltage, its benefit is even better highlighted by the absolute on-resistance.

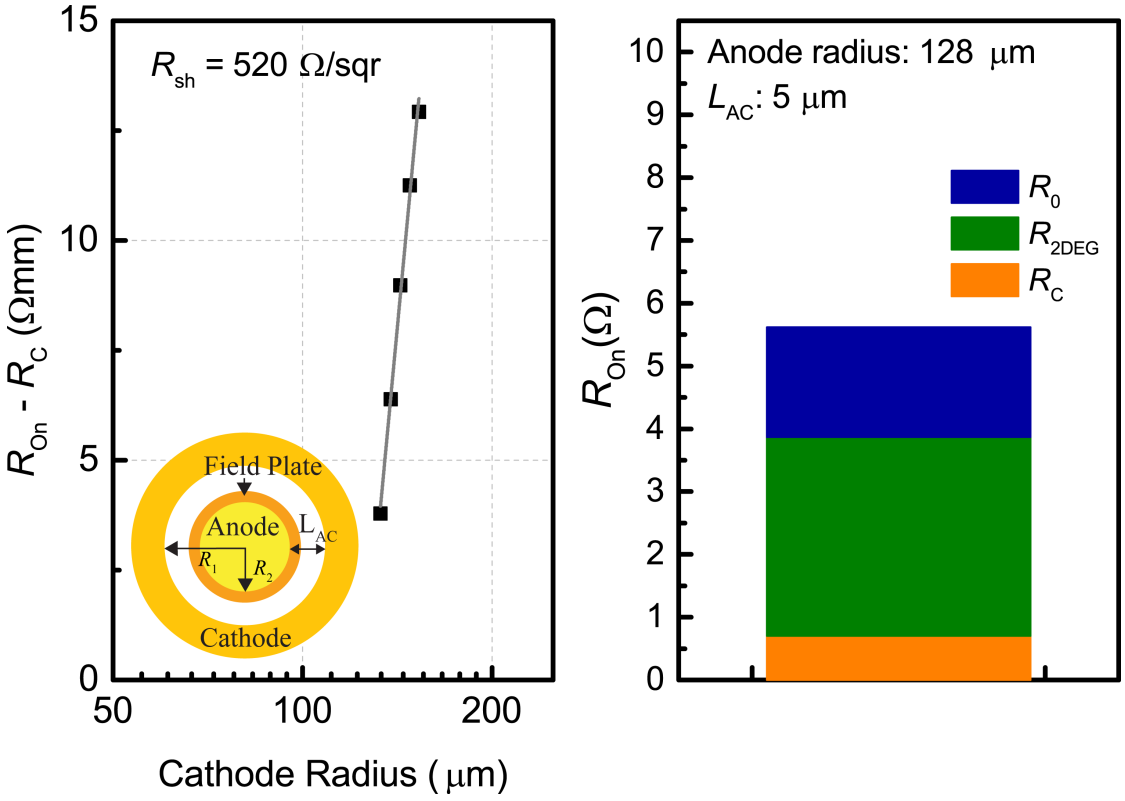

Figure 2.15: (a) On-resistance excluding the contact resistance of SBDs with a constant anode radius of 128 μm and various L_{AC}. The inset figure illustrates the layout of the fabricated diodes. The resistance contributed by the 2D-3D junction is extracted by linear fitting of the experimental data. (b) Breakdown of the components contributing to the total on-resistance.

The reverse bias *I*-*V* characteristics of the fabricated SBDs are plotted in Fig. 2.16. All devices show a low reverse leakage current (<5 μA/mm) up to 700 V reverse bias. With a increasing anode/cathode separation distance, a larger breakdown voltage is obtained, which is a result of the well-known tradeoff between breakdown voltage and on-resistance. A breakdown voltage of 1.93 kV, extracted at a anode current level of

1 mA/mm, is achieved with a L_{AC} of 25 μm. The absolute on-resistance $R_{ON,SP}$ for the SBD, extracted at a anode current density of 100 mA/mm, is 5.12 mΩ · cm^{-2}. This leads to a power figure-of-merit (FOM, calculated by $BV^2/R_{ON,SP}$) of 727 MW/cm^2. These results represented the record breakdown voltage and state-of-the-art performance among all reported GaN-on-Si SBDs. For the SBD with a L_{AC} of 20 μm, a breakdown voltage of 1.6 kV and a $R_{ON,SP}$ of 3.7 mΩ · cm^{-2} are achieved, resulting in a power FOM of 691 MW/cm^2.

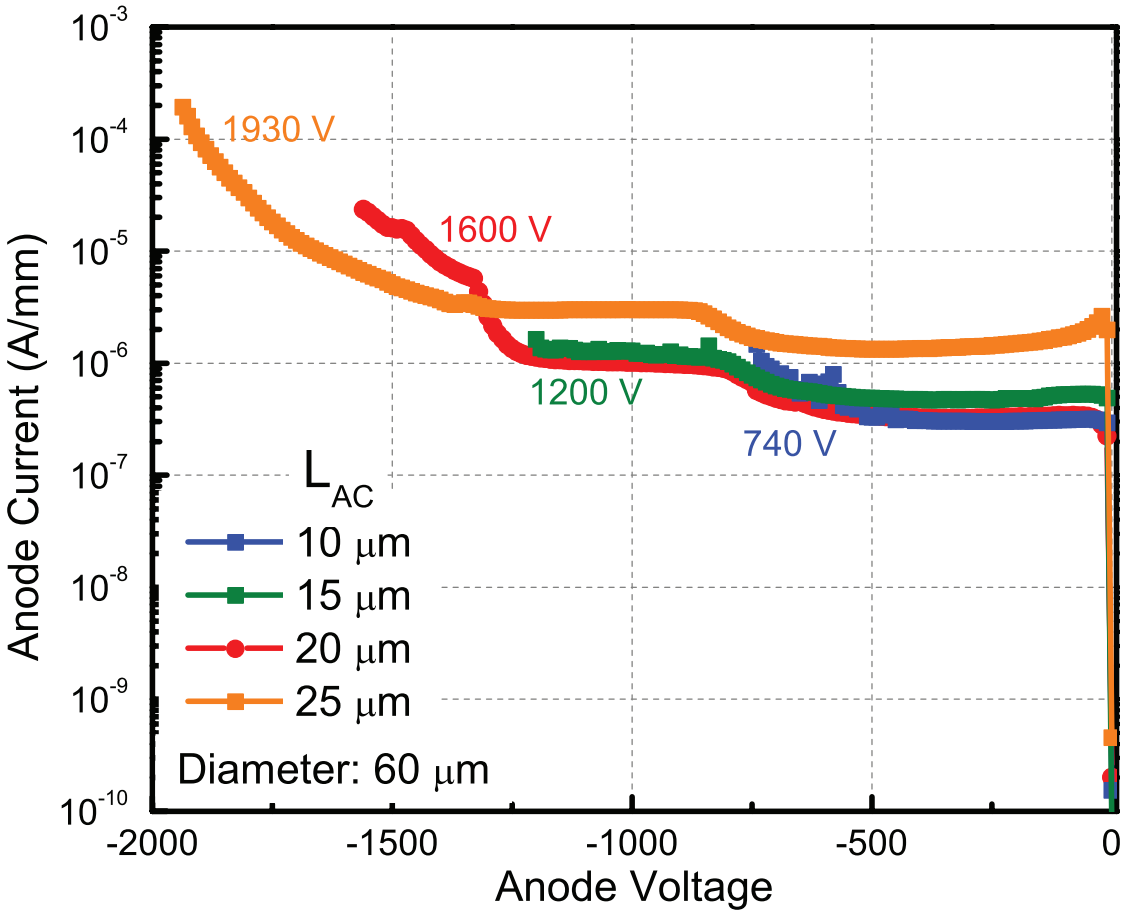

Figure 2.16: Reverse *I-V* characteristics of the fabricated SBDs with recessed anode and double FP. The anode-cathode separation distance ranges from 10 μm to 25 μm, resulting in breakdown voltages ranging from 740 V to 1930 V. A low reverse leakage current of <10 μA/mm is observed up to a reverse bias of 1200 V. (This figure is reproduced from Zhu et al, IEEE EDL 2015.)

For recessed SBDs without FP, the capacitance between anode and cathode is so

small that even the SBDs with a perimeter of 800 μm has capacitances below the minimum measurable capacitance of the Keithley 4200-SCS. This is due to the small effective area of the 2D-3D contact between the anode metal and 2DEG. It is thus difficult to characterize the 2DEG behavior in the SBD under reverse bias. However, with the incorporation of field plates, the anode/cathode capacitance is significantly boosted by the field plates. As a result, the behavior of the 2DEG underneath the field plates can be characterize by monitoring the anode/cathode capacitance. This also allows verification of the effect of field plates described in previous sections. The capacitance-voltage characteristics of the recessed SBD with double FP is shown in Fig. 2.17. The anode perimeter of the SBD is 200 μm. Two capacitance steps can be seen in Fig. 2.17, corresponding to the depletion of the 2DEG underneath each field plate. Note that at $V_{\text{Anode}} < -20$ V, the measured capacitance is at the lower limit of the CV meter. The negligible conductance in Fig. 2.17 is due to the low reverse leakage current.

With the *C*-*V* characteristics measured, the effect of the first field plate on the reverse leakage current of the fabricated SBDs can be investigated by correlating it with the reverse *I*-*V* characteristics, as shown in Fig. 2.18. It is seen in Fig. 2.18 that as the anode voltage decreases from 0 V, the anode current saturates at about the same voltage as the first capacitance step. The sharp capacitance step is due to the depletion of the 2DEG underneath the first field plate, which in turn allows the first field plate to shield the Schottky junction from further increase of electric field and hence the saturation of anode current. This result is consistent of the prior explanation of the working mechanisms of the recessed SBDs with FP.

To understand the role of the second field plate in boosting the breakdown voltage, a set of recessed SBDs with a single FP is compared with recessed SBDs with double FP. The plot of BV versus L_{AC} for recessed SBDs with single FP and double FP is shown

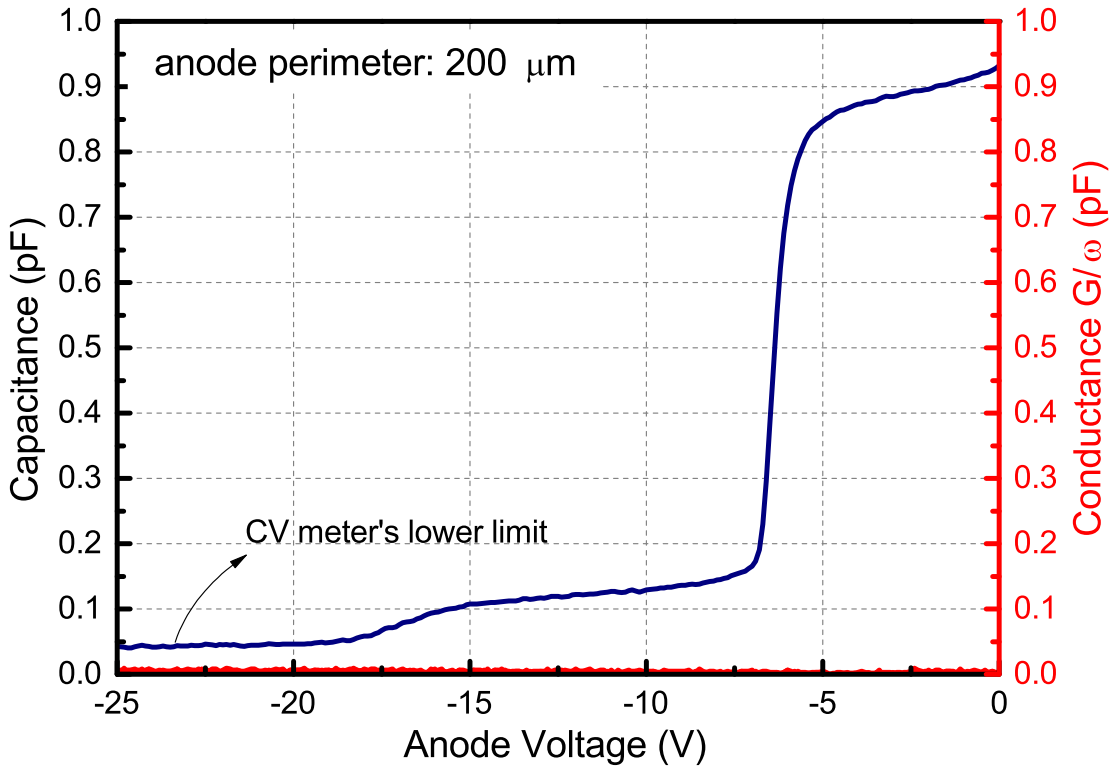

Figure 2.17: *C-V* characteristics of the fabricated recessed SBD with double field plate. Two capacitance steps are observed in the plot, corresponding to the depletion of the 2DEG underneath each field plate. Notice that the measured capacitance measured at V_{Anode} < -18 V remains flat due to the limits of the CV meter.

as Fig. 2.19. Both sets of devices are fabricated with identical processes other than the inclusion of the second field plate. A clear boost of breakdown voltage (5% ≈ 25%) is seen in Fig. 2.19 when the second field plate is incorporated. Both sets of devices show a linear increase of breakdown voltage as the anode/cathode separation is increased from 5 μm to 25 μm. The record high 1.93 kV breakdown voltage is thus attributed to the double field design and fabrication process developments to effectively curb the reverse leakage current.

As the actual breakdown electric field in devices is difficult to monitor, an effective breakdown electric field is often used to compare devices with different breakdown voltage ranges and understand the room for further improvement. One way to calculate the

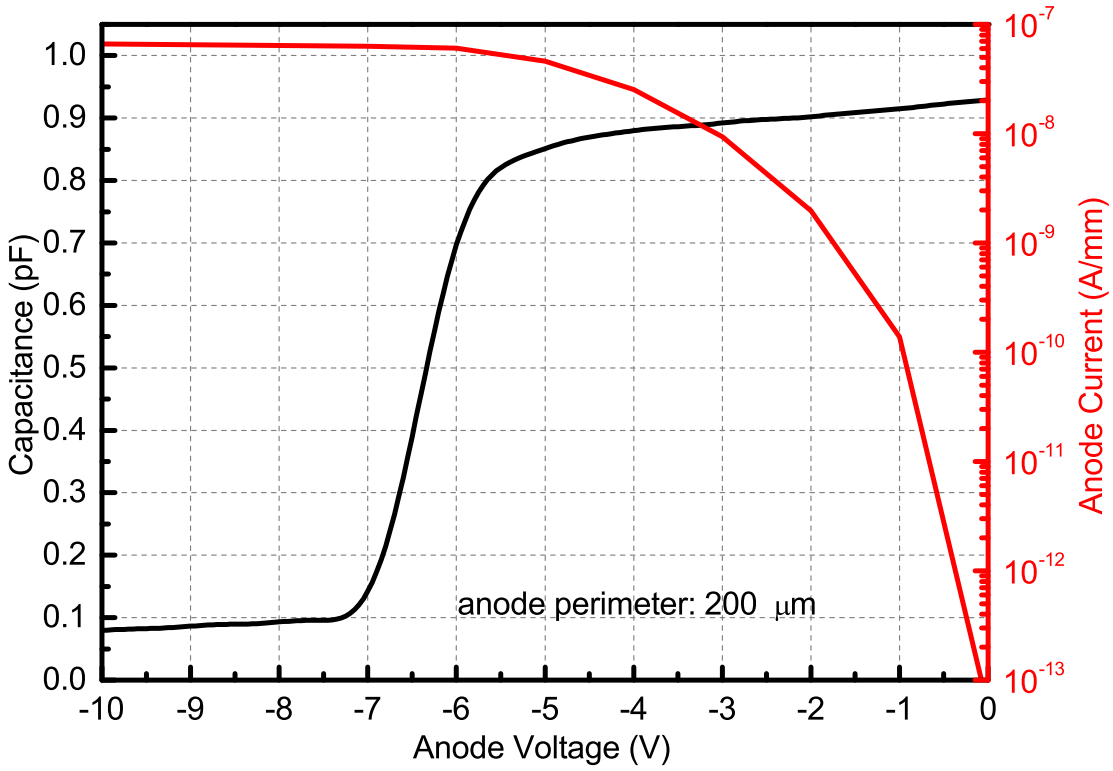

Figure 2.18: Comparison of the measured reverse *I*-*V* and *C*-*V* characteristics of the fabricated recessed SBD with double field plate. The voltage at which the reverse leakage saturates closely match the pinch-off voltage of the first field plate, as seen by the sharp decrease of measured capacitance. (This figure is reproduced from Zhu et al, IEEE EDL 2015.)

effective breakdown field is by dividing the breakdown voltage over the voltage bearing distance, assuming that in an ideal case the electric field can be shaped to be constant. The effective breakdown field is then calculated to be $E_{\mathrm{Br,eff}} = V_{\mathrm{Br}}/L_{\mathrm{AC}} = 0.77$ MV/cm. Another way to calculate the effective breakdown field, which better represents the electric field distribution, is to assume a trapezoidal electric distribution (inset of Fig. 2.19) where the lateral electric field in the region underneath the field plates is constant. Under this assumption, the effective breakdown electric field is calculated to be 1.14 - 1.4 MV/cm, which is still far below the value in bulk GaN (3.4 MV/cm) [76]. It is worth emphasizing that these calculations are not accurate in finding out the actual breakdown electric field in the devices, since two-dimension simulations show that electric field

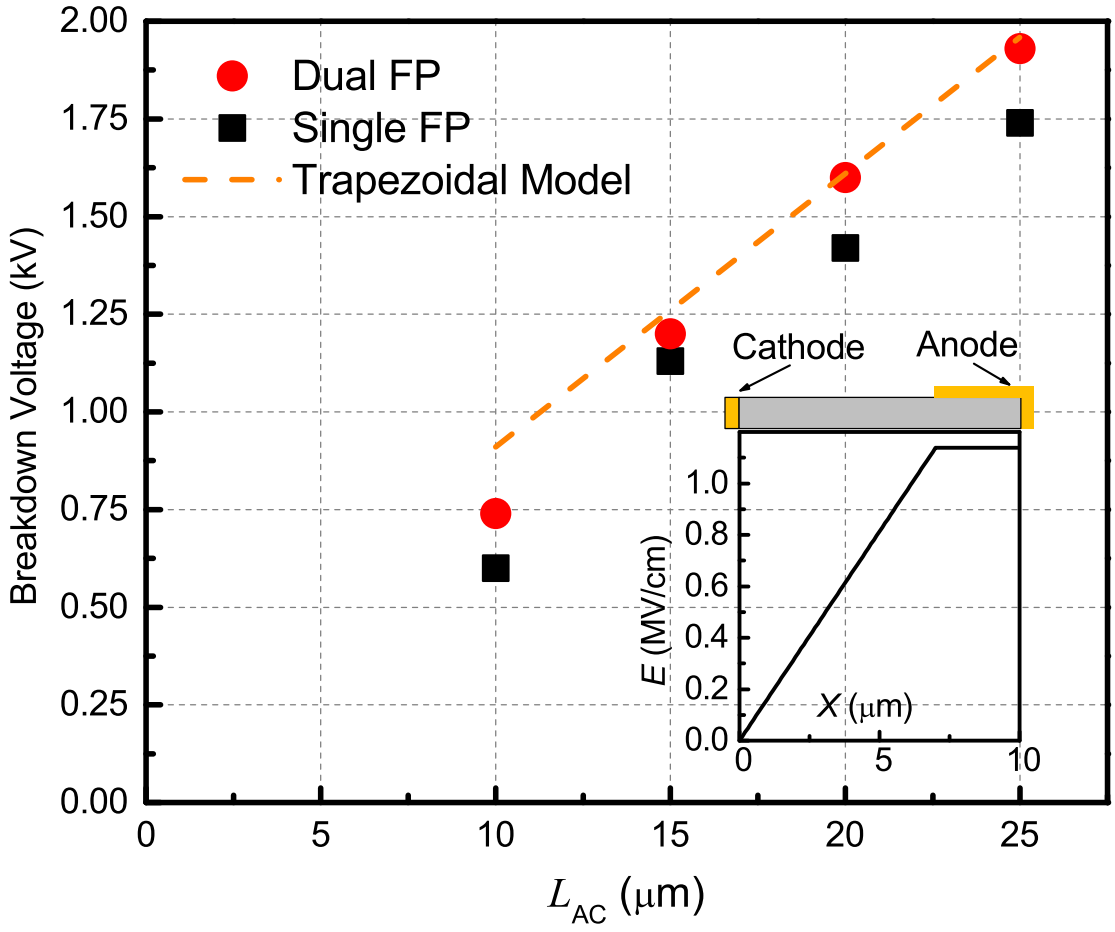

Figure 2.19: BV versus L_{AC} for SBDs with double and single field plate structures. The dash line is the calculated BV using an E_{Cr} of 1.4 MV/cm and the trapezoid electric field profile shown in the inset. (This figure is reproduced from Zhu et al, IEEE EDL 2015.)

spikes at the edges of each field plate as well as the Schottky junction. However, the effective electric field calculation provides insights for further design improvement and a unified approach for comparing devices with different geometries.

As there is an intrinsic trade-off between the turn-on voltage and breakdown voltage, a benchmark plot is shown in Fig. 2.20 to compare the recessed SBDs with double FP to previously reported SBDs. All the reference values in the figure are re-calculated based on the reported data following the definition shown within Fig. 2.14. The SBDs reported in this work has notably the record high breakdown voltage while maintaining a turn-on

voltage below 0.7 V, representing a significant advancement of the performance of GaN SBDs.

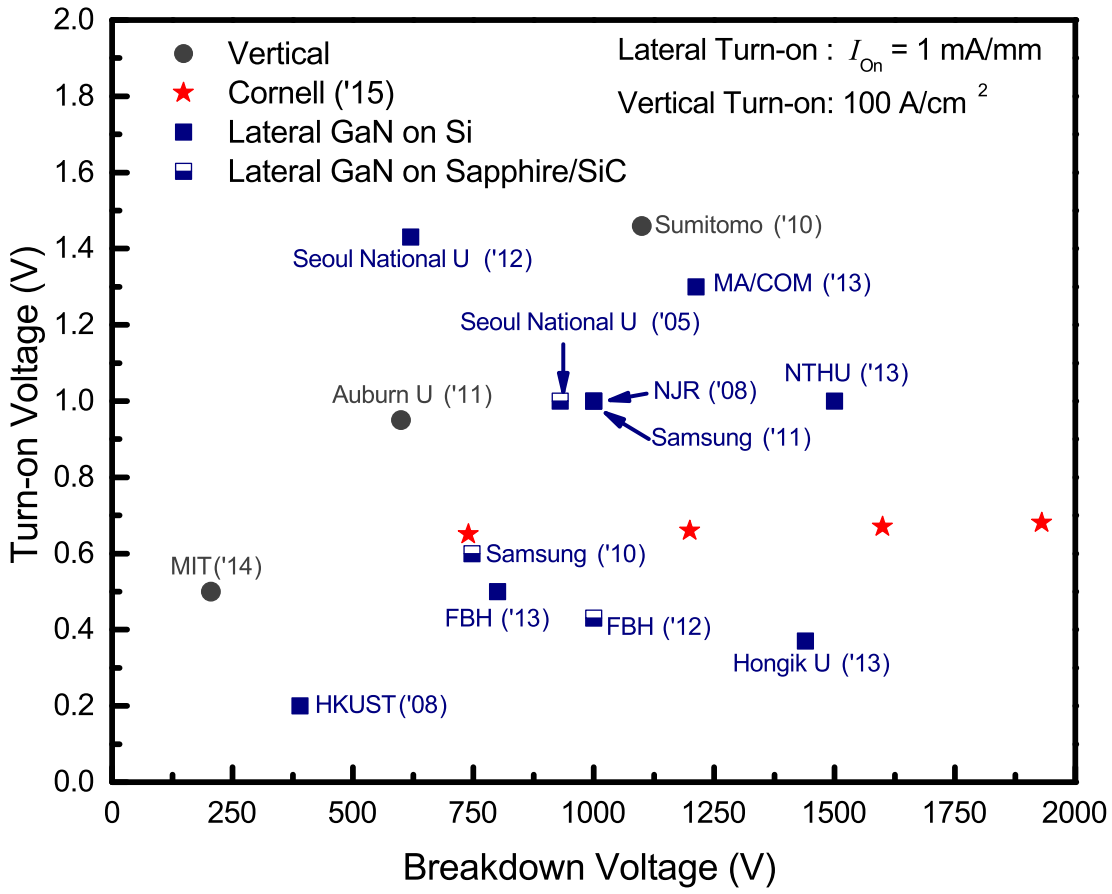

Figure 2.20: Benchmark plot of BV versus turn-on voltage among reported GaN SBDs. The turn-on voltage is extracted at a current density of 1 mA/mm for lateral diodes and 100 A/cm^2 for vertical diodes. The recessed SBDs with double field plate discussed in this work is labeled "Cornell '15".

To compare power devices of different types (diodes or transistors) and different geometries, the devices are benchmarked by their breakdown voltage and specific on-resistance. As there is a trade-off between breakdown voltage and on-resistance, the performance of power devices are fundamentally limited by the intrinsic material properties including critical electric field and carrier mobility. This material dependent limit is calculated by $R_{On} = BV^2/(\epsilon\mu E_{Cr}^3)$, where ϵ, μ and E_{Cr} are the dielectric constant, electron mobility and critical electric field, respectively. Assuming an electron

mobility of 500 cm^2/Vs and a critical electric field of 3.4 MV/cm, the GaN limit is plotted in Fig. 2.21. Fig. 2.21 also presents the benchmark of the fabricated recessed SBDs with double FP among the best reported GaN SBDs, including both lateral [77, 55, 78, 79, 80, 81, 82, 83, 45, 84, 85, 86, 87] and vertical SBDs [88, 73, 89, 76, 90]. All the references values in the benchmark plot have been re-calculated based on the reported data following the definition of absolute $R_{ON,SP}$ depicted in Fig. 2.14. In the benchmark plot, the recessed SBDs with double FP compare favorably to the state-of-the-art GaN SBDs on SiC and sapphire substrates. In comparison to previously reported GaN SBDs with recessed anode in direct contact to the 2DEG, the devices in this work show a $\approx$ 2X improvement in BV: 1900 V vs. 800 V for GaN-on-Si SBDs and 1900 V vs. 1000 V for GaN-on-SiC SBDs. The $R_{ON,SP}$-BV values of all these SBDs with recessed anode fall along the same FOM line representing the best achieved SBDs experimentally, which suggests the recess anode coupled with multiple FPs is a viable technology to achieve high performance GaN rectifiers.

The recessed SBDs are also benchmarked based on the differential on-resistance, as shown by the hollow symbols in Fig.2.21. Based on the differential $R_{ON,SP}$, the performance of the SBDs in this work is close to the GaN limit. By assuming an electron mobility of 1490 cm^2/Vs and a E_{Cr} of 1.5 MV/cm, a good fit between the experimental data and the $R_{ON,SP}$-BV model is achieved, as shown by the dash line in Fig. 2.21. Notice that the fitted critical electric field value is consistent with the effective breakdown field calculated based on a trapezoidal electric field distribution.

Given the advantage in terms of cost GaN-on-Si technology has over other substrates, the SBDs with recessed anode and double field plate structure has great potential for power electronic applications, which are highly sensitive to cost due to the continuous performance improvement in silicon based power devices.

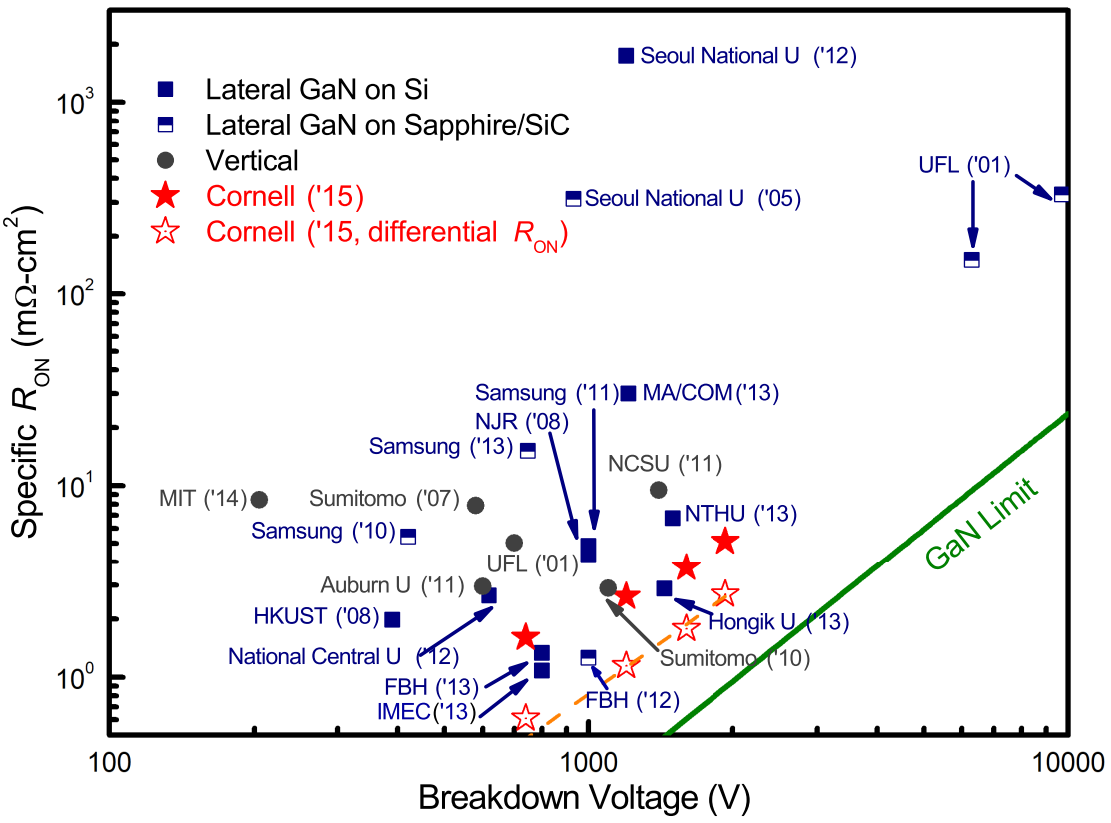

Figure 2.21: Benchmark plot of BV versus $R_{ON,SP}$. All the reference values are re-calculated based on the reported data following the definition of $R_{ON,SP}$ shown in Fig. 2.14 so that the diode turn-on effect is also taken into account, using I_{ON} = 100 mA/mm criteria. The differential RON of the diodes in this letter is also extracted (hollow stars) and modeled (dash line) assuming μ = 1490 cm^2/V · s and E_{Cr} = 1.5 MV/cm. The green line shows the FOM limit of bulk GaN using μ = 500 cm^2/V · s and E_{Cr} = 3.4MV/cm. The recessed SBDs with double field plate discussed in this work is labeled "Cornell '15".

2.6 Summary

In this chapter the development process of a high voltage lateral AlGaN/GaN Schottky barrier diodes (SBDs). The development is aimed at achieving SBDs with a low absolute on-resistance and yet a high breakdown voltage. Through iterations over several device generations, a lateral AlGaN/GaN SBD with a breakdown voltage of over 1.9 kV and a absolute on-resistance of 5.12 mΩ · cm^2 has been achieved. The power figure-of-merit calculated by $BV^2/R_{ON,SP}$ is 727 MW · cm^{-2}, showcasing a state-of-the-art performance.

This was the highest breakdown voltage achieved in GaN SBDs at the time of reporting. Based on the work presented here, Tsou *et al.* carried out further optimization of the fabrication and achieved an even higher breakdown voltage of 2.07 kV [91].

The key design features enabling such high performance include: a recessed anode where the anode metal and 2DEG are in direct contact and double field plate structure which effectively curbs the reverse leakage current and boosts the breakdown voltage. A lot of efforts also went into fabrication process optimization including selecting proper dielectrics for each field plate and the treatment of etched surface. The SBDs with record breakdown voltage are fabricated on GaN-on-Si wafer, which has a much lower wafer cost compared to GaN-on-SiC or GaN-on-sapphire wafers. The record high breakdown voltage demonstrates a promising performance on the GaN-on-Si platform as it continues to attract more research attention thanks to its low cost.

To make the high voltage AlGaN/GaN SBDs a viable commercial product, the improvements required include a further reduction of leakage current and full assessment of their reliability.

CHAPTER 3

GaN MESFETS AND ELECTRON MOBILITY IN GRADED AlGaN

3.1 Introduction

The most commonly adopted technique to achieve n-type doping in GaN is to incorporate Si as substitutional donors during material growth. However, it is also possible to introduce n-type doping in graded $Al_xGa_{1-x}N$ through polarization-induced internal electric field without involvement of intentional impurities (Pi-doping) [34, 35]. The mobility of electrons generated by polarization-induced doping in AlGaN has been previously studied at an electron concentration near 1.5×10^{18} cm^{-3} [48], a carrier concentration relevant to RF devices [49], showing that alloy and phonon scattering are the main scattering mechanisms while neglecting dislocation scattering.

In this chapter, the electron mobility in the Pi-doped AlGaN with a much lower electron concentration of $\sim 10^{17}$ cm^{-3} is studied, with an aim to implement polarization-induced doping in power electronic devices, where a low carrier concentration is desired: about 1×10^{15} to 1×10^{16} cm^{-3} [2] for unipolar drift regions as in metal-oxide-semiconductor field effect transistors (MOSFETs) or about 1×10^{17} cm^{-3} [51] for bipolar drift regions such as super-junctions. The electron mobility is extracted experimentally using the split C-V method by combining current-voltage (I-V) and capacitance-voltage (C-V) characterizations of a field effect transistor (FET). Theoretical calculations of the electron mobility, taking into account ionized/neutral impurity, phonon, charged dislocation and alloy scattering, are carried out and compared with the experimental data. The comparison reveals that for electron concentrations $< 1 \times 10^{17}$ cm^{-3} in both Pi-doped AlGaN and Si-doped GaN, the key to achieving a high electron mobility is to reduce dislocation density to $< 1 \times 10^{17}$ cm^{-2}. Pi-doped AlGaN is shown to have

an advantage in electron mobility over Si-doped GaN at high electron concentrations due to the absence of impurity scattering.

3.2 Epitaxial Layer Design and Characterization

The wafer in this study was grown by metalorganic chemical vapor deposition (MOCVD). The epitaxial growth started on a sapphire substrate with buffer layers, followed by an unintentionally doped (UID) semi-insulating Ga-face GaN with a thickness of 5 μm and a Pi-doped AlGaN with a thickness of t ~ 600 nm. Over this thickness, the Al composition was linearly increased from 0% to 20% toward the wafer surface. During the entire MOCVD growth, the Si precursor was not flown. The one-dimensional (1D) Poisson calculation incorporating polarization effects shows that a uniform electron concentration of $\rho_\pi \cong \frac{\rho_{surf}-\rho_{bulk}}{t} \cong 2 \times 10^{17}$ cm^{-3} is expected due to the spontaneous and piezoelectric polarization in $Al_xGa_{1-x}N$.

The secondary ion mass spectrometry (SIMS) scan of the sample shown in Fig. 3.1 confirms that the Al composition varies linearly from 20% at the surface to 0% at 600 nm depth. The SIMS measurement detection limits for various atoms are listed in the embedded table in Fig. 3.1. It shows that both Si and H levels measured in the sample are at their detection limits of the SIMS measurement, and an increase of C and O (unintentional impurities) with increasing Al composition is observed. The morphology obtained from atomic force microscope (AFM) shown in Fig 3.2 shows a very smooth surface after growth with a roughness root mean square (RMS) value smaller than 1 nm for both 2×2 μm^2 and 5×5 μm^2 scans. Clear atomic steps are also observed in the AFM image, indicating good crystal quality of the Pi-doped AlGaN, although pit-like features are also visible, which are often observed on AlGaN surfaces [92]. Electron transport

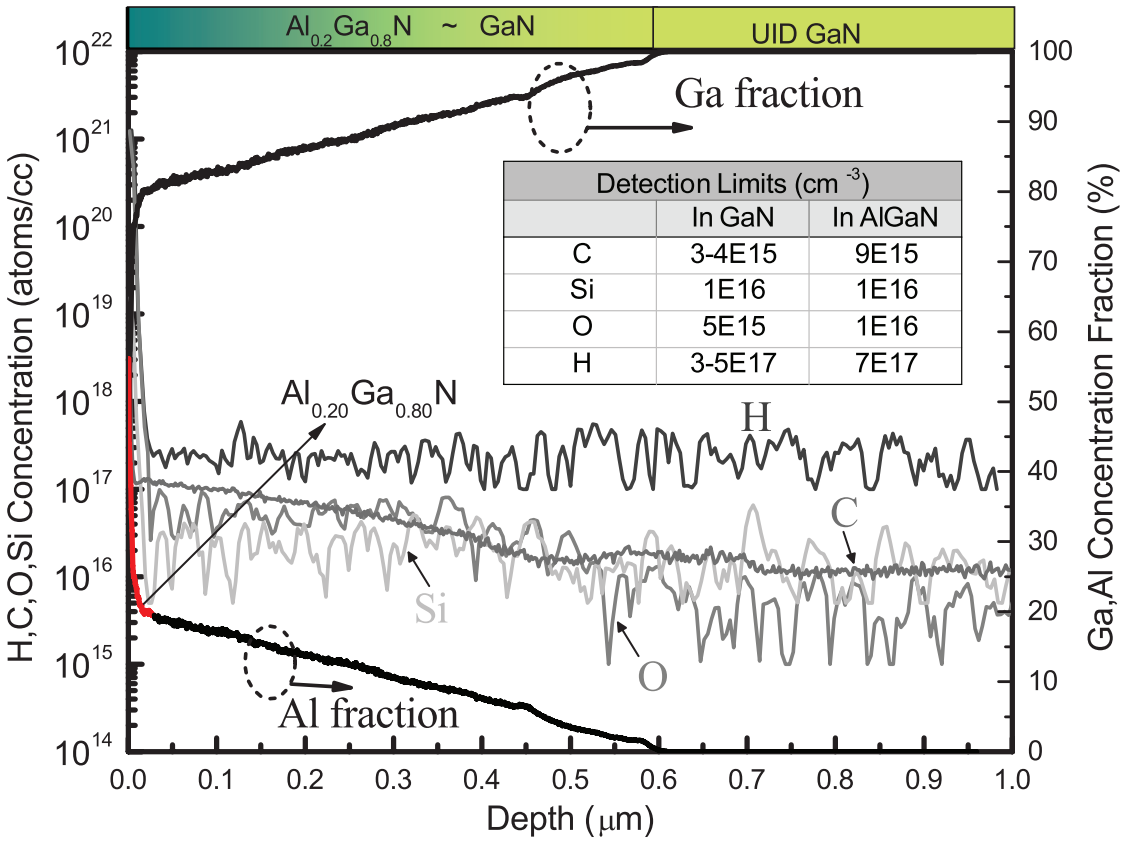

Figure 3.1: Impurity concentration (H, C, O Si) and Ga/Al composition profiles of the MOCVD grown Pi-doped AlGaN from secondary ion mass spectrometry (SIMS) measurement. The inset table shows the detection limits of the SIMS scan.

in Pi-doped AlGaN is characterized with Hall effect measurements at both room temperature (RT) and 77 K. The measured electron sheet concentration drops from 1×10^{13} cm^{-2} at RT to 5.9×10^{12} cm^{-2} at 77 K, while the electron mobility increases from 590 cm^2/Vs to 1540 cm^2/Vs at 77 K. Taking into account the surface depletion depth induced by an assumed surface barrier height of 1 eV, the electron bulk concentration is calculated to be 1.91×10^{17} cm^{-3} at RT and 1.17×10^{17} cm^{-3} at 77 K. Note that the surface depletion depth depends on the calculated bulk electron concentration, which in turn depends on the surface depletion depth. To get a self-consistent estimation of the bulk electron concentration, the following two equations are solved self-consistently through numerical methods.

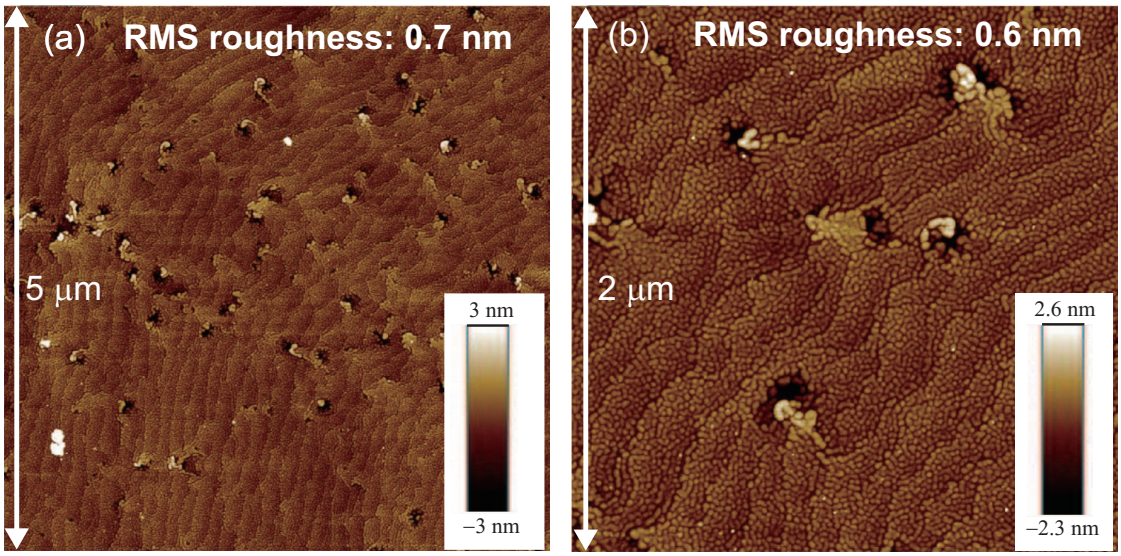

Figure 3.2: AFM images of 5×5 µm^2 and 2×2 µm^2 scan on the Pi-doped AlGaN. Clear atomic steps and smooth surface is observed.

$$n_{bulk} = \frac{n_s}{t_{total} - t_{dep}} \tag{3.1}$$

$$t_{dep} = \sqrt{\frac{2V_b\varepsilon_{GaN}}{qN_D}} \tag{3.2}$$

where n_{bulk} is the bulk electron concentration, n_s is the sheet charge density from Hall effect measurement, t_{total} is the total epitaxial layer thickness (extracted from SIMS), t_{dep} is the surface depletion depth, V_b is the surface barrier height, ϵ_{GaN} is the dielectric constant of GaN, and q is the electron charge.

Since carriers due to polarization-induced doping are activated by electric field, they are expected to exhibit a temperature independent behavior, as opposed to electrons thermally ionized from shallow donors like O that can be largely frozen out at 77 K, thus allowing an accurate measurement of the net polarization-induced doping concentration. The lower than expected carrier concentration of 1.17×10^{17} cm^{-3} at 77 K is attributed to the presence of compensating centers (e.g. C and Ga-vacancies) [93, 94]. To better

understand the origin of n-type doping, a time-dependent electron concentration model is built to interpret the experimental results. The electron concentration is calculated based on charge neutrality. Assuming an unintentional donor (Oxygen) concentration of $N_{\mathrm{D:O}}$ with an activation energy of $E_{A:O}$ along with an unintentional deep acceptor (Carbon) concentration of $N_{\mathrm{A:C}}$, the electron concentration is written as the following:

$$n_{bulk} = N_D^+ + p_{bulk} - N_A^- \approx N_\pi^+ + \frac{N_{D:O}}{1 + g_D e^{\frac{E_F - E_{D:O}}{kT}}} - N_{A:C}^- \tag{3.3}$$

In Eq. 3.3, n_{bulk} is the bulk electron concentration, N_D^+ is the total ionized donor concentration (Pi-doping and impurity doping), p_{bulk} is the bulk hole concentration, N_A^- is the ionized acceptor concentration, N_π^+ is the polarization-induced bound negative charge, g_D is the degree of degeneracy of the valence band, E_F is the Fermi level, k is the Boltzmann constant and T is temperature. Note that $N_{A:C}^-$ is temperature independent because the Fermi level is always above the C energy level in the temperature range of interest (77 - 300 K), thus C acceptors are ionized. N_π^+ is temperature independent due to its lack of requirement for thermal activation.

Through Joyce-Dixon approximation, the Fermi level can be written as:

$$E_F - E_C \approx kT[ln(\frac{n_{bulk}}{N_C}) + 2^{-3/2}(\frac{n_{bulk}}{N_C})] \tag{3.4}$$

where N_C is the effective conduction band density of states. By solving Eq. 3.3 and Eq. 3.4 self-consistently through numerical methods, the temperature dependent bulk electron concentration can be calculated. Similar models can be built for electron concentrations in Si-doped GaN with unintentional donors and acceptors.

In Fig. 3.3, assuming $N_{\mathrm{D:O}}$=6×10^{16} cm^{-3} with an activation energy of 34 meV [95] along with N_{A}=1 × 10^{17} cm^{-3} at mid-gap, the temperature-dependent electron concentration of the Pi-doped AlGaN is shown. For comparison, the electron concentration of

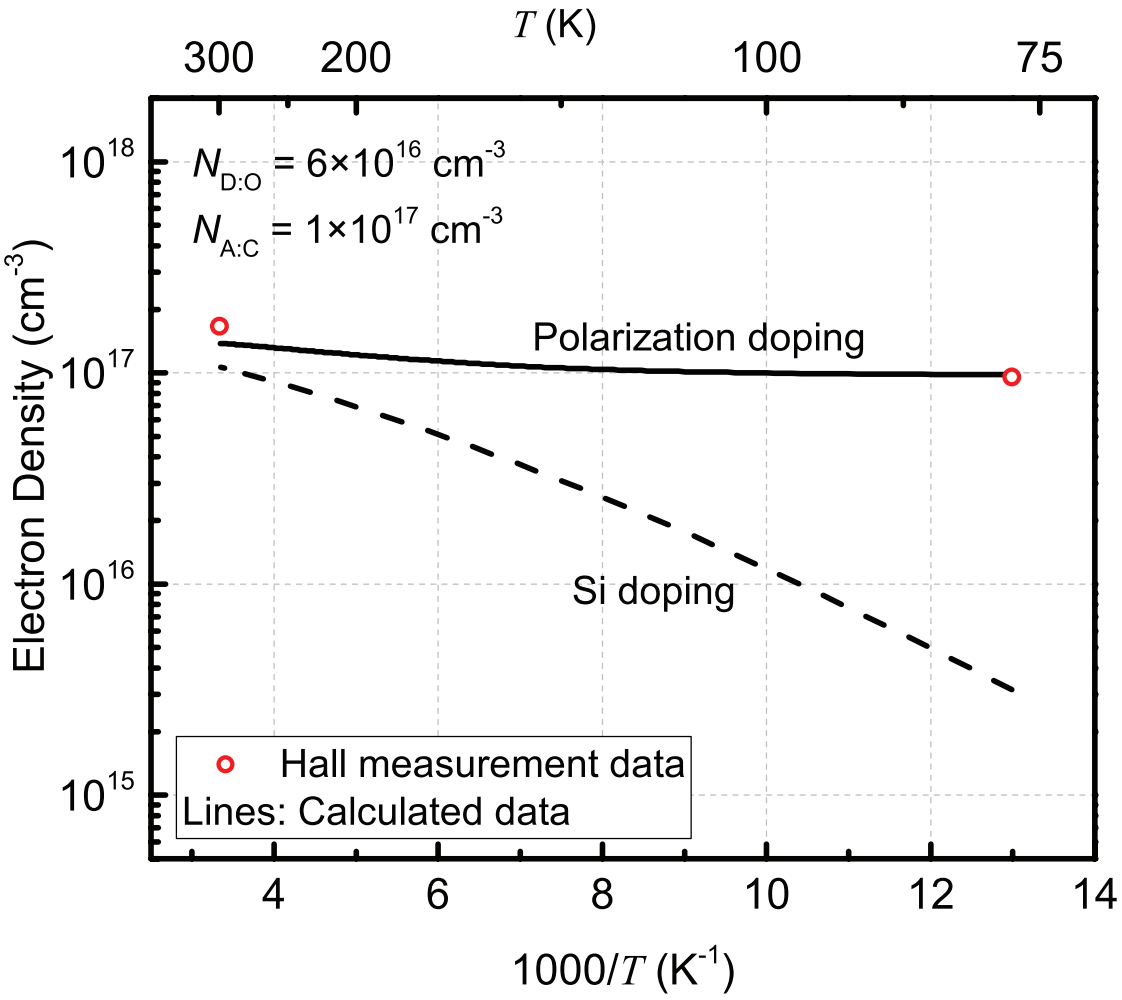

Figure 3.3: Electron concentration obtained from Hall effect measurements at RT and 77 K along with modeled electron concentration versus temperature for Pi-doped and Si-doped GaN, confirming electrons in the AlGaN are indeed induced by polarization doping.

GaN with a Si doping (GaN:Si) concentration of 2×10^{17} cm^{-3} and the same unintentional impurities is also modeled and shown. The plot shows a close match between the model and experimental data. It again confirms that Pi-doping is much more resistant to freeze-out despite the presence of unintentional impurity dopants and compensating centers.

To better understand the origin of electrons, the temperature-dependent electron and bound charge concentrations are plotted in Fig. 3.4 (left). It is noticed in Fig. 3.3

that at 77 K, the O donors are almost completely frozen out and $n_{bulk} = N_{\pi}^{+} - N_{A:C}^{-}$. This freeze-out effect is more severe than that in GaN with only O doping at the same concentration. This augmented freeze-out effect is due to the temperature-independent polarization-induced doping. As the temperature decreases, the Fermi level is mostly pinned close to the conduction band due to the polarization-induced doping, resulting in an even lower activation ratio of O donors compared to that in GaN with Si doping (of the same concentration). To illustrate the augmentation of the freeze-out effect, the comparison between the ionized O donor concentration in Pi-doped GaN with that in Si-doped GaN is shown in Fig. 3.4(right), both with an effective doping concentration of 2×10^{17} cm^{-3} and a compensator concentration of 1×10^{17} cm^{-3}. The ionized O donor concentration is increasingly much lower in Pi-doped GaN compared to Si-doped GaN, due to the pinning of the Fermi level.

The above analysis of the $Al_xGa_{1-x}N$ confirms the successful realization of Pi-doping at a low concentration $\sim 1 \times 10^{17}$ cm^{-3}, although the existence of unintentional donor and acceptor results in a temperature-dependent electron concentration.

3.3 The Role of C in Graded AlGaN

To understand the compensator energy levels in the graded $Al_xGa_{1-x}N$, we collaborated with Sandia National Lab to carry out deep-level optical spectroscopy (DLOS). The DLOS is carried out with Schottky barrier diodes fabricated with the graded $Al_xGa_{1-x}N$. For an accurate DLOS measurement, the fabricated SBDs should have a thin anode metal to allow light transmission to the underlying graded $Al_xGa_{1-x}N$. They also need to be of low reverse leakage current to allow accurate capacitance measurements, as DLOS is based on capacitance-voltage measurement.

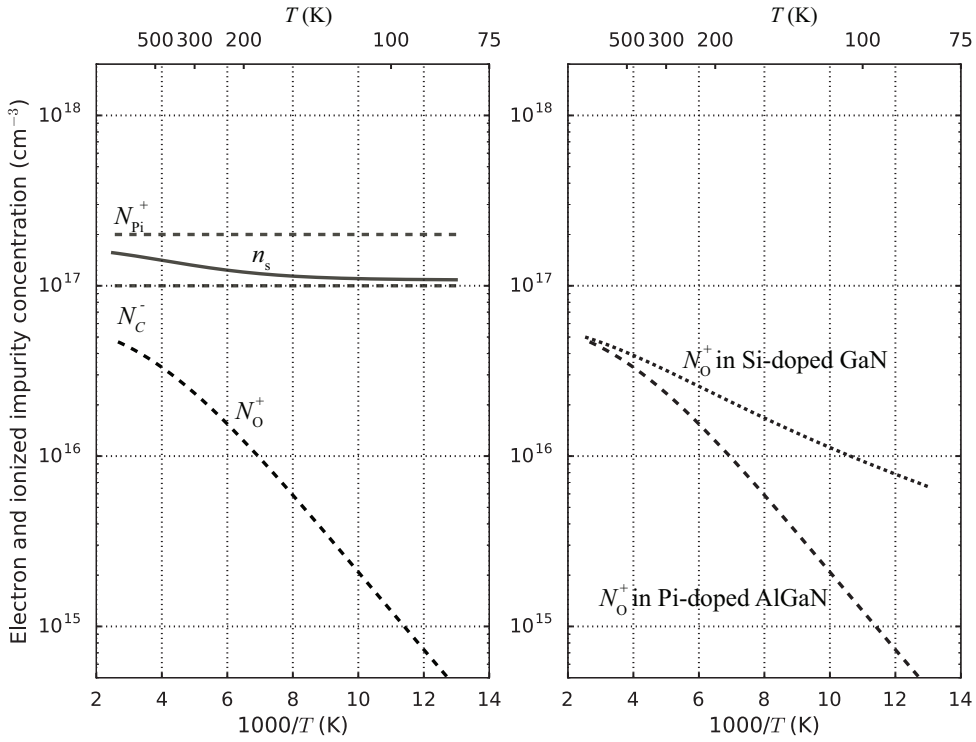

Figure 3.4: (left) Calculated electron and ionized impurity concentrations of the Pi-doped AlGaN. The C and O concentration is based on the SIMS scan. (b) Comparison of the ionized O impurity concentration versus temperature in Pi-doped AlGaN and Si doped GaN. An enhanced freeze-out effect of the O impurity is observed due to Pi-doping.

To meet these requirements, the SBDs are fabricated with MBE regrown contacts [75] with a 8 nm anode metal layer. The MBE regrown contacts eliminates the need of a high-temperature annealing process, which often results in defective oxide on the surface and consequently large leakage current in SBDs. The fabrication process starts with ohmic contact patterning and a dry etching of 50 nm, followed by MBE regrowth of n^+ GaN of 100 nm with a targeted Si doping concentration of 1×10^{20} cm^{-3}. The ohmic contact formation is then completed by depositing metal layers consisting of 40/100 nm Ti/Au with e-beam evaporator. The anodes are formed by depositing a Ni film with a thickness of 8 nm. The *I*-*V* characteristics of the fabricated SBDs are measured and plotted in Fig. 3.5. The reverse leakage current is as low as 1×10^{-11} A, with the

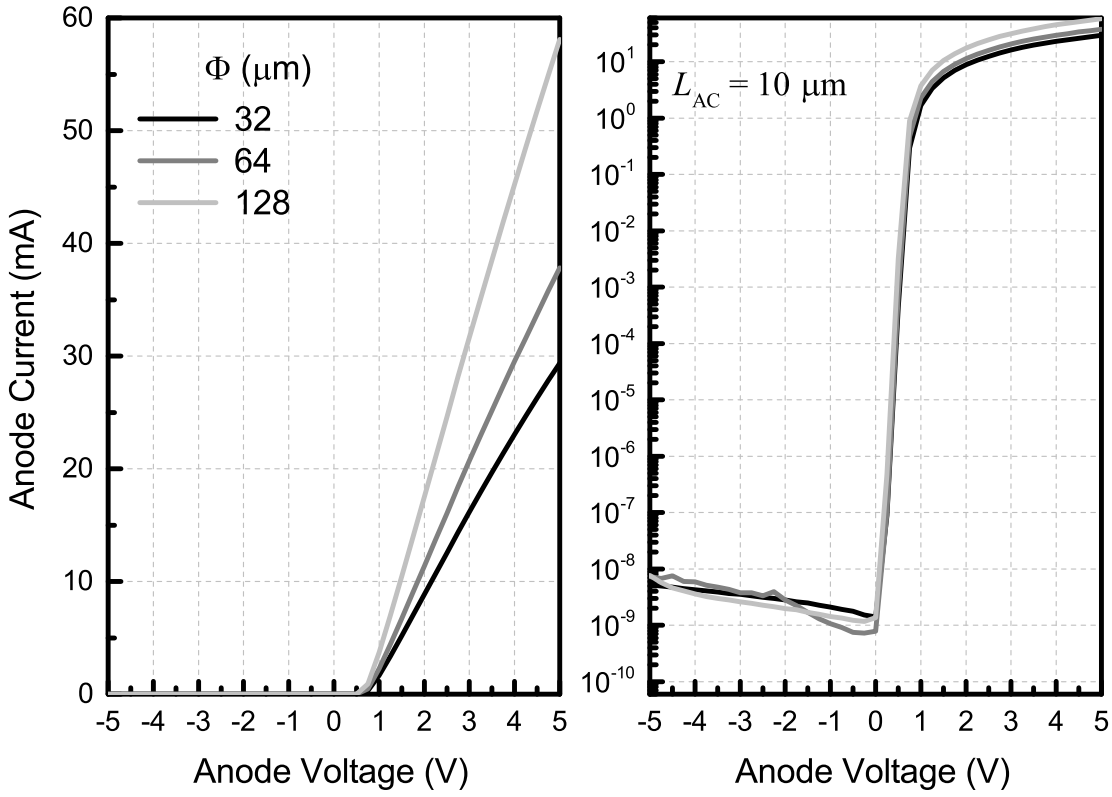

Figure 3.5: *I-V* characteristics of SBDs fabricated on the Pi-doped AlGaN, plotted in linear (left) and semi-logarithmic (right) scale.

anode diameters ranging from 32 to 128 μm. Such low leakage current ensures that the conduction through leakage current is negligible compared to the conductance through the capacitance during the capacitance measurement.

The optical cross sections are calculated with DLOS measurement results under 2 reverse bias voltages and plotted in Fig. 3.6. The 0.5 V and 5.7 V reverse biases correspond to depletion depths of 200 nm and 330 nm. DLOS is sensitive to the material from surface to the edge of depletion and weights the edge of depletion region more than the surface. The weighted average of Al composition under 0.5 V and 5.7 V reverse biases are calculated to be 17% and 14%, respectively. The photon energy at which the optical cross section starts to saturate in Fig. 3.6 corresponds to the apparent bandgap energy in the depletion region. A clear decrease of the apparent bandgap energy is observed as the

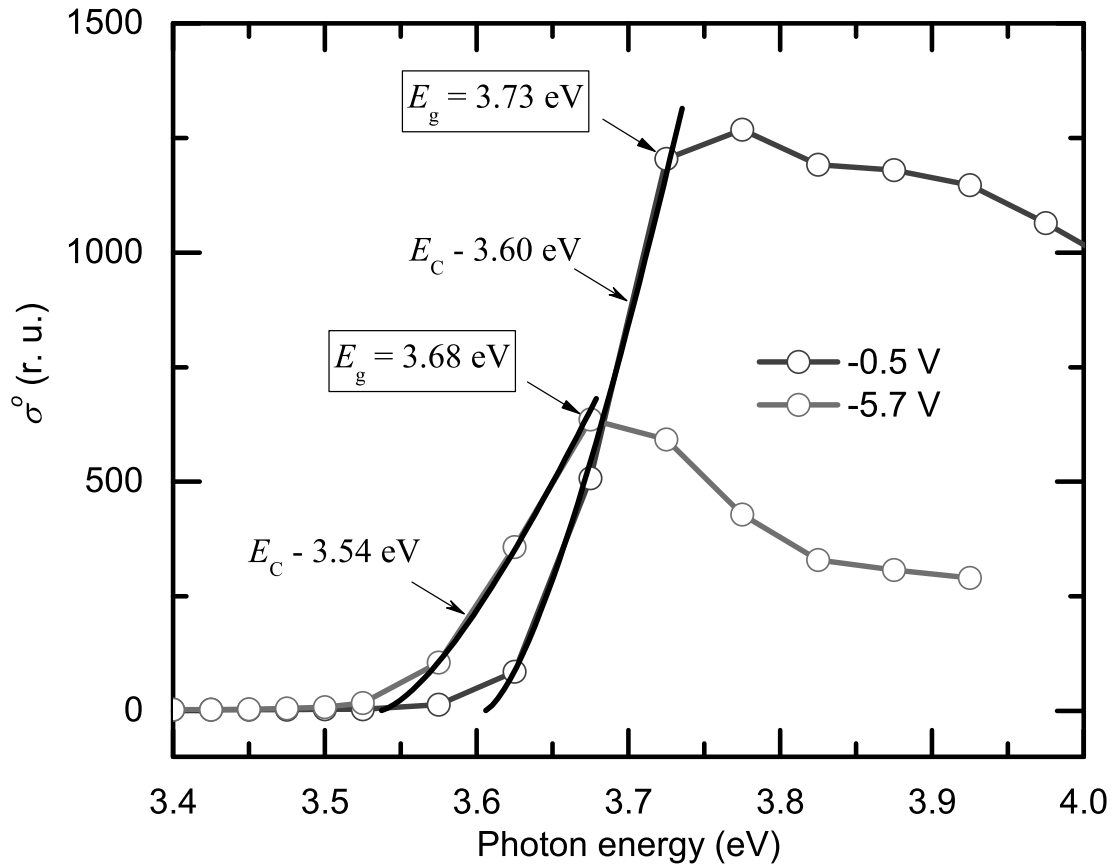

Figure 3.6: Extracted optical cross section spectrum plotted in linear scale. Compensator levels at $E_C - 3.54$ eV and $E_C - 3.60$ eV are revealed. [Courtesy of Dr. Andrew Armstrong at Sandia National Lab]

reverse bias voltages increases, due to the decrease of Al composition as the depletion region extends deeper into the epitaxial $Al_xGa_{1-x}N$ layer.

By fitting of the measured optical cross sections shown in Fig. 3.6, one can identity two compensator energy levels of $E_C - 3.54$ eV and $E_C - 3.60$ eV under 0.5 V and 5.7 V reverse biases. Two additional compensator energy levels, at $E_C - 2.1$ eV and $E_C - 3.1$ eV, are revealed when the optical cross section in semi-logarithmic scale in Fig. 3.7. The *C-V* measurement is performed under various incident photon energies to measure the compensator concentration at each of the energy level mentioned above in the Pi-doped $Al_xGa_{1-x}N$. The extracted electron concentration under various incident

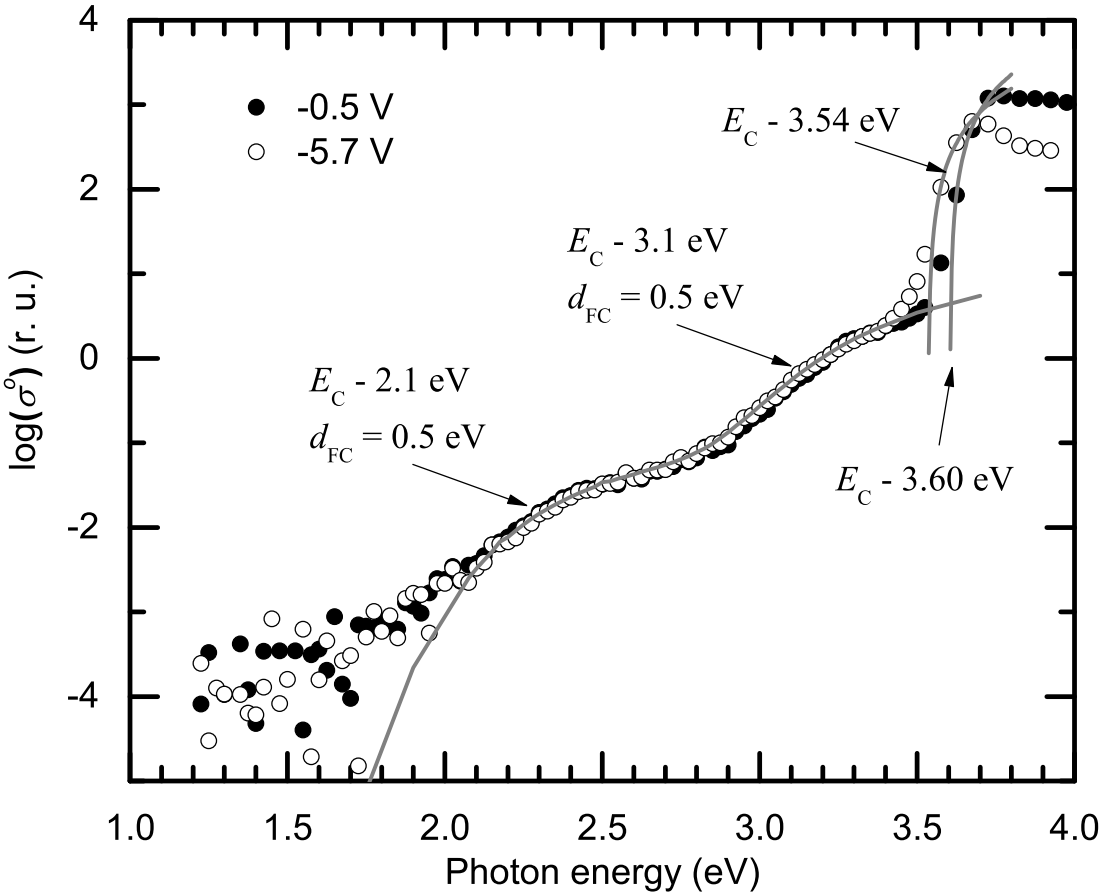

Figure 3.7: Extracted optical cross section spectrum plotted in semi-logarithmic scale. Additional trap levels at $E_C - 2.1$ eV and $E_C - 3.1$ eV are revealed. [Courtesy of Dr. Andrew Armstrong at Sandia National Lab]

photon energies are plotted in Fig. 3.8. The compensator concentration at energy level of $E_C - 3.54$

/3.60 eV, $E_C - 3.1$ eV and $E_C - 2.1$ eV are calculated to be 5.7×10^{16} cm^{-3}, 3.1×10^{16} cm^{-3} and 2.5×10^{15} cm^{-3}. The summation of the compensator concentrations comes to be 0.9×10^{17} cm^{-3} which is close to the 1×10^{17} cm^{-3} level observed in the SIMS measurement. This shows that C impurities in n-type Pi-doped $Al_xGa_{1-x}N$ acts as deep acceptors. It can take different energy level, all of which are below the mid-gap. This lower-than-mid-gap energy levels make the C compensators all ionized as long as the $Al_xGa_{1-x}N$ remains n-type. The results show that to further reduce the effective bulk

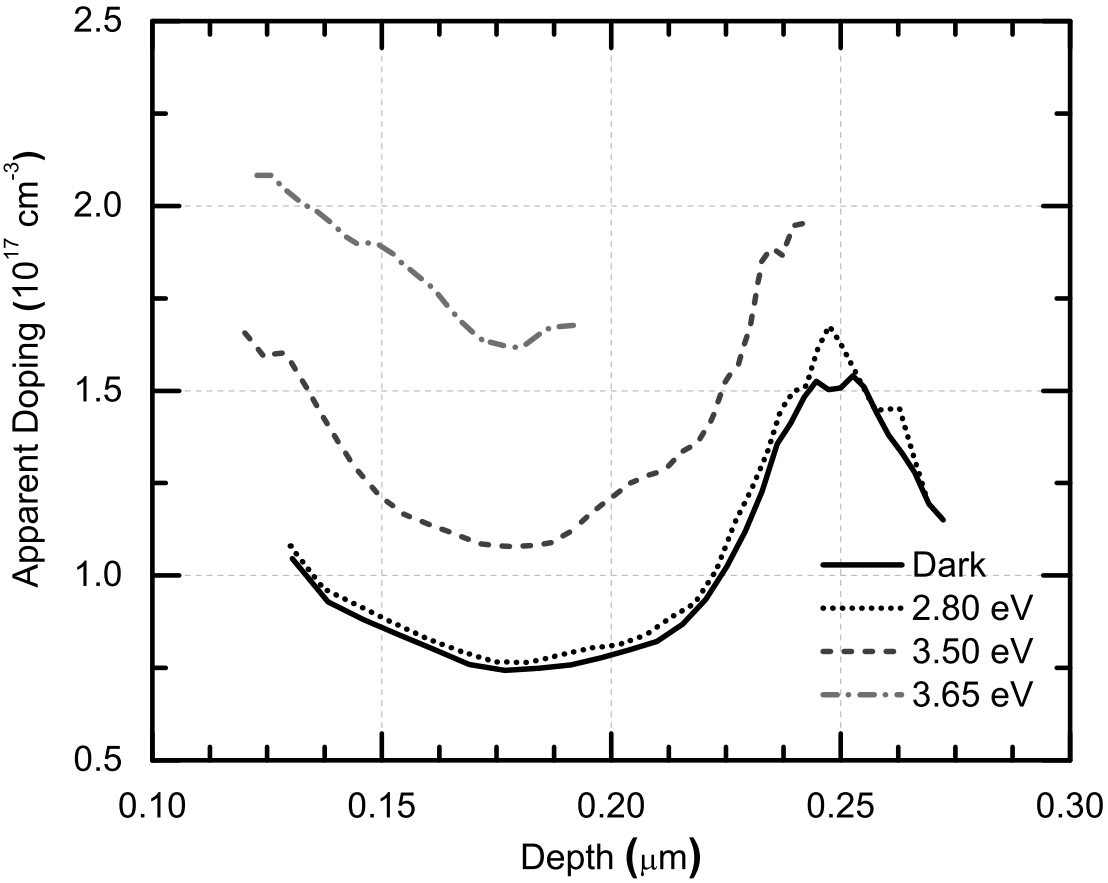

Figure 3.8: Extracted apparent doping concentrations of the Pi-doped $Al_xGa_{1-x}N$ under different lighting conditions. [Courtesy of Dr. Andrew Armstrong at Sandia National Lab]

Pi-doping concentration without severe compensating effects, it is crucial to reduce the unintentional C impurity concentrations

3.4 GaN MESFET Fabrication and Characterization

Metal-semiconductor FETs (MESFETs) were fabricated on the Pi-doped AlGaN sample to further characterize electron transport properties. The process flow includes source/drain ohmic contacts formation, mesa device isolation with Cl2-based inductive-coupled-plasma dry etching, followed by gate metal deposition of Ni/Au. Due to the rel-

atively low doping concentration and high energy bandgap of $Al_{0.2}Ga_{0.8}N$ at the surface, it is difficult to achieve good ohmic contacts with only metal deposition. Two ohmic contact techniques are explored, metal alloy and MBE regrowth of n^+ GaN. The process for realizing ohmic contacts with metal alloy include the deposition of a metal stack consisting of 20/100/40/40/ nm Ti/Al/Ni/Au by e-beam evaporator and a rapid thermal annealing (RTA) process at 890 °C for 18 s. To form ohmic contacts through MBE regrowth, the samples is first patterned and etched, followed by a low-power Cl_2 based dry etching of the $Al_xGa_{1-x}N$ with a etching depth of 50 nm. Then a selective regrowth of 100 nm n^+ GaN is carried out by MBE. The ohmic contact formation is completed with a metal deposition of 40/100 nm Ti/Au. Both techniques are standard processes for forming ohmic contacts in fabricating GaN based HEMTs, where the ohmic metal is separated from the two-dimensional electron gas by a AlGaN or InAlN layer. Ohmic contacts are successfully realized with both techniques with similar contact resistance. However, the MESFETs fabricated with different ohmic contacts show quite different characteristics.

The comparison of measured I_D-V_G characteristics of the MESFETs fabricated with alloyed and MBE regrown contacts are plotted in Fig. 3.9. The semi-logarithmic plot on the left shows that the MESFET with MBE regrown contacts has a 100 times smaller off-sate drain leakage current and >1000 times smaller gate leakage current compared to MESFETs with alloyed contacts. This is likely due to the exposure of sample surface to O_2 during the RTA process. It has been reported that the high temperature RTA process often results in a defective oxide layer on AlGaN/GaN surface [5], causing an increase in gate leakage current and current dispersion in GaN based HEMT fabrication. MBE regrown contacts eliminate the problem as the sample is not exposed to O_2 at a high temperature. The low leakage currents achieved with MBE regrown contacts render an On/Off ratio > 10^5. This low leakage current ensured that the accuracy of the

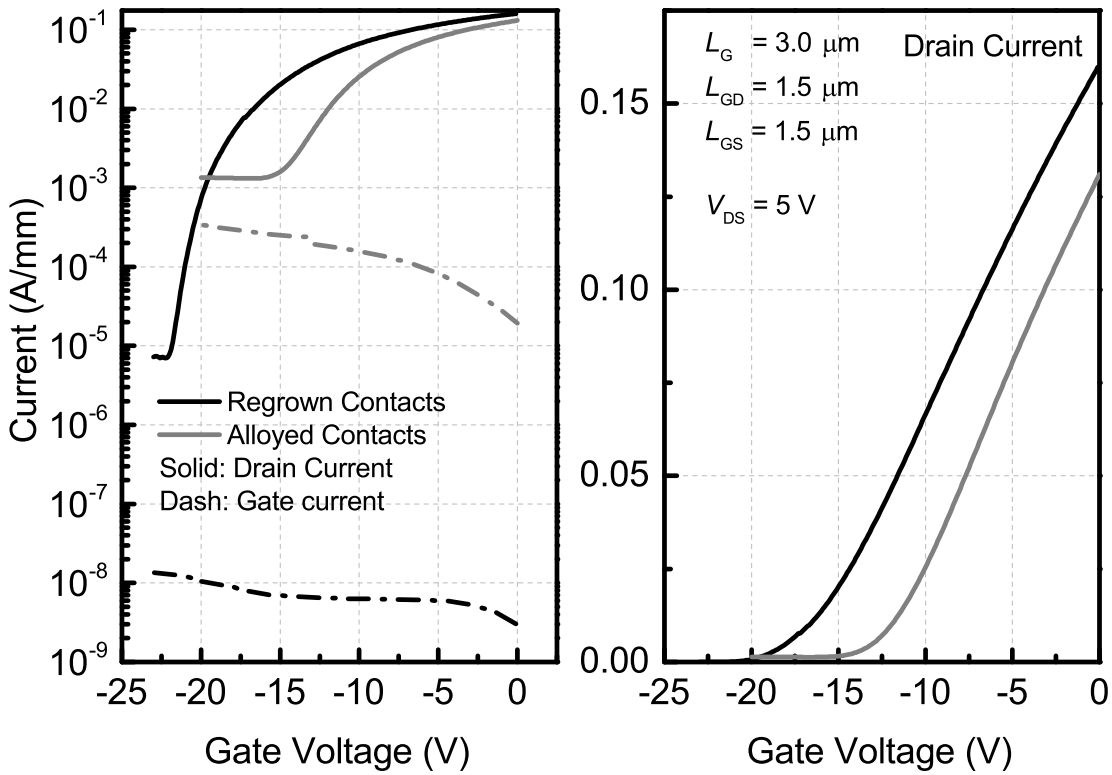

Figure 3.9: Comparison of the transfer *I*-*V* curves of the fabricated MESFETs on the Pi-doped AlGaN with MBE-regrown contacts and alloyed contacts.

capacitance measurement is not distorted by the in-phase conduction. In addition to the leakage current difference between MESFETs with alloyed and MBE regrown contacts, the pinch-off voltage is also observed to be quite different as seen in the linear plot of the I_D-V_G characteristics. This could be due to interface charge in the defective oxide formed on the surface of MESFETs with alloyed contacts. The comparison of I_D-V_D characteristics of MESFETs with alloyed and MBE regrown contacts is shown in Fig. 3.10. Both devices show a well-behaved drain current saturation, while the MESFET with MBE regrown contacts has a higher on-current compared to that with alloyed contacts. The drain saturation current at V_{GS} = 0 V for the MESFET with MBE regrown contacts exceeds 0.2 A/mm. These *I*-*V* characteristics consistent with classic MESFET models makes it possible to extract the electron mobility in Pi-doped $Al_xGa_{1-x}N$.

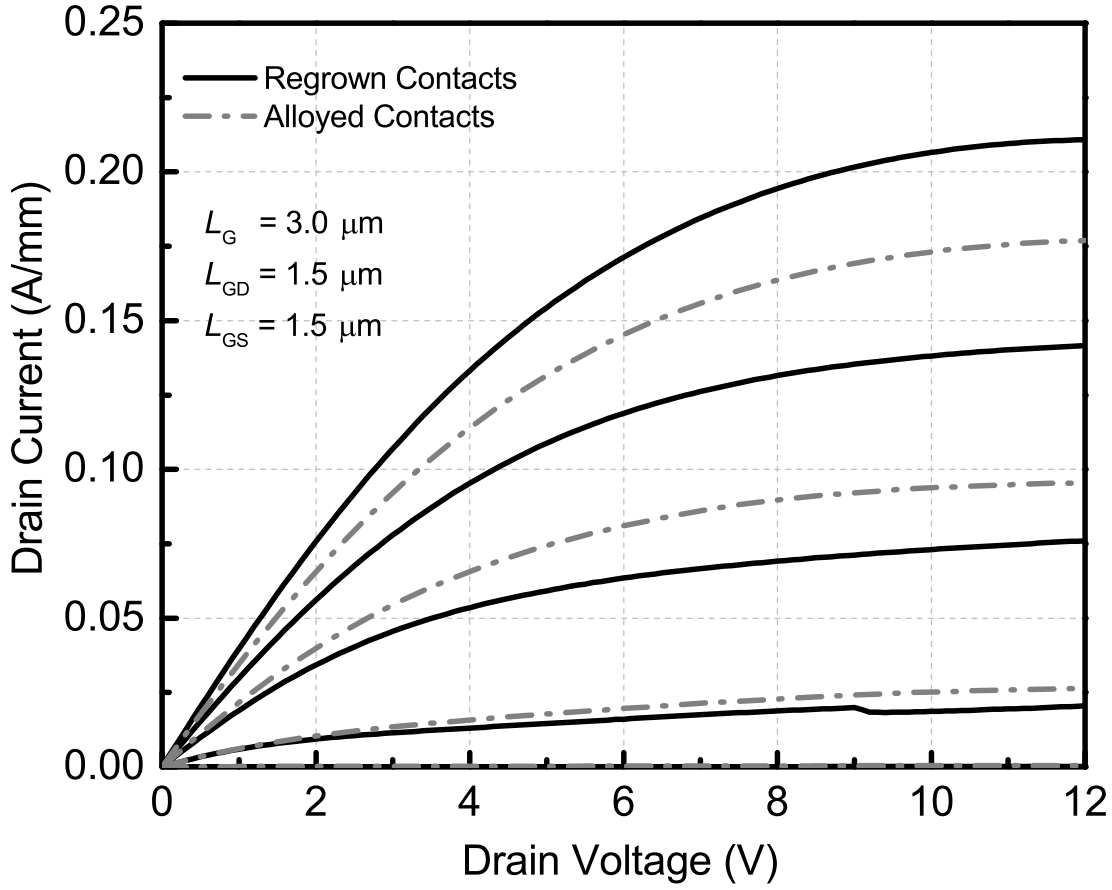

Figure 3.10: Comparison of the family *I*-*V* curves of the fabricated MESFETs on the Pi-doped AlGaN with MBE-regrown contacts and alloyed contacts.

3.5 Electron Mobility Characterization with MESFET

The extraction of electron mobility is carried out by a combination of Capacitance-Voltage (*C*-*V*) measurement and *I*-*V* measurement. The starts with the extraction of electron concentration profile and depletion depth through the *C*-*V* measurement. Then the electron mobility is calculated with the measured *I*-*V* along with the electron concentration and depletion depth.

The C-V measurements were carried out at RT on the MESFETs with source/drain electrically grounded. The measurements are performed by the integrated C-V meter in

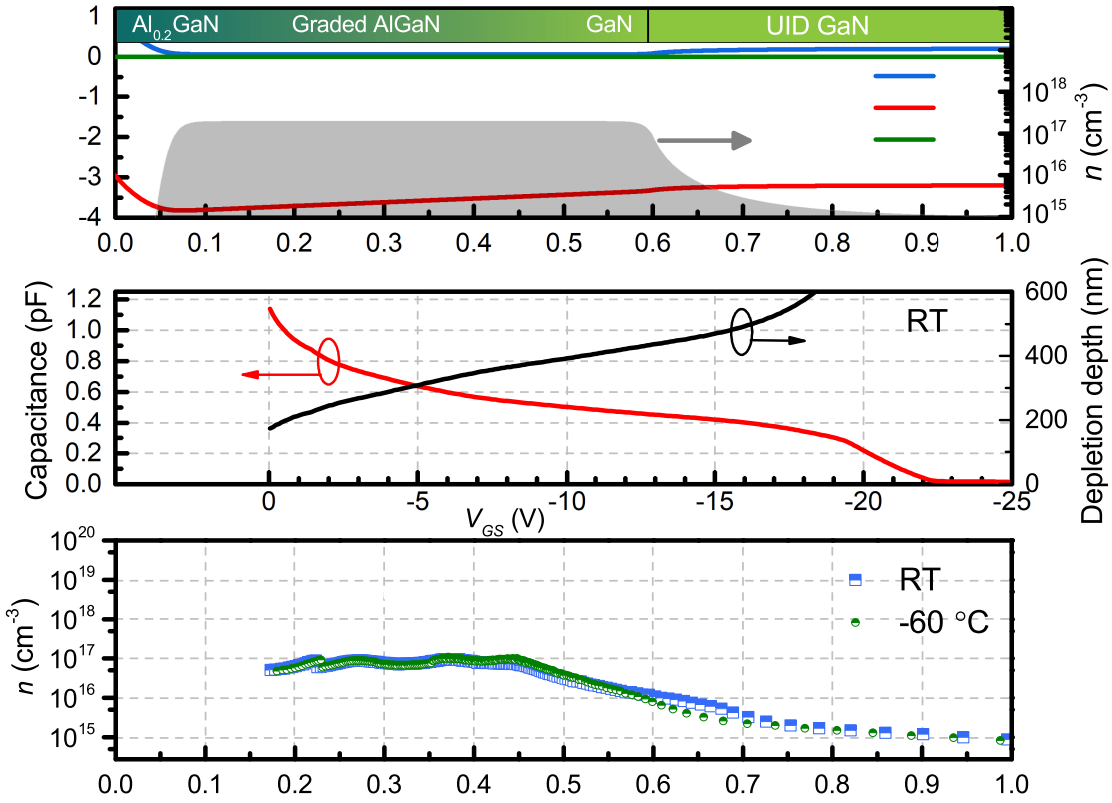

Figure 3.11: (top) Energy band diagram and electron concentration profile along the epitaxial growth direction from 1-D Poisson simulations. (middle) Capacitance/depletion depth as a function of VGS from C-V measurements of the MESFET. (bottom) Extracted doping concentration profile at RT and -60 °C.

Keithley 4200-SCS semiconductor characterizing system. The effective carrier concentration profile was then extracted by calculating the derivative of $1/C^2$, which is plotted in Fig. 3.11 along with the electron energy band diagram and the electron concentration from the 1D Poisson simulation, the *C-V* result and the depletion depth as a function of V_{GS}. The experimentally extracted doping profile shows a concentration around 10^{17} cm^{-3} up to 450 nm deep in the sample followed by a decrease. At 600 nm below the surface, the effective doping concentration drops to $\sim$ 10^{16} cm^{-3}, indicating that the depletion region in *C-V* measurement has reached the UID GaN layer underneath the Pi-doped AlGaN. No freeze-out effect is observed when the C-V measurement is conducted at $-60\,^{\circ}$C compared to RT. The effective doping concentration of $\sim$ 10^{17} cm^{-3}

is about 2 times smaller than the expected 2×10^{17} cm^{-3} from 1D Poisson calculations, which, as pointed out in the Hall effect measurement and DLOS analysis, is most likely due to compensation effects from C incorporated in the epitaxy.

With the C-V measurement results and DC characteristics of the MESFET, electron low-field mobility could be extracted under the gradual channel approximation, i.e. the split C-V method. The circuit model used for mobility extraction is shown in Fig. 3.12. For better accuracy of the split-CV method, the contact resistance as well as the resistance from the access regions are accounted for using the results from transfer length method (TLM) measurements. The DC characteristics were carried out with a 20 µm long gate under a low drain to source voltage V_{DS}=0.1 V, corresponding to an effective electric field of ~50 V/cm, to minimize impact of non-uniform electric field along the FET channel, which is particularly important near the FET pinchoff. The drain current can be written as:

$$I_D(V_{GS}) = \int_{dep(V_{GS})}^{(600\ nm)} n(x) q \mu(x) E_{channel} dx \tag{3.5}$$

where V_{GS} is the applied voltage between gate and source, dep is the depletion depth which is extracted from C-V results, $E_{channel} = \partial V / \partial y$ is the lateral electric field in the channel calculated from the voltage drop across the channel region, $n(x)$ and $\mu(x)$ are the effective doping concentration and the electron mobility at the depth x. $n(x)$ can be extracted from C-V results as shown in Fig. 3.11 (c). Taking the derivative with respect to V_{GS} on both sides of Eq. 3.5:

$$\mu(dep(V_{GS})) = -\frac{d(I_D(V_{GS}))}{dV_{GS}} \frac{1}{W_G \times n(dep(V_{GS})) \times q \times E_{Channel}} \left(\frac{d[dep(V_{GS})]}{dV_{GS}}\right)^{-1} \tag{3.6}$$

where all quantities except the electron mobility are either directly measured, or calculated from I-v or C-V measurement data. With the temperature-dependent DC characteristics and C-V results, the electron field effect mobility profile can be extracted, which

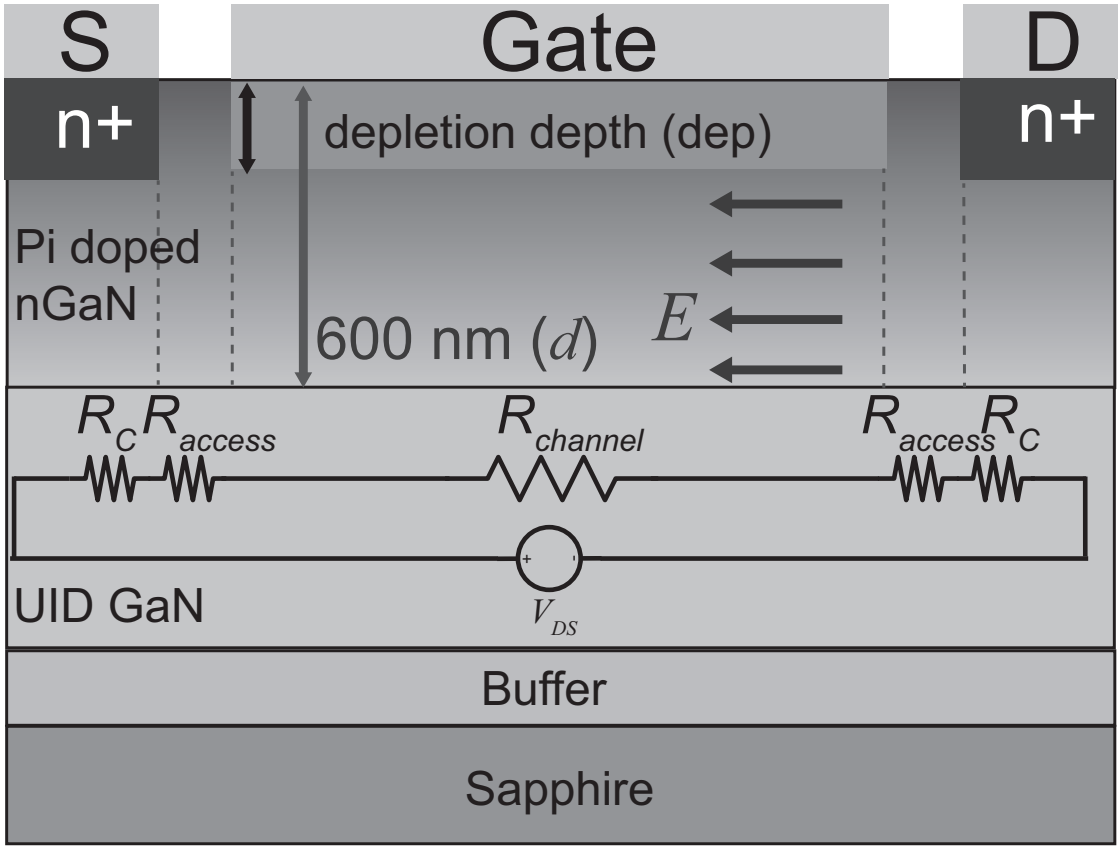

Figure 3.12: Cross section schematic of the fabricated MESFET and the equivalent circuit for electron mobility extraction.

is shown in Fig. 3.13 (a). The electron mobility increases with increasing depth, which is expected since alloy scattering reduces in the lower Al composition layers. Beyond 450 nm depth, the electron mobility starts to decrease due to the decreasing electron concentration thus reduced screening of dislocation scattering, as will be explained in the next section. Another trend shown in Fig. 3.13 (a) is the increase of mobility as the temperature decreases, which is a result of the decrease in phonon scattering [50]. The average mobility weighted by the electron concentration is calculated by:

$$\mu_{average} = \frac{\int_{dep(0)}^{600\ nm} n(x)\mu(x)dx}{\int_{dep(0)}^{600\ nm} n(x)dx} \tag{3.7}$$

The maximum and average electron mobility values are shown in Fig. 4 (b). At RT the extracted electron field mobility ranges from 500 cm^2/Vs to 901 cm^2/Vs, with an

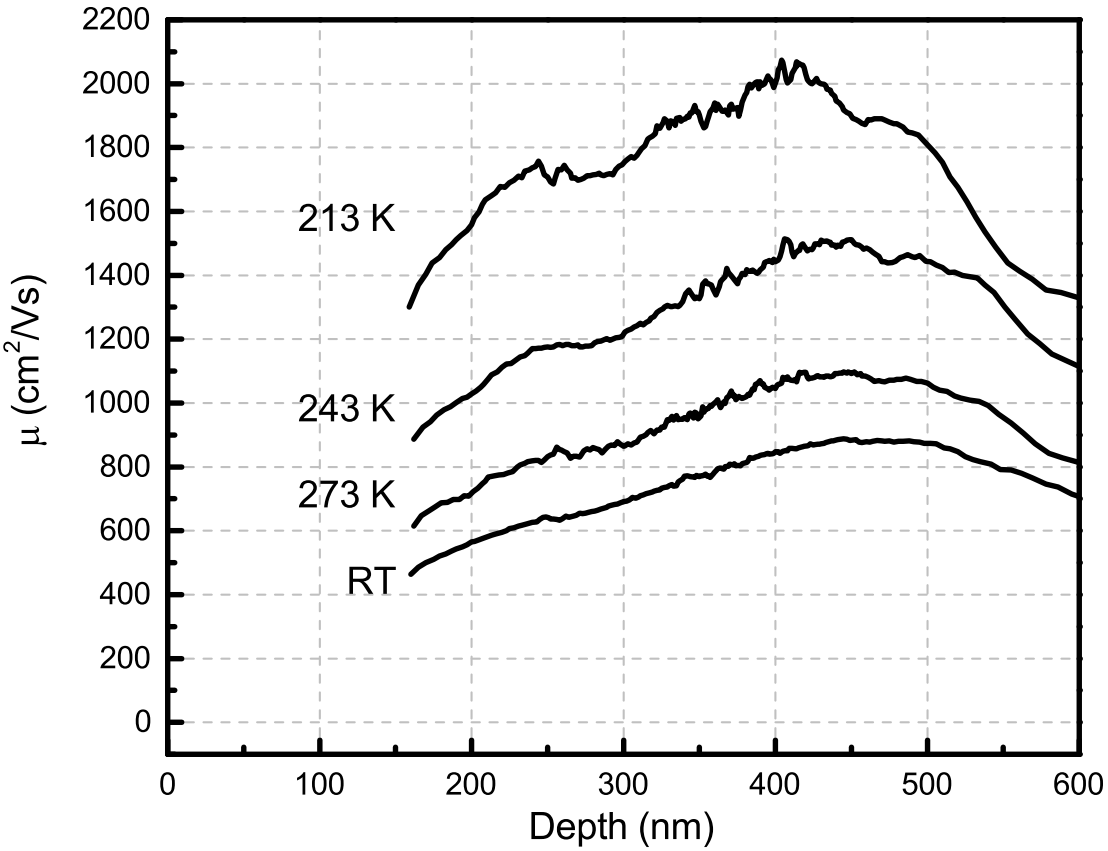

Figure 3.13: Extracted electron mobility as a function of depth from the sample surface at various temperatures.

average mobility of 724 cm^2/Vs. In comparison, the best electron Hall mobility reported in Si doped GaN grown on sapphire substrates with a similar electron concentration is 830 cm^2/Vs at RT [96]. This suggests that the average electron field mobility in Pi-doped AlGaN is comparable to that in Si doped GaN with comparable defect densities near a doping concentration of 10^{17} cm^{-3}. The monotonic increase in both average and maximum electron mobility as temperature decreases is observed in Fig. 3.13(b), with the maximum mobility at 213 K exceeding 2000 cm^2/Vs. The extracted mobility of 900 cm^2/Vs at n~ 10^{17} cm^{-3} in Pi-doped $Al_{0.07}GaN$ is among the highest mobility obtained in n-$Al_{0.07}GaN$ at a similar doping level.

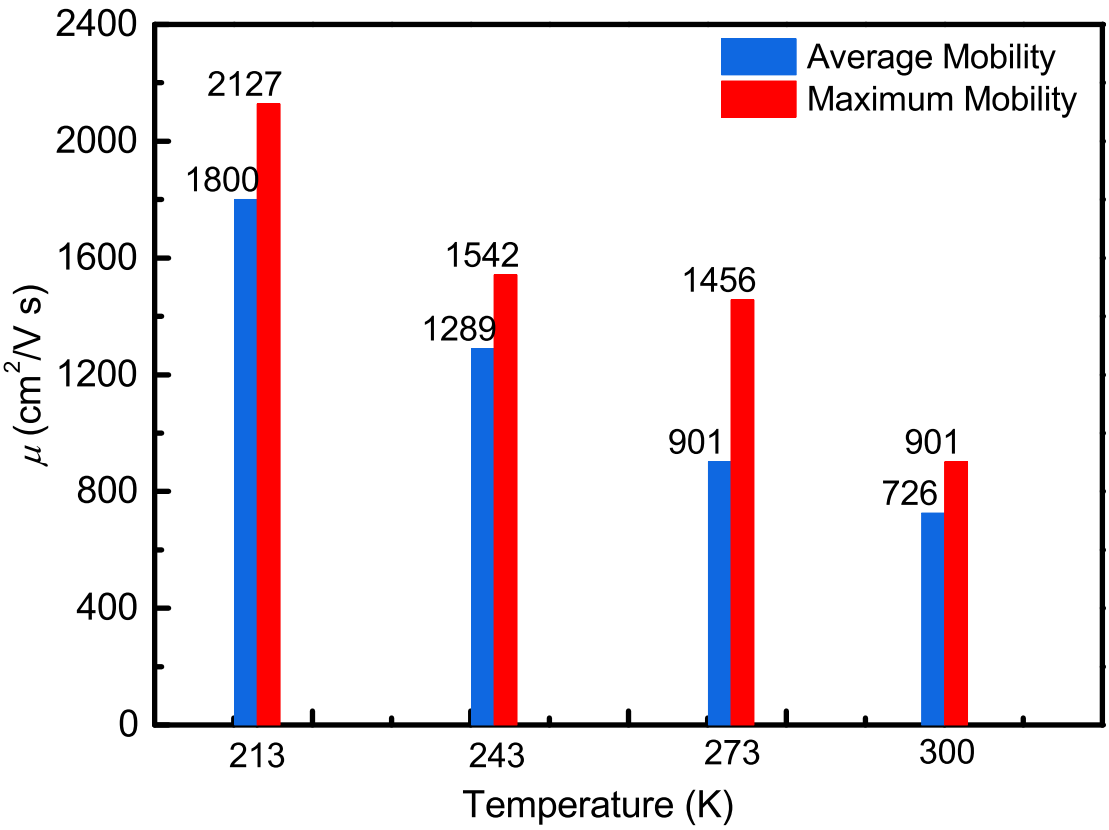

Figure 3.14: Average/maximum electron mobility extracted in the Pi-doped AlGaN versus temperature.

3.6 Modeling of Electron Mobility in AlGaN with Polarization-Induced Doping

To understand the limiting factors of electron mobility in Pi-doped AlGaN, a RT electron mobility model is constructed [97, 36], taking into consideration acoustic and optical phonon scattering, alloy scattering, ionized/neutral impurity scattering as well as dislocation scattering [98, 99]. For improved accuracy, the Al composition and impurity densities of carbon and oxygen from the SIMS measurement, the electron concentration from the C-V measurements are employed in the mobility modeling shown in Fig. 3.15. A dislocation density of 10^9 cm^{-2} is used, which is typical in GaN on sapphire;

since not all dislocations are charged and charged dislocations induce a higher scattering rate, a charge occupation probability also needs to be determined. A good fit using a charge occupation probability of 55% was found between the measured and calculated mobility, as shown in Fig. 3.15; therefore, this value is used throughout all the modeling in this work and the unoccupied dislocations are treated as neutral impurities. The electron component-mobilities limited by various scattering mechanisms for $Al_{0.07}GaN$ (peak mobility observed in this work) with a dislocation density of 10^9 cm^{-2} are modeled and plotted in Fig. 3.16 along with the total electron mobility calculated using the Matthiessens rule; impurity scattering off carbon and oxygen is neglected in Fig. 3.16 in order to delineate the effect of dislocation scattering. Experimental data from this work and Ref. are also plotted for comparison. It is seen that dislocation scattering is the only scattering mechanism that has a significant electron concentration dependence; dislocation-scattering-limited electron mobility decreases with decreasing electron concentration due to weakening of the screening effect at lower electron concentrations. The effect of dislocation scattering can be understood as follows: charged dislocations scatter carriers largely like ionized impurities; a scatter-center volume concentration induced by charged dislocations can be estimated by $N_{\rm dis}/c$ 10^9 $cm^{-2}/0.5$ nm $= 2 \times 10^{16} cm^{-3}$, where N_{dis} is the dislocation density and c is the unit cell height of GaN along the [0001] direction. For $n \gg N_{dis}/c$, the effect of dislocations is sufficiently screened, as in the $Al_{0.15->0.07}GaN$ layer in this work ($\sim 10^{17}$ cm^{-3}) and Ref. ($\sim 10^{18}$ cm^{-3}); for $n \leq N_D/c$, dislocation scattering is not negligible, thus leading to lower mobility in the $Al_{0.07-¿0}GaN$ layer. If dislocation scattering were neglected, on the other hand, the calculated mobility at low carrier concentrations would be much higher, as is the case presented in Ref. . It is also believed that in Ref. a large error is associated with the experimental extraction of the mobility in the $Al_{0.07-¿0}GaN$ layer since it was extracted near the FET pinchoff but a constant current thus a high applied field was used in calculating the carrier mobility.

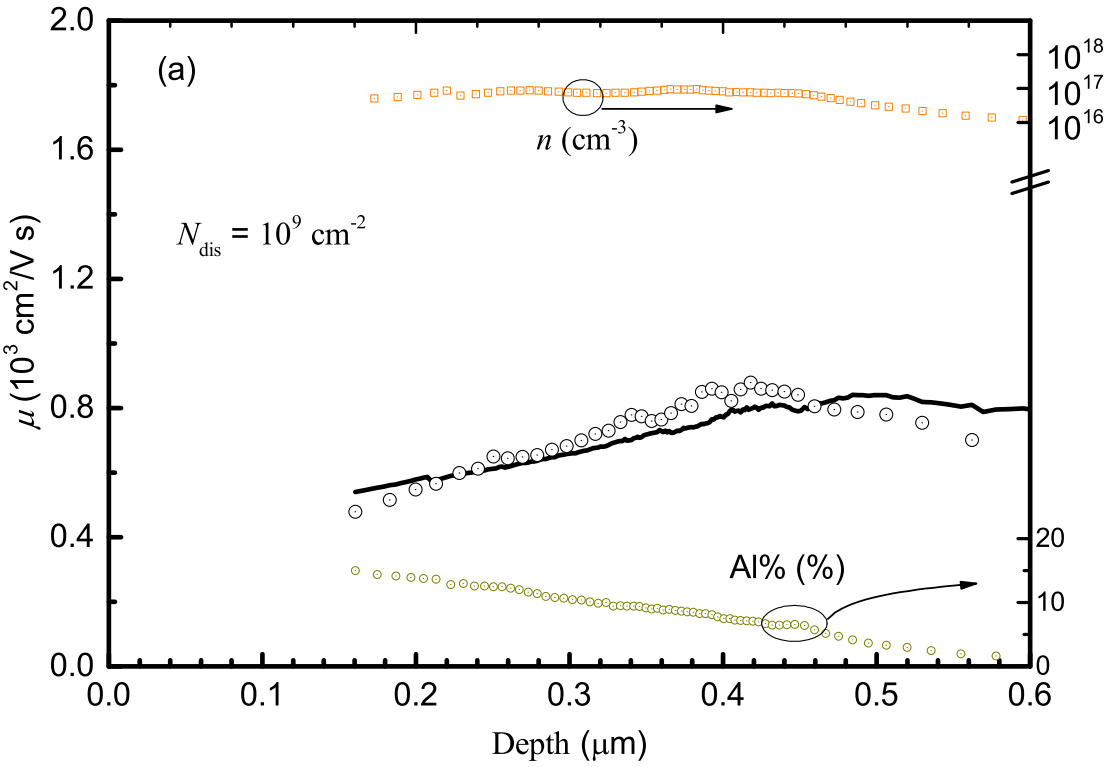

Figure 3.15: Experimentally extracted and calculated electron mobility for the Pi-doped AlGaN as a function of depth from the sample surface along with the measured Al composition and electron concentration. The calculations take into account optical phonon scattering, alloy scattering, dislocation scattering, impurity scattering with the Al, Si and C concentrations all determined from SIMS.

To further illustrate the impact of dislocations in Pi-doped and Si-doped n-GaN, the theoretical electron mobility for Pi-doped AlGaN is plotted in Fig 3.17 as a function of electron concentration with two dislocation densities and at two Al compositions. The modeled electron mobility in Pi-doped $Al_{0.05}GaN$ is then compared with Si-doped GaN, shown in Fig. 3.18. In these models, all the aforementioned scattering mechanisms are considered; however, impurity scattering is excluded in Pi-doped AlGaN assuming an ideal epitaxy, while in Si doped GaN, alloy scattering is excluded and impurity scattering is included using an activation energy of Si: ΔE_D = 20 meV. It can be found in Fig. 3.17 that at a low dislocation density of 10^7 cm^{-2}, the electron mobility in Pi-doped GaN is largely independent of electron concentration. This is because of the dominance of al-

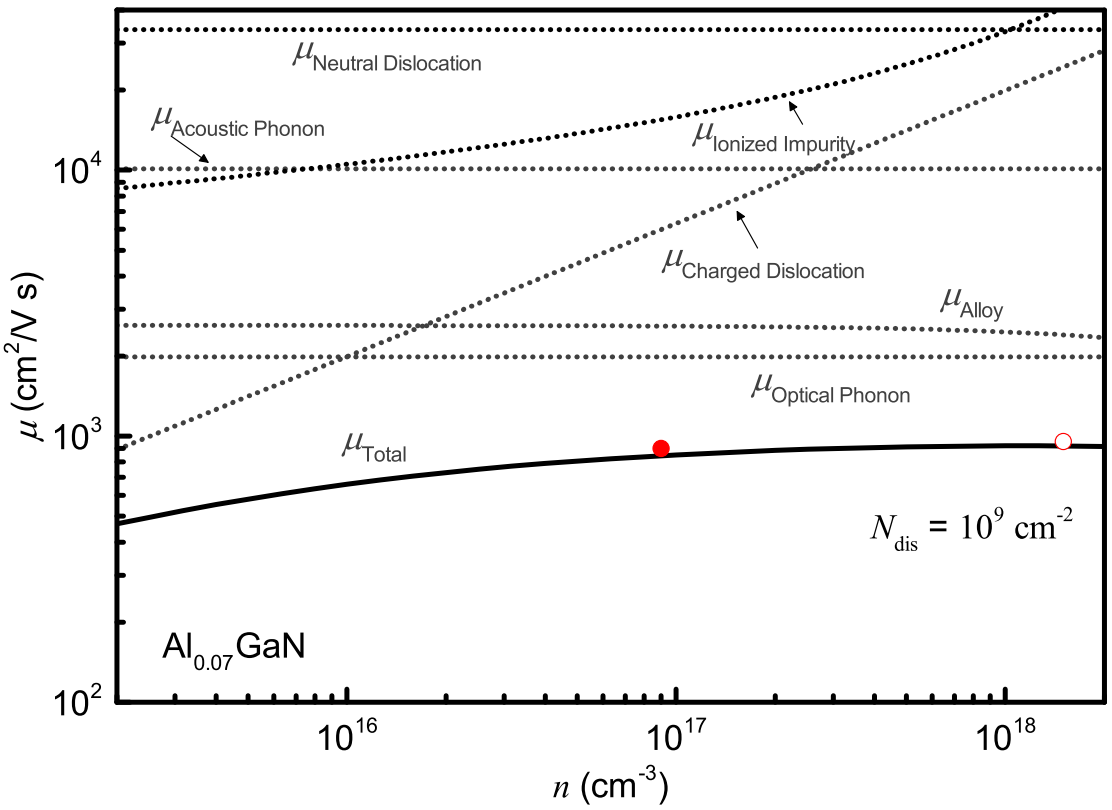

Figure 3.16: Modeled electron mobilities vs. electron concentration in Pi-doped $Al_{0.07}GaN$ with a dislocation density of 10^9 cm^{-2}. The $Al_{0.07}GaN$ is assumed to be free of impurities otherwise. Experimental data from this work (solid red circle) and from Ref. (open red circle). The occupation probability of dislocation is assumed to be 55% in all modeling results and the unoccupied dislocations are treated as neutral impurities.

loy scattering, which is independent of electron concentration in nondegenerate regime. An increase in dislocation density from 10^7 cm^{-2} to 10^9 cm^{-2}, results in an increasingly high dependence of electron mobility on the electron concentration. The effect of dislocation scattering is more pronounced in $Al_{0.07}GaN$ compared to $Al_{0.15}GaN$ because of a lower alloy scattering in $Al_{0.07}GaN$. The significant effect of dislocation scattering is also observed in Si-doped GaN with low electron concentrations, also compared to Pi-doped GaN in Fig. 3.18. At low carrier concentrations ($<2 \times 10^{17}$ cm^{-3}), the presence of dislocations severely degrades mobility in layers doped in both schemes. The experimentally reported mobility values (symbols) for $N_{dis} \sim 10^9$ cm^{-2} are also included. The difference between the experimental values and the modeled values can be attributed to

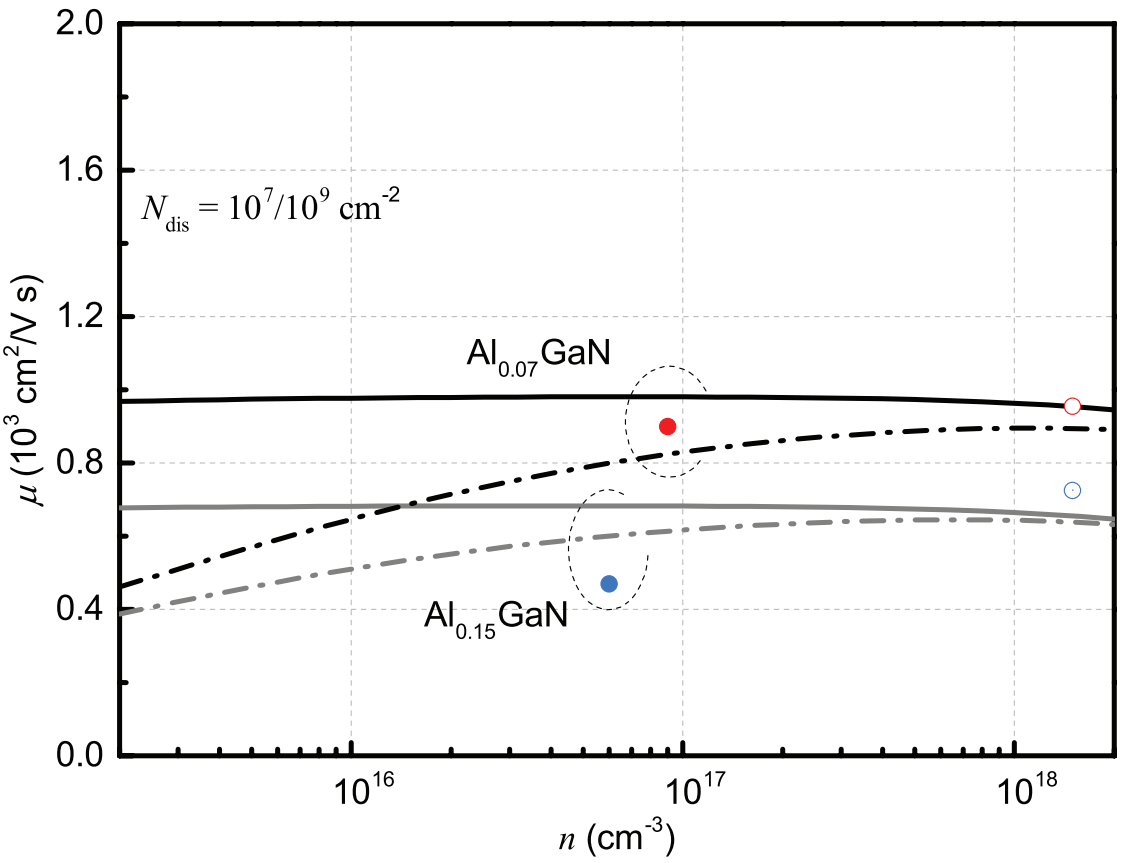

Figure 3.17: Modeled electron mobility in Pi-doped $Al_{0.07}GaN$ and $Al_{0.15}GaN$ assuming an N_{dis} of 10^7 cm^{-2} (solid lines) and 10^9 cm^{-2} (dash-dot lines) with the otherwise same assumptions in Fig. 3.16. Also shown are the experimentally measured electron mobility in AlGaN from this work (solid circles) and Ref. (open circles).

experimental errors as well as scattering due to compensating point defects, which is not included in the models. For $n > 2 \times 10^{17}$ cm^{-3}, the electron mobility is severely degraded by impurity scattering in GaN:Si [100, 101]; on the contrary, the electron mobility in Pi-doped AlGaN remains high for high electron concentrations since there is no impurity scattering. At low electron concentrations, dislocation scattering has a significant impact on electron mobility in both Pi-doped AlGaN and Si-doped GaN. Thus, the key to improving electron mobility for electron concentration $< 10^{17}$ cm^{-3} is to reduce N_{dis}. As a much lower N_{dis} ($< 10^7$ cm^{-2}) is achievable in todays bulk GaN substrates and the subsequent epitaxial layers [46, 102] than GaN on SiC/sapphire substrates, it is

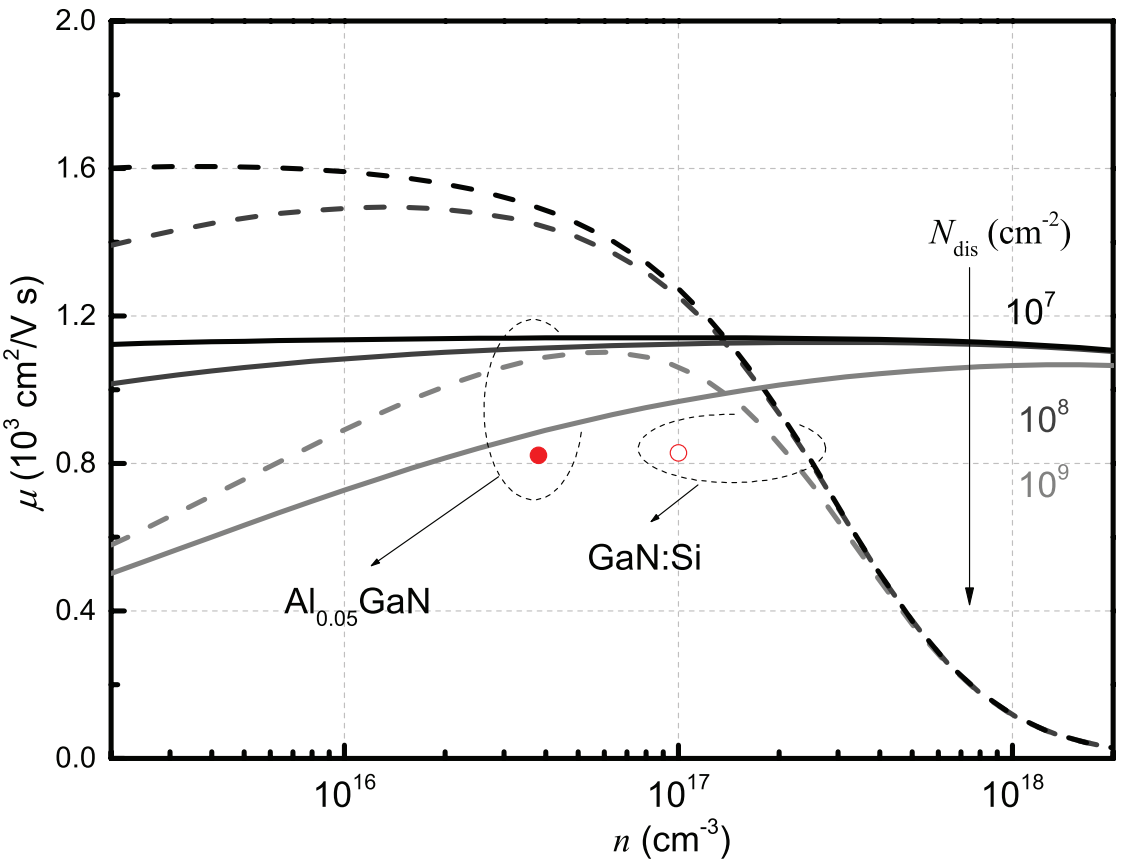

Figure 3.18: Modeled electron mobility in Pi-doped $Al_{0.05}GaN$ and Si-doped GaN as a function of the electron concentration at a few dislocation densities. Also shown are the experimentally measured electron mobility in $Al_{0.05}GaN$ (solid circle, this work) and that in GaN:Si (open circle, Ref.) in GaN on sapphire with similar N_{dis} values. Not shown in the plot, the electron mobility in GaN grown on bulk GaN with Ndis ¡107 cm-2 has been reported to be ~1500 $cm^2/V \cdot s$ near a concentration $\sim 1 \times 10^{16}$ cm^{-2}. The finite differences between the models and experiments is largely attributed to experimental errors as well as the existence of other point defects and defect complexes that are not considered in the models.

feasible to achieve improved electron mobility in Pi-doped AlGaN.

3.7 Summary

In summary, linearly graded $Al_xGa_{1-x}N$ is grown by MOCVD on sapphire substrates with a polarization induced doping of a low and uniform electron concentration near

10^{17} cm^{-3}. A peak electron mobility of ~900 cm^2/Vs at RT is extracted in $Al_{0.07}GaN$. By comparing the experimental data to carrier transport models, dislocation scattering is found to be the significant factor limiting electron mobility when the electron concentration is below 10^{17} cm^{-3}. At low electron concentrations < 10^{17} cm^{-3}, much improved electron mobility can be expected in epitaxial layers grown on bulk GaN substrates with a dislocation density lower than 1×10^7 cm^{-2}.

CHAPTER 4

DEVELOPMENT OF POLARMOSH

4.1 Introduction

Free-standing GaN substrates with continuously improved quality and lowered cost have paved the way for realizing vertical GaN power devices, promising high conduction current but low on-resistance, high blocking voltage and fast switching speed. GaN Metal-Oxide-Semiconductor High Electron Mobility Transistor (MOSHEMT) or MOSFET on top of conducting (drift and drain electrode) layers is an essential element for vertical GaN VDMOS power transistors. GaN MOSHEMTs with a polarization-doped p-AlGaN back barrier on top of conducting layers is named as PolarMOSH. It is a building block for the novel vertical GaN device PolarMOS [2, 103], which takes advantage of the unique polarization properties of GaN for power applications. The cross section schematics of both PolarMOS and PolarMOSH are illustrated in Fig. 4.1.

Experimental realization of HEMTs with a p-type back barrier grown on unintentionally-doped (UID) GaN or n-GaN has been challenging due to the high buffer leakage as well as difficulty in junction placement due to Mg. In metal-organic chemical vapor deposition (MOCVD) growth, Mg tends to incorporate in subsequently grown layer [104, 105, 106, 107], resulting in compensation effects that prevent formation of two dimensional electron gas (2DEG). Chowdhury et al. [3, 108] showed that the Mg diffusion could be suppressed through insertion of an AlN layer or a low-temperature GaN layer. However, in their experiments, Mg doping is carried out through ion implantation and the subsequent layers were regrown using molecular beam epitaxy. The regrowth interface often has high densities of impurities due to exposure to the atmosphere, which leads to high leakage current [109].

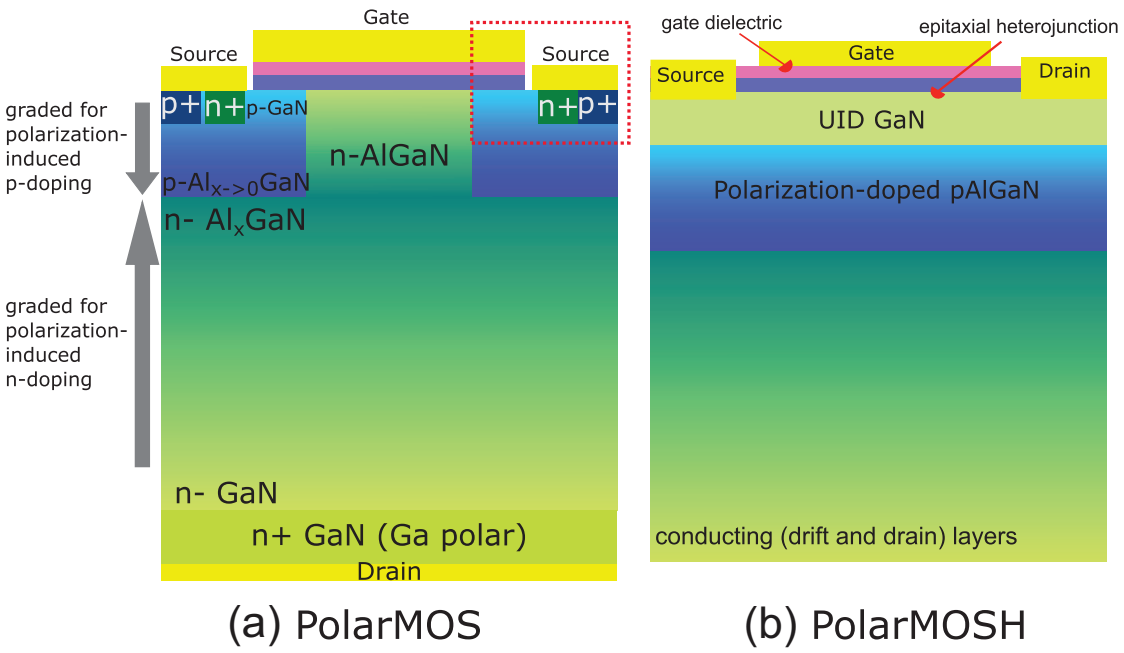

Figure 4.1: Cross section schematics of PolarMOS (a) and PolarMOSH (b). PolarMOS is a novel vertical GaN power transistor [2]. PolarMOSH is a GaN MOSHEMT with a polarization-doped p-AlGaN back barrier on top of conducting layers. It is a building block for PolarMOS, as illustrated by the red rectangle in the left figure.

Here we present the first realization of PolarMOSHs, on free-standing GaN substrates and illustrate the adverse effect of dislocations on buffer leakage by comparing PolarMOSHs grown on SiC and GaN substrates. The experiments started with PolarMOSH epitaxial structures grown on SiC substrates, which show a persistently large buffer leakage current since the p-AlGaN barrier does not effectively block leakage current between 2DEG channel and the underlying layers due to an excessive amount of dislocations ($\sim 10^9$ cm^{-2}). The involvement of Mg doping is found to prevent the formation of 2DEG channel as well as alloyed ohmic contacts [108]. Then the PolarMOSH epitaxial structure was carefully improved to reduce the effects of Mg doping on the 2DEG channel and grown on free-standing GaN substrates. The fabricated PolarMOSHs on free-standing GaN substrates show a high current On/Off ratio of $> 10^{10}$ and a low drain leakage current of < 1 pA/mm .

4.2 Mg Diffusion in MOCVD-Grown p-GaN

It has been reported in the literature that Mg-doped GaN grown by metal-organic chemical vapor deposition (MOCVD) has a so-called "memory effect" [105, 104], where the epitaxial GaN layers grown on top of the Mg-doped layer show a much higher Mg concentration than the background Mg concentration. This effect is observed in both continuous growths where the Mg precursor is shut-off at the end of the growth of the Mg-doped GaN [104], as well as interrupted growths where a separate growth is performed after the completion of the growth of the Mg-doped GaN and the wafers being taken out of the growth chamber where the Mg precursor is never flown during the growth of the layers where Mg doping is not designed.

When an excessively high concentration of Mg is present at AlGaN/GaN heterojunctions, characterizations of the heterojunctions, including Hall effect measurement and *C*-*V*, do not show the presence of 2DEG due to the compensation by Mg and other defects co-existing with Mg. As the goal of utilizing the 2DEG in the end is to form ohmic contact with it and be able to modify its properties, we investigate the impact of the memory effect on the ohmic contact to the 2DEG.

Three wafers are grown by MOCVD on sapphire substrates with the epitaxial layer structures shown in the insets of Fig. 4.2. The samples are named as sample 1-A (wafer ID: R4172), 1-B (wafer ID: R4173)and 1-C (wafer ID: R4194) for easy reference. Sample 1-A is the control sample where a semi-insulating (SI) GaN with a thickness of 4 μm is grown on the GaN-on-sapphire template, followed by the top barrier stack consisting of AlGaN/AlN/GaN with thicknesses of 3 nm/1.5 nm/22 nm. The top GaN layer is doped with Si with a concentration of 5×10^{18} cm^{-3} to increase the electron density of the 2DEG. Both sample 1-B and sample 1-C incorporate a Mg doped p-AlGaN back

barrier. The back barrier consists of 200 nm of p-GaN, two graded p-AlGaN layers of 200 nm each, with a Al composition graded from 0% to 20% and from 20% to 0%. The Mg concentration in all 3 p-type layers is 1×10^{18} cm^{-3}. Following the growth of the p-type back barrier, a thin GaN layer of a thickness of 10 nm is grown and the growth the completed after the growth of the top barrier structure as described for sample 1-A. The only difference between sample 1-B and sample 1-C is that the top GaN layer in sample 1-B is not doped with Si like the other two samples. This is to investigate its impact on the 2DEG density.

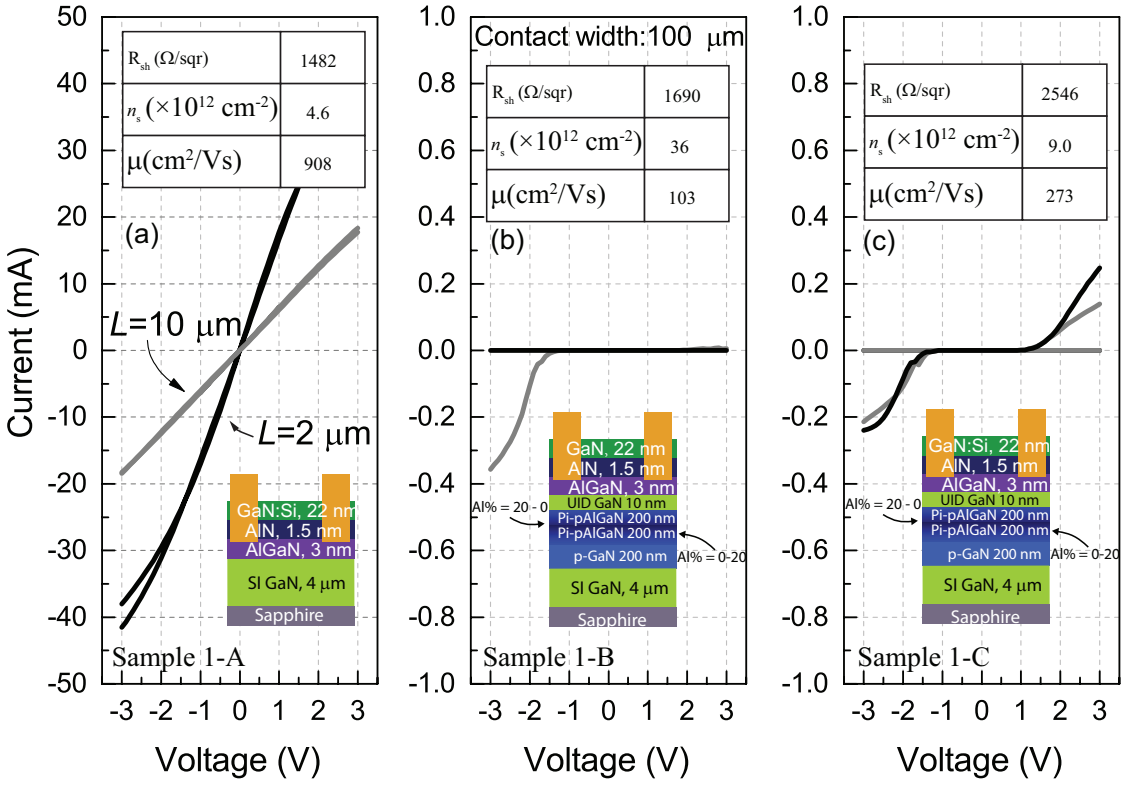

Figure 4.2: Comparison of *I*-*V*s measured on a pair of metal pads on sample 1-A (wafer ID: R4172), 1-B (wafer ID: R4173) and 1-C (wafer ID: R4194). The insets in each sub-figure shows the cross-section schematic of the measure structure and the Hall effect measurement results.

Each sample is characterized with room temperature Hall effect measurement using van der Pauw method. The results are tabulated in the insets of Fig. 4.2 for each sample. Sample 1-A shows a electron concentration of 4.6×10^{12} cm^{-2} and a electron mobility

of 908 $cm^2/V \cdot s$, which are both within the expected range for a 2DEG formed at the AlGaN/GaN heterojunction. In contrast, both sample 1-B and 1-C show low electron mobilities (< 300 $cm^2/V \cdot s$), indicating that the measured conduction is from parasitic leakage paths rather than the 2DEG at the AlGaN/GaN interface. The samples are further characterized with *I*-*V* measurement on a pair of metal pads after forming ohmic contacts. The ohmic contact formation is carried out by depositing a metal stack of Ti/Al/Ni/Au with thicknesses of 20/100/40/40 nm by e-beam evaporation and then annealing the sample in a rapid thermal annealing system. The annealing is performed at 890 °C for 30 s with a constant N_2 flow in the chamber. The ohmic contact formation process is a well established process routinely performed in fabricating AlGaN/GaN HEMTs. The distances between the pair of metal contacts are 2 μm and 10 μm. The measured *I*-*V* results are plotted in Fig. 4.2 for each sample. While the *I*-*V* results measured on sample 1-A shows a linear *I*-*V* behavior and a current density as high as 400 mA/mm, the *I*-*V* measurement on sample 1-B and 1-C yields a very low current (< 4 mA/mm). This low current density, along with the low electron mobility in Hall effect measurement, indicates the absence of 2DEG in sample 1-B and 1-C where Mg doping and polarization doping are both incorporated. This is consistent with previous reports in the literature.

The result of a secondary ion mass spectroscopy (SIMS) scan of the as grown sample 1-B is plotted in Fig. 4.3 (a). A high Mg concentration of 7×10^{17} cm^{-3} is observed at all the epitaxial layer on top of the Mg doped layers, which is about one third of the Mg concentration in the intentionally doped layers. This Mg concentration is significant given that the Mg precursor is shut off after the growth of p-Gan back barrier. Similar plateau of Mg concentration has been reported before which also resulted in the compensation of 2DEG. It has also been shown that the Mg concentration has to be reduced to form 2DEG at the AlGaN/GaN interface.

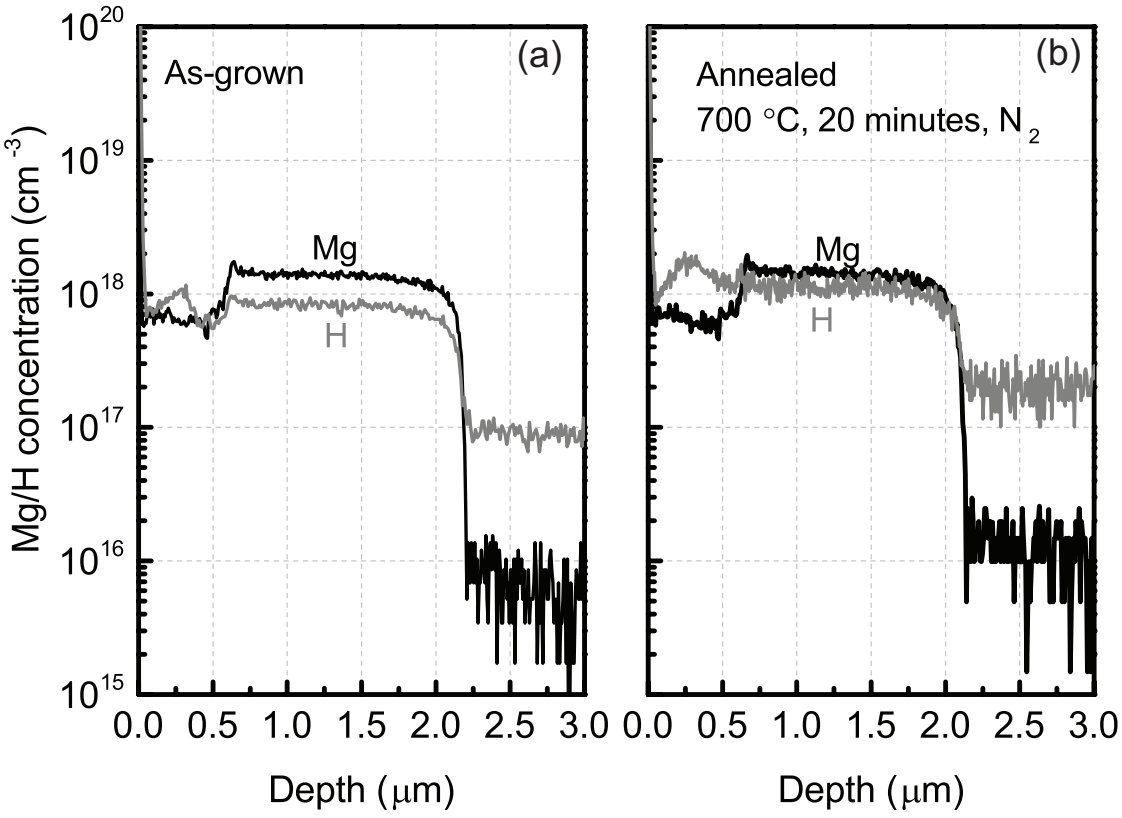

Figure 4.3: Mg and H concentration profiles of the as grown (a) and annealed (b)sample 1-B. The concentrations are measured by secondary ion mass spectroscopy.

From Fig. 4.3, the H concentrations in the Mg doped layer and the layers above are ~7-10 times higher than the background concentration. Since H is well known to passivate Mg and results in highly resistive material, an annealing process is carried out attempted to reduce the H concentration. The annealing performed at 700 °C in a N_2 ambient for 20 minutes in a rapid thermal annealing system, which is close to the standard activation annealing conditions routinely employed for MOCVD grown Mg-doped p-GaN. Another SIMS scan is performed, with the Mg and H concentration profiles plotted in Fig. 4.3(right). By comparing the two plots in Fig. 4.3, no significant change in Mg and H concentration is observed. The difference in the background H concentration is likely due to the fact that the SIMS scans are carried out at two different sites which could have different detection limits for H. In the end, activation annealing

at 700 °C does not reduce the H concentration in the epitaxial layer with intentional and unintentional Mg doping. More about the activation of Mg doped p-GaN buried underneath a not-p-type layer will be discussed further in the later part of this chapter.

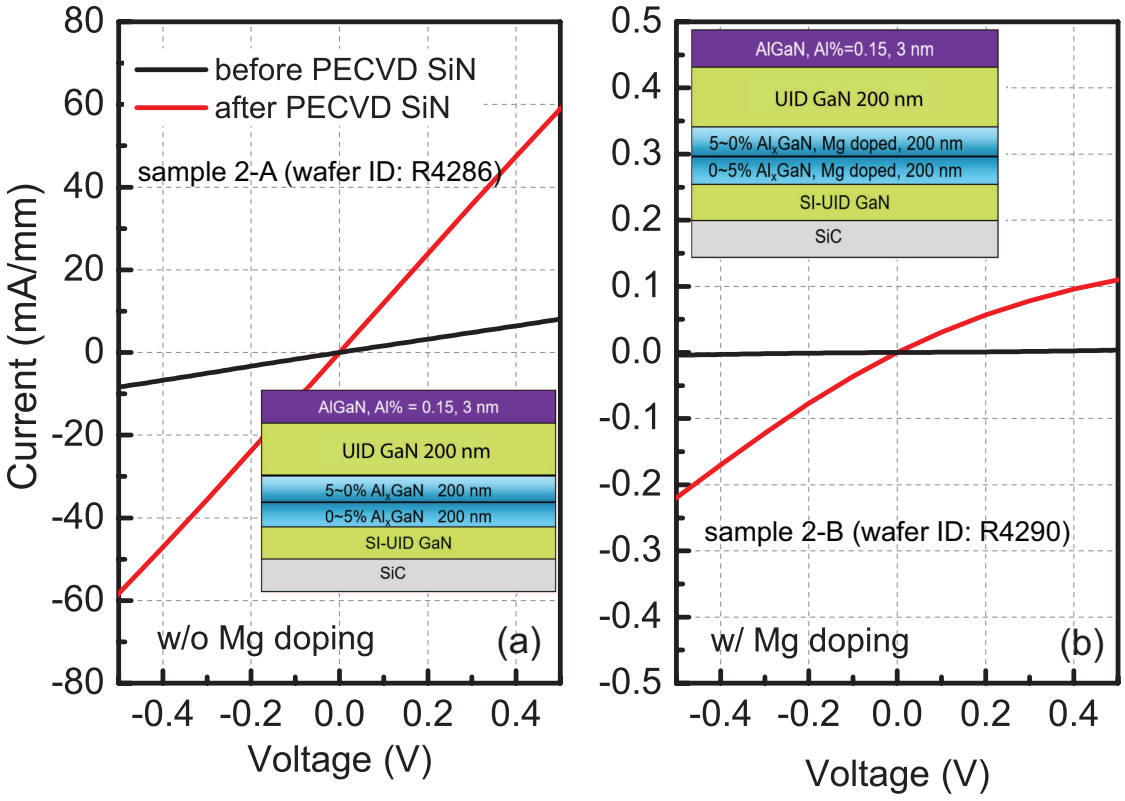

Figure 4.4: Comparison of *I-V* characteristics of a pair of ohmic contacts (2 μm separation) before and after 20 nm PECVD SiNx deposition on (a) sample without Mg doping and (b) sample with Mg doping. Mg doping causes a large decrease in measured currents.

To better delineate the role of polarization-induced doping and Mg doping in affecting the 2DEG at the heterojunction grown above the p-GaN back barrier, a second batch of wafers are grown consisting of two wafers, sample 2-A (wafer ID: R4286) and sample 2-B (wafer ID: R4290), with and without Mg doping. The epitaxial layer structures for each sample is shown in the insets of Fig. 4.4.Both structures were grown on SiC substrates by MOCVD, consisting of a high-resistivity UID GaN layer, 0~5% graded $Al_xGa_{1-x}N$, 5%~0 graded $Al_xGa_{1-x}N$ (with or without Mg), 200 nm UID-GaN,

3 nm $Al_{0.15}Ga_{0.85}N$, while the only difference between the two device structures is the Mg doping in the back barrier. The epitaxial structures were designed for enhancement-mode (E-mode); 20 nm plasma-enhanced chemical vapor deposition (PECVD) SiNx, which is found to increase the 2DEG concentration thus reduce sheet resistance [110], was deposited after Ohmic contacts formation (alloyed Ti/Al/Ni/Au). Figure 4.4 shows the comparison of *I-V* characteristics of ohmic contacts before and after SiNx deposition on both samples. As can be seen from both plots in Fig. 4.4, 20 nm PECVD SiNx is effective in increasing measured current density for both epitaxial structures. However, the measured current density values are quite different. While the current through a pair of ohmic contacts separated by 2 μm could reach 60 mA/mm at 0.5 V bias on the sample without Mg doping, it barely exceeds ~ 0.2 mA/mm on the sample with Mg doping. Further measurement show that, for sample 2-A, the current level on a pair of ohmic contacts separated by 2 μm can exceed 300 mA/mm after SiN_x deposition. The clear contrast of *I-V* characteristics on the two otherwise identical samples shows that the compensating effects is due to Mg concentration, rather than polarization-induced doping. SIMS measurement show that the Mg concentration near the AlGaN/GaN heterojunction is close to 1×10^{17} cm^{-3}.

In order to further reduce the residue Mg concentration at the AlGaN/GaN interface, an even thicker unintentionally doped layer is designed in the epitaxial structure (sample 3). The epitaxial structure of sample 3 (wafer ID: R4435) is shown in Fig .4.5, where a 400 nm UID GaN layer, a 20 nm $Al_{0.15}GaN$ and a 70 nm Si-doped GaN layer are grown following the 300 nm p-AlGaN on a GaN-on-sapphire template. The Al composition of the p-AlGaN layer is graded from 5% to 0%. Notice that the top GaN layer is 70 nm thick, which is much thicker than that the top barriers in a typical AlGaN/GaN heterostructure. This is designed to accurately probe the Mg concentration at the AlGaN/GaN interface, since an artificial increase of atom concentration at

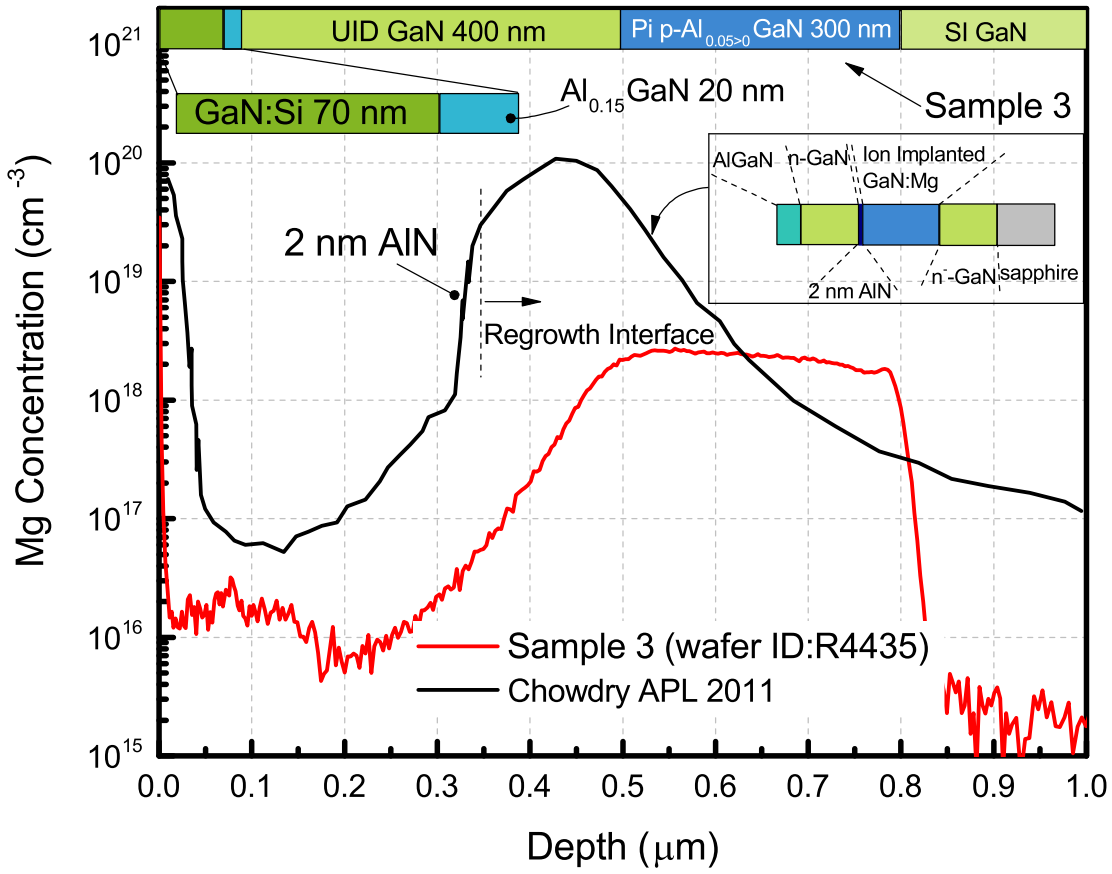

Figure 4.5: Epitaxial structure and Mg concentration profile for sample 3 (wafer ID: R4435). The Mg profile is compared to a previously reported profile [3] where a AlN layer is utilized to reduce the Mg concentration. Sample 3 is grown without interruption while the sample in the reference is re-grown.

the sample surface is always present in SIMS measurement results. Figure 4.5 shows the measured Mg concentration profile of sample 3 in comparison with a similar AlGaN/GaN heterostructure on Mg doped GaN reported in reference. The Mg p-type doping in the reference is implemented by ion implantation and the layers on top of the p-GaN layer is subsequently re-grown. It represents one of the most well controlled Mg concentration in GaN grown on Mg doped p-GaN. From Fig. 4.5, the Mg tail (Mg concentration decaying into the subsequently grown layers) is evident in both sample 3 and the reference. The minimum Mg concentration in the layers on top of p-GaN in sample 3 is about 10 times smaller than that in ref. [3], leading to an even smaller compensation

effect on the 2DEG at the AlGaN/GaN interface. It is worth mentioning that sample 3 is grown in a continuous MOCVD growth, which avoids the problem of high impurity concentrations at regrown interfaces. Another notable difference between the Mg profile of sample 3 and that from ref. is that the intentional Mg doping concentration in sample 3 is about 50 times lower. This may have contributed to the Mg concentration difference at the heterostructure as the Mg concentration decay rates are both around 100 nm/decade (excluding the AlN layer at the regrowth interface).

It is also evident from Fig. 4.5 that the AlGaN/GaN interface , which is 90 nm deep from the surface, is not affected by the Mg concentration increase near the surface. Another wafer grown with similar epitaxial layer structure but a much thinner top barrier, making the AlGaN/GaN interface close to the surface, shows well-behaved 2DEG behavior. These observations together show that more attention should be paid to the Mg concentration in the channel region which is less affected by the artificial concentration increase near the surface.

Since the top barrier in sample 3 is 70 nm thick, making it difficult to achieve good ohmic contacts to the 2DEG and inspect its characteristics, C-V characteristics of Schottky barrier diodes fabricated on the sample are more suitable to probe the 2DEG characteristics. This is because the capacitance measurement is done with small signals where the quality of ohmic contacts has much less influence on the measurement accuracy than the I-V measurements discussed before. The cathodes of the Schottky barrier diodes are formed by performing the standard alloy contact process and the anodes are implemented by depositing Ni/Au with e-beam evaporator. The diodes are in a circular layout and thus self-isolated. The C-V result is plotted in Fig. 4.6, where a clear capacitance step is observed indicating the presence of a 2DEG. Notice that the capacitance measured at $V < -2$ V is ~ 500 pF which is more than 3 times larger than the minimum

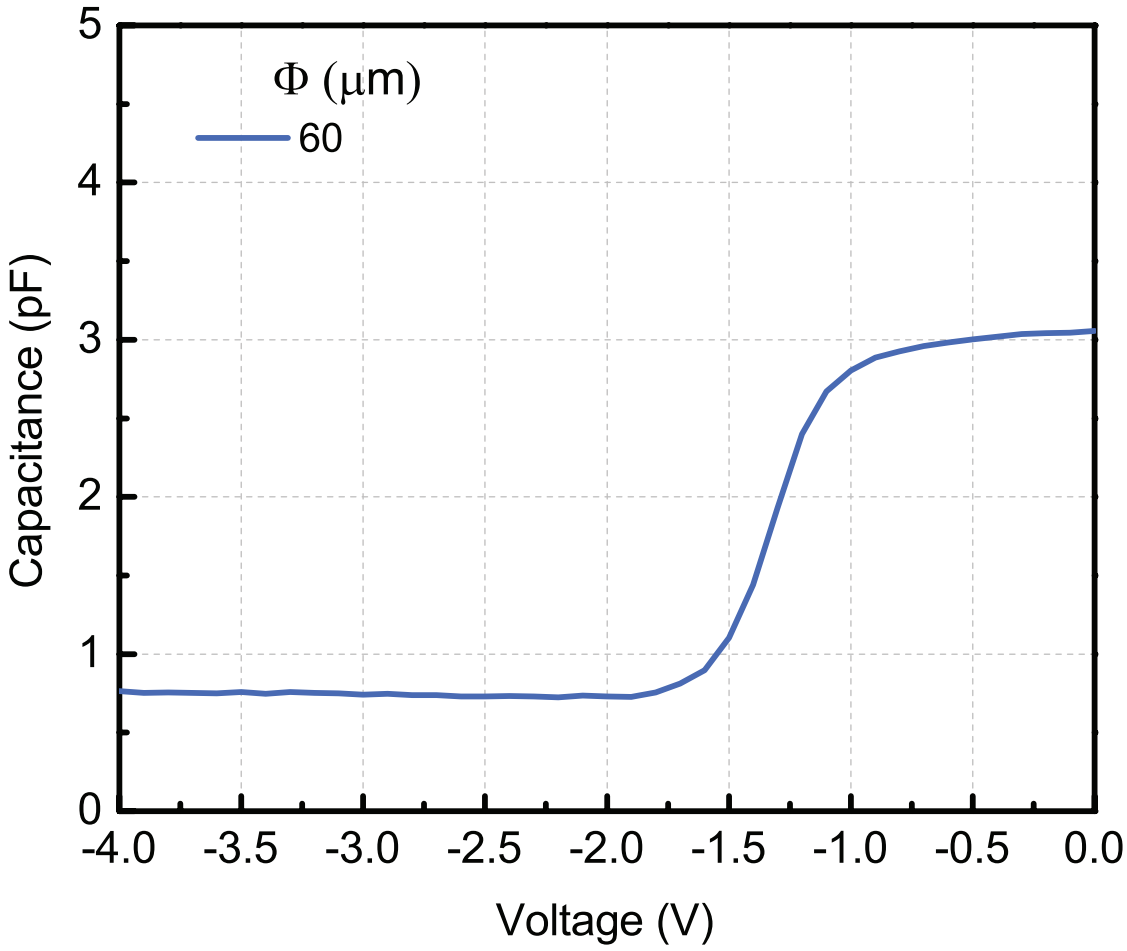

Figure 4.6: Measured *C-V* characteristics of SBD fabricated on sample 3. A sharp drop in capacitance at a bias voltage of -1 V is observed, indicating the presence of 2DEG

measurable capacitance of the CV meter. This phenomenon will be explained later in this chapter.

In this section, the wafer with a AlGaN/GaN 2DEG on top of Mg-doped GaN (sample 3) is demonstrated with a continuous MOCVD growth. This wafer is grown on a sapphire substrate. This demonstration marks promising progress for realizing PolarMOS as forming a 2DEG channel on top of Mg-doped GaN is essential in fabricating PolarMOS.

4.3 Buffer Leakage Issue

Although sample 3 demonstrates a AlGaN/GaN 2DEG on top of Mg-doped GaN completed with a continuous MOCVD growth, it suffers from a buffer leakage problem. The buffer leakage in sample 3 is characterized by measuring the *I*-*V* characteristics of a pair of mesa-isolated ohmic contacts. The measured *I*-*V* characteristics are plotted in Fig. 4.7 with the cross-section of the test structure shown in the inset. Large leakage currents are observed in testing structures with both 2 μm and 10 μm separations.

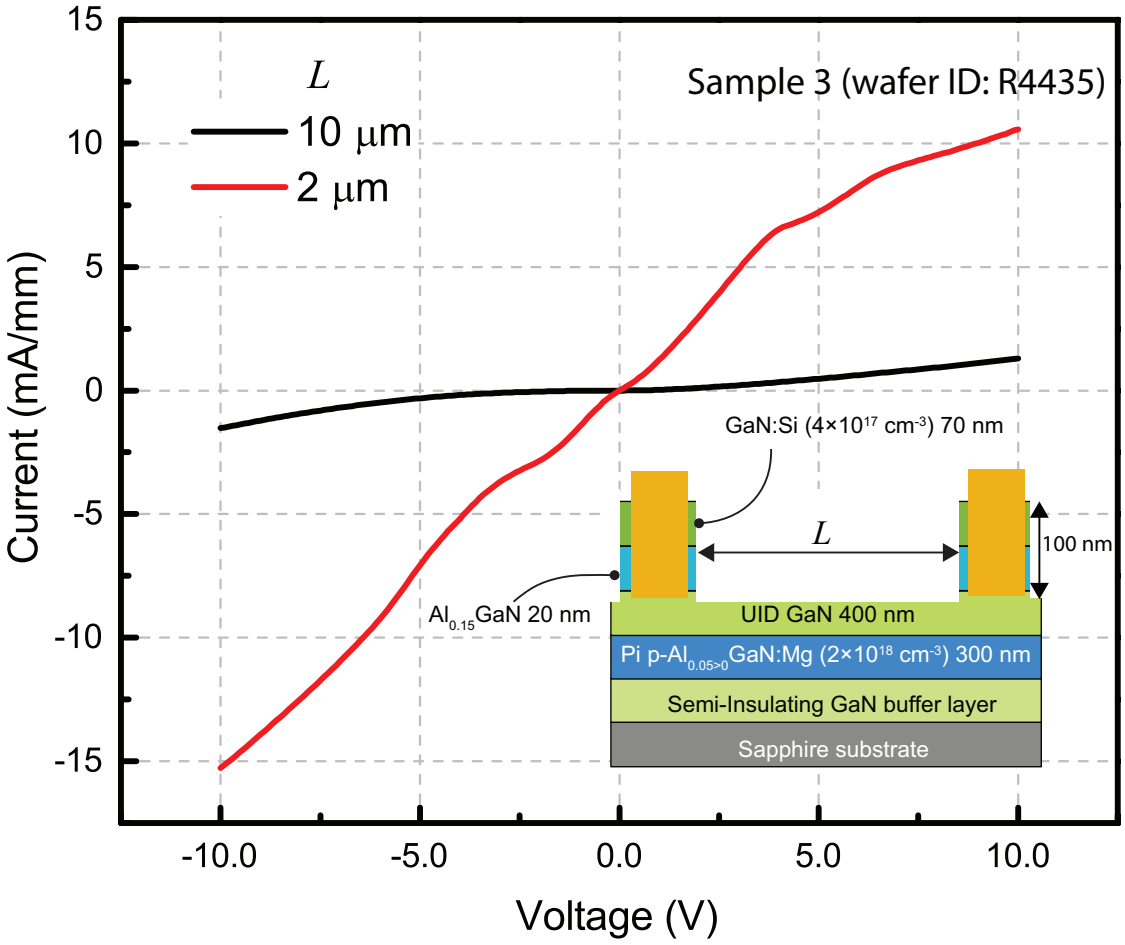

Figure 4.7: Measured *I*-*V* characteristics of a pair of mesa-isolated ohmic contacts. Excessive leakage currents are observed for test structures with 2 μm and 10 μm.

The leakage current issue is also present in sample 2-A and 2-B. Fig. 4.8 shows the

buffer leakage current behavior of sample 2-A and 2-B. Although a reduction of buffer leakage current at low voltage biases is observed when Mg doping is incorporated, the leakage currents on these two samples at 20 V bias are similar and exceed 1 mA/mm. Wafers with such high buffer leakage current is not suitable for transistor fabrication.

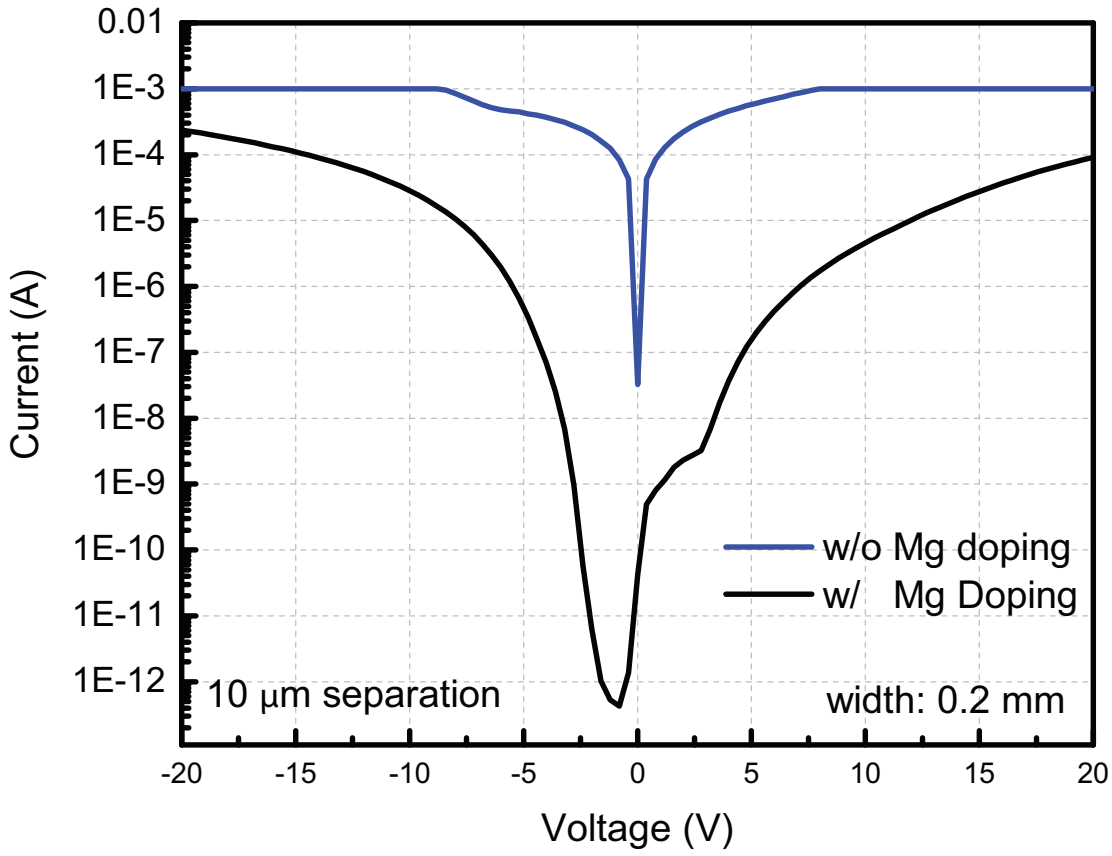

Figure 4.8: Comparison of buffer leakage current on sample 2-A and 2-B. The Mg doping in sample 2-B is seen to reduce the buffer leakage current at low voltage biases, however the buffer leakage currents at 20 V on both samples are similar and exceed 1 mA/mm level.

To identify the leakage current path of sample 2-B, mesa isolation etching of different depths are carried out. The buffer leakage current with different isolation etching depths are then measured and compared. Fig. 4.9 shows the measured leakage current on sample 2-B with 100 nm and 800 nm isolation etching. Also included is the buffer leakage current of a GaN-on-Si wafer. A 10^5X reduction in leakage current is

observed when the isolation etching reaches deeper than the Mg-doped, suggesting that the $Al_xGa_{1-x}N$ layer and the UID GaN layer above contributes to most of the leakage current. However a further study is required to find out the exact amount of leakage current for each leakage path denoted in the upper inset plot in Fig. 4.9. The leakage current after 800 nm deep etching is still orders of magnitude larger than the GaN-on-Si HEMT, which has an impurity-doped semi-insulating GaN buffer layer. This indicates that the leakage path runs through the $Al_xGa_{1-x}N$ to the underlying SI-UID layer (as illustrated in the lower inset plot in Fig. 4.9).

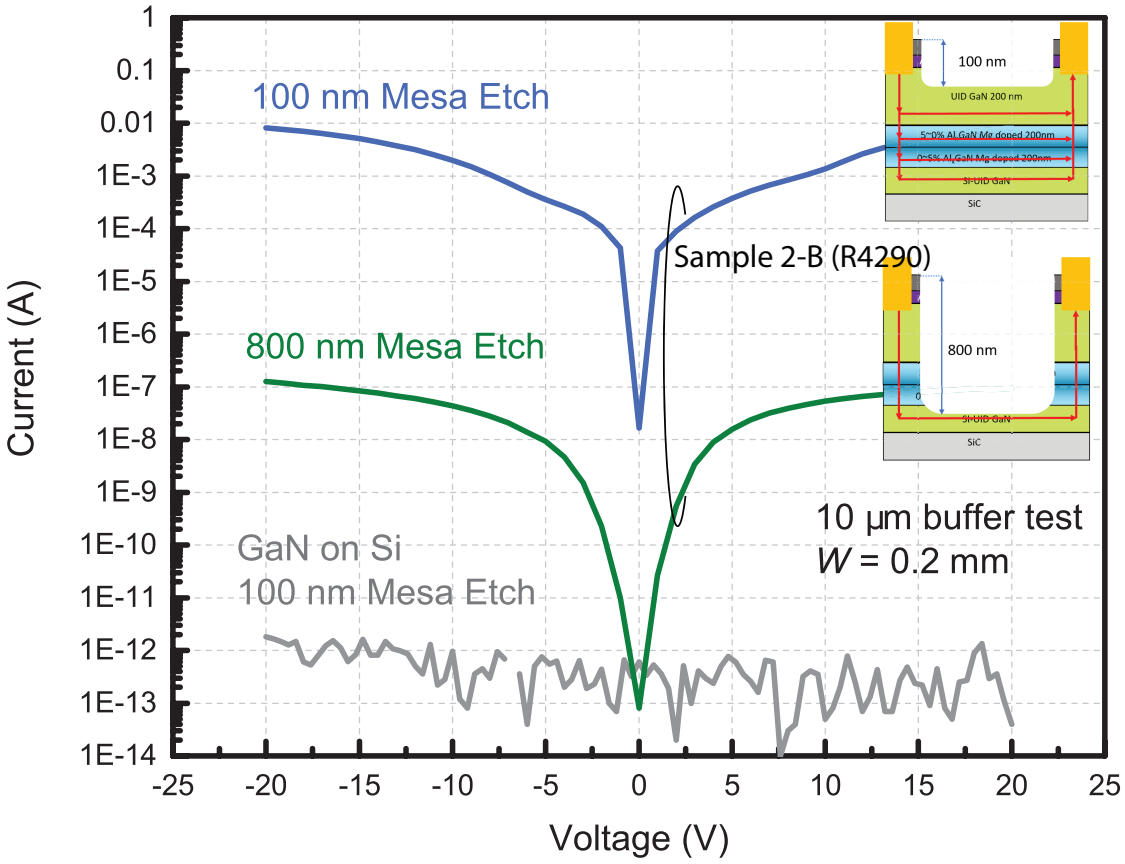

Figure 4.9: Leakage current comparison between sample 2-B with 100 nm and 800 nm mesa etching. Also plotted is the leakage current on a GaN-on-Si HEMT [4, 5]. A large leakage current reduction is observed after deep etching, although the reduced leakage current is still orders of magnitude larger than that on the GaN-on-Si sample. The possible leakage path after 100 and 800 nm etching are denoted as red arrow lines in the inset plots.

PolarMOSH is nevertheless fabricated to show the impact of buffer leakage current on the transistor's characteristics. The PolarMOSH fabrication process following the mesa etch of 100 nm by RIE includes: gate lithography and RIE etching of PECVD SiNx, 20 nm Al_2O_3 deposition by atomic layer deposition (ALD) and gate metal deposition. The I_D-V_D characteristics of the PolarMOSH fabricated on the sample without Mg doping is shown in Fig. 4.10 along with its cross-section schematic. Although a clear gate modulation of drain current is seen from the plot, indicating the presence of electron channel, the excessive buffer leakage current prevents a complete turn-off of the drain current.

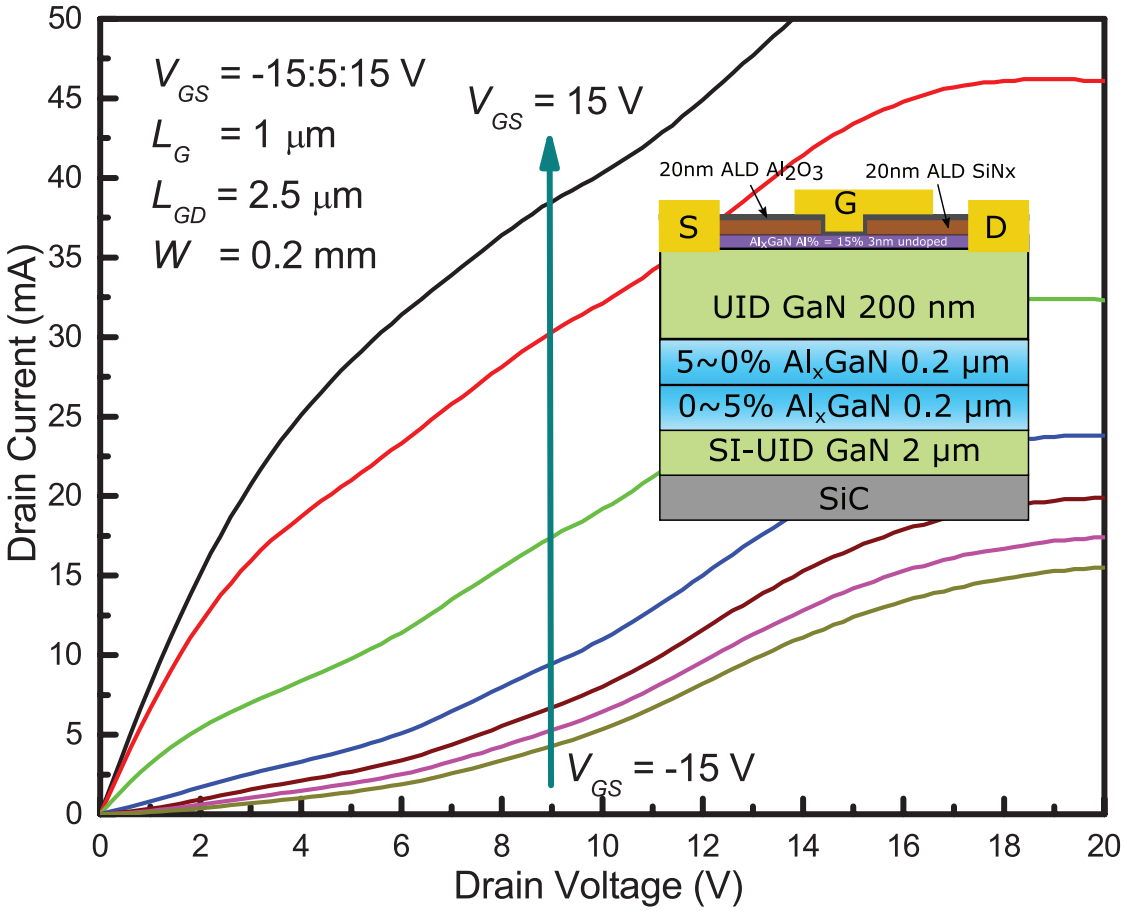

Figure 4.10: $I_D - V_D$ characteristics of MOSHEMT fabricated with sample 2-A (wafer ID:R4286, No Mg doping). Clear gate modulation of drain current is shown. Large leakage current inhibits complete turn-off of drain current.

Free-standing GaN substrates have been an attractive option for achieving electronic devices with low leakage currents. The reported p-n diodes fabricated on free-standing GaN substrates have shown near-unit ideality factor [102], high breakdown voltage (> 3 kV) [111, 112] and a record high power figure-of-merit BV^2/Ron of > 16 GW/cm^2 [102]. These record setting performances is often attributed to the much lower dislocation density of GaN grown on free-standing GaN substrates compared to that grown on sapphire/SiC substrates [46, 113]. To reduce the dislocation-induced buffer leakage current of PolarMOSH samples, one wafer (sample 4, wafer ID: R4452) with a layer structure similar to that of sample 3 is grown by MOCVD on a free-standing GaN substrate. According to the specification provided by the substrate vendor,this GaN substrate has a screw dislocation density $<1 \times 10^6$ cm^{-2} which is 1000 times smaller than GaN grown on sapphire/SiC substrates. The epitaxial structure of sample 4 is shown shown in Fig. 4.11, along with the atom concentrations, Ga and Al compositions of sample 4 measured by a SIMS scan.

To show the impact of substrates on the buffer leakage current, the buffer leakage currents of sample 3 and sample 4 with different isolation etching depths are compared. Three etching depths are employed during the mesa etching process: 300 nm, 500 nm and 800 nm. These etching depths are chosen so that the etching will stop at the UID GaN layer, the Mg-doped layer and the layer underneath the Mg-doped layer, respectively. As illustrated in Fig. 4.12(a), with each increase of etching depth, one additional layer is removed and hence the elimination of one leakage path (labeled ”1”, ”2” and ”3”). The measured buffer leakage current is plotted in Fig. 4.12(b). A larger than 1000 times reduction in buffer leakage current is shown on sample 4 in comparison to that of sample 3. The buffer leakage current gradually decreases as the etching depth increases, which is consistent with the leakage path analysis.

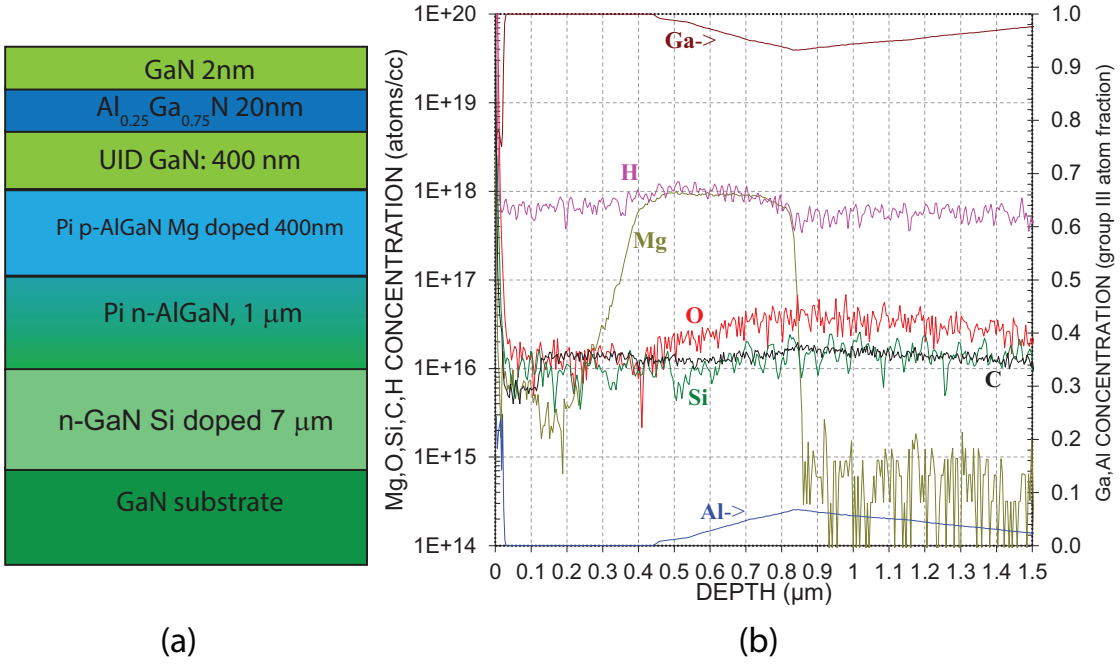

Figure 4.11: (a) Epitaxial structure of sample 4 (wafer ID: R4452). (b) Atom concentrations as well as Ga and Al compositions measured by a SIMS scan on sample 4.

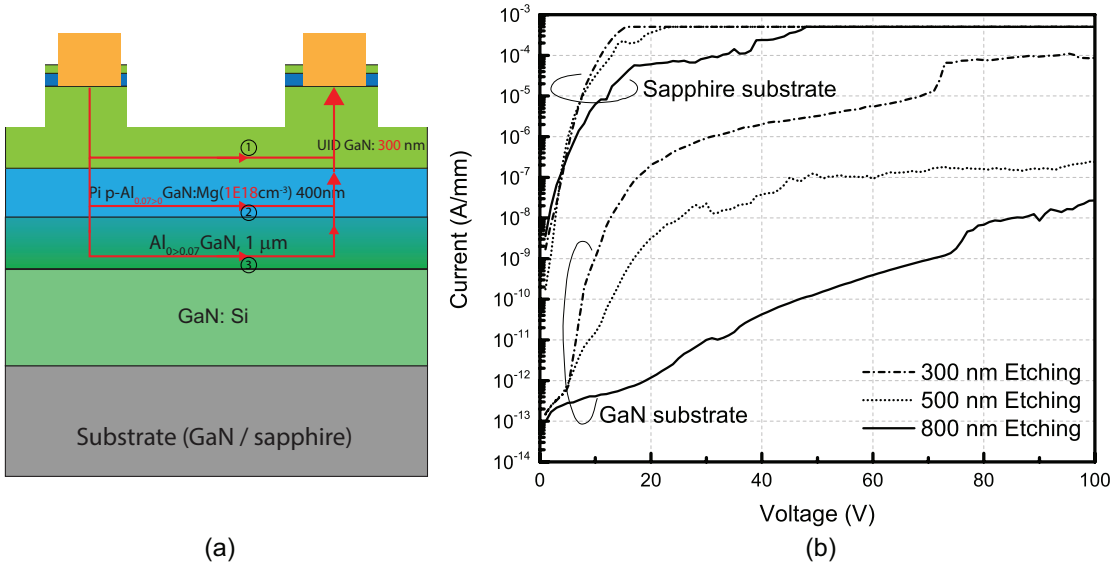

Figure 4.12: (a) Illustration of buffer leakage path on sample 3 (sapphire substrates, wafer ID: R4435) and sample 4 (GaN substrates, wafer ID: R4452). (b) Comparison of buffer leakage current of sample 3 and sample 4. Three different isolation etching depths are employed to identify the contribution of each layer to the total leakage current.

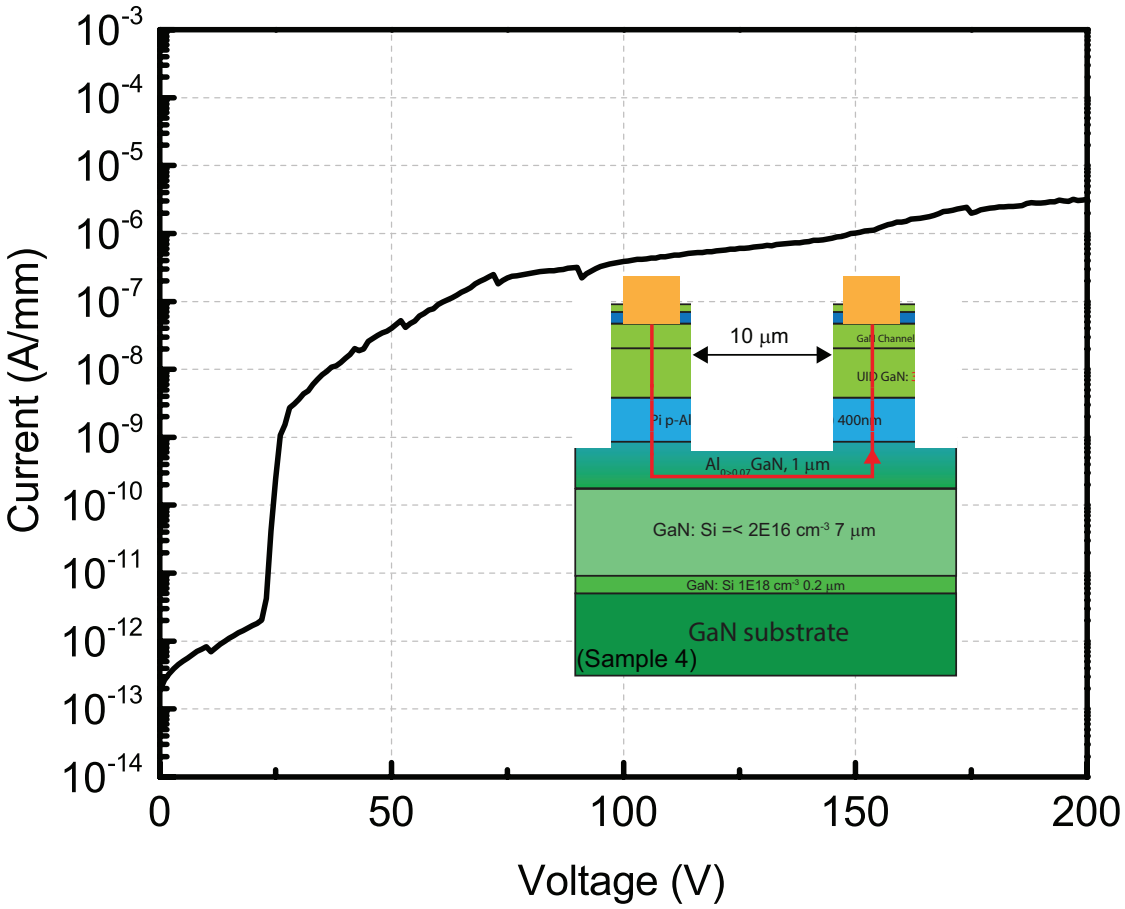

Figure 4.13: Breakdown characteristics of a pair of mesa-separated ohmic contacts on sample 4. The separation distance is 10 μm.

By employing free-standing GaN substrates for the wafer expitaxy, the buffer leakage issue is largely curbed. On sample 4, the buffer-leakage test structure with a separation distance of 10 μm is shown to have a breakdown voltage of > 200 V (Fig. 4.13). Since most of the high voltage in a off-biased PolarMOS is sustained by the current aperture and drift region, a 200 V breakdown voltage is sufficient for PolarMOS development.

4.4 Ohmic Contact Formation

Having resolved the issue of buffer leakage current, PolarMOSH development is faced with a new challenge on achieving good ohmic contacts to the 2DEG channel. Fig. 4.14 shows the measured *I*-*V* characteristics of TLM patterns with standard alloyed contacts fabricated on sample 4. A current saturation level of ~200 mA/mm is observed, regardless of separation distance. The current saturation is caused the reduced dislocation density in GaN grown on free-standing GaN substrates, as alloyed ohmic contacts rely on a high dislocation density to achieve good contacts [6]. The PolarMOSH transistor fabricated on sample 4 with standard alloyed ohmic contacts shows a drain current saturation level ~ 200 mA/mm, which is consistent with the current saturation observed in the TLM patterns.

The PolarMOSH fabrication on sample 4 follows the standard MOSHEMT fabrication process with a 20 nm of Al_2O_3 deposited by atomic layer deposition (ALD) as the gate dielectric. The measured transfer and family *I*-*V* characteristics are plotted in Fig. 4.15. Good transistor characteristics are shown, including a drain current on/off ratio > 10^{12}, a threshold voltage is extracted to be ~ −5 V by linear extrapolation and well-behaved drain current saturation in the family *I*-*V* curves. However, the alloyed contacts throttle the maximum drain current at ~ 200 mA/mm.

To eliminate the current throttle put on the PolarMOSH by the alloyed contacts, the ohmic contacts must be made without relying on a high dislocation density. MBE regrown contacts [75], which are achieved by etching of the ohmic contact area and then selectively regrown n^+-GaN to directly contact the 2DEG, have shown great advantages in achieving a low contact resistance and a small current collapse [5, 114]. Due to the nature of the direct contact between the 2DEG and the regrown n^+-GaN, the regrown

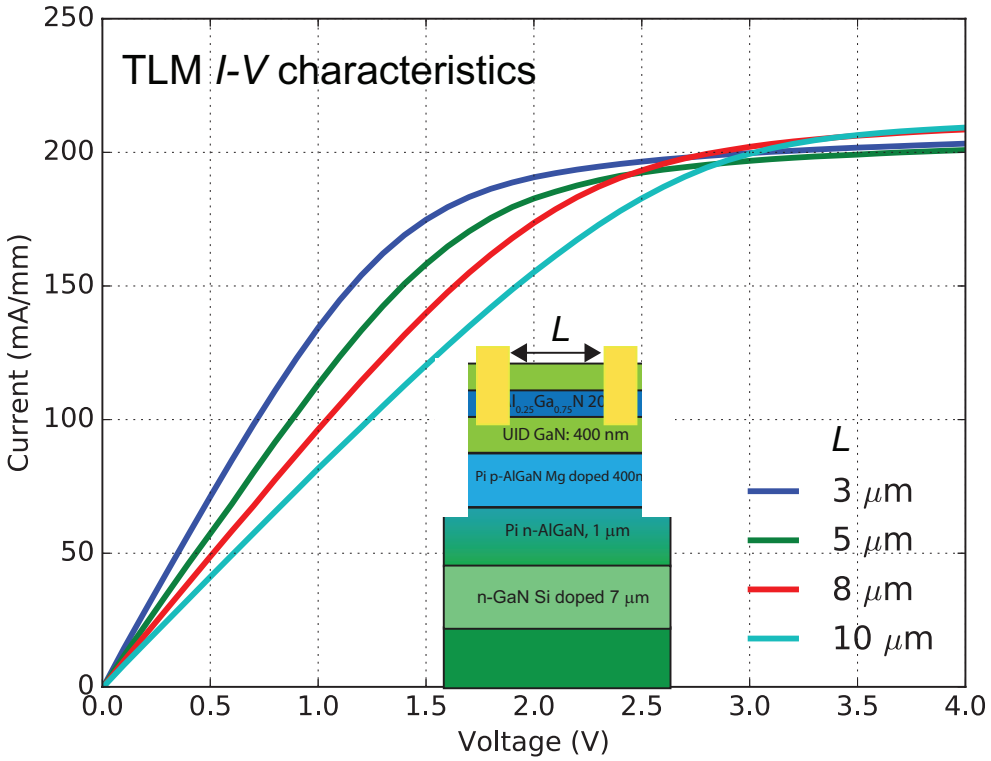

Figure 4.14: Measured *I-V* characteristics of TLM patterns with standard alloyed contacts fabricated on sample 4. A current saturation level of ~200 mA/mm is observed, regardless of separation distance. The current saturation is likely caused by the reduced dislocation density in GaN grown on free-standing GaN substrates, as alloyed ohmic contacts rely on a high dislocation density to achieve good contacts [6].

ohmic contacts do not rely on a high dislocation density. To compare the saturation current level of alloyed contacts and regrown contacts on free-standing GaN substrates, the measured *I-V* characteristics of a pair of alloyed/regrown contacts are plotted in Fig. 4.16. It is seen in Fig. 4.16 that the regrown contacts have a saturation more than 3 times larger than that of alloyed contacts, although the contact resistances are extracted to be both close to 2.0 $\Omega \cdot$ mm. Notice this contact resistance for the regrown contacts is much higher than those reported, especially compared to those for RF application where

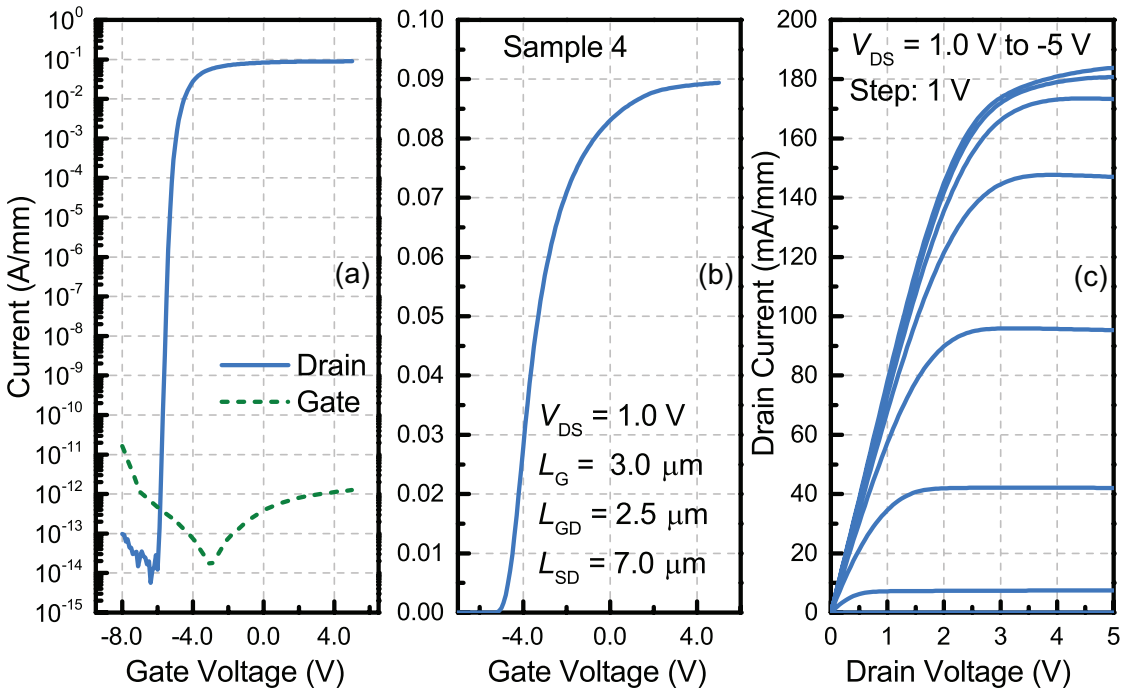

Figure 4.15: Measured *I*-*V* characteristics of the PolarMOSH fabricated on sample 4. The transfer *I*-*V* characteristics are plotted in both semi-logarithmic (a) and linear (b) scale. The family *I*-*V* curves (c) show a maximum saturation current of ~200 mA/mm, which is close to the saturation current observed in Fig. 4.14. This indicated that the drain current in these transistors are limited by the alloyed ohmic contacts.

a contact resistance $< 0.1\ \Omega \cdot$ mm is often reported. This is because: 1. the 2DEG concentration in RF applications is usually much higher ($>1 \times 10^{13}$ cm^{-2} vs. 6×10^{12} cm^{-2}) than that in sample 4; 2. The regrowth condition on free-standing GaN has gone through much less optimization to achieve a good ohmic contacts. With more optimization done, the contact resistance of the regrown contacts are expected to improve.

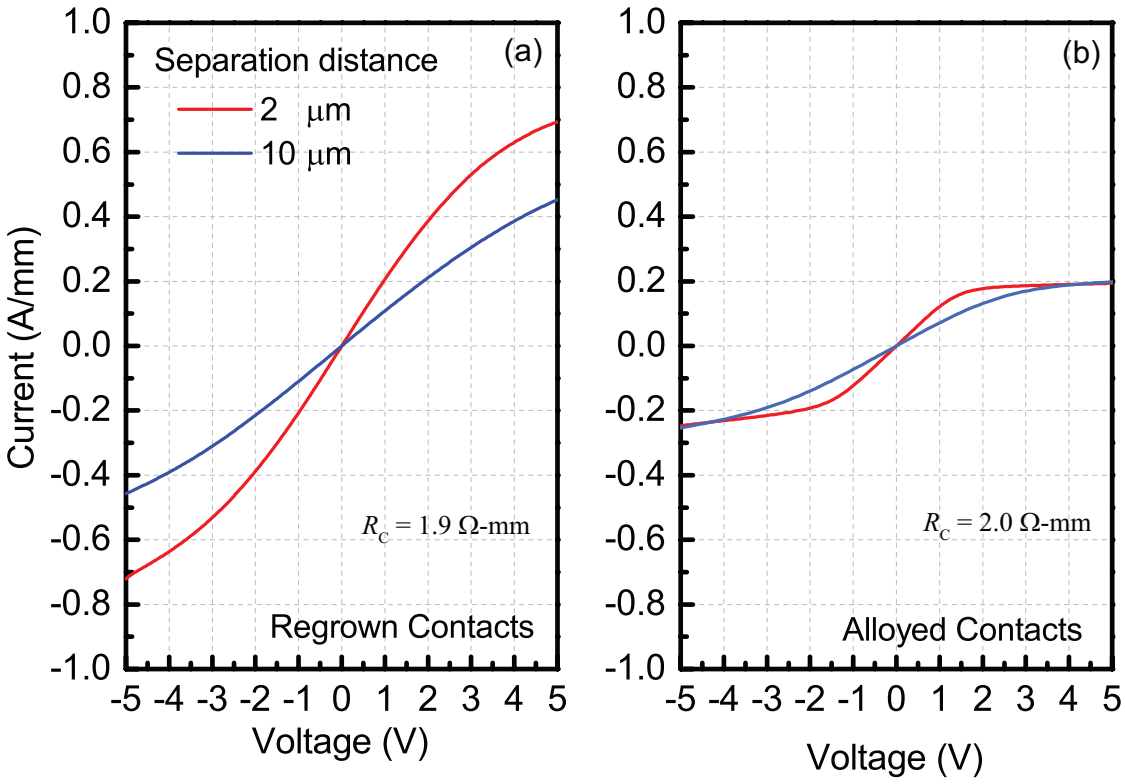

Figure 4.16: Measured *I-V* characteristics of a pair of regrown contacts (a) and alloyed contacts (b) on sample 4. The separation distances between the contacts are 2 μm and 10 μm. Compared to the alloyed contacts, the regrown contacts shows a much larger (> 3X) saturation current.

4.5 Interpreting C-V Characteristics of 2DEG on Conducting Substrates

As describe in section 4.2, a large residue capacitance is often observed when characterizing the 2DEG of a PolarMOSH wafer using capacitance-voltage method. This residue capacitance is larger than the minimum measurable capacitance of the CV meter and can be no trivial compared to the maximum capacitance measured. As a result, the origin of this residue capacitance must be understood in order to accurately probe the 2DEG concentration using *C-V* method. It is worth mentioning that *C-V* method is the preferred method to characterize the 2DEG on conducting substrates as the contactless

probe system and Hall effect measurements are largely overwhelmed by the conducting substrates.

To understand the measured capacitance of the fabricated AlGaN/GaN Schottky barrier diodes on p-type GaN, a capacitance model is built based on the device geometry. The capacitance model and its equivalent circuit is shown in Fig. 4.17. The capacitances measured with and without depletion of the 2DEG are modeled separately in Fig. 4.17(a) and (b). With the 2DEG not depleted, the p-type layer is screened and has no effect on the measured capacitance. The measured capacitance is similar to that on semi-insulating layers and is determined by the capacitance between the anode metal and the 2DEG, as shown in Fig. 4.17(a). However, when the 2DEG underneath the anode is depleted, the measured capacitance is affected by the underlying p-type layer as shown in Fig. 4.17(b). In this case, the measured capacitance is equivalent to two capacitors in serial connection as depicted by the equivalent circuit in Fig. 4.17(c). The measured capacitance then cannot be interpreted simply as the anode capacitance.

The equivalent circuit drawn in Fig. 4.17 shows the need to fully assess the measured capacitance by taking the cathode and the 2DEG in the anode/cathode separation region into account in order to correctly interpret the measured capacitance. However, this analysis can be simplified under the condition that the capacitance between the cathode connected region (cathode and the anode/cathode separation region) and the p-type layer ($C2$) is much larger than that between the anode and the p-type layer ($C1$). When $C2 \geq 10C1$, the total measured capacitance can be approximated to be $C1$ with an accuracy $< 10\%$.

The capacitance model is then verified quantitatively with the Schottky barrier diodes fabricated on sample 3. The measured C-V characteristics for diodes with various anode diameters are plotted in Fig. 4.18. The capacitances with and without the deple-

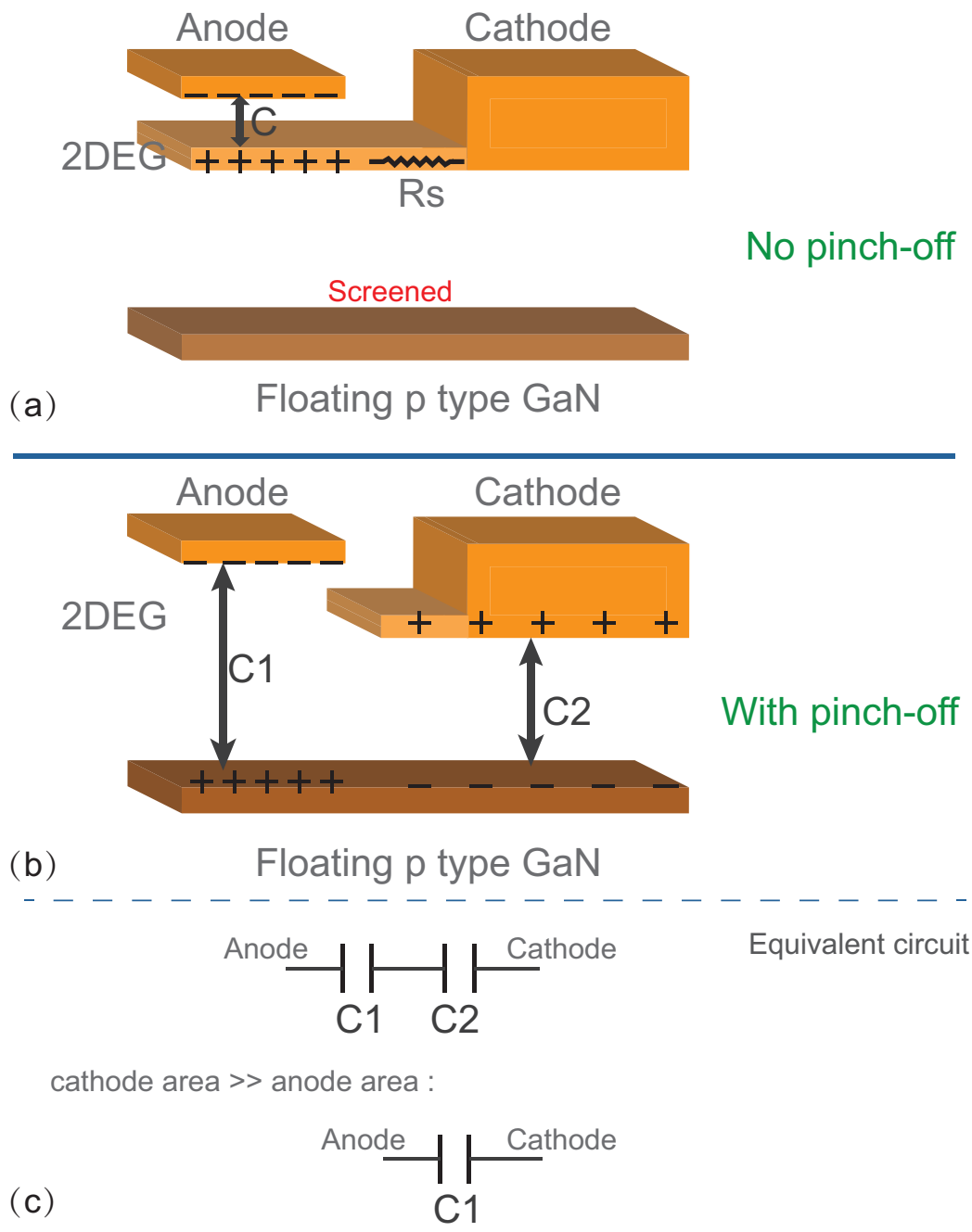

Figure 4.17: Capacitor model for AlGaN/GaN Schottky barrier diodes when (a) $V_{\text{Anode}} > V_{\text{pinch-off}}$ and (b) $V_{\text{Anode}} < V_{\text{pinch-off}}$. The measured capacitance in (a) is determined by the capacitance between the anode metal and the 2DEG, with the p-type layer being screened by the 2DEG. When the 2DEG is depleted by the anode, the measured capacitance in (b) is equivalent to two capacitors in series connection as shown in (c). In the usual case of anode area being far smaller than the cathode area, the measured capacitance is dominated by the capacitance between the anode metal and the underlying p-type layer.

tion of the 2DEG underneath the anode (C_0' and C_0) can be calculated by the following equations:

$$C_0' = \frac{A_{Anode}\epsilon}{t_{GaN\_Top} + t_{AlGaN\_Top} + t_{UID,GaN}} = 17.1 \text{ nF/cm}^2 \tag{4.1}$$

$$C_0 = \frac{A_{Anode}\epsilon}{t_{GaN\_Top} + t_{AlGaN\_Top}} = 93.4 \text{ nF/cm}^2 \tag{4.2}$$

where ϵ is the dielectric constant of GaN/AlGaN, A_{Anode} is the unit anode area and t_{GaN_Top}, t_{AlGaN}, $t_{UID,GaN}$ represent the thickness of the top GaN layer, the top AlGaN layer and the UID GaN layer, respectively. Notice the C_0' has been approximated to the capacitance between the anode metal and the p-type layer, since the fabricated SBDs satisfy the assumption that $C2 \geq 10C1$ as described before. Both calculated capacitance values agree well with the measurement data, showing that the model indeed can correctly explain the C-V characteristics.

The significance of the capacitance model on characterizing 2DEG on a conductive layer through C-V measurement lies in the calculation of 2DEG concentration. On a typical GaN HEMT sample, the 2DEG is on top of a thick semi-insulating layer. Therefore, the measured capacitance is negligible when the 2DEG underneath the anode metal is depleted. The 2DEG concentration can be obtained by integrating the capacitance over the applied voltage from the minimum capacitance to zero bias condition. For a 2DEG on a relatively close p-type layer, however, the integration should be performed between the pinch-off voltage and zero bias condition. This is explained next with measured C-V data.

The comparison of C-V characteristics of Schottky barrier diodes on sample 4 and a regular GaN HEMT wafer is shown in Fig. 4.19. The regular GaN HEMT wafer for comparison here has a 4 μm thick semi-insulating layer. The shaded areas in Fig. 4.19 represents the integrated area for calculation of the 2DEG concentration. The calculated

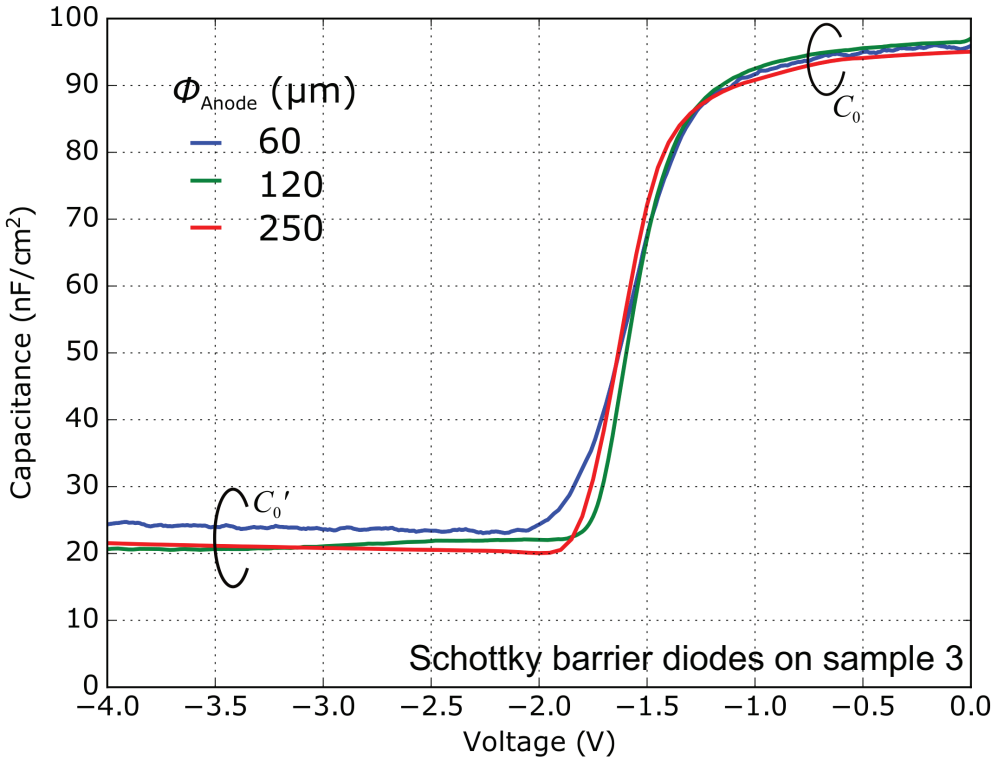

Figure 4.18: Measured C-V characteristics of Schottky barrier diodes fabricated on sample 3. Both C_0 and C_0' can be quantitatively explained by the capacitance model shown in Fig. 4.17.

2DEG concentrations are both consistent with Hall effect measurement results. When the distance between the 2DEG and the p-GaN layer decreases, the residue capacitance (C_0' in Fig. 4.18) increases. It is then more important to exclude the residue capacitance from the 2DEG concentration calculation.

It is also worth mentioning that the application of this capacitance model is not limited to 2DEGs on top of p-type layer. Similar interpretations can be made with 2DEGs on a *conducting* layer. In fact, on GaN HEMT wafers, similar C-V characteristics are observed when the buffer layer is thin[115, 116]. Such not-negligible residue capacitance has not been fully understood in the literature.

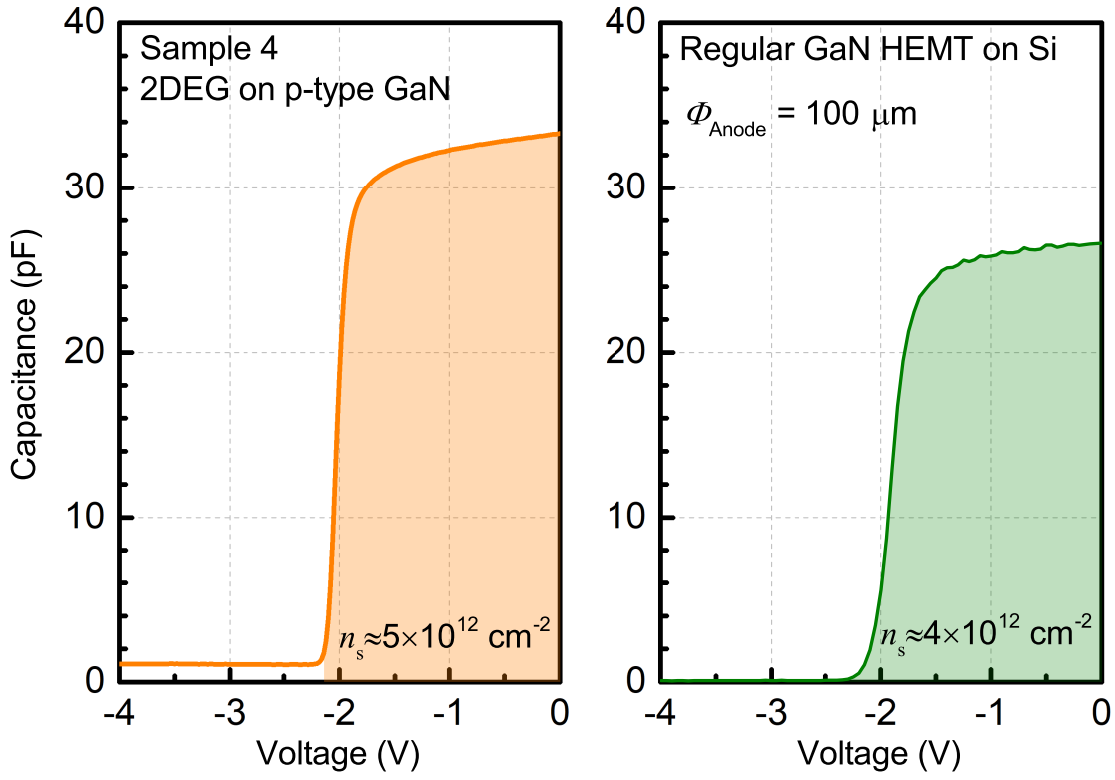

Figure 4.19: Comparison of the *C-V* characteristics of Schottky barrier diodes fabricated on sample 4 and a regular GaN HEMT wafer. The GaN HEMT wafer has a 4 μm semi-insulating buffer layer. The shaded areas shows the integrated area for calculation of the 2DEG concentrations. The calculated 2DEG concentrations are both consistent with Hall effect measurement results.

4.6 PolarMOSH Fabrication Process and Characteristics

Having resolved the issues involved in the fabrication of PolarMOSH including curbing the effect of Mg tail in MOCVD grown material, reducing buffer leakage current and achieving good ohmic contacts to 2DEG on free-standing GaN substrates. PolarMOSH fabrication process is then carried out with MBE regrown contacts on another wafer with epitaxial layers grown by MOCVD on a free-standing GaN substrate. The epitaxial layers grown on this wafer (sample 5, wafer ID: R4509) consists of 200 nm n^+-GaN, 7 μm n^--GaN, 100 nm graded p-AlGaN with Al% graded from 15% to 0% and a Mg concentration of 5×10^{18} cm^{-3}, 250 nm UID GaN, 25 nm $Al_{0.25}GaN$ and 2 nm GaN on

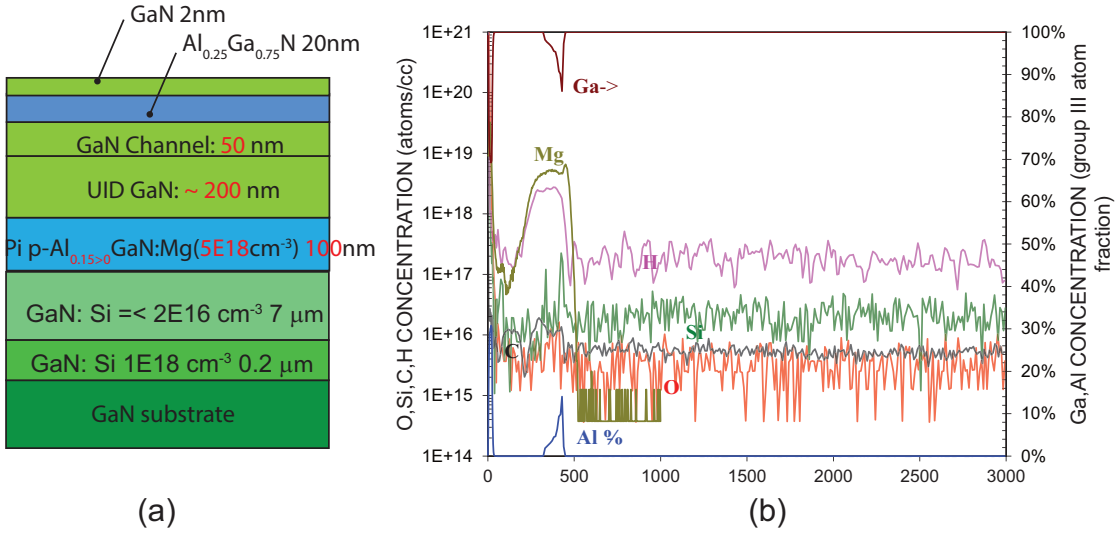

Figure 4.20: (a) Sketch of the epitaxial structure of sample 5 (wafer ID: R4509). (b) Atom concentrations and GaAl composition in sample 5, as measured by SIMS.

top. The epitaxial structure and SIMS results of sample 5 are shown in Fig. 4.20.

SIMS scan show that the Mg impurity has a ~100 nm/decade decay rate in the UID layer and the Mg concentration at the 2DEG channel is $\sim 1 \times 10^{17}$ cm^{-3}. Other unintentionally doped impurities including C and O are close the the SIMS detection limit. As discussed in prior sections, due to the conducting nature of the substrate, proper device isolation and selective contacts are required to characterize the 2DEG by either Hall effect measurement or Lehighton contactless probe system. *C-V* measurement by Hg probe does show a sharp decrease in capacitance, indicating the presence of a 2DEG.

The PolarMOSH fabrication process starts with mesa isolation. SiO_2 is first deposited as hard mask for dry etching. Mesa isolation patterns are then defined by photolithography and SiO_2 etching by buffered HF. After removing the photoresist, the mesa isolation process is completed by Cl_2 based dry etching with inductively couple plasma RIE and subsequent removal of SiO_2 mask by buffered HF. SiO_2 instead of photoresist is selected as the etching mask because it renders a cleaner etched surface and sidewall.

Additionally, photoresist tends to cross-link after a long dry etching process and can be difficult to remove. For the PolarMOSH fabrication described here requires a dry etching >4 minutes and may result in photoresist residue that cannot be removed. It is important to point out that the isolation etching should etch through the p-type layer for proper isolation the active devices and testing structures. For the devices with an isolation etching of only ~100 nm, *I*-*V* and Hall effect measurements are severely distorted by the large leakage current.

Following the mesa isolation etching, ohmic contacts are formed by selective MBE regrowth of n^+-GaN and deposition of Ti/Au by E-Beam evaporator. This is a standard process for MBE regrown contacts and has been described in details in chapter 2. A layer of 20 nm Al_2O_3 is then deposited by ALD as the gate dielectric. The gate pattern is subsequently defined by photolithography. The fabrication process is completed with gate metalization by evaporating Ni/Au and performing lift-off process.

The measured transfer *I*-*V* curves are plotted in both semi-logarithmic and linear scale as shown in Fig. 4.21. Thanks to the low gate and buffer leakage current, an on/off ratio $> 10^8$ is achieved as shown in the semi-logarithmic plot. The minimum substhreshold slope (SS) is calculated to be 90.5 mV/decade.

The family *I*-*V* curves of the PolarMOSH fabricated on sample 5 is shown in Fig. 4.22. Well-behaved drain current saturation and gate modulation of the drain current are observed, indicating good transistor characteristics. A maximum on-current > 0.6 A/mm and a on-resistance $\sim 6\ \Omega \cdot$ mm are achieved. Normalizing the on-resistance by the active device area, the on-resistance translates to a specific on-resistance of 0.25 $m\Omega \cdot cm^2$, which is very competitive even compared to the state-of-the-art GaN vertical devices. These excellent characteristics of the fabricated PolarMOSH shows that the issues brought by the Mg doping in the back barrier have been largely been curbed. The

aforementioned low on-resistance is in part due to the low contact resistance. The TLM (without gates) measurement results show a total metal/2DEG contact resistance of 0.3 $\Omega \cdot$ mm has been achieved with the metal/n^+-GaN contact resistance being as low as 0.07 $\Omega \cdot$ mm. As discussed before, although these values are not as low as the best reported in GaN HEMTs for RF applications where the 2DEG concentration is typically much higher ($>1 \times 10^{13}$ cm^{-2}), they nevertheless represent decent ohmic contacts, especially considering that the contact resistance in power transistors is generally not significant in its contribution to the total on-resistance. In power transistor, where the drift region length ranges from a few micron to hundreds of microns depending on the application, it is usually the drift region that contributes to most of on-resistance.

To further illustrate the importance of incorporate MBE regrown contacts, the family

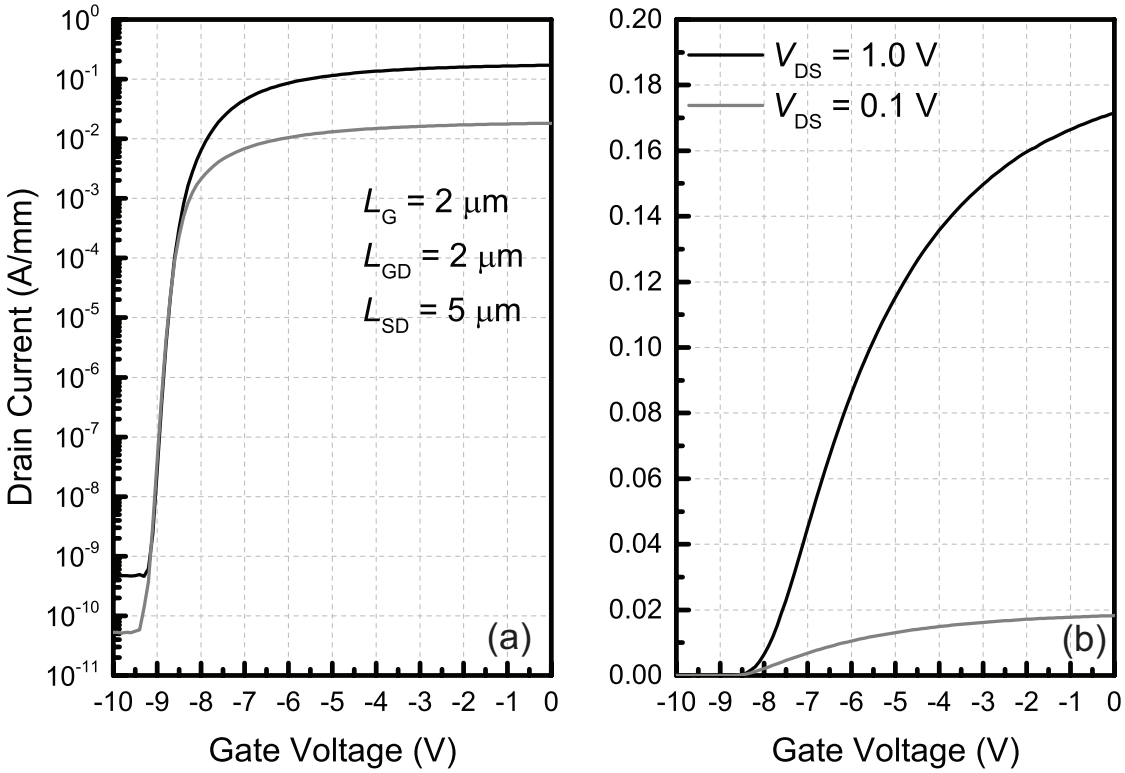

Figure 4.21: Transfer *I-V* characteristics of the PolarMOSH fabricated on sample 5 (wafer ID: R4509) plotted in semi-logarithmic (a) and linear (b) scale. A on/off ratio $> 10^8$ is achieved as shown in the semi-logarithmic plot.

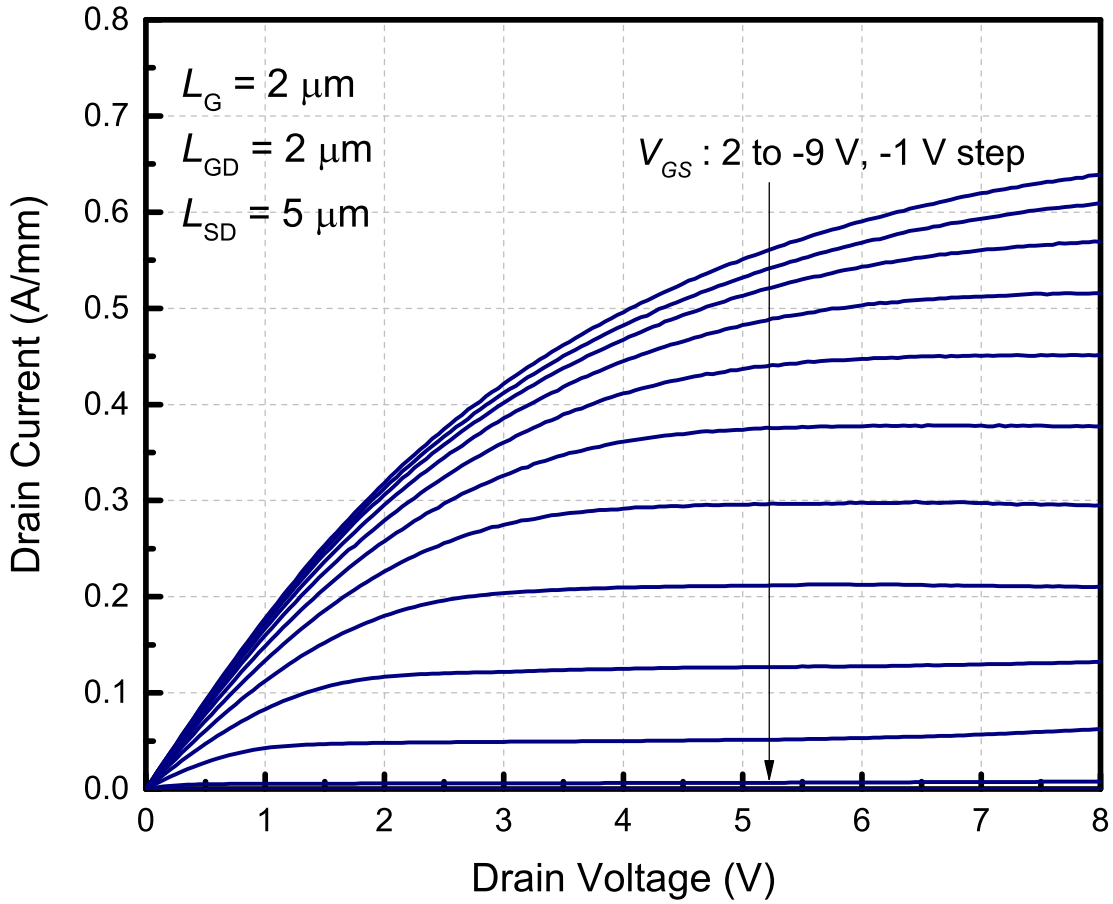

Figure 4.22: Family *I-V* curves of the PolarMOSH fabricated on sample 5. Well-behaved drain current saturation and gate modulation of the drain current are observed.

I-V curves of PolarMOSH fabricated with alloyed contacts and MBE regrown contacts are compared in Fig. 4.23. The PolarMOSH with MBE-regrown contacts shows a maximum on-current that is more than 2 times (> 0.65 A/mm vs. 0.25 A/mm) higher than that with alloyed contacts and similar dimensions. MBE-regrown contacts also leads to a ~70% reduction (6 Ω · mm vs. 20 Ω · mm) in the extracted on-resistance. The pinch-off voltage of the PolarMOSH with alloyed contacts is also different (-5 V vs. -9 V). The exact cause of this difference in pinch-off voltage is not yet clear. However, two factors may have lead to this difference: surface oxidation causing a decrease of 2DEG concentration and interface charge at the Al_2O_3/GaN interface altering the pinch-off voltage.

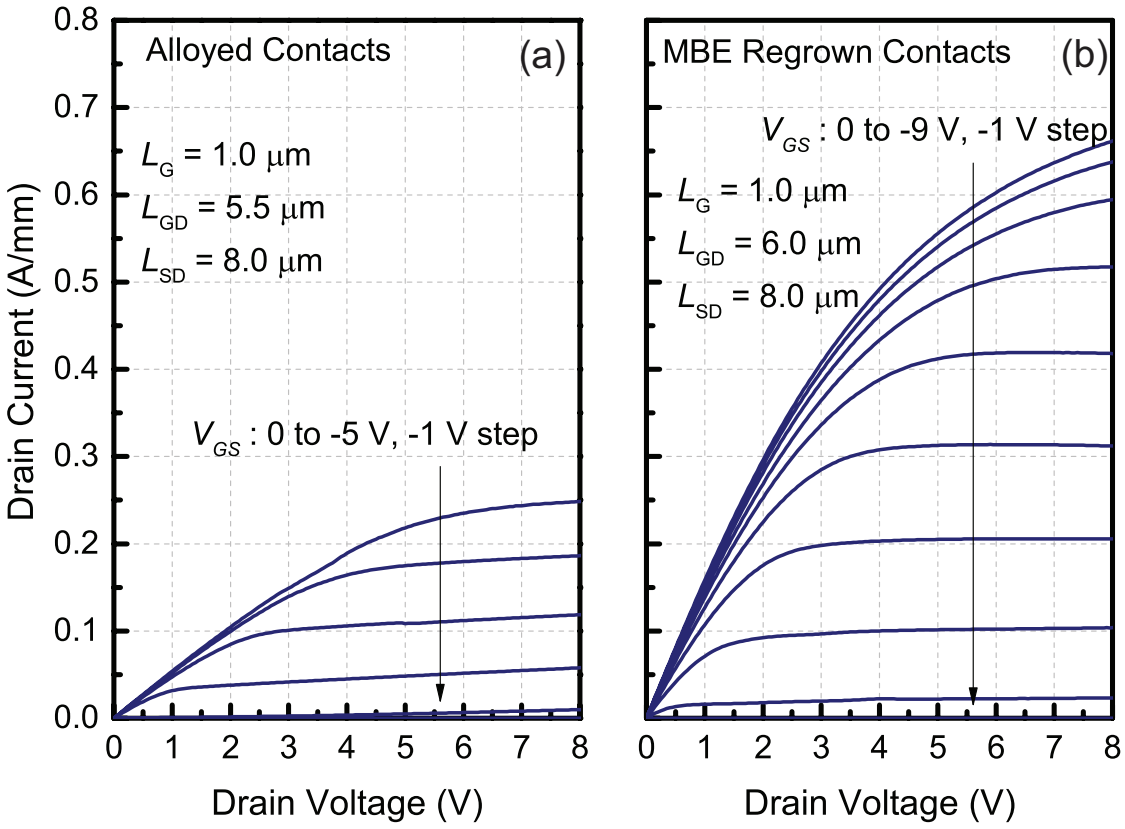

Figure 4.23: Measured family *I-V* curves of PolarMOSH fabricated with alloyed (a) and MBE-regrown (b) contacts.

Another important metric to consider in evaluating GaN HEMTs is its current collapse characteristics. When GaN HEMT is biased with pulsed waveforms whose quiescent condition stresses the transistor at off-state, a decrease in drain current is often observed [117, 118, 119]. This decrease in drain current is referred to as current collapse. Current collapse occurs when the trap states (interface traps or traps in bulk materials) in the transistor, cannot respond fast enough to the applied waveforms. Surface/interface traps are often found to have a large influence on the transistor's current collapse characteristics. MBE-regrown contacts, thanks to its lack of surface oxidation during processing, has been reported to lead to improved current collapse in comparison to alloyed contacts. The comparison of pulsed *I-V* characteristics between PolarMOSH with alloyed contacts and MBE-regrown contacts is shown in Fig. 4.24. In the pulsed

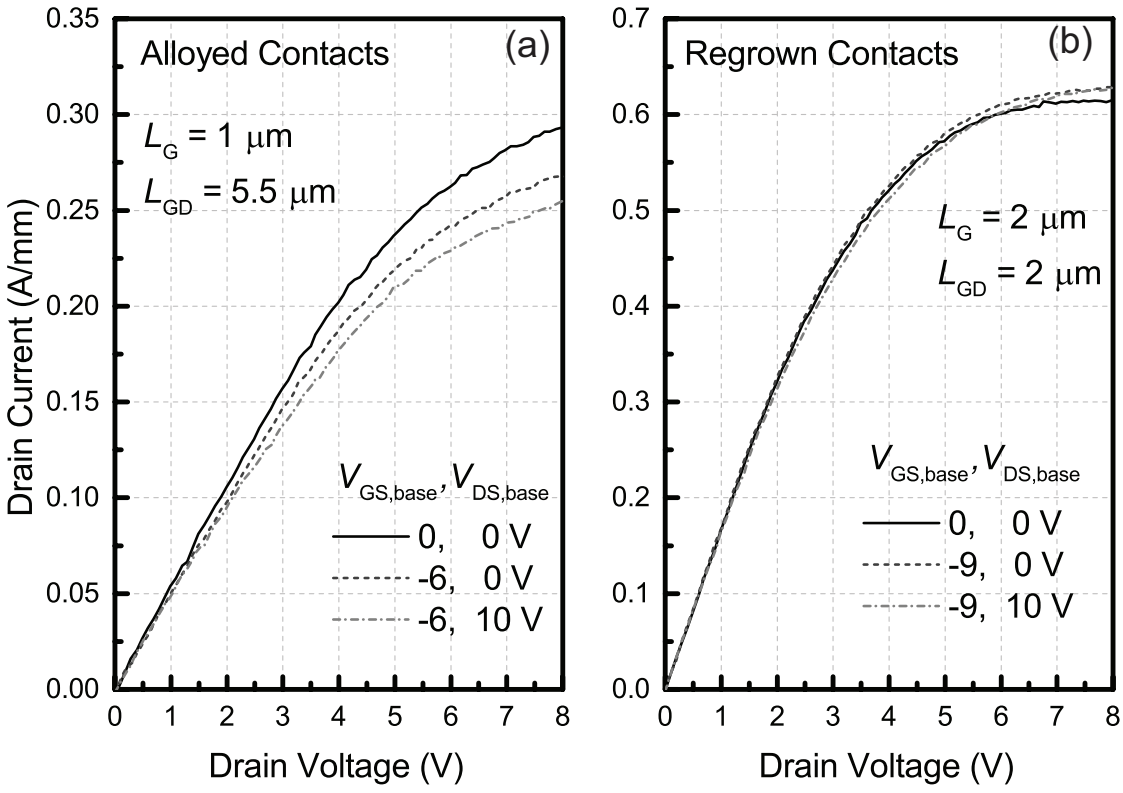

Figure 4.24: Pulsed *I*-*V* characteristics with various quiescent bias conditions for PolarMOSH with alloyed contacts (a) and MBE-regrown contacts (b). The applied voltage pulses have a pulse width of 500 ns and a period of 0.5 ms, leading to a duty cycle of 0.001. This small duty cycle minimizes the effect of self-heating.

I-*V* measurement, synced voltage pulses are applied to both the gate and drain. The quiescent bias conditions are varied to see the effect of gate/drain stress on the drain current. All applied pulse waveforms have a pulse width of 500 nm and a period of 0.5 ms, leading to a small duty cycle of 0.001. This small duty cycle is selected to minimized the self-heating effect. The pulsed drain bias is swept from 0 V to 8 V, while the gate bias is kept at 0 V. A ∼14% drain current collapse (calculated at V_{DS} = 10 V) is observed on the PolarMOSH with alloyed contacts when the transistor is stressed by the gate and drain at the quiescent bias condition. In contrast, the PolarMOSH with MBE-regrown contacts shows no appreciable current collapse at all. While this clearly highlights the benefits of MBE-regrown contacts, it is worth mentioning that even the current collapse in the PolarMOSH with alloyed contacts is quite small compared to GaN HEMTs on

foreign substrates (Si, sapphire or SiC).

4.7 Summary

In conclusion, the development of a GaN MOSHEMT on a graded p-AlGaN back barrier, namely PolarMOSH, is discussed. This development has been a collaborative effort between Cornell University, IQE and Qorvo. The challenges in developing PolarMOSH include minimizing the effect of unintentional Mg concentration on the 2DEG, reducing buffer leakage current and achieving good ohmic contacts.

By incorporating a UID GaN layer on top of the p-AlGaN layer and employing a much lower Mg concentration within the p-AlGaN layer, the Mg concentration at the 2DEG channel is reduced to be as low as $\sim 1 \times 10^{16}$ cm^{-3}, thus showing no obvious effect on the properties of the 2DEG. Even when the Mg concentration at the 2DEG channel is $\sim 1 \times 10^{17}$ cm^{-3}, a decent 2DEG and hence a GaN MOSHEMT with good transistor characteristics.

The buffer leakage issue is largely curbed by employing free-standing GaN substrates instead of foreign substrates like SiC or sapphire. Detailed buffer leakage comparison between epitaxial wafers grown on sapphire substrates and free-standing substrates show that free-standing GaN substrates leads to a 100X reduction in buffer leakage current. Considering the large difference in dislocation density between these two types of substrates, the leakage reduction indicates that the leakage path through the dislocations are largely responsible to the total buffer leakage current.

The issue with alloyed ohmic contacts arises when free-standing GaN substrates are employed. The maximum current measured on a pair of these alloyed contacts are

found to be throttled at a level of 0.2 ~ 0.3 A/mm, regardless of the separation distance. This is likely caused by the low dislocation density in the epitaxial layers grown on free-standing GaN substrates. MBE-regrown contacts, which does not rely on metal diffusion through dislocations, can eliminate the ohmic contact issue.

In the development process, a capacitance model is built to interpret the *C*-*V* characteristics of SBDs fabricated on AlGaN/GaN heterostructures on top of a nearby conducting layer. This capacitance model qualitatively and quantitatively explains the measured *C*-*V* characteristics and provides guideline in calculating 2DEG concentration from the measured *C*-*V* curve. It is also applicable to characterizing 2DEG on a conducting substrates.

Finally, a PolarMOSH with MBE-regrown contacts has been demonstrated with a on/off ratio $> 10^8$, on-current > 600 mA/mm and minimal current collapse observed. The excellent device performance shows the feasibility of fabricating GaN MOSHEMTs on a Mg doped back barrier.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In this work, polarization induced doping in GaN is explored for power applications. This include both the polarization-induced (Pi-induced) two-dimensional electron gas (2DEG) and the more unique polarization-induced bulk doping.

Although tremendous progress has been made in improving the performance of GaN power high electron mobility transistors (HEMTs), which takes advantage of the polarization-induced 2DEG, the lagging performance of GaN 2DEG based diodes is holding the GaN HEMTs back from becoming a integral platform for power applications. The high dislocation density associated with GaN grown on foreign substrates (sapphire and SiC) results in a high reverse leakage current and an early device breakdown. To solve the leakage current and early breakdown issue, a lateral AlGaN/GaN Schottky barrier diode (SBD) with recessed anode and double field plate is developed. This recessed anode and double field plate design put the dislocations out of the focus of reverse leakage current and effectively reduces the reverse leakage current. At the same time, this recessed anode is in direct contact with the 2DEG which reduces the forward turn-on voltage and hence the absolute on-resistance, compared to the traditional planar SBDs. The GaN-on-Si SBD developed based on this design shows a record-breaking breakdown voltage of 1.9 kV and state-of-the-art on-resistance. The excellent performance of this SBD represents a significant advancement of GaN 2DEG based power diodes. The full compatibility of the fabrication process and the competitive cost of GaN-on-Si technology further enhances the potentials of this SBD for power applications.

To exploit the unique Pi-induced bulk doping in GaN for power applications, one must apply this doping technique at a low doping concentration and study the properties of the doped material. A polarization-doped $Al_xGa_{1-x}N$ with a Pi-induced doping concentration $\sim 1 \times 10^{17}$ cm^{-3} is experimentally demonstrated here in this work. The electron mobility is characterized through a combination of *I*-*V* and *C*-*V* measurement. The experimentally obtained electron mobility compares favorably to that reported in impurity doped GaN with a similar concentration, showcasing the potential of Pi-induced bulk doping in power applications. A theoretical model for electron mobility in Pi-doped $Al_xGa_{1-x}N$ and impurity-doped GaN is built based on the experimental data. The theoretical model reveals that dislocation scattering weighs heavily on the electron mobility when the electron concentration is below 1×10^{17} cm^{-3}, for both Pi-doped and impurity-doped materials. It is thus essential to reduce the dislocation density in GaN epitaxial layers as the doping concentrations are lowered to achieve high breakdown voltages in power applications. Fortunately, high quality, free-standing GaN substrates with dislocation densities of 1×10^6 cm^{-2} or even lower recently became available with continuously lowering costs. The low dislocation density of these substrates will translate to the low dislocation densities of the epitaxial GaN materials, and thus retain the advantage of high electron mobility in both Pi-doped and impurity-doped GaN. A n-type doping concentration as low as 3×10^{16} cm^{-3} has recently been achieved with Pi-doping on free-standing GaN substrates (manuscript in preparation by Dr. Kazuki Nomoto), which marks further progress towards utilizing Pi-doping technique for power applications.

One of the key challenges in developing vertical GaN power transistors is realizing GaN n-p-n structures with a high breakdown voltage. Due to the difficulty in activating the buried Mg-doped p-GaN layers the n-p-n structures, MOCVD-grown GaN n-p-n structures with only impurity doping usually show very low breakdown voltages due to the punch-through of the buried p-GaN layer. Incorporating Pi-doping in the buried

p-GaN layer, which does not require an activation process, has been found to greatly increase the measured breakdown voltages of GaN n-p-n structures. A maximum breakdown voltage of 600 V is achieved when the Al composition in the buried p-GaN layer is graded from 7% to 0%. Further improvements in breakdown voltage can be realized by increasing the maximum Al composition.

The Pi-induced bulk doping is put into application in developing the GaN MOSHEMT with a Pi-doped p-$Al_xGa_{1-x}N$ back barrier, referred to as PolarMOSH. In addition to the aforementioned difficulty in activating a buried p-GaN layer, there are three major issues involved in developing PolarMOSH. The first issue is the residue Mg concentration in layers grown on top of Mg-doped GaN by metal-organic chemical vapor deposition (MOCVD). By incorporating a thick UID layer on top of the Mg-doped GaN and reducing the Mg doping concentration in the Mg-doped layer, the Mg concentration at the 2DEG channel is reduced to below 1×10^{17} cm^{-3} and decent 2DEG characteristics are achieved on a Pi-doped p-$Al_xGa_{1-x}N$ back barrier. The second issue is the buffer leakage current observed in PolarMOSH wafers grown on foreign substrates. The buffer leakage is due to the large dislocation density in the materials grown on these substrates. The employment of high quality, free-standing GaN substrates largely curbs the leakage current and enables the realization of well-behaved transistor characteristics on the PolarMOSH wafer. The third issue is the difficulty in making good ohmic contacts to the 2DEG through the standard alloy process when free-standing GaN substrates are used. This issue is solved by deploying non-alloyed contact regrown by molecular beam epitaxy (MBE). As a result, a PolarMOSH with high on/off ratio ($>10^8$), large on-current (>600 mA/mm), low on-resistance (0.25 $m\Omega \cdot cm^2$) and minimum current collapse has been demonstrated. As PolarMOSH is an integral component of the GaN vertical power transistor, referred to as PolarMOS, the demonstration of PolarMOSH is an important stepping stone in realizing PolarMOS and eventually exploiting Pi-induced

bulk doping for power applications.

5.2 Future Work

5.2.1 GaN Vertical Diodes

The availability of high quality, free-standing GaN substrates is set to transform GaN power devices as fully vertical devices can be made with epitaxial materials grown on such bulk substrates. One of the devices that has been made possible by the free-standing GaN substrates is the fully vertical Schottky barrier diodes. Fully vertical SiC SBDs with an operating voltage up to 1700 V are already commercially available, while fully vertical GaN SBDs are still lagging behind in reported performance in the literature with the highest reported breakdown voltage of ~1100 V [73]. One way to improve the breakdown voltage of vertical GaN SBDs is to lower the net doping concentration. Due to the high background impurity concentration, the net doping concentration [76, 31] in the n^--GaN is generally higher than that in SiC. However, with the improvements in GaN epitaxy, the background impurity concentration keeps decreasing. Consequently, the net doping concentration is also decreasing, making it more suitable for fabrication of high voltage SBDs.

Another way to improve the breakdown voltage of vertical GaN SBDs is to adopt polarization-induced doping in the drift region [120, 121]. For Pi-doped $Al_xGa_{1-x}N$, the highest Al composition resides at the surface, which suspends the highest electric field under reverse bias. Since $Al_xGa_{1-x}N$ has a wider band gap and larger breakdown field, it leads to a larger breakdown field in the SBD and thus a higher breakdown voltage can be achieved. The challenge in implementing such devices lie in good epitaxy control

to bring the Pi-induced doping concentration close to that of impurity doping. Some preliminary results of vertical GaN SBDs with Pi-induced doping in the drift region is described next.

The epitaxial layers grown by MOCVD consists of 0.2 μm n^+-GaN/7 μm n^--GaN/1 μm Pi-doped $Al_xGa_{1-x}N$. The Pi-doped $Al_xGa_{1-x}N$ is realized by linearly grading the Al composition from 0% at the bottom of the layer to 7% at the surface (wafer ID: R4387). A control wafer, having identical layer structure except the top layer being replaced by a impurity-doped n^--GaN (wafer ID: R4386), is also grown for comparison. All epitaxial layers are grown by MOCVD along *c*-axis on free-standing Ga-face GaN substrates. The Schottky barrier diode fabrication process starts with deposition of 200 nm SiO_2 by plasma enhanced chemical vapor deposition (PECVD), followed by anode lithography and wet etching of SiO_2 by buffered HF. The anode metal of Ni/Au is then deposited by e-beam evaporator. For SBDs without field plates, the anode area is smaller than the wet etched area. The cathode contacts are formed by depositing Ti/Au by e-beam evaporator on the back of the sample.

C-*V* measurements show that the Pi-doped $Al_xGa_{1-x}N$ has a doping concentration of $\sim 2.5 \times 10^{16}$ cm^{-3}, while the impurity-doped n^--GaN has a doping concentration of $\sim 1 \times 10^{16}$ cm^{-3}. The forward *I*-*V* characteristics of the fabricated SBD with Pi-induced doping is plotted in Fig. 5.1 in both linear and semi-logarithmic scales. A low turn-on voltage of ~0.7 V, high current density of 2000 A/cm^2 at 2 V forward bias and a low ideality factor of ~1.1 are observed. These forward characteristics are already close to the state-of-the-art specifications for vertical GaN SBDs.

The reverse *I*-*V* characteristics of SBDs with and without field plate, fabricated on both the wafer with Pi-induced bulk doping and the control wafer are plotted in Fig. 5.2. A boost in breakdown voltage by the addition of field plate is clearly seen for SBDs

fabricated on both wafers. More importantly, a higher breakdown voltage of >400 V (vs. ~375 V) is observed on the wafer with Pi-induced doping, despite the higher doping concentration at the end of the drift region.

Considering that the maximum Al composition in this wafer is only 7% and the doping concentration is relatively high, a much larger boost in breakdown voltage can be expected in the future when the maximum Al composition can be increased and the doping concentration be decreased at the same time. Notice that, a lower Pi-induced doping concentration yet a higher maximum Al composition requires the Al composition to be graded over a much thicker layer. More improvement in the control of Al composition and the strain associated with thick AlGaN growth during epitaxy is needed to fully realized the potential of Pi-induced doping in vertical GaN SBDs.

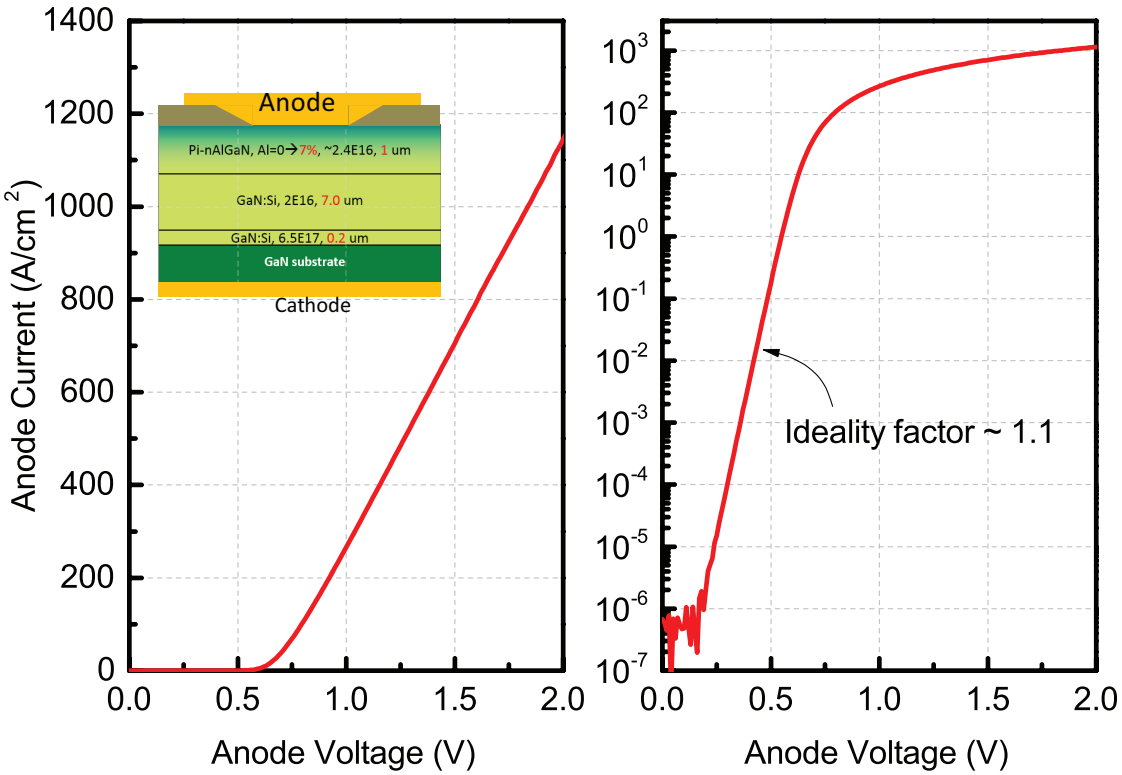

Figure 5.1: Forward *I-V* characteristics of SBDs with Pi-induced doping in the drift region.

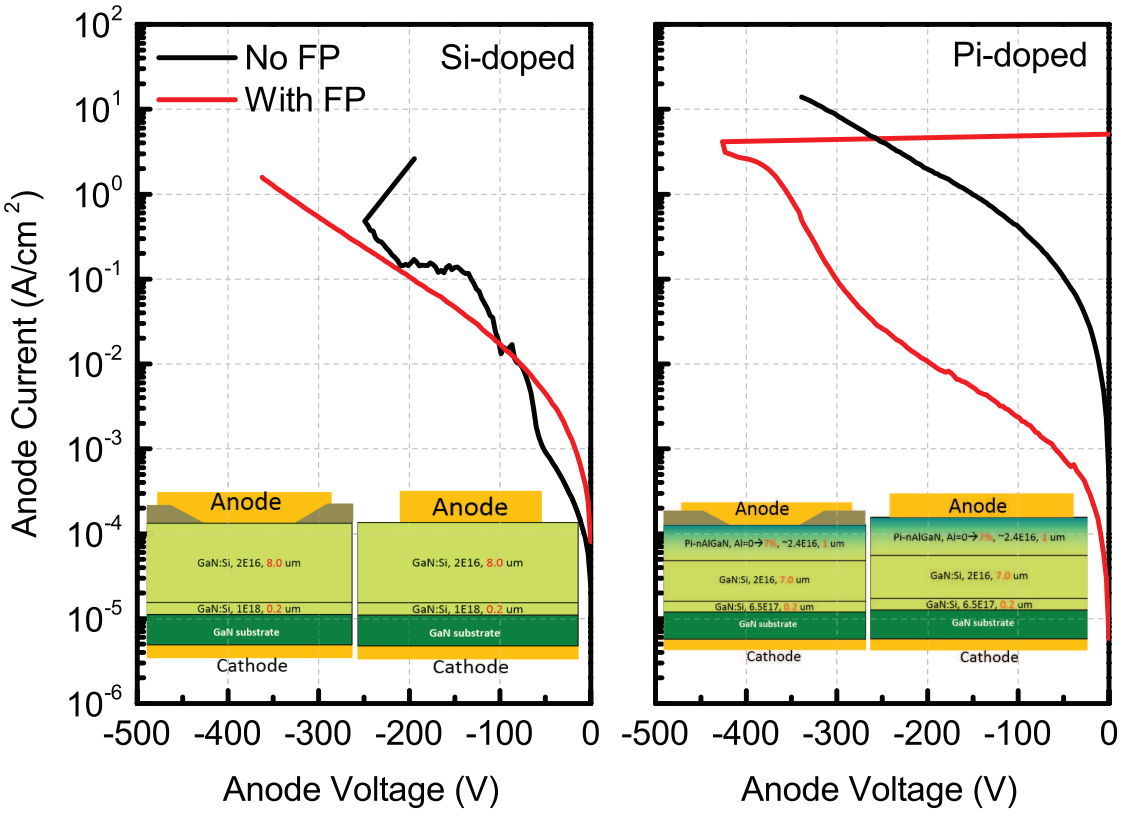

Figure 5.2: Comparison of *I*-*V* characteristics of SBDs with Pi-induced doping (wafer ID: R4387) and impurity doping (wafer ID: R4386). Both SBDs with and without field plate are fabricated on each wafer.

The reverse leakage current shown in Fig.5.2 is also noticeably high, especially compared to GaN p-n diodes where the leakage current could stay below 1×10^{-6} A/cm^2 at a reverse bias beyond 1000 V. To reduce the reverse leakage would also require improvement in epitaxy as well as surface passivation technique. More advanced edge termination techniques [122, 76, 123] can also be applied to boost the breakdown voltage.

5.2.2 Vertical GaN Power Transistors

PolarMOS

Vertical transistor's great potential in scaling up the conduction current and the recent availability of free-standing GaN substrates have driven the research in GaN vertical GaN power transistors. Some impressive progress has been reported in the literature recently. The reported GaN UMOS-like vertical transistors have reached a breakdown voltages of 990 V[124] on a 480 μm^2 active area and >600 V on a large 0.5 mm^2 active area [125]. GaN static induction transistor, also called vertical fin transistor, is reported to reach a breakdown voltage of 800 V at an active area of 900 μm^2. GaN vertical transistors with regrown channel, also have been reported to reach breakdown voltages as high as 1.5 kV [126] and 1.7 kV [127]. These advancements of vertical GaN transistors showcase the potential of GaN in high power, high current applications.

Meanwhile, the vertical GaN power transistor enabled by polarization-induced doping, referred to as PolarMOS is the ultimate high-speed power transistor [2]. The cross-section schematic of the PolarMOS is shown in Fig. 5.3. The high breakdown voltage of PolarMOS is enabled by the thick drift layer made of either impurity or polarization doped n^--GaN ($N_D \leq 1 \times 10^{16}$ cm^{-3}). The p-type region of the body p-n diode is formed by polarization-induced doping. This polarization-doped p-AlGaN can achieve full ionization of acceptors over its Mg-doped counterpart, thus reducing the frequency dispersions associated with high activation energy of Mg in GaN. Another important benefit of this deive design is that the maximum electric field, expected to be at the lower corner of the p-AlGaN region, lies inside the $Al_xGa_{1-x}N$ which has a higher band gap and breakdown electric field than GaN. This brings PolarMOS an edge in breakdown voltage over other purely GaN based transistors. On top of the p-type GaN and

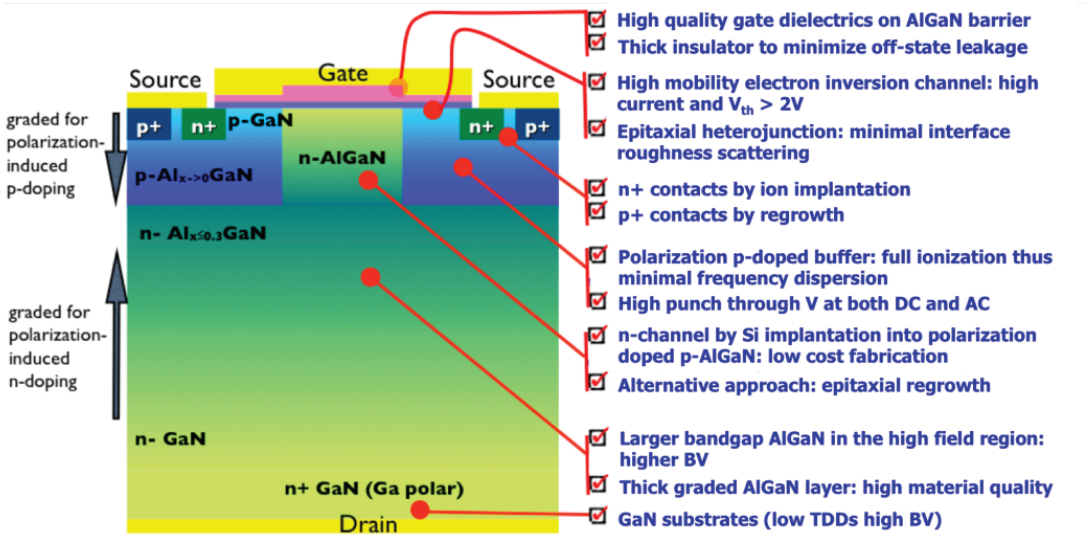

Figure 5.3: Fig.3 The ultimate GaN power transistor PolarMOS, featuring AlGaN in the high field region to achieve higher breakdown voltage, polarization p-doped buffer to achieve full dopant ionization, thus minimizing frequency/temperature dispersion and enabling high punch through voltage at both DC and AC, high mobility electron inversion channel for high current and adjustable threshold voltage > 2 V. Reproduced from ref. [2]

n^--$Al_xGa_{1-x}N$ sits a thin unintentionally doped GaN, a thin AlGaN top barrier and a gate dielectric layer. The high quality of the epitaxial interface between the AlGaN top barrier and the UID GaN ensures a high electron mobility and thus a low channel resistance. The p-type back barrier [128, 129], along with the sub-critical thickness AlGaN top barrier [130] enables a threshold voltage >2 V.

Simulation results on PolarMOS, shown in Fig. 5.4, suggest that PolarMOS promises a higher $BV^2/R_{ON,SP}$ and thus an outstanding performance among other solutions with a similar breakdown voltage. The key challenge in realizing PolarMOS is in implementing the current aperture structure, as has been observed in CAVET devices [108, 109, 131]. This current aperture structure can be fabricated by either regrowth or ion implantation, both require more extensive research to achieve high voltage devices.

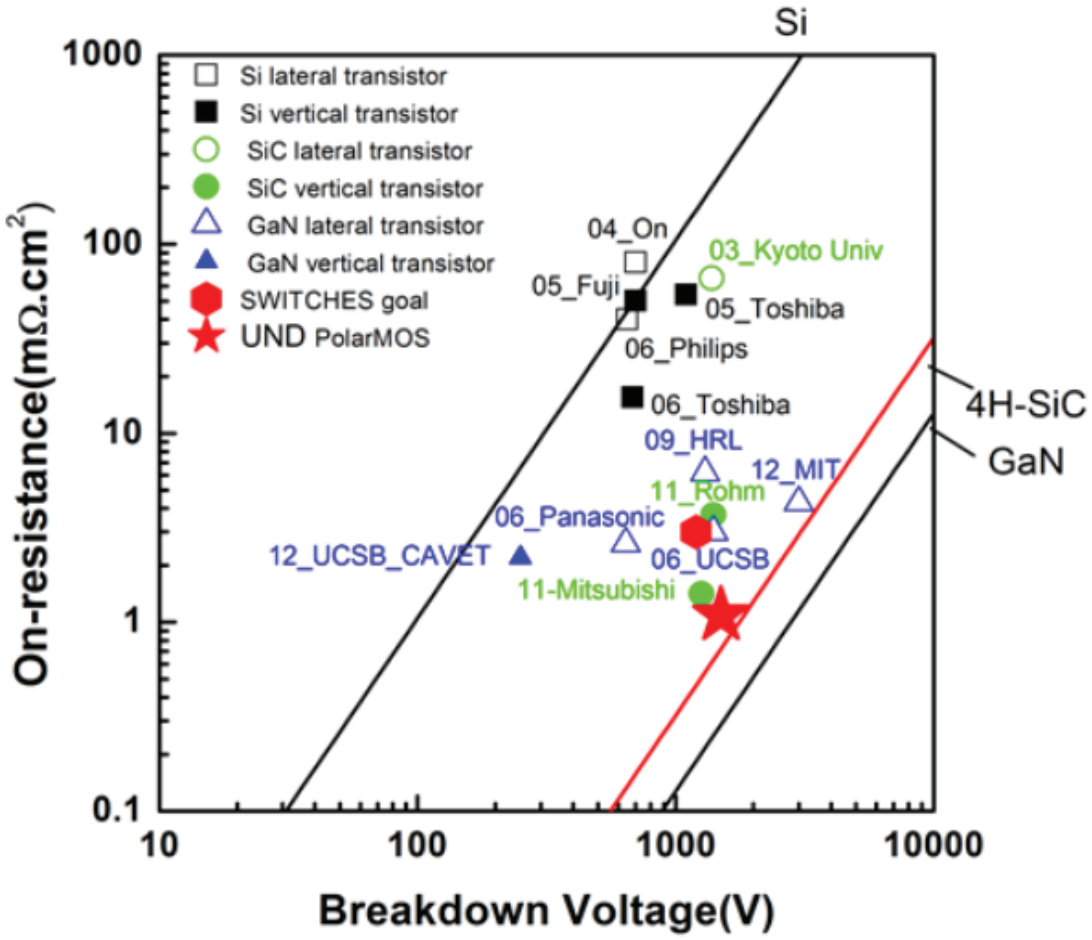

Figure 5.4: Benchmark of power transistors near V_{Br} of 1000 V. In advanced device architectures such as IGBT and superjunction MOS, Si power devices surpass the theoretical limit of unipolar devices. Both SiC and GaN power transistors exhibit room for improvement. GaN PolarMOS stands out compared to other solutions, promising a higher $V_{\mathrm{Br}}^2/R_{\mathrm{ON,SP}}$ figure of merit. Reproduced from ref. [2]

APPENDIX A

ERROR ANALYSIS OF SPLIT-CV METHOD IN MESFET

Split-CV method, which extracts carrier mobility through a combination of *C*-*V* and *I*-*V* measurements has been widely adopted in evaluating carrier mobilities in MOSFETs [132, 133]. As the split-CV method is based on transistors after complete fabrication processes, it is particularly valuable in its capability in evaluating the effect of fabrication processes of on the channel mobility [134, 135]. The errors of the channel electron mobility in MOSFETs extracted through split-CV method have been well studied and documented [136, 137] through experiments and simulations. However, the error analysis of MESFET based split-CV method has not been reported. In this chapter, the errors associated with the MESFET based split-CV method is analyzed and the corrections to improve its accuracy is evaluated through simulation.

A.1 Derivation of Electron Concentration Extraction by *C*-*V* Method

One of the prerequisites of the MESFET based split-CV method is to extract the carrier concentration profile of the MESFET channel. Using a MESFET with a n-type doped channel as an example, the extraction is carried out by following these equations:

$$C = \frac{A \times \varepsilon}{W}, \tag{A.1}$$

Where C is the measured capacitance, A is the gate area, W is depletion depth at the applied voltage and ε is the dielectric constant of the channel material. The measured capacitance C can also be written as:

$$C = \frac{dQ}{dV} = \frac{A \times q \times N(W) \times dW}{dV}, \tag{A.2}$$

where $N(W)$ is the doping (electron) concentration at the depth W, q is the electron charge. Incorporating the following equation

$$\frac{dW}{dV} = \frac{dW}{dC}\frac{dC}{dV}, \tag{A.3}$$

the n-type doping concentration is then expressed as

$$N(W) = n = -\frac{C^3}{A^2 \times \varepsilon \times q \times (dC/dV)} = \frac{2}{A^2 \times \varepsilon \times q \times (d(1/C^2)/dV)}. \tag{A.4}$$

Notice that in deriving these equations, it is assumed that all n-type doping concentration is equal to the free electron concentration, which is true for most n-type GaN with a low doping concentration ($<2 \times 10^{17}$ cm^{-3}) and minimal amount of compensation centers.

A.2 Derivation of Mobility Extraction

Excluding the effects of parasitic resistance, the drain current measured on a long-gate MESFET, under a small drain bias voltage ($V_{DS} \ll V_{Th}$) can be written as:

$$I_D(V_{GS}) = W_G \times \int_{dep(V_{GS})}^{t_{epi}} n(x) \times q \times \mu(x) \times E_{Channel} dx, \tag{A.5}$$

where W_G is the gate width, dep is the depletion depth, x is the depth from surface, n is the electron concentration at the depth of x, $\mu(x)$ is the electron mobility at the depth of x and $E_{Channel}$ is the channel electric field. This drain current expression is written based on the assumption that the electron concentration and the depletion depth across the gate is uniform. It is important that the applied drain voltage is low enough to make these two assumptions valid. Taking the derivative over V_{GS} on both sides of Eq. A.5, the following equation can be obtained:

$$\frac{d(I_D(V_{GS}))}{dV_{GS}} = -W_G \times n(dep(V_{GS})) \times q \times \mu(dep(V_{GS})) \times E_{Channel} \times \frac{d[dep(V_{GS})]}{dV_{GS}}. \tag{A.6}$$

By re-arranging Eq. A.6, the electron mobility can be extracted by:

$$\mu(dep(V_{GS})) = -\frac{d(I_D(V_{GS}))}{dV_{GS}} \frac{1}{W_G \times n(dep(V_{GS})) \times q \times E_{Channel}} (\frac{d[dep(V_{GS})]}{dV_{GS}})^{-1}. \quad \text{(A.7)}$$

$$n(dep(V_{GS})) = \frac{2}{q \times \varepsilon \times A^2 \times d(1/C^2)/dV} \quad \text{(A.8)}$$

$$dep = \frac{A \times \varepsilon}{C} \quad \text{(A.9)}$$

A.3 Simulation Setup and Results

To analyze the errors of MESFET-based split-CV method, two-dimensional *I*-*V* and *C*-*V* simulations are performed using Sentaurus TCAD. The analysis is carried out with simulation because there is no uncertainties in the actual channel mobility, since it can be preset to a precise value. By comparing the extracted mobility to the preset value, one can evaluate the errors associated with the split-CV method and the efficacy of various corrections.

In the simulation, a MESFET with a cross-section shown in A.1 is simulated. The electron mobility is set to be a constant value of 1200 $cm^2/V \cdot s$. The device dimensions and the layered materials are specified in the cross section. The gate length is varied from 7 μm to 20 μm. The ohmic contact resistance is set to be 0.5 $\Omega \cdot mm$ for both source and drain. The simulated *C*-*V* characteristics, plotted in Fig. A.1, is similar to that observed in experiment as shown in chapter 3. The capacitance step in Fig. A.1 corresponds to the depletion region reaching the semi-insulating GaN. *I*-*V* simulations also show well-behaved MESFET transfer and output characteristics.

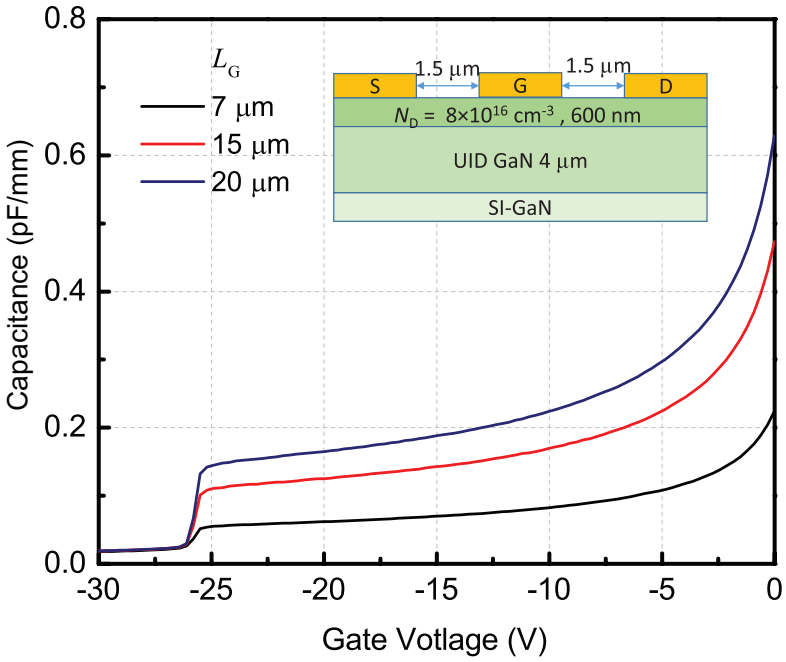

Figure A.1: Simulated *C-V* characteristics of MESFETs with various gate lengths. The MESFET cross section schematic is shown in the inset figure.

A.4 Parasitic Resistance and Capacitance Correction

Taking the source and drain parasitic resistance into consideration, the channel electric field can be corrected as:

$$E_{Channel} = \frac{V_{Channel}}{L_{Gate}} = \frac{V_{DS} - I_D \times R_{S,D}}{L_{Gate}} = \frac{V_{DS}}{L_{Gate}}(1 - \frac{R_{S,D}}{R_{S,D} + R_{Channel}}). \tag{A.10}$$

In the simulation, the parasitic resistance is extracted by simulating MESFETs with identical dimensions other than the gate length. By plotting total resistance versus gate length, the parasitic resistance can be extracted. As a result, the electron mobility profile extracted with and without the parasitic resistance correction is plotted in Fig. A.2. It is seen that the extracted electron mobility based on a L_G = 20 μm MESFET has a smaller error compared to that extracted using a a L_G = 7 μm MESFET. And the parasitic resistance corrections shows a much larger improvement in the accuracy of the extracted electron mobility for the MESFET with a smaller gate length. These observations are

understandable since the parasitic resistance bears a larger impact on the total resistance for the device with a smaller gate length. A smaller gate length also results in a higher channel electric field, impacting the validity of the uniform electron concentration assumption.

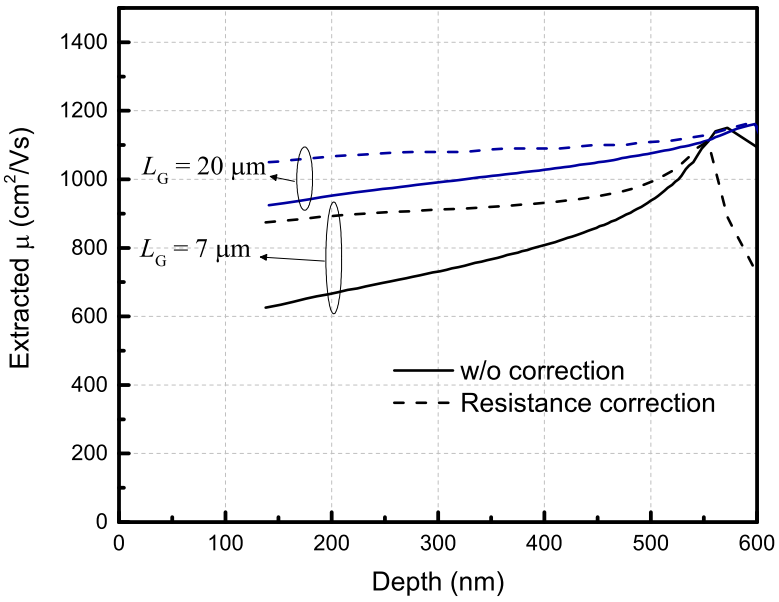

Figure A.2: Extracted electron mobility profiles with and without parasitic resistance correction, for MESFETs with gate lengths of 7 μm and 15 μm. A drain-source bias of 0.1 V is used for the *I*-*V* simulation.

Another trend observed in Fig. A.2 is that the impact of the parasitic resistance correction decreases as the depletion depth increases. This is due to the significance of the parasitic resistance being reduced by the increasing channel resistance as the depletion depth increases. It is seen from Fig. A.2 that it is important to perform the parasitic resistance correction for improved accuracy of the extracted channel electron mobility.

Besides the parasitic resistance correction, another important correction to consider is the parasitic capacitance correction, especially for MESFETs with a small gate length.

In aforementioned derivations, it is assumed that the measured capacitance is equal

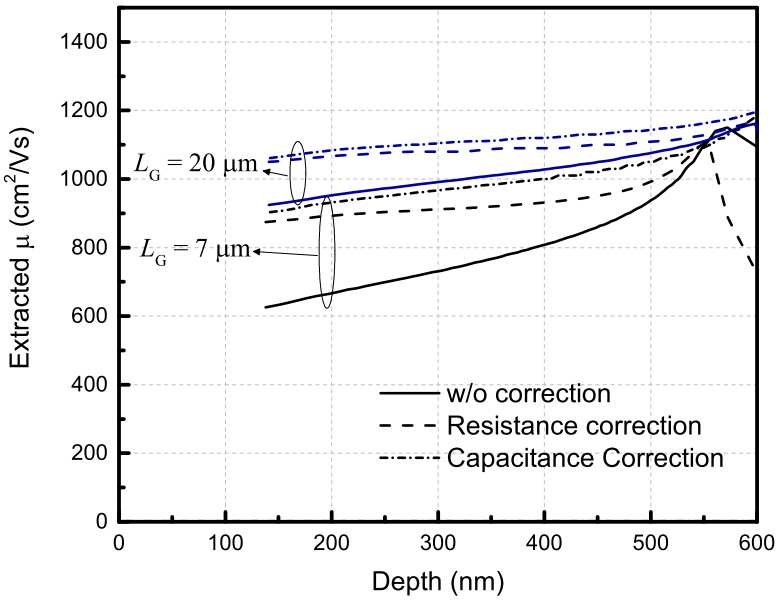

Figure A.3: Extracted electron mobility profiles with and without parasitic capacitance correction, for MESFETs with gate lengths of 7 μm and 15 μm. A drain-source bias of 0.1 V is used for the *I*-*V* simulation.

to the gate capacitance. However, parasitic capacitance can not be avoided during in capacitance measured. The parasitic capacitance can be extracted similar to the extraction of parasitic resistance. And the channel capacitance can be written as:

$$C_{Channel} = C_{Measured} - C_{Parasitic}. \tag{A.11}$$

The impact of parasitic capacitance correction on the extracted electron mobility is plotted in Fig. A.3. It is seen that the parasitic capacitance correction results in only a marginal improvement on the accuracy of the extracted mobility for a MESFET with L_G = 15 μm, while the improvement is much more noticeable on a MESFET with L_G = 7 μm.

To have a quantitative insight into the impact of the parasitic resistance and capacitance correction, the average extracted electron mobility is calculated and plotted in Fig. A.4, along with its percentage error. While the accuracy improvement brought by the parasitic resistance correction is noticeable for both L_G = 7 μm and L_G = 15 μm

MESFET, the parasitic capacitance correction on a L_G = 15 μm MESFET only results in a 1% improvement in the accuracy of the extracted electron mobility.

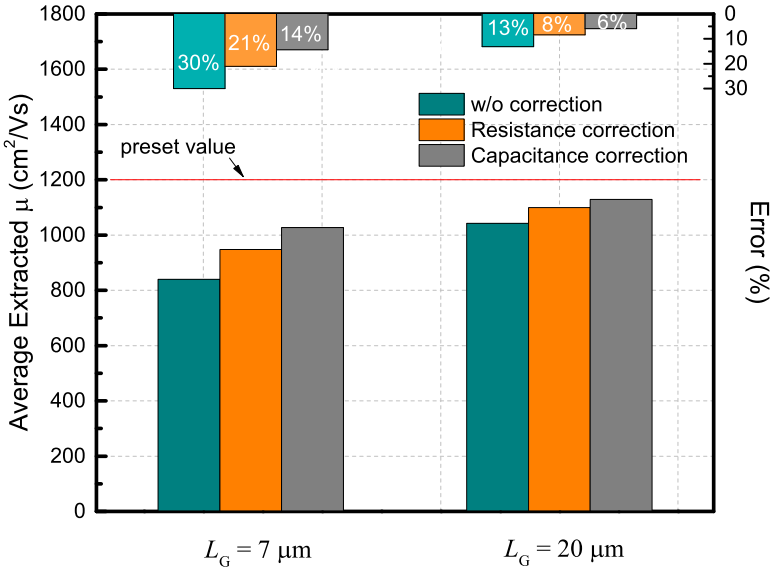

Figure A.4: The impact of the parasitic resistance and capacitance correction on the average extracted electron mobility and its percentage error for MESFETs with L_G = 7 μm and L_G = 15 μm.

A.5 The Effect of Drain Voltage

The accuracy of split C-V method depends on the validity of the constant electron concentration assumption. When a high drain voltage is applied in the *I*-*V* measurement, the electron concentration at the drain end of the channel starts decreasing as a result of increased drain-gate voltage. This could result in a significant degradation in the accuracy of the extracted electron mobility.

To understand the quantitative limits of the applied drain voltage, electron mobility profiled extracted with different drain bias voltages are plotted in A.5. Both parasitic resistance and capacitance corrections are performed. A severe degradation of the accu-

racy of the extracted electron mobilities is observed when the drain bias voltage exceeds 1 V on a L_G = 20 μm MESFET. No significant influence of V_{DS} is seen as long as V_{DS} < 1 V.

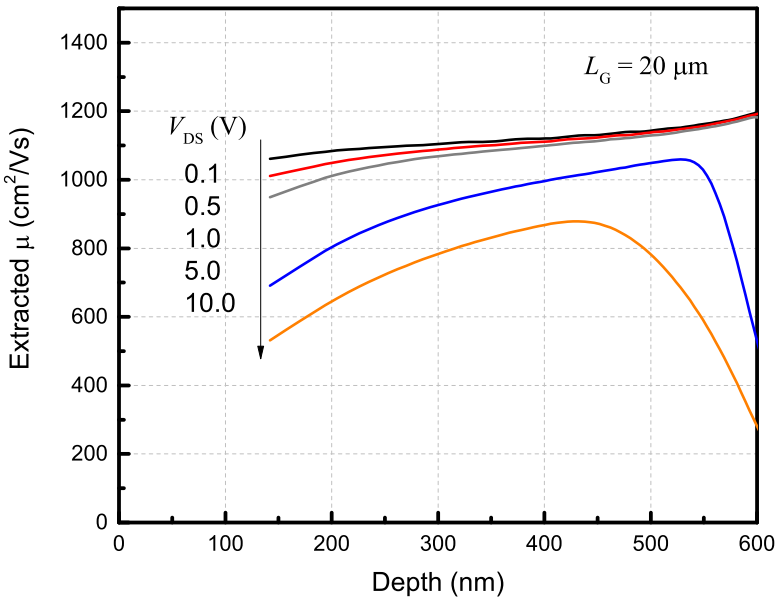

Figure A.5: Electron mobility profiles extracted with different drain bias voltages. Both parasitic resistance and capacitance corrections are performed. A severe degradation of the accuracy of the extracted electron mobilities is observed when the drain bias voltage exceeds 1 V on a L_G = 20 μm MESFET.

A.6 Conclusion

In this section, the errors associated with MESFET based split-CV method is studied through simulation results. By comparing the extracted electron mobility with the pre-set value, the error is quantitatively assessed. The significance of parasitic resistance and capacitance correction, and the effect of drain bias voltage are all evaluated quantitatively.

The results show that for a L_G = 20 μm MESFET, parasitic resistance correction

brings a noticeable improvement in accuracy while parasitic capacitance results in only a marginal difference. Meanwhile, the drain bias voltage has a insignificant influence on the extracted mobility when it is below 1 V on a L_G = 20 μm MESFET.

These results show that mobility extraction shown in chapter 3 has an good accuracy $\sim$ 10%. They also provide quantitative insights into the accuracy of MESFET based split-CV method in general and can serve as a guideline in performing split-CV measurements.

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