VARIATION TOLERANT CALIBRATION CIRCUITS FOR HIGH PERFORMANCE I/O

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Continuous scaling of CMOS processes leads to increasing integration of digital and analog subsystems on one chip. But the impact of process variation on these analog blocks is more pronounced than on the digital components, which raises the need for accurate calibration circuits in these systems. Current-steering thermometer digital-to-analog converters (DACs) are used as calibration tools in many such high speed I/O systems. As we move towards lower technology nodes, the overall DAC area is decreasing. But this degrades matching and therefore affects the DACs' accuracy. In this work, we propose a dual-calibration technique to improve the matching accuracy and the static linearity of a current-steering thermometer DAC. The novelty of the proposed scheme lies in obtaining the best samples from the error distribution using redundancy for improved matching followed by adaptively reordering these samples to reduce error accumulation. We consider the statistical basis for each of these methods and demonstrate new tools to enable statistical modeling of the proposed technique. Using these tools we demonstrate 36% and 51% reduction in differential non-linearity (DNL) and integral non-linearity (INL), respectively for an 8-bit current-steering thermometer DAC with two redundant cells per row. This matches well with the Monte Carlo simulations' result - 38% for DNL and 55% for INL. To complete the validation cycle, we fabricated an 8-bit current-steering thermometer DAC with two redundant cells per row in TSMC 65nm CMOS process. We show an improvement of 36% in DNL and 50% in INL from measurement of 16 chips. In I/O systems,

it is important to consider the calibration technique's algorithmic complexity too. By normalizing the INL and DNL improvements with complexity, our technique results in better performance compared to other similar existing techniques. We also demonstrate the area benefit of our technique over the baseline case with no calibration and predict that this improvement will only get better as CMOS process technology scales down. Lastly, we show the advantage of using the dual-calibrated DAC in the phase interpolator (PI) of a high speed I/O link model over the use of a baseline DAC in the presence of random variation.

BIOGRAPHICAL SKETCH

Ishita Mukhopadhyay was born in New Delhi, India in October 1986. She grew up in New Delhi from where she graduated her high school in 2004. She received her Bachelor in Technology and Master in Technology in electrical engineering from Indian Institute of Technology (IIT), Delhi, India in 2008 and 2009, respectively.

In 2009, Ishita moved to Ithaca, NY in the position of a Graduate Research Assistant in Dr. Apsel's lab at Cornell University. She started working in improving accuracy of various analog and mixed signal circuit blocks in the presence of process, voltage and temperature variation. For her thesis, she has worked on developing variation tolerant calibration circuits for high performance I/O, focusing specifically on improving linearity of current-steering thermometer digital-to-analog converters.

During the summer and fall of 2011, she was an intern with Intel Corporation, Santa Clara, CA working on evaluating high volume manufacturing test quality of design-for-test circuits in I/O in presence of significant process variation. She was a recipient of the Intel PhD Fellowship in 2012.

To

Maa and Baba and Mihir

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CHAPTER 1

INTRODUCTION

1.1 Digital-to-Analog Converters (DACs)

The integration of digital and analog subsystems on one chip is increasing with the scaling of CMOS processes. Hence, the circuits providing the interface between these subsystems are one of the important blocks for the whole system. To convert a digital data, like a stream of binary bits, into an analog signal, like a current or a voltage, a digital-to-analog converter (DAC) is used. DACs can be broadly categorized as thermometer or binary [1], which is based on the way the digital inputs are decoded inside the DAC. An N-bit thermometer DAC has 2^N-1 unit cells as shown in Figure 1.1.

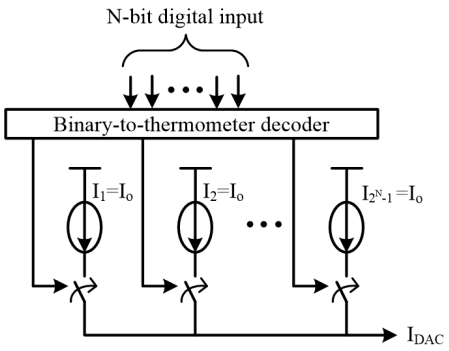


Figure 1. 1. Current-steering thermometer DAC

Each unit cell is addressed separately. For this, the input digital code is first converted into a thermometer code. This thermometer code is used to control the switches inside each unit cell to turn it on or off. Since only one unit cell is switched on for 1 LSB (least significant bit) increase

in the input digital code, thermometer DACs are guaranteed to have monotonic behavior. But with increasing resolution, the area of this type of DAC increases as powers of 2.

In a binary DAC, as shown in Figure 1.2, the input digital code directly controls the switches inside each cell of the DAC.

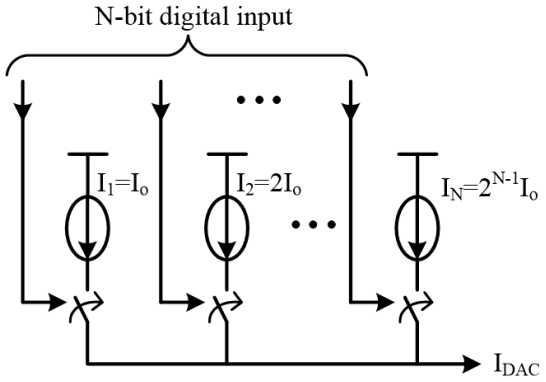


Figure 1. 1. Current-steering binary DAC

Each DAC cell is binary weighted, i.e., the output of each successive cell is twice that of the next closest least significant bit. Compared to thermometer DACs, binary DACs require less area. But large switching errors and linearity issues are associated with these. For example, at the half-scale transition for an N-bit binary DAC, the cell controlled by the MSB (most significant bit) is switched on and all other cells are turned off which may result in a large glitch at the output.

The segmented DAC design utilizes the benefits of both the types of the DACs - unary for its monotonic and better linearity and binary for lower area. The MSBs control the unary part of the segmented DAC while the binary part is controlled by the LSBs. The division of the input digital bits into MSBs and LSBs depends on the required accuracy versus the area and power constraints.

In many applications, DACs are often used as calibration tools. In such scenarios, current-steering thermometer coded DACs are mostly used because of their speed and also because they offer the best calibration accuracy by avoiding glitches caused by majority carry operations in binary coded DACs. Since for such purposes DACs provide accurate biasing current, it is the static linearity of these DAC which is of major concern.

1.2 Precision versus mismatch

Even though thermometer coded DACs usually demonstrate monotonic behavior and good linearity, the matching accuracy between its unit cells ultimately dictate the overall linearity of the DAC. In this section we first discuss the different types of variation in present day CMOS processes followed by what impact they have on the matching accuracy of the unit cells of thermometer DACs. We conclude this section by discussing the various existing techniques to improve this matching between the unit cells in the presence of device mismatch and variation.

1.2.1 Mismatch and variation in CMOS processes

Gordon Moore proposed the Moore's law in 1965 which basically states that the number of transistors placed in a particular amount of area in an integrated circuit (IC) will double every 18 months [2]. With continual shrinking of transistor sizes, the CMOS industry continues to follow Moore's law. Although this scaling down of CMOS is economically advantageous, the devices are more vulnerable to process variation and device mismatches. Though variations like these existed throughout the history of CMOS technology, as devices scale down these variations are

becoming a larger percentage of the critical dimensions. This ultimately degrades the overall performance of circuits; especially analog blocks which are severely affected by device mismatches [3].

Process variations can be broadly categorized as inter-die or intra-die variations.

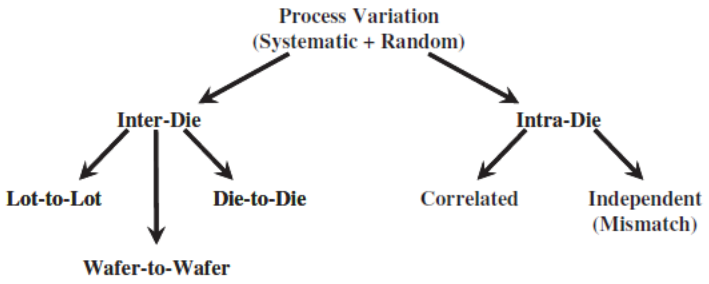
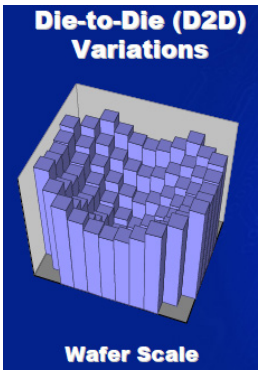
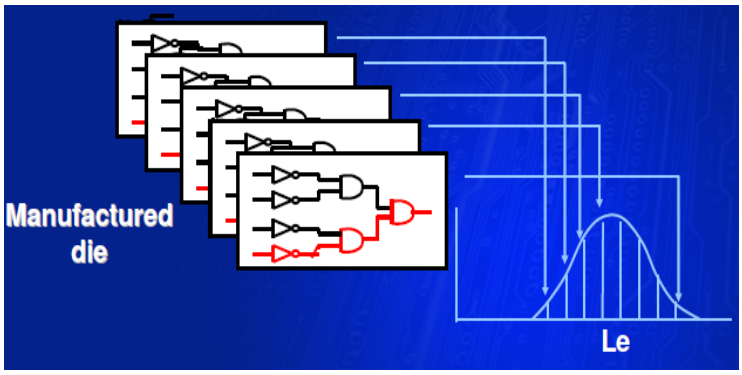


Figure 1. 2. Division of process variation according to geometric scale [4]

Inter-die consists of lot-to-lot, wafer-to-wafer and die-to-die variations whereas intra-die consists of random independent mismatches and correlated systematic variations.



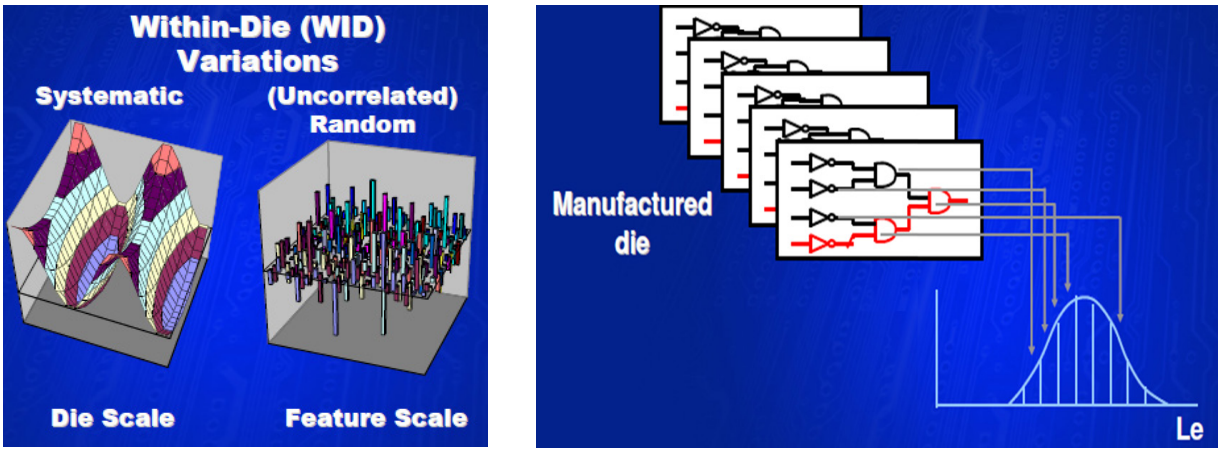


(a) Wafer scale variation depiction (b) Difference in circuit performance

Figure 1. 3. Inter-die variations [5]

As seen from Figure 1.4, due to inter-die variations, the same device placed in the same location in a chip, has different electrical characteristics for different wafers and for different dies from a single wafer. These variations are caused by manufacturing equipment properties, process

temperature, wafer polishing and placement. They affect every element in the circuit equally and thus increasing circuit variability [6]. In contrast, intra-die variations affect different elements in a circuit differently as shown in Figure 1.5. This increases mismatch between circuit elements leading to possible reduction in functional yield [6].



(a) Spatial representation (b) Difference in device performance

Figure 1. 4. Intra-die variations [5]

At the die scale, systematic variations occur which are deterministic and can be predicted and modeled. For example, fluctuations of the focus and exposure of lithography system for various layout patterns lead to systematic variations [4]. This type of variation has spatial correlation and we can use distance dependent models to characterize it. In cases where process simulations do result in accurate depiction of these errors, test structures can be used on chip for characterization [7]. At the feature scale though, process conditions vary randomly from one location to another within a die which results in random variations or device mismatch. For example, the number of discrete dopant atoms in any area can be treated as a Poisson process dependent on area [8] which causes independent and random variations in transistors properties, even when drawn

identically and placed in closed proximity. Figure 1.6 shows how this random dopant fluctuation (RDF) affects the electrical potential.

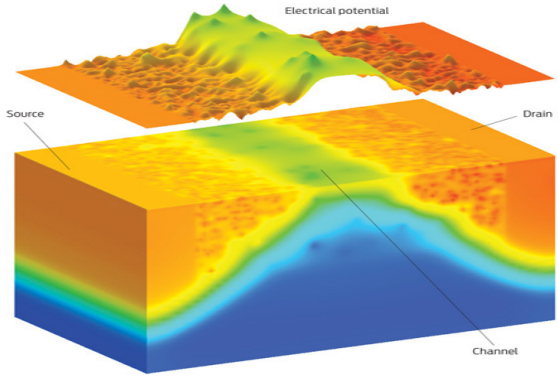


Figure 1. 5. Cross-section of transistor with RDF [9]

This RDF leads to variation in one of the critical parameters of the transistor – threshold voltage (V_{th}). With decreasing feature sizes, the impact is increasing as shown in Figure 1.7.

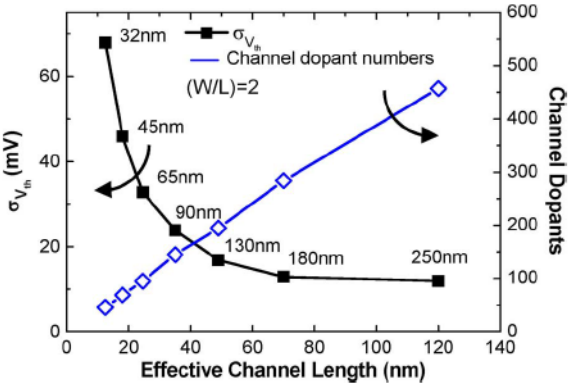


Figure 1. 6. Threshold voltage variation due to RDF [10]

Line edge roughness (LER) is another phenomenon responsible for fluctuations in V_{th}. LER basically distorts the shape of the gate along the channel width as shown in Figure 1.8.

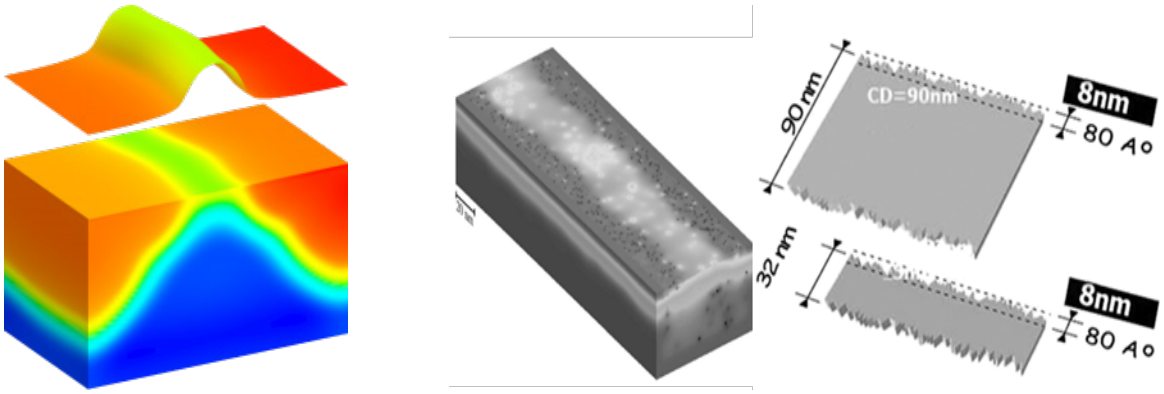


Figure 1. 7. Impact of line edge roughness in smaller feature sizes

The variance of LER doesn't scale with technology [11] and hence for smaller feature sizes it raises a growing concern. Figure 1.9 shows the impact of LER on the variance of V_{th}. As expected, with increasing fluctuations, the variance of V_{th} increases.

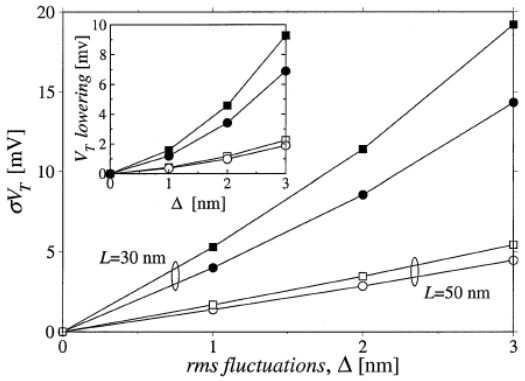


Figure 1. 8. LER's impact on variance of V_{th} [11]

The combined effect of RDF and LER on the threshold voltage is given by

$$\sigma_{Vth}^2 = \sigma_{Vth,RDF}^2 + \sigma_{Vth,LER}^2 \tag{1.1}$$

Figure 1.10 shows variation in threshold voltage due to both RDF and LER.

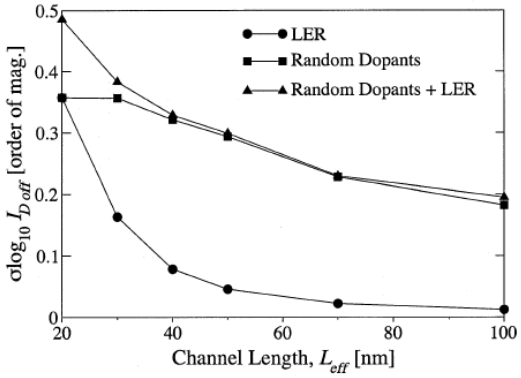


Figure 1. 9. Variation in V_{th} due to RDF and LER [11]

Along with RDF and LER, there are other sources of random variations like granularity of the poly-silicon gate, oxide thickness variations and metal gate granularity. So one can see that as we move to smaller feature sizes all these variations majorly impact the transistor performance.

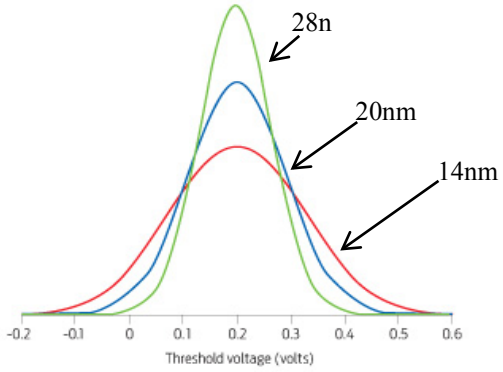


Figure 1. 10. Widening variability in V_{th} [9]

With scaling down of CMOS processes, the size of transistors is decrease resulting in reduction of the area of the DAC unit cell and the overall DAC area. But unfortunately, matching of the unit cells does not scale with process. For a given process and technology the mismatch amongst the unit cells is inversely proportional to the area [8]. Hence, even though the minimum feature size is decreasing, we cannot take the advantage of this area reduction fully due to the decrease in accuracy of the unit cells which ultimately increases the non-linearity of DACs.

1.2.2 Existing techniques to improve accuracy of thermometer DACs

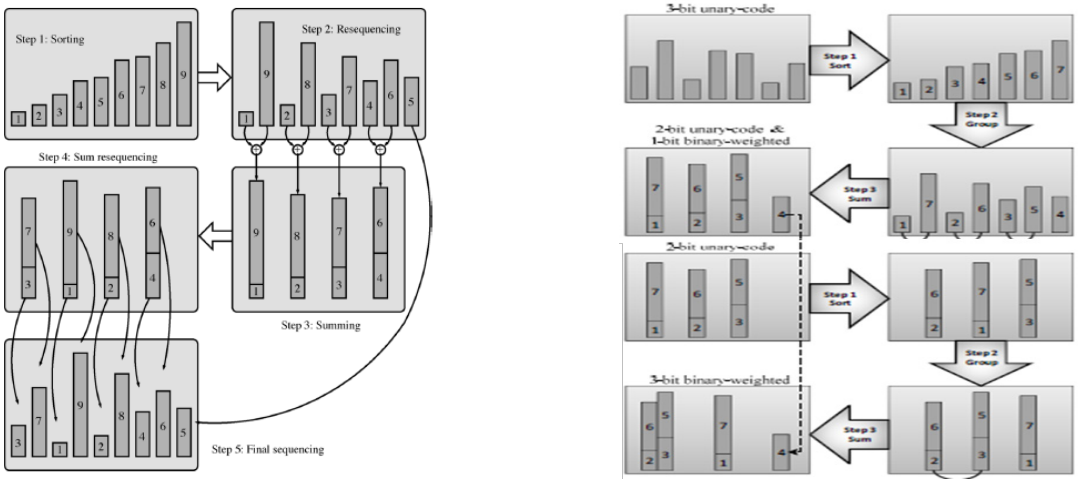
The previous sub-section discussed the various variations that are present in CMOS processes and how they impact the transistor's performance. We also know that the overall linearity of the thermometer DAC depends on the matching between its unit cells ([1], [12]) and this mismatch increases with decrease in area of the cells. This implies that unit cells of the DAC need to be made larger to overcome the detrimental effect of increased non-linearity and to maintain yield. Various pre-processing techniques such as special layout implementations [13], [14], and biasing and routing schemes [15] have been used to compensate for this loss in accuracy without growing the unit cells. These approaches are good for removing systematic geometric errors. But as feature size becomes smaller with each transistor having lower atoms in its gate channel, random device mismatches are becoming the more dominant type of variation in 65nm technologies and beyond [4]. Since it's very difficult to contain random mismatches by using only pre-fabrication techniques like circuit layout, pre-processing techniques are not able to eliminate random mismatch errors as these methods lack the capability to improve matching accuracy post-fabrication. Hence, calibration becomes essential.

Using calibration to improve matching between the DAC unit cells consists of mainly two schools of thought. First method of calibration basically involves correcting the output of each unit cell such that it is equal to a particular reference of choice. In [16] a calibration DAC (CALDAC) is used inside each MSB controlled current cell to calibrate the output current. Similarly in [17], each MSB current source is compared to an external reference current and subsequently corrected for. A self-trimming scheme is shown in [18] where a common 12-bit CALDAC is used to trim each MSB current source. The work in [19] too discusses an on-chip

self-calibration scheme which uses a 1-bit analog-to-digital converter (ADC), an 8 stage finite state machine (FSM) and small CALDAC within each current source of the DAC. In [20], extra transistors are used in each current source of the DAC which are reconfigurable to provide a correcting current to the output of the unit cell. Though all these techniques using some form of calibration current to correct for the mismatch error in the unit cells improve the matching and hence the static linearity of the DAC, these techniques consume a large amount of area (which may not scale well with technology) and hence, lead to increased power consumption as well as complexity.

The second manner of improving matching involves adjusting the switching sequence of the unit cells such that mismatch error cancellation is achieved with successive cell addressing. Techniques like dynamic element matching (DEM) ([21] – [23]) and dynamic mismatch mapping (DMM) [24] are targeted specifically to reduce dynamic linearity. Hence, they do not reduce the overall power of the mismatch error which is important for improving the static linearity. Also, DEM is known to increase the noise floor [25] and it extensively relies on pseudo-random sequence generators with a guarantee of improved linearity only with sufficient averaging. A novel switching-sequence post-adjustment (SSPA) technique is developed in [26] where the currents from all the unit cells are first sorted in ascending order. Then the current cell with maximum deviation from the average current is grouped with the current cell with minimum deviation followed by the pairing of the second maximum current cell with the second minimum current cell and so on. Then these pairs are again sorted in ascending order followed by ungrouping of the pairs resulting in the final sequence of addressing (Figure 1.12(a)). The complete-folding technique in [27] extends this SSPA method. Instead of re-sequencing just once like in the SSPA scheme, in the complete-folding method the re-sequencing is continued

without any ungrouping till the number of elements in the final sequence is equal to the number of input bits. In other words, it converts a thermometer DAC into a binary DAC with the knowledge of the mismatch errors (Figure 1.12(b)).



(a) SSPA [26] (b) Complete folding [27]

Figure 1. 11. Switching schemes

The addressing scheme in [28] works along the same line as the SSPA and the complete-folding but instead of using the mismatch errors in the unit cells to optimize the switching, the differential non-linearity (DNL) at each code is used to obtain the required optimal addressing of elements. The scheme in [29] achieves good integral non-linearity (INL) improvement as it first turns the cell with maximum deviation from the average currents followed by several cells having opposite deviation to nearly cancel the error accumulation.

Most of these techniques utilizing various switching sequence optimization focus on reducing the error accumulation at the output without changing the magnitude of the individual errors. Also all these techniques look at all the DAC cells to derive their optimized switching sequence. This

in turn leads to significant increase in the algorithmic complexity of the addressing scheme and hence more time and higher power consumption for calibration is required.

1.3 Thesis organization

With the increasing use of current-steering thermometer DACs for the purpose of providing accurate biasing or as a calibration tool in various places such as in high speed I/O systems [30] and wireless [31] applications, it is necessary to improve the static linearity of these DACs in the presence of variations, especially random variations. Due to the nature of application of these DACs, they cannot consume large amount of area and power. Hence, it is also crucial for the calibration technique developed for improving the static linearity of these DACs to be implemented on-chip without much overhead in area, power and complexity.

In this work we propose a dual-calibration technique to improve static linearity in thermometer DACs. The dual-calibration technique utilizes the two-dimensional nature of the thermometer DAC to reduce its algorithmic complexity. The first calibration technique targets the underlying reason for non-linearity by reducing mismatch between the unit cells using *redundancy*. The technique introduces redundant cells followed by eliminating outliers which are farthest from the mean. The second technique relies on *reordering* of the cells' addresses based on their relative values to minimize accumulation of errors, and is similar to switching sequence optimization schemes. Targeting specifically static non-linearity, we first provide a mathematical basis to analyze the effects of both the techniques of the proposed dual-calibration in chapter 2. In chapter 3, we present the design challenges imposed by the dual-calibration scheme followed by discussion of the on-chip implementation of the proposed technique along with the required

calibration circuits. We also discuss the measurement results, which indicate agreement with the proposed models through a consistent improvement in static non-linearity over a baseline case. We conclude the chapter with a comparison of the proposed technique with the existing calibration methods along with the area implications. In chapter 4 we first give a general overview of I/O links followed by a discussion on the usage of DACs as calibration tools in I/O. We also discuss the impact of using our proposed dual-calibrated DAC on the overall performance of I/O through our I/O link model developed in MATLAB. Lastly, in chapter 5 we summarize our work followed by a brief discussion on a modular addressing scheme to extend the redundancy method of our dual-calibration technique without involving significant redesign and we also propose some future research directions.

CHAPTER 2

A DUAL-CALIBRATION TECHNIQUE FOR THERMOMETER DACS

2.1 Introduction to chapter

Current-steering thermometer DACs are used in various applications as calibration tools. Even in the presence of process variation and random device mismatches, they need to provide accurate biases. But the matching of the unit cells of the DAC degrades due mismatch errors. Hence, in this work we propose a new dual-calibration technique to improve the static linearity of these current-steering thermometer DACs in the presence of random mismatch errors. In this chapter we develop the mathematical background of the proposed calibration technique. First we present a general overview of how mismatch errors affect the static linearity of thermometer DACs. Following that, we introduce the two schemes of the dual-calibration technique and mathematically analyze both the schemes individually to derive the relation between the variance of the non-linearity of the DAC and the variance of the mismatch errors. We conclude this chapter by formulating the dual-calibration technique and validating the predictions of improved matching given by the theory with Monte Carlo simulation results of the proposed technique.

2.2 Static non-linearity in thermometer DACs

An N-bit current steering DAC consists of $2^N - 1\ (= n)$ identical unit current cells in a 2-dimensional (2D) matrix form as shown in Figure 2.1.

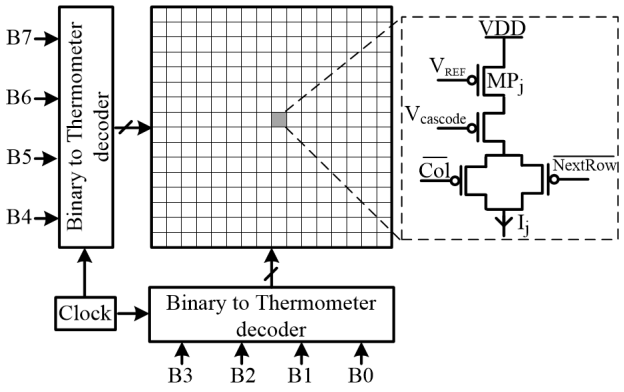


Figure 2. 1. 2-dimensional (2D) thermometer DAC architecture

Since the random variations of current sources are determined by the inherent properties of the technology used they can be assumed to be independent from each other and follow normal distribution [32]. The current contribution of the j^{th} unit cell is given by

$$I_j = I_0 \cdot (1 + \varepsilon_j) \tag{2.1}$$

Here, the nominal current the unit cells are designed for is I_0 and $\varepsilon_j \sim N(0, \sigma_\varepsilon^2)$ is the random independent mismatch error in the unit current cells due to variations in the main current transistor MP_j which can be biased from a bandgap reference. For an input code k $(0 < k \leq n)$, where $n = 2^N - 1$, we express the DAC output current as

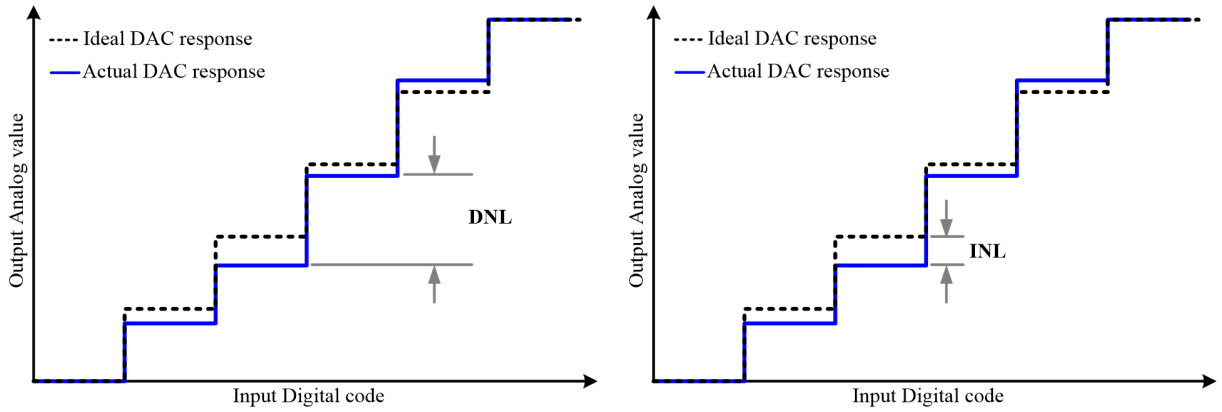
$$I(k) = \sum_{j=1}^{k} I_j = I_o\left(k + \sum_{j=1}^{k} \varepsilon_j\right) \tag{2.2}$$

The mean or the LSB current, is given as

$$I_{LSB} = (1/n) \sum_{j=1}^{n} I_j = I_o\left(1 + (1/n) \sum_{j=1}^{n} \varepsilon_j\right) \tag{2.3}$$

From (2.3) it's clear that if there are no mismatch errors amongst the unit cells, the mean current (I_{LSB}) will be equal to the nominal current (I_o). Mismatches in these unit cells lead to two types

of errors – differential non-linearity (DNL) and integral non-linearity (INL) as shown in Figure 2.2.



(a) Differential non-linearity (DNL) (b) Integral non-linearity (INL)

Figure 2. 2. Two types non-linearity associated with thermometer DAC

DNL is the deviation of the difference between two successive DAC output currents normalized by the LSB current from the ideal step size of 1. INL is defined as the deviation of the analog output from ideal DAC output in the absence of mismatch errors, normalized by the LSB current. It is the accumulation of errors or, the summation of DNL at each code. The DNL and INL after offset and gain correction, in terms of Least Significant Bit (LSB), for an input code k are given [32], [33] by

$$DNL(k) = \big(\big(I(k) - I(k-1)\big)/I_{LSB}\big) - 1 \tag{2.4}$$

$$INL(k) = (I(k) - k.I_{LSB})/I_{LSB} \tag{2.5}$$

respectively. By substituting (2.2) and (2.3) in both (2.4) and (2.5), we get,

$$DNL(k) = \big(\varepsilon_k - (1/n)\sum_{j=1}^{n}\varepsilon_j\big)/\big(1 + (1/n)\sum_{j=1}^{n}\varepsilon_j\big) \tag{2.6}$$

$$INL(k) = \left(\sum_{j=1}^{k} \varepsilon_j - (k/n) \sum_{j=1}^{n} \varepsilon_j\right) / \left(1 + (1/n) \sum_{j=1}^{n} \varepsilon_j\right) \quad (2.7)$$

respectively. For large n, we re-write (2.6) and (2.7) as

$$DNL(k) = \left(1 - (1/n)\right)\varepsilon_k - (1/n) \sum_{j=1, j\neq k}^{n} \varepsilon_j \quad (2.8)$$

$$INL(k) = \sum_{j=1}^{k} \varepsilon_j - (k/n) \sum_{j=1}^{n} \varepsilon_j \quad (2.9)$$

respectively. The overall DNL and INL of the DAC is the maximum of the absolute value of (2.8) and (2.9), respectively.

From (2.8), we observe that overall DNL of the DAC, DNL_{DAC} depends on the worst absolute mismatch error amongst the unit cells. Also, upon taking variance on both sides of (2.8) and (2.9), we derive the variance of the DNL and INL, which determine the yield, as

$$\sigma^2_{DNL(k)} = \sigma^2_{DNL} = ((n-1)/n)\sigma^2_{\varepsilon} \quad (2.10)$$

$$\sigma^2_{INL(k)} = (k \cdot (n-k)/n)\sigma^2_{\varepsilon} \quad (2.11)$$

respectively. Therefore, both the DNL and the INL have normal distribution centered at zero with variance as given in (2.10) and (2.11) respectively.

From (2.10) and (2.11) we see that the variance of both the DNL and the INL is proportional to the variance of unit cells, σ^2_{ε}. Therefore, to improve the linearity of the DAC, we need to reduce σ_{ε}, which we achieve by *redundancy* – the first method of our dual-calibration technique. We can also see from (2.11) that the variance of the INL, unlike that of the DNL in (2.10), does

depend on the input code k. Hence, we accomplish further reduction of the variance of the INL by *reordering* the addressing of the unit cells. The following sections in this chapter discuss the theoretical basis of these two techniques in detail followed by the mathematical analysis of our proposed dual-calibration technique.

2.3 Redundancy

Let us assume the simple case of considering the DAC as a collection of normally distributed elements, such as the current sources. Now if we introduce n_{red} redundant elements in the n existing elements and then remove the outliers in this sampled set based on their deviation from the mean current source, we will be left with a normal distribution with its tails cut off as shown in Figure 2.3.

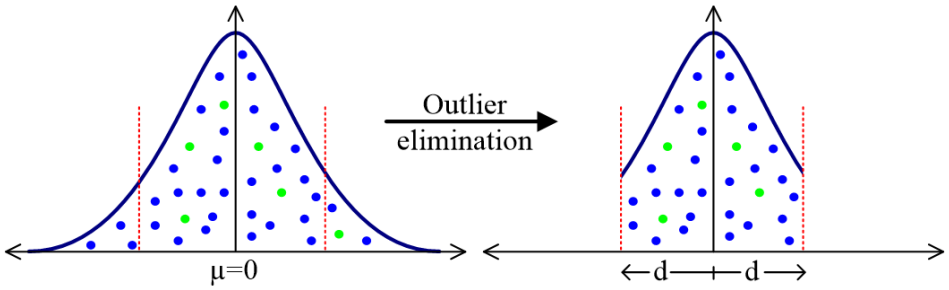


Figure 2. 3. Pictorial representation of the redundancy scheme showing introduction of redundant samples (green) followed by outlier elimination near the tail of the distribution

This resulting distribution resembles a truncated Gaussian distribution with hard finite cutoffs, determined by the degree of redundancy. If we consider the cutoffs at a distance d, symmetrical with respect to the mean (Figure 2.3), the relation between the amount of redundancy, r and the cutoffs is then given by

$$d/\sigma_\varepsilon = \Phi^{-1}\big(1-(r/2)\big) \tag{2.12}$$

Here, $r = n_{red}/(n_{red}+n)$ and $\Phi^{-1}(x)$ is the inverse standard normal cumulative distribution function. Using the properties of $\Phi^{-1}(x)$ we observe that d decreases as r increases. Hence the resulting error's standard deviation decreases and therefore, variance of DNL decreases as dictated by (2.10).

In general, the variance of the truncated Gaussian distribution of the mismatch error after outlier elimination is given [34] by

$$Var(\varepsilon|\varepsilon_{min}<\varepsilon<\varepsilon_{max}) = {\sigma_\varepsilon}^2\left[1+\frac{\alpha\phi(\alpha)-\beta\phi(\beta)}{\Phi(\beta)-\Phi(\alpha)}-\left(\frac{\phi(\alpha)-\phi(\beta)}{\Phi(\beta)-\Phi(\alpha)}\right)^2\right] = \sigma_{\varepsilon_{red}}^2 \tag{2.13}$$

Here, $\alpha = \varepsilon_{min}/\sigma_\varepsilon$, $\beta = \varepsilon_{max}/\sigma_\varepsilon$, $\phi(x)$ is the probability distribution of the standard normal distribution and $\Phi(x)$ is its cumulative distribution function. To prove that $\sigma_{\varepsilon_{red}}^2 < \sigma_\varepsilon^2$, let's first consider the following term

$$1+\frac{\alpha\phi(\alpha)-\beta\phi(\beta)}{\Phi(\beta)-\Phi(\alpha)}-\left(\frac{\phi(\alpha)-\phi(\beta)}{\Phi(\beta)-\Phi(\alpha)}\right)^2 \tag{2.14}$$

Since it's a two sided truncation of a zero mean Gaussian, $\alpha<0<\beta$, and therefore, $\Phi(\beta)>\Phi(\alpha)$. So the denominator is positive for both the second and third terms in (2.14). As $\phi(\alpha)>0$ and $\phi(\beta)>0$, the second term of (2.14) is always negative whereas, the third is always positive, because it's a square term. Hence, the result of (2.14) is always less than 1. Therefore,

$${\sigma_\varepsilon}^2 > \sigma_{\varepsilon_{red}}^2 \tag{2.15}$$

This reduction in variance due to introduction of outliers allows for the overall magnitude of mismatch errors, $|\varepsilon|$ to reduce as well. Figure 2.4 depicts the reduction in variance for an 8-bit

thermometer current steering DAC after removal outliers, i.e., outlier-free DAC, through 5000 Monte Carlo simulations. In the baseline DAC case, where no redundant unit cells have been added, all the current sources contribute to the DNL and INL. The colored pane shows the simulation results of the implementation of the redundancy technique and how $\sigma^2_{\varepsilon_{red}}$ reduces as we increase n_{red}. From Figure 2.4 we observe that the truncated Gaussian model (the black mesh) fits well with the simulation results. We also see that a sharp decline in $\sigma^2_{\varepsilon_{red}}$ is obtained with only few number of redundant unit cells, which suggests we have more reduction in mismatch error than area penalty by implementing the redundancy technique.

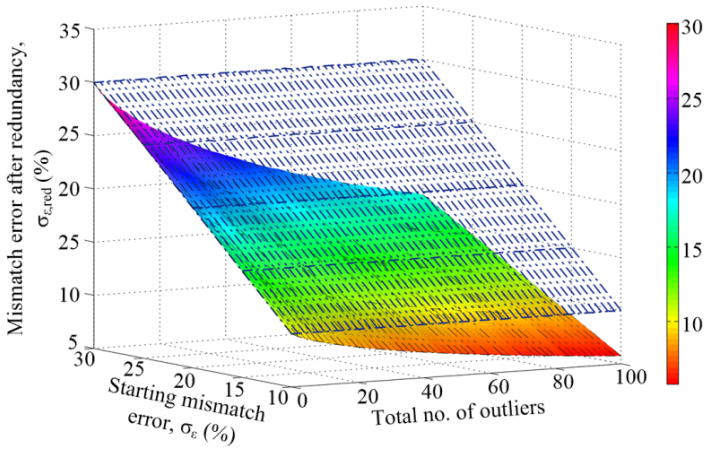


Figure 2. 4. Reduction of variance of mismatch error due to redundancy technique; baseline DAC (top blue mesh), truncated Gaussian model (black mesh), simulated outlier-free DAC(colored plane)

The effect of improving matching by redundancy on the worst DNL is shown Figure 2.5. As expected from (2.8), with improved matching and reduced $|\varepsilon|$, the values of $\mathrm{DNL}_{\mathrm{DAC}}$ decrease. Figure 2.6 shows the variance of the DNL. As predicted by (2.10), with reduction in the variance of the mismatch errors, the variance of the DNL decrease.

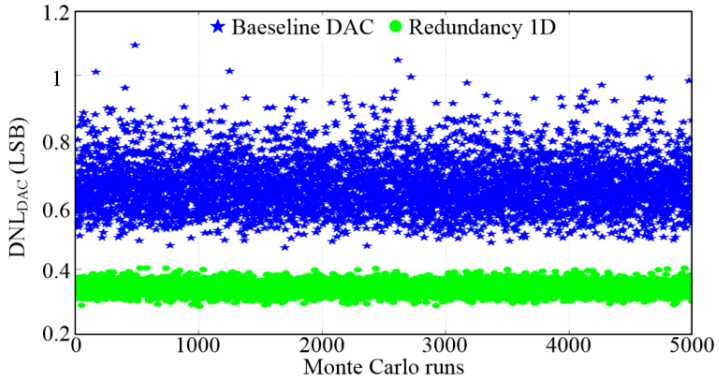


Figure 2. 5. Monte Carlo simulations of the worst case DNL amongst all codes for 8-bit thermometer DAC with 20% starting mismatch between unit cell and 32 outliers

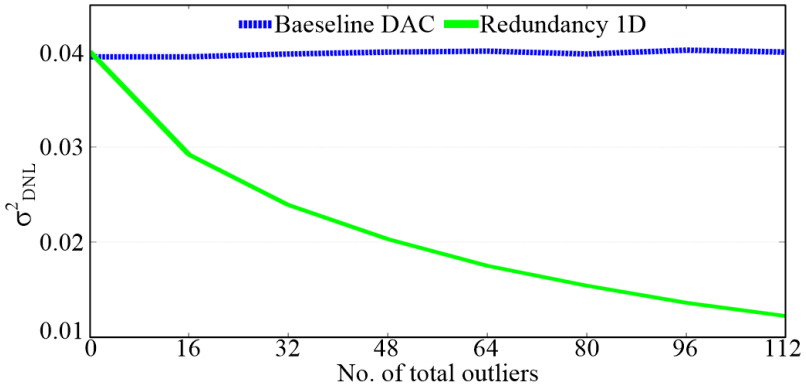


Figure 2. 6. Variance of DNL for 8-bit thermometer DAC with 20% starting mismatch between unit cells

The 1-dimensional (1D) case discussed till now is not realistic in circuit terms. In order to minimize addressing, switching and routing complexity, thermometer DACs are implemented as 2-dimensional (2D) arrays (Figure 2.1) with n unit cells accessed sequentially in a raster scan. Hence, we modify the redundancy technique for easy decoding of the digital input. There are n_{rows} in the DAC and we introduce $n_{red,2D}$ redundant elements in each row. So each row has $n_{cols} + n_{red,2D}$ elements. Owing to this small sample size, a sample of independent normally distributed outputs from the DAC unit cells in a row cannot be approximated as a truncated

normal distribution [35]. As the mismatch errors are sampled from a normal distribution, we approximate the sampled units of each row from a Student's t-distribution with $(n_{cols} - 1)$ degrees of freedom. The sampled variance of each row is given as

$$S_i^2 = \left(\sum_{j=1}^{n_{cols}} (\varepsilon_{i,j} - \overline{\varepsilon_i})^2\right)/(n_{cols} - 1) \tag{2.16}$$

Since each S_i^2 has been generated from Student's t-distribution's sampled values, the set of S_i^2 of the n_{rows} rows are chi-squared random variables [ref]. We can now estimate the true unknown variance of the outlier-free DAC using an unbiased estimator using S_i^2. In other words, $E[S_i^2] = \sigma_{\varepsilon_{red,2D}}^2$, the variance of a 2D outlier-free DAC. We get the 95% confidence interval based on a Student's t-distribution with $(n_{cols} - 1)$ degrees of freedom as

$$\overline{S^2} - t_{\frac{\alpha}{2},n_{cols}-1}\sqrt{\frac{\sigma^2(S^2)}{n_{cols}}} \leq \sigma_{\varepsilon_{red,2D}}^2 \leq \overline{S^2} + t_{\frac{\alpha}{2},n_{cols}-1}\sqrt{\frac{\sigma^2(S^2)}{n_{cols}}} \tag{2.17}$$

In (2.17), $\overline{S^2}$ is the mean of the sampled variances, $\sigma^2(S^2)$ is the variance of the sampled variances of each row, $\alpha = 0.05$ and thus, we are estimating 95% confidence in the accuracy of our model.

The errors bars in Figure 2.7 show the upper and lower bounds of our estimation for $\sigma_{\varepsilon_{red,2D}}^2$ against the empirical results for the 2D DAC various values of $n_{red,2D}$ with $\alpha = 0.05$. We observe that for each case our model predicts $\sigma_{\varepsilon_{red,2D}}^2$ within 1% error. As expected, 1D DAC has lower variance values than the 2D square DAC since removing $n_{red,2D} \times n_{rows}$ outliers over the entire design space, results in tighter error distribution around the mean.

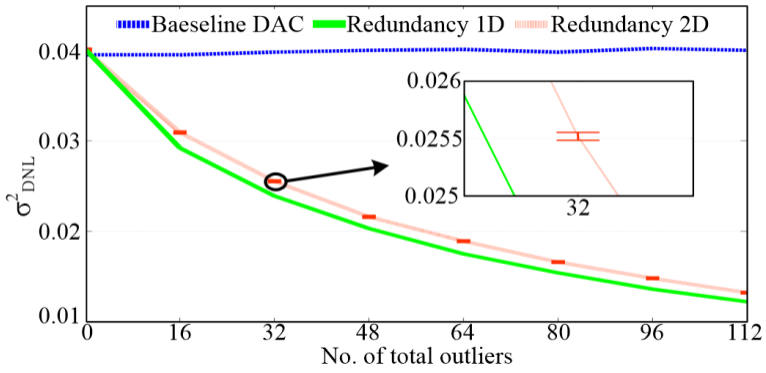


Figure 2. 7. Theoretical variance of DNL for different number of outliers, where redundancy 1D shows truncated Gaussian model and error bars represent accuracy of the model used for the 2D DAC

With a starting current source mismatch of 20% for an 8-bit DAC, Monte Carlo runs for both the 1D and 2D DAC in Figure 2.8 show significant DNL_{DAC} reduction, agreeing with our models. The total number of outliers was kept same for both the cases, i.e., two redundant unit cells per row for 2D DAC and total of 32 redundant cells for the 1D DAC.

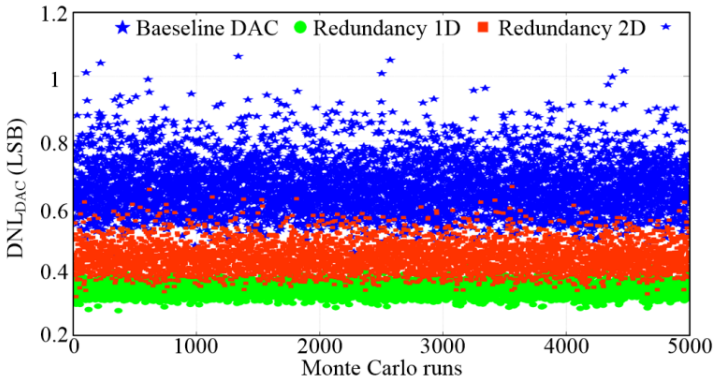


Figure 2. 8. Monte Carlo simulations of the worst case DNL amongst all codes for 8-bit thermometer DAC with 20% starting mismatch between unit cells and 2 outliers per row

We also observe from (2.11) that our redundancy technique helps in reducing $\sigma^2_{INL(k)}$ as well, by reducing the variance of the mismatch error.

2.4 Reordering

The overall INL of the DAC, INL_{DAC} occurs when maximum error accumulation takes place, which corresponds to the first term in (2.9). As designers, we have control over the switching scheme. By obtaining a-priori knowledge of the relative values of the cells, we can modify the switching scheme with an efficient, low hardware overhead technique to alternate between minimum and maximum elements or vice versa. This allows us to negate the deviation from the ideal behavior due to previous current sources with the present current source as shown in Figure 2.9.

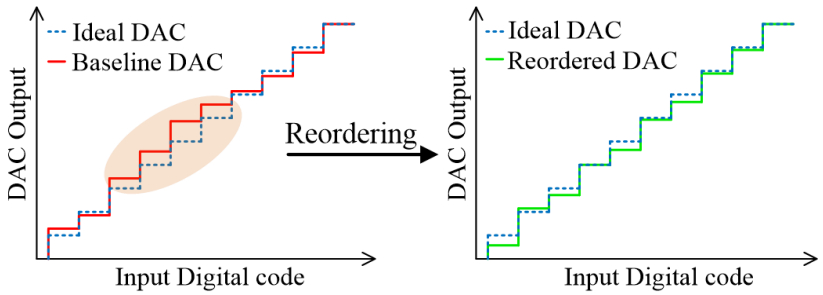


Figure 2. 9. Graphical representation of reordering scheme showing significant reduction in error accumulation (shaded area in left)

First we consider all n unit cells together (1D DAC case) instead of the 2D case. When we arrange the independent random mismatch errors ε_j in increasing order of their values for the modified switching algorithm, the resulting ordered errors are no longer independent. To derive the INL equation using these ordered elements, we need to look at order statistics [36] of these error elements. The order statistics of a random sample, like the mismatch errors of the DAC unit cells, are the sample values in ascending order and are denoted by $\varepsilon_{(1)}, \varepsilon_{(2)}, \cdots, \varepsilon_{(n)}$, where $\varepsilon_{(i)}$ is

the i[th] smallest mismatch error. Hence, the reordering scheme of minimum-maximum pairing changes the switching order of the cells to $\{\varepsilon_{(1)}, \varepsilon_{(n)}, \varepsilon_{(2)}, \varepsilon_{(n-1)}, \cdots\}$. Using this modified switching in (2.9) and that $\sum_{i=1}^{n} \varepsilon_{(i)} = \sum_{j=1}^{n} \varepsilon_j$, we can rewrite the expression for INL(k) after reordering as

$$INL_{reorder}(k) = \sum_{i=1}^{\lfloor k/2 \rfloor} \left(\varepsilon_{(i)} + \varepsilon_{(n-i+1)}\right) + (k \bmod 2) \cdot \varepsilon_{(\lceil k/2 \rceil)} - (k/n) \sum_{j=1}^{n} \varepsilon_j \qquad (2.18)$$

The first term of (2.18) has a value close to zero since successive elements of the reordered set cancel each other. The second term of (2.18) adds a single, decreasing error for every odd code k only. Since the first term of (2.9) is always a cumulative sum of errors and there is no guarantee on what trends successive element errors will follow, we conclude that the sum generated in (2.18) will always be less than (2.9), confirming that INL_{DAC} is reduced with reordering. Figure 2.10 shows the reduction in INL_{DAC} through Monte Carlo simulations.

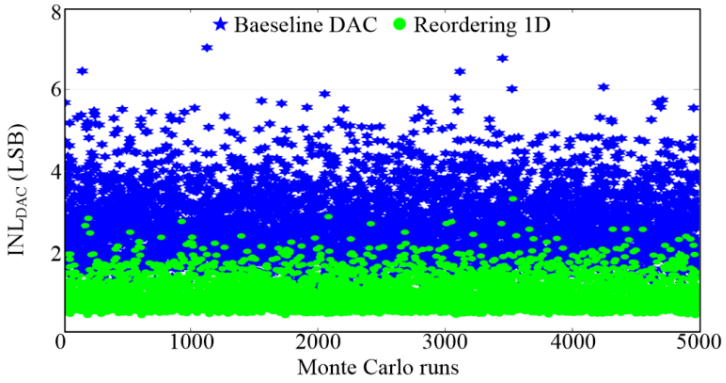


Figure 2. 10. With 20% current source mismatch error, 8-bit thermometer DAC's worst case INL amongst all codes for 5000 Monte Carlo runs

Assuming $\sum_{j=1}^{n} \varepsilon_j = \varepsilon_{sum}$ and $E[\varepsilon_{sum}] = 0$, the variance of INL after reordering is given by

$$\sigma^2_{INL_{reorder}(k)} =$$

$$(k/n)^2\sigma^2_{\varepsilon_{sum}} + \sum_{i=1}^{\lfloor k/2 \rfloor}\left(\sigma^2_{\varepsilon_{(i)}} + \sigma^2_{\varepsilon_{(n-i+1)}}\right) - 2(k/n)\sum_{i=1}^{\lfloor k/2 \rfloor}\left(E\left[\varepsilon_{(i)}\varepsilon_{sum}\right] + E\left[\varepsilon_{(n-i+1)}\varepsilon_{sum}\right]\right) + 2\sum_{i=1}^{\lfloor k/2 \rfloor}\sum_{j=1}^{\lfloor k/2 \rfloor}\sigma\left(\varepsilon_{(i)}, \varepsilon_{(n-j+1)}\right) + 2\sum_{i<j}^{\lfloor k/2 \rfloor}\left(\sigma\left(\varepsilon_{(i)}, \varepsilon_{(j)}\right) + \sigma\left(\varepsilon_{(n-i+1)}, \varepsilon_{(n-j+1)}\right)\right) + (k \bmod 2)\cdot\left\{\sigma^2_{\varepsilon_{(\lceil k/2 \rceil)}} - 2(k/n)E\left[\varepsilon_{(\lceil k/2 \rceil)}\varepsilon_{sum}\right] + 2\sum_{i=1}^{\lfloor k/2 \rfloor}\left(\sigma\left(\varepsilon_{(i)}, \varepsilon_{(\lceil k/2 \rceil)}\right) + \sigma\left(\varepsilon_{(n-i+1)}, \varepsilon_{(\lceil k/2 \rceil)}\right)\right)\right\} \quad (2.19)$$

Here, $\sigma\left(\varepsilon_{(i)}, \varepsilon_{(j)}\right)$ is the covariance between the i[th] and j[th] order statistics and the following simplification has been used

$$\sigma\left(\varepsilon_{(i)}, \varepsilon_{sum}\right) = E\left[\varepsilon_{(i)}\varepsilon_{sum}\right] - E\left[\varepsilon_{(i)}\right]\cdot E\left[\varepsilon_{sum}\right] = E\left[\varepsilon_{(i)}\varepsilon_{sum}\right] \quad (2.20)$$

The probability density function (pdf) of the j[th] order statistics, $\varepsilon_{(j)}$ is given [37] as

$$f_{\varepsilon_{(j)}}(x) = \left(\frac{n!}{(j-1)!\,(n-j)!}\right)\cdot\left[\int_{-\infty}^{x} f(x)\,dx\right]^{j-1}\cdot f(x)\cdot\left[\int_{x}^{\infty} f(x)\,dx\right]^{n-j} \quad (2.21)$$

Here $f(x)$ is the pdf of the Gaussian distribution that the mismatch errors follow. The joint pdf of the i[th] and j[th] order statistics $(1 \le i < j \le n)$ is given as

$$f_{\varepsilon_{(i)},\varepsilon_{(j)}}(u,v) = \left(\frac{n!}{(i-1)!\,(j-1-i)!(n-j)!}\right)\cdot\left[\int_{-\infty}^{u} f(x)\,dx\right]^{i-1}\cdot\left[\int_{v}^{\infty} f(x)\,dx\right]^{n-j}\cdot f(u)\cdot f(v)\cdot\left[\int_{-\infty}^{v} f(x)\,dx - \int_{-\infty}^{u} f(x)\,dx\right]^{j-1-i} \quad (2.22)$$

for $(-\infty < u < v < \infty)$. Using (2.21) and (2.22), the required parameters in (2.19) can be computed and the variance of INL after reordering can be obtained. We observe that minimizing error accumulation by reordering does reduce the variance of INL across all codes k as shown in Figure 2.11.

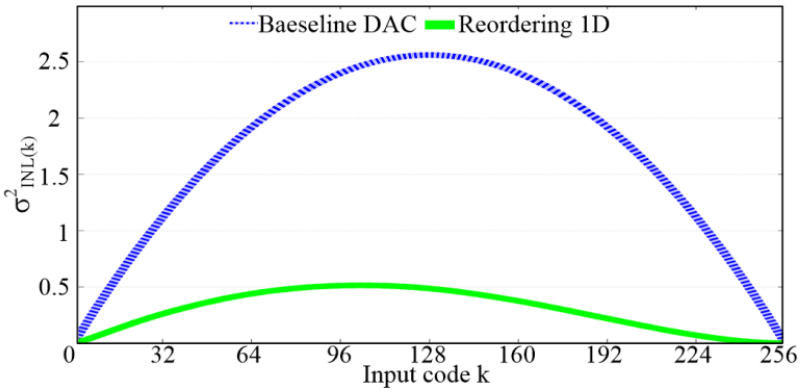


Figure 2. 11. Theoretical variance of INL for each code for 8-bit thermometer DAC with 20% current source mismatch error of the unit cells

To implement reordering for the more practical 2D thermometer DAC, we modify the reordering technique to alternate the switching sequence row-wise. We reorder the rows based on their sum of errors, $\varepsilon_{row,i}$ instead of individual elements to minimize the hardware costs. We access the rows as $\{\varepsilon_{row,(1)}, \varepsilon_{row,(n_{rows})}, \varepsilon_{row,(2)}, \varepsilon_{row,(n_{rows}-1)}, \cdots\}$, where $\varepsilon_{row,(i)}$ is the i[th] order statistics of $\{\varepsilon_{row,j} \mid j = 1\ to\ n_{rows}\}$. We sequentially access current elements within a row like it is done for the baseline case. In this case, assuming the input code $k = q \cdot n_{cols} + r$, the INL after reordering is given as

$$INL_{reorder,2D}(k) =$$

$$\begin{cases} \sum_{i=1}^{\left\lfloor \frac{q}{2} \right\rfloor} \left(\varepsilon_{row,(i)} + \varepsilon_{row,(n_{rows}-i+1)}\right) + \varepsilon_{row,\left(\left\lceil \frac{q}{2} \right\rceil\right)} + \sum_{i=1}^{r} \varepsilon_{\left(n_{rows}-\left\lceil \frac{q}{2} \right\rceil+1,i\right)} - \frac{k}{n}\varepsilon_{sum}; & for\ odd\ q \\ \sum_{i=1}^{\left\lfloor \frac{q}{2} \right\rfloor} \left(\varepsilon_{row,(i)} + \varepsilon_{row,(n_{rows}-i+1)}\right) + \sum_{i=1}^{r} \varepsilon_{\left(\left\lceil \frac{q}{2} \right\rceil+1,i\right)} - \frac{k}{n}\varepsilon_{sum}; & for\ even\ q \end{cases} \quad (2.23)$$

Here $\varepsilon_{(j,i)}$ is the i[th] mismatch error in the row whose sum of error is $\varepsilon_{row,(j)}$. Similar to the expression in (2.19), the variance of the 2D reordered DAC can be obtained from (2.23).

Since we reorder only the rows and sequentially access unit cells within the rows, it limits the overall reduction of INL_{DAC} of 2D reordered DAC when compared to the 1D reordered DAC as shown through Monte Carlo simulations in Figure 2.12.

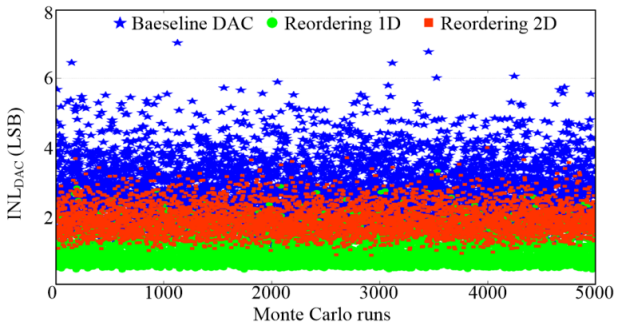


Figure 2. 12. With 20% current source mismatch error, 8-bit thermometer DAC's worst case INL amongst all codes for 5000 Monte Carlo runs

Its variance, in Figure 2.13, however, has a similar envelope to the 1D reordered DAC with parabolic trends within a row. This is because unit cells are not reordered within a row and hence demonstrating behavior consistent with the baseline DAC behavior.

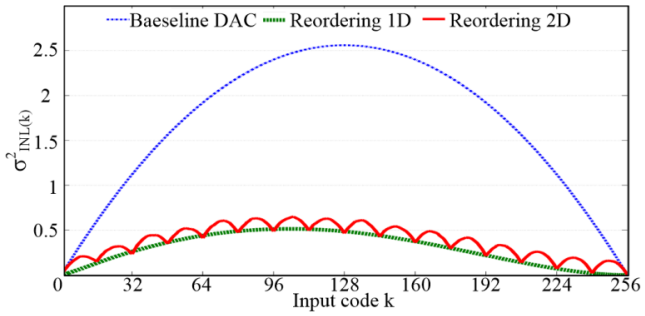


Figure 2. 13. Theoretical variance of INL for each code for 8-bit thermometer DAC with 20% current source mismatch error of the unit cells

Even with the limitations of row-wise reordering, simulations show at least a 41% reduction in INL_{DAC} across different values of σ_ε as shown in Figure 2.14.

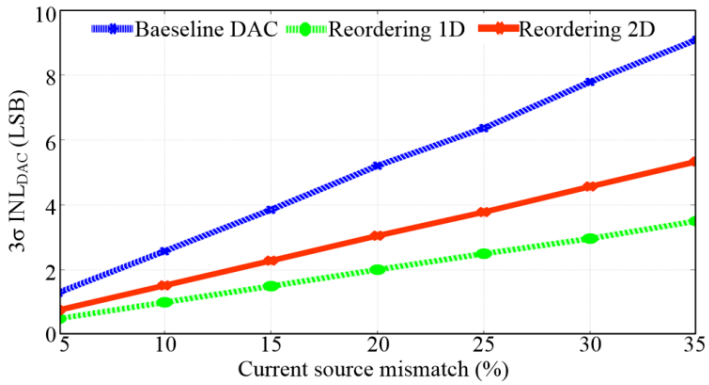


Figure 2. 14. Reduction in INL_{DAC} of 8-bit thermometer DAC by implementation of the reordering scheme for different current source mismatch errors

As reordering only changes the sequence of accessing the unit cells, it does not change the variance of the mismatch errors of the unit cells. Hence, it does not affect the DNL_{DAC}.

2.5 Dual-calibration technique

In one hand, redundancy helps in improving the mismatch between the DAC's unit cells whereas on the other, reordering helps in reducing error accumulation. Thus we propose a dual-calibration technique for a thermometer DAC where we first use redundancy within rows to reduce $|\varepsilon|$ and σ_ε of unit sources, followed by row-reordering to further reduce the INL. For 20% current source mismatch error in minimum length devices and 2 outliers per row, we observe 38% reduction in the 3σ of DNL_{DAC} simulated across 5000 Monte Carlo runs as shown in Figure 2.15. This matches well with our redundancy model as 36% improvement in matching is observed for same number of outliers (Figure 2.7).

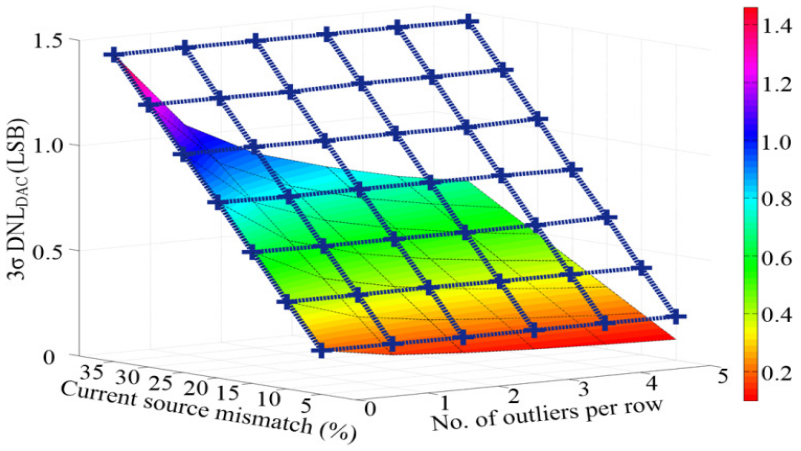


Figure 2. 15. Reduction in 3σ DNL_{DAC} of 8-bit thermometer DAC by implementation of the dual-calibration technique; baseline DAC (top mesh plane), dual-calibrated DAC (bottom plane)

Figure 2.16 shows the simulated improvement in INL_{DAC} for the dual-calibration scheme. The top mesh plane corresponds to the baseline DAC. The intermediate plane is when only redundancy part of the dual-calibration technique is implemented. With redundancy alone, for 20% current source mismatch error and 2 outliers per row we get 22% improvement in the 3σ of INL_{DAC}, making it evident that reducing the absolute error and its variance has a direct impact on INL. If we use this improved matching between unit cells due to redundancy in our reordering model, we obtain 51% INL improvement. In Figure 16 the bottom plane shows the INL_{DAC} when complete dual-calibration scheme is implemented. We see that with our proposed calibration technique, we reduce the 3σ of INL_{DAC} by over 55% in simulation, which agrees with our theory.

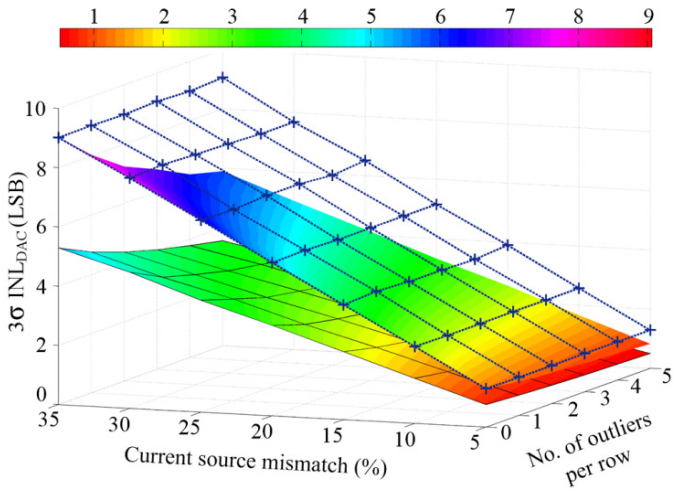


Figure 2. 16. Reduction in 3σ INL_{DAC} of 8-bit thermometer DAC by implementation of the dual-calibration technique; baseline DAC (top mesh plane), outlier-free DAC (intermediate plane), dual-calibrated DAC (bottom plane)

CHAPTER 3

ON-CHIP IMPLEMENTATION OF THE DUAL-CALIBRATION TECHNIQUE

3.1 Introduction to chapter

The previous chapter discussed the mathematical modeling of the proposed dual-calibration technique and laid the foundation of our work. To implement this calibration on-chip raises a number of concerns. This chapter starts with the discussion on the design requirements for the dual-calibrated DAC and the associated challenges. Following this, we first look at the on-chip implementation of the outlier-free DAC, which was the first generation of the proposed DAC design. Though the measured results of the outlier-free DAC matched well with the predicted improvement given by our theoretical models and simulation results in chapter 2, there was certain number of issues with the generation 1 of the DAC, as discussed in section 3.3.4, which lead to the development of the second generation of the proposed DAC. This generation is the on-chip implementation of the dual-calibrated DAC. Section 3.4 discusses the required circuit blocks and the calibration steps. We conclude this chapter by explaining the experimental results of the dual-calibrated DAC. We show measured linearity improvement, both in the DNL and the INL, given in section 3.5.1 that agree with our models and simulation results. We also compare this work with other similar calibration technique in terms of complexity and observe how the dual-calibration technique scales with technology.

3.2 Design considerations and challenges

Thermometer DACs are used in high speed I/O systems for offset correction in continuous-time linear equalizers, for providing coefficients for direct-feedback equalizers [38], and in phase interpolators [39], etc. Resolution typically ranges from 5 to 8 bits, motivating our choice of an 8-bit current-steering thermometer DAC as our target case. In chapter 2 we introduced the concept of adding redundant cells to improve the matching and static non-linearity in thermometer DAC's. Figure 7 in chapter 2 indicates that a total of 32 outliers in an 8bit DAC, 2 outliers in each row, show significant improvement in the matching between the unit cells. Hence, we explore a circuit design in this chapter where we add 2 redundant cells per row in our 8-bit DAC, i.e., $n_{red} = 2$.

As a circuit designer, there are number of challenges associated with complete on-chip implementation of a 2D dual-calibrated DAC. The important challenges are:

i. Determination of a suitable and inexpensive reference to carry out the redundancy scheme
ii. Determination of outliers for each row
iii. Once the outliers have been determined, how to disable the corresponding unit DAC cells
iv. Addressing of the unit cells to take into account the outlier unit cells' position
v. Ranking of the rows of the outlier-free DAC according to the reordering algorithm introduced in chapter 2
vi. Storing of the row ranks
vii. Addressing DAC while taking row ranks into consideration

In the rest of the chapter, we will discuss how the above challenges are addressed in the circuit implementation of the dual-calibrated DAC with 2 outliers per row.

3.3 First generation of our proposed DAC: outlier-free DAC

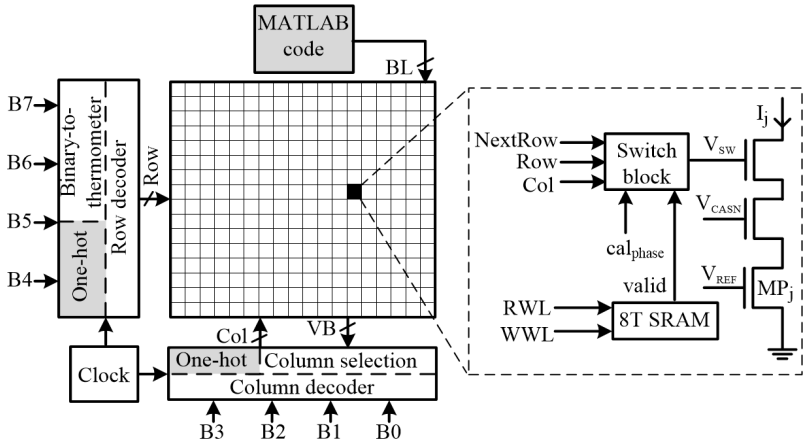


Figure 3. 1. Complete outlier-free DAC design

As the first design, we aimed at developing only the outlier-free DAC shown in Figure 3.1. Out of the challenges discussed in the previous section, we concentrated only on the on-chip implementation of disabling the outliers in each row and altering the addressing scheme for the columns to carry out outlier elimination. To carry out the calibration process, we first determine all the unit cell currents by traversing through each cell using one-hot decoders for both row and column addressing. This information is then used by our MATLAB program to determine the outliers in each row using the mean current of the complete DAC as the reference. The program identifies 2 unit cells which have maximum absolute difference from the mean current. After the outlier determination process, a stream of bits is used to write the status of each unit cell in the associated memory as shown in Figure 3.2.

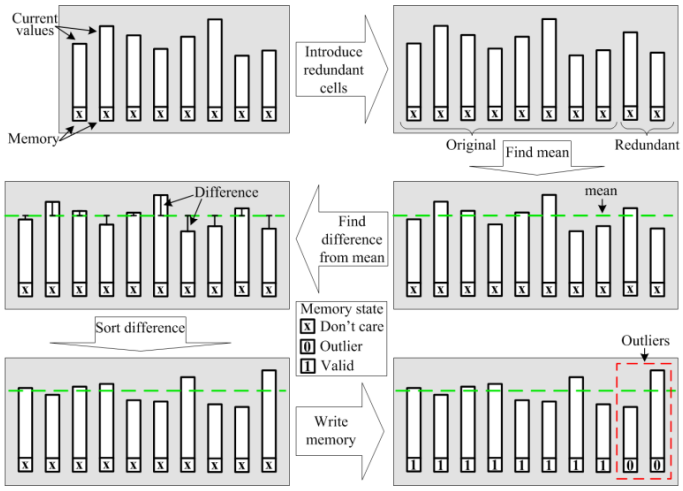


Figure 3. 2. Algorithm for on-chip implementation of redundancy scheme

For row addressing of this outlier-free DAC, standard binary-to-thermometer decoder is used. As for the column addressing, an alternate column decoder is developed to take into account the position of the outliers in each row. The following sub-sections discuss the designs of the unit cell to implement the disabling of outliers and of the column section decoder along with experimental results followed by the issues in the generation 1 of the DAC design laying the path for the second generation of the DAC.

3.3.1 DAC unit cell design – generation 1

After we determine the outliers in each row using the currents of each unit cell as the inputs to our MATLAB program, this information is stored in the unit cells as a "valid" bit in the memory associated with each DAC unit cell. We store a 0 if the unit cell is an outlier or 1 if it is to be considered in the DAC array. Figure 3.3 shows the design of the generation 1 DAC unit cell.

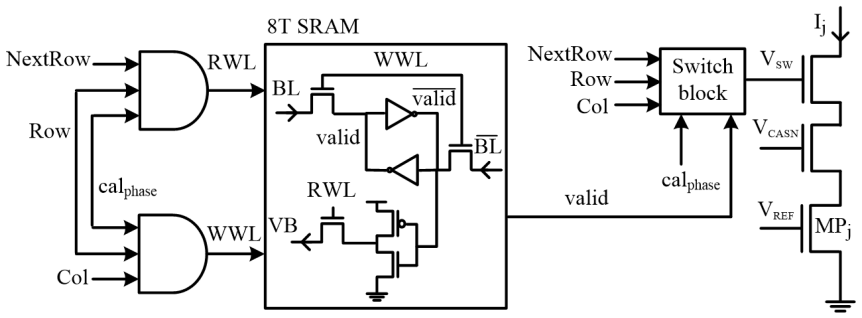


Figure 3. 3. Design of the unit cell – generation 1

A slight variation of the 8T SRAM proposed in [40], which has a separate read-out switch to decouple the writing and reading phase of the SRAM, was used as the memory. The switch logic block is implemented using standard digital logic gates. It controls the switching of the DAC unit cell depending on the row, the next row, the column and the valid bit values of the unit cell. Both the write enable signal, WWL and the read enable signal, RWL were generated within each cell as shown using outputs of the row and column decoders and the phase of calibration of the DAC. All the SRAMs share the input data bit lines – BL and $\overline{BL}$. The read out switch in the 8T SRAM enables the column selection decoder to read the valid bit in the last accessed row of the DAC. The unit cells in the previous rows are controlled by the $valid$ signal alone. The outputs of all the unit cells are connected together.

The valid bits of all the cells are written one by one by enabling the WWL signal of that particular unit cell. Hence 287 address cycles are required for writing the valid bits of all DAC unit cells as there are total of 287 unit cells (255 unit cells for the 8-bit DAC with 32 outliers).

3.3.2 Column selection decoder

After the determination of all the outliers and the storing of the status of each unit cell of the DAC, to complete the outlier elimination process, the column addressing of the dual-calibrated DAC needs to be altered from a standard thermometer DAC, which uses a binary-to-thermometer decoder for the addressing of its cells. The column selection decoder of the dual-calibrated DAC maps the column bits of the DAC via a binary-to-thermometer decoder as shown in Figure 3.4.

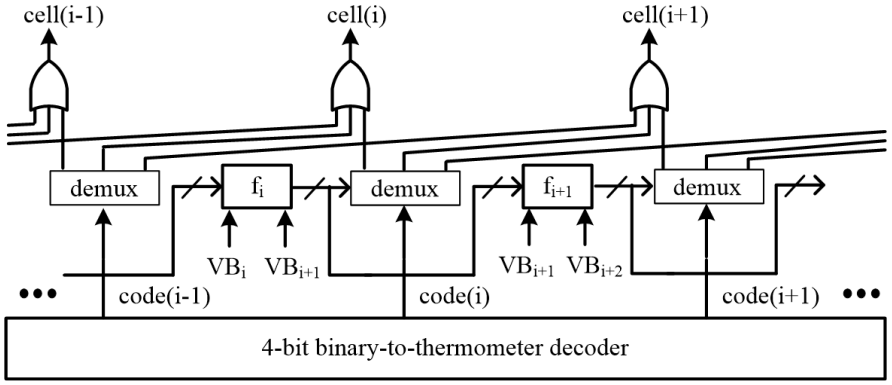


Figure 3. 4. Column selection decoder

Because of the redundant and "invalid" cells, the decoder also needs to consider the status stored in the memories of the cells in a row. If a cell is invalid, then it is skipped by the decoder. If the i^{th} unit cell has a valid status, then the i^{th} thermometer decoder output, code(i) is passed as the column signal for the i^{th} cell. If the i^{th} unit cell is an outlier, code(i) is passed to the $(i+1)^{th}$ unit cell. If both i^{th} and $(i+1)^{th}$ unit cells are outliers for the row, then $(i+2)^{th}$ unit cell gets the code(i). In other words, the i^{th} mapping function, f_i uses the status of the i^{th} and $(i+1)^{th}$ unit cells, VB_i and VB_{i+1} and maps the i^{th} thermometer decoder output, code(i) to the i^{th}, $(i+1)^{th}$ or $(i+2)^{th}$ unit cell of the row as follows

$$f_i(VB_i, VB_{i+1}, f_{i-1}) = VB_i + VB_{i+1} + f_{i-1} \quad 0 \le i \le 15 \tag{3.1}$$

Here, $f_{-1} = 0$. The f_i block is implemented using a 2-bit adder and the 2-bit output controls the i^{th} demultiplexer (demux). The demux passes the code(i) to the appropriate cell depending on f_i. The code(i) goes to the i^{th} cell if $f_i = 0$ or to the $(i+1)^{th}$ cell if $f_i = 1$ or else to the $(i+2)^{th}$ cell. The value of f_i can be at most 2 since there are only 2 redundant cells per row.

3.3.3 Experimental results of first generation DAC

We taped out the first generation of the DAC design in TSMC 65nm CMOS process and the chip micrograph is shown in Figure 3.5.

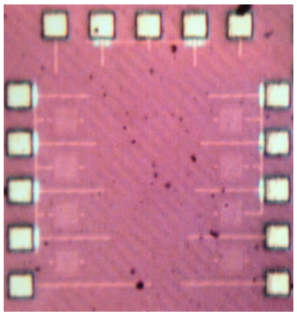
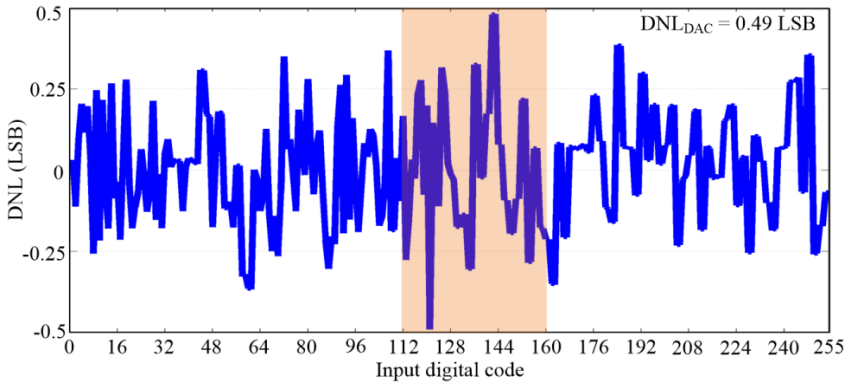
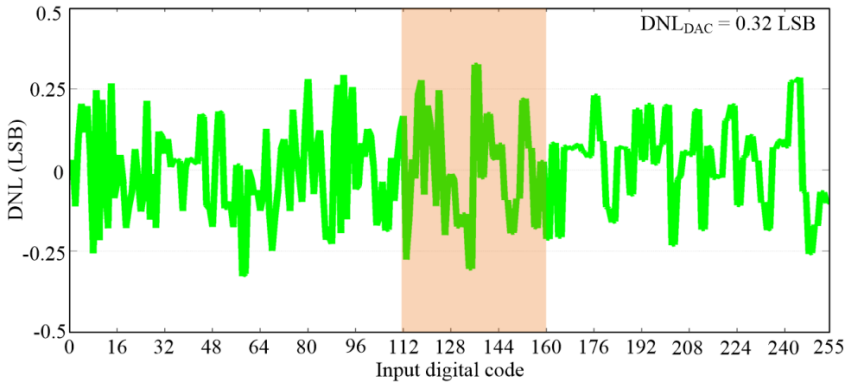


Figure 3. 5. Chip micrograph of the 8-bit outlier-free DAC (generation 1 DAC design)

DNL measurement from one of the chips tested is given in Figure 3.6. We observed that for the baseline case of the 8-bit thermometer DAC, DNL_{DAC} (the maximum absolute DNL across all codes of the DAC) was 0.49 LSB. By including just 2 outliers per row, the DNL_{DAC} of the 8-bit outlier-free DAC was reduced to 0.32 LSB. This shows a 35% DNL_{DAC} reduction. This matches well with our theory and simulation results which predicted an improvement of 36% and 38%, respectively as discussed in chapter 2.



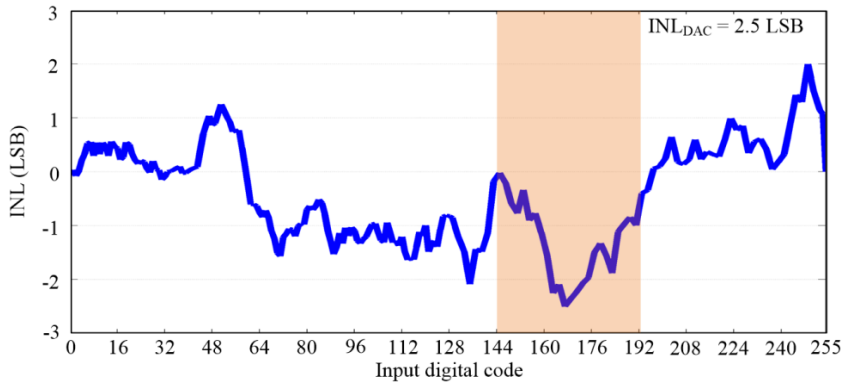
(a) DNL of Baseline DAC



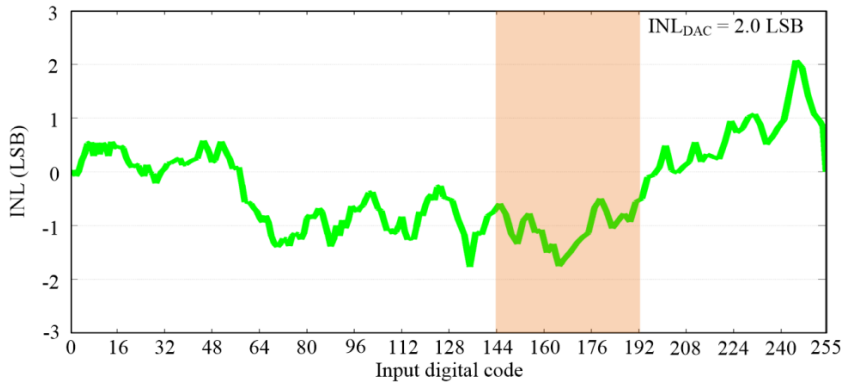
(b) DNL of outlier-free DAC

Figure 3. 6. Measured DNL from generation 1 DAC design. Shaded area is used to emphasize the reduction in DNL

As discussed in chapter 2, redundancy also helps in improving the INL_{DAC} (maximum absolute INL across all codes of the DAC) by reducing the variance of the mismatch error. Fig, 3.7 shows the measured INL from one of the chips of the generation 1 of the DAC. The INL_{DAC} for the baseline DAC was 2.5 LSB. With the introduction of redundant unit cells followed by outlier elimination, the INL_{DAC} dropped to 2 LSB, resulting in a 20% improvement in INL_{DAC}. This agrees with our simulation results discussed in chapter 2 which showed an improvement of 22% in 3σ of INL_{DAC}.



(a) INL of Baseline DAC



(b) INL of outlier-free DAC

Figure 3. 7. Measured INL from generation 1 DAC design. Shaded area is used to emphasize the reduction in INL

3.3.4 Issues with generation 1 design

The first generation of the DAC design was developed with the goal of implementing an outlier-free DAC on-chip. It only addressed couple of the challenges of the complete on-chip implementation of the dual-calibrated DAC. Hence, the second version of the DAC needed to be developed to address the other challenges. Also, the design of the unit cell for the generation 1 of the DAC was not optimal. The logic for the enable signals and the switching contributed to a lot of the area in the unit cell. The problem was that all the required signals were generated within

each cell without any sharing within a row or a column. The second generation of the DAC design needed to address this concern by making a lot of these signals shared between either the rows or the columns and hence decreasing the size of the dual-calibrated DAC's unit cell, justifying the need to use dual-calibration technique instead of just increasing the size of the current source of the unit cell to improve DAC linearity.

3.4 Second generation of our proposed DAC

As some of the challenges were not met by the first generation of the DAC, the second generation of the DAC design addresses those challenges discussed earlier for the on-chip implementation of the dual-calibrated DAC. They are given as follows:

i. On-chip determination of a suitable and inexpensive reference to carry out the redundancy scheme
ii. Determination of outliers for each row
iii. Reducing area of unit cell by sharing common signals
iv. Ranking of the rows of the outlier-free DAC according to the reordering algorithm introduced in chapter 2
v. Storing of the row ranks
vi. Addressing DAC while taking row ranks into consideration

Figure 3.8 shows the complete dual-calibrated DAC architecture. The outputs of all the unit cells in a row are connected together. The outputs of the different rows are connected together through

switches which are controlled by the *Row* signal from the row selection decoder. By doing so, we have moving the switching logic outside the unit cell and hence, reduced the area of the cell.

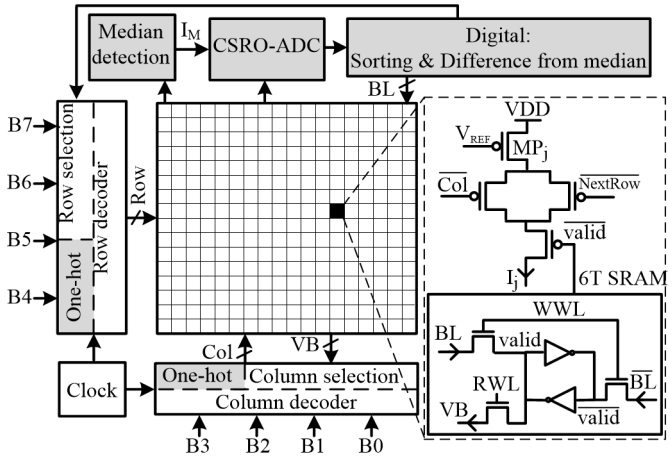


Figure 3. 8. Complete 8-bit dual-calibrated thermometer DAC architecture with all the calibration blocks and modified unit cell (shaded blocks used only during calibration)

Calibration occurs only at the beginning of operation and proceeds as follows. Initially we write 1 to all the memory units in the cells so that currents from all the unit cells can be accessed. Then, we determine the median, in place of the mean, as will be discussed in the next sub-section, using the median detection block. Next, we find the outliers in each row by first converting the analog current values from each cell and the median current to digital words. Then we calculate the absolute difference between the median value and the unit cell values and denote the two cells per row with the maximum absolute difference as the outliers. Following the outlier determination process, we write the status of each unit cell row-wise to obtain the outlier-free DAC. After this, we convert the row currents of the outlier-free DAC into digital words. Finally, we determine the row ranks as per algorithm of row reordering discussed in chapter 2 and then store the row ranks in the memory bank of the row selection decoder.

The following sub-sections discuss the choice of on-chip reference for the redundancy scheme and the implementation details of the different blocks required for the dual-calibration technique.

3.4.1 Reference selection

In order to implement the redundancy method of the dual-calibration technique, we must identify the outliers in each row. To do so, we compare each unit cell's output with the mean current of the DAC and use the difference to determine if that cell is an outlier as discussed in Section II. Using the mean current as the reference is expensive, due to the need to compute and store this value and continuously refresh the stored value due to leakage. Instead, we compute a median current of the DAC as a reference.

We can calculate the error induced by this approximation as ϵ, the error between the DAC's mean current, I_μ and the median current, I_M. For I_M to be a viable reference and to be used instead of the mean current, probability that $I_\mu - \epsilon < I_M < I_\mu + \epsilon$ should be 1. In other words, the following needs to hold

$$\int_{I_\mu-\epsilon}^{I_\mu+\epsilon} f_{I_M}(i_M)\, di_M \to 1 \tag{3.2}$$

Here, $f_{I_M}(i_M)$ is the probability density function (pdf) of the median current. To determine $f_{I_M}(i_M)$, we use order statistics of the DAC's unit cells. Since the unit cell currents are random samples from a Gaussian distribution and the median current is the middle value when all the cell currents are arranged in increasing order, its pdf is given [37] as

$$f_{I_M}(i_M) = \left(n!/\left(\left(\frac{n-1}{2}\right)!\right)^2\right)\left[\int_{-\infty}^{i_M} f(x)\, dx\right]^{\frac{n-1}{2}} \cdot f(i_M) \cdot \left[\int_{i_M}^{\infty} f(x)\, dx\right]^{\frac{n-1}{2}} \tag{3.3}$$

Here, $f(x)$ is the pdf of the unit cells and is Gaussian.

For a sufficiently large n, (3) can be simplified as

$$f_{I_M}(i_M) = \left(n \cdot f(i_M) / \sqrt{\pi \frac{n-1}{2}}\right) \exp\left(\frac{-(i_M - i_\mu)^2}{1/\left(2(n-1) f_{I_\mu}(i_\mu)\right)^2}\right) \tag{3.4}$$

Here $f_{I_\mu}(i_\mu)$ is the pdf of the mean which equals to $f(x)$ for sufficiently large n. Figure 3.9 shows the validity of the approximation of median as the mean with respect to the total number of unit cells in the DAC.

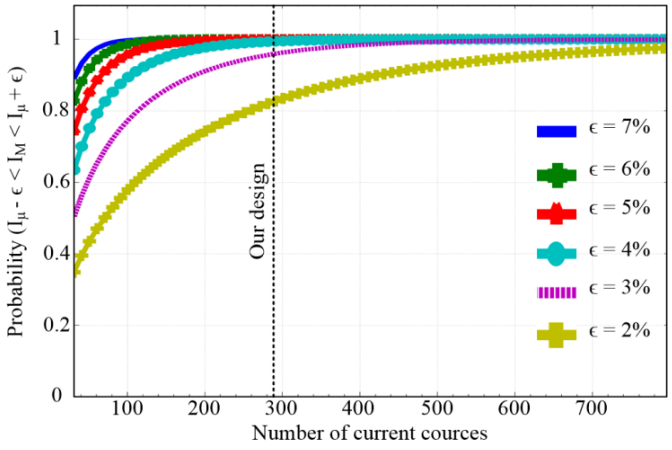


Figure 3. 9. Convergence of median to mean with 20% current source mismatch error

For the 8-bit dual-calibrated thermometer DAC with 2 outlier per row, i.e., total of 288 unit cells or current sources, the error in the approximation, at worst, is 4% which is acceptable for the given current source mismatch ($\sigma_\varepsilon = 20\%$).

3.4.2 Median detection

To determine the median current we estimate the median value by comparing the current from the median cell (Figure 3.10), with current from each of the unit cells. We traverse through the

DAC unit cells using one-hot decoder for both the column and row addressing. The median cell is tuned to an output current such that the number of DAC unit cells with currents higher than the median cell's is equal to the number of DAC unit cells with lower currents.

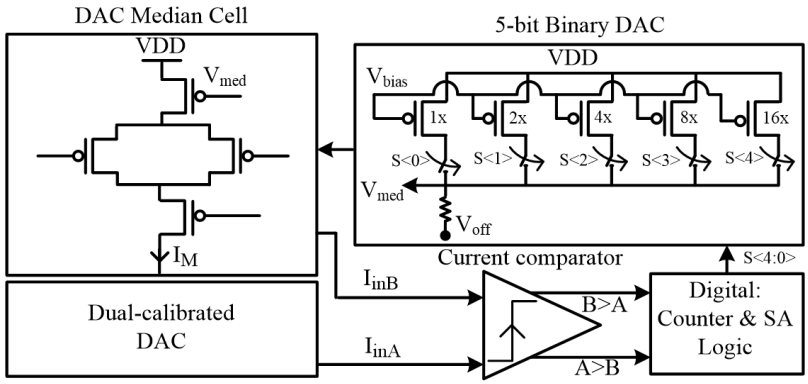


Figure 3. 10. Median detection circuit

To compare the median current with the unit cell currents, a fast comparator with high accuracy is required. We use a current comparator with nonlinear feedback (through inverter Inv1) to obtain high resolution for small current differences as shown in Figure 3.11.

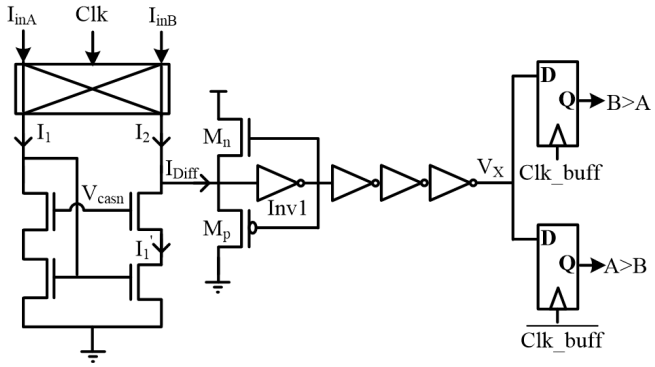


Figure 3. 11. Current comparator used in median detection circuit (Clk_buff is a delayed version of Clk)

To understand the working of the comparator let's suppose $I_{inA} < I_{inB}$. During the positive clock phase, $I_1 = I_{inA}$ and $I_2 = I_{inB}$. If the bottom NFET transistors are well matched, then

$I_1' = I_1$ and $I_{Diff} = I_2 - I_1' = I_{inB} - I_{inA}$. Since I_{Diff} is a positive current, the feedback inverter Inv1 regulates the bias of M_p to maintain I_{Diff} and forces V_X high. The output signal $B > A$ becomes high. On the negative clock phase, the input currents are switched. Now, $I_1 = I_{inB}$ and $I_2 = I_{inA}$ and hence, I_{Diff} is a negative current. The feedback inverter Inv1 now regulates the bias of M_n to maintain I_{Diff} and V_X is asserted low. The output signal $A > B$ becomes low. For the opposite case when $I_{inA} > I_{inB}$, during the positive clock phase I_{Diff} is a negative current. Hence, V_X is low which makes the output signal $B > A$ to become low. During the negative clock phase, I_{Diff} is a positive current and V_X is pulled up making the output signal $A > B$ to go high. For the situation when $I_{inA} = I_{inB}$, V_X remains low during both phases of the clock and hence both output signals remain low.

A low resolution binary DAC is used to tune the bias of the median cell as shown in Figure 3.10. We successively approximate the position of the median cell's current within the DAC array until it lies in the center of the array as expected. As there are 288 unit cells in the DAC, using this successive approximation (SA) logic based median detection requires a maximum of 1440 address cycles to determine the median, with a 5-bit binary DAC.

3.4.3 Outlier determination

Outliers are those DAC unit cells whose values lie in the tails of the distribution of the currents from the unit cells. As discussed earlier, we use the median current, I_M as the reference and the absolute difference from the median current determines if a unit cell is included in the array or considered an "outlier". Hence, to determine the outlier cells of the dual-calibrated DAC, we

obtain the 2 unit cells in each row whose absolute mismatch from I_M is the maximum. We can carry out this operation either in analog domain or in digital domain. For analog domain implementation, we first need to find the unit cell in each row with maximum absolute difference from I_M by comparing each unit cell's current with I_M using an analog current comparator and then to determine the second outlier, we disable this first outlier cell and consider the rest of the unit cells in the row for the next set of comparisons. For digital domain implementation, we need to first convert all the current of the unit cells and median current into their digital counterparts. This would be followed by subtraction of the digitized median current from the digitized unit cells' current values. And lastly, we would pick the 2 with the largest magnitude and term then as outliers. For our dual-calibrated DAC implementation, we chose to go with the digital domain implementation of the outlier determination since digital circuits are less affected with CMOS scaling and lesser power consumption.

3.4.4 Analog to digital conversion

To digitize the unit cells' currents and the median current, low resolution analog to digital conversion is performed using a current starved ring oscillator ADC (CSRO-ADC) as shown in Figure 3.12. One-hot decoders are used for addressing the individual unit cells.

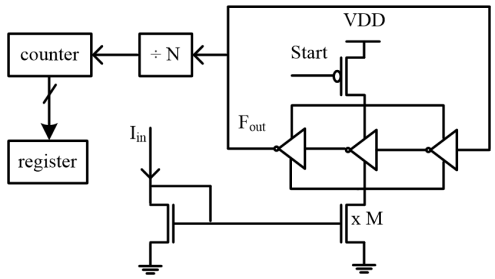


Figure 3. 12. Current starved ring oscillator analog to digital converter

The current from a unit cell is fed to the CSRO-ADC. The frequency of the output F_{out} is determined by (5), where M is the factor by which the input current is scaled, V_{DD} is the supply voltage, C_L is the capacitive load seen at the output of each stage and N is the number of stages, which is three in our case.

$$F_{out} = (M\ I_{in})/(2N\ VDD\ C_L) \tag{3.5}$$

Hence, the frequency of the output, F_{out} is a function of the input current. The counter counts the cycles of the output, F_{out} for a fixed time while the Start pulse is low and then saves the result in a register. To compare this value with current from another unit cell of the DAC, we simply feed in the new current to the CSRO-ADC and repeat the process. The output of the counter is then saved in another register and the contents of the two registers are compared to determine a winner. To convert all the 288 unit cells' currents into their digital counterparts requires 288 address cycles.

3.4.5 Design of a DAC unit cell – generation 2

Like in generation 1, once the outliers for each row of the DAC have been determined this information is stored in the unit cells as a "valid" bit in the memory associated with each DAC unit cell. The proposed DAC cell is similar to a standard single-ended DAC cell except for the additional memory to store the "valid" bit (VB), shown in Figure 3.13.

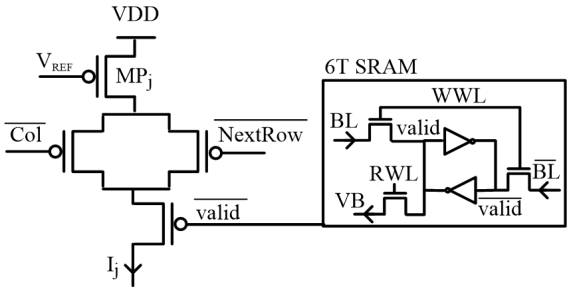


Figure 3. 13. Unit cell of the dual-calibrated thermometer DAC

For the second generation of the unit cell we use a standard 6T SRAM as the memory along with a separate read-out switch since we realized that the isolation inverter close to the read-out switch in the 8T SRAM of the generation 1 unit cell (Figure 3.3) can be removed without lowering the performance of the memory unit. All the SRAMs share the input data bit lines – BL and $\overline{BL}$, columnwise. The read out switch enables the column selection decoder to read the valid bit in the last accessed row of the DAC. The unit cells in the previous rows are controlled by the $valid$ signal alone. All the enable signals for the SRAMs, i.e., WWL and RWL are generated internally (but outside the unit cell) using only outputs from the row selection decoder as follows

$$Enable_{signal} = cal_{phase} \cdot Row \cdot \overline{NextRow} \tag{3.6}$$

Here, $Enable_{signal}$ can be either WWL or RWL depending on the phase of calibration, cal_{phase} (WWL is $Enable_{signal}$ when writing the status of all unit cells and RWL is $Enable_{signal}$ when we have to reach the stored status of these cells). All SRAMs in a row share the read (RWL) and write (WWL) signal. All the unit cells in a column share the output of the read-out switch of the SRAM, i.e, the signal VB. But since only the last accessed row's RWL is high, the column selection decoder only gets the valid bits of that row.

The valid bits of all the cells in a row are written together by enabling the WWL signal of that particular row. Hence 16 address cycles are required for writing the valid bits of all DAC unit cells.

3.4.6 Row rank determination

For the reordering scheme of the dual-calibration technique, we need to determine the reordered ranks of the rows depending on the magnitude of the individual row currents. For this, we first obtain the digital counterparts of the row currents using the CSRO-ADC in Figure 3.12. During this phase of calibration, one-hot decoder is used for row addressing and the column selection decoder is used for column addressing as we need to obtain the row currents of the outlier-free DAC. To convert the row currents of the outlier-free 8-bit thermometer DAC into digital words requires 16 address cycles. After obtaining the digital words, these are sorted and reordered according to the reordering algorithm to obtain the ranks of the rows.

3.4.7 Row selection decoder

For implementing the reordering scheme, the standard binary-to-thermometer decoder needs to be replaced with an alternate decoder which accesses the rows according to their respective order. So, once the ranks of the rows have been determined, the row orders are stored in a memory bank consisting of 16 4-bit SRAMs. Each row rank is written sequentially using the one-hot decoder for addressing the rows and it requires 16 address cycles for writing all the row ranks. During DAC operation, the incoming row bits, rb, are compared with the stored ranks

using digital comparators as shown in Figure 3.14 to switch on the appropriate rows. For rows with $rank > rb$, $NextRow$ is high and for rows with $rank \geq rb$, Row is set high.

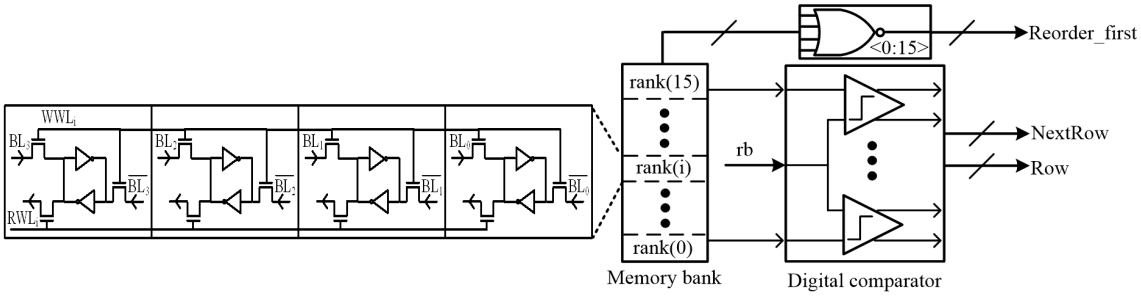


Figure 3. 14. Row selection decoder

In a standard 8-bit thermometer DAC, there are only 255 unit cells. But for the 8-bit dual-calibrated DAC, we need all 256 unit cells since the physical location of the unit cell corresponding to input code 0 is not known a priori. It can be any one of the unit cells in the 0th column of the DAC. One way to remove the contribution of this 0th unit cell is to remove it during post processing of the DAC output, i.e., remove it from the DAC output current at each input code in software. For our dual-calibrated DAC implementation, we disable this 0th unit cell on-chip. To do so, we add the $Reorder\_first$ signal in the row selection decoder which is high for the row with the rank of 0 and low for rest of the rows. We also add a switch inside each unit cell in the 0th column which disables the current source of the 0th unit cell using the value of $Reorder\_first$ signal.

3.5 Experimental results of dual-calibrated DAC

We fabricated an 8-bit current steering thermometer DAC in TSMC 65nm CMOS process with two redundant DAC cells in each row. The die photograph is shown in Figure 3.15.

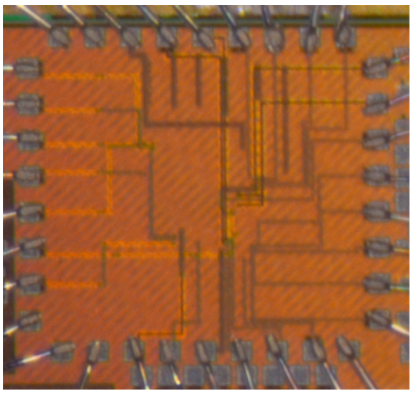
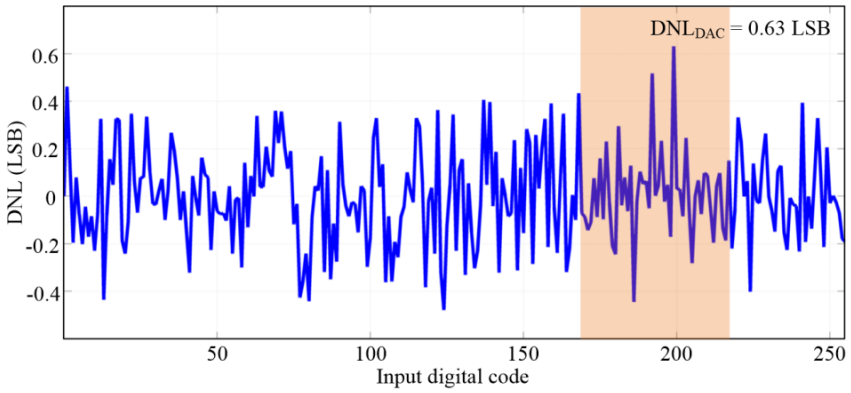


Figure 3. 15. Chip micrograph of the dual-calibrated DAC

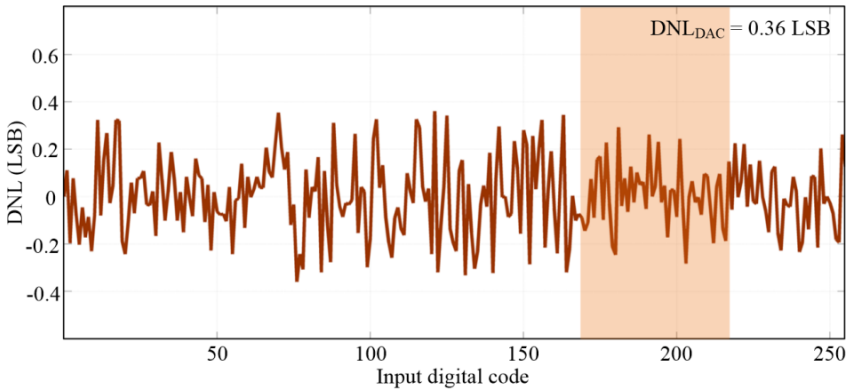
The total active core area of the dual-calibrated DAC is 0.01 mm^2 and it consumes 0.6mW using a 1V supply. The digital sorting operations were performed off-chip while all other conversion, calibration, and comparison blocks were integrated on-chip.

3.5.1 Static linearity performance improvement

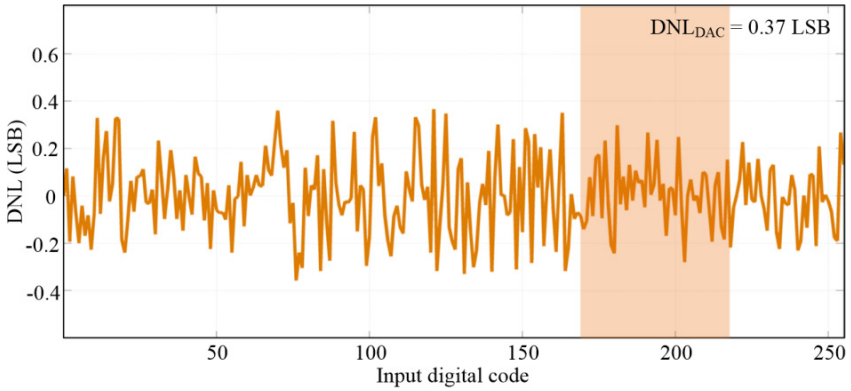
In order to observe the linearity improvement across process, we measured 16 samples across one run. Figure 3.16 and Figure 3.17 shows the measured DNL and INL from one of the chips, respectively.



(a) DNL of Baseline DAC



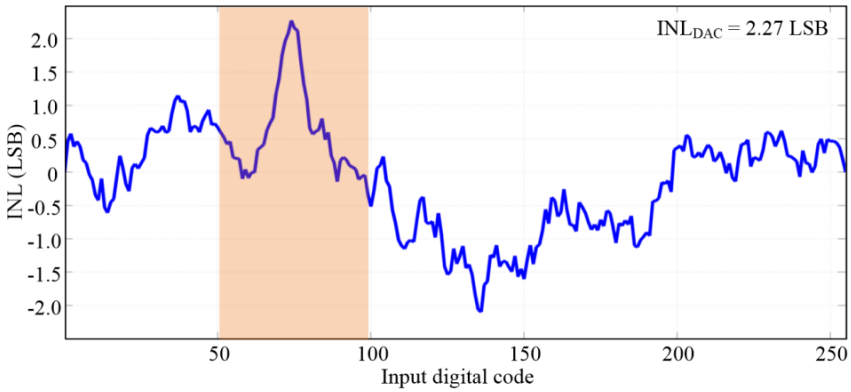
(b) DNL of dual-calibrated DAC (ideal: complete off-chip calibration)



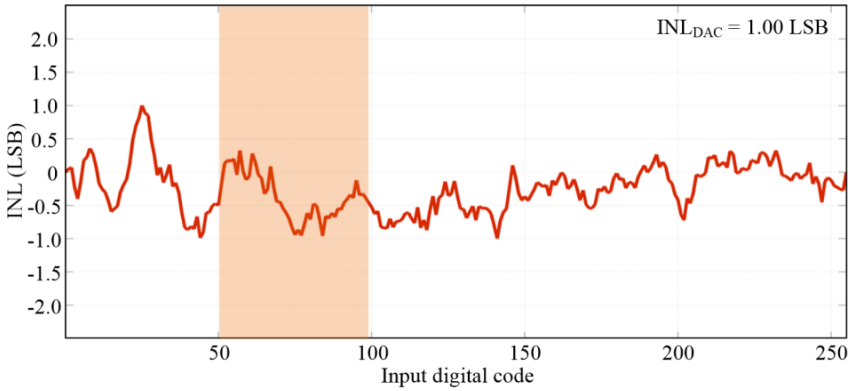
(c) DNL of dual-calibrated DAC (testing: using on-chip calibration circuits)

Figure 3. 16. Measured DNL from generation 2 DAC design. Shaded area is used to emphasize the reduction in DNL

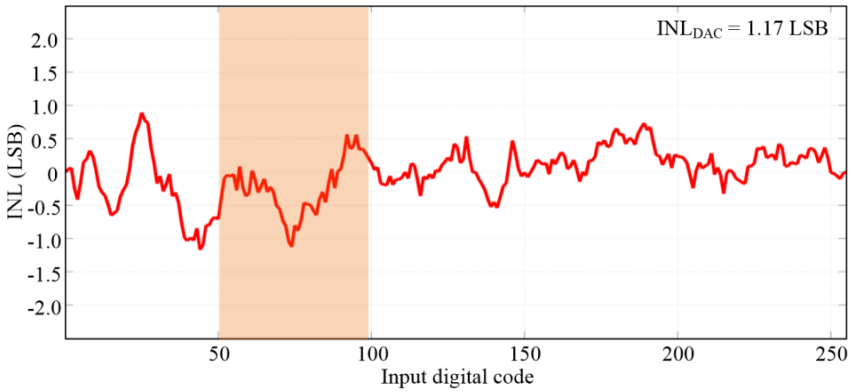
As we observe from comparing Figure 3.16(b) and Figure 3.16(c) and from comparing Figure 3.17(b) and Figure 3.17(c), any inaccuracy in our calibration circuits (median detection, CSRO-ADC) does not affect the overall performance improvement.



(a) INL of Baseline DAC



(b) INL of dual-calibrated DAC (ideal: complete off-chip calibration)



(c) INL of dual-calibrated DAC (testing: using on-chip calibration circuits)

Figure 3. 17. Measured INL from generation 2 DAC design. Shaded area is used to emphasize the reduction in INL.

From the scatter plot in Figure 3.18 we can visualize how the two methods of the dual-calibration technique impact the DAC linearity.

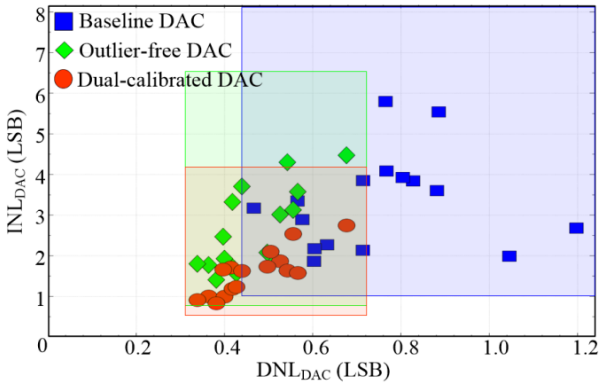
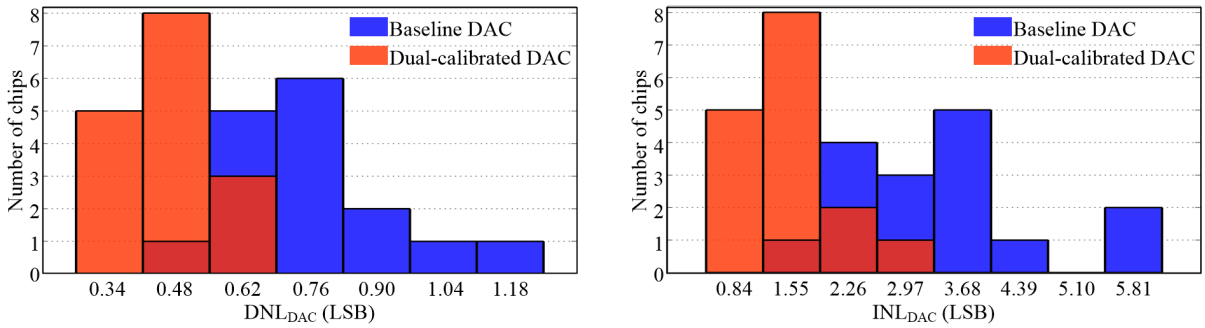


Figure 3. 18. Measured results from 16 chips in TSMC 65nm (with average starting mismatch of around 20% between DAC cells) overlaid on the simulation results from the 5000 Monte Carlo runs

By first implementing redundancy and obtaining an outlier-free DAC, the DNL_{DAC} is reduced from 0.75 LSB to 0.47 LSB on average. We also note that the INL_{DAC} decreases from 3.23 LSB to 2.64 LSB on average, showing a 20% improvement which matches with our simulation results as discussed in chapter 2. INL_{DAC} further reduces to 1.58 LSB by reordering, showing an additional 40% improvement in linearity. The boxed regions in Figure 3.18 indicate the three sigma span of the expected results from simulations and the measured results are contained within these regions as expected.



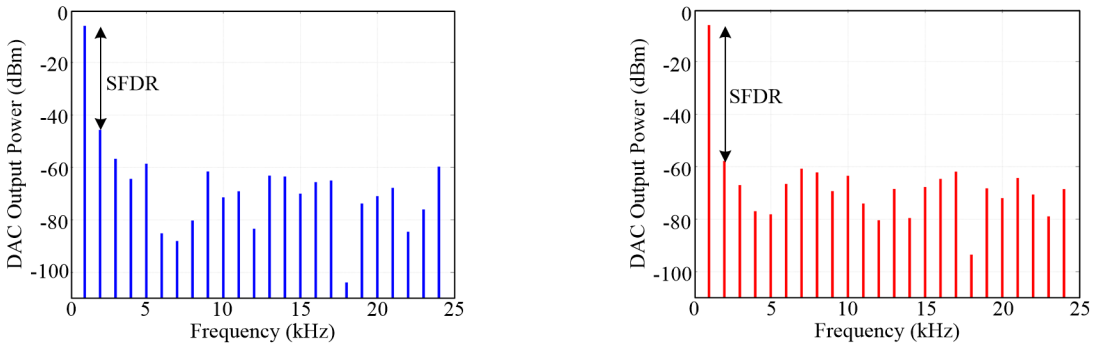
(a) measured DNL_{DAC} (b) measured INL_{DAC}

Figure 3. 19. Histograms of measured linearity for 8-bit current steering thermometer DAC

From Figure 3.19 we observe an improvement of 36% in DNL_{DAC} and 50% in INL_{DAC} on average by implementing the dual-calibration technique. These measured results of DNL_{DAC} and INL_{DAC} match well with the simulated results (chapter 2), which showed an improvement of 38% and 55%, respectively and our theoretical models (chapter 2), which predicted an improvement of 36% and 51%, respectively.

3.5.2 Dynamic linearity performance improvement

Though the dual-calibration technique aims at improving the static linearity of the DAC, to see how its benefits extend to improvement in the dynamic linearity of the DAC, we measured SFDR for a 1 kHz input signal and 50 kHz sampling frequency. Figure 3.20 shows the output spectrum of one of the measurements and we note that improving the linearity of the DAC improves the SFDR.



(a) Baseline DAC (b) Dual-calibrated DAC

Figure 3. 20. Measured SFDR of 8-bit current steering thermometer DAC

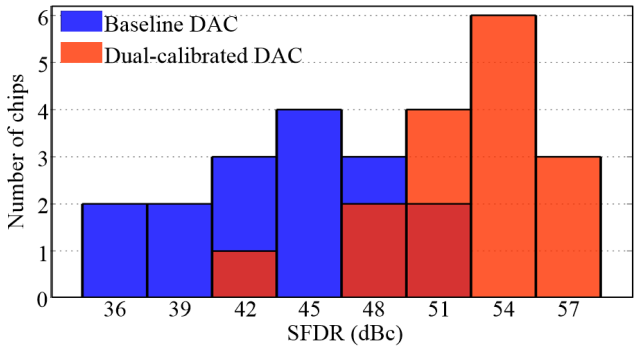


Figure 3. 21. Histogram of measured SFDR for 8-bit current steering thermometer DAC

We observe from the histogram of the SFDR measurements in Figure 3.21 that we get 20% improvement in the SFDR on an average by implementing the dual-calibration technique.

3.6 Comparison with existing techniques

Table 3.1 compares measured results of the proposed dual-calibration technique and other calibration techniques like the DMM [25], SSPA [26], and the DNL-based switching [28] discussed in section 1.2.2, all focusing on improving static linearity for thermometer DACs.

Table 3.1

COMPARISON OF DIFFERENT CALIBRATION TECHNIQUES BASED ON STATISTICS OF THE DISTRIBUTION

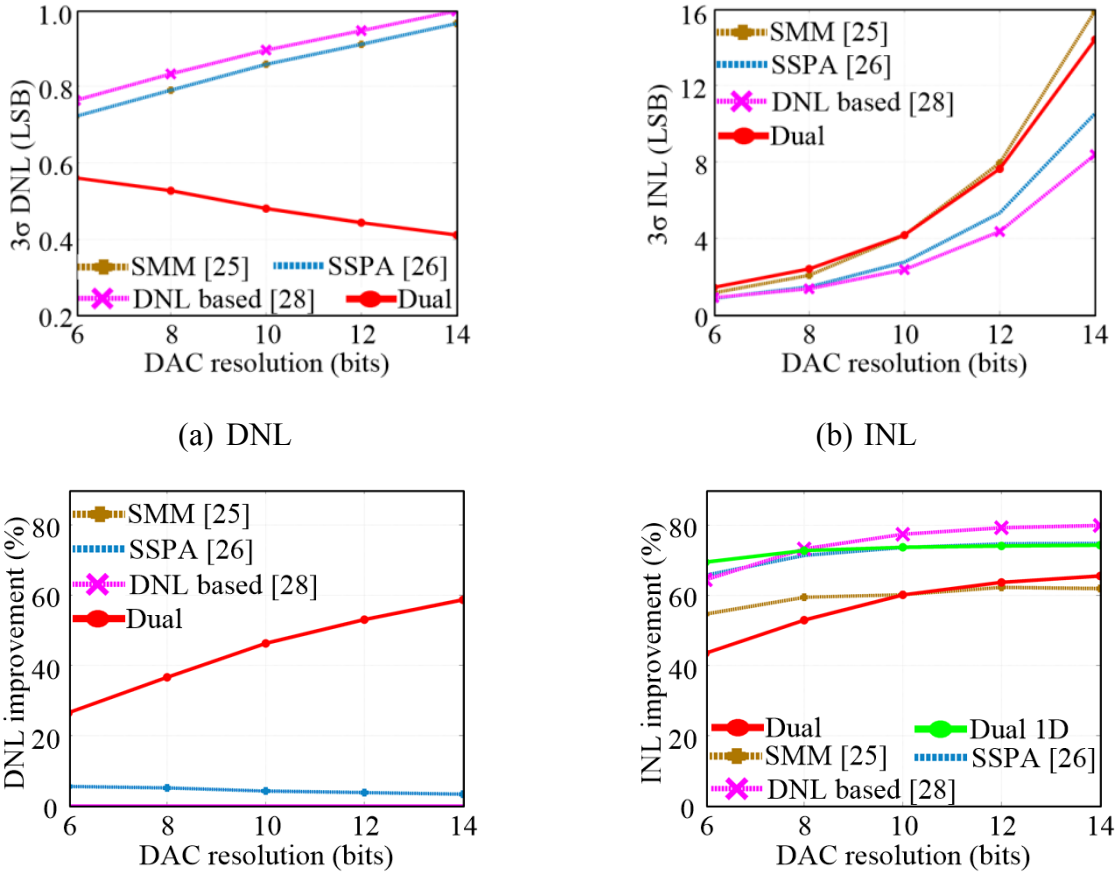
	[25]	[26]	[28]	This work
Process	0.14 µm	0.18 µm	0.35 µm	65 nm
Resolution of DAC	14	14[a]	10	8
DNL improvement (%)	0	16.34	0	36.07
INL improvement (%)	43.75	44.56	43.94	50.05
Algorithm complexity[b]	$O(n^2)$	$O(n^2)$	$O(n^2)$	$O(n)$

[a] 14-bit DAC but algorithm applied to only the 7 MSB unary bits.

[b] n is the total number of thermometer coded unit cells.

For a more fair comparison, we simulated all these calibration techniques for different DAC resolutions having 20% current source mismatch error in the unit cells. The redundancy ratio was kept at 12.5% for every DAC size. Static mismatch mapping (SMM) uses the same algorithm given in [25] but is applied for static mismatch errors. Figure 3.22 shows the 3σ of the DNL and the INL for all the calibration techniques under consideration. Due to the outlier elimination process, we observe significant improvement in DNL (Figure 3.22(c)) for the proposed dual-

calibration. The dual-calibrated DAC achieves less reduction in INL but with an upward trend (Figure 3.22(d)).



(a) DNL (b) INL

(c) DNL improvement (d) INL improvement

Figure 3. 22. Comparison between calibration schemes in terms of (a) DNL, (b) INL and the (c) DNL and (d) INL improvement for different DAC resolutions and 20% mismatch error

In I/O systems, the calibration of these DACs occurs not only during startup but also during idle modes of I/O to track any temperature variations. Hence, it is important to consider the overhead of complex calibration algorithms that come at a cost in power. In the proposed DAC, algorithmic complexity is linearly dependent on the number of unit cells compared to other

calibration techniques in which there is quadratic dependence as observed from Figure 3.23 (the slope is twice for other schemes compared to our proposed method).

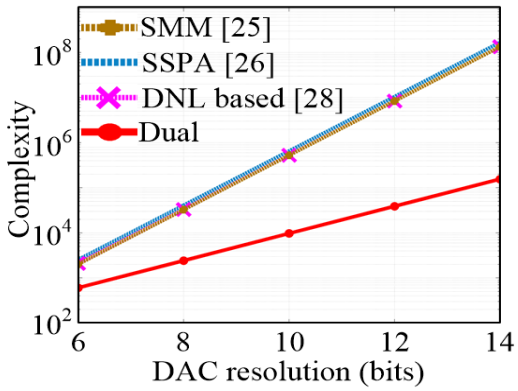
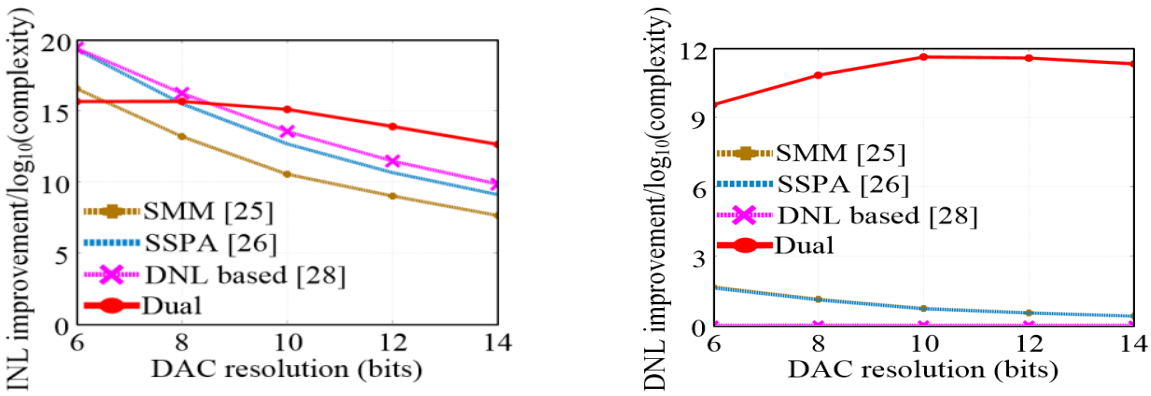


Figure 3. 23. Comparison between calibration schemes in terms of algorithmic complexity for different DAC resolutions and 20% mismatch error

Even the complete-folding algorithm in [27], which shows simulated results, has a complexity of $O(n^2)$. The reduced complexity of the proposed dual-calibration technique lies in the fact that the two schemes of the dual-calibration are applied on the columns and the rows separately instead of considering all n elements of the DAC together. This significantly reduces the number of elements to be processed by each method and hence the complexity. As complexity refers to the number of steps required to compute the algorithm, reducing it equates directly to less time and power required for calibration. Hence, we believe a better figure of merit to compare different algorithms for our target application is to normalize the improvement obtained with respect to the order of computation steps (Figure 3.23) as shown in Figure 3.24. The reason behind choosing this particular figure of merit is the approximate exponential nature of the INL for different DAC resolutions (Figure 3.22(b)). Therefore, the INL improvement curve also has an exponential nature (it follows the curve of $1 - e^{-x}$ function). As seen from Figure 3.24(a), the dual-calibrated DAC results in better performance with respect to other techniques. From

Figure 3.22, we know the performance of dual-calibrated DAC is better compared to others with respect to DNL, but for completeness Figure 3.24(b) shows improvement in DNL using the above figure of merit.



(a) INL improvement normalized with algorithmic complexity

(b) DNL improvement normalized with algorithmic complexity

Figure 3. 24. Comparison between calibration schemes in terms of (a) INL and (b) DNL improvement normalized with algorithmic complexity for different DAC resolutions and 20% mismatch error

We also observe from Figure 3.22(d) that if the dual-calibration scheme is applied element wise, instead of row-wise to the DAC, it results in better INL reduction (similar performance as the switching schemes in ([26], [28]), but at the expense of algorithmic complexity which now increases to $O(n^2)$.

In our design, 1-bit SRAM is required for each unit cell (including 12.5% of outliers) along with N/2-bit SRAM for storing rank of each row. So a total of $2^N \cdot (1.125) + (N/2) \cdot 2^{N/2}$ memory cells are needed. For other schemes, an N-bit SRAM is associated with each unit cell to store its rank within the DAC since they consider all unit cells together. So a total of $N \cdot (2^N - 1)$

memory cells are required. This results in at least an order of magnitude more memory overhead compared to our method (Figure 3.25).

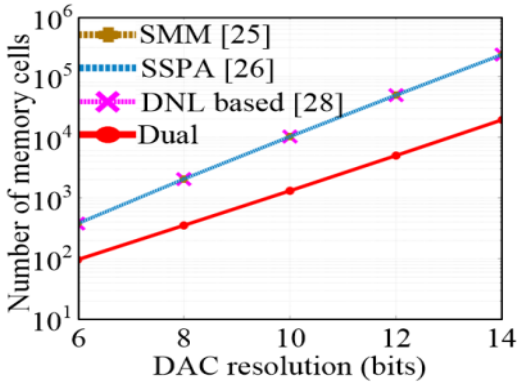
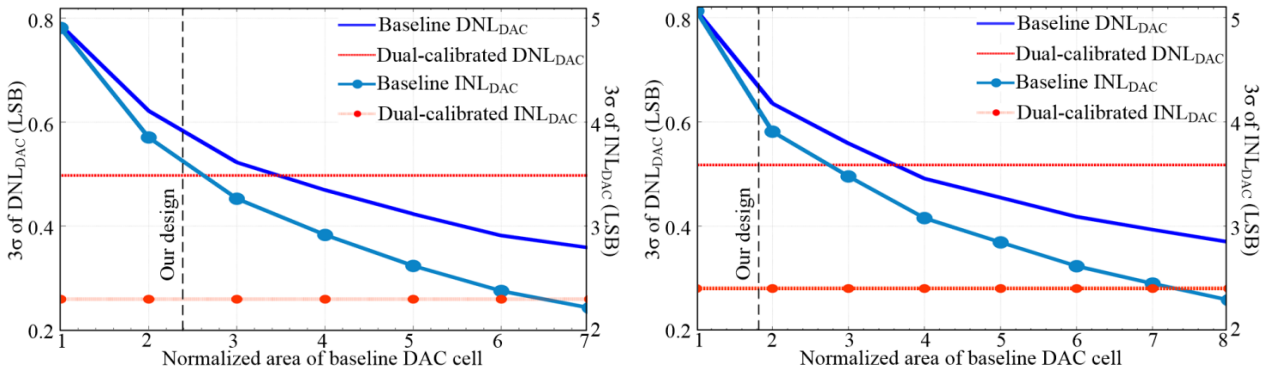


Figure 3. 25. Comparison between calibration schemes in terms of memory area overhead for different DAC resolutions and 20% mismatch error

Hence, we conclude, that for applications of DACs in calibration of I/O circuits such as phase interpolators, where complexity and area overhead of DAC's calibration is important, our technique results in a better performance tradeoffs compared to other schemes.

3.7 Scaling of area overhead

To estimate the hardware overhead of the dual calibration, consider the 8-bit thermometer DAC with 2 outliers per row. For a fair comparison, we normalize the area of the dual-calibrated DAC including the overhead due to the redundant unit cells, extra switches and SRAMs, to the area of a non-calibrated or baseline DAC.



(a) TSMC 65nm CMOS process (b) TSMC 45nm CMOS process

Figure 3. 26. Comparison of area of a single DAC cell with respect to DNL and INL across technology nodes

Based upon simulations of a baseline DAC, we find that for the same power consumption, the non-calibrated DAC's unit cell needs to be 1.5 and 2.6 times larger than that of the dual-calibrated DAC to achieve the same 3σ of DNL_{DAC} and INL_{DAC}, respectively as shown in Figure 3.22(a). To visualize how the proposed technique will perform as technology scales, we obtained a similar area overhead plot in TSMC 45nm CMOS process as shown in Figure 3.22(b). The additional components required by the dual-calibration scheme like the SRAM scale better with process unlike the analog components. As a result, the size of the current source and hence the unit cell must be increased to achieve similar mismatch profile in 45nm as that in 65nm. From Figure 3.22(b) we observe that for the same power consumption, the non-calibrated DAC's unit cell now needs to be 2 and 4 times larger than that of the dual-calibrated DAC to achieve the same 3σ of DNL_{DAC} and INL_{DAC}, respectively. The dual-calibration technique therefore systematically reduces the area penalty required to contain mismatch errors that cause static non-linearity.

CHAPTER 4

MODELING OF HIGH SPEED I/O LINKS

4.1 Introduction to chapter

This chapter discusses one of the potential applications of the proposed dual-calibrated DAC. In high speed I/O links, various types of DACs are used to serve different purposes. Many times the correct functioning of some of the circuits of I/O links strongly depends on the accuracy of these DACs. Hence, as the precision of the DACs degrade in the presence of process variation and device mismatch, the correctness of the circuit blocks in I/O also reduce. This leads to reduction in overall performance of the link.

In this chapter, we first start with a general description of the high speed I/O architecture and the related circuit and channel issues as we increase the data rate of signals, followed by how DACs can help mitigate some of the circuit related issues. In section 4.3 we describe the different I/O circuit blocks where DACs are used along with how the performance of these circuit blocks depend on the linearity of the DAC, with section 4.3.1 concentrating specifically on one of the critical blocks of the high speed I/O – the phase interpolator. In Section 4.4 we discuss the implementation details of the modeling of an I/O link in MATLAB to observe how the linearity of DACs impacts the overall performance. Lastly, we conclude the chapter by comparing the simulation results of using the dual-calibrated DAC in the phase interpolator against that of using a baseline DAC, in the presence of random device mismatches.

4.2 High speed I/O transceivers

A typical high speed I/O link is given in Figure 4.1.

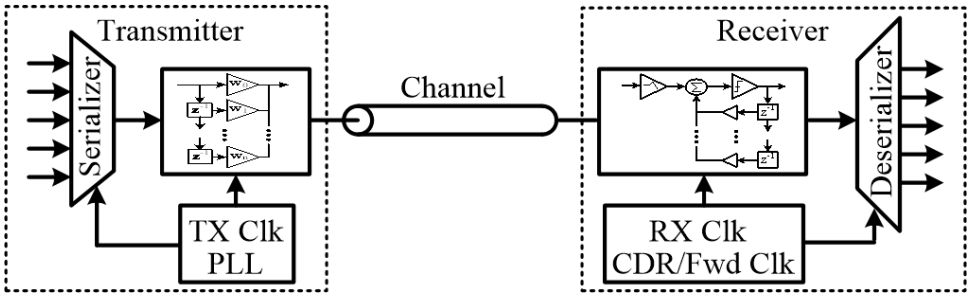


Figure 4. 1. High speed serial I/O link

It consists of a transmitter, a channel and a receiver. The transmitter converts the digital binary data into analog data and sends it across the channel. The channel is the medium of communication between the transmitter and the receiver, which can be the free space for wireless communications or traces on a printed circuit board (PCB) that connect different components in a backplane system as shown in Figure 4.2.

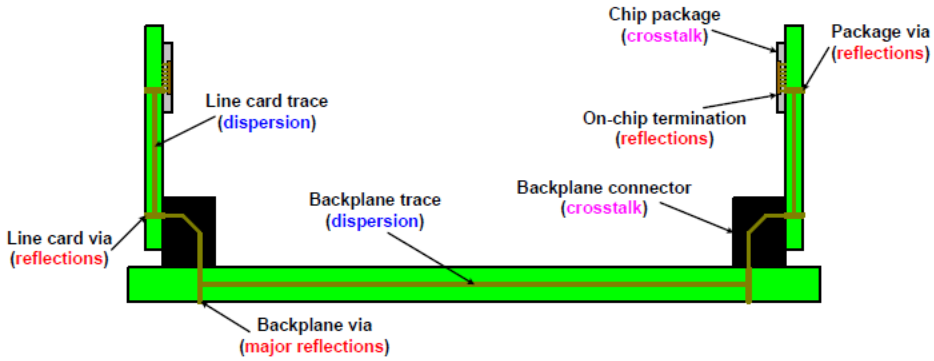


Figure 4. 2. Backplane link

The receiver receives the incoming analog waveform and converts it back to digital binary data. For this conversion, the receiver requires the optimal timing instants to sample the incoming

signal. There are various I/O clocking schemes [41] to determine these timing instants. Following are the broad categories of the different clocking schemes:

i. Common clock:

   There is a synchronized global clock for the transmitter and the receiver.

ii. Forwarded clock:

   The transmitter sends the data along with a strobe, which is another clock. Both the transmitted data and the strobe are driven by the same bus clock.

iii. Embedded clock:

   The clock to determine the sampling instants is embedded within the transmitted data. The receiver requires a timing recovery circuit block to recover this embedded clock.

With increasing data rates, both the circuit and channel related issues emerge. As the bit-period shrinks due to high data rates, issues such as transmitter and receiver bandwidth along with clock jitter limit the overall performance of the I/O link. Increased process variation with smaller feature sizes also degrades the overall performance. The channel too starts to behave as a lossy transmission line due to skin effect and dielectric loss, which become prominent in high frequency regime. Frequency response of a typical channel is shown in Figure 4.3. As we can observe, for data rates of more 10 Gbps we get more than 15dB of attenuation through the channel.

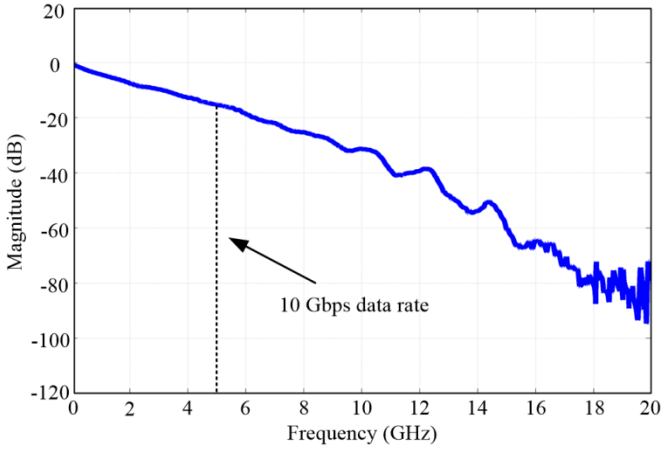


Figure 4. 3. Frequency response of channel (25" FR408 Through Backplane channel - backdrilled with moderate crosstalk)

All of the above factors lead to spreading of adjacent bits over each other resulting in inter-symbol interference (ISI). The deterioration of the signal due to ISI reduces both the voltage and timing margin of the signal. We can see from Figure 4.4 the gradual closing of the eye of the received signal with increasing data rate due to increase in ISI.

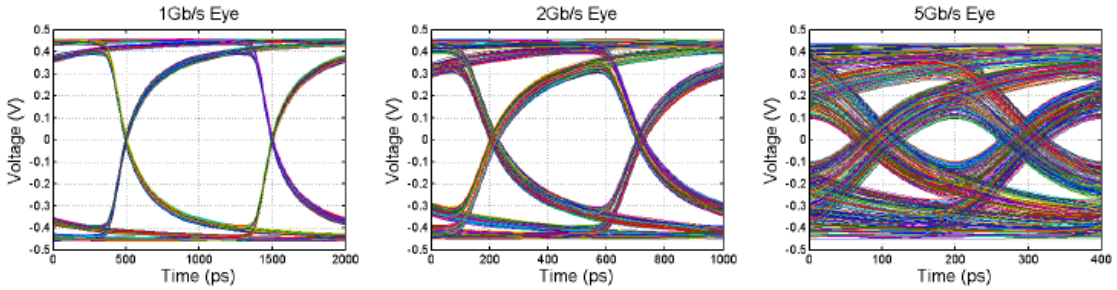


Figure 4. 4. Effect of ISI on the eye-diagram of the received signal with increasing data rate [42]

This decrease in the voltage and timing margin results in increased bit error rate (BER) at the receiver side. Various techniques are utilized to reduce the BER, both on the transmitter (pre-emphasis) and on the receiver (equalization) end to combat the channel related issues. The presence of process variation and devices mismatches further deteriorate the performance of the

I/O links. Hence, accurate tap weights for the equalization techniques, offset compensation and tunable bias currents are required for many of the circuit blocks in I/O. Current steering thermometer DACs are ideal candidates to carry out such type of calibration.

4.3 DACs in high speed I/O links

Many high speed I/O transceiver designs have been published in the literature. Figure 4.5 shows one of them.

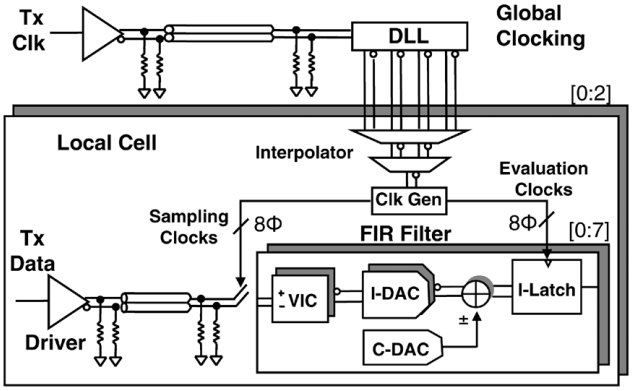


Figure 4. 5. High speed I/O transceiver [39]

DACs (mostly current steering DACs) are generally used for providing some sort of corrections as seen from Figure 4.5, where the I-DAC provides the tap weights for the FIR filter and the C-DAC provides the offset current for compensation due to device mismatches. Other examples where current steering DACs provide tap coefficients are given in [43], [44]. DACs are also used for providing offset compensation to linear equalizers [45]. Figure 4.6 shows an example where current steering DACs are used to tackle offset problem in both equalizer and the sampler blocks in the receiver.

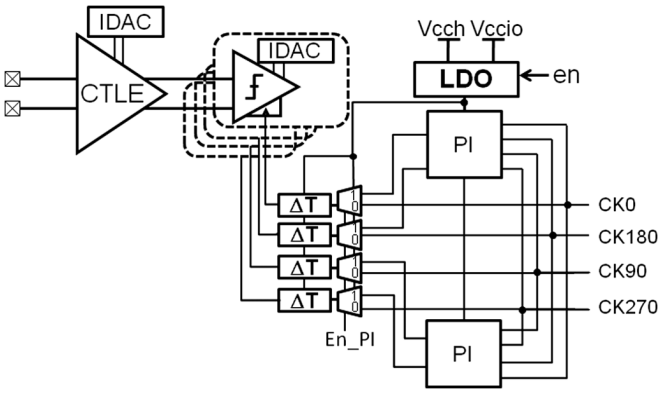


Figure 4. 6. High speed I/O transceiver utilizing DAC for offset compensation [46]

Another example of offset removal by DACs in the receiver's sampler is given in [47]. DACs are also used in high speed I/O as a driver at the transmitter end [38], [48] of the link.

Sometimes DACs are used to provide accurate reference or biasing to a stage like the phase rotator block in the receiver [47]. For example, Figure 4.7 shows a couple of 5-bit DACs used to provide programmable delay in an oscillator delay stage which can be tuned to correct for device mismatch and process variation.

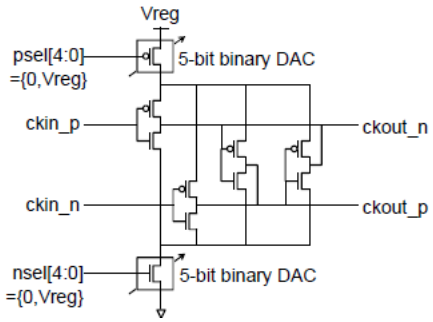


Figure 4. 7. Programmable delay by using DAC [49]

4.3.1 Effect of DAC on the linearity of Phase interpolator (PI)

One of the critical blocks of an I/O is the phase interpolator (PI). It takes the recovered clock from the clock and data recovery (CDR) circuit block and interpolates it such that the receiver's sampler samples the received data at the correct instant of time. DACs are used to provide the required interpolation steps by controlling the bias currents in the PI circuit as given in [50] or as shown in Figure 4.8.

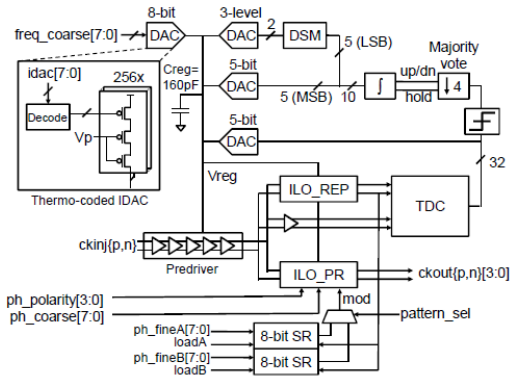


Figure 4. 8. An 8-bit DAC controlling the coarse interpolation steps of the PI [49]

Random and systematic variations make the PI nonlinear [46]. These nonlinearities in the PI circuit block may results in incorrect sampling of the received data leading to increased BER. To understand the causes for these nonlinearities, let's consider the schematic of the PI circuit given in Figure 4.9.

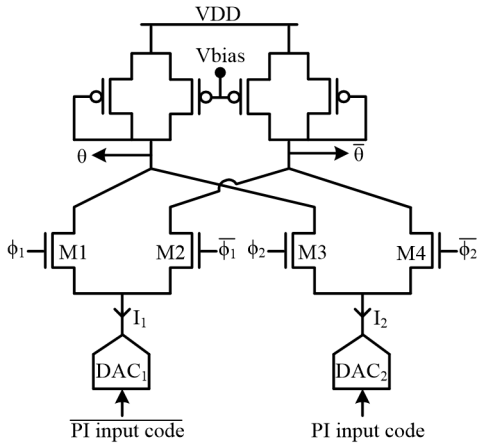


Figure 4. 9. PI circuit

The DACs provides the tail currents for the PI block. The PI interpolates between the two input signals to produce an output with a phase which is the weighted sum of the phases of the input signals. Suppose, the inputs have phases equal to ϕ_1 and ϕ_2. Then, for a digital input code k, the phase of the output signal of the PI, $\Theta(k)$ is given by

$$\Theta(k) = \frac{I_1(n-k)}{I_1(n-k)+I_2(k)}\phi_1 + \frac{I_2(k)}{I_1(n-k)+I_2(k)}\phi_2 \tag{4.1}$$

Here I_1 and I_2 are the currents provided by the two DACs and n is the total number of unit cells in each DAC. The mismatch in the input transistors, M1-M4 can be reduced by making them large or by layout techniques. The other major contributor to PI non-linearity is the linearity of the DACs. If the DACs are non-linear, it negatively impacts the PI performance. To determine the effect of DAC non-linearity on the PI, we find the DNL and INL of the PI in terms of σ_ε (mismatch error in the unit cells of the DAC). The DNL and INL of the PI for an input code k is given as

$$DNL_\Theta(k) = \frac{\Theta(k)-\Theta(k-1)}{(\phi_2-\phi_1)/n} - 1 \tag{4.2}$$

$$INL_{\Theta}(k) = \frac{\Theta(k) - \phi_1}{(\phi_2 - \phi_1)/n} - k \tag{4.3}$$

First, let's consider the case when only DAC_1 is non-ideal and DAC_2 is ideal, i.e., DAC_2 has no mismatch errors amongst its cells. Then the PI's DNL and its variance is given as

$$DNL_{\Theta}(k) = \left(\frac{k-1}{n}\right)\varepsilon_{n-k+1,1} \tag{4.4}$$

$$\sigma^2_{DNL_{\Theta}}(k) = \sigma^2_{\varepsilon}\left(\frac{(k-1)^2}{n^2}\right) \tag{4.5}$$

Here, $\varepsilon_{j,1}$ is the mismatch error of the j^{th} unit cell of DAC_1. Similarly, the PI's INL and its variance is given by

$$INL_{\Theta}(k) = \frac{k}{n}\sum_{i=1}^{n-k}\varepsilon_{i,1} \tag{4.6}$$

$$\sigma^2_{INL_{\Theta}}(k) = \sigma^2_{\varepsilon}\left(\frac{k^2}{n^2}(n-k)\right) \tag{4.7}$$

For the reverse case when DAC_1 is an ideal DAC and DAC_2 is a non-ideal DAC with mismatch errors, the DNL and INL of the PI and their variances are given by

$$DNL_{\Theta}(k) = \left(\frac{n-k}{n}\right)\varepsilon_{k,2} \tag{4.8}$$

$$\sigma^2_{DNL_{\Theta}}(k) = \sigma^2_{\varepsilon}\left(\frac{(n-k)^2}{n^2}\right) \tag{4.9}$$

$$INL_{\Theta}(k) = \frac{(n-k)}{n}\sum_{i=1}^{k}\varepsilon_{i,2} \tag{4.10}$$

$$\sigma^2_{INL_\Theta}(k) = \sigma^2_\varepsilon \left(k \frac{(n-k)^2}{n^2} \right) \tag{4.11}$$

Lastly, we consider the case where both the DACs are non-ideal and assume that the mismatch errors in both DACs are random, uncorrelated and follow $\sim N(0, \sigma^2_\varepsilon)$. The standard deviation of the DNL and INL of the PI in this scenario is given as

$$\sigma_{DNL_\Theta}(k) = (\sigma_\varepsilon / n)\sqrt{(k-1)^2 + (n-k)^2} \tag{4.12}$$

$$\sigma_{INL_\Theta}(k) = \sigma_\varepsilon \sqrt{k(n-k)/n} \tag{4.13}$$

Figure 4.10 and Figure 4.11 show the plot of the standard deviation of PI's DNL and INL, respectively across all codes for DAC having resolution of 8 bits.

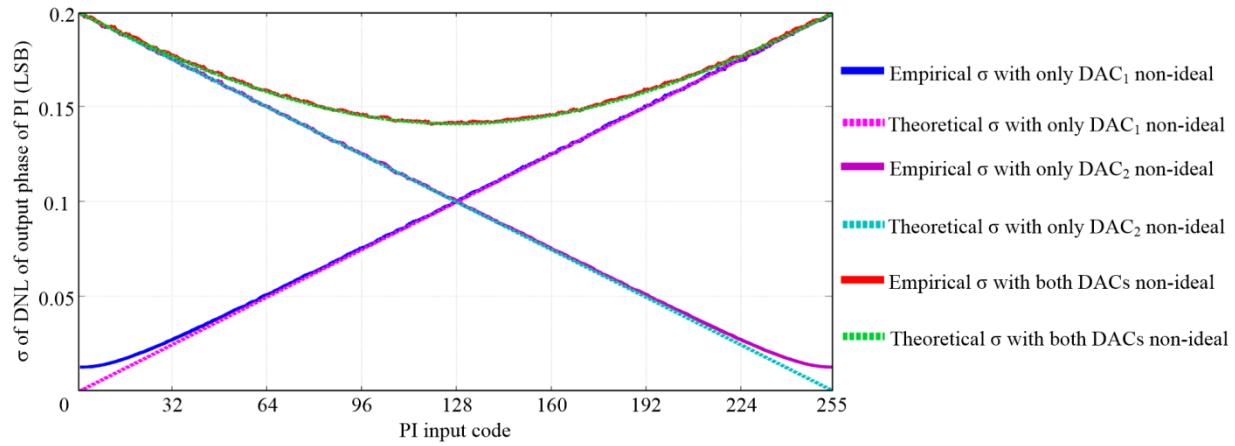


Figure 4. 10. DNL of PI

As observed from both the plots, the theoretical values of the standard deviation of DNL and INL match well with empirical results through Monte Carlo simulations.

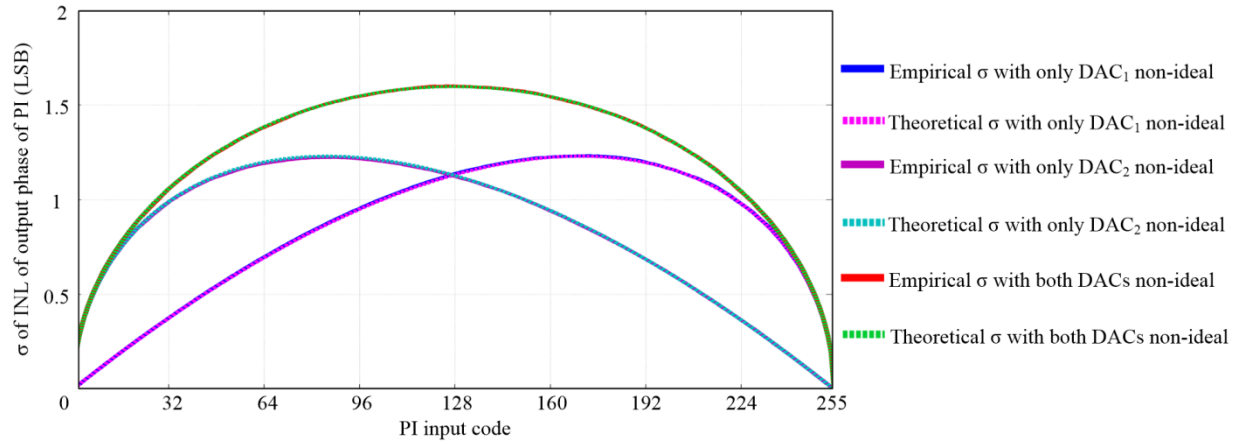


Figure 4. 11. INL of PI

4.4 Modeling of high speed I/O

As discussed in the previous section, DACs are used in various circuit blocks of high speed I/O for providing accurate biases or references which can be used as tap coefficients, for offset calibration or as phase interpolation steps. To obtain finer resolution of the phase interpolation steps, higher resolution static DACs need to be used. But high resolution intrinsic DACs suffer from increased variation as discussed in chapter 1 and 2. This increased variation in turn affects the linearity of the PI as shown in section 4.3.1. Therefore, there exists a tradeoff between the resolution and the variation or power or area [49]. We observe that the proposed dual-calibrated DAC is an ideal candidate for this situation where we require higher resolution DAC with improved static linearity without much power or area overhead.

To observe the effects of using the dual-calibrated DAC to improve the resolution accuracy of PI circuit block, we modeled an I/O link in MATLAB. We developed the I/O model for a data rate of 10 Gbps. We assumed ideal transmission from the transmitter end of the I/O chain. The

transmitter was modeled with a random binary number generator. To imitate real situation where data has non-zero rise and fall time, the number generator was followed by a buffer which modified the rise and fall time to 20ps. The rest of this section discusses the implementation details of receiver model and the following section show the simulations results.

4.4.1 Channel model

The channel response shown in Figure 4.3 was used for the channel model. We used rational fitting with 248 poles to accurately represent the channel response. As seen from Figure 4.12, the fitted model represents the channel response reasonably well in the frequency band of interest. The deviation between the actual response and the model is only visible in frequencies greater than 15 GHz. The transfer function obtained from rational fitting is then incorporated in our MATLAB I/O model.

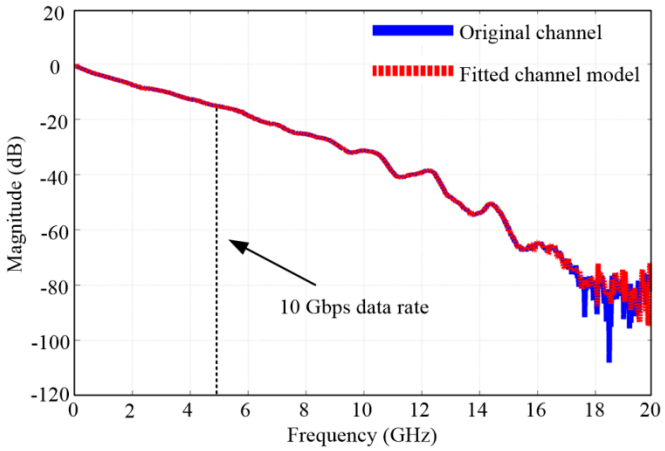
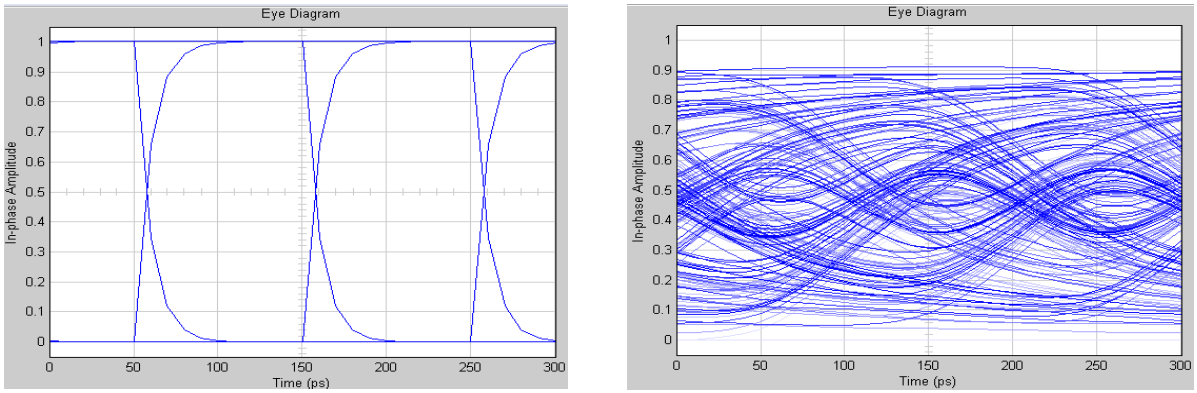


Figure 4. 12. Channel model

Figure 4.13 shows the eye diagrams of the transmitted signal and of the received data at the front end of the receiver chain after the channel. Since the channel attenuates the signal by 18 dB at

5GHz (10 Gpbs data rate), the receiver front end sees almost a closed eye as seen from Figure 4.13(b).



(a) Transmitted signal (b) Signal after channel

Figure 4. 13. Eye diagrams of transmitted and receiver front end signal

4.4.2 Equalizer model

Since the received eye is almost closed after the channel, equalization is required. The goal of equalization is to flatten the frequency response of the system out to the Nyquist frequency to remove the time-domain ISI. It can be done either on transmitter or receiver end or both. As observed from Figure 4.3, the channel attenuates the high frequency component of the transmitted signal. This in turn leads to degradation of the transitions within the signal. To boost the high frequency components of the signal, pre-emphasis is used at the transmitter end before the signal is sent across the channel [43]. Figure 4.14 shows how emphasizing the transitions (high frequency component of the signal) and de-emphasizing no transition region (low frequency) of the transmitted signal can improve the signal quality after the channel attenuation.

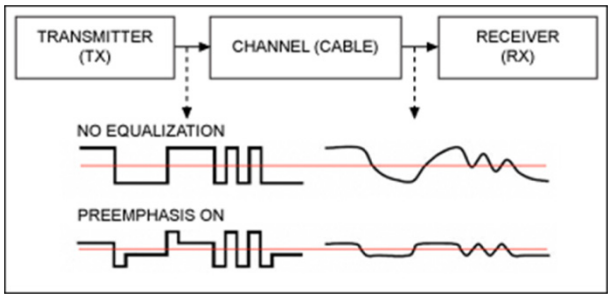


Figure 4. 14. Pre-emphasis in time domain [51]

Pre-emphasis can be implemented simply using a 2-tap finite impulse response (FIR) filter as shown in Figure 4.15 or by more complex FIR filters having more taps as given in [52].

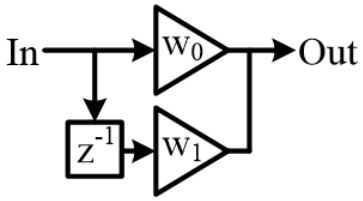


Figure 4. 15. Simple 2-tap pre-emphasis implementation

By utilizing pre-emphasis at the transmitter, ideally a flat system response, i.e., uniform attenuation can be obtained within the desired frequency bandwidth. This results in significant reduction in ISI and opening of the received eye as shown in Figure 4.16.

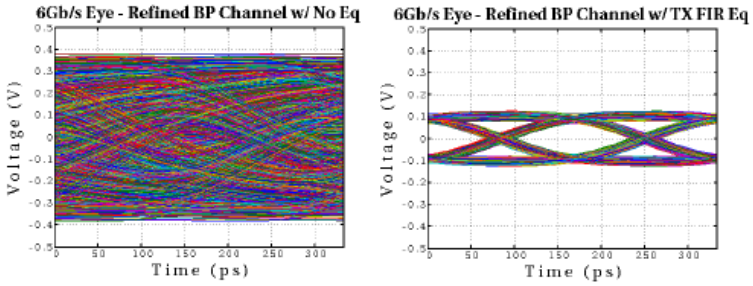


Figure 4. 16. Effect of pre-emphasis on received signal's eye-diagram [42]

Though pre-emphasis does not amplify noise, it does attenuate the low frequency content of the signal. Also, a "back-channel" is required to tune the tap coefficients ([53], [54]) since the channel is not usually known a priori.

Unlike pre-emphasis filtering, equalization at the receiver does not attenuate the low frequency content and no "back-channel" is required to tune the equalizer coefficients. There are mainly the following three ways to carry out this:

i. Receiver FIR

ii. Continuous/Discrete time linear equalizer (CTLE/DTLE)

iii. Decision feedback equalizer (DFE)

Figure 4.17 gives a typical implementation of the receiver FIR. The precision of the filter taps is important and they can be adaptively tuned. One of the major challenges faced by any receiver FIR implementation is the design of the analog delay cells [55].

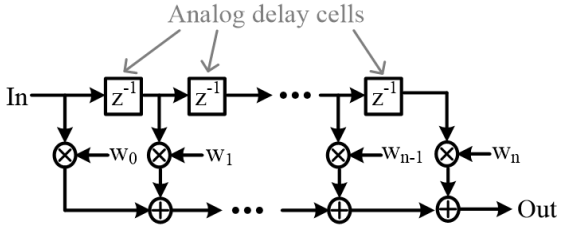


Figure 4. 17. Receiver FIR implementation

The receiver FIR equalization can be shifted to digital domain to make use of digital delay cells which are easier to implement. But the received signal, which is analog in nature, needs to be converted into a digital signal [56]. This requires the use of fast ADCs leading to high power consumption [57].

Another technique of equalization is to use linear equalizers (LE) at the receiver. DTLE are designed using digital filters. Compared to DTLE, CTLE are gaining attention in terms of noise and jitter. They also provide gain along with equalization with low area and power overhead. CTLE can have either passive structure [56] or can be combined with an amplifier to provide gain as shown in Figure 4.18.

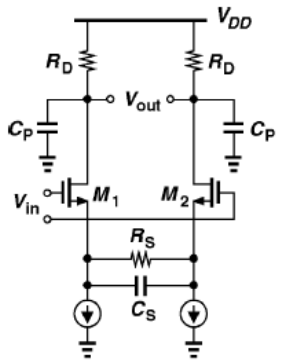


Figure 4. 18. Active CTLE [58]

To achieve the required voltage and timing margin at the receiver, tuning of CTLE may be required. There are number of ways to adaptively tune the CTLE response like measurement of the high and low frequency spectrum content of random data [59], measurement of the high and low frequency average amplitude of the output [60], or the monitoring of the data edge distribution [61].

Even though significant eye opening can be obtained using active CTLE as shown in Figure 4.19, they are sensitive to process, voltage, temperature (PVT) variations and are generally limited to 1st order compensation.

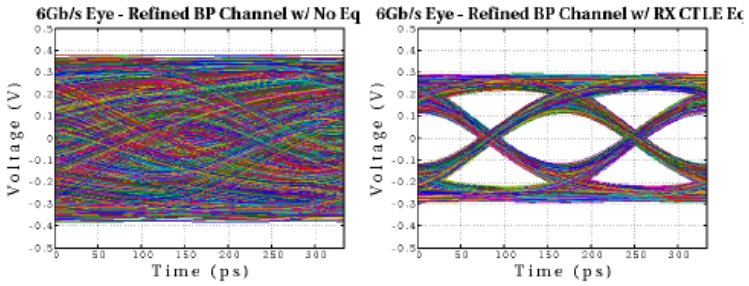


Figure 4. 19. Effect of equalization by implementing active CTLE [42]

DFE is a non-linear filter which overcomes some of the problems associated with the linear equalizers. It uses a linear combination of the past decisions made by the slicer at the receiver, as shown in Figure 4.20, to compensate for the loss due to channel attenuation.

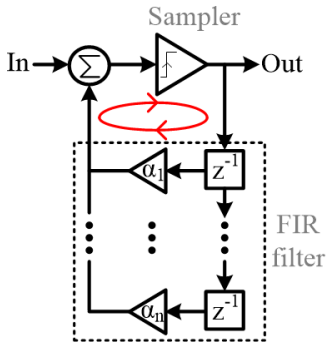


Figure 4. 20. Implementation of DFE with FIR filter feedback (feedback timing path in red)

The DFE implementation with *n*-tap FIR filter in feedback only cancels ISI due to the first *n* post-cursors. Therefore, many taps may be required to cancel any long-tail ISI. Some channels can be termed as "smooth" channels (not many reflections) like the ones associated with on-chip wires and silicon carrier wires. The long-tail ISI of these channels can be approximated as exponentially decaying. For such cases, IIR filter is used in the DFE feedback path [62].

Compensation by DFE does not lead to any noise and crosstalk amplification and significant eye opening can be obtained as shown in Figure 4.21. The filter taps can be tuned adaptively ([38], [63]) without the use of any "back-channel".

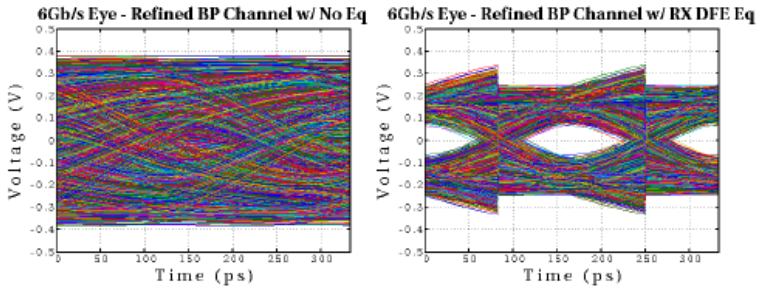


Figure 4. 21. Effect of DFE compensation on the eye diagram of the received data [42]

Although the DFE architecture is vulnerable to error propagation, the probability of error propagation is low in practical links having BER equal to 10^{-12}. Also since DFE uses only past decisions for equalization, it cannot cancel pre-cursor ISI (Figure 4.22).

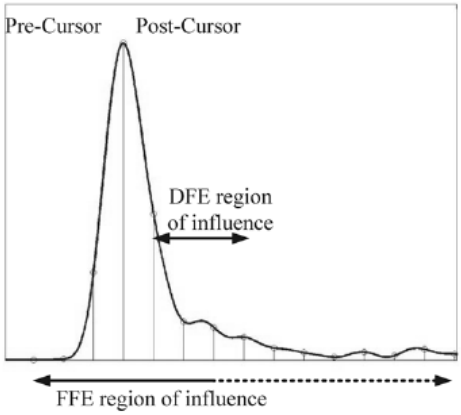


Figure 4. 22. ISI and region of influence of equalization methods [38]

The feedback timing path is one of the critical aspects for the DFE design. The delay of this path should be less than 1 unit interval (UI) and for higher data rates, this imposes stringent requirements on the design of the circuit blocks that lie on this path. More efficient DFE designs

like the half-rate DFE [38] or the loop-unrolling DFE [64] architectures relax this critical path timing requirement.

For our I/O model, we only implemented receiver equalization. A two pole, single zero active CTLE was modeled based on the design shown in Figure 4.18. The zero compensates for the loss due to the channel and opens the eye. The real poles ensure that there is no gain boosting beyond a certain frequency (the signal bandwidth given by the second pole, ω_{p2} of the CTLE) as any amplification beyond signal bandwidth merely amplifies more high frequency noise. The gain boosting is given by ([58])

$$gain\ boosting = A_0 \frac{\omega_{p1}}{\omega_z} \tag{4.14}$$

Here, A_0 is the DC gain, ω_{p1} is the location of the first pole and ω_z is the location of the zero. As seen from (4.14), if the signal loss is low then ω_{p1} and ω_z can be close. But if the loss due to the channel is high then the first pole should be further apart from the zero to achieve significant gain boosting. As a one-pole approximation of the channel, the zero is positioned close to the frequency where the channel response shows 3dB attenuation. Keeping all these constraints in mind, in our model of the CTLE the zero was located at 1 GHz, the first pole at 5.5 GHz and the second pole at 7 GHz.

Figure 4.23 shows the opening of the eye of the equalized signal. Since significant eye opening was achieved through our model with linear equalizer, model for the DFE circuit block was not used.

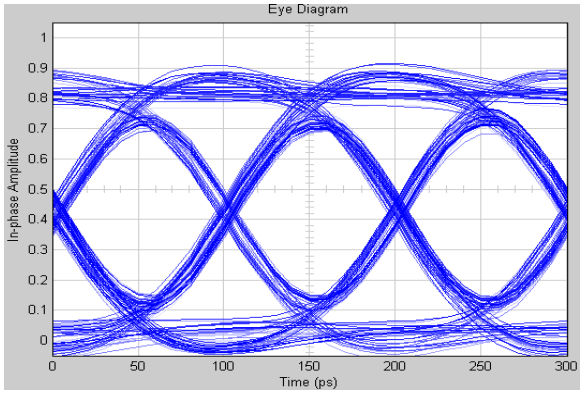


Figure 4. 23. Eye diagram of equalized signal

4.4.3 Sampler model

The receiver's sampler was modeled as a simple threshold block. Since the output of the threshold block had a zero rise and fall time, a buffer similar to the one used in the transmitter side was used to obtain a 20ps rise and fall time. Till this point, every block in the receiver chain of our model was noiseless. But this was too ideal. The sampler itself adds switching noise [65]. Hence, to model this noise, random Gaussian noise was added to the buffered sampler's output to represent the real case more closely. Figure 4.24 shows the eye diagram of the output from this noisy sampler.

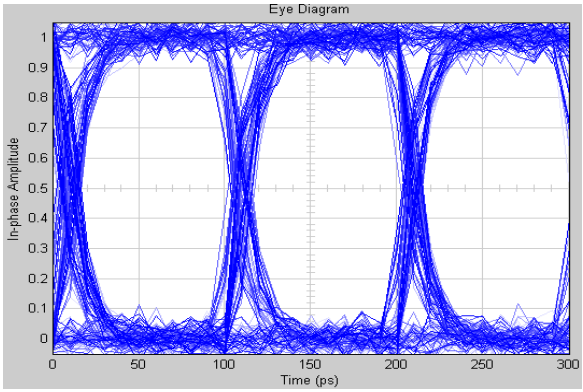


Figure 4. 24. Eye diagram of output signal from the noisy sampler

4.4.4 Complete receiver model with BER test setup

The complete MATLAB model of the receiver chain is shown in Figure 4.25 with the different blocks of the model clearly marked.

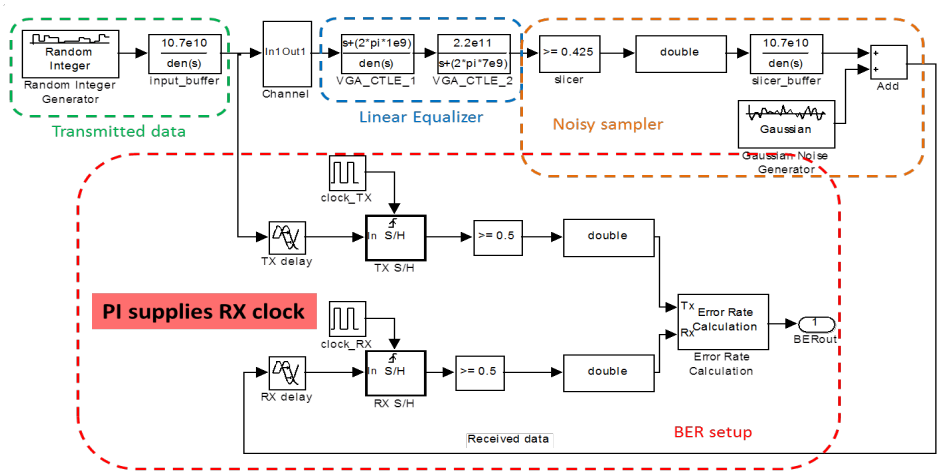


Figure 4. 25. MATLAB model of I/O receiver

To observe the effect of PI's non-linearity due to the non-linearity of the DAC on the overall performance of the link, we took the BER measurement at the output. For the BER measurement, we needed to compare the corrected received data with the transmitted data. But the receiver chain introduces some delay. Hence, we delayed the transmitter data such that it matches the delay in the receiver chain. The clock to sample the transmitter data and the receiver data were kept the same except for the phase associated with the receiver clock. The PI block provided the clock for the sampling in the receiver of high speed I/O. Therefore, in our model we modified the phase of the receiver clock according to (4.1) to represent the effect of PI's linearity on the BER performance.

In high speed I/O, the data is usually divided into odd and even parts.

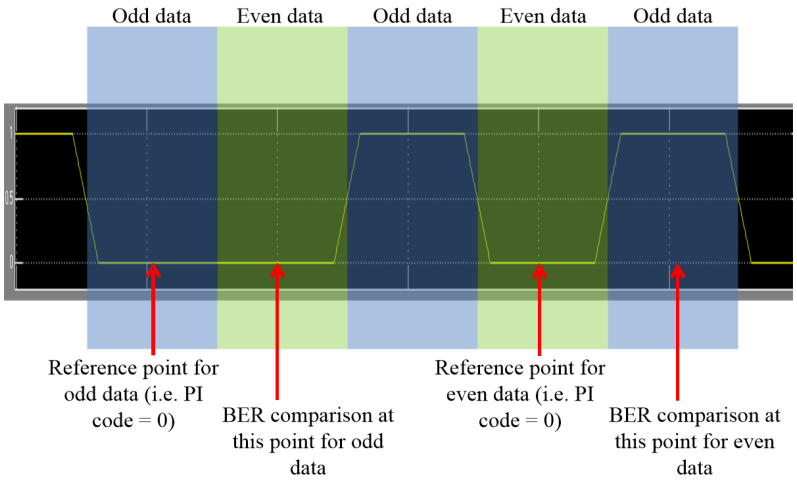


Figure 4. 26. Odd and even data sampling and BER measuring time instants

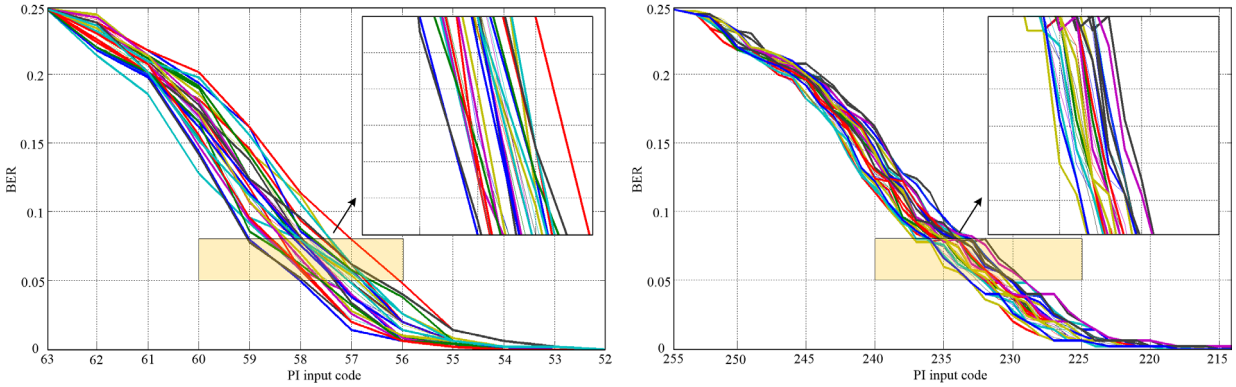
Hence, as seen from Figure 4.26, the odd (even) data was sampled during the first (second) half of the clock period and the BER was calculated during the second (first) half of the clock period.

4.5 Simulation results

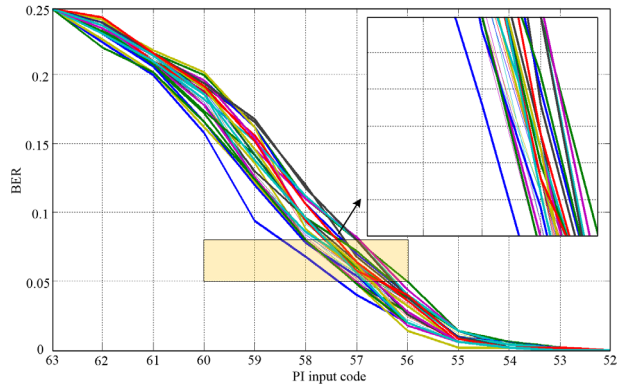
Using our MATLAB model of the I/O, we carried out the BER measurements for the data rate of 10 Gbps. To obtain the bathtub curve for the BER, we started with center of the received signal's eye and then increased the digital input of the DAC in the PI to move towards the edge of the eye. By controlling the sign of the phase of the receiver clock, movement towards both edges of the eye was possible. Each input code corresponded to a sampling instant at which we calculated the BER value. By plotting these BER values against the digital input code, the bathtub curve was obtained. This procedure of obtaining BER curve was performed twice - first for the baseline DAC case where there was 20% current source mismatch between the unit cells and second for the dual-calibrated DAC where this mismatch between the unit cells was reduced by our proposed calibration technique. In the interest of time and resources, we considered only 500

samples of random binary transmitted data. Also, only one side of the BER curve is shown in this section to clearly demonstrate the performance improvement.

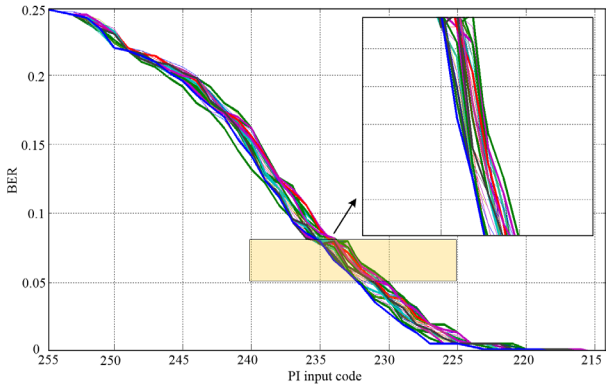
We first carried out the experiment of comparing different resolutions of the DAC on the performance of the I/O link. As we can see from Figure 4.27, the variation in the BER curve is lesser for an 8-bit DAC than a 6-bit DAC. This can be attributed to the fact that finer resolution is achieved through the 8-bit DAC. We also observe that the dual-calibrated DAC reduces the variation in both cases. For fair comparison, same amount of redundancy overhead was kept for both the resolutions of the DAC. In other words, the redundancy ratio within each row was equal to 12.5%.



(a) 6-bit baseline DAC (b) 8-bit baseline DAC



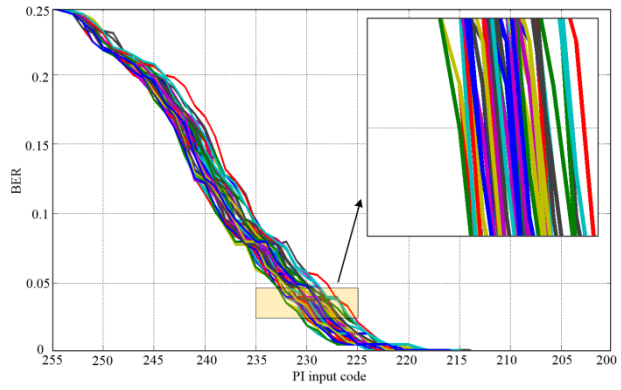
(c) 6-bit dual-calibrated DAC



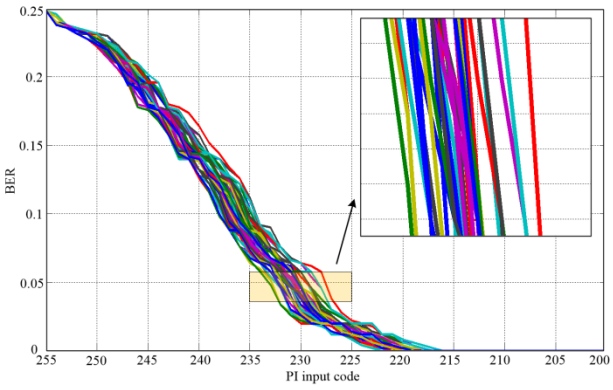
(d) 8-bit dual-calibrated DAC

Figure 4. 27. Performance comparison for 6-bit and 8-bit DACs

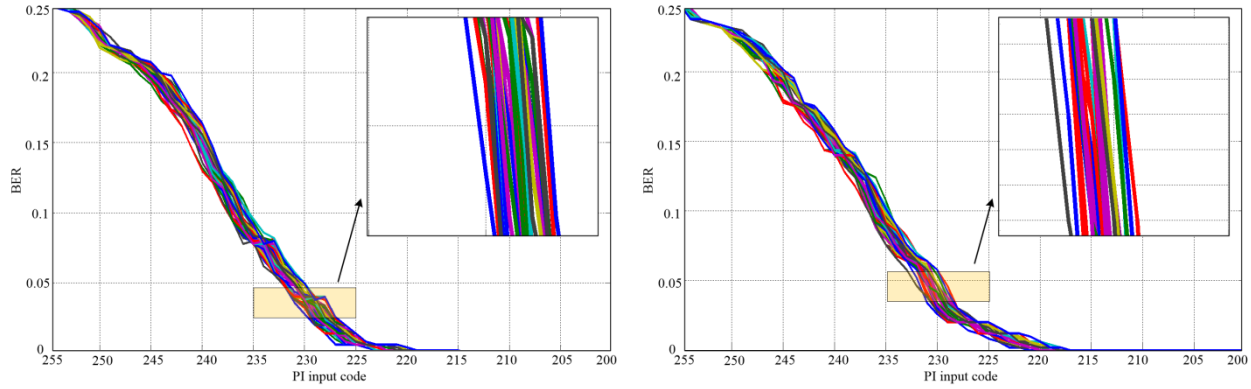
We next looked at how the performance changes for different swings of the transmitted data. Sometimes the data is transmitted with lower swing that the available full-scale to save power. For this experiment, we changed the swing of the transmitted data to 300mV from 1V. We also had to adjust the sampler setting to account for the lower swing of the data. We got similar performance improvement in this case of lower swing as seen from Figure 4.28.



(a) 8-bit baseline DAC full 1V swing



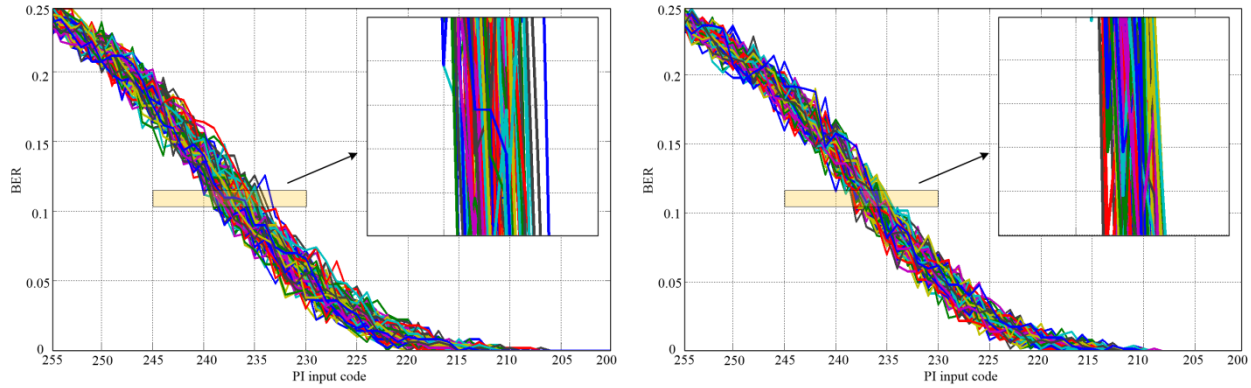
(b) 8-bit baseline DAC 300mV swing



(c) 8-bit dual-calibrated DAC full 1V swing (d) 8-bit dual-calibrated DAC 300mV swing

Figure 4. 28. Performance comparison with different transmitted data swing

Lastly, we looked at the performance of the dual-calibrated DAC in the presence of clock jitter. We see from Figure 4.29 that even in the presence of clock jitter of around 2 ps, the dual-calibrated results in a better performance than the baseline DAC.



(a) 8-bit baseline DAC (b) 8-bit dual-calibrated DAC

Figure 4. 29. Performance comparison in presence of clock jitter

CHAPTER 5

CONCLUSION

5.1 Summary

Analog subsystems in high performance I/O are fabricated alongside high performance digital processors that rely on scaled CMOS processes. The impact of process variation on these analog blocks is even more pronounced than on the digital components, which raises the need for accurate calibration circuits for the blocks in these systems. Current-steering thermometer DACs are used as simple and compact calibration tools in many such high speed I/O systems. In these applications it is undesirable to use large and complex DACs since both area and power are constrained. With the scaling of CMOS processes and availability of smaller feature sizes, the overall area of circuits is decreasing. But for a given process the matching of the unit cells in a thermometer DAC is inversely proportional to their area and the matching accuracy does not scale with process. Due to this the overall static linearity of the DAC is affected. But good static linearity is crucial for the DAC to be used as a calibration tool. Hence, we are not able to fully utilize the benefits of smaller transistor sizes. So to improve the matching of these unit cells in the presence of random mismatches (which are more dominant for smaller feature sizes), a calibration scheme is required with low overhead of area, power and complexity.

In this work, we propose a new dual-calibration technique for thermometer DACs to reduce static non-linearity errors in thermometer DACs. This proposed dual-calibration technique combines both the schools of thought that exist for calibration of DACs – trimming of unit cells

and optimized addressing of unit cells – to arrive at a solution which targets both the critical parameters of the static linearity of DACs. This kind of combined optimization approach is missing from existing calibration techniques in literature which have a single focus only. We demonstrate the use of redundancy within rows to reduce mismatch between the DAC's unit elements and tighten the error distribution around the median – which is proved to be a good approximation of the mean. To minimize cumulative error and hence INL, we demonstrate element reordering which leads to cancellation of mismatch errors with successive addressing. One of the main advantage of the dual-calibration over other existing calibration techniques of similar nature lies in the fact that it takes advantage of the two-dimensional nature of the thermometer DAC. The other techniques take into account all the elements of the DAC together, i.e., considering the DAC as a one-dimensional array. This increases their algorithmic complexity. In contrast, the dual-calibration treats the columns and the rows separately. Thereby, we significantly reduce the number of elements to be processed by each method and hence the complexity. Reducing the complexity directly implies that less time and power is required for calibration.

The mathematical tools that we have developed demonstrate the relationship between redundancy, reordering and DAC linearity. Though we present our results for a given mismatch error and DAC size, the equations we derive hold true for any given size and element mismatch. One of the crucial parameters determining the yield is the variances of the DNL and the INL. Using the models described in this work, these important parameters can be found directly without computing a very large number of space and time consuming Monte Carlo runs. This decreases design turn-around time significantly and helps designers accurately model the performance of large systems early on in design. From the measurement of 16 chips of the dual-

calibrated 8-bit current steering DAC, we observe 36% DNL and 50% INL improvement which matches well with the Monte Carlo simulations as well as with the results of our developed theoretical models.

As the algorithmic complexity of the calibration scheme is critical for our target application of the DACs, we believe a good figure of merit to compare different DAC calibration schemes is to normalize the improvement achieved in linearity with the algorithmic complexity. Using this figure of merit, through simulations we observe that the dual-calibration technique results in better performance over other similar techniques. We also demonstrate the area benefit of the dual-calibration technique over the baseline case with no calibration and predict through simulations that this improvement will only get better as CMOS process technology scales down.

Lastly, we look at one of the potential applications of our dual-calibrated DAC – use for providing bias current for the PI block in I/O. We develop the linearity relation between the PI block and the DAC. Through Monte Carlo simulations of our MATLAB model of the I/O link, we observe that the BER performance is improved by using the dual-calibrated DAC over the baseline DAC in the presence of device mismatches.

5.2 Modular addressing

Though we achieve significant improvement in matching accuracy of the unit cells of the DAC because of the redundancy method with minimal hardware complexity, scalability of this technique does impose a few challenges, in terms of ease of implementation. As we increase the resolution (N) of the DAC, more unit cells are required and hence, the DAC's active core area

changes. Also, peripheral blocks controlling the DAC cells' memory need to be changed to incorporate the increase in number of cells. More importantly, to maintain the same amount of redundancy, number of outliers in each row need to be increased. Hence, the column selection decoder needs to be redesigned completely to accommodate the increase in the DAC unit cells, the number of outliers as well as the increase in the input thermometer code. In contrast, it is much easier to change the standard binary-to-thermometer decoder to accommodate the increase in resolution of the DAC. To overcome the challenges in scaling of the redundancy scheme of the dual-calibration, we propose a modular addressing scheme for the DAC with redundancy. The scheme combines the advantages of improved matching due to redundancy with ease of implementation of modular design for scaling. The following sub-sections give the design details followed by discussion of simulation results.

5.2.1 Implementation of modular addressing

The fundamental principle behind the modular addressing scheme is to make a high resolution (*Ntarget*) target-DAC from a single high accuracy low resolution (*N*) DAC with minimal hardware overhead and complexity. Figure 5.1 shows the architecture of the proposed modular DAC.

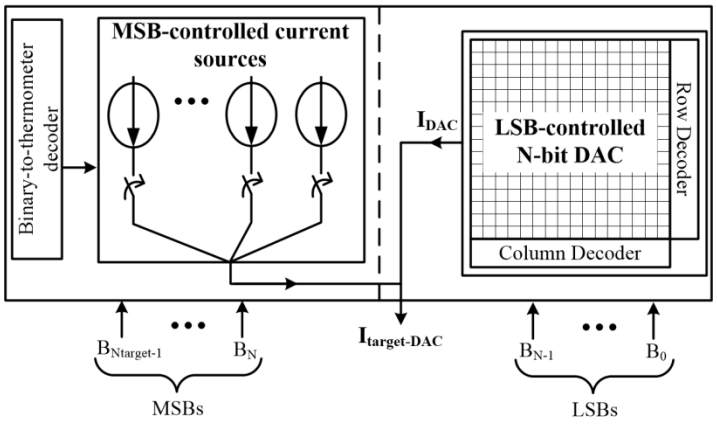


Figure 5. 1. Modular DAC architecture

We divide the desired number of the bits, *Ntarget* into 2 parts – *N* LSBs and rest as the most significant bits (MSBs). The single low resolution DAC equipped with redundancy is controlled by the *N* LSBs. The thermometer codes of the MSBs control the $2^{Ntarget-N} - 1$ current sources. Each current source is designed to carry a nominal current equal to the maximum current of the low resolution DAC. Though these current sources are relatively big so that they can carry larger current, they still suffer from process variation [7], which affects the overall accuracy of the high resolution target-DAC. Also, the maximum current of the low resolution DAC may change from one chip to another. Hence, these current sources are calibrated using a current comparator. The current comparator design used here is similar to the one used in median detection as discussed in section 3.4.2 and is again shown here in Figure 5.2.

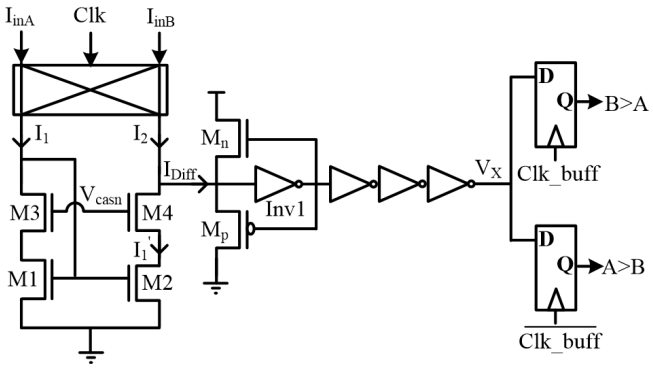


Figure 5. 2. Current comparator (Clk_buff is a delayed version of Clk)

Each current source is matched with the LSB-controlled DAC's maximum current, one at a time, during calibration. The comparator's resolution decides how close the current sources are to the maximum current of the LSB-controlled DAC, which ultimately affects the target-DAC's accuracy. Since this current comparator has to compare large magnitude currents (around 2^N times the LSB current of the N-bit DAC), the current mirror (transistor pair M1-M2) has to be large. For better matching in this case of wide transistors (large W), it is a good strategy to have equal transistors in parallel, each having W not much greater than the length (L). Using the information during both clock phases, we determine whether there is a mismatch between the inputs or not. If no mismatch then both the outputs of the comparator will remain low. If mismatch is detected, then the gate voltage of the MSB-controlled current source, which is being calibrated, is changed according to the comparator outputs, i.e., its increased if comparator output A>B is high (here input A is the MSB-controlled PMOS current source) or vice versa. One of the major factors in the comparator design is the trade-off between the comparator's resolution and its area. For higher resolution, the current mirrors need to be made larger. However, since the target-DAC's linearity is unaffected as long as the difference between the LSB-controlled DAC's maximum current and that of the MSB-controlled current sources is less than the worst step size of the LSB-controlled DAC, the design spec on the comparator is eased.

5.2.2 Simulation results

In order to demonstrate the advantage of using our proposed modular DAC scheme, we simulate a 10-bit dual-calibrated current-steering thermometer DAC using a single 8-bit dual-calibrated current-steering thermometer DAC and calibrated current sources in MATLAB environment. Ideally, we could design a 10-bit DAC from scratch with 4 redundant cells per row. This would give the best performance, and is our actual design target (target-DAC), but would require complete redesign of the addressing scheme to be compatible with the larger DAC. However, in order to minimize design cost, we use our 8-bit DAC module, already designed using the redundancy technique with 2 outliers per row.

To obtain the resolution of our current comparator, we simulate our comparator design in Cadence Virtuoso environment using TSMC 65nm technology. The cascode transistors (M3-M4) are NMOS with typical threshold voltage while the current mirror pair (M1-M2) are NMOS with low threshold voltage. The nominal current for the 8-bit DAC is 2.4μA. Hence, the nominal currents for the comparator are 256 times this current. We determine the resolution to be 0.09%, after running Monte Carlo simulations for the main source of mismatch in the comparator, i.e., the current mirror. The area of the comparator is 35% of the 8-bit DAC's active core area.

Including the comparator resolution, we model the performance of a 10-bit modular DAC. Figure 5.3 shows the improvement in both the INL_{DAC} (worst case INL of the DAC) and the DNL_{DAC} (worst case DNL of the DAC) over a standard 10-bit thermometer DAC without any calibration based on 5000 Monte Carlo simulations.

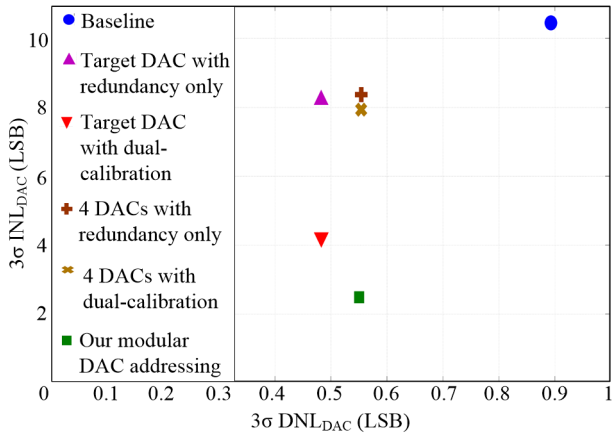


Figure 5. 3. Impact of proposed modular scheme on linearity, using 8-bit DAC(s) to make a 10-bit DAC (20% mismatch in intrinsic DAC's unit cells)

We improve the 3σ performance of the DNL_{DAC} by 38% and the 3σ performance of the INL_{DAC} by 76.6% when compared to the baseline DAC. Without the modular scaling technique, a designer could redesign the entire DAC for 10 bits using the dual-calibration technique with 4 outliers per row. When compared to the target 10-bit DAC with the same percentage of redundancy as that of the 8-bit DAC we achieve an improvement of 41.8% in INL_{DAC}. Our 3σ of the DNL_{DAC} is 0.0672 LSB more than that of the target-DAC in this case, however, our circuit's area is only 60% of this target-DAC's area. Another concept of modular design is demonstrated in [13] in which four low resolution DACs are connected together to obtain a higher resolution DAC. Figure 5.3 shows the results of connecting four 8-bit dual-calibrated DACs together. Each DAC is modeled with redundancy of 2 outliers per row. By comparing the response from both the modular schemes, we observe that though our modular design has a similar impact on the DNL_{DAC}, it shows significant improvement in the INL_{DAC}, reducing it by 68.2%. The reason for this is that any reordering (based on sorting of elements) reaps more benefit if all elements are taken together instead of grouping the samples first and then applying reordering.

We next compare these two modular schemes by modeling three 8-bit DACs, each calibrated using techniques discussed in the literature – SSPA [26], DMM [25] and complete-folding (CF) [27]. All three calibration methods optimize the switching sequence of the DAC unit cells with algorithms having complexities of $O(n^2)$ (chapter 3), where n is the total number of unit cells in the DAC, in order to achieve benefits in static and dynamic nonlinearity. Due to this they cannot be scaled very easily without redesign of the calibration and addressing scheme.

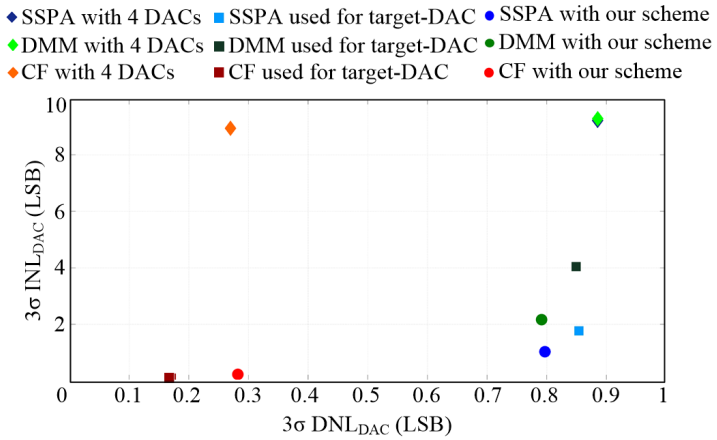


Figure 5. 4. Performance comparison of proposed modular scheme on linearity, using 8-bit DAC(s) equipped with different calibration techniques to make a 10-bit DAC (20% mismatch in intrinsic DAC's unit cells)

Figure 5.4 demonstrates the superior performance of our modular addressing scheme by comparing the performance of our proposed scheme against the case of using four separate DACs connected together. We obtain a 69.6%, 88.6% and 97.4% improvement in INL_{DAC} using our modular addressing scheme against the other modular scheme for DACs calibrated using SSPA, DMM and complete-folding methods, respectively. When compared to intrinsic 10-bit calibrated DAC, our modular DAC outperforms in both cases where the target-DAC is calibrated with the SSPA and DMM techniques. For the target-DAC calibrated using the complete-folding

technique, the INL_{DAC} has similar impact. Though DNL_{DAC} with our modular scheme is 0.1 LSB more for this case, our scheme performs better in terms of circuit modifications, area and complexity.

5.3 Future research directions

The techniques developed in this work reduce the effects of variation and device mismatch in thermometer DACs. The methods used to implement these techniques on chip demonstrate their correctness and through the measurement results, we have validated the theoretical, simulation and the experimental results. The following sub-sections briefly discuss some potential extensions of this work.

5.3.1 ABS circuit

For the purpose of determination of outliers for the redundancy scheme we convert the analog value of the median and the output of the unit cells to their digital counterparts and compute their difference in digital domain. But for a better range, the error between the median and the output of unit cells can be computed first and then this error can be digitized and sorted for outlier determination. For this an absolute (ABS) circuit is required as shown in Figure 5.5.

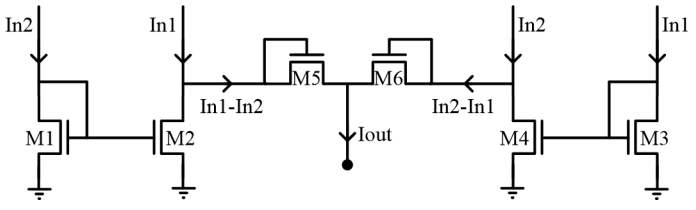


Figure 5. 5. Schematic of ABS circuit

The ABS circuit inputs two currents, In1 and In2 and gives the absolute error between them as the output, Iout. The working of the circuit is as follows. If In1>In2 then M5 turns on as I_{M5}=In1-In2>0 and M6 is off since I_{M6}=In2-In1<0. Hence, at the output we get I_{M5}. For the opposite scenario when In2>In1, M5 is off and M6 is turned on. Hence, Iout = I_{M6}. Therefore there is always a positive current flowing through the output node in the direction shown. To remove any mismatches between the NFET pairs (M1, M2 and M3, M4) of the current mirrors, dynamic element matching (DEM) can be introduced as well.

5.3.2 Addition based current source

To reduce the magnitude of the mismatch error itself, some form of trimming is required. Instead of post-fabrication trimming, we can use the addition based current source [66] as shown in Figure 5.6.

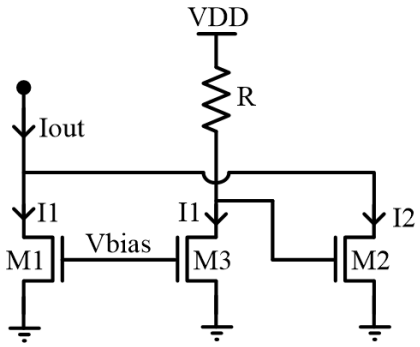


Figure 5. 6. Addition based current source

The output current, Iout is set by I1 and I2. Any increase in I1 will result in decrease of the gate voltage of M2. This in turn will decrease I2. Hence, by properly setting the value of the resistor, R the variance of the output current can improved by a factor of 2 [67].

5.3.3 Dependence of I/O blocks on DAC linearity

As discussed in chapter 4, various circuit blocks in the I/O system use DACs. In this work, we have developed the linearity relation between one the critical blocks of the I/O – the PI and the DACs controlling its tail currents. Similar relationships can also be developed for the other I/O blocks like the DFE and the CTLE. Using all these in a mathematical model of an I/O link, we can derive the variance of the BER at the output. Developing such a mathematical tool will help circuit designers to quantify the severity of process variation and random mismatches on the yield of I/O circuits with faster turn-around time.

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