INTEGRATED DISPERSIVE DELAY LINE (DDL) FOR REAL TIME ANALOG SIGNAL PROCESSING

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INTEGRATED DISPERSIVE DELAY LINE (DDL) FOR REAL TIME ANALOG SIGNAL PROCESSING

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The dispersive delay line (DDL) is a very useful device in the communication system for decades. It is widely utilized in the radar communication system, optical communication system, ultra-wide-bandwidth (UWB) system, etc. Even though there are a number of DDLs operating in microwave, RF, photonics regime, etc., few attempts have been reported towards the integration of this useful device. Our work focuses on the integration of the DDL with standard CMOS process. There are two major challenges in the integration of the DDL, on-chip loss and the non-idealities in DDL's performance. In this thesis, we present three major attempts to solve these challenges and all of these attempts employ the distributed amplifiers (DAs). In the DA, the artificial transmission line section is very size efficient in providing enough group delay and the gain cells are capable of gain compensation for on-chip loss. The first attempt employs the specially designed highly dispersive artificial transmission line section. The second attempt employs the multi-path approach to compensate the great loss near the cutoff frequency. The third attempt, however, employs the backward traveling gain port of the DA to realize a reconfigurable integrated transversal filter. Since most of the existing DDLs can be mapped to transversal filters with correspondent tap coefficients, the reconfigurable integrated transversal filter can be utilized to achieve multiple DDL functions.

This thesis also includes the demonstration of the real time analog signal processing using these integrated DDLs, including the first on-chip demonstration of the temporal imager (TI), time stretching (TS) system, and real time spectrum analysis using the integrated DDL with the third attempt. Our integrated DDL has low TBP value of five and practical design considerations of the integrated TS system with small TBP remain unexplored. We derive the time resolution of a general TS system using both the principle of uncertainty and the Short Time Fourier Transform (STFT) method. This fundamental result enables a designer to understand the qualitative relationship between the TBP and the best possible resolution of the TS system.

BIOGRAPHICAL SKETCH

Bo Xiang was born in the Chengdu, Sichuan, China. In 2005, he received his Bachelor of Science Degree from the Electrical and Computer Engineering of Peking University, Beijing. After finishing his undergraduate studies, he went to Department of Electrical and Computer Engineering of University of California, Davis and earned the Master of Science Degree in 2007. Then he joined the MS-PhD program in Department of Electrical and Computer Engineering in Cornell University, Ithaca, NY.

To my parents, Mingjian Jiang and Qian Xiang

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CHAPTER 1

INTRODUCTION

1.1 Background of Dispersion and Existing Dispersive Delay Lines (DDLs)

Dispersion describes the phenomenon of pulse spreading caused by different frequency components of a signal or pulse traveling at different velocities and experiencing different amounts of group delay (Figure 1-1).

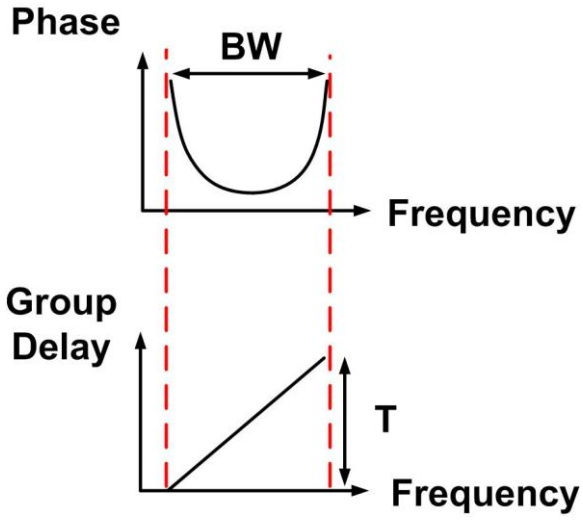

Figure 1-1 Illustration of a DDL with linear dispersion characteristic.

In optical communication, the chromatic dispersion of the optical fiber induces the pulse spreading which results in inter-symbol interference (ISI). This has been one of the biggest challenges for the optical network engineers when they attempt to enhance the data rate of existing optical communication systems. However, one can make use of the dispersion in spreading a pulse. A typical example is the photonic time stretch

analog-to-digital conversion (TS-ADC) [1]. The input signal, which is modulated onto a chirped carrier, gets spread by the single-mode fiber (SMF) and the signal envelope is stretched. In this way, the original signal is effectively slowed down and the lower rate ADC can be used to sample the fast signal. The typical photonic TS-ADC exhibits the stretch factor of 10 [1]. The TS-ADC can be pushed to its extremes with a stronger dispersive device, e.g. distributed Raman dispersive element, to realize the femto-second real-time single-shot digitizer, whose stretch factor is 250 [2].

Generally speaking, the dispersion in any medium will cause the pulse spreading and inter-symbol-interference (ISI) (as shown in Figure 1-2), but the chromatic dispersion of the typical electrical transmission line is relatively small as compared to dispersion in optical fiber. The dispersion provides a frequency-to-time mapping and it is capable of representing the signal spectrum in a real-time manner. Therefore, the electronic engineers have deliberately designed the dispersion engineered device, also known as dispersive delay line (DDL) or chirped filter, to perform real time analog signal analysis and processing. This thesis focuses on the integration of the DDL using a standard CMOS process and the real time analog signal processing blocks based on the integrated DDL.

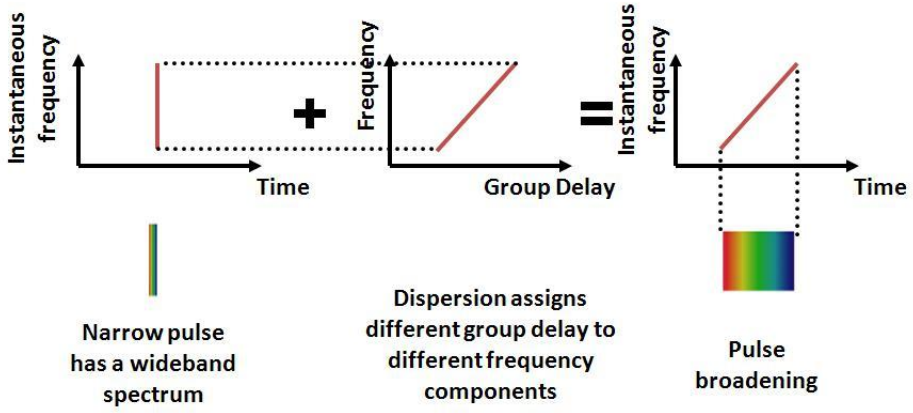

Figure 1-2 Pulse broadening as the narrow pulse propagates through a dispersive channel.

DDLs have been widely used in communication systems for signal detection and analysis for decades. DDLs are especially useful in wideband systems and spread spectrum systems. In radar communication and ultra-sonic systems, SAW DDLs are used for real-time signal analysis including Fourier Transform, Chirp Z Transform, waveform synthesis, programmable correlator, variable delay line, etc [3]. The SAW DDLs have the most compact size among the existing DDLs, but its high insertion loss and low operating frequency range are the main drawbacks [3]. With the discovery of the high-temperature superconductors (HTSs), engineers have implemented the HTS DDL with low insertion loss, compact size and wider frequency band (~ 10 GHz) that can operate at microwave frequencies [4]. The HTS DDLs are designed for wideband compressive receiver, which rivals the sensitivity of the narrowband receiver, and real-time spectrum analysis operating at higher frequency range rather than the SAW DDLs [4, 5]. The major drawback of the HTS DDLs is that they operate at the ultra-low temperature (4 K ~ 80 K). Engineers continue to search for the delay lines that can operate at room temperature with acceptable insertion loss, and they make use of the copper coplanar waveguides (CPW) [6] or microstrip lines [7]. With high speed materials (e.g. Rogers material), the microstrip DDL exhibits low insertion loss (< 5 dB), operates at room temperature, and works up to 10 GHz. The microstrip DDL exhibits varying characteristic impedance along the line. Since the microstrip DDL shares the same operating frequency range with the ultra-wide-bandwidth (UWB) signals, a number of microstrip DDLs are designed for the applications in UWB systems. The UWB signals are pulsed signals with limited time length (~ 1 ns) and wide frequency range (3 GHz to 10 GHz) [6, 7]. This feature also

complies with the attributes of the DDLs because the group delay is a parameter that is related to the wideband operation and is meaningless for the narrowband signal. The microstrip DDLs have been utilized for real-time spectrum analysis [8], tunable time delay line [9], frequency discrimination [10], time-stretching (TS) system [11], etc. The major drawback of the CPW or microstrip DDL is that their size is on the scale of the wavelength of the carrier signal (~ 10 cm for 10 GHz). Another well-known DDL based on microstrip technology is the composite right / left handed (CRLH) DDL which is basically a meta-material structure [12]. Its application includes pulse position modulation (PPM) [13], compressive receiver [14], pulse generation, true time delayers (TTD), frequency resolved electrical grating (FREG), spatial-temporal Talbot effect, etc [12]. The CRLH DDLs employ the lumped elements (inductors and capacitors) to realize the right hand and left hand sections. They require the values of these lumped elements to be accurate and the size of the existing CRLH DDLs is around 10 cm. Table 1-1 includes a comparison of different types of existing DDLs.

Category	Advantage	Disadvantage
Optical Fiber [1, 2]	High Frequency (~ 100 THz) and TBP (~ 1000)	Huge length (~ 10 km), Cumbersome Elements, Costly Laser Sources
SAW [3]	Large TBP (~ 1000), Compact (5 mm ~ 5 cm)	Low Frequency (< 1 GHz), Large Insertion Loss (> 20 dB)
HTS [4, 5]	UWB Range (~ 10 GHz), Medium TBP (10 ~ 50), Low Loss (< 5 dB)	Ultra Low Temperature (4 K ~ 85 K)
CPW and Microstrip [6-11]	UWB Range (~ 10 GHz), Medium TBP (10 ~ 50), Low Loss (< 5 dB)	Size Scaled with Wavelength (~ 10 cm)

CRLH [12-14]	UWB Range (~ 10 GHz), Medium TBP (~ 10), Low Loss (< 5 dB)	Accurate Lumped Elements, Big Size (~ 10 cm)

Table 1-1 Comparison of Different Types of DDLs.

1.2 Progressions of the Integrated DDLs

Even though the DDL is so important and useful in a variety of applications, there are few attempts to integrate a DDL on chip even if the integration would greatly reduce its size and cost, and increase the number of systems in which they could be leveraged. As shown in Table 1-1, optical DDLs are based on the dispersion provided by the single mode fiber (SMF) or dispersion compensated fiber (DCF), which need kilometers to generate nanoseconds of delays [1, 2]. SAW DDLs are the most compact among the existing DDLs, but they have insertion loss (above 20 dB) and only operate at low frequency (below 1 GHz) [3]. HTS DDLs can be implemented with compact size and engineers have successfully confined a long delay line (2 meters or more) into a small area (2 inches in diameter) without degrading its electromagnetic performance. However, the HTS DDLs need to be cooled to ultra-low temperature (85 K) for the lines to be superconductive, and this constraint limits its application in current UWB systems [4, 5]. CPW and microstrip DDLs operate with low insertion loss, but their size is on the order of the carrier wavelength (~ 10 cm), preventing them from integration [6-11]. Meta-material DDLs employ only lumped elements and occupy tens of centimeters, and their passive nature prevents integration due to on-chip loss [12-14]. The integration of the DDL remains unexplored.

This thesis explores the challenges and the possible solutions towards the integration of the DDL in standard CMOS process. There are two major barriers to the integration of DDLs. First, the size of the DDL determines the total group delay variation it can provide. Larger delay requires bigger size. Miniaturization requires a structure that can provide a large delay over size ratio and can significantly slow down the propagating signal. Second, on-chip loss increases significantly as we add more delay blocks to generate larger dispersion. Therefore, we need to search for an active device that can provide large enough group delay variance and a good candidate is distributed amplifier (DA). In the DA, the delay is provided by the artificial transmission line and the gain is provided by the gain cells. The parasitic capacitances at the gate and the drain of the transistors are absorbed into two artificial transmission lines, enabling its ability of the high speed and wideband operation. The conventional DA is designed to be dispersion-free. In our case, however, we need to deliberately introduce dispersion.

Our first attempt towards the integration of the DDL employs the forward gain of the DA equipped with the specially designed dispersion enhanced artificial transmission line. The dispersion enhanced artificial transmission line incorporates an LC tank, functioning as a frequency dependent inductor. With this technique, we implement the first integrated DDL in 130 nm IBM 8RF CMOS process [15]. The integrated DDL operates from 11 GHz to 15 GHz and provides the dispersion of 1 ns. This integrated DDL provides a plausible solution to the two challenges of integration stressed earlier in this section, but it has an intrinsic drawback. It utilizes the dispersion near the cutoff frequency of the artificial transmission line, and the highest dispersion (1 ns) is associated with biggest attenuation (35 dB).

In order to improve the performance of the first integrated DDL, we employ the multi-path approach in our second attempt. The input signal is split into multiple

frequency components by a bank of bandpass filters (BPFs) and each frequency component is assigned with a particular group delay and gain profile. The BPF operating near the cutoff frequency of the DA exhibits high gain to compensate for the big attenuation. Compared to the previous integrated DDL, the improved integrated DDL shows 60% more dispersion at the frequency of 6 dB loss [16]. The two DDLs discussed above are the first two attempts towards the integration of this useful device and both of them employ the forward gain of the DA. However, both integrated DDLs have non-linear dispersion characteristic induced by the resonance tank in the artificial transmission line section. Therefore, we move forward to search for the approaches that can provide controllable dispersion characteristic and gain profile.

We reinvestigate into the existing DDLs including SAW DDLs [3], HTS DDLs [4, 5] and microstrip DDLs [6-11] and discover that all of them utilized the reflective wave as the output signal and can be modeled with a non-uniform line in general. In a non-uniform line, the input signal is reflected at different locations along the line and the reflected waves are summed up at the input port. This feature reminds us of the transversal filter in which the input signal is tapped out at different locations and summed up at the output port [6]. In the conventional transversal filter structure, the output port is loaded with a large number of gain cells, and this will greatly degrade the performance of the transversal filter. In this thesis, we employ the reverse gain port of the DA to realize the transversal filter [17]. As the signal propagates along the gate line, the gain cells turn the voltage mode input signal into a current mode output signal on the drain line. The current mode output signal is turned back into the voltage mode by a matched resistance at the reverse gain port. In this way, the input signal is effectively reflected at each gain cell and summed up at the reverse gain port. The heavy loading of the gain cells is distributed along the drain line and the frequency performance is enhanced over the conventional transversal filter. Fortunately,

transversal filter has been integrated on chip and widely used in equalizers [17]. In this thesis, we implemented the reconfigurable integrated transversal filter in 130 nm IBM8RF CMOS process. Now that we have determined the structure of the integrated DDL, we proceed to find out the relationship between the non-uniform line and the tap coefficients of the transversal filter. An arbitrary non-uniform line can be characterized using the Riccati equation [7]. The Riccati equation provides a connection between the impedance profile of the non-uniform line to its transfer function. Therefore, given enough information of the non-uniform line, e.g. the structure or the impedance profile, we can obtain its transfer function by solving the Riccati equation. We can also obtain the impulse response by taking the inverse Fourier Transform (IFT) of the transfer function. Sampling the impulse response with delay between the adjacent taps gives the correspondent tap coefficients of the transversal filter. This is the third attempt towards the integration of the DDL. One of the major advantages of this integrated DDL is the reconfigurability. Multiple non-uniform lines can be realized with a single chip by changing its tap coefficients. For example, in this thesis, the reconfigurable integrated transversal filter with the area of 2 x 1.6 mm x 5 mm is utilized to realize the transfer function of four different non-uniform line based DDLs, each one is 80 mm in length. Furthermore, the reconfigurable integrated transversal filter provides gain to these transfer functions. Instead of going through the process of design and fabrication four times, we can make use of a single device to realize multiple transfer functions. The reconfigurable integrated transversal filter is not limited to only four different transfer functions, it is able to realize the transfer function of any arbitrary non-uniform line. The experimental demonstration of the reconfigurable integrated transversal filter is realized with an FR-4 printed circuit board (PCB) and the chips are placed onto the QFP packages PLQ06401 and wirebonded for connection. The FR-4 material and

wirebonds degrade the high frequency performance of the reconfigurable integrated transversal filter to the cutoff frequency of 4.5 GHz and the high frequency performance can be enhanced if high speed probes are involved in the measurement. This thesis provides a proof-of-concept demonstration and the operation frequency can be scaled up with specially designed elements such as gain cells and delay blocks.

1.3 Advance of Theory on Real Time Signal Processing

In addition to the design and implementation of the integrated DDLs, this thesis also includes the advanced theory of the real-time signal processing. As mentioned earlier in Section 1.1, the photonic TS system can be used for accurate operation like ADC and single shot digitizer. The error introduced by the stretching process is negligible in photonic TS system because of its large time-bandwidth product (TBP) (~ 1000). In our electronic TS system, however, the TBP is on the order of 5. As a result, the stretching process in the electronic TS system involves significant errors and distortions as compared to that of the photonic TS system [16]. Therefore, the electronic TS system is not suitable for the accurate operation such as data conversion, but is a good candidate for the operation that does not require high level of accuracy such as pulse detection. However, the error and distortion of the stretching process of the TS system with low TBP remains unexplored. In this thesis, we perform the theoretical analysis of an ideal TS system with low TBP, which qualitatively explains how the TBP value affects the errors and distortions in the general time stretching process [16]. Moreover, we also discovered that the time stretching process that employs the chirped signal and the dispersion can also be explained with the Short Time Fourier Transform (STFT) [18]. The input chirped pulse and the output chirped

pulse form a pair of Fourier Transform, and by applying the principle of uncertainty, we can derive the time resolution in the stretching process. The physical explanation of the time resolution in the stretching process can be expressed as follows, one cannot map a specific point of the input pulse or original pulse to its correspondent point of the output pulse or the stretched pulse. Instead of that, one can map a time slot in the input pulse and find the correspondent time slot in the output pulse. The energy in the input time slot is preserved in the output time slot. In this way, we discover that the large TBP results in a finer time resolution and a more accurate stretching process [16]. The analysis indicates the theoretical limit on the accuracy and time resolution of a TS system with low TBP. The theory proposed in this thesis can also be applied to analyze the general TS system with arbitrary TBP value.

1.4 Advance of Applications / Experimental Demonstrations

With the integrated DDLs implemented in this thesis, we successfully perform the on-chip demonstration of several real time signal analysis and processing blocks. The first application is the temporal imager (TI) [15]. The TI employs a ramping VCO to generate the chirped carrier and an integrated DDL to provide dispersion to the chirped signal. It operates from 11 GHz to 15 GHz and is capable of stretching a 1 ns pulse into a 2 ns pulse and compressing a 2 ns pulse into a 1 ns pulse.

The second application is the time stretching (TS) system in which the input signal is time-scaled into a stretched version. The TS system is a special case of the TI system and we use the similar setup as the TI system. The TS system employs the ramping VCO and the improved DDL for better accuracy. It is capable of stretching a single 1 ns pulse into a 2 ns pulse and two 1 ns pulses into two pulses with the total

length of 3 ns. Compared to the TI system which employs the first integrated DDL, the TS system exhibits lower distortion in the stretching process and stronger ability in preserving the pulse shape.

The third application introduced in this thesis is the real time spectrum analysis (RTSA) realized with the DDL based on the reconfigurable integrated transversal filter. The 0.6 ns input pulse stream, which is a 6 bit long 10 Gbps pulse stream, is sent through the integrated DDL whose operating range is 0.4 GHz to 4 GHz and the total dispersion is 1.2 ns. The different frequency components of the input pulse stream experience different amounts of group delay and end up at different time locations of the output signal. The envelope of the output signal resembles the spectrum from 0.4 GHz to 4 GHz in a 1.2 ns window. Like other electronic DDLs, the integrated DDL also suffers from low TBP, which means that the output signal does not have a large number of carrier cycles to fully characterize all the details of the spectrum as the photonic real-time spectrum analyzer does. However, it can be used for the rough spectrum estimation of the pulse signal in real time manner. Compared to the commercialized real time spectrum analyzer, it is compact in size and consumes much less power.

1.5 Organization of the Thesis

The thesis focuses on the integration of the DDL and its applications in a real time manner. It also reveals the potential of integrating the complicated real time analog signal processing system on chip. Chapter 2 discusses the first integrated DDL based on the dispersion-enhanced DA using 130 nm IBM8RF CMOS process. It explains the fundamental theory, design procedure, simulation, and experimental demonstration in

detail. Moreover, we present the integrated time stretching (TS) system using a ramping voltage controlled oscillator (VCO) and the first integrated DDL. The integrated TS system operates in the range of 11 GHz to 15 GHz, and is capable of stretching a 1 ns up-chirped pulse to a 2 ns pulse as well as compressing a 2 ns down-chirped pulse to a 1 ns pulse. There is one drawback of this DDL though. It makes use of the dispersion near the DA's cutoff frequency and the largest dispersion is associated with the highest attenuation. This causes the errors and distortions in the stretching and compression process, and we develop an improved DDL to overcome this drawback.

We take a step forward in Chapter 3 by applying the multi-path approach to the first integrated DDL and implement the second integrated DDL. Before going into the DA, the input signal is first split into multiple channels by a bank of BPFs and then launched into different locations of the DA. In this way, the dispersion provided by the DA is fully utilized and the gain of the BPFs can be adjusted to compensate for the loss where the largest dispersion occurs. Compared to the first integrated DDL, this DDL improves the dispersion by 60% and exhibits 1.5 ns of dispersion at the 6 dB loss point. We implement the TS system using the ramping VCO and the improved DDL. This TS system can stretch a 1 ns up-chirped pulse to a 2 ns pulse, and stretch two 1 ns up-chirped pulses to two pulses with total length of 3 ns. Even though we improve the integrated DDL, the stretching process still exhibits distortions and the theoretical analysis is needed for a satisfactory explanation.

In Chapter 4, we perform theoretical analysis of a general TS system with ideal components. The ramping VCO generates an ideal linear chirp and the DDL is an all-pass filter with perfect quadratic phase in the frequency range of interest. It is well-known that the TS system can be applied to accurate operation in photonic TS ADC because of their large TBP value. The analysis presented in this chapter covers a more

general case with arbitrary frequency operation range, dispersion value and TBP value. This analysis provides a good insight for the electronic engineers on the relationship between the distortion of a stretching process and the TBP value of the TS system. Furthermore, we also make an interesting discovery that the input chirped pulse and the output chirped pulse form a pair of Fourier Transform. Applying the principle of uncertainty, we propose the idea of time resolution in the stretching process. The physical explanation of the stretching process can be understood as follows, a certain time slot of the input chirped pulse is stretched into its correspondent time slot of the output chirped pulse, where the energy of both slots are preserved. The time resolution is also related to the TBP, larger TBP gives rise to a finer time resolution. We also use short time Fourier Transform (STFT) to present the stretching process in a more illustrative way.

Since there are intrinsic non-idealities in the first two integrated DDLs, we start searching for the better candidate of integrated DDLs in Chapter 5. This chapter starts with the review of the existing reflective-type DDLs, which can be modeled as a non-uniform line. Most of the existing DDLs employ the reflected wave as its output and can be characterized with a single governing equation, known as Riccati equation. The Riccati equation relates the physical structure or impedance profile of an existing DDL to its reflective transfer function. The reflective-type DDLs or the non-uniform transmission line can be modeled and realized with a transversal filter. The tap coefficients can be obtained by sampling the impulse response of the non-uniform line. We propose the design procedure that maps the design of the non-uniform line DDL to the correspondent tap coefficients of the reconfigurable integrated transversal filter. The reconfigurable integrated transversal filters have already been used for equalization in the digital communication systems, so we can take the similar design and implementation for our application. The reconfigurable integrated transversal

filter is implemented in 130 nm IBM8RF CMOS process with the area of 1.6 mm x 5 mm. This chapter also provides the experimental demonstration using the reconfigurable integrated transversal filter. In this thesis, we present four examples showing that the reconfigurable integrated transversal filter can be utilized to realize the reflected transfer functions of multiple non-uniform line DDLs. By properly adjust the tap coefficients we can generate the similar transfer function as the non-uniform line DDL with gain. Furthermore, we also perform the first on-chip real-time spectrum analysis with the DDL realized with the reconfigurable integrated transversal filter.

Finally, Chapter 6 is the conclusion of this thesis. This thesis not only fills the blank spot in the dispersion engineer, but also opens up the door for the integration of various real time signal analysis and processing systems. This chapter also discusses the future direction towards the integration of the DDL using standard CMOS process.

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CHAPTER 2

INTEGRATED DDL BASED ON DISPERSION ENHANCED DA

Our first attempt towards the integration of DDL employs the dispersion enhanced distributed amplifier (DA). It is the first on-chip design and implementation of an active integrated dispersive delay line (DDL). This integrated DDL exhibits nanosecond delay variation in the frequency band from 11 GHz to 15 GHz. An on-chip temporal imager (TI) is implemented with this integrated DDL and a linear chirp generator, realized by ramping the control voltage of a voltage controlled oscillator (VCO). The experimental data exhibits stretching as well as compression on the pulsed signal with this system.

2.1 Introduction

An ideal dispersive delay line (DDL) is characterized by its quadratic phase response and uniform magnitude response over some frequency range [1]. The DDL is the key component that performs various analog signal processing applications, including time manipulation for ultra-wideband (UWB) signals [1], real-time spectrum analysis [2], compressive receiving [3] and photonic time-stretching [4], etc.

Surface acoustic wave (SAW) DDLs and magneto-static wave (MSW) devices are the most widely utilized and commercialized DDLs. SAW DDLs are known for their large delay (~1 us), compact size (~10 mm), limited operating frequency range (less than 1 GHz) and big insertion loss [5]. The MSW DDLs can support high frequency and wide-band operation, but require a permanent magnet and complex fabrication [6].

Photonic DDLs are usually realized with dispersion in single mode fiber (SMF) (~1

km) [4] or chirped fiber Bragg gratings (CFBG) (~40 cm) [7] and leverage the extremely high frequency and relatively large bandwidth of optical systems to produce large time-bandwidth products (TBP). While the large TBP of such systems enables high performance, the use of precision optical components (e.g. mode-locked lasers) largely confines these to a laboratory setting. Many practical implementations of an analog signal processor would benefit from board- or chip-scale integration.

Inspired by optical CFBGs, the chirped electromagnetic bandgap (CEBG) DDL has been demonstrated for ultra-wideband (UWB) signals (3 GHz to 10 GHz) [1]. However, its size scales in accordance with the wavelength of the carrier (~10 cm), preventing it from on-chip integration. Another DDL in the microwave regime (~2 GHz) is the composite right/left handed (CRLH) transmission line, but it is still a board level design and occupies tens of centimeters [3].

Among all the existing DDL techniques, with size varying from 10 mm to 1 km (single mode fiber is close to 1 km) [1-7], none has achieved on-chip integration. In this letter, we introduce the first on-chip design and implementation of the monolithic active DDL in a 130 nm CMOS process. The comparison of the performance of the current DDLs is presented in Table 2-1.

Our unique approach combines a dispersive resonance circuit with the distributed amplifier (DA). Since a DA can be designed for a wide range of cutoff frequencies, this approach allows a DDL to be implemented at virtually any microwave frequency. The DA provides a broad frequency operation range as well as enough gain to compensate for on-chip loss. With this active DDL, we have demonstrated an on-chip temporal imager [8-10], which is capable of pulse stretching and compression. With this technique, the UWB receiver bandwidth could be cut in half, allowing shorter pulses and wider band operation.

Category	Material	f_C* (GHz)	BW* (GHz)	Stretch (ns/mm)	Insertion Loss (dB)
SAW [5]	LN*	0.35	0.08	167	30 ~ 40
MSW [6]	Magnetic	3	0.5	50	30
Optical [4]	Optical	1.3×10^5	10 ~ 50	1.9×10^{-6}	3
CEBG [1, 2]	Electrical	2 ~ 14	15	0.02	7
CRLH [3]	Electrical	2.5	1	7.5×10^{-3}	3
ADDL	CMOS	13	4	0.33	15 (gain)

* LN = Lithium Niobate, f_C = Center Frequency, BW = Bandwidth

Table 2-1 Comparison of the Performance of the Current DDLs

2.2 Design of the Active DDL

The design of the active DDL employs the DA structure shown in Figure 2-1. In a conventional DA, the parasitic capacitances at the gate and the drain of the transistors are absorbed into two artificial transmission lines, called the gate and drain line respectively. As the input signal propagates along the gate line, each gain cell generates a forward and backward traveling current on the drain line [11]. The DA is designed such that the forward traveling current is added up in phase at the output port while the backward traveling current is fully absorbed at the reverse port termination. The group delay through a DA is clearly proportional to the number of gain cells, so a long DA is required for an effective DDL. However, the number of gain cells cannot increase to infinity because the loss of the lumped elements limits the number of transmission line sections and gain cells. The optimum number of cells in a DA is

typically between 3 to 8 [11]. In order to extend the group delay beyond this limit, the DDL presented in this paper is realized by cascading 3 optimized DAs (each with 4 gain cells) shown in Figure 2-1, resulting in a total of 12 gain cells.

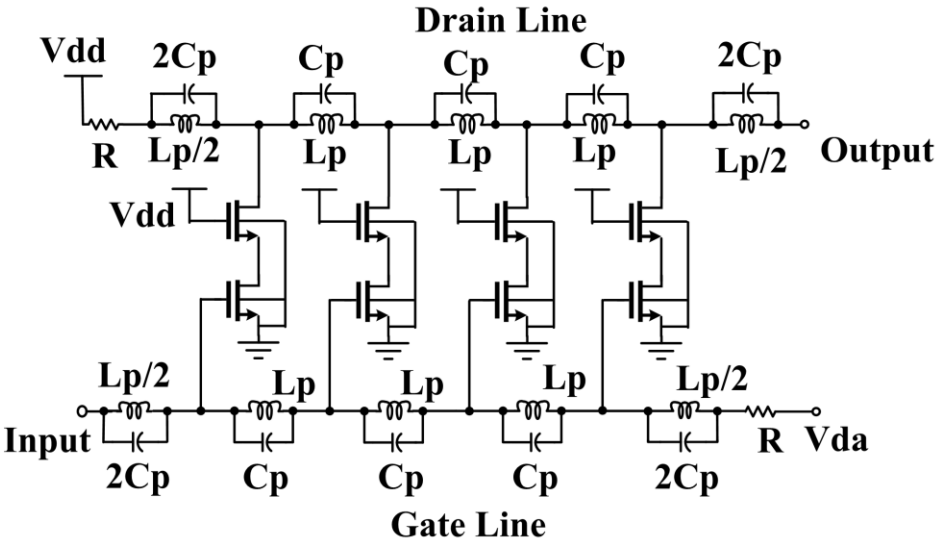

Figure 2-1 Schematic of the proposed DA. The active DDL is realized by cascading 3 DAs. R=50 Ω, Lp=415 pH, Cp=187 fF, all the NMOS transistors have the same size: 60 um/0.12 um, Vdd=1.2 V, Vda=0.6 V.

The group delay characteristic can be derived by taking the negative derivative of the phase term in the gain of the DA. The simulation shows that the group delay of the DA comes mainly from the artificial transmission line, with only 10% of the group delay contributed by the gain cells. We neglect the group delay of the gain cells and focus on the artificial transmission line, which is usually realized with filter sections composed of lumped elements to form simple low pass filter L-sections. The group delay of the L-section exhibits a rapid increase within a limited frequency range near the cutoff frequency [11]. Here we employ a modified version of the L section to enhance this dispersion over a wider frequency range. Figure 2-2 shows the modified

L-section as well as the comparison of the dispersion characteristic of a conventional L-section and our dispersion-enhanced L-section. The group delay of the conventional L-section (inset (a) of Figure 2-2) is [11].

$$\tau_g(\omega) = \frac{\sqrt{LC}}{\sqrt{1-\frac{\omega^2 LC}{4}}} \tag{2.1}$$

In the modified L-section (inset (b) of Figure 2-2), the inductor is replaced by a parallel LC tank (dispersive resonance circuit) which can be described by an effective inductance, $L_{eff}(\omega)$, which increases as frequency approaches resonance,

$$j\omega Lp \parallel \frac{1}{j\omega Cp} = \frac{j\omega Lp}{1-\omega^2 LpCp} = j\omega L_{eff}(\omega) \tag{2.2}$$

Thus, each dispersion-enhanced L-section appears electrically shorter at the low frequency and electrically longer at the high frequency, than its conventional counterpart.

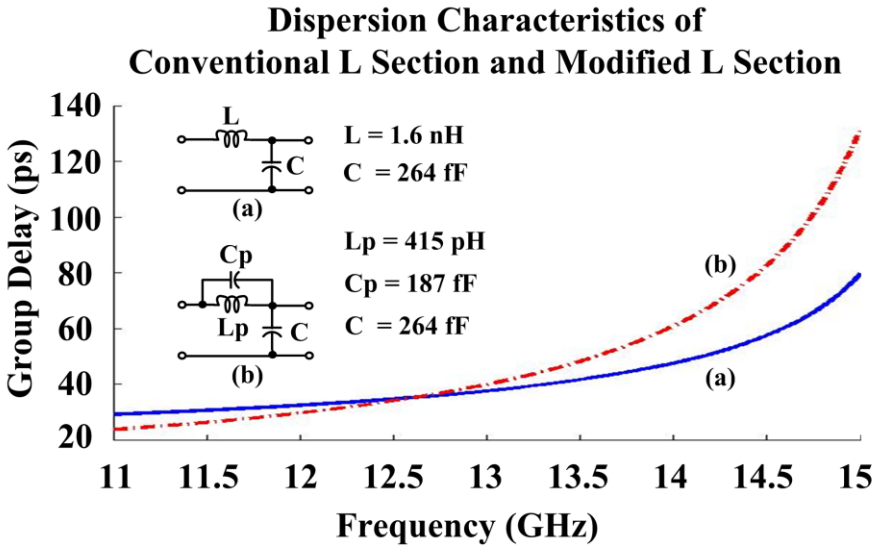

Figure 2-2 Comparison of the group delay of the conventional L section (solid line)

and modified L section (dashed line). The insets illustrate the schematic of the conventional (a) and the modified (b) L sections.

2.3 On-Chip Demonstration of Temporal Imaging

In this section, we will present a typical example of real time analog signal processing. This is also the first attempt towards integration of real time analog signal processing block using the standard CMOS process.

2.3.1. Principle of the Temporal Imaging

As described in the introduction, DDLs offer a wide range of applications in real-time analog signal processing and this section focuses on a class of analog processors called temporal imagers. Temporal imaging refers to the manipulation of the duration of signals in time such as stretching, compressing, or inverting [9]. The name arises from a mathematical analogy to paraxial optical imaging. Caputi proved the concept utilizing three separate DDLs in the microwave regime [8] while Kolner implemented a photonic temporal imager with a quadratic phase modulator [9]. The most recent temporal imager is based upon the four wave mixing (FWM) time lens with quadratic phase characteristic [10].

In our simple imager scheme (Figure 2-3), the input signal is first modulated against a chirped carrier and then sent through the DDL. The DDL provides different amounts of group delay to the different frequency components of the chirped pulse, yielding modification of the pulse envelope duration. More specifically, a positively chirped carrier (i.e. one whose instantaneous frequency increases with time) will be stretched

by a positively dispersed DDL. Conversely, a pulse with a negatively chirped carrier will be compressed by the same DDL [8]. It acts like a temporal-lens that can perform stretching and compressing of an image in time. While most temporal imagers use an additional DDL to convert a broadband pulse into the chirped carrier, our sub-micron CMOS platform allows this implementation to generate a chirp directly by sweeping the control voltage of a voltage controlled oscillator (VCO). The VCO is a basic LC tank with a negative-g_m cross-coupled pair. A MOS varactor in the tank provides a tuning range from 10 to 20 GHz. Whether the output is up- or down-chirped is determined by the sign of the slope of the control voltage. This signal is then mixed with an input pulse signal. The control voltage ramp and the input signal are synchronized by an external clock.

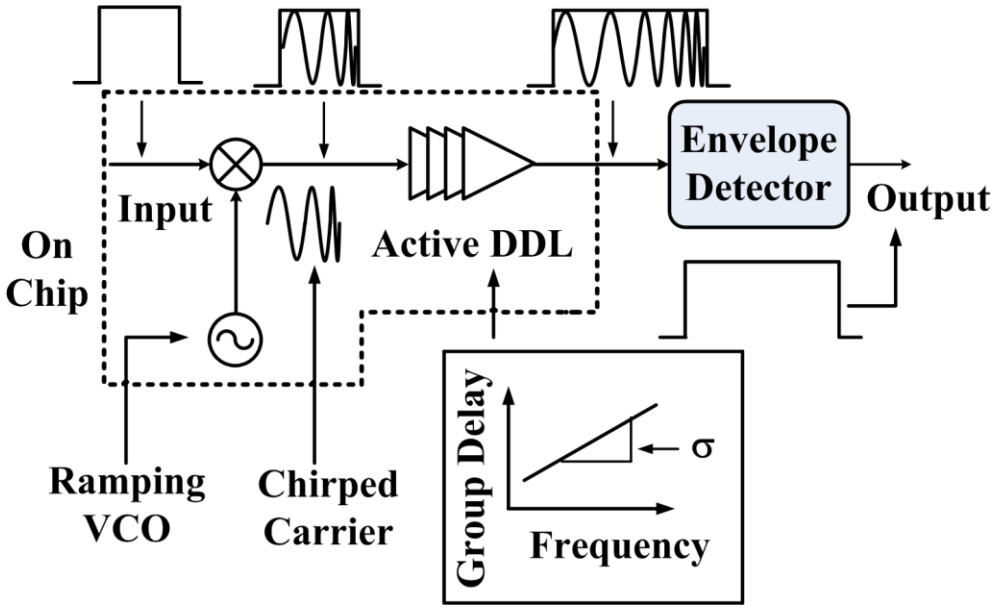

Figure 2-3 Block diagram of the on-chip temporal imaging demonstration. The inset box shows the linear group delay characteristic of the active DDL.

2.3.2. Experimental Demonstration

Figure 2-6 shows the die photo of the ramping VCO and active DDL implemented in a 130 nm CMOS process. 3 DAs (each with 4 unit cells) are cascaded to realize the active DDL. Figure 2-4 shows the measurement results of the magnitude response as well as the group delay characteristic of the active DDL, which is 1 GHz lower than the simulation results because of the on-chip loss and parasitic capacitance. The non-constant magnitude response and the nonlinearity in the group delay reduce the utility of the DDL in high precision applications, but it is sufficient for this proof-of-concept demonstration. The ramping VCO is capable of generating a chirped carrier in the DDL's dispersive bandwidth (11 GHz to 15 GHz) with uniform amplitude. However, amplitude variation could be incorporated into the system to compensate for gain variation. The measured spectrum of the chirped carrier exhibits a good uniformity throughout the operating frequency range, indicating that the chirp is linear with time.

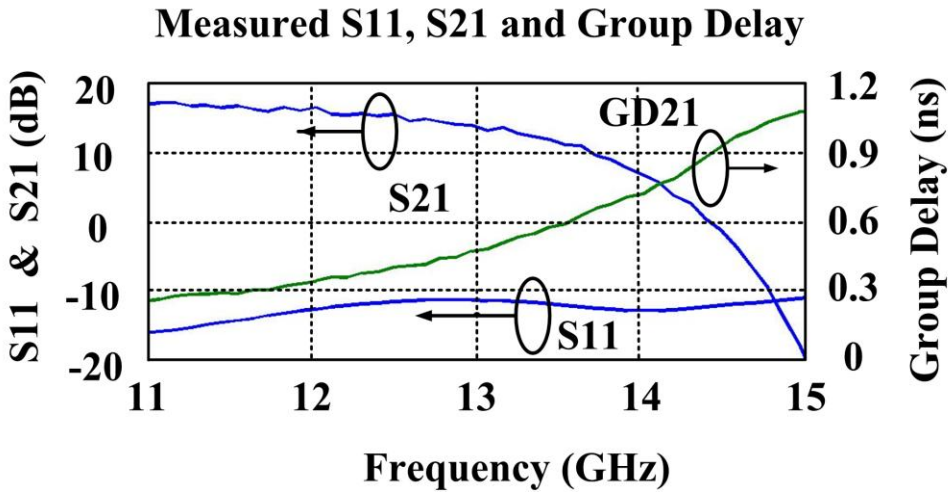

Figure 2-4 Measurement of S11, S21 and group delay of the active DDL.

Figure 2-5 shows the measurement results of on-chip demonstration of temporal

imaging. It compresses a 2 ns down-chirped pulse (Figure 2-5 (a)) into a 1 ns pulse (Figure 2-5 (b)), while stretching a 1 ns up-chirped pulse (Figure 2-5 (c)) into a 2 ns pulse (Figure 2-5 (d)). The temporal imager exhibits a compression factor of 2 on a 2 ns pulse and a stretching factor of 2 on a 1 ns pulse. Both input pulses employ appropriate pulse shaping, and the stretched pulse shows decaying amplitude with time because the higher frequency components, which occur later in time, experience higher attenuation [12].

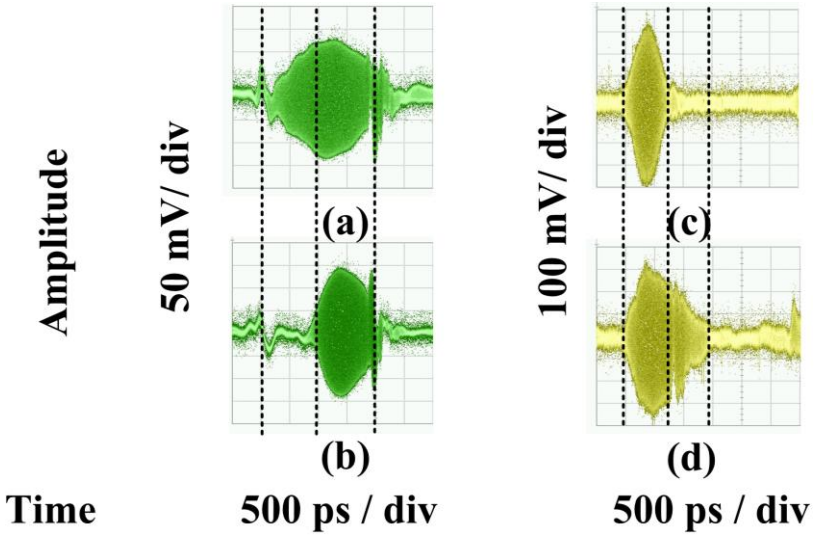

Figure 2-5 Experimental demonstration of temporal imaging, (a) 2 ns input pulse, (b) compressed pulse, (c) 1 ns input pulse, (d) stretched pulse.

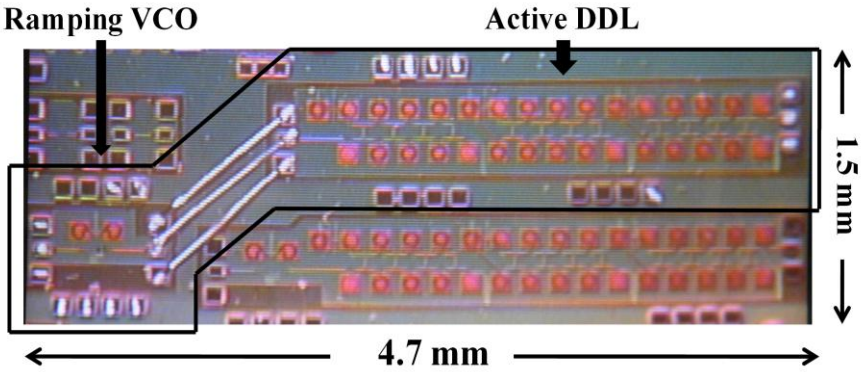

Figure 2-6 Die photo of on-chip demonstration of temporal imaging. To match-up a suitable combination of chirp generator and active DDL, very short bond wires were used as on-chip interconnect, which had no significant impact on the predicted performance.

2.4 Conclusion

The active DDL is the first attempt of integrating a DDL on a CMOS chip. The temporal imager implemented with this active DDL is presented as a proof-of-concept for on-chip real-time analog signal processing in the microwave regime. This DDL is a basic building block for many analog signal processing functions and opens the door for analog processors which are orders of magnitude smaller than those demonstrated to date.

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CHAPTER 3

INTEGRATED DDL WITH MULTI-PATH APPROACH

In this chapter, we make improvements over the first attempt on the integrated DDL by using the multi-path approach. In the first integrated DDL, largest dispersion (~ 1 ns) is associated with the highest loss (~ 35 dB). The DDL implemented in this chapter solves this problem by splitting the signal into different frequency channels and assign each channel with designate group delay and gain profiles. The improved DDL exhibits 60% more dispersion than the first integrated DDL at the 6 dB loss point. We use the similar setup and implement the first on-chip Ku-Band nanosecond scale time-stretching (TS) system in a 130 nm CMOS process.

3.1 Multi-Path Approach

In the last chapter, we design and implement the first integrated DDL using the standard CMOS process. However, it has intrinsic drawback because it employs the dispersion near the cutoff frequency of the DA. The more the dispersion it provides, the more attenuation the signal will experience. In order to further improve the dispersion and provide gain compensation at higher frequencies, we propose to design the active DDL with a multi-path approach. The signal is first divided into several frequency channels (Figure 3-1 (a)) and each channel is assigned with different group delays while the amplitude information of the spectral contents is preserved (Figure 3-1 (b)). One can also adjust the gain profile of each channel to compensate for the unexpected attenuations. The overall transfer function of the active DDL is similar to a

bandpass filter (BPF) with designated group delay characteristic, which is linear in our case.

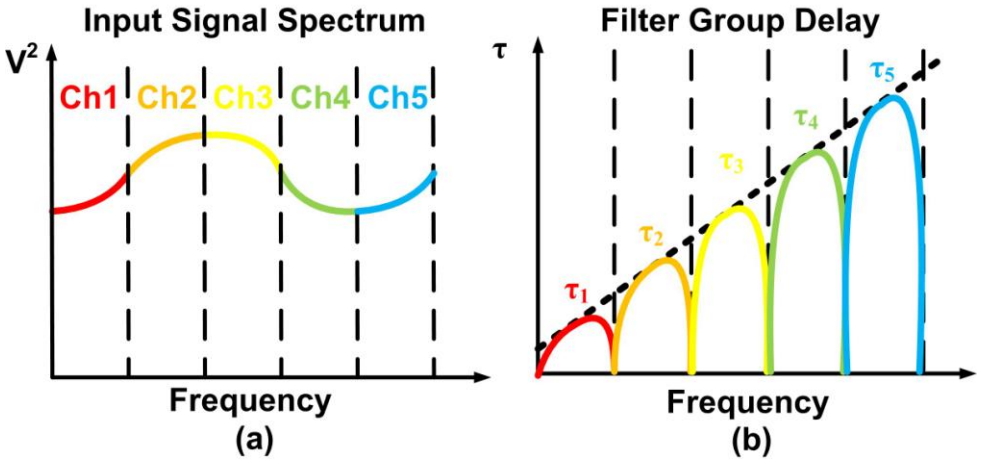

Figure 3-1 Illustration of multi-path approach: (a) the input signal is chopped into different frequency bands, (b) each channel is assigned with a specific group delay.

3.2 Circuit Design and Simulation

Our proposed design utilizes three paths, which is shown in Figure 3-2. Three bandpass filters (BPFs) [1] are employed for frequency division and three-stage cascaded distributed amplifiers (DA) of the last chapter are utilized to provide group delay assignment to each channel. The outputs of three channels are launched into the different locations of the cascaded distributed amplifiers (DA). The output of Channel 3, which contains higher frequency components, is sent through more stages of DAs, while the output of Channel 1, which contains lower frequency components, is sent through fewer stages of DAs. Compared to the previous active DDL, the multi-path design provides another degree of freedom in gain compensation. Since Channel 3 passes through most number of DA stages, it will experience more gain than Channel

1 and 2. Therefore, we use four stage BPFs for Channel 1 and 2 to compensate for the gain variations, while Channel 3 employs a three stage BPF. Furthermore, the output of Channel 3 is launched into the gate line of the DA while the outputs of Channel 1 and 2 are launched into the drain line. Therefore, BPF of Channel 3 is loaded with a 50Ω resistor (Figure 3-3 (a)), whereas the BPFs of Channel 1 and 2 employ an open drain structure to provide high output impedance (Figure 3-3 (b)). The BPFs are centered at 12.7 GHz, 14 GHz and 15.3 GHz individually with the same 3 dB bandwidth of 1.3 GHz [1]. The BPFs are realized by cascading multiple stages of cascode amplifiers loaded with LC tanks for the sake of gain and bandwidth.

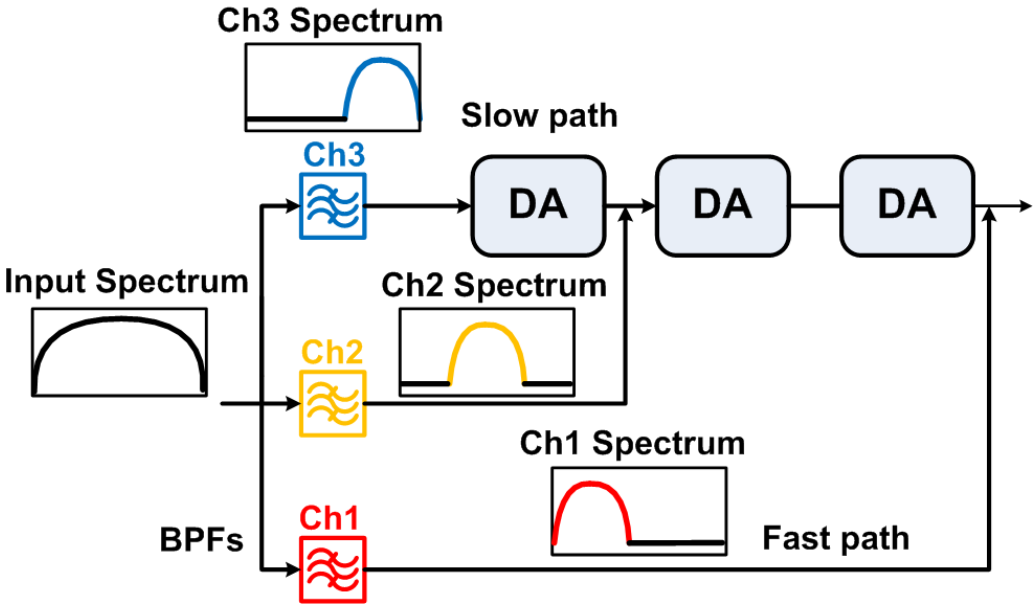

Figure 3-2 Improved DDL with three paths.

Fig. 3-4 shows the comparison in simulated gain and dispersion characteristic of both approaches. The multi-path approach improves the 6 dB bandwidth from 15 GHz to 15.5 GHz, and enhances the dispersion from 0.9 ns to 1.5 ns.

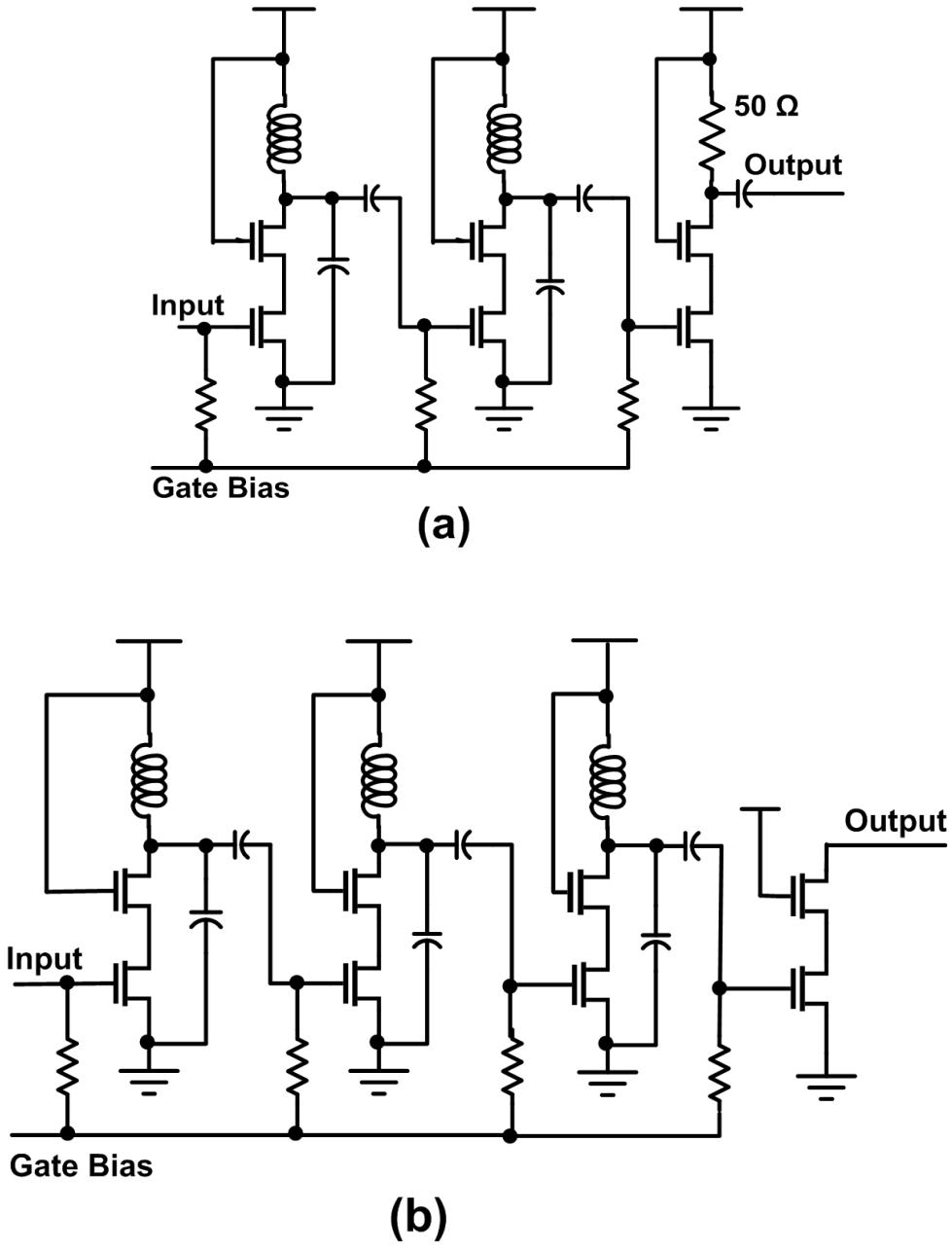

Figure 3-3 Circuit schematic: (a) BPF of Channel 3, (b) BPF of Channel 1 and 2.

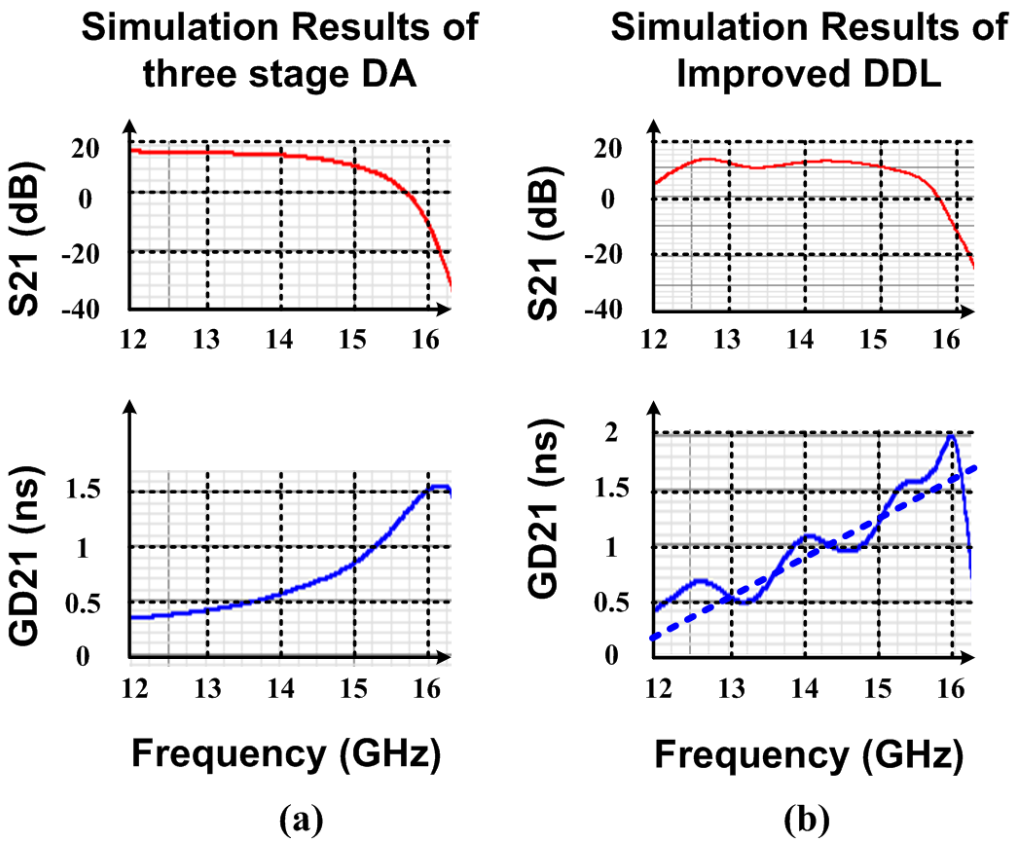

Figure 3-4 Comparison of gain (red) and group delay (blue) of the single path DDL using cascaded DAs (a) and improved multi-path DDL (b).

3.3 On-Chip Demonstration of Time Stretching (TS) System

3.3.1. Introduction of the TS system

In modern communication systems, signals of very high frequency and ultra-wide-bandwidth (UWB) are of great interest. It is a challenge for many conventional signal processing schemes to process these signals, for applications such as signal detection

and data conversion. One possible solution is to reduce the burden on conventional signal processing schemes by slowing down the signal with a time-stretching (TS) system. Such a system is capable of performing temporal manipulation on time-windowed or pulsed signals. A typical TS system can stretch and compress a pulse signal [2]. Stretching a signal in time will alleviate the burden on sampling rate, enabling a low frequency sampler to measure a high frequency signal [2], while compressing a signal will enhance signal to noise ratio (SNR) at the given transmitter power [3].

The idea of time-stretching originates from chirped radar design [3-5]. The technique is based upon the application of dispersive devices which implement a frequency dependent group delay. Figure 3-5 provides a basic idea of a typical TS system. The input signal is modulated with an up-chirped carrier, whose instant frequency increases with time, and then sent through the dispersive filter. Since different frequency components of the chirped signal experience different group delays in the dispersive filter, the output signal is expected to be a stretched version of the input signal.

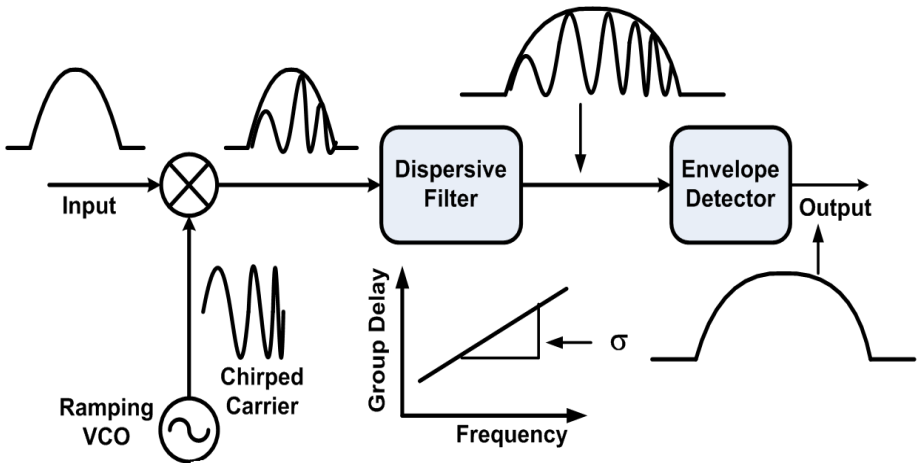

Figure 3-5 A schematic illustration of a typical time-stretching (TS) system. σ is the slope of the group delay (group delay variation over bandwidth).

While the TS system was first proposed by Caputi in 1970's [4], theory of the TS system can be traced back to 1960's [5]. The photonic TS system is famous for its ultra-fast high accuracy operation, in applications such as data conversion [6]. Various photonic TS ADCs have been implemented with highly dispersive devices such as dispersion compensated fiber (DCF) [6] and single mode fiber (SMF) [7], yielding a high time-bandwidth product (TBP) of the system. There is clear motivation for considering systems in the RF frequency range. Even though there are several state-of-the-art TS systems, none of them have achieved on-chip integration. Optical TS systems have the advantage of extremely large stretch factors (~250) and very fine resolution (~ 100 fs) [6]. However, they require costly and bulky elements including dispersion compensated fibers, a mode lock laser and electro-optic modulators [6-9]. The on-board microwave TS system, which employs microstrip Chirped Electromagnetic BandGap (CEBG) delay lines, is capable of stretching ultra-wideband (UWB) signals (3 GHz ~ 10 GHz) [2], but its size is on the order of the wavelength of the carriers (10 cm ~ 30 cm), and grows bigger as the dispersion becomes stronger [2]. The major challenge in implementing an on-chip TS system lies in the size optimization and loss compensation of the dispersive filter. The only previous integrated DDL, presented in last chapter, utilizes the dispersion near the cutoff frequency of the distributed amplifier (DA), and therefore realizes an increase in the group delay coupled with an associated increase in the loss [10]. In this chapter, we utilize bandpass filters (BPF) to compensate for the loss and further enhance the dispersion of the DA. With the improved integrated DDL, we successfully implemented the Ku Band TS system in 130 nm CMOS process.

3.3.2. Experimental Demonstration

We implement the on-chip TS system with the ramping VCO of the last chapter and the improved DDL of this chapter. In this section, two sets of experimental demonstrations are performed to prove the stretching functionality of the TS system. The measurement setup follows the system block diagram in Figure 3-5. A 1 ns input pulse with a sinusoidal pulse shape is generated. The shaped pulse has better performance over the square pulse because it exhibits a much smaller out of band ripple. The control signal (Vctrl) applied to the ramping VCO is synchronized with the input pulse signal. A 50 GHz oscilloscope is utilized to detect the envelope of the output signal. The first experiment demonstrates the stretching of a single pulse. Figure 3-6 (a) and (b) show the simulation results of the 1 ns pulse being stretched into a 2 ns pulse, while Figure 3-6 (c) and (d) exhibits the measurement results. The second experiment employs two subsequent sinusoid-shaped pulses as the input signal. Figure 3-6 (e) and (g) shows the simulation and measurement results of the two input pulses respectively. Both pulses have 1 ns pulse width and are separated by 1 ns in time. After going through the TS system, both pulses are stretched and separated by 2 ns, shown in Figure 3-6 (f) for simulation and Figure 3-6 (h) for measurement. The total temporal length of the two pulses is stretched from 2 ns to 3 ns, which corresponds to the dispersion of the improved DDL.

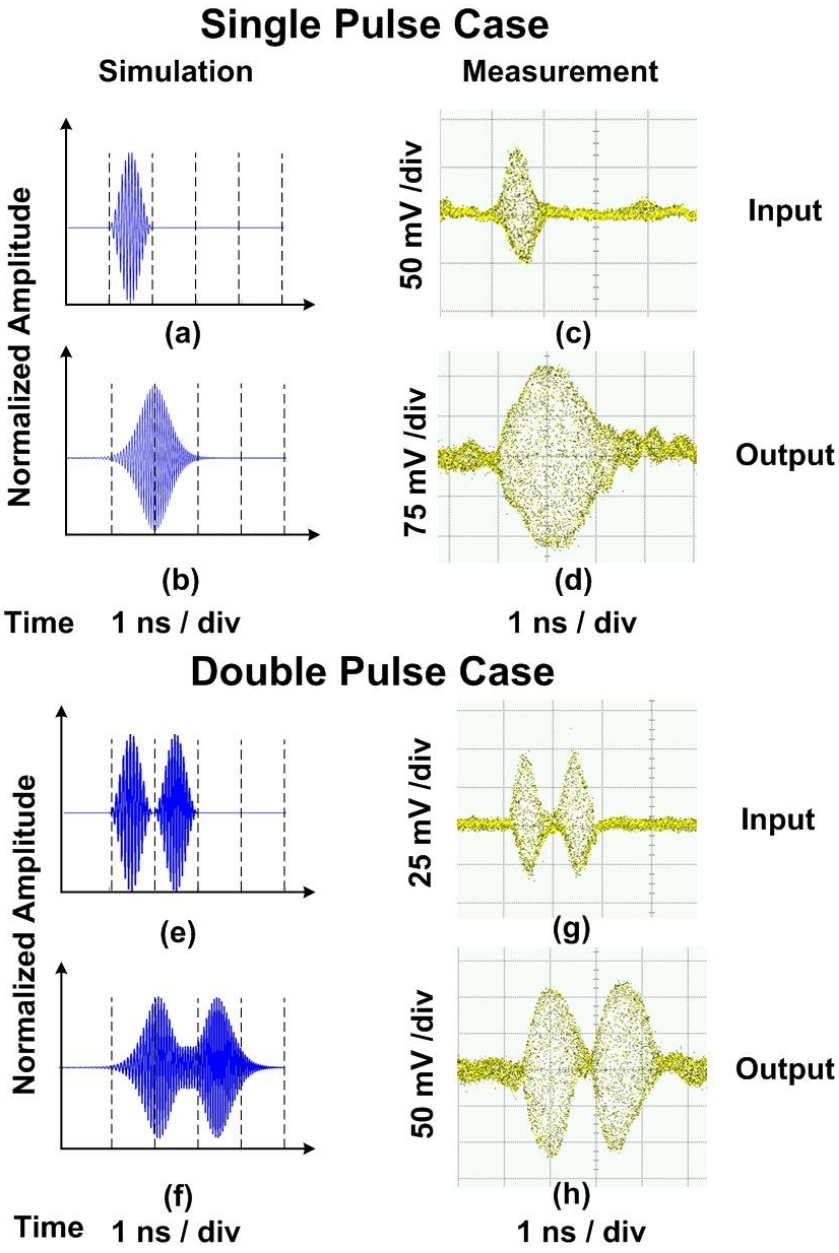

Figure 3-6 Top four figures show the single pulse case: (a) and (b) show the simulated input and output pulses, (c) and (d) show the measured input and output pulses. Bottom four figures show the double pulse case: (e) and (f) show the simulated input and output pulses, (g) and (h) show the measured input and output pulses.

3.4 Conclusion

This chapter presents an improved version of the first integrated DDL introduced in the last chapter. This improved DDL takes advantage of the multi-path approach and fully utilizes the dispersion provided by the dispersion-enhanced DA. Furthermore, we present an experimental implementation of the first on-chip Ku-band nanosecond TS system in 130 nm CMOS process with the total area of 1 mm x 4.5 mm (Figure 3-7). Compared with previous counterparts in chirped radar communication, UWB signal processing, and optical ADCs, this TS system achieves more stretching per unit size, enabling on-chip integration. It employs the active structure, the distributed amplifier (DA), to compensate for the on-chip loss. This TS system shows sufficient stretching ability on the pulsed signal. Furthermore, this system shows the potential to realize more complicated time scaling functionalities in addition to stretching. For instance, pulse compression is achievable if the input signal is modulated with a down-chirped carrier.

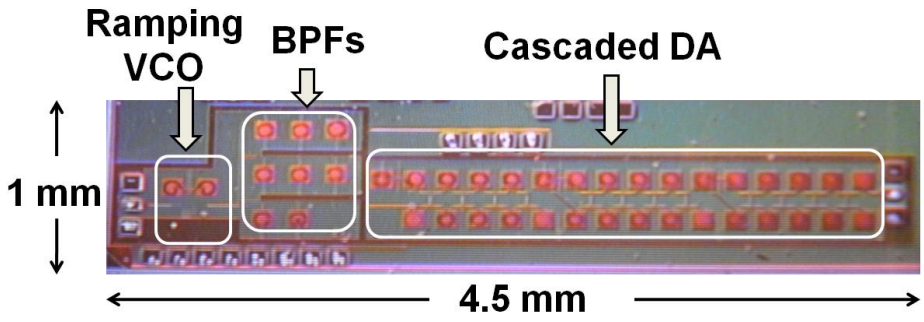

Figure 3-7 Integrated Ku-Band TS system.

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CHAPTER 4

THEORETICAL ANALYSIS OF THE TIME STRETCHING (TS) SYSTEM

The integrated DDLs presented in Chapter 2 and 3 have been used to implement the on-chip real-time analog signal processing blocks, known as time stretching (TS) system. Compared to the existing photonic TS system, the integrated TS system has much smaller time-bandwidth product (TBP) and exhibit higher distortion. The theory analysis presented in this chapter explores the DDL-based time stretching process and explains the impact of the TBP value on practical design considerations. The analysis of this chapter is based upon an ideal TS system with linearly chirped carrier and the DDL with perfect linear group delay and all pass amplitude characteristic. We also derive the time resolution of a general TS system using both principle of uncertainty and the Short Time Fourier Transform (STFT) method. This fundamental result enables a designer to understand the qualitative relationship between the TBP and the best possible resolution of the TS system.

4.1 Introduction

While the TS system was first proposed by Caputi in 1970's [1], theory of the TS system can be traced back to 1960's [2]. The photonic TS system is famous for its ultra-fast high accuracy operation because of the high TBP value it can provide. Han performed practical analysis of the photonic TS system including loss and dispersion of the optical fiber, modulation scheme, the effect of time-bandwidth product, etc [3, 4]. However, detailed theory of TS systems in the RF frequency range is lacking. Systems operating in this range have a much lower TBP and error and distortion

calculation is critically important. This chapter provides the theoretical basis of TS system operating in the RF frequency range and can be applied to TS in other operating ranges with proper adjustment. Furthermore, we address the important question of error or distortion in signals in the time domain as they pass from the input to output. We theoretically describe how energy in the input signal is converted to the output, and how well this energy (and therefore the signal envelope) can be resolved in time.

4.2 Theory of an Ideal TS System

In a TS system (Figure 4-1), a time-windowed or pulsed signal is sent through a dispersive device, mixed against a chirped carrier generated by a second dispersive device and then applied to a third dispersive device. The dispersion slopes σ1, σ2 and σ3 (group delay variation over bandwidth) determine the functionality of the TS system: stretching, compression, or time reversal [1]. Kolner provided the detailed mathematical derivation illustrating that the function of the first and third dispersive device in time domain resembles the spatial paraxial diffraction [5, 6]. The second dispersive device functions as a lens in time domain, which provides quadratic phase modulation to the incoming light wave. That is the reason why the second dispersive device is regarded as the time-lens [5, 6]. Similar technique is taken to realize the Chirped Electromagnetic BandGap (CEBG)-based TS system for UWB signals [7]. Photonic TS systems have a similar structure, utilizing the dispersion compensated fiber (DCF) as the dispersive device [8]. For our system, we minimize the number of the dispersive devices to reduce area and allow on-chip integration (Chapter 4).

We provide the theoretical basis and tools to analyze an ideal TS system with following assumptions. First, the ramping VCO generates a perfect linearly chirped carrier. Second, the DDL has all-pass amplitude response with perfectly linear group delay characteristic. Third, the input signal is a time windowed signal and it is

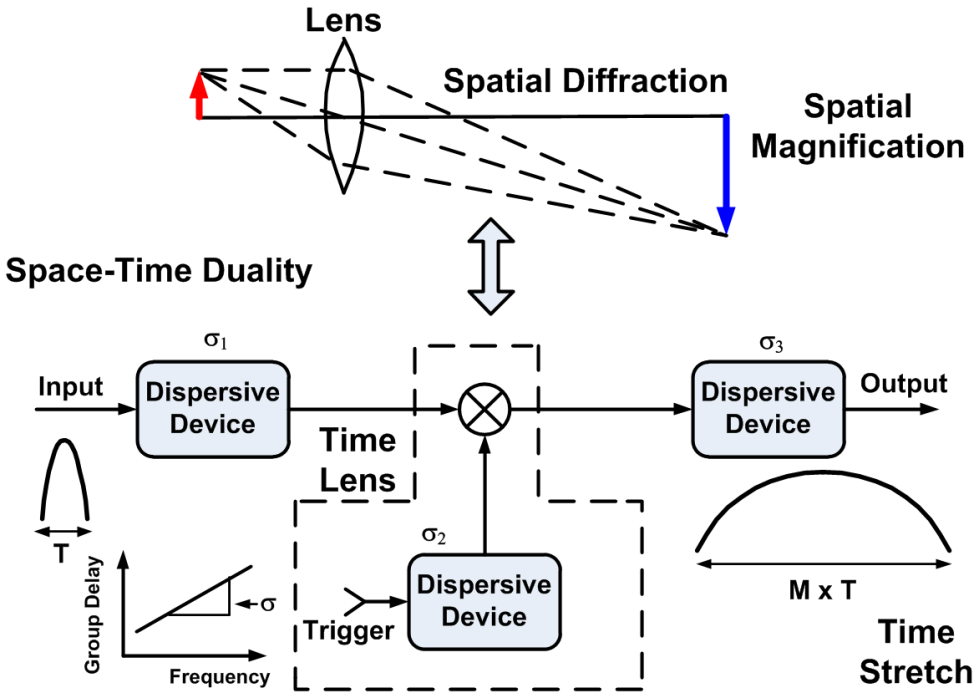


Figure 4-1 Space-Time Duality between spatial magnification and time stretch [5, 6].

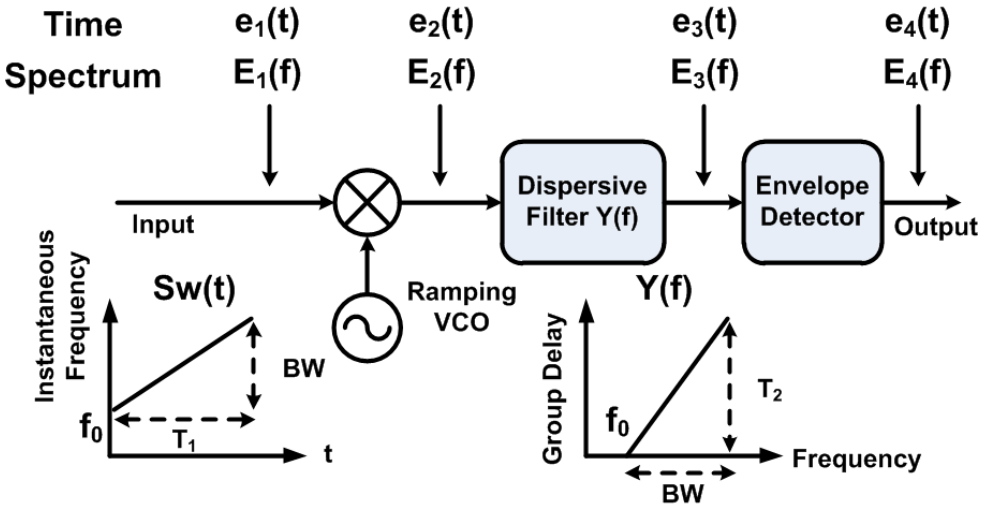


Figure 4-2 Proposed TS system with linear chirp modulation and linear dispersive delay line (DDL).

synchronized with the chirped carrier. Last, the carrier frequency range is much higher than the signal bandwidth. With these assumptions, we redraw Figure 3-5 as Figure 4-2 with the characteristics of both the chirped carrier Sw(t) in time domain and the DDL transfer function Y(f) in frequency domain, which can be represented as,

$$Sw(t) = e^{j2\pi\cdot\left(f_0 t+\frac{k_1 t^2}{2}\right)} \tag{4.1}$$

$$Y(f) = e^{-\frac{j\pi(f-f_0)^2}{k_2}} \tag{4.2}$$

$$k_1 = BW/T_1 \ , k_2 = BW/T_2 \tag{4.3}$$

As shown in Figure 4-2, T_1 represents the length of the input signal, and T_2 represents the dispersion of the DDL. Sw(t) is valid within the time window of input signal (0 to T_1) and Y(f) is valid within the operating frequency range (f_0 to f_0+BW). The signals at different locations of the system are represented in both time domain as $e_i(t)$ and frequency domain as $E_i(f)$ (i=1,2,3,4). Input signal $e_1(t)$ is modulated against the chirped carrier, generating $e_2(t)$, expressed as

$$e_2(t) = e_1(t)\cdot e^{j2\pi\cdot\left(f_0 t+\frac{k_1 t^2}{2}\right)} \tag{4.4}$$

$$E_2(f) = \int_{-\infty}^{+\infty} e_1(t)\cdot e^{j2\pi(f_0 t+\frac{k_1 t^2}{2})}\cdot e^{-j2\pi ft}dt \tag{4.5}$$

When signal $E_2(f)$ passes through DDL Y(f), we obtain $E_3(f)$,

$$E_3(f) = E_2(f) \cdot Y(f)$$

$$= \int_{-\infty}^{+\infty} e_1(\tau) \cdot e^{j2\pi\left(f_0\tau + \frac{k_1\tau^2}{2}\right)} \cdot e^{-j2\pi f\tau} d\tau \cdot e^{-\frac{j\pi(f-f_0)^2}{k_2}} \tag{4.6}$$

Applying inverse Fourier Transform, we can obtain $e_3(t)$,

$$e_3(t) = \int_{-\infty}^{+\infty} E_3(f) \cdot e^{j2\pi ft} df$$

$$= \int_{-\infty}^{+\infty} e_1(\tau) \cdot e^{j2\pi\left(f_0\tau + \frac{k_1\tau^2}{2}\right)} d\tau \int_{-\infty}^{+\infty} e^{j2\pi f(t-\tau) - \frac{j\pi(f-f_0)^2}{k_2}} df$$

$$= \int_{-\infty}^{+\infty} e_1(\tau) \cdot e^{j2\pi\left\{\left(f_0 t + \frac{k_2}{2}t^2\right) + \left[\left(\frac{k_1+k_2}{2}\right)\tau^2 - k_2 t\tau\right]\right\}} d\tau \tag{4.7}$$

$$\cdot \int_{-\infty}^{+\infty} e^{-\frac{j\pi}{k_2}[(f-f_0) - k_2(t-\tau)]^2} df$$

The integration in the frequency domain is a Fresnel Integration [1, 2], which can be calculated as,

$$\int_{-\infty}^{+\infty} e^{-\frac{j\pi}{k_2}[(f-f_0) - k_2(t-\tau)]^2} df = \sqrt{k_2} \cdot e^{-j\frac{\pi}{4}} \tag{4.8}$$

Then equation (4.7) can be simplified as,

$$e_3(t) = \sqrt{k_2} \cdot e^{j2\pi\left(f_0 t + \frac{k_2 t^2}{2}\right) - j\frac{\pi}{4}}$$

$$\cdot \int_{-\infty}^{+\infty} e_1(\tau) \cdot e^{j2\pi\left[\left(\frac{k_1+k_2}{2}\right)\tau^2 - k_2 t\tau\right]} d\tau \tag{4.9}$$

Up to now, the derivation is accurate without involving any approximation. However, calculation of the integral is complicated by the non-steady state characteristic of the signal. In order to calculate the integral term of equation (4.9), we rewrite the phase term as,

$$\varphi(\tau) = 2\pi\left[\left(\frac{k_1 + k_2}{2}\right)\tau^2 - k_2 t\tau\right]$$

$$= \pi(k_1 + k_2)\cdot\left[\left(\tau - \frac{k_2}{k_1 + k_2}t\right)^2 - \left(\frac{k_2}{k_1 + k_2}t\right)^2\right] \qquad (4.10)$$

Then equation (4.9) can be rewritten as,

$$e_3(t) = \sqrt{k_2}\cdot e^{j2\pi\left(f_0 t + \frac{k_1 k_2 t^2}{2(k_1+k_2)}\right) - j\frac{\pi}{4}} \cdot \int_{-\infty}^{+\infty} e_1(\tau)\cdot e^{j\pi(k_1+k_2)\cdot\left(\tau - \frac{k_2}{k_1+k_2}t\right)^2} d\tau \qquad (4.11)$$

The integral term in equation (4.11) resembles a Fresnel Integral except for the amplitude term $e_1(\tau)$. Numerical integration indicates that the major contribution of Fresnel Integral comes from the vicinity ($\pm\varepsilon$) around the point where the phase term equals zero, or equivalently, near the time point of

$$\tau_0 = \frac{k_2}{k_1 + k_2}t \qquad (4.12)$$

This point can also be obtained by setting $\varphi'(\tau) = 0$, regarded as the stationary phase point [2]. At the time locations far away from the stationary phase point, the phase term experiences fast variations and tends to cause cancellation with their adjacent

points in the integral. As a result, we can approximate the result by replacing the integral limit with$\tau_0 \pm \varepsilon$. The numerical integration of the Fresnel Integral indicates that ε should be proportional to $\sqrt{2\pi/\varphi''(\lambda)}$.

$$\varepsilon \propto \sqrt{\frac{2\pi}{\varphi''(\lambda)}} \tag{4.13}$$

With the previous assumption that the carrier frequency range is much higher than the input signal bandwidth, it is valid to conclude that the input signal changes much slower than the carrier. In the integral from $\tau_0 - \varepsilon$ to $\tau_0 + \varepsilon$, the input signal can be represented with $e_1(\tau_0)$. Therefore, we can rewrite the integral in equation (4.11) as follows,

$$e_1(\tau_0) \cdot \int_{\tau_0-\varepsilon}^{\tau_0+\varepsilon} e^{j\pi(k_1+k_2)\cdot\left(\tau-\frac{k_2}{k_1+k_2}t\right)^2} d\tau$$

$$\approx e_1(\tau_0) \cdot \sqrt{\frac{1}{k_1+k_2}} \cdot e^{+j\frac{\pi}{4}} \tag{4.14}$$

Substituting equation (4.13) and (4.14) back into equation (4.11), we can obtain the output signal represented with the input signal,

$$e_3(t) = \sqrt{\frac{k_2}{k_1+k_2}} \cdot e_1\left(\frac{k_2}{k_1+k_2}t\right) \cdot e^{j2\pi\left(f_0 t+\frac{k_1 k_2 t^2}{2(k_1+k_2)}\right)} \tag{4.15}$$

This analysis is a special case of the Principle of Stationary Phase (PSP) analysis, which is based on the same assumption that the integral of a signal modulated against

a fast varying phase can be represented with the integral of vicinity of the stationary phase point [2]. PSP analysis is capable of dealing with nonlinear chirp and nonlinear dispersion as well.

Here we introduce the stretch factor, represented as the ratio of output signal time duration over input signal time duration,

$$M = \frac{T_1 + T_2}{T_1} \tag{4.16a}$$

with equation (4.3), the stretching factor can be illustrated as,

$$M = \frac{k_1 + k_2}{k_2} \tag{4.16b}$$

Substituting equation (4.16) back into equation (4.15), we obtain,

$$e_3(t) = \sqrt{\frac{1}{M}} \cdot e_1\left(\frac{t}{M}\right) \cdot e^{j2\pi\left(f_0 t + \frac{k_1 t^2}{2M}\right)} \tag{4.17}$$

Equation (4.17) intuitively explains the stretching process, the input signal duration is stretched by a factor of M, the amplitude shrinks by a factor of $\sqrt{M}$, which agrees with the law of energy conservation. The chirp function is still linear with the identical bandwidth of the input signal, only the chirp rate reduces by a factor of M. After envelope detection, the output signal envelope is obtained,

$$e_4(t) = \sqrt{\frac{1}{M}} \cdot e_1\left(\frac{t}{M}\right) \tag{4.18}$$

4.3 Distortion Analysis of an Ideal TS System

As we mentioned before, the analysis of the previous section is also regarded as the Principle of Stationary Phase (PSP) analysis. Because the signal is not in steady state, we approximate the conversion from frequency to time by calculating around the stationary phase point where the signal contribution is greatest. The error of the approximation arises from equation (4.14) when moving the input signal out of the integral and representing it with its value at stationary phase point [2]. Haggarty successfully provided the error estimation to this approximation by performing series expansion with saddle point integration [9]. The error bound is given in percentage of the ideally stretched signal in equation (4.18),

$$S_e = j \cdot \frac{1}{2} \cdot \frac{e_1''(\tau_0)}{e_1(\tau_0)} \cdot \frac{1}{|\varphi''(\tau_0)|} \tag{4.19}$$

$$\varphi''(\tau_0) = 2\pi(k_1 + k_2)$$

where τ_0 is the stationary phase point shown in equation (4.12), and $\varphi''(\tau_0)$ stands for the second derivative of the phase term of the integral in equation (4.9) [9]. In order to minimize the error, we need to choose a smooth signal whose $e_1''(\tau_0)/e_1(\tau_0)$ is relatively small. This explains the errors and distortions associated with stretching of an input square pulse [2, 10]. Apart from this requirement, a square pulse passed through a TS system is distorted because it has large skirts in frequency domain exceeding the operating frequency range of the chirped carrier and the DDL [2, 10]. The distortion of the square pulse worsens with the decreasing time-bandwidth product (TBP) [11]. Therefore, the best input signal pulse shape to exploit the benefit of the TS system should be smooth and frequency limited. The best option would be Gaussian pulse. In practice, it is very difficult to construct a Gaussian signal, instead,

we need to use other plausible signals as replacement. A straightforward choice is a sinusoid. Complete analysis concerning all the error terms with edge effects is beyond the scope of this paper. In the rest of the chapter, we take sinusoid signal as the input signal of the TS system.

Equation (4.19) indicates that the error bound exhibits time dependence. It is necessary to analyze the distortion raised by the stretching process. In order to do that, we take the FFT of the stretched pulse envelope with the input of a sinusoid signal. The distortion factor is evaluated as the ratio of the desired signal intensity over the total intensity of undesired spectral components (higher order harmonics). The distortion factor shown in Figure 4-3 is translated into dB. A higher distortion factor results in less distortion in the output signal. Here we consider another variable, time-bandwidth product (TBP). In our system, there are two blocks characterized by TBP, one is at the chirped carrier generation and the other is at DDL. These are defined as follows,

$$\begin{cases} \mathrm{TBP}_1 = \mathrm{T}_1 \cdot \mathrm{BW} = \mathrm{k}_1 \cdot \mathrm{T}_1^2 \\ \mathrm{TBP}_2 = \mathrm{T}_2 \cdot \mathrm{BW} = \mathrm{k}_2 \cdot \mathrm{T}_2^2 \end{cases} \tag{4.20}$$

Since distortion analysis gives more information than error analysis in the dynamic operation of the TS system, we perform the distortion analysis with respect to different TBP_1. The distortion factor increases with an increasing TBP_1. A higher TBP_1 leads to more cycles of the chirped carrier inside the signal envelope. As a result, more details of the signal envelope can be described by the chirped carrier. When TBP_1 exceeds a certain value (~200 in our case) the distortion factor will experience saturation around 62 dB. This sets the limit for the integrated TS system if we intend to use it for data conversion. Considering the analysis assumes a noiseless system, the signal to noise and distortion ratio will be worse in the presence of the noise. By inspecting the

distortion, we can estimate the upper limit of the effective number of bits (ENOB) a TS-ADC can achieve.

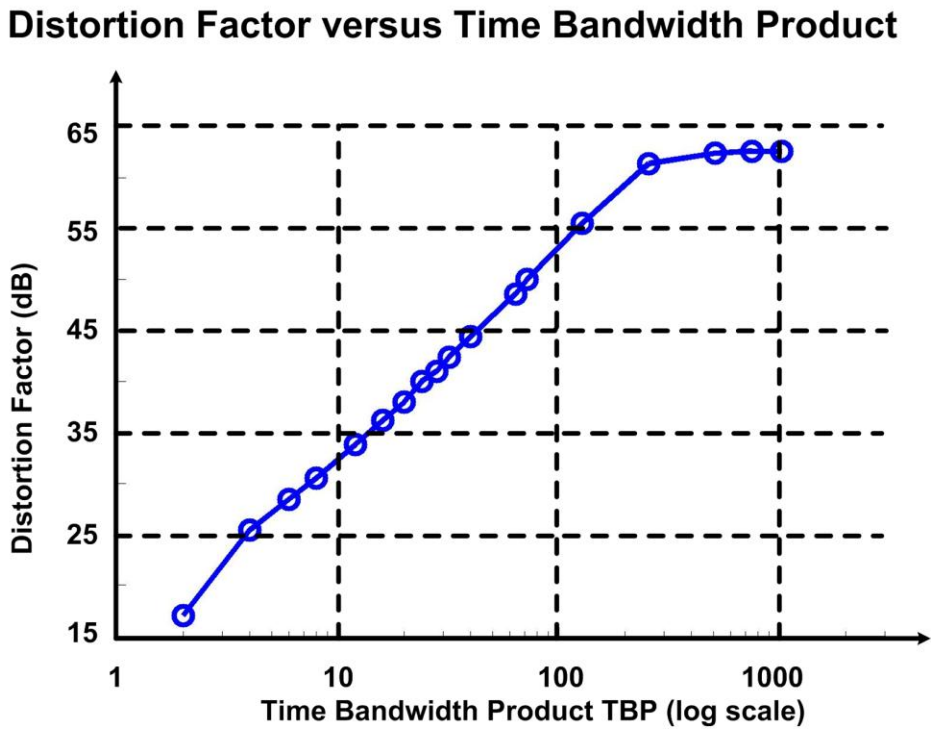


Figure 4-3 Distortion analysis of the ideal TS system.

Since our system has the TBP of 4 with the distortion of 25 dB, the upper limit of the ENOB of our system is 3.8 bits. One thing to mention here is that the carrier frequency range of the TS system analyzed in this work is limited to RF and microwave range. It can be utilized to predict the photonic TS system, but the analysis requires more practical considerations such as the dispersion characteristics of the optical fiber [3, 4, 8]. Furthermore, Figure 4-3 shows that the distortion changes with TBP at a slope of 20 dB / decade, which means TBP has the linear relationship with the distortion of system.

4.4 Time Resolution Analysis of the Ideal TS System

In the previous section, we analyze the error and distortion of the ideal TS system, in this section we perform the analysis focusing on the time domain of the signal. This is critically important for TS applications since understanding how accurately the energy at the input is resolved at the output in time will determine the utility of the system. Previous analysis has not rigorously described this. Kolner [3] and Han [5] only commented on the time-resolution or time-aperture of the photonic TS system, which has ~100 THz of carrier frequency and very large TBP but did not provide analysis. This work deals with the time resolution of the general TS system operating at a lower frequency range with medium or low TBP. The results can also be applied to photonic TS system with proper adjustment. Equation (4.19) indicates that the input signal, with proper chirp modulation, and the stretched signal form a pair of Fourier Transforms [2, 5]. This can be more obvious if we define a new variable f_2 as,

$$f_2 = k_2 t \tag{4.21}$$

Due to equation (4.3), $1/k_2$ represents the dispersion slope and f_2 has the unit of Hz. Rewriting equation (4.9) with this newly defined variable, we obtain,

$$e_3(t) = e_{3M}(f_2)$$

$$= \sqrt{k_2} \cdot e^{j2\pi(f_0\frac{f_2}{k_2}+\frac{f_2^2}{2k_2})-j\frac{\pi}{4}} \cdot \int_{-\infty}^{+\infty} e_{1M}(\tau) \cdot e^{-j2\pi f_2 \tau} d\tau \tag{4.22}$$

where $e_{1M}(\tau) = e_1(\tau) \cdot e^{j2\pi\left(\frac{k_1+k_2}{2}\right)\tau^2}$

As can be seen from the equation (4.22), e_3 and e_{3M} have similar waveform shape, e_{3M} is connected to e_3 with a scale factor of $1/k_2$. k_1 represents the chirp rate of the

input chirped pulse and $1/k_2$ represents the dispersion slope of the DDL. The signal $e_{1M}(\tau)$ and $e_{3M}(f_2)$ form a pair of Fourier Transforms. The signal $e_{1M}(\tau)$ has the envelope of the input signal and the quadratic phase term indicating a chirping rate of k_1+k_2, in other words, the instantaneous frequency is changing along the time axis. A typical analysis that provides solutions to the signal of this category is joint time-to-frequency analysis. Due to the principle of uncertainty in the Fourier Transform of equation (4.22) [12],

$$2\pi\Delta f_2\Delta\tau \geq \frac{1}{2} \tag{4.23}$$

With equation (4.23), we obtain,

$$2\pi k_2\Delta t\Delta\tau \geq \frac{1}{2} \tag{4.24}$$

Substituting equation (4.3) into equation (4.24) leads us to the following relation,

$$\Delta t\Delta\tau \geq \frac{1}{4\pi k_2} = \frac{T_2}{4\pi BW} \tag{4.25}$$

Usually the principle of uncertainty can be illustrated with the time-frequency resolution cells [12]. Notice this is a stretching process, the input signal $e_1(\tau)$ is stretched into the output signal $e_3(t)$ by the stretching factor of M, expressed in equation (4.16). In this case, we can modify the time-frequency resolution cells to input time, output time resolution cells. The principle of uncertainty is very important in determining the time resolution of the TS system and it can be explained as follows. For a specific point on the input signal $e_1(\tau)$, we are unable to point out the corresponding point on the output signal $e_3(t)$. Instead, the energy within a certain time slot $\Delta\tau$ of the input signal gets stretched into the correspondent time slot Δt of the output signal. Even though the Fourier Transform pair contains carrier information,

the envelope detection will capture the energy inside each time slot which is more critical for time stretch systems which seek to improve sampled performance. Therefore, the lower limit of the time slot of the input signal is defined as the time resolution of the TS system. Since the output signal is the stretched version of the input signal, we can obtain the following scaling equation between the input and output time axis,

$$t = M \cdot \tau \tag{4.26a}$$

$$\Delta t = M \cdot \Delta\tau \tag{4.26b}$$

From equation (4.25) and (4.26),

$$\Delta\tau^2 \geq \frac{T_2}{4\pi \cdot M \cdot BW} \tag{4.27}$$

With equation (4.16), we can provide the estimation of the time resolution,

$$\Delta\tau \geq \frac{1}{2} \cdot \sqrt{\frac{T_{eff}}{\pi \cdot BW}} \tag{4.28}$$

where $T_{eff} = T_1 T_2/(T_1 + T_2)$.

In this case, the input signal can be divided into a number of slots with given time resolution, expressed as,

$$N = \frac{T_1}{\frac{1}{2} \cdot \sqrt{\frac{T_{eff}}{\pi \cdot BW}}} = 2 \cdot \sqrt{\pi \cdot TBP_1 \cdot \left(1 + \frac{T_1}{T_2}\right)} \tag{4.29}$$

We can examine the time resolution $\Delta\tau$ and the number of time slots N with different stretching time T_2 (assuming T_1 is fixed). When $T_2 << T_1$, $T_{eff} = T_2$, T_2

dominates T_{eff}. In the extreme case when $T_2 = 0$, there is no stretch effect at all, the output signal is identical to the input signal, therefore, the time resolution can be infinitely small and the number of time slots (represented as N in the following sections) can be infinitely large. As T_2 increases, the time resolution increases and N decreases. When $T_2 >> T_1$, T_1 dominates T_{eff} and the time resolution has the upper bound limitation of

$$\frac{1}{2} \cdot \sqrt{\frac{T_1}{\pi \cdot BW}} = \frac{1}{2} \cdot \sqrt{\frac{1}{\pi \cdot k_1}} \tag{4.30a}$$

the number of time slots has the lower bound limitation of

$$2 \cdot \sqrt{\pi \cdot \mathrm{TBP}_1} \tag{4.30b}$$

This is a very interesting feature of the TS system stating that even if the TS system employs a DDL with very large dispersion, the time resolution of the TS system is determined by the chirp rate (k_1) of the chirped carrier and the number of time slots (N) is determined by the time-bandwidth product (TBP_1) of the chirped modulated input signal. Figure 4-4 shows the change of the time resolution and N with respect to different stretching time (DDL delay variance) T_2. Like the simulation in the previous section, the parameters are chosen based on the integrated TS system, T_1=1 ns, BW=4 GHz, T_2 ranges from 0.2 ns to 5 ns.

A larger TBP_1 yields better time resolution to both input signal and stretched signal. One reason is that TS system with larger TBP_1 contains more carrier cycles inside the signal envelope, which is capable of carrying more information and better characterizing the input signal envelope as compared to the lower TBP_1 situation [4]. This is also the reason why photonic TS systems perform better than their microwave counterparts.

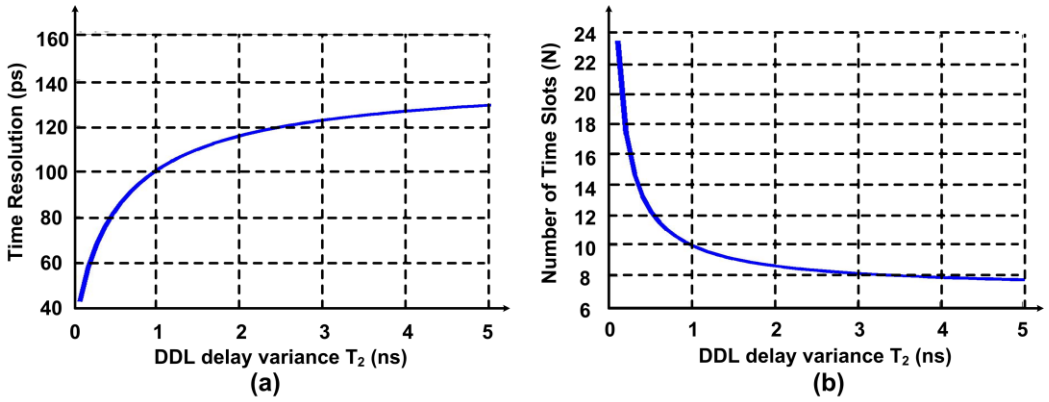


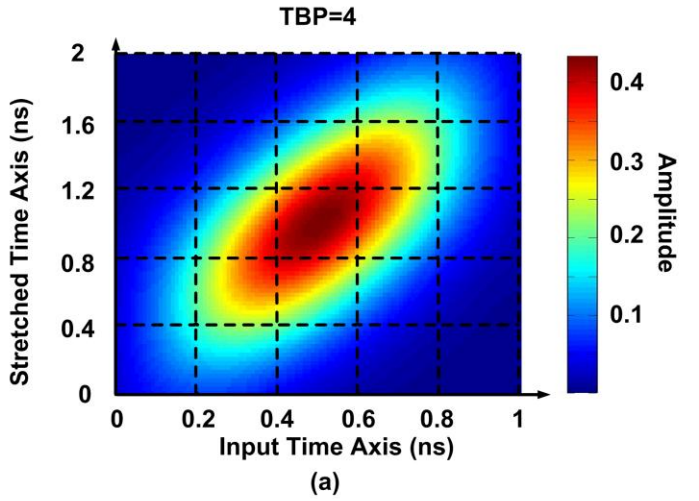
Figure 4-4 (a) Time resolution and (b) number of time slots N changes versus DDL delay variance

Time-frequency representation (TFR) combines the conventional Fourier Transform signal spectrum information together with the corresponding time locations of various spectral components. A typical TFR analysis is the Short Time Fourier Transform (STFT). Instead of performing the Fourier Transform directly to the input signal, STFT employs a sliding window, usually Gaussian shape, to choose different portions of the input signal along the time axis, and perform the Fourier Transform individually [12, 13]. As a result, multiple spectrums with respect to different time locations can be obtained. Instead of a one dimensional spectrum containing only frequency domain information from conventional Fourier Transform, STFT will generate a two dimensional spectrum with both time and frequency information [14].

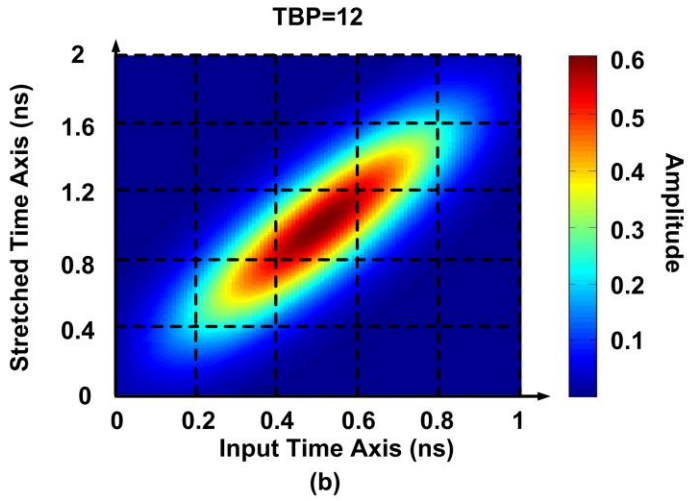
The two dimensional spectrum is usually regarded as Spectrogram, which is capable of providing the information of time-frequency mapping of the input signal. In the TS system, as explained previously, the input signal and the stretched signal forms a pair of Fourier Transform [15]. A physical explanation of the time stretching process is that the energy in a particular time slot of the original signal gets stretched and appears

in the corresponding time slot of the stretched signal. Utilizing STFT, we can allocate a specific time slot in the original signal with its corresponding time slot in the stretched signal. In this work, we use amplitude, not power, to characterize the TS system in the spectrogram because the analysis is taken out in amplitude domain. Figure 4-5 represents the STFT of the TS system, the x axis is the input time axis, from 0 to 1 ns, and the y axis is the output time axis, from 0 to 2 ns. Three TS system with TBP_1 of 4, 12 and 40 are presented. As TBP_1 increases, the shape of the STFT gets squeezed towards the line y=2x, representing the 2X stretching process. Moreover, the maximum amplitude value of spectrogram increases as well. This is because the resolution decreases and number of slots increases with an increasing TBP_1, providing a more accurate allocation from input signal to output signal.

We can apply the theoretical analysis of this chapter to explain the measured output signals of the last chapter (Figure 3-6). From the distortion analysis, we can obtain the highest distortion factor of 25 dB (Figure 4-3) with TBP of 4. In the test setup, we utilize the equivalent time oscilloscope for envelope detection. By inspecting the envelope, we can estimate the distortion of the output signal envelope. The estimated distortion of the stretched single pulse is 12 dB, it is worse than the estimated distortion of an ideal TS system with same TBP (4) in Figure 4-3 because the integrated TS system suffers from the non-idealities of including the noise of the active components, imbalance of differential-to-single ended AM modulation, nonlinearities of the chirp generation and DAs, ripples in gain and group delay, etc. Due to the limitation of the quantitative measurement of the uncertainty, we can explain the time resolution of the integrated TS system with a qualitative perspective. The input signals of both single pulse case and double pulse case exhibit sharp peaks.


TBP=4
Stretched Time Axis (ns)
Input Time Axis (ns)
Amplitude
0
0.2
0.4
0.6
0.8
1
1.2
1.6
2
0.1
0.2
0.3
0.4

(a)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Input Time Axis (ns)
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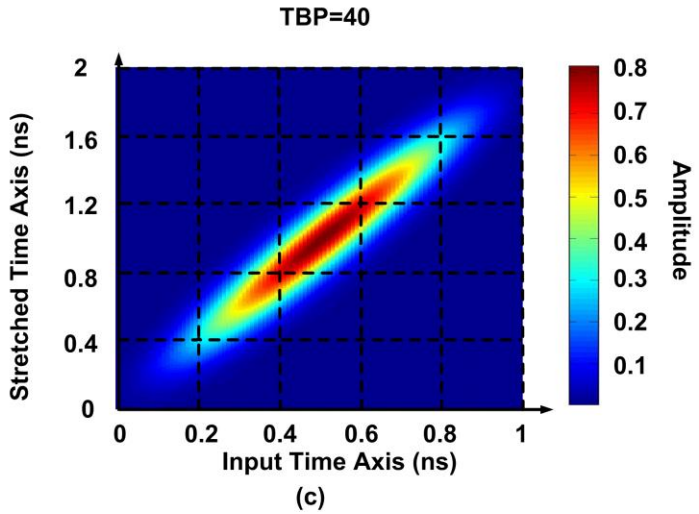
0.2
0.4
0.6
0.8
1
1.2
1.6
2
0.1
0.2
0.3
0.4
0.5
0.6

(b)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Input Time Axis (ns)
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0.4
0.6
0.8
1
1.2
1.6
2
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8

(c)

Figure 4-5 Time resolution analysis utilizing Short Time Fourier Transform (STFT) with respect to different time-bandwidth product (TBP).

If the TS system is designed with a relatively large TBP (as shown in Figure 4-5 (c)), it is capable of capturing more details of these peaks, yielding the output signals with sharp peaks as well. While on the other hand, if the TS system is designed with a relatively low TBP (as shown in Figure 4-5 (a)), it is incapable of capturing sharp peaks, and the output peaks will be relatively flat as compared to the input. Since our integrated TS system has relatively low TBP, the time resolution is relatively low, thus the peaks of both output signals exhibit smooth and flat tops. If we were to have larger TBP, we can expect the top part to be sharper and to follow the ideally stretched pulse more accurately.

4.5 Conclusion

In this chapter we developed the theory analysis of a general TS system, providing the estimation of error, distortion and time resolution. It also provides a qualitative explanation of the relationships between these features (error, distortion and time resolution) and the time-bandwidth product (TBP). Even though the analysis is based upon operation in the RF range, it can be modified and applied to photonic TS system. Since photonic TS system is usually equipped with large time-bandwidth product (~100 to 1000), it is still favorable to use photonic TS system for high accuracy operations such as data conversion. RF TS system, on the other hand, is limited by its time bandwidth product (~10) in performing high accuracy operations. It can be employed for other applications which have lower requirements on the accuracy, such

as pulse detection in UWB range. It can also be utilized for data conversion with lower accuracy.

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CHAPTER 5

RECONFIGURABLE DDL AND REAL TIME SPECTRUM ANALYSIS

This chapter provides the theoretical analysis and physical implementation of a reconfigurable integrated dispersive delay line (DDL) in the IBM 8RF 130 nm CMOS process. Different categories of DDLs have been analyzed and we find that all reflective-type quasi-periodic DDLs share the same type of governing equation, known as the Riccati equation. Moreover, all of these DDLs can be modeled as transversal filters. With this intuition, we show that the reverse gain port of a distributed amplifier (DA) can be used to realize the integrated reconfigurable transversal filter. We successfully demonstrate a reconfigurable integrated DDL that is capable of achieving multiple transfer functions by altering the tap coefficients and polarities. We also provide the experimental demonstration of the real time spectrum analysis with reconfigurable integrated DDL.

5.1 Introduction

The integrated DDL realized in Chapter 2 employs the dispersion near the cutoff frequency of the DA. Even though the integrated DDL realized in Chapter 3 makes significant improvements, the non-idealities in the dispersion characteristic and the gain profile are still inevitable. In order to solve this problem, we reinvestigate the existing DDLs and find out that most of them share two common characteristics. First, most of the existing DDLs are reflective type DDLs, in which the input wave is reflected at multiple locations along the DDL. All of the reflected waves add up at the input port and can be separated out by a circulator. Second, most of the existing DDLs

have the quasi-periodic structure, meaning their structure or impedance profile is changing with a varying period. We discover that the reflective type DDL can be modeled with the non-uniform transmission line. Furthermore, we note the connection between the structures of the non-uniform transmission line and its reflective transfer function at the input port [1] and find out that this duality can be used to derive an equivalent transversal filter for any non-uniform transmission line. Therefore, as long as we are given the structure of the non-uniform transmission line, we can obtain its impulse response through the Riccati equation. This in turn leads us to the design of a transversal filter by providing the tap coefficients and polarity. We exploit this idea and build an on-chip reconfigurable transversal filter with tunable coefficients as an alternative to a static non-uniform transmission line. The major achievement of this chapter as compared to the previous integrated DDL [2-4] is the reconfigurability. By changing the tap coefficients and polarities, we are able to realize the multiple transfer functions with a single chip. However, if we employ the existing approaches, e.g. microstrip lines [5-7], multiple static non-uniform lines are required to realize these functions. Since each non-uniform line requires individual design and fabrication process, the complexity of designing multiple non-uniform lines increases greatly as the number of desired transfer functions increases. With the approaches introduced in this chapter, we can achieve the reconfigurable integrated transversal filter while the other existing approaches, e.g. microstrip lines [5-7] cannot be adjusted post fabrication. We also present the first on-chip demonstration of real time spectrum analysis with the reconfigurable integrated transversal filter.

5.2 Theory Analysis of Dispersive Delay Lines (DDLs) Based on Non-Uniform Transmission Lines

There are various categories of dispersive delay lines (DDL) including surface acoustic wave (SAW) [8, 9], superconductive [10, 11], non-uniform transmission line based on coplanar waveguide (CPW) and microstrip [1, 5, 6, 12-23]. One characteristic in common is that their structures can be modeled with a general almost-periodic non-uniform transmission line [24]. Starting from the analysis of the non-uniform transmission line shown in Figure 5-1, we are able to obtain a single first order differential equation to fully describe the frequency responses of the non-uniform transmission lines from their structure. The equation is also known as Riccati Equation, expressed as follows,

$$\frac{d\rho}{dx} + \frac{1}{2} \cdot \frac{d\ln Z_0}{dx} \cdot (1 - \rho^2) - 2\gamma \cdot \rho = 0 \qquad (5.1)$$

where ρ is the reflection coefficient along the line, Z_0 is the impedance profile, γ is the propagation constant, consisting of the real part α and the imaginary part β. The reflection coefficient ρ is a function of frequency f and location x along the non-uniform line. As in the previous work on the non-uniform DDL, ρ in this paper specifically refers to the reflection coefficient at the input port. We also discover that all of the DDLs can be traced back to their unique Riccati Equation, and can be modeled with the corresponding non-uniform transmission line shown in Figure 5-1. The frequency response is determined from the impedance profile through the Riccati Equation. The response of the non-uniform transmission line can be explained utilizing either Maxwell's Equations or Coupled Mode Theory. We can divide the non-uniform line into discrete sections with uniform impedance. When the

propagating wave sees the varying impedance at each interface of the adjacent sections, the coupled counter-propagating wave is generated. The coupling coefficient is a function of location x, represented as,

$$K(x) = -\frac{1}{2} \cdot \frac{1}{Z_0} \cdot \frac{dZ_0}{dx} = -\frac{1}{2} \cdot \frac{dlnZ_0}{dx} \tag{5.2}$$

All of the coupled counter-propagating waves are summed up at the input port of the non-uniform line. Therefore, the non-uniform line can also be modeled with a transversal filter or finite impulse response (FIR) filter.

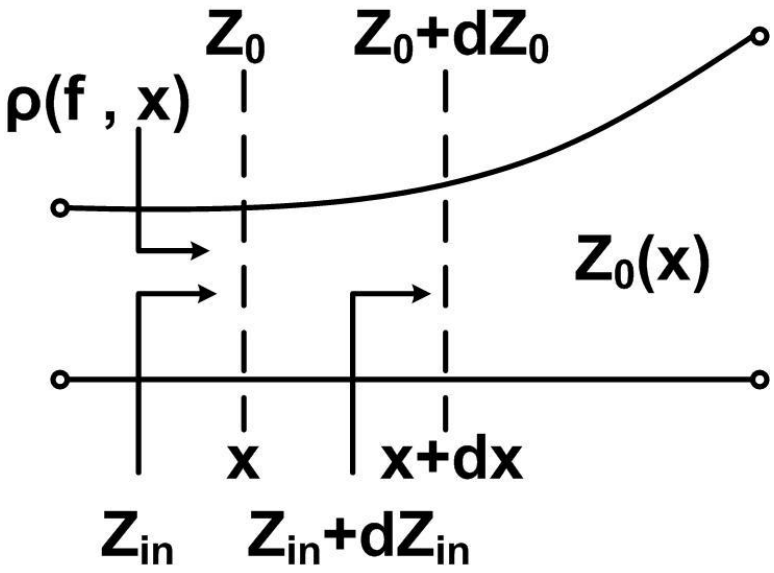

Figure 5-1 Non-Uniform Transmission line, $Z_0(x)$ is the characteristic impedance along the line, Z_{in} is the impedance looking into the far end of the line.

5.3 Riccati Equation and Its Solution

The Riccati equation completely characterizes the non-uniform transmission line given its impedance profile. As discussed in [1, 25], not all the Riccati equations have closed form solutions. If the impedance variation is relatively small, the Riccati equation can be simplified, and is possible to have a closed form solution. If the impedance variation is not small, we need to employ numerical integration to solve the Riccati equation [1, 5].

5.3.1. Small Reflection Approximation and Simplified Riccati Equation

As shown in Figure 5-1 and last section, we can divide the non-uniform transmission line into multiple sections. Qualitatively speaking, when the impedance profile exhibits small variation, the reflection at the interface of the adjacent section is very small. As a result, the reflection coefficient ρ at each interface is very small as well. Therefore, the $(1-\rho^2)$ term can be replaced with unity. Together with equation (5.2), the Riccati equation (5.1) can be simplified as,

$$\frac{d\rho}{dx} = 2 \cdot \gamma \cdot \rho + K(x) \tag{5.3}$$

From the practical standpoint, the $(1-\rho^2)$ term takes into the consideration of the loss on the forward traveling wave due to the reflections occurring at every section interface. Here we assume that the transmission line is lossless and the loss of the forward traveling wave is totally induced by the reflection.

5.3.2. Solution to the Simplified Riccati Equation

With the assumption of small reflection or weak coupling, the Riccati equation (5.1) can be simplified to equation (5.3) neglecting the secondary reflection term. The simplified Riccati equation (5.3) is a first order differential equation which can be solved with a standard procedure [26]. Here are some of the assumptions, first, the non-uniform line ranges from -L/2 to L/2, and we assume that the end point L/2 is properly terminated for impedance matching. Second, the non-uniform transmission line is lossless, and the propagation constant can be represented with jβ.

$$\rho(\beta) = \frac{-\int_{-\infty}^{+\infty} K(x_1) \cdot e^{-2 \cdot j\beta x_1} dx_1}{e^{j\beta L}} \tag{5.4}$$

The integration limit can be from [-L/2, +L/2] to [-∞, +∞] because K(x) is zero in the region beyond the non-uniform line region. The ratio 2 shows up in the phase term because the reflected wave travels twice the distance as the impedance profile location. Now we need to define a scaled function of K(x) as,

$$K_1(2x) = K(x) \tag{5.5}$$

Substitute equation (5.5) into equation (5.4), we obtain another expression of equation (5.4)

$$2 \cdot \rho(\beta) \cdot e^{j\beta L} = \int_{-\infty}^{+\infty} -K_1(2x_1) \cdot e^{-j\beta(2x_1)} d(2x_1) \tag{5.6}$$

If we replace $2x_1$ with another variable x_2, equation (5.6) is transformed into,

$$2 \cdot \rho(\beta) \cdot e^{j\beta L} = \int_{-\infty}^{+\infty} -K_1(x_2) \cdot e^{-j\beta x_2} dx_2 \tag{5.7}$$

This way, we find out that the scaled function $-K_1(x)$ and $2 \cdot \rho(\beta) \cdot e^{j\beta L}$ form a pair of Fourier Transforms. The Fourier Transform pair described by equation (5.7) utilizes the propagation constant β and location x as a pair of variables. This pair works well for the non-uniform line design, but not for the transversal filter design, which utilizes discrete delay blocks and gain cells to provide delay and reflection. Therefore, we need to rewrite the Fourier Transform Pair in equation (5.7) with the variables of time t and radian frequency ω. The distance x and the propagation constant β are related to the time t and radian frequency ω via the following equations,

$$\beta = \frac{\omega}{v} \tag{5.8a}$$

$$v = \frac{c}{\sqrt{\varepsilon_r}} \tag{5.8b}$$

$$t = \frac{x}{v} \tag{5.8c}$$

where v is the speed of the EM wave propagation, c is the speed of light in free space, and ε_r is the relative permittivity of the printed circuit board dielectric material. Combining equations (5.7) and (5.8), we can derive the Fourier Transform Pair with time and radian frequency. In this way, we can obtain two sets of Fourier Transform Pairs from equation (5.7) with two sets of variables,

$$-K_1(x) \overset{FT}{\leftrightarrow} 2 \cdot \rho(\beta) \cdot e^{j\beta L} \tag{5.9a}$$

$$-K_1(t) \overset{FT}{\leftrightarrow} 2 \cdot \rho(\omega) \cdot e^{j\omega L} \tag{5.9b}$$

The two sets of Fourier Transform Pairs can be utilized to describe the same non-uniform transmission line. If the design is based upon the coupling coefficients along the locations of the non-uniform transmission line, we can use equation (5.9a), if the

design is based upon the impulse response in time domain, we can use the equation (5.9b). The two sets can be transferred to each other with the equation (5.8). This Fourier Transform relationship is also introduced in [16, 17, 27-29].

5.3.3. Numerical Integration Approach to Solve the Riccati Equation

When the impedance profile experiences large variance and the small reflection approximation no longer applies. In this case, the Riccati equation cannot be simplified into equation (5.3). As discussed earlier this section, not all the Riccati equations have the closed form solutions, therefore, we need to utilize numerical integration to obtain the reflection coefficient. We start with the same boundary condition that the output (x=-L/2) of the non-uniform transmission line is terminated with 50 Ω impedance, indicating no reflection at this particular point. The non-uniform transmission line is divided into multiple sections, and the reflection coefficient $\rho(\omega)$ can be numerically integrated section by section from the output interface (x=-L/2) to the input interface (x=L/2).

5.4 Design Procedure of Integrated DDL

So far we have proved that any arbitrary non-uniform line can be described with its unique and correspondent Riccati equation. Given a specific impedance profile $Z_0(x)$, we can obtain the transfer function of the non-uniform line by solving the Riccati equation. The physical explanation of the wave propagation in the non-uniform line can be explained in the following way. The forward propagating wave is coupled into the backward propagating wave, and the coupling coefficient is determined by the

impedance profile of the non-uniform line. The coupling process can be effectively explained with the transversal filtering structure, where the propagating signal is tapped out at multiple points along the delay line and summed up with different tap gain coefficients. It is valid to state that each non-uniform line can be mapped into the transversal filter with correspondent tap coefficients. Therefore, a reconfigurable transversal filter, which is equipped with adjustable tap coefficients, can be applied to realize the transfer functions of multiple non-uniform lines. In other words, multiple non-uniform lines can be mapped into a single reconfigurable transversal filter with different sets of tap coefficients. In this paper, the non-uniform line DDLs are mapped into different sets of tap coefficients and the correspondent integrated DDLs are realized with an on-chip reconfigurable transversal filter.

There is one question that can be raised here, why not directly implement the non-uniform transmission line on chip? If so, we will be confronted with two major challenges. First, in order to have the coupling of the EM wave take place, the length of the transmission line should be on the order of the wavelength. In this work the frequency operation range of interest is within the ultra-wide-band (UWB) region, from 3 to 10 GHz. The wavelength of the microwave carrier with the frequency of 10 GHz is on the order of 30 mm, which is too large for integration. Second, the integrated passive structures (like inductors) generate huge on-chip loss. Therefore, it is impossible to directly implement the non-uniform transmission line on chip. Instead of directly implementing the non-uniform transmission line, we utilize the equivalent transversal filter structure to realize the transfer function of the non-uniform line. The transversal filter employs artificial transmission lines, which are capable of providing desired delays with relatively small area and the reflection, or coupling, is realized with tap gain cells [30-32]. In this way, we avoid the necessity of EM wave coupling by replacing the non-uniform line with a transversal filter. Furthermore, the

reconfigurability of the transversal filter enables us to realize various non-uniform line responses with a single chip by changing the tap coefficients.

The design procedure of the integrated DDL described in this section includes two parts. The first part describes the circuit design of the integrated transversal filter and is illustrated in detail in Section 5.4.1. The second part explains the procedure of choosing the tap coefficients for different categories of DDLs and is illustrated in detail in Section 5.4.2. Compared to the continuously varying non-uniform line, the integrated transversal filter has a finite number of taps and exhibits a discrete manner. This discrete manner sets a limitation on the frequency operation range of realizable DDL because of the aliasing effect. The practical design considerations will be explained in detail in Section 5.4.3.

5.4.1. Integrated Reconfigurable Transversal Filter

The integrated DDL is based upon a transversal filter shown in Figure 5-2. The two major building blocks of the transversal filter are the delay block and the gain cell. Ideally one can have two degrees of freedom in the design of a transversal filter, the delay values and tap gain coefficient. Since it is difficult to control the exact values of the delay on chip, we choose to use identical delay and variable tap gain coefficients. Besides, it is challenging to implement the on-chip transversal filter with the structure shown in Figure 5-2 because the output port or the summation point is loaded with a large number of gain cells, and the heavy loading will degrade the speed and frequency performance of the transversal filter.

In order to solve this problem, we employed the reverse gain port of the distributed amplifier (DA) to realize the transversal filter, shown in Figure 5-3 [30-32]. In the distributed amplifier, the heavy loading of the gain cells is distributed along the drain

line and the frequency performance is enhanced over the conventional transversal filter structure shown in Figure 5-2. The input signal propagates along the gate line, and the gain cell turns the input voltage mode signal into the output current mode signal. The forward gain port of the drain line is properly terminated to avoid reflection of the forward traveling wave, and the backward traveling wave is summed at the reverse port in the current mode. The reverse port is loaded with a 100 Ω termination resistor which turns the current mode signal back into voltage mode at the output. This integrated transversal filter employs a differential structure in which the return current path is shortened and the common mode noise is reduced.

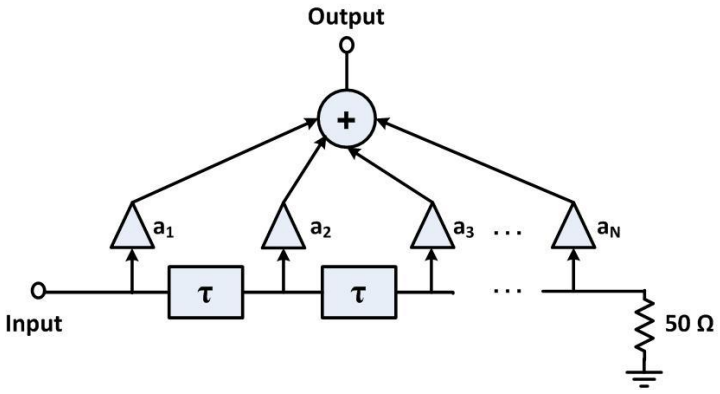

Figure 5-2 Transversal filter structure.

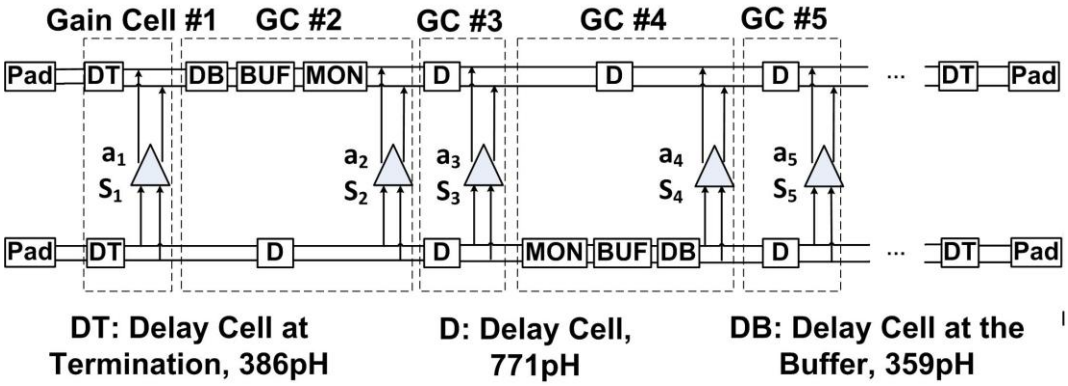

Figure 5-3 Integrated transversal filter based on the reverse gain of the distributed amplifier (DA).

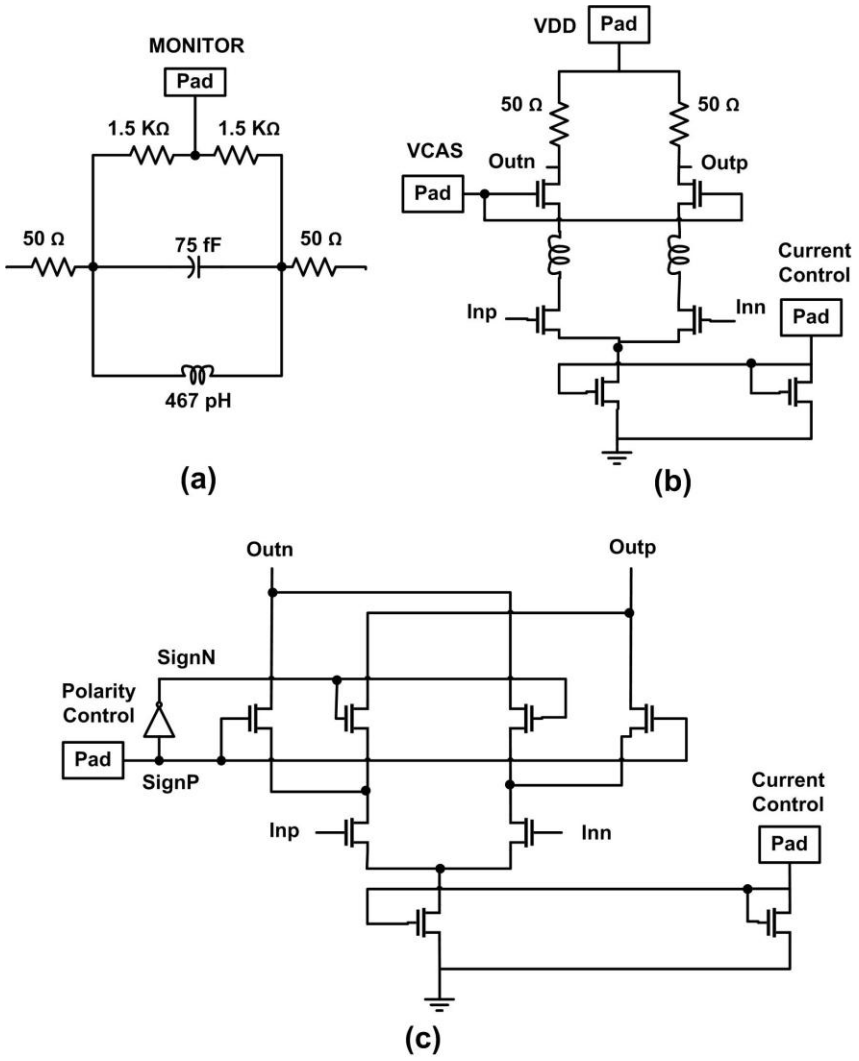

Figure 5-4 Circuit details of the integrated transversal filter, (a) monitor / impedance matching circuit (MON), (b) buffer amplifier (BUF), (c) differential variable gain cells (GC).

The delay block between the adjacent taps is realized with L section based artificial transmission line, shown as D in Figure 5-3. The delay block at the pad, shown as DT in Figure 5-3, is modified for impedance matching. As the signal propagates along the gate line and the drain line, the signal is attenuated by the artificial transmission line.

In order to compensate for the on-chip loss, several buffer amplifiers are inserted into the gate line and the drain line. The buffer amplifier contains three circuits, a monitoring circuit (MON), a differential amplifier (BUF) and a delay cell at the buffer output (DB). The circuit design details are shown in Figure 5-4. The monitoring circuit (MON) has two functions, first, it can provide the monitoring point of the gate line or drain line voltage, and second, it can provide a matched termination at the input of the differential amplifier (BUF) and avoid multiple reflections between two buffer amplifiers. The matched section is based on the pi-type matching network and is optimized to yield the best performance. The differential amplifier (BUF) employs a cascode structure with an inductor inserted between the input device and cascode device for bandwidth extension. Each output is loaded with a 50 Ω resistor for impedance matching, and the current is provided with the voltage supply. Since there is no DC current flowing along the gate line of the DA, the buffer amplifiers on the gate line is connected to an identical voltage supply of 2 V. However, the buffer amplifier on the drain line is not only responsible for the amplification, but also responsible for supplying current to the gain cells. Therefore, the voltage supply of the buffer amplifiers on the drain line should be able to vary to maintain the voltage bias (1.5 V) on the drain line. The gain of the buffer amplifier is determined by the current source controlled by the off-chip DAC (AD5308). The delay cell (DB) at the output of the differential amplifier (BUF) employs the conventional L section with a smaller inductance (359 pH) compared to that of the delay cells (D) between the adjacent gain cells (771 pH) in order to compensate for the delay introduced by the differential amplifier (BUF). Figure 5-4 (c) shows the schematic of the gain cells realized with a Gilbert Gain Cell. The gain is controlled by the current source connected to the off-chip DAC (AD5308), and the polarity is controlled by choosing to turn on the proper cascode device pair. The polarity control is realized with the FPGA and the off-chip

multiplexer (MAX4053A) to provide the voltage of 1 V and 2 V representing 0 and 1 of the polarity. The gain cell turns the input voltage mode signal into the output current mode signal. The drain line is terminated with the 50 Ω resistances at both positive and negative signal line of the differential line and the output current mode signal is translated into the voltage mode signal at every termination. The tap gain cells can also be utilized to compensate for the on-chip loss introduced by the artificial transmission line. The delay cells and the gain cells provide different delays and gain coefficients to generate the output signal propagating on the drain line based on the input signal propagating on the gate line. The generated output signals are summed at the reverse gain port to realize the transversal filter function.

Even though we utilize the transversal filter to realize the transfer function of the non-uniform line, it is intrinsically different from the non-uniform line in principle because the non-uniform line employs the EM wave coupling, which continuously takes place along the line while the transversal filter uses a discrete set of taps and the number of taps is finite. Therefore, we need to carefully choose the delay values to avoid aliasing in the transfer function. This will be discussed in detail in Section 5.4.3.

We implement the integrated transversal filter with 130 nm IBM8RF CMOS process. Ideally, given enough area, we can implement the reconfigurable transversal filter with desired group delay variations in a single chip. For our demonstration, however, the maximum group delay we can achieve with the given area (1.6 mm x 5 mm) is 500 ps. Therefore, we cascade two chips for large enough group delay variation. The two chips are placed onto the two individual PFQ packages PLQ06401 which are soldered onto the testing board shown in Figure 5-5. Each chip provides the maximum delay of 500 ps together with 12 taps and the delay between the adjacent taps is approximately 50 ps. The integrated transversal filter employs a total number of 20 taps. Figure 5-6 (a) shows the measured phase response of each tap and Figure 5-6

(b) shows the measured magnitude response of a typical tap. The integrated transversal filter exhibits a cutoff frequency of 4.5 GHz because we utilize the FR-4 board to perform the demonstration. The high speed signals go through 0.6 inch of FR-4 coplanar waveguide (CPW) transmission line and the wirebonds, which degrade the higher frequency performance. The transversal filter can operate to higher frequency range if the high speed probes are applied for measurements. Figure 5-6 (a) indicates that there exists a gap between tap 12 and tap 13 because the two chips are separated by two wirebonds which introduce an extra of 150 ps delay. This is also proved in the step responses of individual taps (tap 1, 6, 11, 16 and 20) shown in Figure 5-7 (a). There are 150 ps extra delay between tap 11 and tap 16 as compared to the other adjacent taps. The step response of a typical tap with different tap weights is shown in Figure 5-7 (b). In this way, we have successfully designed, implemented and characterized the integrated transversal filter in standard CMOS process.

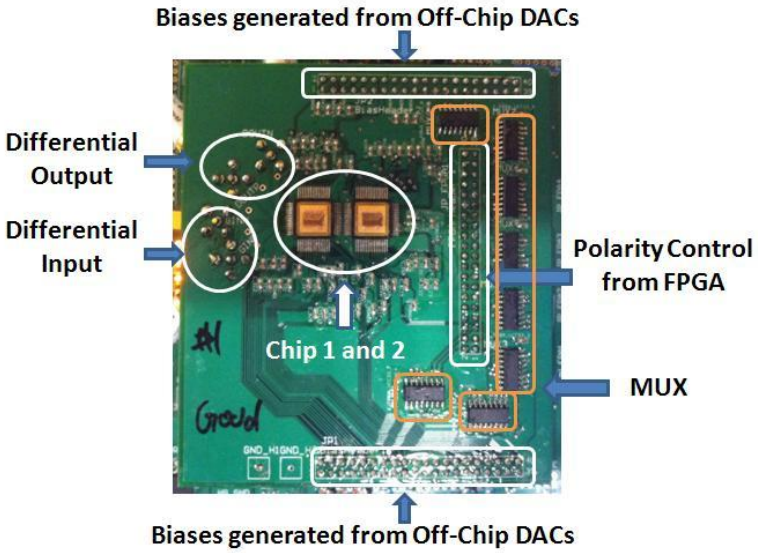

Figure 5-5 Test board of the integrated DDL.

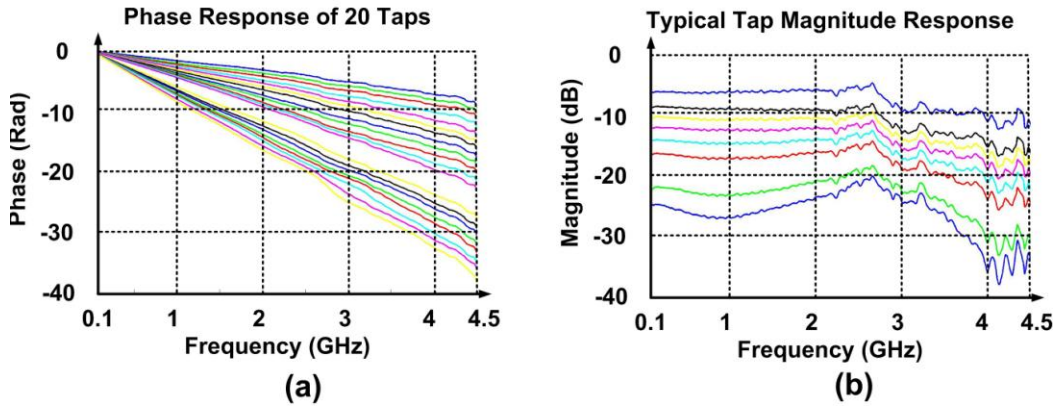

Figure 5-6 (a) Phase response of 20 taps (2 chips) and (b) a typical tap response with variable gain coefficient.

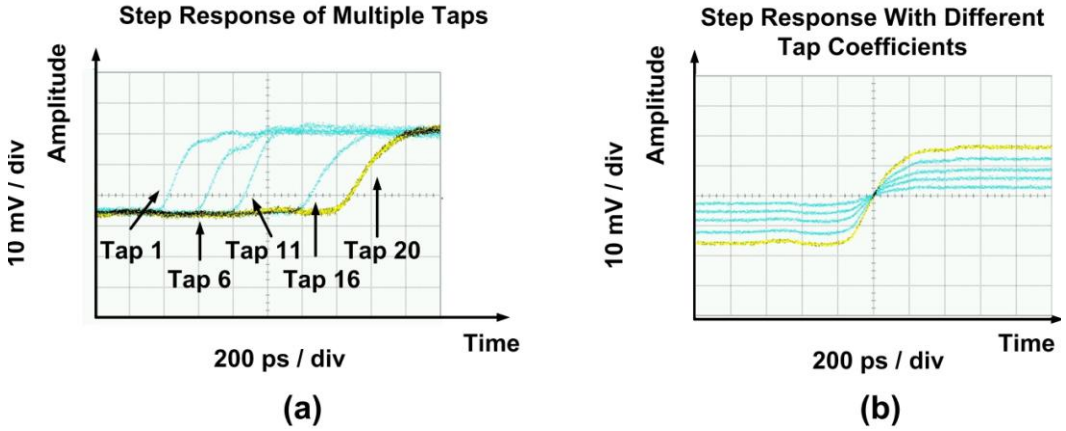

Figure 5-7 Time domain measurement, (a) the time relation of different taps and (b) the step response of a typical tap with different tap coefficients.

5.4.2. Tap Coefficients of the Designate DDL

Up to now, we have completed the first part of the design procedure of the reconfigurable DDL. In this section, we will demonstrate the approach of obtaining

the tap coefficients of the designate DDL and show how it can be reconfigured. The procedure of obtaining the tap coefficients based on the designate DDL is illustrated in Figure 5-8. Given the impedance profile of the non-uniform line based DDL, we can find out its transfer function or reflection coefficient ρ by solving the Riccati equation. Then we can obtain the impulse response by taking the Inverse Fourier Transform (IFT). Sampling the impulse response with the delay between the adjacent taps gives us the correspondent tap coefficients including tap weights and polarities.

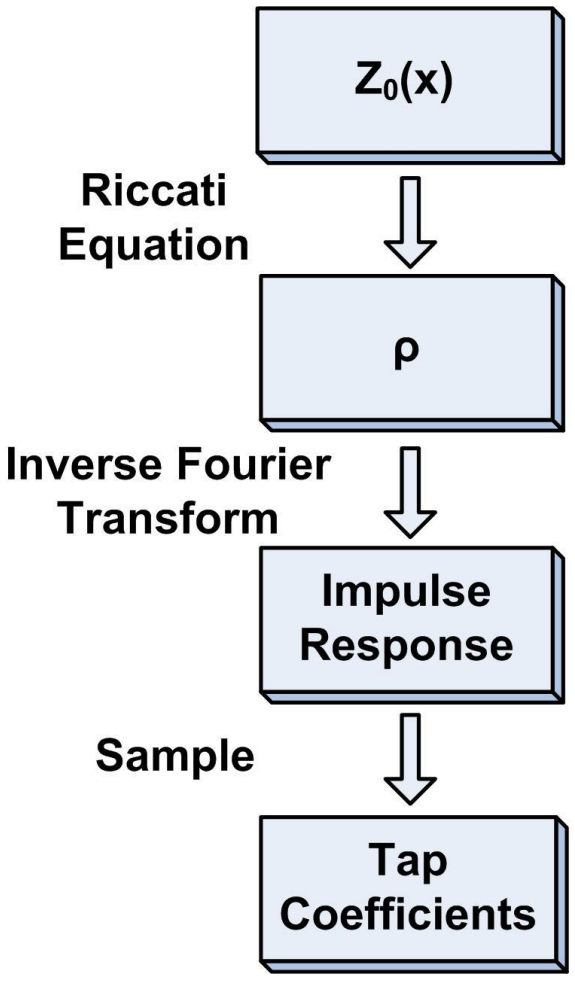

Figure 5-8 Design procedure of obtaining tap coefficients from the designate non-uniform line.

As we discussed in Section 5.3.1 and 5.3.2, the impulse response is very close to the coupling coefficient along the line under the condition of small reflection. If the small reflection approximation does not hold, we need to utilize the numerical integration discussed in Section 5.3.3 to obtain the impulse response. Once we obtain the impulse response of the designate DDL, we can sample the impulse response with the delay between the adjacent taps of the transversal filter. The acquired information is the coefficient and polarity of each individual tap. In this way, we can utilize a transversal filter to achieve the same transfer function of any arbitrary non-uniform line. This feature is very important because it provides us with an efficient approach to implement the integrated version of the non-uniform line transfer function with standard CMOS process. Many of these transfer functions, for example a chirped delay line in the UWB band, have previously been impossible to realize on chip using other methods. We cannot directly build the on-chip non-uniform line for the consideration of size and loss. It is also not practical to implement the integrated DDLs with only lumped elements as the CRLH DDLs [33, 34] because they require accurate values of the lumped elements which are difficult to achieve on chip. The reconfigurable integrated transversal filter on the other hand, has solved the problems of size and loss, furthermore, it enjoys a large number of degrees of freedom in design and the inaccuracy can be compensated.

As discussed earlier, this integrated reconfigurable transversal filter can be applied to achieve the transfer function of any arbitrary non-uniform line. Therefore, we choose the non-uniform line based DDL as the goal of the design. The design equation and the impedance profile of the non-uniform DDL is given in a number of previous papers [1].

$$Z_0(x) = 50 \cdot exp\left(A \cdot W(x) \cdot sin\left(\frac{2\pi}{a_0} \cdot x + C \cdot x^2 - C \cdot \left(\frac{L}{2}\right)^2\right)\right) \quad (5.10a)$$

$$W(x) = exp\left(-4 \cdot \left(\frac{x - L/4}{L}\right)^2\right) \quad (5.10b)$$

where $Z_0(x)$ is the impedance profile along the non-uniform line, whose range is from –L/2 to +L/2, A is the weighting factor controlling the modulation depth of the impedance variation, W(x) is a windowing function, it is made asymmetric to compensate for the frequency dependent loss over the DDL. Table 5-1 provides a summary of the parameters given in the impedance profile equation,

Symbol	Details	Expression
ε_r	Relative permittivity in PCB	6.8
c	Speed of EM wave in free space	3 x 10^8 m/s
v	Speed of EM wave in PCB	$c/\sqrt{\varepsilon_r}$
T	Total delay of the DDL	1.2 ns
L	Total length of the DDL	$T \cdot v$
f_C	Center frequency of the DDL	/
BW	Bandwidth of the DDL	/
a_0	Local spatial period at x=0	$v/(2 \cdot f_C)$
C	Chirp rate of the DDL	$(4\pi \cdot BW)/(v^2 \cdot T)$

Table 5-1 Design parameters in impedance profile function.

where ε_r is the relative permittivity of the printed circuit board (PCB) dielectric material described in equation (8), c is the speed of EM wave in free space, v is the speed of the EM wave traveling in the PCB line, T is the total delay provided by the non-uniform line DDL, L is the total length of the non-uniform line DDL, f_C is the center frequency of the operation range, BW is the operation bandwidth of the DDL, a_0 is the local spatial period at x=0, C determines the chirping rate of the DDL. The key design parameters of the DDL are the center frequency f_C, operation bandwidth BW and total delay T. One thing to mention is that the impedance profile proposed in [4] is for designing the DDL with linear dispersion characteristic. We can use this impedance profile equation to redesign the DDL to accommodate for our integrated DDL properties, and we will provide the demonstration of four different DDLs in Section 5.5.

Now that we have obtained the impedance profile function of the designate non-uniform DDL, we can follow the steps in Figure 5-8 to obtain the tap gain coefficients and polarities. Finally we need to simulate the frequency response of the transversal filter with the tap information to verify the transfer function.

5.4.3. Practical Design Considerations

As discussed earlier in this section, we will be confronted with several practical design considerations when we implement the integrated reconfigurable transversal filter and apply the tap coefficients to achieve designate DDL functions. The first non-ideality of the practical design comes from the tap gain cells. We use the standard Gilbert Cell to achieve gain control and polarity control [30-32, 35, 36]. In each tap gain cell, the gain control is realized with a current source controlled by an off-chip

DAC (AD5308), while the polarity control is realized by alternating the bias voltage of the cascode devices. The off-chip DAC (AD5308) is an 8-bit DAC with 1 V voltage operating range and 4 mV resolutions. Therefore, we cannot achieve any arbitrary gain value with the tap gain cell. Instead, the gain values will be divided into multiple levels. In the practical design, the operation range of the control voltage is from 0.26 V to 0.4 V associated with 8 different levels of gain, which translates to a 3 bit tap gain control.

The second practical design consideration is the choice of delay blocks. We choose passive L sections as our delay blocks, and there are other alternatives, such as active delay blocks and integrated coplanar waveguide. Figure 5-8 indicates that the delay blocks are utilized to sample the designate impulse response. Therefore, the delay blocks operate as a sampling clock and this feature will put the constraint on the frequency range of the DDL. Suppose the DDL operates at the center frequency of f_C, bandwidth of BW and exhibits the total delay of T, the operating frequency range is from f_C-BW/2 to f_C+BW/2. According to the Nyquist Theorem, sampling frequency should be at least twice as high as the high end of the operating frequency. As a result, we can obtain the lowest sampling rate required in this situation,

$$f_S \geq 2 \cdot (f_C + \frac{BW}{2}) \tag{5.11a}$$

The delay value between the adjacent tap is bounded by,

$$\Delta\tau = \frac{1}{f_S} \leq \frac{1}{2 \cdot (f_C + \frac{BW}{2})} \tag{5.11b}$$

We can also obtain the constraint on the number of taps,

$$N = \frac{T}{\Delta\tau} \geq 2 \cdot (f_C + \frac{BW}{2}) \cdot T \qquad (5.11c)$$

The equation (5.11) sets the principal limit in the transversal filter design. In practice, however, we need to have enough design margin and the numerical simulation is able to help us to optimize the design. In our design, the delay between the adjacent taps is 50 ps, yielding the sampling frequency of 20 GHz. Therefore, the highest operation frequency limitation of the transversal filter is 10 GHz.

The third practical design consideration is the delay gap between the two chips. The wirebonds and the FR4 transmission line introduce an extra delay of 150 ps between tap 12 and tap 13. This can be translated into three taps (tap 13, 14, and 15) with tap gain coefficient of 0 and the second chip should be starting from tap 16. This will bring along some discrepancies between the designate DDL transfer function and that achieved with integrated reconfigurable transversal filter. This problem is not intrinsic and can be solved if we are given large enough chip area to integrate the transversal filter in a single chip.

5.5 Experimental Demonstration of Integrated Reconfigurable DDL

Up to now, we have proven that the transversal filter can be utilized to realize the frequency response of the arbitrary non-uniform line. The physical implementation of the integrated reconfigurable transversal filter is illustrated in Section 5.4. In this section, we will follow the steps in Section 5.4 and provide experimental demonstration of multiple integrated DDLs by properly adjusting the tap coefficients of the integrated reconfigurable transversal filter.

5.5.1. Frequency Domain Demonstration of Multiple DDLs with Integrated Reconfigurable Transversal Filter

In this section, we modify the parameters in [1] to accommodate our transversal filter. The highest frequency is less than 4.5 GHz, and the total delay is 1.2 ns. We follow the design procedure proposed in Section 5.4.2 and demonstrate four different transfer functions with the integrated reconfigurable transversal filter. First we need to choose the frequency operating range, and then with the given parameters, we can obtain the impedance profile equation using Table 5-1. Then we can follow the steps in Figure 5-8 to obtain the correspondent tap coefficients. The first demonstration is presented in Figure 5-9. Figure 5-9 (a) shows structure of non-uniform line 1, which is 80 mm in length to provide the group delay variance of 1.2 ns. Figure 5-9 (b) and (c) show the simulated magnitude response and group delay characteristic of the designate non-uniform line. Following the steps in Figure 5-8, we can find out the correspondent tap coefficients. Applying the tap coefficients to the reconfigurable integrated transversal filter yields the integrated DDL1. Figure 5-9 (d) and (e) show the measured magnitude response and group delay characteristic of the integrated DDL1. As can be seen from the figures, the measured results are very close to the simulated results. The simulated response exhibit insertion loss because the non-uniform line is a passive structure. The measured response exhibits gain because the integrated reconfigurable transversal filter employs active element, and tap coefficients are specifically chosen and scaled according to impulse response to yield gain. We modify the tap coefficients of the integrated reconfigurable transversal filter to realize four different DDLs, shown separately in Figure 5-9, 5-10, 5-11, 5-12. All of the DDLs are designed based on the correspondent non-uniform lines. The comparisons indicate that the integrated reconfigurable transversal filter can be used to successfully reproduce the transfer function of the given non-uniform line and provide gain to it. DDL1 operates from 0.4

GHz to 4 GHz with the negative chirp of 1.2 ns as shown in Figure 5-9. DDL2 operates from 0.4 GHz to 4 GHz with the positive chirp of 1.2 ns as shown in Figure 5-10. DDL3 operates from 0.2 GHz to 2 GHz with the negative chirp of 1.2 ns as shown in Figure 5-11. DDL4 operates from 0.5 GHz to 2.5 GHz with the positive chirp of 1.2 ns as shown in Figure 5-12. As mentioned before, the integrated reconfigurable transversal filter is realized with two separate chips mounted on two QFP packages PLQ06401 to generate enough dispersion (shown in Figure 5-5). It is plausible to cascade more chips to generate more dispersion. The area of a single chip is 1.6 mm x 5 mm, the photo of the chip is shown in Figure 5-15. The power supply of the chip ranges from 2 V to 2.5 V depending on the tap gain coefficients. The current supplies ranges from 200 mA to 300 mA, also depending on the tap coefficients.

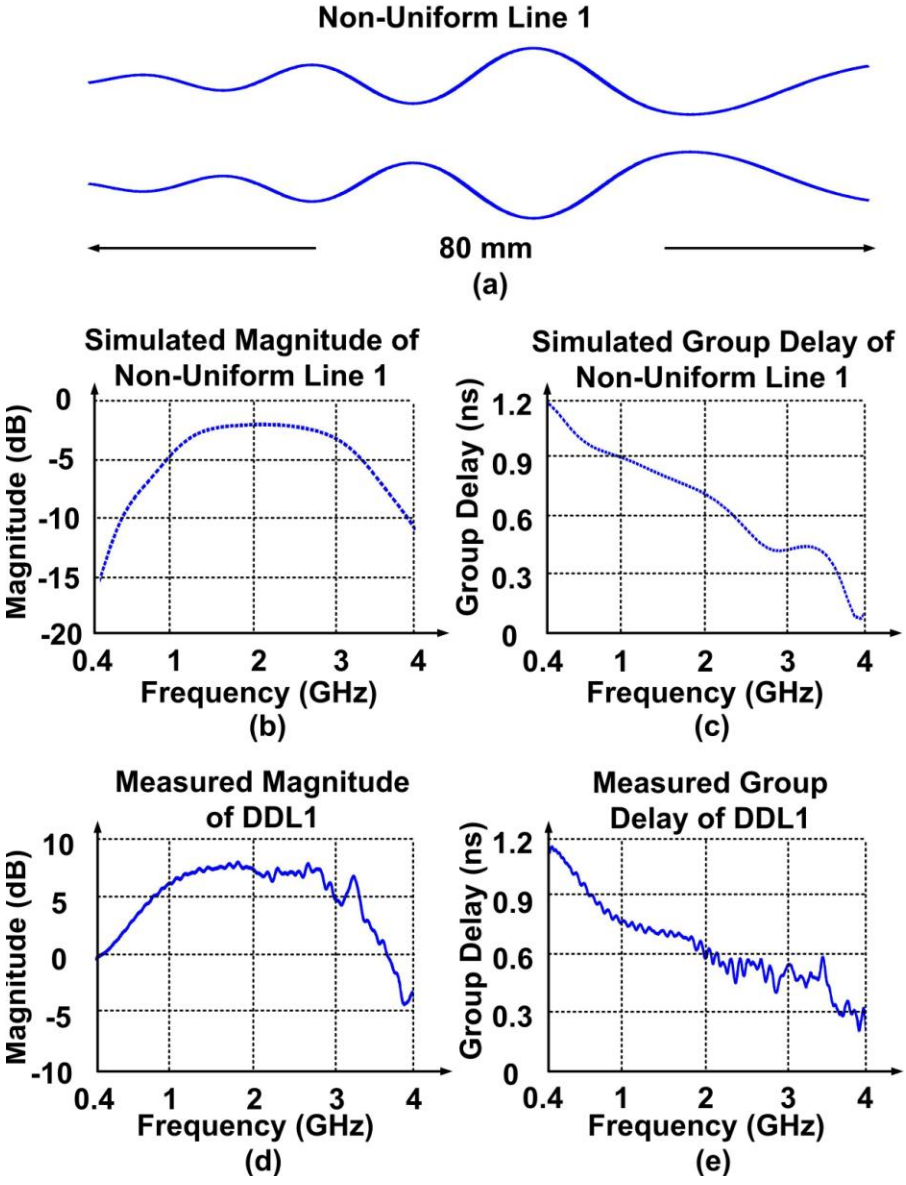

Figure 5-9 Simulated and measured magnitude and group delay of DDL1.

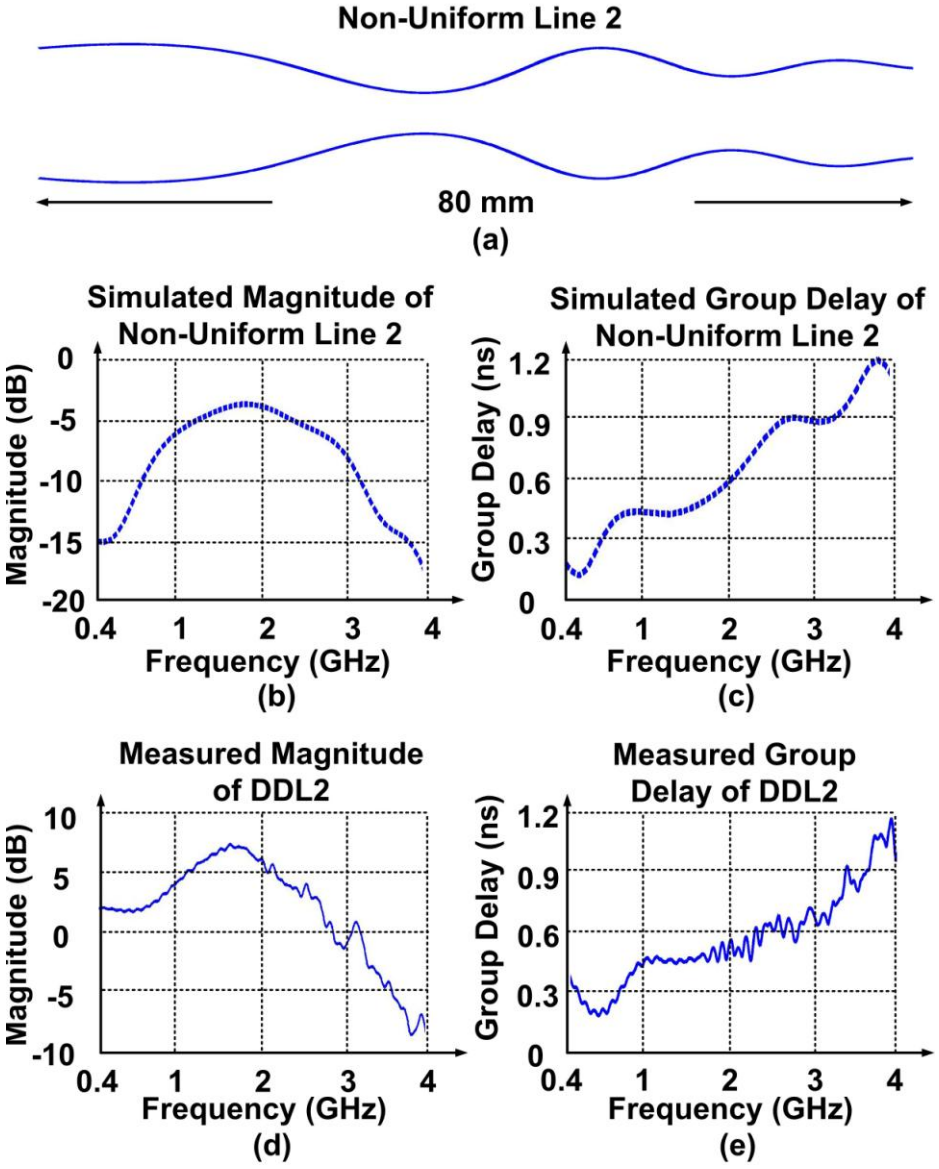

Figure 5-10 Simulated and measured magnitude and group delay of DDL2.

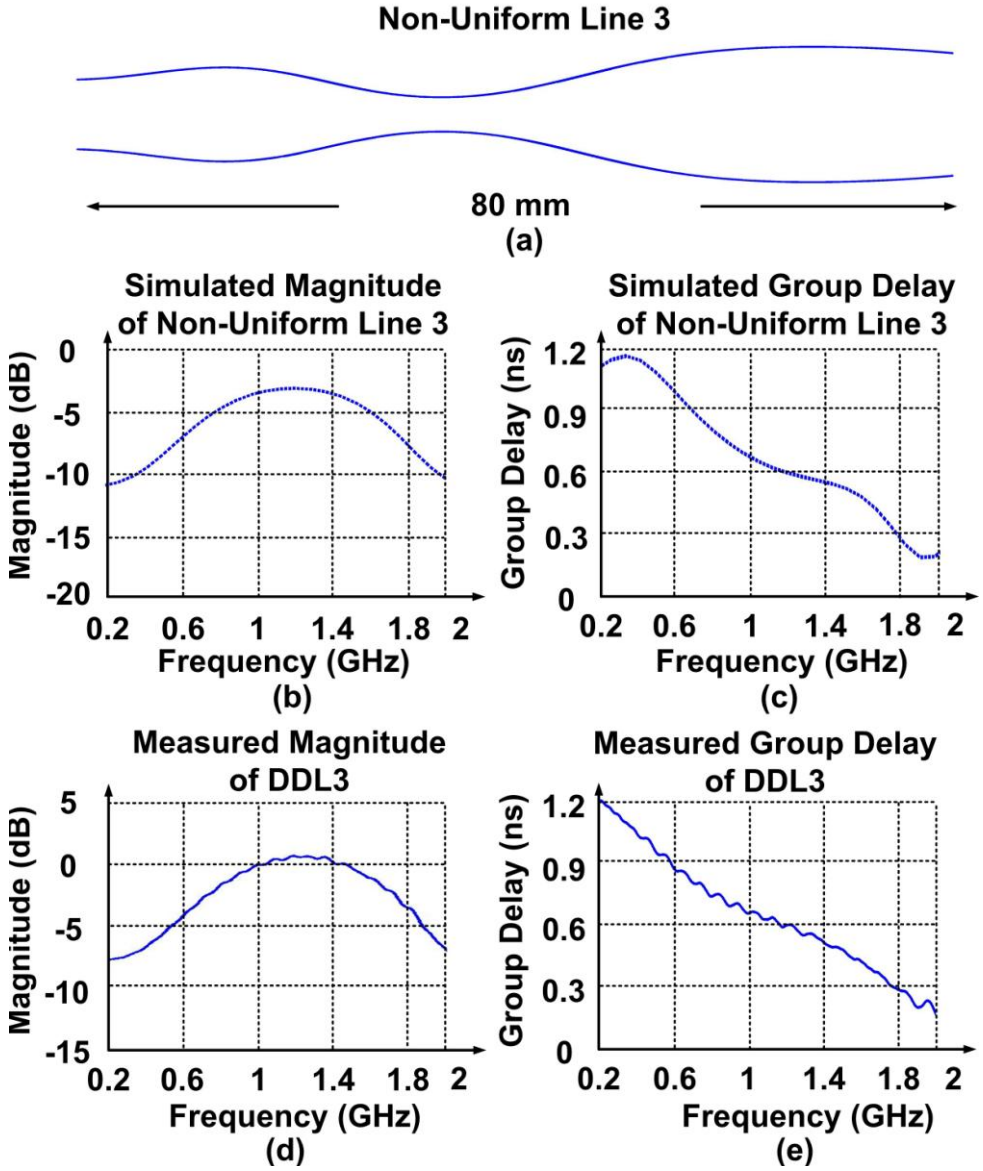

Figure 5-11 Simulated and measured magnitude and group delay of DDL3.

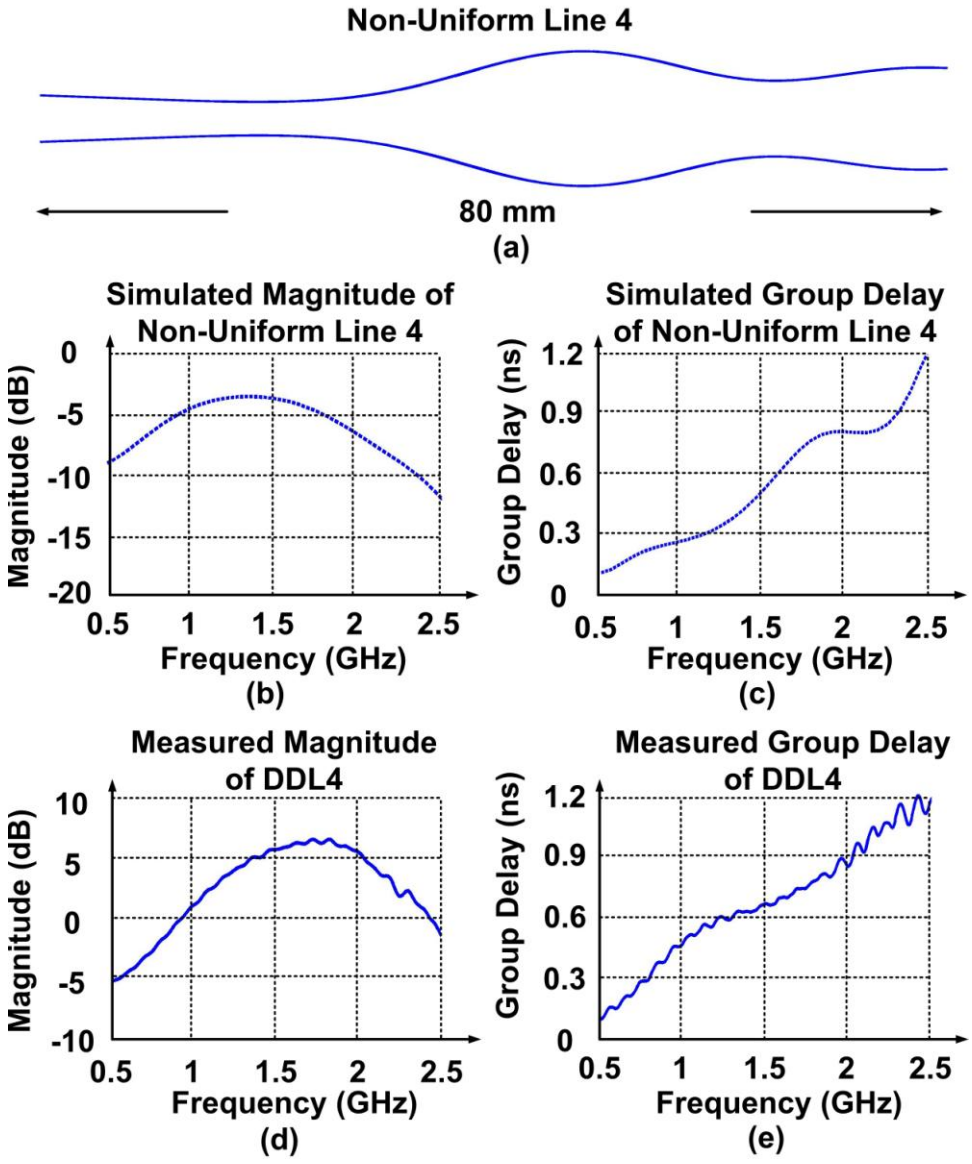

Figure 5-12 Simulated and measured magnitude and group delay of DDL4.

5.5.2. Real Time Spectrum Analysis Using the Integrated Reconfigurable DDL

In this section, we will provide the real time demonstration of the DDLs realized in Section 5.5.1. The linear DDL can be used for real time spectrum analysis since it provides a time to frequency mapping. Different frequency components experience different amounts of group delay when they pass through the DDL, spreading them out in time according to their spectral components. Since the DDL utilizes the group delay variance of different frequency components, the actual output signal in time domain is a representation of the spectrum mapped to the time domain. In order to obtain the spectrum of the input signal, we need to take the envelope of the output signal. Similar real-time spectrum analysis has been demonstrated in the previous work [37] using the non-uniform line operating from 4 GHz to 8 GHz with 1 ns negative chirp. In order to perform the real time spectrum analysis, the DDL should satisfy the following condition [37, 38],

$$\left| \frac{\Delta t_{in}^2}{4 \cdot T/BW} \right| < 1 \tag{5.12}$$

where Δt_{in} is the time duration of the input signal, T/BW is the dispersion slope of the DDL. The envelope of the output signal resembles the Fourier Transform of the input signal and the operating range of the DDL based real time spectrum analysis is limited to the frequency range of the DDL. For example, DDL1 of Section A is capable of analyzing the spectrum from 0.4 GHz to 4 GHz. We have shown the real time spectrum analysis demonstration using DDL1 with 0.6 ns pulse streams. The pulse streams are generated based on a 6 bit 10 Gbps signal using Anritsu Pulse Pattern Generator MP1763C. These are similar to the pulses examined in [37] but there is one difference in our case. Our integrated DDL utilizes a differential structure and the

signal bit stream needs to be adjusted to the differential signaling, meaning that the bit 0 is represented as -1 in our structure. We provide the demonstration of two sets of pulse streams (011001) and (110100) shown in Figure 5-13 and 5-14. Figure 5-13 (a) and 5-14 (a) shows the simulated spectrum of the two pulse streams. Figure 5-13 (b) and 5-14 (b) shows the measured output signal of the integrated DDL. The output stream is 1.2 ns long mapping to a frequency range of 0.4 GHz to 4 GHz. Since DDL1 is negatively chirped, the low frequency content appears at the leading edge of the output signal and we need to reverse the output signal envelope to properly display the spectrum [37]. Figure 5-13 and 5-14 indicate that the envelope of the output signal provides a good approximation to the spectral content of the input signal. We have successfully demonstrated that the reconfigurable integrated DDL is capable of real-time spectrum analysis.

There are some slight discrepancies between the simulated spectrum and measured output envelope because the DDL1 is not a perfect linearly dispersive line. Furthermore, the frequency range is 4 GHz and the dispersion is 1.2 ns, yielding the time-bandwidth product of five, not enough for spectrum analysis requiring high resolution and accuracy.

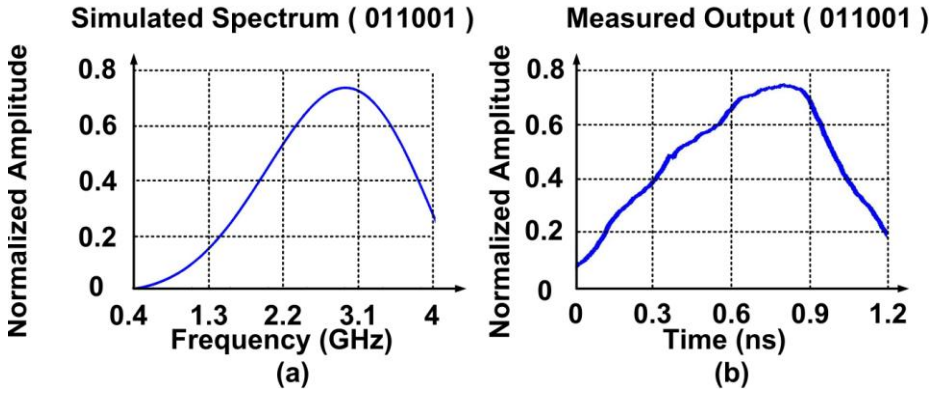

Figure 5-13 Real time spectrum analysis of the bit stream 011001.

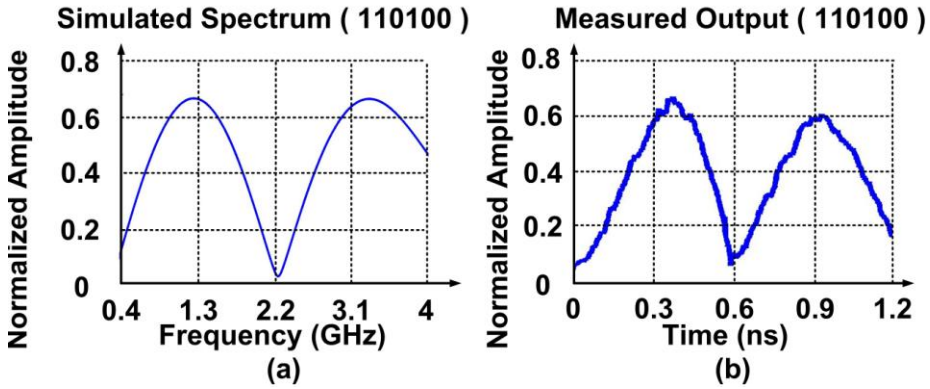

Figure 5-14 Real time spectrum analysis of the bit stream 110100.

Using the approach introduced in this chapter, we can design the integrated transversal filter with higher frequency operating range, larger group delay and more number of taps for the purpose of more accurate real time spectrum analysis.

5.6 Conclusion

Dispersive delay line (DDL) has been utilized widely in communication systems for decades. The applications include real time Fourier Transform [9], temporal imaging [5], pulse position modulation [39], frequency discrimination [34], compressive receiver [33], controllable delay line [6], etc. Even though numbers of DDLs have been reported, very few of them are implemented on-chip, leaving a blank spot of this capable and useful device. In this chapter, we have taken a different approach toward DDL design and have demonstrated a proof-of-concept design at 4.5GHz that is both integrated on chip and reconfigurable. We have recognized that the previous efforts of implementing DDLs are based on the wave propagation and reflection in the different

types of materials. The Riccati equation describes the relationships between the reflection coefficient at the input end of a corrugated structure and its local reflection coefficients along the structure. In this way, given enough information, e.g. the material and structure, of a DDL of any type, the Riccati equation associated with this DDL can be obtained, and can be solved for its transfer function.

We have used this idea in the design of a reconfigurable transversal filter and a method to map any non-linear transmission line onto this filter through tuning its tap coefficients. Using this technique, we can adjust both magnitude response and the group delay characteristics of our filter. We successfully demonstrated that this DDL can be used to realize multiple DDL functions, and could be used to replace the design of several DDL's or allow redesign of the transfer function post-fabrication.

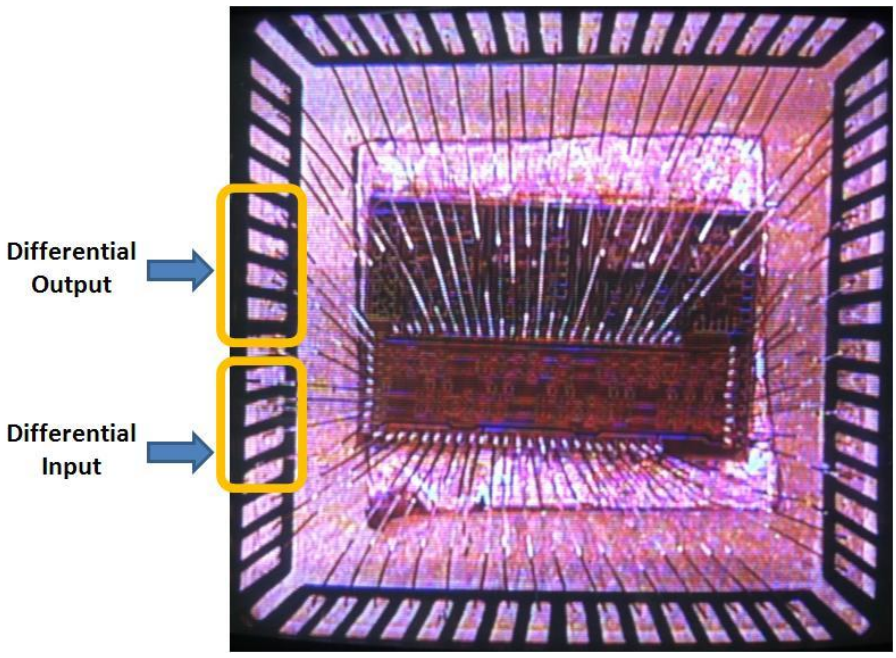

Figure 5-15 Die photo of the wirebonded chip and package.

We have demonstrated this through the design of four different types of DDLs in this work. We also performed the experimental demonstration of the real time spectrum analysis using one of the reconfigurable integrated DDL. Although our demonstration was limited to 4.5 GHz due to packaging on FR4 test boards, the idea can still be employed to implement DDL operating in higher frequency range if the probes are employed. Also this DDL can be scalable to higher frequencies, the frequency limit of this DDL comes from the delay block, the buffer amplifier and the Gilbert Gain Cells. As long as one can improve the frequency operating range of these building blocks, the DDL can be redesigned and moved to higher frequency and a wider range of applications.

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CHAPTER 6
CONCLUSION

6.1 Summary of Major Contributions

The major contributions of the work described in this dissertation are summarized as follows:

1. Propose and implement the first integrated dispersive delay line (DDL) with the dispersion enhanced distributed amplifier (DA). The DDL overcomes the two major obstacles of integration, the large size associated with the delay and the large on-chip loss by utilizing the dispersion enhanced artificial transmission line section and the active elements.
2. Improve the first integrated DDL by using the multi-path approach, which provides a better control on the dispersion characteristics and the gain profiles. The improved DDL makes full use of the dispersion provided by the first integrated DDL by providing gain compensation at high frequencies.
3. Propose and implement the first reconfigurable integrated DDL, which is capable of realizing multiple DDL transfer functions over different frequency ranges. This reconfigurable integrated DDL saves the effort of going through multiple design and manufacturing procedures for different DDLs.
4. Perform the experimental demonstration of the first on-chip temporal imager (TI).
5. Perform the experimental demonstration of the first on-chip time-stretching (TS) system.

6. Perform the experimental demonstration of the first on-chip real time spectrum analysis.

6.2 Suggestions for Future Work

1. Scale up the reconfigurable integrated DDL to higher frequency operation range by using the high speed CMOS process.
2. Increase the dispersion of the reconfigurable integrated DDL by using the more area-efficient delay blocks, e.g. active delays.
3. Implement more accurate integrated real time signal processing and analysis blocks with the integrated DDL of higher frequency and larger dispersion, e.g. the Fourier Transformer, Chirped Z Transformer, etc.
4. Move the off-chip DACs and MUX on chip to realize a complete integration of the DDL which can be applied directly in the UWB system.
5. The reconfigurable integrated transversal filter can also be applied for pulse shaping, arbitrary waveform generation and equalization in the UWB system.