DEPOSITED SILICON PHOTONICS: OPTICAL INTERCONNECT DEVICES IN POLYCRYSTALLINE SILICON

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DEPOSITED SILICON PHOTONICS:

OPTICAL INTERCONNECT DEVICES IN POLYCRYSTALLINE SILICON

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Silicon photonics has tremendous potential to provide high-bandwidth and low-power data communication for applications such as computing and telecommunication, over length scales ranging from 100 kilometers over fiber to centimeter-length on-chip waveguides. Many silicon photonic building blocks have been demonstrated to date, but critical work remains to determine the best approaches for integrating together silicon photonics with microelectronics.

In this thesis, I explore a novel method for integration of silicon photonics on the CMOS platform by using a deposited material: polycrystalline silicon. I will show the first demonstrations of electrically-active optical filters, modulators, and photodetectors in this material. In principle, this material platform would allow for the integration of silicon photonic devices and systems on top of any substrate, including complex CMOS and memory chips or even glass and plastic substrates.

In Chapter 1, I introduce the state-of-the-art in silicon photonics, describe several integration schemes under development, and introduce the idea of using deposited materials. In Chapter 2, I demonstrate the use of polysilicon to make integrated microring resonators, and show the integration of different silicon materials together. Chapter 3 discusses the use of polysilicon as both an optical waveguiding layer and an electrode material in slot waveguides for the application of light emitters. Chapter 4 demonstrates the use of

a pump-probe experiment to measure the free carrier lifetime in the material and demonstrate all-optical modulation. In Chapter 5, I demonstrate the first high-speed integrated electro-optic modulator in polysilicon, a necessary device for optical transmitters. In Chapter 6, I show how defects inside the same material enable integrated photodetectors at near-infrared telecommunication wavelengths. Chapter 7 shows initial results in adapting the material processing for lower temperatures, necessary for integration on top of CMOS. Finally Chapter 8 concludes with an outlook for the field.

BIOGRAPHICAL SKETCH

Kyle Preston grew up in the Rochester, NY area, graduated from Fairport High School in 2002, and entered Cornell University to study electrical engineering. At Cornell, he completed an undergraduate internship at Sandia National Laboratories working on hardware development. Kyle graduated Magna Cum Laude from Cornell University in 2006 with a B.S. in Electrical and Computer Engineering and entered the M.S./Ph.D. program to study silicon photonics in the Cornell Nanophotonics Group led by Prof. Michal Lipson. During his Ph.D., he was a research intern at IBM Research and was a recipient of the IBM Ph.D. Fellowship for 2010-2011. Kyle's graduate research centered on materials and devices for high-speed integrated optical interconnects.

To my family and to Dana, for unwavering love and support.

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Optical Communication

In recent years, there has been tremendous growth in the amount of data that people generate and consume. The expansion of broadband wired Internet access has spawned new ways to share video, experience television and movies, and connect people together through voice and video calls. A similar expansion in wireless and cellular data is enabling constant connectivity including video streaming and teleconferencing on mobile devices. Many types of enhanced sensing techniques, for instance high-resolution time-resolved medical imaging, generate enormous sets of data to be transported, stored, and retrieved. In the computing domain, the continuation of Moore's Law has resulted in systems with exponentially increasing computational power, resulting in a need for exponentially increasing data bandwidth to keep pace.

Optics plays an increasingly important role in all of these areas. Fiber optics forms the backbone of the Internet, connecting together continents, cities, and now neighborhoods. Optics is pushing closer to the consumer through Fiber-to-the-Home (FTTH) and Fiber-to-the-Office (FTTO) deployments to provide data bandwidths which are not achievable over traditional electrical connections. The use of fiber connections to cellular towers is increasing along with wireless bandwidth demands. Finally, optical connections are now standard in datacenter, cloud computing, and high-performance computing applications to connect large numbers of computer racks together.

The advantages of optics compared to electrical connections are primarily bandwidth, power consumption, and distance. For instance, the 10 Gigabit Ethernet standard[1] contains specifications for either optical or copper connections; the optical specification 10GBASE-ER extends as far as 40 km over single-mode fiber, while the copper specification 10GBASE-T is limited to 100 m. Similarly, the 40 Gigabit Ethernet standard[2] optical specification 40GBASE-LR4 extends to 10 km, while the copper specification 40GBASE-CR4 is limited to only 7 m. Metal interconnects are fundamentally limited due to resistance, parasitics, and crosstalk. Especially important is that losses increase as the frequency increases, due to the skin effect. Techniques such as equalization or error correcting codes can extend the bandwidth or distance at the expense of energy consumption per bit. In contrast, optical connections offer a fundamentally enormous carrier bandwidth on the order of 200 THz for infrared light, which can be exploited using wavelength division multiplexing (WDM) to send many individual signals on individual colors of light.

The main disadvantage to optics has been cost. Traditionally many discrete components must be precisely aligned and packaged together to create optical systems. An interesting trend has been the adoption of optics at shorter and shorter length scales versus time. This is because the benefits of optics become greater along with demands for increased data rates and reduced power consumption. For instance, datacenters and high performance computing currently use fiber optics to connect racks of computers together. It is expected that optics will penetrate further into the systems and closer to the processor units in the coming years, to the level of the server, circuit board, or even all the way to the computer chip.

[1] IEEE Std 802.3-2008
[2] IEEE Std 802.3ba-2010

There is a real need for optics at the computer chip level in the coming years. Miller [1] has demonstrated this using numbers derived from the International Technology Roadmap for Semiconductors (ITRS)[3], the main roadmap for the semiconductor industry. Based on the 2007 ITRS roadmap[4], between 2007 and 2022 the technology node (roughly the minimum transistor gate length in the CMOS process) decreases from 65 nm to 11 nm. The increase in number of transistors is related to an increase in the number of floating point operations that can be performed, from 1 TFLOP in 2007 to 7.2 TFLOPs in 2015 to 96.8 TFLOPs in 2022. Correspondingly, the chip I/O bandwidth must scale from 11 Tb/s in 2007 to 82 Tb/s in 2015 in order to maintain the architecturally optimum ratio of around one byte per FLOP. By 2022, the I/O bandwidth must scale to 230 Tb/s just to keep a ratio of 0.3 byte/FLOP (as the roadmap assumes that 1 byte/FLOP is no longer feasible). At the same time, the chip area is not changing dramatically due to yield and cost reasons, meaning that the number of signal pins increases very slowly with chip packaging capabilities. The only way to satisfy the bandwidth demands is to scale the off-chip clock from 4.88 GHz to 67.5 GHz by 2022, an extremely difficult challenge. At the same time, the total power consumption of the chip saturates at around 200 W due to the limits of heat dissipation. Miller predicts that the total power allocated for off-chip communication must fall more than an order of magnitude from 3500 fJ/bit to 170 fJ/bit, even as the clock rate increases more than 10×. These concurrent demands for bandwidth density and power consumption cannot be met with existing electrical interconnect technology.

Figure 1.1 shows a recent prototype implementation to bring optical communication all the way to the chip level [2]. In this demonstration, 2×12 arrays

[3]See http://www.itrs.net/reports.html
[4]See http://www.itrs.net/Links/2007ITRS/Home2007.htm

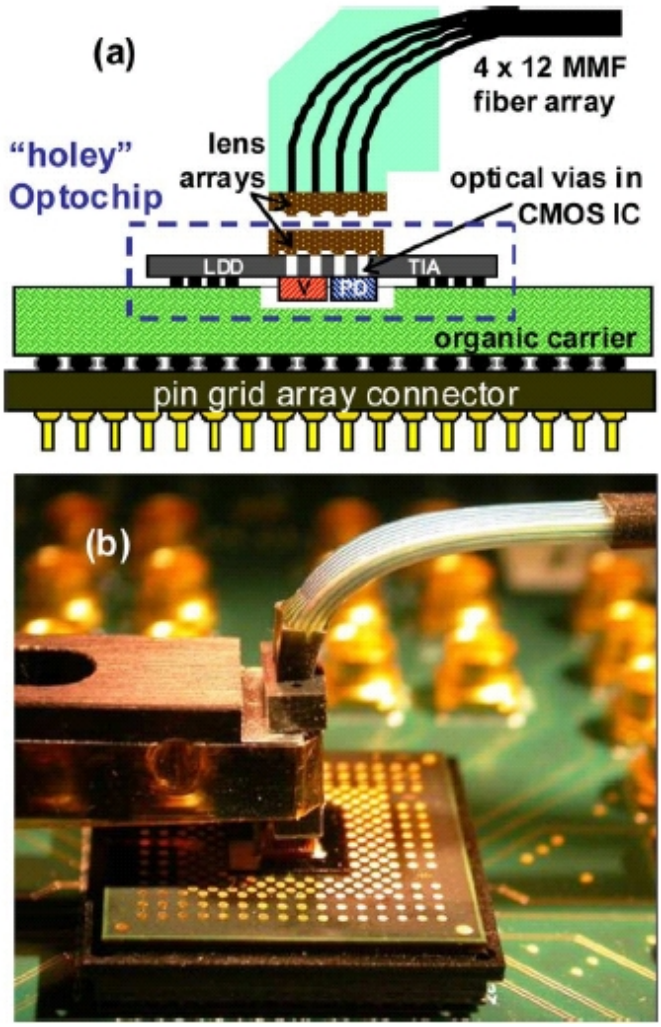


Figure 1.1: (a) Schematic and (b) photograph of IBM photonic integration using chip packaging of traditional optical components. The optical transceiver module combines arrays of VCSELs and photodiodes with their corresponding circuits and couples to a 4×12 array of multimode fibers. 300 Gbps full-duplex operation was demonstrated. Reproduced with permission from [2] (copyright 2011 IEEE).

of 850 nm-wavelength GaAs vertical cavity surface emitting lasers (VCSELs) and photodiodes are flip-chip bonded onto a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC). The CMOS chip contains the driver circuits required to power and directly modulate the VCSELs, as well as the transimpedance amplifier (TIA) and limiting amplifier (LA) stages to am-

plify the photodetector output. Holes are opened through the CMOS chip to allow optical access to the devices, which couple to a 4×12 array of multimode fibers. This module could be further packaged with microprocessor or memory chips on a multi-chip module (MCM) as part of a larger parallelized computing system. This is an impressive demonstration of the scaling of traditional optical components, but it also demonstrates that traditional packaging still creates a bandwidth density bottleneck that will be limited by the pitch of the flip-chip signal I/Os. Additionally, the packaging introduces electrical parasitics which can limit the potential performance of the optical devices and their microelectronic circuits.

1.2 Silicon Photonics

Silicon photonics has been a rapidly progressing field over the previous decade. A key development was the availability of high-quality silicon-on-insulator (SOI) wafers [3] with the proper dimensions for near-IR waveguiding: a silicon layer of around 200-250 nm on a buried oxide layer of 1-3 μm. Many critical devices have been demonstrated and improved in the past years: electro-optic modulators to convert data from the electrical domain to the optical domain [4, 5, 6]; low-loss waveguides and fiber couplers [7]; filters and switches [8, 9]; epitaxially grown germanium-on-silicon photodetectors [10]; and heterogeneously integrated III-V compound semiconductors for on-chip laser sources [11, 12].

The key to the promise of silicon photonic technology is that multiple optical functions can be monolithically integrated on a single chip using the highly

advanced silicon CMOS processing technology. Figure 1.2 shows a silicon modulator, silicon waveguide, and germanium-on-silicon photodetector integrated together to form an optical communication link [13]. The ultimate potential of silicon photonics lies not only with the monolithic integration of optical communication devices, but the optical devices together with the driver and receiver circuits. This can provide for extremely high bandwidth density and the minimization of electrical parasitics from traditional microelectronic packaging. Economically, the silicon photonics platform benefits from the semiconductor industry's massive investment in silicon material processing and the economies of scale from piggybacking on top of existing CMOS manufacturing.

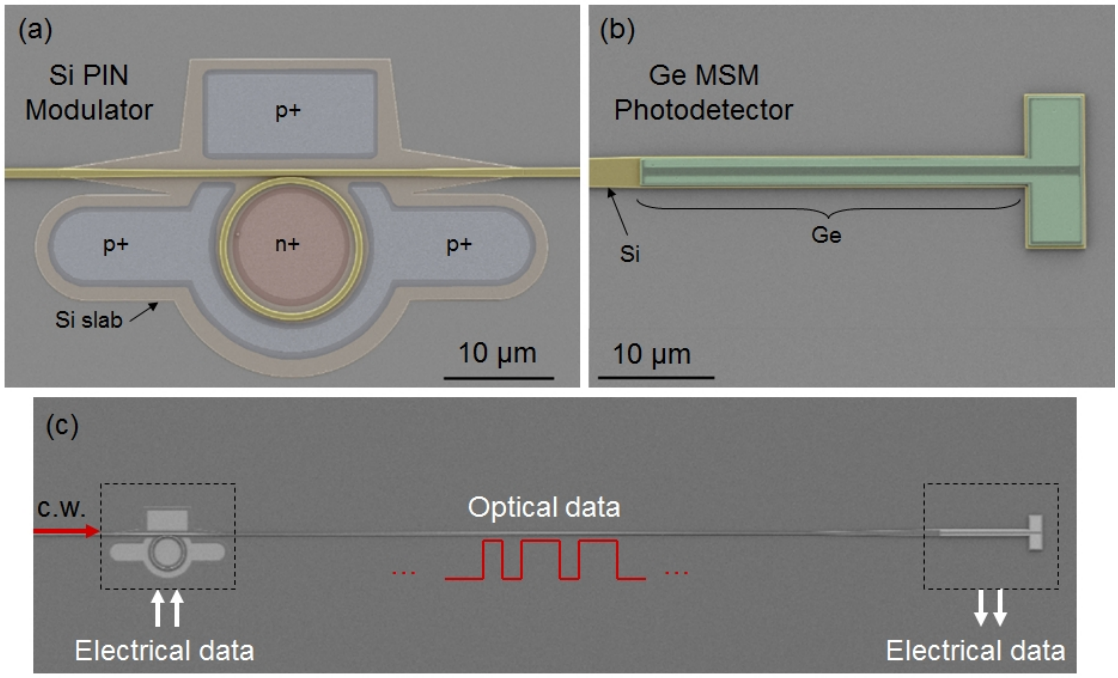


Figure 1.2: Monolithic integration of silicon photonic components [13]. (a) False-color SEM image of silicon microring electro-optic modulator. (b) False-color SEM image of germanium-on-silicon photodetector. (c) SEM image of devices connected by a silicon optical waveguide.

A current debate within the silicon photonics community revolves around the precise implementation of silicon photonics that will achieve the best ratio

of benefits to costs. In one approach, *chip packaging*, silicon photonic chips and microelectronic chips are fabricated independently and combined using traditional packaging techniques such as wire bonding or flip-chip bonding. Figure 1.3 shows a recent demonstration of of silicon photonic integration using the chip packaging approach. The key advantage is that the best-available fabrication process can be used for each chip: highly optimized CMOS processes for the circuits, and specialized photonic fabrication for the optical chip. However, the use of traditional packaging means that chip-scale bandwidth density cannot fundamentally improve very much, and electrical parasitics will ultimately limit the system performance.

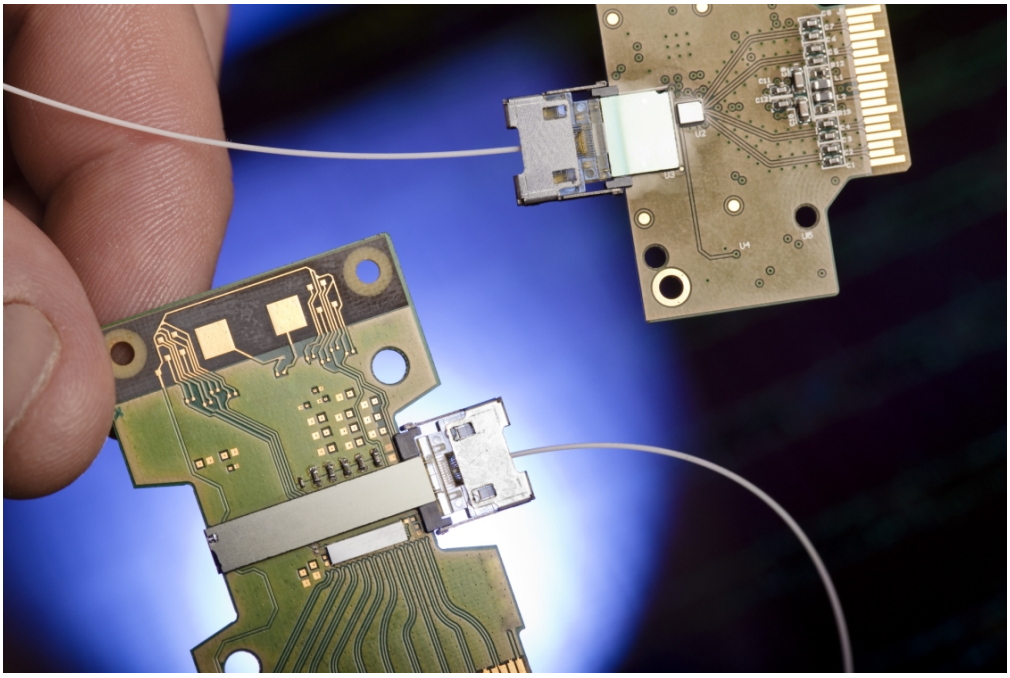


Figure 1.3: Photograph of Intel silicon photonic integration using chip packaging. The silicon photonic chip with III-V lasers, silicon modulators, and silicon multiplexer (large central chip) is flip-chip bonded to a circuit board next to a small CMOS chip with transmitter circuits. Similar integration is performed at the receiver end to demonstrate a 4×12.5 Gbps link. Reproduced with permission from [14].

Another approach, *monolithic front-end integration*, places the optical and mi-

croelectronic devices in the same SOI layer of crystalline silicon on a single chip [15]. The approach offers the tightest integration of optics and electronics to minimize electrical parasitics and maximize bandwidth density. However, it also places severe limitations on the performance of transistors within this process. At a wavelength of 1550 nm, a sub-micron silicon waveguide requires a lower cladding of at least one micron to maintain low-loss operation. In contrast, SOI transistors have consistently scaled to smaller buried oxide thicknesses on the order of 100 nm, due to both thermal and electrostatic limitations. Using a thick buried oxide SOI substrate fundamentally limits transistors to gate lengths greater than 100 nm, which is a tremendous limitation on performance and scalability. In principle, this monolithic integration could be combined with chip packaging to provide some monolithic circuit functionality while leaving the highest performing circuits to an externally packaged chip, but this solution is not ideal as overall performance will again be limited by the packaging. Additionally there has been work to integrate waveguides in the front end of a bulk-Si or thin-SOI substrate [16, 17, 18, 19, 20], but this requires processing steps that interact with the silicon transistor layer in some fashion.

The work in this thesis lays the groundwork for an intermediate approach lying between the two mentioned above: *monolithic back-end integration* [21]. In this approach, a separate layer of silicon photonic devices would be monolithically integrated in a plane that is separate from the transistor layer. In this way, the transistor layer can be formed with little or no change to its optimized fabrication process, eliminating the main challenge with front-end integration. At the same time, monolithic integration results in a dramatic improvement in bandwidth density and parasitics compared to the chip packaging approach. Metal vias can connect electro-optic devices directly to the circuits sitting below.

It is important to realize that multiple layers of the standard silicon photonic material, crystalline silicon, cannot be formed using standard manufacturing processes (although techniques do exist such as oxygen implantation [22], epitaxial overgrowth [23], and wafer bonding [24]). Instead, silicon can be deposited in many different compositions and phases. The main choices for deposited silicon waveguiding materials are presented in Table 1.1, along with crystalline silicon for comparison. A critical missing functionality is that none of these deposited materials possess adequate electrical properties for electro-optic devices for modulation, switching, and photodetection: silicon nitride and oxynitride are insulators, and hydrogenated amorphous silicon (a-Si:H) has very poor electrical properties due to its disordered crystal structure. This can be quantified in the effective carrier mobility, which is on the order of 1 $cm^2\,V^{-1}\,s^{-1}$ for a-Si:H compared to the order of 1000 $cm^2\,V^{-1}\,s^{-1}$ in crystalline silicon.

Material	n	Typical Loss (dB/cm)	Summary
Crystalline silicon	3.48	3	Not deposited. Must be formed by epitaxial crystal growth.
PECVD hydrogenated amorphous silicon	3.6-3.8	3	Poor electrical properties due to disordered structure.
LPCVD silicon nitride	2	0.5	Deposited at around 800 °C for purest form of the material.
PECVD silicon nitride	2-2.2	1.5	Deposited at $\leq$ 400 °C and not as pure.
Silicon oxynitride	1.6-1.9	< 1	Composition can be varied by changing deposition conditions.

Table 1.1: Crystalline silicon compared to deposited silicon photonic waveguide materials

This thesis focuses on the development of polycrystalline silicon for integrated optics. Polysilicon is a phase of deposited silicon material, potentially suitable for monolithic back-end integration, which can have electrical properties approaching those of single-crystalline silicon. The following section reviews previous work on polysilicon as an integrated optic material.

1.3 Prior Art for Integrated Polysilicon Photonic Devices

Polycrystalline silicon is the traditional gate electrode material of the CMOS transistor. For an excellent overview of the material fabrication and properties, see Ref. [25] by T. Kamins. The material consists of crystalline regions called *grains* which are separated by disordered *grain boundaries*. Additionally the crystalline grains can contain crystal defects. The material properties are determined by the size and structure of the grain boundaries, which can be controlled based on the fabrication conditions [26].

The work in this thesis owes a significant debt to the research group of Prof. Kimerling at MIT which performed initial groundbreaking research in the area of integrated polysilicon waveguides. Polysilicon was a promising option for waveguides before the widespread availability of crystalline SOI because it is a high-refractive-index material that is commonly available in CMOS processes. Initial work demonstrated the challenges of the material, namely the propagation loss due to scattering, absorption, and surface roughness; early work in 1983 by Jackson et al. at PARC indicated optical losses on the order

of 300 dB/cm [27]. In 1996, Foresi et al. [28] demonstrated large (1×8 μm) multimode waveguides deposited directly in the polycrystalline phase at 625 °C. Losses were reduced from 77 dB/cm to 34 dB/cm by including a chemical mechanical polishing (CMP) step to reduce surface roughness. Later in 1996, Agarwal et al. [29] showed a loss reduction in similarly large waveguides to 15 dB/cm through two process improvements: first, depositing the material in the amorphous phase at 560 °C to obtain a smooth top surface followed by a 600 °C crystallization anneal; and second, hydrogenating the material in an electron-cyclotron resonance (ECR) plasma chamber to fill dangling bonds at the grain boundaries and reduce absorption. In 1997, Liao et al. [30, 31] further reduced the loss to 9 dB/cm by increasing the annealing temperature to 1100 °C and reducing the waveguide height to 200 nm which slightly delocalizes the mode, although the waveguides were still multimode. Finally in 2000, Maki et al. [32] demonstrated the use of polysilicon in a microring resonator with a loaded quality factor Q_L = 7000.

During the time that the work in this thesis was being performed, several other groups demonstrated waveguide improvements in polysilicon. In 2008, Fang et al. at IME A*STAR demonstrated losses of 6.5 dB/cm in a single-mode waveguide by delocalizing the mode with an oxynitride cladding [33]. In 2009, Zhu et al. at IME A*STAR showed losses of 8 dB/cm in oxide-clad single-mode waveguides [34], and Orcutt et al. demonstrated 7 dB/cm in 120 nm tall × 350 nm wide oxide-clad single-mode waveguides fabricated at Micron Technologies [35].

In this thesis I present work that extends the use of polysilicon to many types of devices: microring resonators with Q_L = 20,000 [36], slot waveguide micror-

ing resonators with Q_L = 54,000 as a platform for light emitting devices [37], all-optical modulators with 135 ps response time [38], electro-optic modulators operating at 2.5 Gbps [39], and photodetectors operating in the λ = 1550 nm wavelength band [40]. I also show initial results for reducing the thermal budget of device fabrication by implementing excimer laser annealing to crystallize the material [41].

CHAPTER 2

MICRORING RESONATORS

We demonstrate optical microresonators in polycrystalline silicon with quality factors of 20,000. We also demonstrate polycrystalline resonators vertically coupled to crystalline silicon waveguides in a multi-layer integration scheme. Electrically active photonic structures fabricated in deposited polysilicon layers would enable the large-scale integration of photonics with current CMOS microelectronics[1].

2.1 Introduction

On-chip silicon photonic networks are a promising solution for the interconnect bottleneck in high performance microelectronics [42, 43], but the additional silicon real estate required to integrate hundreds or thousands of microphotonic devices is one of the main barriers to their immediate implementation. Many planar silicon photonic building blocks have been recently demonstrated [44, 45, 15, 46, 47, 48, 49, 50]. Most of the major progress in silicon photonics has been based on single-crystalline silicon on insulator (SOI), which is widely available and has well-understood material properties. By itself, however, the SOI platform restricts active electronic and photonic devices to a single layer. This limits the number of devices that can fit on a chip.

Vertical integration of multiple silicon layers would resolve the issue of limited real estate on a chip by separating the photonic waveguides and devices from the microelectronics. Several schemes for fabricating multiple single-

[1]Portions of this chapter are reproduced with permission from [36].

crystalline silicon layers have been demonstrated, including wafer bonding [24], epitaxy [23], and separation by implantation of oxygen (SIMOX) [22] techniques. While in the future one or more of these methods may become feasible from a manufacturing standpoint, none of them is currently a standard CMOS fabrication technique.

Using only standard CMOS techniques, vertical integration could be achieved by depositing thin films of silicon. These films are not crystalline but rather are polycrystalline or amorphous, and therefore it is not immediately clear whether they have suitable optical and electrical properties. While waveguides made from hydrogenated amorphous silicon (a-Si:H) deposited by plasma-enhanced chemical vapor deposition (PECVD) have been demonstrated with propagation losses of a few dB/cm [51, 52], the electrical carrier mobility in such films is on the order of 1 $cm^2\,V^{-1}\,s^{-1}$ [53]. This value is around three orders of magnitude lower than the mobility in crystalline silicon. As a result, a-Si:H films are not appropriate for active devices such as electro-optic modulators, which are critical components for on-chip optical networks.

Polycrystalline silicon, or polysilicon, can have an electronic carrier mobility on the order of 100 $cm^2\,V^{-1}\,s^{-1}$ [25] and therefore may enable the integration of electrically active photonic devices with CMOS microelectronics. Polysilicon has largely been ignored by the photonics community due to the challenges introduced by its optical losses. A few exceptions include a three-dimensional photonic crystal with an infrared band gap [54], a MOS based electro-optic modulator which included a polysilicon gate built into a centimeter-length crystalline silicon waveguide [4], and passive polysilicon waveguides and ring resonators [30, 31, 32]. Optical material loss mechanisms in polysilicon are

dominated by scattering and absorption at the polysilicon grain boundaries, whose size and nature are greatly influenced by deposition and annealing conditions [30]. By using high temperature (1100 °C) anneals and special hydrogen plasma passivation steps, channel waveguides with losses as low as 9 dB/cm [31] and resonators with loaded quality factors of 7,000 [32] were demonstrated by Kimerling et al.

In this chapter we experimentally demonstrate high performance polysilicon photonic ring resonators with loaded quality factors of 20,000 for wavelength filtering applications [55] and show for the first time the ability to vertically integrate polysilicon structures with low loss single-crystalline materials. Additionally we examine the use of polysilicon for electro-optic modulators, which are important photonic devices for on-chip optical networks.

2.2 Fabrication

We fabricate high quality factor resonators as shown in Fig. 2.1. A 2 µm silicon dioxide layer is thermally grown on a four-inch silicon substrate and a thin film of amorphous silicon is subsequently deposited using low-pressure chemical vapor deposition (LPCVD) at 550 °C. Using atomic force microscopy (AFM), we measure the root mean square (RMS) surface roughness of this film to be 0.3 nm. In order to stabilize the smooth top surface during crystallization and limit the migration of silicon atoms, we allow a native oxide to grow [25] and to limit accidental oxidation we deposit 60 nm of silicon nitride by LPCVD. We then anneal the samples in N_2 at 600 °C, which crystallizes the amorphous silicon into polycrystalline silicon, and we further anneal several samples at 1100 °C, which

maximizes the crystallized fraction and removes defects from the crystalline regions [30, 31]. Finally we remove the silicon nitride layer in hot phosphoric acid. The final thickness of the film is 220 nm, and the final RMS surface roughness is measured by AFM to be 0.7 nm. XR-1541 e-beam resist is spun on to a thickness of around 100 nm and patterned by e-beam lithography (JEOL 9300), and the pattern is transferred by inductively coupled plasma reactive ion etching (ICP-RIE) using a chlorine-based silicon etch recipe (PlasmaTherm 770). Finally, a 3 µm SiO_2 cladding layer is deposited by PECVD at 400 °C.

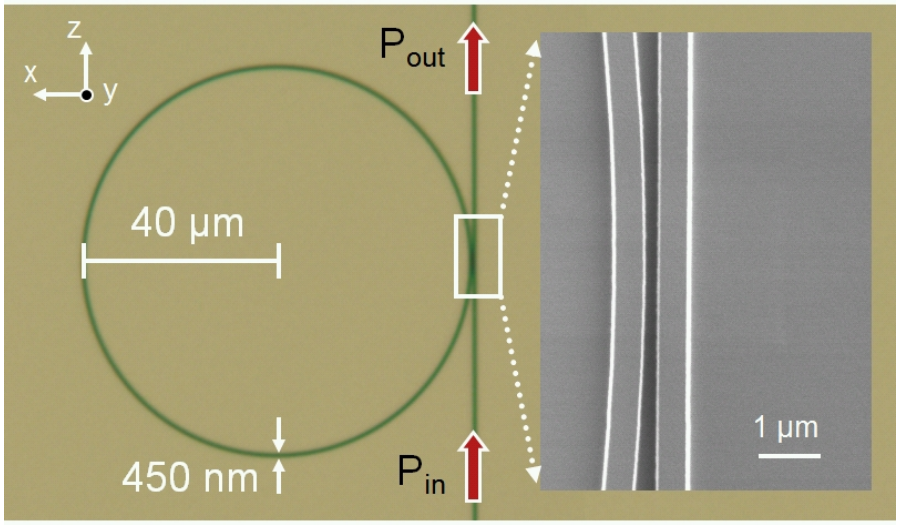


Figure 2.1: Optical microscope image and scanning electron microscope (SEM) inset of a polysilicon waveguide side coupled to a polysilicon ring resonator.

2.3 Characterization

We measure the transmission spectrum of the quasi-TM (*y*-polarized electric field) mode in order to determine the resonant properties of the device. A schematic of the test setup is shown in Fig. 2.3 and described as follows. Light from a tunable infrared laser is sent through a polarization controller, out of a

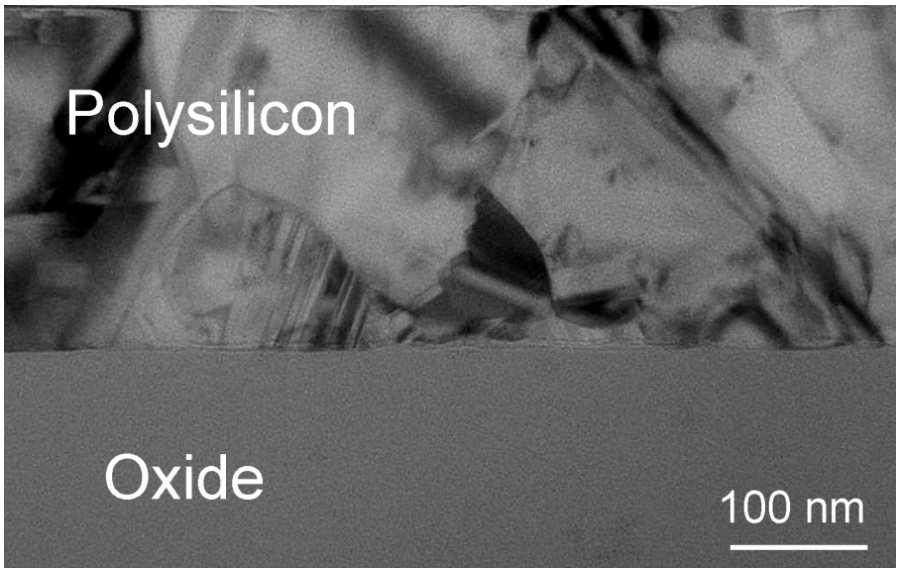


Figure 2.2: Cross-sectional transmission electron microscope (TEM) image of deposited polysilicon film (1100 °C anneal) showing crystalline grains separated by grain boundaries.

tapered lens fiber, and coupled on- and off-chip using adiabatic nanotapers at the ends of the patterned waveguides [7]. The output from the chip is collected by an objective lens, passed through a polarization filter, and measured with an infrared detector. The figures of merit for the microring as a wavelength filter are the loaded quality factor $Q_{loaded} \approx \lambda_0/\Delta\lambda_{FWHM}$ and the extinction ratio $ER = 10\log(P_{min}/P_{max})$, with $\Delta\lambda_{FWHM}$ the full width at half-maximum, P_{min} the transmission on resonance, and P_{max} the maximum transmission off resonance. The Q_{loaded} of a resonator coupled to a single waveguide is described as:

$$\frac{1}{Q_{loaded}} = \frac{1}{Q_0} + \frac{1}{Q_{coupling}} \tag{2.1}$$

where Q_0 is the intrinsic quality factor of the device and $Q_{coupling}$ arises from coupling to the bus waveguide. For a maximum extinction ratio, the critical coupling condition $Q_0 = Q_{coupling}$ should be met. This lowers the loaded Q to half the intrinsic value.

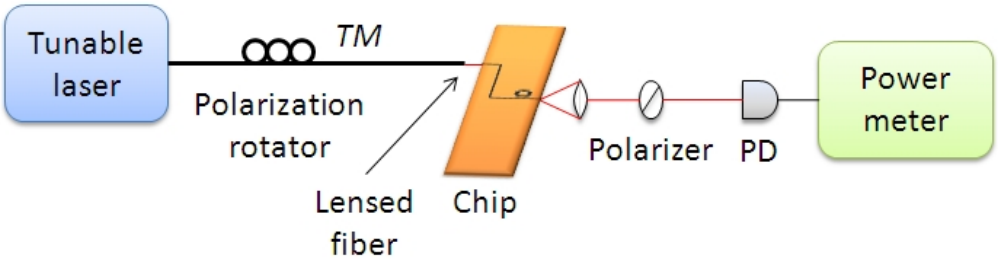
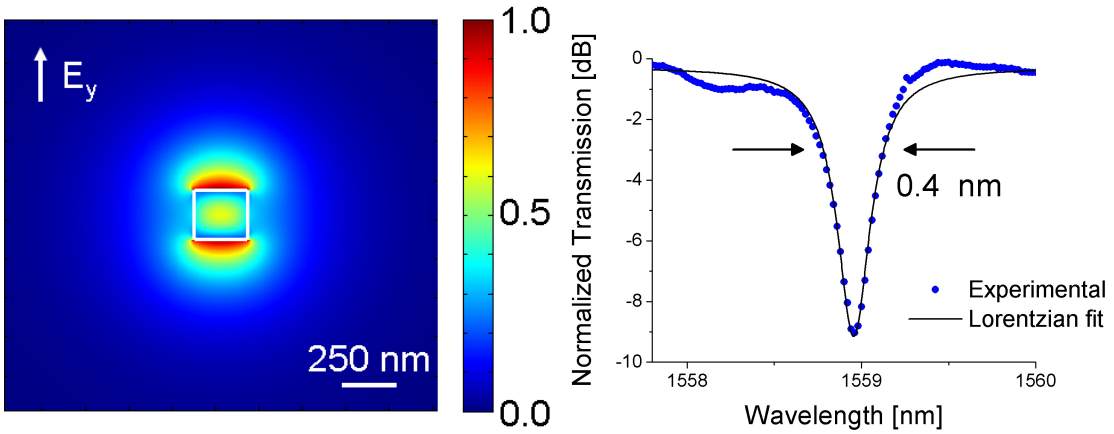


Figure 2.3: Experimental setup for measuring waveguide-integrated devices on a silicon chip.

First we examine polysilicon devices that were only annealed at 600 °C, just above the minimum temperature for crystallization. We design devices with a cross-section of 250 nm wide by 220 nm tall to slightly delocalize the optical mode. This causes the mode to have a lower confinement factor [56] in the waveguide core (as discussed in the next chapter) and experience less modal loss due to material loss in the polysilicon. The mode profile for the quasi-TM (y-polarized) mode of such a waveguide surrounded by SiO_2 cladding is shown in Fig. 2.4a and we find $n_{eff} = 1.56$ using a finite difference mode solver. Figure 2.4b shows a transmission spectrum for a 40 µm radius ring with $\Delta\lambda_{FWHM} = 0.4$ nm and $Q_{loaded} = 3,900$. Based on the Q and extinction ratio, we estimate the loss in the ring to be 60 dB/cm.

Next we examine devices annealed at a maximum temperature of 1100 °C and find significantly reduced losses, even for a 450 nm by 220 nm with a larger silicon confinement. The mode profile of such a polysilicon waveguide is shown in Fig. 2.5a, as simulated by a finite element mode solver. The effective index of the TM-polarized mode is calculated to be $n_{eff} = 1.76$ at $\lambda = 1550$ nm using $n_{Si} = 3.48$ and $n_{oxide} = 1.46$. Figure 2.5b shows a transmission spectrum for a 40 µm radius ring with $\Delta\lambda_{FWHM} = 0.079$ nm, $Q_{loaded} = 20,000$ and a maximum extinction ratio of 24 dB, indicating that the resonator is nearly critically coupled.



(a) (b)

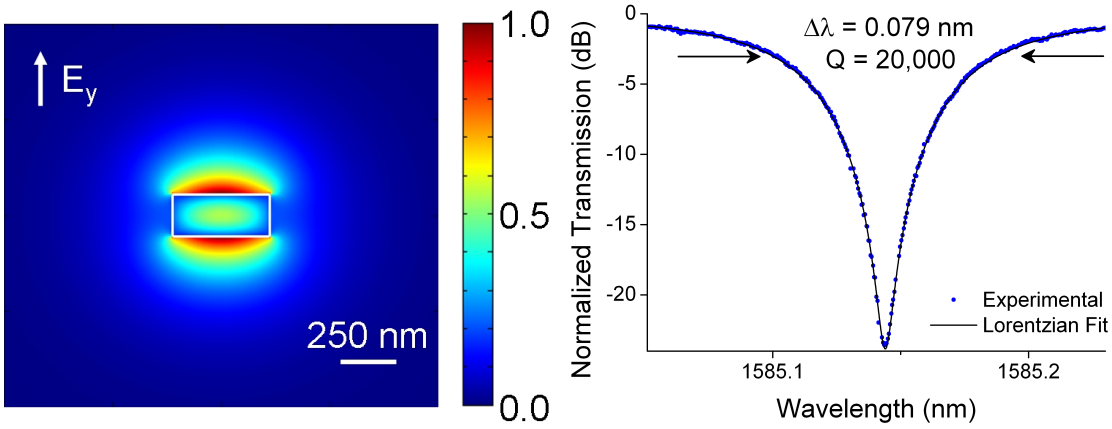
Figure 2.4: Polysilicon microring resonator annealed at a maximum temperature of 600 °C. (a) Quasi-TM polarized optical mode of a polysilicon waveguide with 250 nm wide × 220 nm tall cross-section calculated with a finite element mode solver. (b) Transmission spectrum for a 40 µm radius polysilicon ring resonator.

The group index n_g can be calculated from the measured free spectral range (FSR) and the path length L as $n_g \approx \lambda_0^2/(FSR)(L)$ [57]. From the measured free spectral range of 2.345 nm, we calculate $n_g = 4.26$ near $\lambda_0 = 1585$ nm. When critically coupled to a single bus waveguide, Q_{loaded} can be written as [57]:

$$Q_{loaded} = \frac{1}{2}Q_0 = \frac{\pi n_g}{\lambda_0 \alpha_{ring}} \tag{2.2}$$

where α_{ring} is the total propagation loss per unit length in the ring. Using Eq. 2.2 we estimate a propagation loss in the ring $\alpha_{ring} = 18$ dB/cm and an intrinsic quality factor $Q_0 = 40,000$.

The refractive index of the film is approximately equal to its value in crystalline silicon because the volume of the polycrystalline film is mostly single crystalline, but interspersed with nanometer-thin amorphous grain boundaries. To compare the relative size of the crystalline grains to the size of our waveguides, we use a defect etching scheme. First we perform a partial thermal ox-



(a) (b)

Figure 2.5: Polysilicon microring resonator annealed at a maximum temperature of 1100 °C. (a) Quasi-TM polarized optical mode of a polysilicon waveguide with 450 nm wide × 220 nm tall cross-section calculated with a finite element mode solver. (b) Transmission spectrum for a 40 µm radius polysilicon ring resonator.

idation of an unclad sample which has polysilicon waveguides. During this process, oxygen diffuses quickly into the amorphous silicon grain boundaries and oxidizes the boundaries more rapidly than the crystalline grains [25]. After wet etching the grown oxide with hydrofluoric (HF) acid, we are then able to observe the grain size of the polycrystalline silicon using a standard top-down SEM. Figure 2.6 shows an SEM image of the coupling region between a ring and a waveguide in a defect etched polysilicon sample. We estimate an average grain size of 300 nm using the line-intercept method [58]. This measured average grain size is comparable to reported values for similarly prepared polysilicon films [30]. Using a first-order approximation of each grain as a 300 nm crystalline silicon cube with 1 nm thick amorphous silicon boundary on each surface, we can estimate that the volume of our polysilicon film is more than 97% crystalline.

For on-chip optical networks where the flow of light is dynamically con-

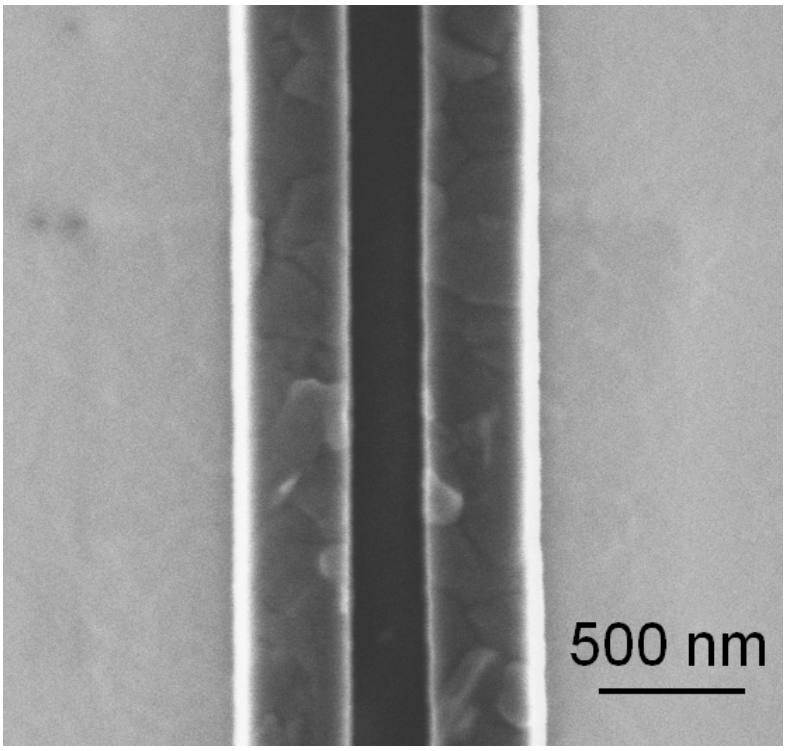


Figure 2.6: Coupling region between two defect etched polysilicon waveguides showing an average grain size of approximately 300 nm.

trolled, we expect both the electrical and optical properties of polysilicon to support ring resonator-based active devices such as switches and modulators. Plasma dispersion is the dominant electro-optic effect in silicon [59] and is the mechanism for high speed signal modulation. From the relation between the index of refraction and the carrier concentration [59] we find that a carrier concentration of $\Delta N = \Delta P = 3.4 \times 10^{16}\,\mathrm{cm}^{-3}$ shifts the refractive index of the polysilicon by $\Delta n = -1.7 \times 10^{-4}$. Using a finite element mode solver program, we estimate a corresponding shift in the modes effective index of $\Delta n_{eff} = -8.6 \times 10^{-5}$ and a shift of the resonant wavelength in Fig. 2.5b of $\Delta\lambda = -0.079\,\mathrm{nm}$. This gives rise to a modulation depth as high as 22 dB. The required carrier concentration is comparable to that used in state of the art ring resonator-based GHz electro-optic modulators in crystalline silicon [60]. The electrons and holes can be introduced

either optically using a pump beam, or electrically using a PIN diode. Polysilicon electrical devices such as diodes and transistors are commonly used in thin-film displays [25]. This is possible because adequately doped polysilicon films (on the order of 1×10^{17} cm^{-3}) can have electrical carrier mobility and resistivity within about an order of magnitude of their values in crystalline silicon [25].

2.4 Integration with Crystalline Silicon Waveguides

To demonstrate the suitability of the polysilicon platform for vertical integration, we fabricate resonators which are offset-vertically coupled to low-loss waveguides of a different material (in this case, crystalline silicon). The integration of deposited active devices with low-loss bus waveguides would enable massive integration of photonic networks on chip. While our demonstration uses crystalline silicon to efficiently guide light to and from polysilicon resonators, any low-loss optical material could be used in a final system. For example, amorphous silicon [51, 52] or silicon nitride [61, 62] films could be deposited and patterned into low-loss waveguides above or below the polysilicon rings. By depositing layers of two different materials, one can take advantage of the benefits of each; for instance, an optical network could use the electrical characteristics of polysilicon for active switching devices, while still benefiting from the optical properties of amorphous silicon to guide light over centimeter-long distances on chip.

The processing steps to fabricate polysilicon resonators over SOI waveguides are shown in Fig. 2.7, as generated in the ATHENA process simulator from

SILVACO[2]. For the crystalline substrate we use an SOI wafer containing a 3 µm buried oxide layer and a 250 nm thick crystalline silicon layer. Waveguides are patterned in the crystalline silicon layer by e-beam lithography and RIE, shown in Fig. 2.7(a), and a 350 nm film of oxide is deposited from a tetraethoxysilane (TEOS) precursor by PECVD, shown in Fig. 2.7(b). We then deposit a 250 nm thin film of amorphous silicon in an LPCVD furnace tube and carry out crystallization anneals at 600 °C and 1100 °C, shown in Fig. 2.7(c), as in Section 2.2. Racetrack resonators with different radii and coupling lengths are then patterned in the polysilicon layer by e-beam lithography and RIE, shown in Fig. 2.7(d). Finally, we deposit a PECVD oxide cladding, shown in Fig. 2.7(e). Note that the process does not include the use of chemical mechanical polishing (CMP). In order to ensure that the racetrack is not located on the hill created by the non-planar surface, a center-to-center horizontal offset larger than 800 nm is needed between the resonator and the adjacent waveguide. We use racetrack resonators to increase the coupling between the waveguides and the resonator in this arrangement. We also use waveguides and resonators with a 350 nm wide cross section to decrease the optical confinement and therefore increase the coupling as compared to 450 nm wide structures.

The fabricated structure is shown in Fig. 2.8a before oxide cladding, as in Fig. 2.7d. In Fig. 2.8b we show the quasi-TM spectrum of a structure with a racetrack of radius r = 40 µm and a coupling region length L_0 = 3 µm. Note that for these dimensions the resonator is undercoupled at shorter wavelengths but comes closer to critically coupled at longer wavelengths. At wavelengths near λ_0 = 1600 nm, the FSR is measured to be 2.3 nm and the group index is calculated to be n_g = 4.33. We measure Q_{loaded} values over 4,000 and extinction ratios near

[2]SILVACO International, 4701, Patrick Henry Drive, Blg 1, Santa Clara, California.

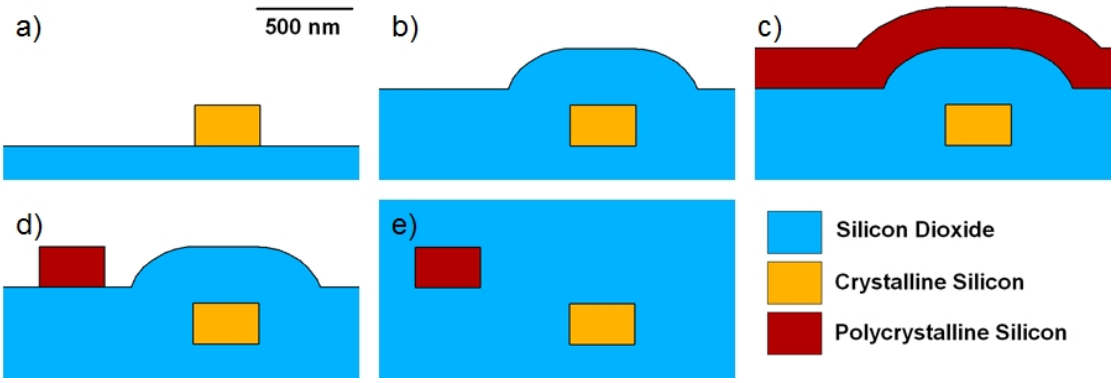
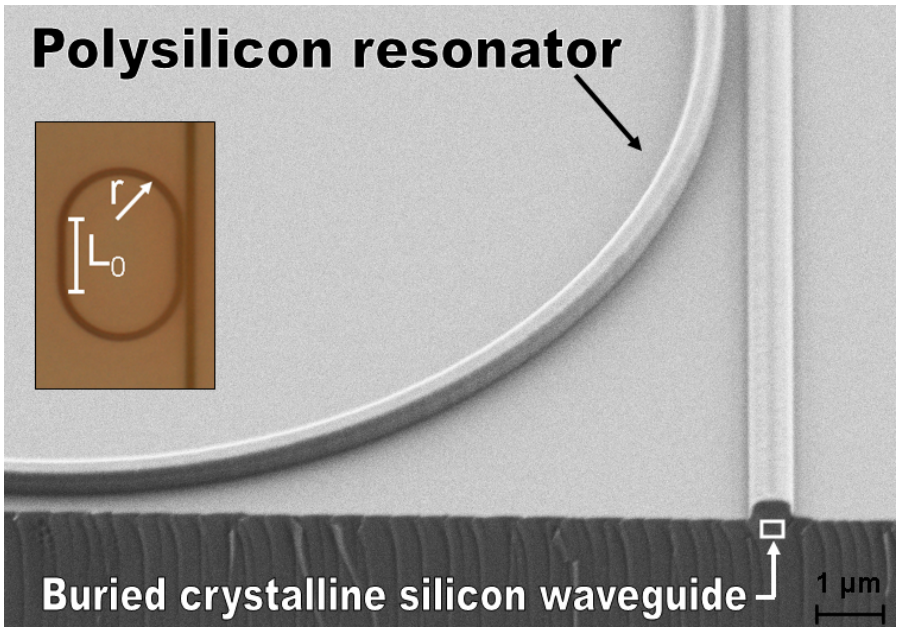


Figure 2.7: Process flow for vertical coupling sample. (a): Definition of crystalline silicon waveguides by e-beam lithography and etching. (b): Deposition of TEOS oxide by PECVD. (c): Deposition of amorphous silicon layer, and anneal steps to crystallize amorphous silicon to polycrystalline silicon. (d): Definition of polysilicon resonators by e-beam lithography and etching. (e): Deposition of oxide cladding by PECVD.

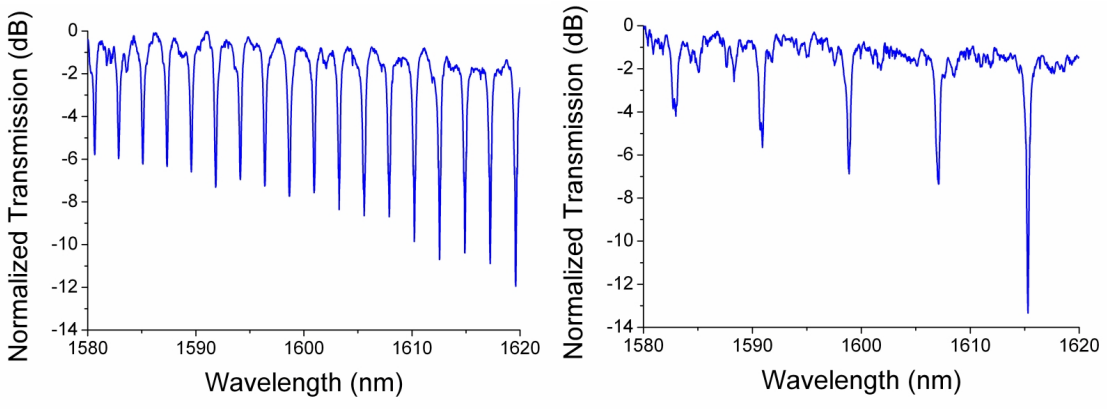
10 dB. Figure 2.8c shows a smaller racetrack with $r = 10\,\mu m$ and $L_0 = 5\,\mu m$. Here we measure once again Q_{loaded} values approaching 4,000 and extinction ratios greater than 10 dB, but with a larger free spectral range of 8.08 nm near $\lambda_0 = 1600\,nm$. We calculate the group index to be $n_g = 4.35$.

2.5 Discussion

We have demonstrated CMOS-compatible polysilicon resonators with intrinsic Q_0 values of 40,000. The primary limitations on Q are scattering from sidewall roughness, scattering due to a refractive index difference between the crystalline grains and amorphous silicon grain boundaries, and absorption due to dangling bonds at the amorphous grain boundaries. Lower losses and higher Q values could be achieved by implementing hydrogen passivation of the dangling bonds at the polysilicon grain boundaries [31].



(a)



(b) (c)

Figure 2.8: Polysilicon racetrack resonators coupled to crystalline silicon waveguides. (a): Cross-section SEM of the structure before top oxide cladding. Inset: Definition of r and coupling length L_0. (b) and (c): Quasi-TM polarized transmission as a function of wavelength for (b) r = 40 µm, L_0 = 3 µm and (c) r = 10 µm, L_0 = 5 µm.

We have also demonstrated for the first time to our knowledge a mixed-silicon optical system, in this case crystalline silicon waveguides coupled vertically to polysilicon resonators with Q_{loaded} values of 4,000. A previous demonstration of vertical coupling used polysilicon for both the waveguide and the

resonator and Q_{loaded} values of 1,000 were shown [63]. We could increase both the Q values and the amount of coupling by using a planarization step such as CMP. The rings or racetracks could then be placed directly above the waveguides, increasing the quasi-TM mode overlap and coupling even for larger vertical separations. Also, the polishing step could produce a smoother oxide surface to deposit silicon onto, potentially making lower loss polysilicon films with higher Q values.

The maximum processing temperature is an important consideration for the integration of photonics with CMOS microelectronics. Polysilicon processed at 1100 °C is compatible with front end of the line fabrication, above the crystalline silicon transistor layer but below the metal interconnect layers and before ion implantation. The polysilicon layer could also be introduced on top of the metal interconnect layers after all of the electrical processing is completed. In order to achieve this, the annealing temperature could be reduced below 450 °C using excimer laser annealing. This technique has been demonstrated to crystallize low temperature amorphous silicon into large-grain polycrystalline silicon for thin film transistors [64, 65] and we shall investigate its use in Chapter 7. With grain sizes in these films on the order of micrometers, an entire photonic device could fit within a single grain and exhibit near-single crystalline behavior.

CHAPTER 3

SLOT WAVEGUIDE MICRORING RESONATORS FOR LIGHT EMISSION

We demonstrate horizontal slot waveguides using high-index layers of polycrystalline and single crystalline silicon separated by a 10 nm layer of silicon dioxide. We measure waveguide propagation loss of 7 dB/cm and a ring resonator intrinsic quality factor of 83,000. The electric field of the optical mode is strongly enhanced in the low-index oxide layer, which can be used to induce a strong modal gain when an active material is embedded in the slot. Both high-index layers are made of electrically conductive silicon which can efficiently transport charge to the slot region. The incorporation of conductive silicon materials with high-Q slot waveguide cavities is a key step for realizing electrical tunneling devices such as electrically pumped silicon-based light sources[1].

3.1 Introduction

The remaining critical capabilities yet to be demonstrated on the integrated silicon photonic platform using standard microelectronic fabrication processes are electrically pumped amplification and lasing within a silicon waveguide [66]. Silicon is an excellent waveguide material because it is transparent in the telecommunications band at $\lambda = 1550\,\text{nm}$ and can be processed inexpensively, but it is a poor gain material due to its indirect bandgap. Therefore it is advantageous to combine a silicon waveguide structure with a more efficient 1550 nm gain material for on-chip applications. Electrically pumped lasers have been demonstrated with III-V materials evanescently coupled to a silicon waveguide [47, 11], however these approaches rely on a wafer bonding step which

[1] Portions of this chapter are reproduced with permission from [37].

is low throughput and not currently a standard microelectronic fabrication process. Optically pumped lasing has been shown in erbium-doped oxide structures [67, 68], but electrical pumping of insulating materials is not straightforward.

One possible solution for electrically pumped amplification within a silicon waveguide is to combine an erbium-doped insulator with the slot waveguide geometry [69, 70, 71]. A slot waveguide is formed by separating two regions of high refractive index by a subwavelength slot of low refractive index. A guided optical mode with a polarization normal to the slot interface (the "slot mode") has a large electric field enhancement within the low-index slot region [72, 73] which supports an efficient conversion of material gain to modal gain [56]. Figure 3.1 demonstrates the field enhancement in a horizontal slot of silicon dioxide ($n_{oxide} = 1.46$) in a silicon waveguide ($n_{Si} = 3.48$). The low-index region could be an erbium-doped silicon-rich oxide [74] or nitride [75] that is electrically excited by carrier tunneling through the slot region and emits into the waveguide mode. Erbium-doped films can be fabricated by standard techniques such as ion implantation or sputter deposition and do not require a wafer bonding step. Previous work in amorphous silicon slot waveguides has yielded promising optical results [76, 77, 78], however the typical electrical mobility is too low for an efficient on-chip electrical device.

Slot waveguides are attractive for light emission and amplification because they provide a strong electric field enhancement in the slot region [72, 73] which can be filled with an active material. The mode overlap induces an efficient conversion of the slot's local material gain g_{slot} to a modal gain g_{modal}, resulting in a large waveguide power amplification $P(z) = P(0)\exp(g_{modal}z)$. The percent

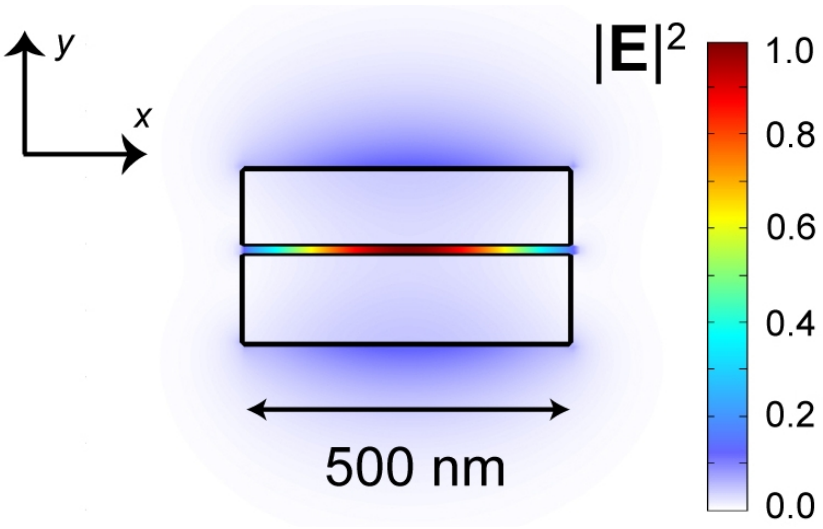


Figure 3.1: $|\mathbf{E}|^2$ of the fundamental y-polarized quasi-TM slot mode at $\lambda = 1550\,\text{nm}$ as calculated by a finite difference mode solver. The high-index regions (bounded by black) have $n_{Si} = 3.48$ and the slot and cladding have $n_{oxide} = 1.46$. The bottom and top silicon layers are 140 nm tall and 120 nm tall respectively, and the slot is 10 nm tall. The effective index is $n_{eff} = 1.87$ and the slot confinement factor [56] is $\Gamma = 0.28$.

of material gain converted to modal gain is characterized by $\Gamma = g_{modal}/g_{slot}$, the confinement factor [56, 79]:

$$\Gamma = \frac{n_{slot} \iint\limits_{slot} |\mathbf{E}|^2 \, dxdy}{Z_0 \iint\limits_{\infty} \text{Re}\{\mathbf{E} \times \mathbf{H}\} \cdot \hat{\mathbf{z}} \, dxdy} \tag{3.1}$$

where n_{slot} is the real part of the refractive index of the slot region, Z_0 is the impedance of free space, $\hat{\mathbf{z}}$ is the direction of propagation, and $\mathbf{E}$ and $\mathbf{H}$ are the mode's electric and magnetic fields. A slot mode provides high electric field intensity in the slot ($\varepsilon|\mathbf{E}|^2$) per unit power in the waveguide mode ($\mathbf{E} \times \mathbf{H}$), satisfying the condition for large Γ even for a deeply subwavelength slot size that allows for electrical tunneling.

In this chapter we design, analyze, and experimentally demonstrate a novel silicon slot waveguide structure with geometry and materials suitable for elec-

trical pumping of an active gain material.

3.2 Device Design

The key considerations in designing a slot waveguide suitable for electrical injection are the waveguide geometry, orientation, and choice of materials. To keep the operating voltage of the proposed device at reasonable levels, we choose the size of the oxide slot to be 10 nm. This allows for future electrical excitation of a gain material by Fowler-Nordheim tunneling through oxide with a voltage drop across the slot on the order of volts, since the onset of tunneling is typically around 5 MV/cm = 0.5 V/nm of tunneling distance [69]. In order to achieve low losses with such a small slot size, we choose the horizontal slot configuration. This way the different waveguide regions can be formed by deposition or growth techniques with nanometer-scale accuracy and subnanometer surface roughness. This is in contrast to a vertical slot which must be defined lithographically and etched down into a silicon waveguide [72, 73] which is difficult for a slot size below 50 nm.

We choose a top layer of polysilicon to provide good electrical conductivity for the device. Ideally, crystalline silicon (c-Si) would be used for both the top and bottom layers, but multiple layers of c-Si can only be obtained by nonstandard techniques such as wafer bonding [80], epitaxial overgrowth [81], or oxygen implantation [22]. Hydrogenated amorphous silicon (a-Si:H) can be used in horizontal slot waveguides with good loss values $\approx 2 - 4$ dB/cm [76, 77, 78, 82], but this material is poorly suited for the proposed electrical-injection device due to very low electrical carrier mobility. Optical-quality thin films of a-Si:H

are deposited by plasma enhanced chemical vapor deposition (PECVD) at low temperatures, typically around 200 °C [83, 84, 51]. At these temperatures a significant atomic percentage of hydrogen is incorporated in the material to fill dangling Si bonds [85] and prevent optical loss by absorption. Despite their excellent optical properties, a-Si:H films suffer from low electrical carrier mobility μ on the order of $1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [85] (corresponding to high resistivity $\rho \propto 1/\mu$). In contrast, the electrical mobility of polycrystalline silicon can be much better, on the order of $100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [25]. Drift current density through a material is defined as $\mathbf{J} = nq\mu\mathbf{E}$ (with n the carrier density, q the electron charge, and $\mathbf{E}$ the voltage per length applied across the material), so a 100× decrease in μ implies that a 100× higher voltage will be required to inject the same current $\mathbf{J}$ through a material. For example, if a voltage drop of a few volts is required across a polysilicon slab connecting a metal contact to the waveguide, then a few hundred volts may be required across a similar a-Si:H electrode. This presents serious design challenges for the realization of a reliable and efficient on-chip device using a-Si:H.

In this work we use a layer of deposited polysilicon, which exhibits good electrical properties. Polysilicon is a standard deposited microelectronic material that consists of crystalline grains separated by disordered grain boundaries. Polysilicon has typically been considered a poor optical material not suitable for low-loss applications because it is inhomogeneous and inherently has some optical loss due to scattering. However, channel waveguides have recently been demonstrated with losses on the order of 10 dB/cm or less [31, 36, 33] when the material is processed to have smooth interfaces and a maximized grain size such that only a few grain boundaries are present per waveguide cross-section. Here we demonstrate the first use of optical-quality polysilicon in a slot waveguide

configuration, with the primary goal of minimizing the waveguide loss inside a resonator for light emission applications.

3.3 Fabrication

Fabrication of the slot waveguides, shown in Fig. 3.2, is done on a commercial four-inch silicon-on-insulator wafer. We start with a 250 nm layer of single-crystalline silicon on a 3 µm buried oxide layer, then thin the top silicon layer to 145 nm by thermal oxidation and remove the grown oxide with hydrofluoric acid. Then we grow a 10 nm silicon dioxide layer for the slot region using dry thermal oxidation at 950 °C. This leaves a 140 nm bottom layer of c-Si. Using atomic force microscopy (AFM), we measure the root mean squared (r.m.s.) roughness of the top oxide interface to be below 0.2 nm. We deposit a 120 nm top layer of amorphous silicon by low pressure chemical vapor deposition (LPCVD) at 550 °C and anneal the wafer in N_2 at a maximum temperature of 1100 °C to crystallize the film into polysilicon [36]. We determine the r.m.s. roughness of the top surface to be 0.5 nm by AFM, as shown in Fig. 3.3. A cross-sectional transmission electron microscope (TEM) image is shown in Fig. 3.4, where the polycrystalline nature of the top layer is visible. The layer thicknesses are chosen to optimize the modal confinement Γ in the slot region for the final waveguide structure [56]. To pattern waveguides and resonators, we use e-beam lithography (JEOL 9300) and a 100 nm layer of XR-1541 e-beam resist before etching the structures with chlorine-based inductively coupled plasma reactive ion etching (PlasmaTherm 770). A sequence of silicon etching, oxide etching, and silicon etching is used to transfer the pattern through all of the layers. Finally, we clad the structures in a 3 µm PECVD silicon dioxide layer before

dicing and polishing the end facets of the chip.

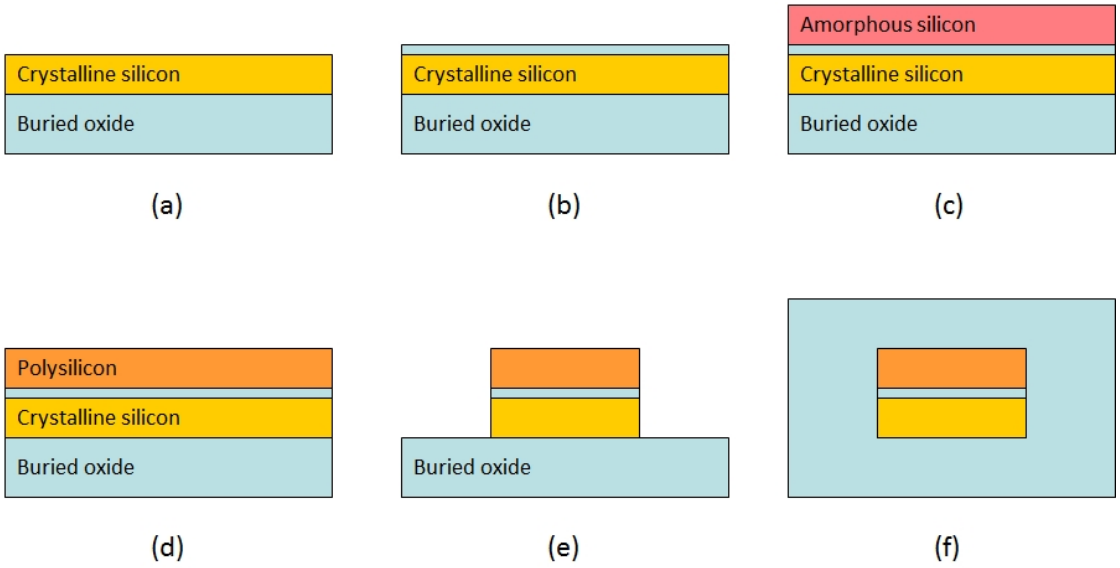


Figure 3.2: Fabrication steps for horizontal slot waveguide. (a) SOI wafer with top layer thinned to 140 nm. (b) Oxidation growth of 10 nm SiO_2 layer. (c) Deposition of LPCVD a-Si. (d) Crystallization anneal to form polysilicon. (e) Lithography and etching to form waveguide structure. (f) PECVD oxide cladding.

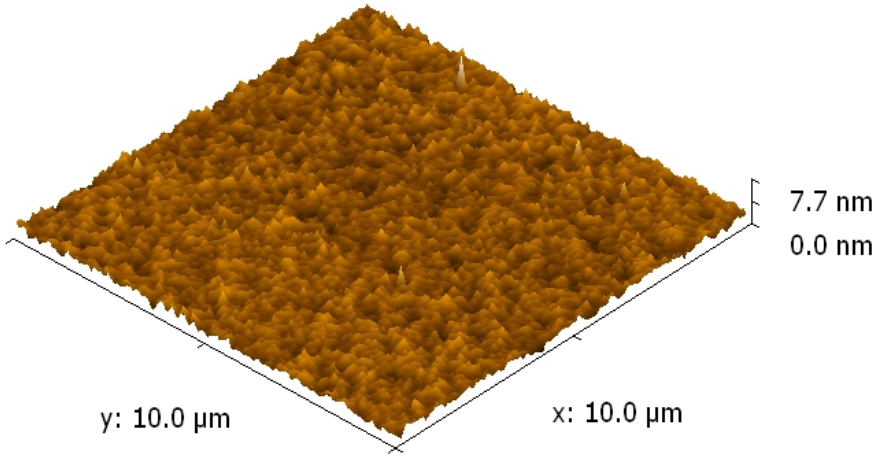


Figure 3.3: AFM measurement of the polysilicon top surface over a 10 µm square field. The rms roughness is 0.5 nm and the total range is ±3.7 nm from the mean value.

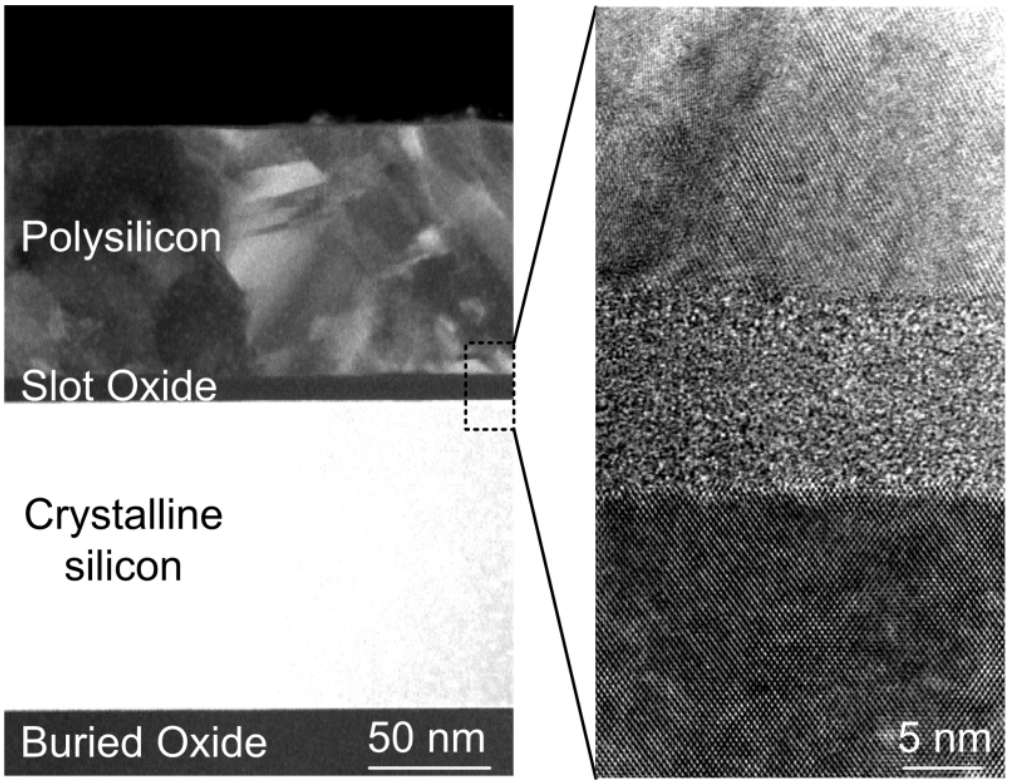


Figure 3.4: a) Dark field STEM (scanning tunneling electron microscope) image of the fabricated material stack. (b) Bright field TEM image of the slot region showing the polycrystalline, amorphous, and single crystalline layers (top to bottom).

3.4 Experiment

We measure the loss in 500 nm-wide waveguides (see Fig. 3.1) by employing the cutback method with multiple waveguides of increasing path length, shown in Fig. 3.5. Light from a tunable infrared laser passes through a polarization controller and is coupled on- and off-chip using a tapered lens fiber and patterned waveguide nanotapers [7]. Output from the chip is collected by a lens and focused through a polarization filter onto a detector. At a given wavelength, we record the transmission through each waveguide and plot the relative transmission on a logarithmic plot as shown in the inset of Fig. 3.6. The slope of a linear fit gives the waveguide loss, which we calculate to be 7.3 dB/cm at $\lambda = 1550$ nm

with a standard error of 0.4 dB/cm. Figure 3.6 shows the same measurement repeated at many wavelengths, and we find losses of around 6-8 dB/cm within the C-band emission window of erbium.

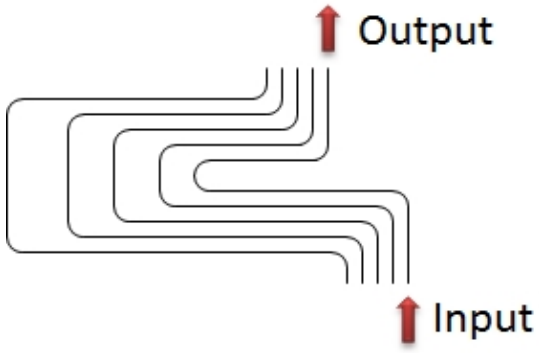


Figure 3.5: Diagram of chip layout used for the "cutback method" approach of measuring waveguide loss.

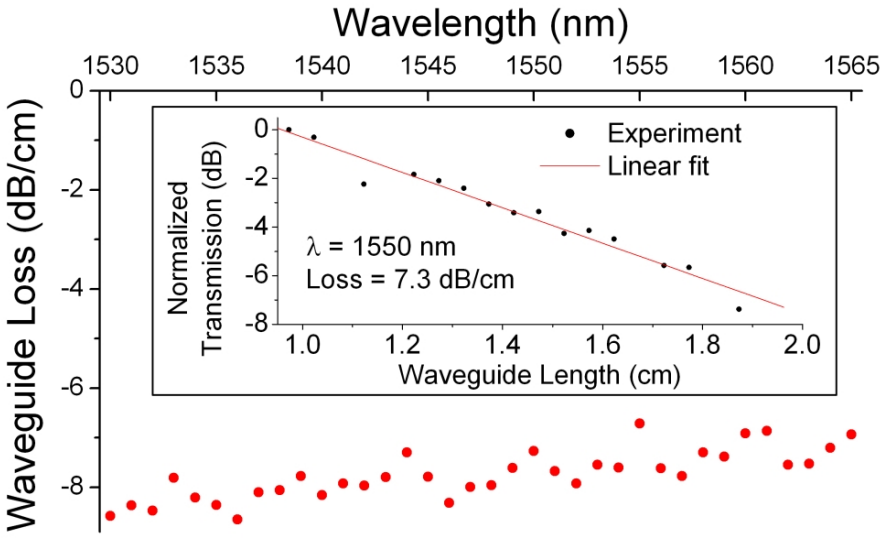


Figure 3.6: Measurement of propagation loss in slot waveguides using the cutback method. (inset) Single measurement at $\lambda = 1550$ nm with a loss of 7.3 ± 0.4 dB/cm.

We also demonstrate high-quality-factor ring resonator cavities based on these horizontal slot waveguides. In order to minimize excess bending, scattering, and coupling loss in the resonator, we choose a relatively large 100 µm radius ring coupled to a bus waveguide with a coupling gap of 550 nm as shown

in Fig. 3.7(a). Using the radius of the ring and the measured free spectral range (FSR) as a function of wavelength in the inset of Fig. 3.7(c), we can calculate the group index $n_g(\lambda) = \lambda^2/(FSR \times 2\pi R)$ [36]. A comparison to finite difference modal simulations in Fig. 3.7(b) provides strong experimental evidence that we are indeed operating in the TM-polarized slot mode. A close scan of a resonance at $\lambda_0 = 1552.12\,\text{nm}$ is shown in Fig. 3.7(c). We measure a resonant linewidth $\Delta\lambda_{FWHM} = 29\,\text{pm}$ which corresponds to an undercoupled quality factor $Q_{loaded} =$ 54,000. We fit this resonance to a Lorentzian of the form [86]:

$$T = \frac{(a-r)^2 + \frac{4\pi^2 raL^2 n_g^2}{\lambda_0^4}(\lambda-\lambda_0)^2}{(1-ra)^2 + \frac{4\pi^2 raL^2 n_g^2}{\lambda_0^4}(\lambda-\lambda_0)^2} \tag{3.2}$$

where L is the path length around the ring, $n_g = 3.50$ is the measured group index, and our two fitting parameters are a coupling term r and a loss term a. The least squares Lorentzian fit with values $a = 0.948$ and $r = 0.978$ is shown in Fig. 3.6(c). This corresponds to a propagation loss within the ring $\alpha_{ring} = -2\ln(a)/L = 1.7\,\text{cm}^{-1} = 7.4\,\text{dB/cm}$ and an intrinsic quality factor $Q_0 = (2\pi n_g)/(\lambda_0 \alpha_{ring}) = 83{,}000$ [36]. The loss calculated in the resonator matches closely with the straight waveguide loss measurement in Fig. 3.4. This indicates that excess bending loss and coupling loss in the resonator are negligible (within the error of the waveguide measurement) due to the large ring radius (100 µm) and coupling gap (550 nm).

3.5 Discussion

Slot waveguides provide a large electric field confinement in a low-refractive-index material (Eq. 3.1) which can provide a strong interaction with a gain material for amplification and light emission. We calculate the waveguide presented

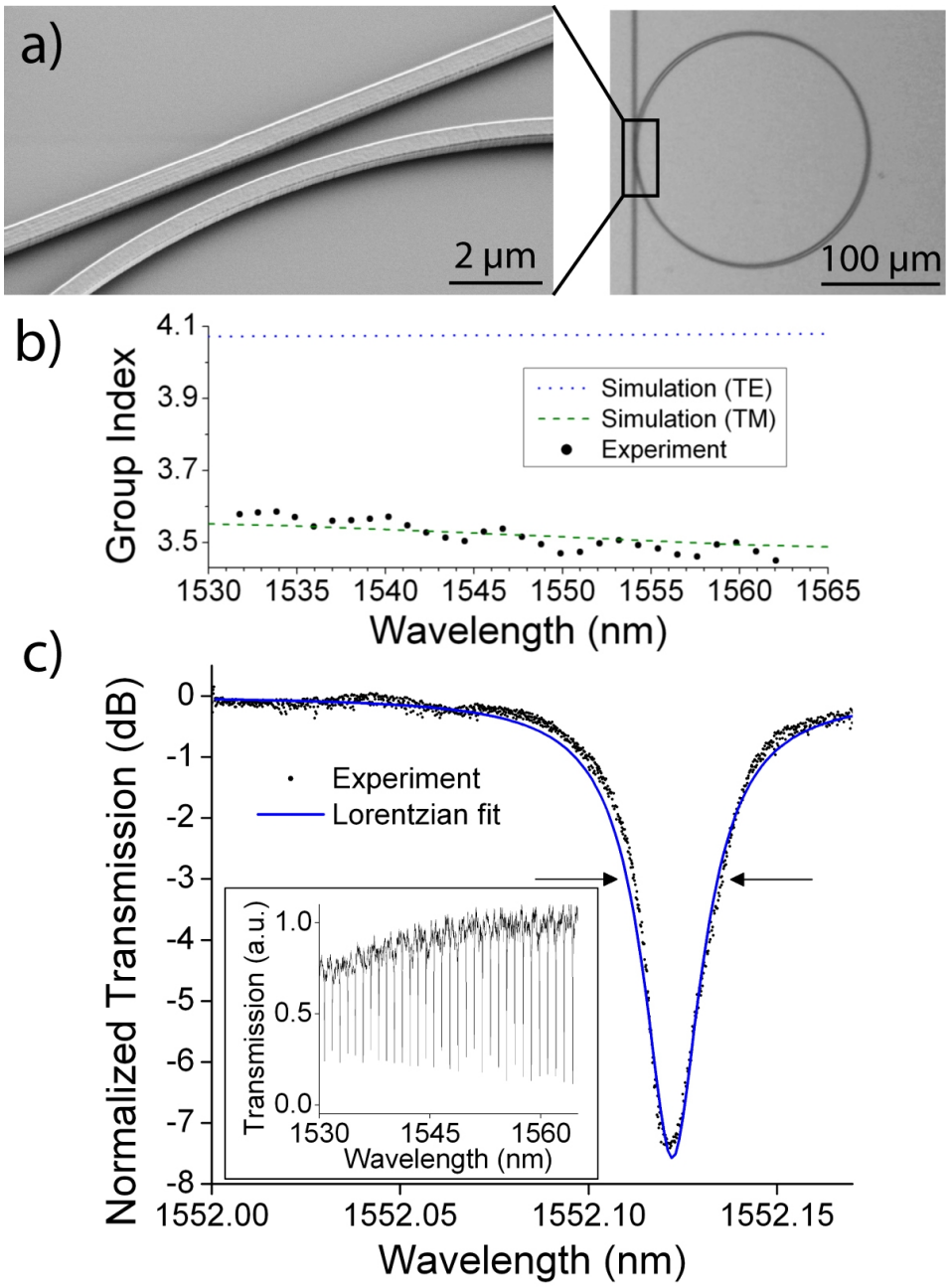


Figure 3.7: (a) Tilted angle SEM (before oxide cladding) and optical microscope image of 100 μm radius ring resonator and bus waveguide. (b) Experimental measurement (dots) of the group index based on the measured free spectral range as a function of wavelength. The comparison with simulation indicates we are operating in the TM-polarized slot mode shown in Fig. 3.1. (c) Resonance at $\lambda_0 = 1552.12$ nm with intrinsic quality factor $Q_0 = 82{,}000$. (inset) Wider sweep showing FSR used to calculate group index in (b).

here to have confinement $\Gamma = 28\%$ inside the 10 nm slot at $\lambda = 1550$ nm. This is close to the fully optimized value of $\Gamma_{max} = 33\%$ for a 10 nm oxide slot in silicon [56].

Based on typical material gain values and our waveguide geometry, we can calculate the minimum waveguide loss α required to achieve lasing in these structures. Given a typical emission cross section $\sigma_{Er} = 6 \times 10^{-21}\,\mathrm{cm}^2$ for erbium ions in silica [87, 88] and an average erbium doping concentration $n_{Er} = 2 \times 10^{20}\,\mathrm{cm}^{-3}$ [87, 88], one could expect a material gain $g_{slot} = \sigma_{Er} n_{Er} = 1.2\,\mathrm{cm}^{-1} = 5.2\,\mathrm{dB/cm}$ which can be inserted into the slot. Given confinement $\Gamma = 0.3$ determined by the waveguide geometry, we then require a maximum propagation loss $\alpha = g_{modal} = \Gamma g_{slot} = 1.6\,\mathrm{dB/cm}$ in order to reach the laser oscillation condition, or equivalently a minimum resonator intrinsic quality factor $Q_0 = (2\pi n_g)/(\lambda_0 \alpha) = 400{,}000$ with $n_g = 3.5$ and $\lambda_0 = 1550$ nm.

Future generations of these devices will therefore require either an increase in confinement Γ or a decrease in propagation loss α to achieve lasing. Waveguides can be designed with multiple slots to increase both Γ and the achievable gain g_{modal} without significantly increasing the propagation loss α [76]. The inclusion of two 10 nm slots separated by 50 nm of silicon can result in confinement factors $\Gamma > 50\%$, thereby increasing the acceptable waveguide losses to around 3 dB/cm. Several approaches then exist for the moderate loss reduction required from 7 dB/cm to 3 dB/cm. We estimate that 2-3 dB/cm of the current 7 dB/cm loss comes from sidewall scattering and absorption (similar to that seen in c-Si [89]) and the remaining 4-5 dB/cm of waveguide loss is due to material loss (absorption and scattering) in the polysilicon [31]. Several methods used to successfully reduce sidewall loss in c-Si include roughness reduction

by e-beam resist smoothing (pre-etching) [89] and waveguide surface smoothing and passivation by oxidation (post-etching) [90]. Additionally, it has been reported that hydrogen passivation of grain boundary states inside polysilicon improves the material loss by several dB/cm [31]. Conservatively, we expect that greater than 50% improvement is achievable in both of the loss categories, which would result in the required overall loss reduction from our measured value of 7 dB/cm.

In conclusion, we have demonstrated horizontal slot waveguides and resonators designed for efficient electrical injection by incorporating electrically active high-index materials suitable for electrodes and a 10 nm thin oxide slot suitable for carrier tunneling. This class of structures may enable on-chip silicon-based amplifiers and light sources when combined with a suitable gain material in the slot (such as an erbium-doped silicon-rich oxide or nitride) and a forward-biased PIN diode for carrier injection.

CHAPTER 4

ALL-OPTICAL MODULATORS

We experimentally demonstrate on-chip active photonic devices fabricated from deposited polycrystalline silicon. The demonstrated modulator is based on all-optical carrier injection in a micrometer-size resonator and has a modulation depth of 10 dB and a temporal response of 135 ps. Grain boundaries in the polycrystalline silicon (polysilicon) material result in faster electron-hole recombination, enabling a shortened carrier lifetime and a faster optical switching time compared to similar devices based on crystalline silicon[1].

4.1 Introduction

Active silicon photonic devices, which dynamically control the flow of light, have received significant attention for their use in on-chip optical links and networks. High-speed active silicon photonic modulators and switches rely on the plasma dispersion effect [59], where a change in carrier concentration causes a change in refractive index. This refractive index change can be utilized in micrometer-length resonators [91, 60] or millimeter-length Mach-Zehnder interferometers [4], and the necessary change in carrier concentration can be introduced either by optical pumping [92, 93] or by direct electrical injection and depletion [91, 60, 4]. Crystalline silicon has previously been used to demonstrate these all-optical and electro-optic modulators, which normally limits the devices to a single layer.

The fabrication of active modulators and switches in deposited polysili-

[1]Portions of this chapter are reproduced with permission from [38].

con would enable the vertical integration of photonic links and networks with CMOS microelectronics. Passive sub-micron cross-section waveguides and ring resonators have been demonstrated in polysilicon films [31, 36], but active polysilicon devices have yet to be demonstrated. In this chapter, we demonstrate a modulator based on deposited polysilicon. The device uses an all-optical scheme to inject free carriers and change the effective index in the structure [59]. We also demonstrate that the carrier lifetime in these polysilicon devices is shorter than in similar crystalline silicon devices.

4.2 Fabrication

Fabrication is very similar to the devices in Section 2.2 but is repeated here for completeness. We fabricate the devices by growing a 2 µm layer of thermal oxide on a silicon wafer and depositing 250 nm of amorphous silicon by low pressure chemical vapor deposition at 550 °C. We then anneal the film at 600 °C and 1100 °C to crystallize it into polysilicon and minimize optical losses [31, 36]. We pattern 450 nm-wide devices by e-beam lithography (JEOL 9300) and chlorine-based etching (PlasmaTherm 770). A fabricated microring resonator is shown in the SEM image in the Fig. 4.1 inset before cladding with oxide by plasma enhanced chemical vapor deposition. A resonance at $\lambda_0 = 1568.28$ nm for the quasi-TM polarized mode in the through-port spectrum of an oxide-clad 40 µm-radius ring resonator is shown in Fig. 4.1. The full width at half-maximum bandwidth is $\Delta\lambda_{FWHM} = 0.140$ nm, corresponding to a loaded quality factor $Q_L = \lambda_0/\Delta\lambda = 11,200$ and a photon lifetime $\tau_{ph} = Q_L\lambda_0/(2\pi c) = 9.3$ ps. The extinction ratio on resonance is more than 18 dB, indicating near-critical coupling.

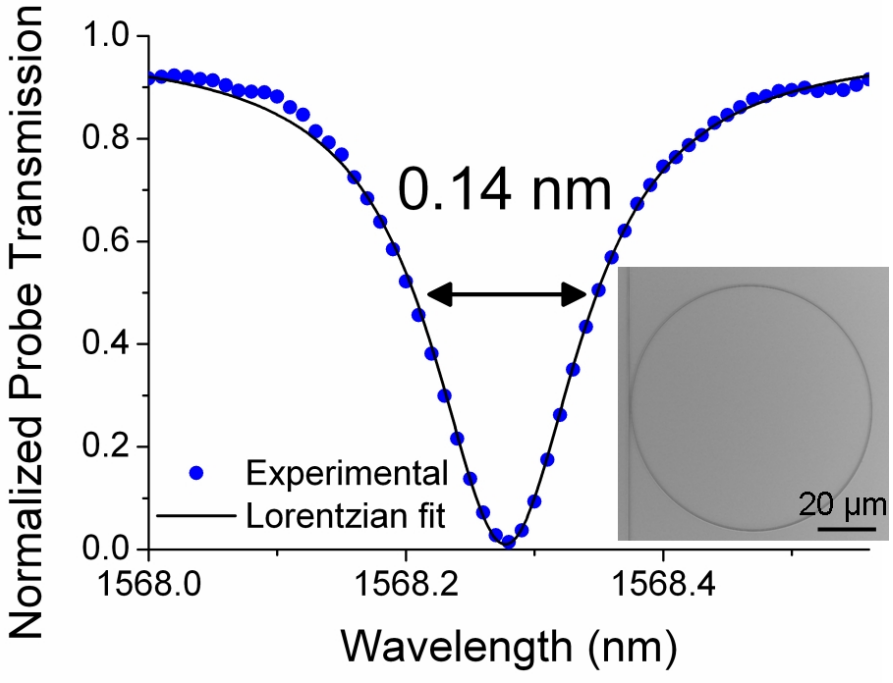


Figure 4.1: Through-port spectrum of a polysilicon ring resonator in quasi-TM mode. Inset: SEM of polysilicon ring resonator and bus waveguide.

4.3 Experiment

We demonstrate all-optical modulation of the device using a pump-probe optical setup, shown in Fig. 4.2. A mode-locked Ti:sapphire laser provides 100 fs pulses of light with an 80 MHz repetition rate at $\lambda = 820$ nm, which we frequency-double to $\lambda_{pump} = 410$ nm with a beta barium borate (BBO) crystal. Pump pulses are focused from above onto the ring resonator, where the light is absorbed to generate free carriers and blue-shift the resonance by the free carrier plasma dispersion effect [59]. A quasi-TM polarized continuous-wave probe beam is coupled on- and off-chip using nanotapers [7]. Time-resolved output from the chip is collected by an objective lens, passed through a polarization filter, collimated into an optical fiber, and sent to a 15 GHz photodetector.

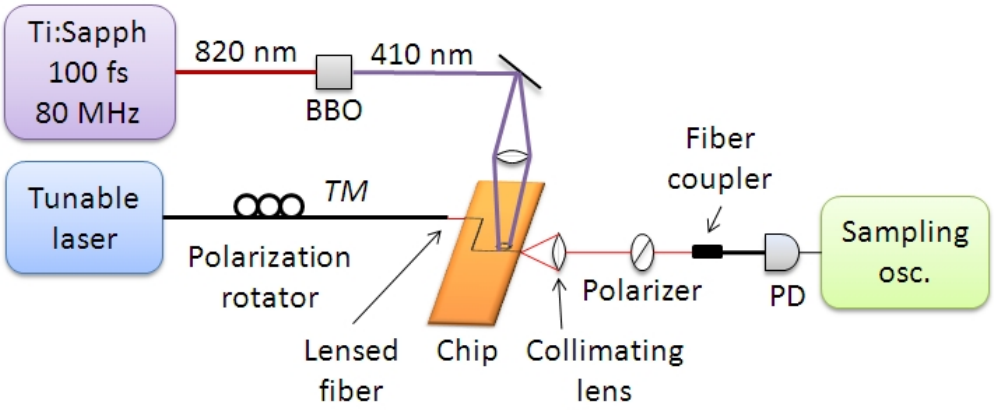


Figure 4.2: Experimental setup for pump-probe measurements of carrier lifetime and all-optical modulation.

Free carrier plasma dispersion acts to reduce the silicon material refractive index and increase the loss as a function of the electron and hole concentrations. This can be described by the Drude-Lorenz equations [59] or by the experimentally measured quantities [94]:

$$\Delta n = -(8.8 \times 10^{-22}\Delta N + 8.5 \times 10^{-18}(\Delta P)^{0.8}) \tag{4.1}$$

$$\Delta \alpha = 8.5 \times 10^{-18}\Delta N + 6 \times 10^{-18}\Delta P \tag{4.2}$$

where Δn is the change in the real part of the refractive index, $\Delta \alpha$ is the change in the loss in cm^{-1}, ΔN is the change in electron concentration in cm^{-3}, and ΔP is the change in hole concentration in cm^{-3}. Note that these equations are valid at $\lambda = 1550$ nm and only for the carrier concentration range between 1×10^{17} and 1×10^{20}. At values down to 1×10^{16}, it was recently shown that the free carrier dispersion effect is stronger than what would be expected by extrapolating from these equations [95].

In a waveguide structure, the optical mode experiences a change in effective index $\Delta n_{eff} = \Gamma \Delta n$ where Γ is the modal confinement factor of Eq. 3.1. If the waveguide is in a resonator structure, then the resonant wavelength is shifted

by an amount $\Delta\lambda = \lambda_0 \Delta n_{eff}/n_g$ where n_g is the group index.

A typical measured response from the pump-probe experiment is shown in Fig. 4.3 for $\lambda_{probe} = 1568.12\,\text{nm}$ and a pump pulse arriving at time $t = 0$. The measurable extinction ratio is limited by the relatively slow response of the detector in approximately the first 150 ps. The 10 dB extinction shown in Fig. 4.3 corresponds to a wavelength shift $\Delta\lambda = 0.14\,\text{nm}$, or an effective index shift $\Delta n_{eff} = 1.76 \times 10^{-4}$. This is equivalent to a change in the refractive index of silicon $\Delta n_{Si} = 2.06 \times 10^{-4}$ which is caused by a maximum carrier concentration $\Delta N = \Delta P = 4.19 \times 10^{16}\,\text{cm}^{-3}$ generated from the absorbed pump light. Given the resonator volume $V = wh2\pi r = 2.827 \times 10^{-11}\,\text{cm}^3$, this corresponds to 1.18×10^6 electrons and holes in the device. Then given the energy per absorbed photon $E = \hbar\omega = 4.84 \times 10^{-19}\,\text{J/photon}$ and 1.18×10^6 absorbed photons, we estimate that a switching energy of 573 fJ is required for this device to reach a 10 dB modulation depth. The recovery time required from the onset of the pump pulse to return to -1 dB is 250 ps, which is approximately a factor of 3 faster than the recovery time in a similar single-crystalline silicon device [92, 93].

4.4 Measurement of Free-Carrier Lifetime

An advantage of the polycrystalline material, in addition to serving as a platform for monolithic 3D integration, is its lower carrier lifetime when compared to crystalline silicon. This is a critical property in the design of high speed modulators. A measured exponential decay of the number of free carriers in a device provides an effective carrier lifetime, described as the parallel combination of all

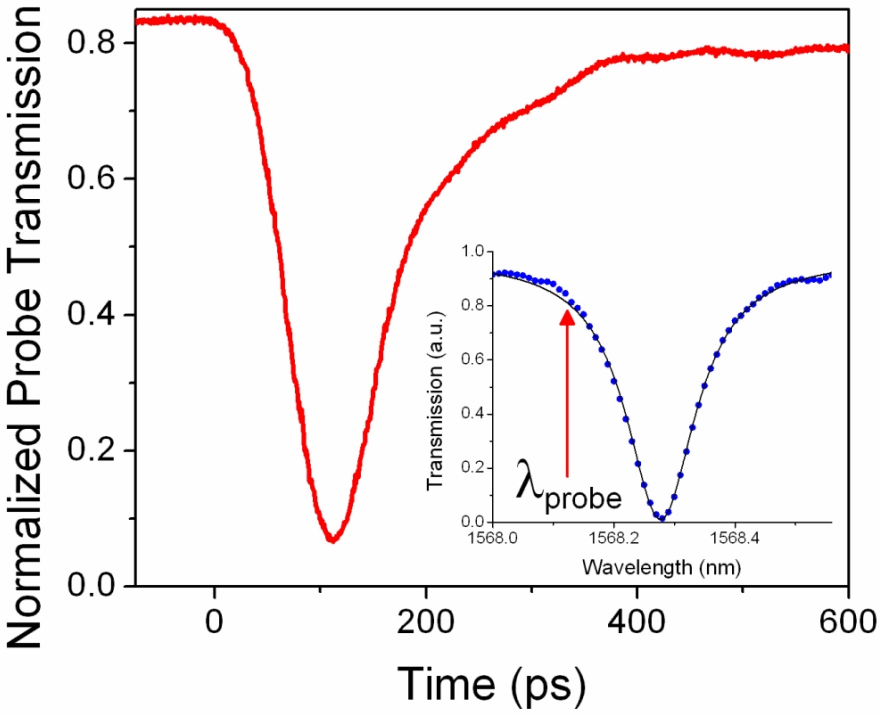


Figure 4.3: All-optical modulation in a polysilicon ring resonator with a 10 dB modulation depth. Inset: Location of the probe wavelength relative to the microring resonant wavelength.

the available relaxation pathways:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surf}} + \frac{1}{\tau_{diff}} + \ldots \tag{4.3}$$

where τ_{bulk} is the bulk recombination lifetime for silicon, τ_{surf} is the lifetime for fast recombination at the surfaces of the silicon structure, and τ_{diff} is the lifetime for carriers to diffuse away from the optical mode. Bulk recombination τ_{bulk} in silicon is on the order of 1 µs or more [96] and can be ignored when faster mechanisms are present. Sub-micron 450 nm wide by 250 nm tall channel waveguides in single crystalline silicon have $\tau_{eff} \approx \tau_{surf} \approx 450$ ps [92, 93]. One approach for lifetime reduction is to physically alter the silicon by ion implantation, which creates defects throughout the material. These defects act both as traps and recombination centers for free carriers (decreasing τ_{eff}) [97] and as scattering points for light (increasing optical losses and lowering resonator

quality factors). This technique has recently been demonstrated using Ar+ implantation in a photonic crystal cavity [98] and O+ implantation in a crystalline silicon ring resonator [99].

The use of polysilicon decreases the effective carrier lifetime due to an effect similar to carrier annihilation by ion implantation. Polycrystalline silicon consists of regions of crystalline silicon separated by nanometer-thin grain boundaries. This is shown in the transmission electron microscope (TEM) image in Fig. 2.2 of a polysilicon film before lithography. The disordered boundaries consist mostly of amorphous silicon and typically contain a trap density around mid-10^{-12} cm^{-2} of grain boundary area [25]. Grain boundaries and defects within the crystalline grains act as both traps and recombination centers for free carriers [100]. Given a grain size of approximately 300 nm [31, 36] and the empirical relation $\tau_{eff,poly} = 5 \times 10^{-6} d$ with d the grain size in cm [100], we would expect a carrier lifetime on the order of 150 ps.

We directly measure the carrier lifetime in our devices by decoupling the carrier response from the resonator's Lorentzian lineshape. To do this, we tune the probe wavelength to the near-linear portion of the resonance ($\lambda_{probe} \approx 1568.3$ nm) and use small pump energies to perturb the resonance while keeping the probe within the linear regime. The decay tail in Fig. 4.4 is then linearly related to the recombination of free carriers and the experimental lifetime can be extracted by fitting a simple exponential. Averaged across multiple measurements, we find an effective carrier lifetime $\tau_{eff} = 135 \pm 5$ ps, which is a 3.3 times reduction as compared to crystalline silicon [92, 93]. To further quantify the lifetime reduction, we use the form of Eq. 4.3 with only $\tau_{surf} = 450$ ps from the crystalline silicon experiment and an additional relaxation pathway τ_{gb} due to grain

boundaries and additional defects within the grains. Using this first-order approximation we calculate $\tau_{gb} = (\tau_{eff}^{-1} - \tau_{surf}^{-1})^{-1} = (135^{-1} - 450^{-1})^{-1} = 200\,\text{ps}$. This shows that the additional recombination we have introduced is approximately twice as fast as the preexisting surface recombination.

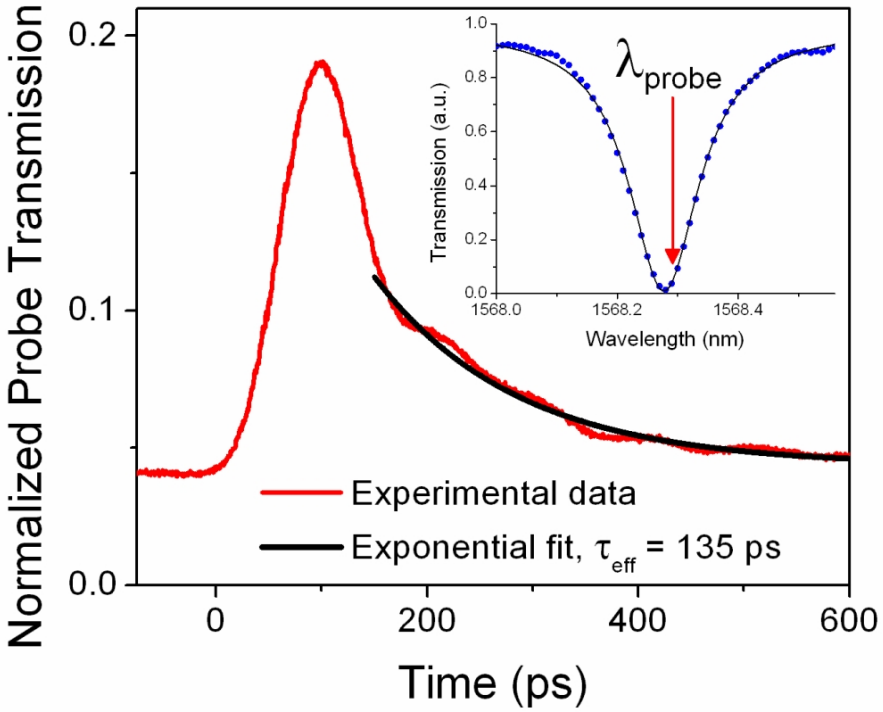


Figure 4.4: Measurement of effective carrier lifetime using a pump pulse with small energy. Inset: Location of the probe wavelength relative to the microring resonant wavelength.

4.5 Discussion

Decreased carrier lifetime in polysilicon comes at the expense of increased optical losses; however, we show here that these losses still enable sufficiently high-Q resonators to be used as high-speed, low-switching energy modulators. The trade-off between speed and optical loss exists because the same grain boundaries and defects that lower the lifetime also cause optical loss by Rayleigh scat-

tering (due to inhomogeneity) and absorption (due to dangling bonds). The increased losses are a challenge for resonator-based all-optical and electro-optic modulators because they increase the energy per bit required to achieve a given modulation depth. Higher losses lead to lower Q-factors and broader resonances, meaning that more energy must be put into the resonator to shift by a larger $\Delta\lambda$ and maintain the same modulation depth. While Q-values are highly dependent on fabrication conditions, the polysilicon resonator shown here has a Q-value 2 to 3 times lower than crystalline silicon resonators fabricated using the same lithography and etching steps [60]. In addition to the achievable resonator quality factor, the loss value is important for bus waveguides that guide light to and from the modulator. In Section 2.3 we demonstrated polysilicon waveguide losses on the order of 20 dB/cm, which is too high for centimeter-length bus waveguides in a practical on-chip link or network. However, an advantage of working with deposited materials is that active polysilicon devices could be combined with low-loss waveguides of a different material [36] such as silicon nitride or amorphous silicon.

In conclusion, we have demonstrated an all-optical modulator in polysilicon with a high extinction ratio and low power consumption comparable to crystalline silicon but with a shorter free carrier lifetime. While the carriers here were injected using an all-optical scheme, electro-optic modulation could be achieved by embedding a PIN junction around the ring resonator [91, 60] in the polysilicon material [25]. Polysilicon as a platform for active photonic devices could enable the monolithic 3D integration of photonics on a CMOS compatible chip.

CHAPTER 5

ELECTRO-OPTIC MODULATORS

In the previous chapter we demonstrated all-optical modulators using polysilicon microring resonators, where the control was made using a second pump beam. In this chapter we show the demonstration of an electro-optic modulator where control is done using an integrated electrical diode[1].

We demonstrate a micrometer-scale electro-optic modulator operating at 2.5 Gbps and 10 dB extinction ratio that is fabricated entirely from deposited silicon. The polycrystalline silicon material exhibits properties that simultaneously enable high quality factor optical resonators and sub-nanosecond electrical carrier injection. We use an embedded $p^+ - n^- - n^+$ diode to achieve optical modulation using the free carrier plasma dispersion effect. Active optical devices in a deposited microelectronic material can break the dependence on the traditional single layer silicon-on-insulator platform and help lead to monolithic large-scale integration of photonic links and networks on a microprocessor chip.

5.1 Introduction and Background

Photonic links and networks on a silicon microelectronic chip offer the opportunity to overcome the power and bandwidth limitations in traditional microprocessor interconnects [42, 101]. One critical device for on-chip optical networks is a silicon high-speed waveguide-integrated electro-optic modulator, which converts data from the electrical domain to the optical domain. All previous examples of these modulators (including interferometer [4, 45, 6, 102, 103]

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and microresonator [5, 104, 9, 105] geometries) have been fabricated on single-crystalline silicon-on-insulator (SOI) [3]. Reliance on the SOI platform presents two difficult challenges for the integration of optics with microprocessor chips. First, the large-scale integration of hundreds of optical devices would take a prohibitive amount of real estate away from transistors in the same silicon layer, and second, the buried oxide thickness in standard microelectronic SOI is much smaller than the optical wavelength and therefore not appropriate for a waveguide cladding [106, 16]. Here we show the first demonstration of GHz-speed electro-optic modulation in a deposited microelectronic film. The use of deposited material, here polycrystalline silicon (polysilicon), would enable the monolithic integration of optics in a separate layer of a microprocessor chip and provide the flexibility needed for optical system design.

The requirements for both chip real estate and device compatibility indicate that photonic devices and electronic devices should be on separate layers of a microprocessor chip [107]. One option for multilayer integration is to fabricate separate electronic and photonic SOI wafers followed by wafer thinning, bonding, and metallization to connect the layers, however the required processes are not yet cost effective and are therefore not in current production [108]. A simpler, monolithic approach would be to deposit silicon-based layers above the transistor layer and process them into optical devices [109]. Previous active switching or modulating devices in deposited microelectronic films such as silicon nitride or amorphous silicon have relied on the thermo-optic effect [110] which is limited to low speeds in the MHz regime [8]. Liu et al. recently demonstrated a GHz-speed, epitaxially grown GeSi electro-absorption modulator integrated with CMOS circuits [111], however epitaxial growth typically requires a crystalline seed which limits where the material can be grown.

A silicon microring modulator uses free carrier dispersion [59] to slightly shift the resonant wavelength of the device. Electrons and holes decrease the refractive index of silicon which results in a blue-shift of the resonance. A continuous wave input with a fixed wavelength can then be switched between a low transmission state and a high transmission state due to the highly nonlinear transmission function. In the previous chapter, we used an optical pump to introduce the electrons and holes. Here we will use an electrical diode to inject and extract the free carriers. A key concern is whether the polycrystalline material has appropriate electrical properties for efficient injection and extraction.

5.2 Polysilicon Electro-optic Properties

In this work we show integrated electro-optic devices in deposited polysilicon, a standard microelectronic material containing crystalline grains separated by thin amorphous grain boundaries [25]. Previous optical devices in the polysilicon-on-insulator material system included passive waveguides with loss on the order of 10 dB/cm [31, 112, 33], optical filters [106, 36], and a recent demonstration of all-optical modulation [38]. Here we demonstrate electro-optic functionality by embedding a $p^+-n^--n^+$ diode [113, 114] around a polysilicon ring resonator. In order to achieve good optical and electrical properties, we use photonic structures with cross sectional dimensions of hundreds of nanometers, on the order of the material grain size [38]. This enables sub-nanosecond carrier injection and optical modulation using the free carrier dispersion effect [59].

The polysilicon material system differs from single-crystalline silicon in

three critical ways that affect electro-optic modulator design and performance: effective carrier mobility μ_{eff}, effective free carrier lifetime τ_{fc}, and optical loss α. All three parameters are affected by the grain boundaries that exist throughout the material. For instance, grain boundaries in polysilicon present a potential barrier to the flow of carriers which results in decreased effective carrier mobility μ_{eff} [25, 115]. Mobility in various phases of silicon ranges from the order of $1000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$(single crystalline silicon) to less than $1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ (amorphous silicon).

Background doping of the device region is required to ensure sufficient charge injection because intrinsic undoped polysilicon is extremely resistive (corresponding to low mobility μ) [25]. An increase in doping above the grain boundary trap density improves the electrical injection [25, 114], but this is a trade-off with increased optical loss due to free carrier absorption [59]. In doped polysilicon, some percent of dopant atoms segregate to low energy positions at the grain boundaries where they do not contribute carriers. Additionally, the carriers themselves can fill in grain boundary trap states [25] where they will not contribute to free carrier dispersion. To keep the background free carrier losses low, we conservatively choose an average *n*-type doping level $N_d \approx 2 \times 10^{17}\,\mathrm{cm^{-3}}$. We estimate that this produces a free carrier concentration $n \leq 1 \times 10^{17}\,\mathrm{cm^{-3}}$ which keeps excess free carrier loss below 4 dB/cm [59].

Grain boundaries and other intragrain defects in polysilicon induce a fast carrier recombination lifetime, which allows a polysilicon modulator to reach a steady state carrier concentration faster than a comparable crystalline silicon device. This lifetime was measured in previous work to be on the order of $\tau_{fc} \approx 100\,\mathrm{ps}$ for a grain size of approximately 300 nm in a 450 nm by 250 nm

channel waveguide [38]. In addition to decreased τ_{fc} and μ_{eff}, optical losses are moderately increased in polysilicon due to scattering and absorption of light at the grain boundaries [31], though resonator quality factors of 20,000 are achievable [36] which is more than sufficient for a modulator device [104].

5.3 Fabrication

Fabrication of the devices is performed using standard microelectronic processes. We start with a silicon wafer and grow a 3 µm thermal oxide isolation layer. We then deposit a 270 nm layer of amorphous silicon by low pressure chemical vapor deposition (LPCVD) at 550 °C and crystallize the film into polysilicon by a thermal anneal at a maximum temperature of 1100 °C. Background doping of the resonator area is done by opening windows in positive e-beam resist and performing Phosphorus ion implantation with a dose of $4.7 \times 10^{12}\,\mathrm{cm}^{-2}$ and energy of 130 keV. We pattern waveguides and resonators using e-beam lithography (JEOL 9300) and XR-1541 resist, and transfer the pattern using chlorine-based inductively coupled plasma reactive ion etching (PlasmaTherm 770), leaving a 40 nm slab of silicon for electrical access. We dope p^+ and n^+ contact regions in the slab by BF_2 and Phosphorus ion implantation at $1.2 \times 10^{15}\,\mathrm{cm}^{-2}$ dose and clad the structures in 1 µm silicon dioxide by plasma enhanced chemical vapor deposition (PECVD). We then anneal the sample in N_2 for 30 minutes at 600 °C, 15 minutes at 900 °C, and 15 seconds at 1050 °C for silicon regrowth and dopant activation. (By ending with the high temperature rapid thermal anneal, we maximize the number of dopant ions that are electrically active [25].) Finally we open vias to the contact regions in order to form nickel silicide contacts and aluminum pads using e-beam evaporation and

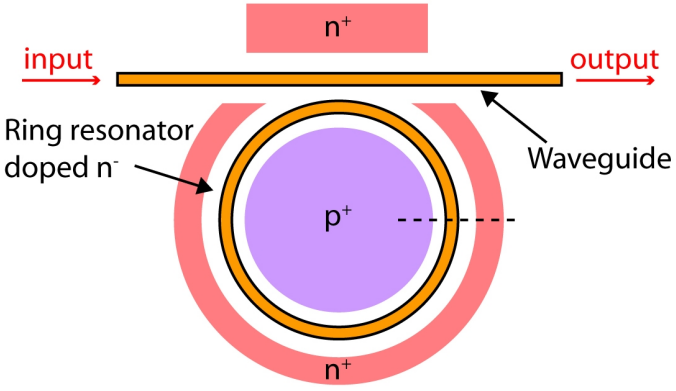
liftoff steps. The device consists of a 10 µm radius polysilicon ring resonator embedded in a 40 nm tall $p^+ - n^- - n^+$ diode and laterally coupled to a polysilicon waveguide. A cross-sectional schematic, top view schematic, and top view microscope image are shown in Fig. 5.1.

5.4 Experiment

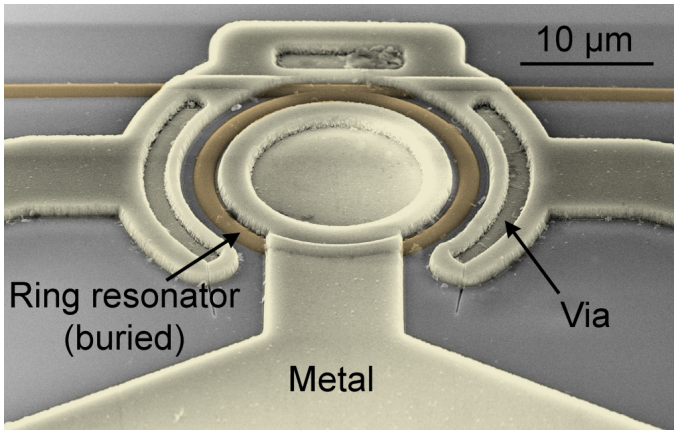
We first analyze the electro-optic device with DC measurements. The experimental setup is shown in Fig. 5.2 and is described as follows. Optical measurements are performed using a tunable infrared laser coupled through a polarization controller to a tapered lens fiber. Light is coupled on and off chip via nanotaper mode converters [7]. Output from the chip is collected by an objective lens, passed through a polarization filter, and focused on a photodetector.

Figure 5.3a shows a measured resonance at $\lambda_0 = 1550.35$ nm with spectral 3 dB linewidth $\Delta\lambda_{FWHM} = 0.45$ nm, loaded quality factor $Q_L = \lambda_0/\Delta\lambda_{FWHM} = 3400$ and 16 dB extinction ratio. Other devices from this fabrication run exhibited quality factors exceeding 10,000. We perform a DC electrical measurement on the device to obtain a diode IV curve shown in Fig. 5.3b. The device exhibits an on-resistance of approximately 3.5 kΩ, which includes contact resistance at the p^+ and n^+ regions and series resistance through the lightly doped waveguide and slab regions.

We demonstrate 2.5 Gbps modulation and measure a 10 dB modulation depth with a non-return-to-zero (NRZ) $2^7 - 1$ pseudo random bit sequence (PRBS) electrical signal applied with a ±4 V swing and a 4 V DC bias. For AC measurements, output light from the chip is collimated, coupled to a fiber,



(a)



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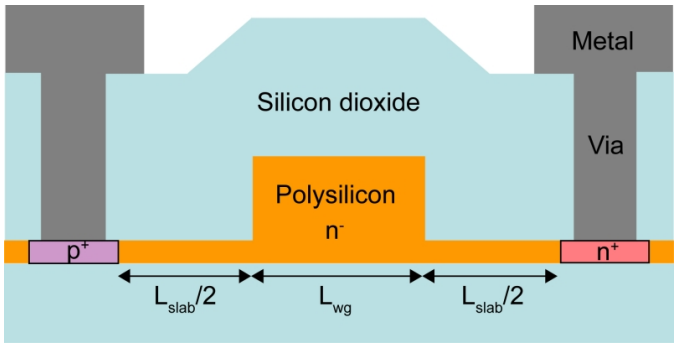


(c)

Figure 5.1: Polysilicon electro-optic modulator device structure. (a) Top view schematic showing the doping regions of the device that form a $p^+ - n^- - n^+$ diode around a ring resonator. (b) Tilted view colorized scanning electron microscope (SEM) image. The polysilicon resonator and 450 nm-wide bus waveguide are buried under 1 µm silicon dioxide. (c) Cross-section schematic of the device (not to scale).

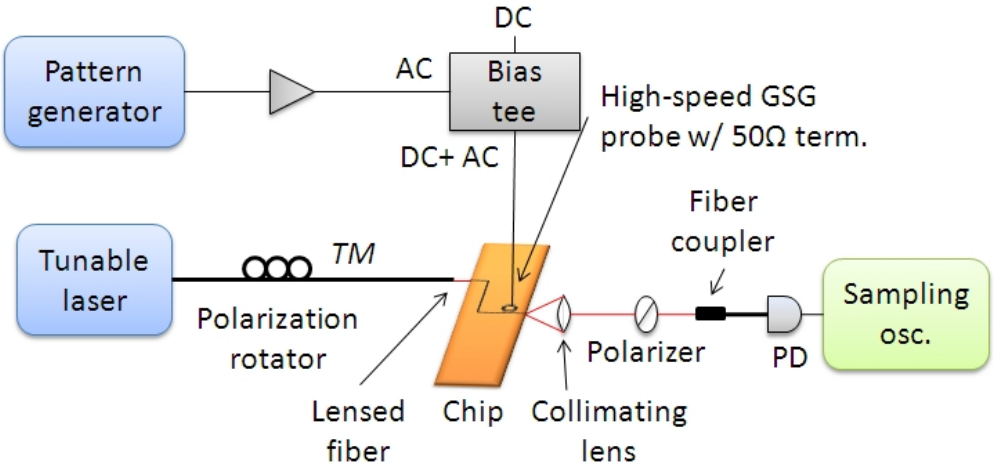


Figure 5.2: Experimental setup for measuring waveguide integrated electro-optic modulator. For DC measurements, the high-speed probe is replaced by an unterminated DC probe.

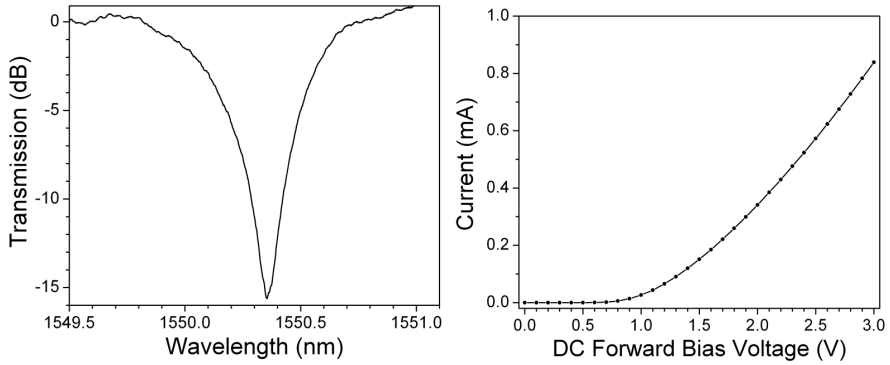


Figure 5.3: DC optical and electrical measurements. (a) Wavelength scan showing through port transmission for quasi-TM polarization with quality factor $Q = \lambda_0/\Delta\lambda_{FWHM}$ = 3,400 and 16 dB extinction ratio. (b) Electrical IV curve demonstrating DC diode characteristics.

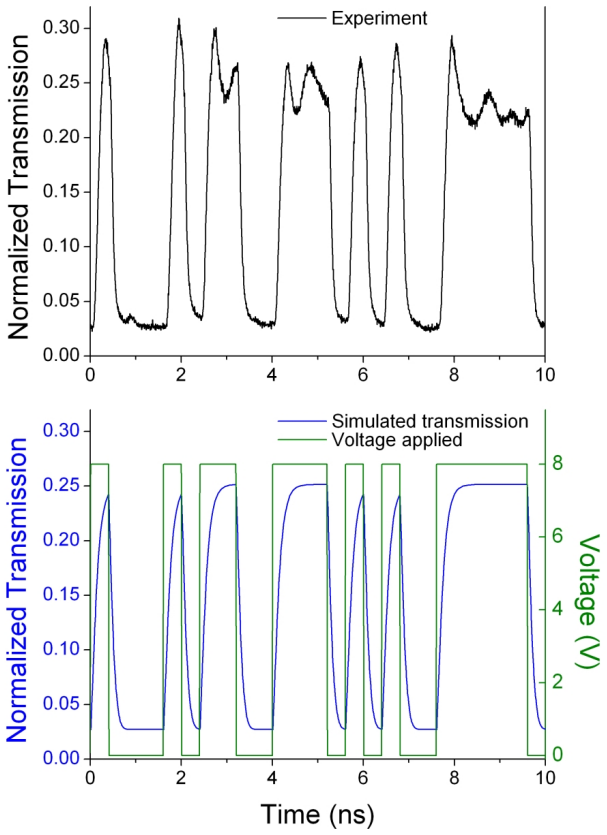
passed through a fiber pre-amplifier and tunable filter, and recorded by an oscilloscope with a 20 GHz photodetector. The oscilloscope is triggered to the pattern generator which provides the NRZ electrical signal to a high-speed amplifier and bias tee circuit. By forward biasing the diode and injecting free carriers into the ring, the resonant wavelength blue shifts and changes the probe wave-

length transmission from low to high. Figure 5.4a and 5.4b show the optical transmission and frame-averaged optical eye diagram when the wavelength is tuned to minimize the off-state transmission. The slight overshoot and oscillation of the high transmission of the waveform in Fig. 5.4 is caused by electrical impedance mismatch, coupled with the fact that the voltage swing here is not sufficient to reach full optical transmission. Comparing the measured 10 dB extinction ratio in Fig. 5.4a to the 16 dB extinction on resonance in Fig. 5.3a, we estimate a 6 dB insertion loss and a maximum wavelength shift $\Delta\lambda \approx 130\,\text{pm}$. This $\Delta\lambda$ corresponds to an effective index shift $\Delta n_{eff} = n_g \Delta\lambda/\lambda_0 = 3.66 \times 10^{-4}$ given a group index $n_g = 4.36$ found with a finite difference modesolver program. Based on modesolver simulation, this Δn_{eff} is caused by a silicon refractive index change $\Delta n = 3.7 \times 10^{-4}$, which is caused by a carrier injection level $\Delta N = \Delta P = 8.4 \times 10^{16}\,\text{cm}^{-3}$ [59]. We estimate energy consumption of 950 fJ/bit and power consumption of 2.4 mW based on the voltage swing, bit rate, carrier lifetime, device size, and charge injection levels.

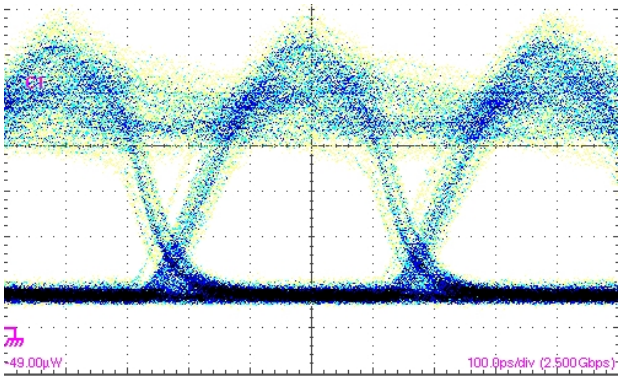
The carrier mobility μ can be estimated from the measured DC on-resistance using the formula [114]:

$$R_{on} = \frac{1}{q\mu n w}\left(\frac{L_{slab}}{h_{slab}} + \frac{L_{wg}}{h_{wg}}\right) \tag{5.1}$$

where q is the electron charge, n is the free carrier concentration ($\approx 1 \times 10^{17}\,\text{cm}^{-3}$), w is the circumference of the ring (62.8 µm), L_{slab} is the total cross-section length of the slab region between the n^+ and p^+ regions (1.55 µm), L_{wg} is the width of the waveguide (0.45 µm), h_{slab} is the height of the polysilicon slab (40 nm), and h_{wg} is the waveguide height (270 nm). By attributing the full 3.5 kΩ to material resistance, we calculate a first-order lower bound for the carrier mobility $\mu = 100\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$. This is only one order of magnitude lower than values in crystalline silicon [25], which explains why the electrical performance



(a)



(b)

Figure 5.4: Electro-optic response of the polysilicon modulator. (a) Experimental (top) and simulated (bottom) optical transmission and and (b) experimental frame-averaged optical eye diagram for NRZ 2.5 Gbps $2^7 - 1$ PRBS signal. Simulation of electro-optic response is performed using bulk distributed material parameters $\tau_{fc} = 80\,\text{ps}$, $\mu_n = 100\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$, and $\mu_p = 50\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$.

can approach that seen in crystalline SOI devices.

We model the operation of the device using SILVACO Atlas[2] simulation software and show excellent agreement with experimental results. As a first order model of the effect of grain boundaries on the polysilicon electrical properties, we define silicon bulk material properties within our device, including a free carrier lifetime $\tau_{fc} = 80\,\text{ps}$ and an effective carrier mobility $\mu_n = 100\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ for electrons and $\mu_p = 50\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ for holes. We use Shockley-Read-Hall (SRH) and Klaassen models for carrier recombination and mobility, and the surface recombination velocity is taken to be 16,000 cm/s which is consistent with SOI modeling [116]. We apply the same voltage signal as was used in the experiment in Fig. 5.4 (without ringing) and solve for the transient charge concentrations $\Delta N(t)$ and $\Delta P(t)$ in the waveguide region. These values are then converted to a wavelength shift $\Delta\lambda(t)$ and excess loss $\Delta\alpha(t)$ (from Eq. 4.1 and 4.2) which are put into a steady-state Lorentzian resonance model to find the optical response. Note that a time domain optical model is not required because the cavity photon lifetime $\tau_p = Q_L\lambda/(2\pi c) = 2.7\,\text{ps}$ is much less than the charge injection time. The result for optical transmission is shown in the bottom of Fig. 5.4a, which demonstrates excellent agreement in rise time, fall time, and extinction ratio with the experimental results at the top of the figure.

5.5 Discussion

The polysilicon device shown here demonstrates speed and energy consumption (2.5 Gbps and 950 fJ/bit) approaching those in state-of-the-art crystalline

[2]SILVACO International, 4701, Patrick Henry Drive, Blg 1, Santa Clara, California.

silicon microresonator devices (≈ 20 Gbps and ≈ 100 fJ/bit [104, 9]). The reduced carrier mobility μ in polysilicon necessitates the use of a slightly higher forward bias voltage for the on-state which increases power consumption, however this is partially compensated by the fast carrier recombination [38] which eliminates the need for a reverse bias voltage for the off-state. The optical transmission in Fig. 5.4 exhibits a 90%-10% fall time of 120 ps with 0 V applied for the off-state. The 10%-to-90% rise time in Fig. 5.4 is 150 ps, indicating a possible bit rate > 5 Gbps. With moderately improved Q and electrical characteristics, we expect the insertion loss could be reduced to near 0 dB and the speed increased to tens of Gbps using pre-emphasis techniques [60].

Electrical properties of the device can be improved by two main approaches: optimizing the background doping concentration and decreasing the device size. The background doping strongly influences the electrical mobility and resistance obtained in the film, which in turn strongly affect the speed and power consumption [25, 115]. Optimal conditions may be found at a higher doping concentration N_d that further improves the mobility without negatively affecting off-state Q. Energy consumption can be greatly reduced to potentially tens of fJ/bit by decreasing the size of the resonator to smaller microring [117] or 1-D cavity geometries [118, 91], since switching energy scales inversely with resonator size [117].

The primary consideration for photonic integration with the CMOS process flow is the temperature required for device fabrication [109]. The highest temperature in our process is the 1100 °C crystallization anneal which is used to maximize the grain size and minimize the optical loss [31]. Because of the relatively high temperature, these devices would need to be fabricated before any

doping or silicidation is performed on the silicon transistor layer. Note however that a high temperature thermal anneal is not fundamentally required for large grain polycrystalline films. Crystallization by nanosecond excimer laser annealing can be used to achieve grain sizes of micrometers without any steady state heating of the substrate. This technique is currently used extensively in the thin film transistor industry to produce polycrystalline films on glass and plastic substrates [119]. With a low-temperature process below 450 °C, active polysilicon devices could be integrated with low loss amorphous silicon or silicon nitride waveguides on top of the CMOS metal interconnect layers. This type of post-backend processing would enable optical functionality on a CMOS chip with minimal changes to the microelectronic process flow.

For the first time to our knowledge, we have demonstrated GHz-speed electro-optic modulation in a deposited microelectronic material. The polycrystalline silicon exhibits optical and electrical properties which enable modulation of the transmission through a microring resonator on a 150 ps timescale. This work represents a step towards adapting high-performance silicon photonic devices for monolithic large-scale integration with standard CMOS microelectronics.

CHAPTER 6

PHOTODETECTORS

6.1 Introduction

In this chapter, we demonstrate photodiodes in deposited polycrystalline silicon at 1550 nm wavelength with 0.15 A/W responsivity, 40 nA dark current, and GHz time response. Sub-band absorption is mediated by defects that are naturally present in the polycrystalline material structure. The material exhibits a moderate absorption coefficient of 6 dB/cm which allows the same microring resonator device to act as both a demultiplexing filter and a photodetector. We discuss the use of deposited silicon-based CMOS materials for nanophotonic interconnects[1].

6.2 Background

The crystalline silicon-on-insulator (SOI) platform enables modulation and low-loss waveguiding in the telecommunication wavelength bands centered at λ = 1.3 µm and 1.55 µm. These functions can be implemented due to the 1.12 eV bandgap of bulk crystalline Si which only produces significant linear absorption for $\lambda < 1.1$ µm, as shown in Fig. 6.1. To add infrared photodetection to silicon photonic circuits, III-V compound semiconductors can be integrated on top of silicon waveguides by bonding techniques [120, 121]. This is not ideal due to the heterogeneous integration and the incompatibility of III-V materials

[1]Portions of this chapter are reproduced with permission from [40].

with silicon CMOS processing. A preferred alternative is to integrate germanium as an absorbing material in CMOS processing environments and several groups [10] have achieved very good photodetector characteristics with high responsivity ~ 1 A/W, low dark current, and high speed ~ 40 GHz. Germanium is already used in CMOS foundries to create strained-silicon and SiGe transistors. However, epitaxial growth of Ge on Si requires complex processing steps to manage the 4% lattice mismatch between the two crystals, as well as a crystalline starting material to act as a template for the Ge crystal.

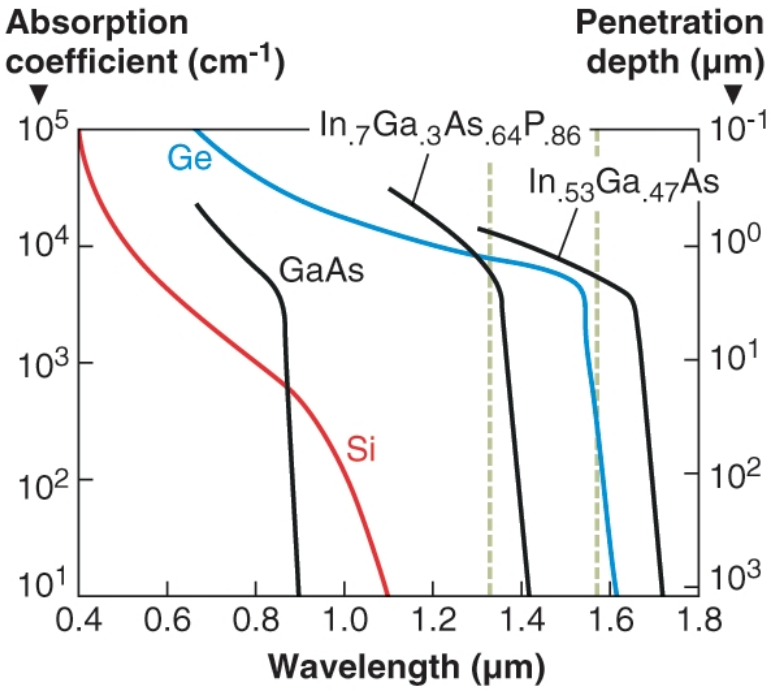


Figure 6.1: Absorption spectra of various semiconductor materials [122]. Silicon traditionally absorbs for wavelengths below 1100 nm, so germanium photodetectors have been integrated on the silicon platform for infrared absorption.

It is known that silicon can generate photocarriers via sub-band absorption of light with $\lambda > 1.1$ μm when defects are present that contribute energy states within the bandgap. This was first shown experimentally by Fan and Ramdas in 1959 [123] and explored theoretically by Wolf in 1960 for photovoltaic appli-

cations [124] in order to generate more photocurrent from the infrared tail of the solar spectrum. However, Shockley and Queisser noted in 1961 [125] that the fast electron-hole recombination introduced by the defect states more than outweighs the extra generation from infrared photons. This has proven to be true and there is no longer much development on the impurity photovoltaic effect, though theoretically it has been shown that solar cell efficiency may be improved by 1-2% [126].

The sub-band absorption of light has been shown in crystalline SOI devices to make infrared photodetectors. The surfaces of an etched waveguide are enough to cause surface state absorption, measured with a relatively low responsivity $R = 0.036$ A/W in thin waveguides [127] or $R = 0.00025$ A/W in microring resonators [128]. Jessop, Knights, et al. showed that the absorption can be further enhanced by distributing defects throughout the waveguide by ion implantation [129, 130, 131]. By engineering the defects and reducing the device size to sub-micron cross-section, Geis, Spector, et al. demonstrated photodetectors with $R \gg 1$ A/W (with avalanche enhancement) and bandwidth > 30 GHz in different device configurations [132, 133, 134]. Recently the device size has been reduced by using a microring resonator for multiple round-trips of light through the same implanted region [135, 136], but all demonstrations to date have required single-crystalline SOI as a starting material.

Here we show infrared photodiodes in polycrystalline silicon (polysilicon), a standard deposited material that can be integrated in the CMOS material stack. The use of deposited silicon-based materials can enable new flexibility in system architecture and chip fabrication [31]. Visible-wavelength photodiodes (650-850 nm wavelength) have previously been demonstrated by sev-

eral groups [137, 138, 139, 140, 141, 142]. We have previously used polysilicon to build integrated optical filters [36] and electro-optic modulators [39] at $\lambda = 1550\,\text{nm}$ for monolithic integration of optical functionality onto a microelectronic chip. The results presented here demonstrate that at least 12% of the propagation loss in these sub-micron polysilicon waveguides is due to sub-band absorption that generates useful photocarriers. Polysilicon can therefore be used for both the modulator and photodetector at the start and end of an optical link on a CMOS chip. Infrared absorption in polysilicon is mainly due to mid-gap states from the dangling Si bonds in the material [25], as shown in Fig. 6.2. For example, if donor electrons are trapped in these states, then absorption of a photon with 0.8 eV energy ($\lambda = 1550$ nm) is sufficient to promote the electron to the conduction band.

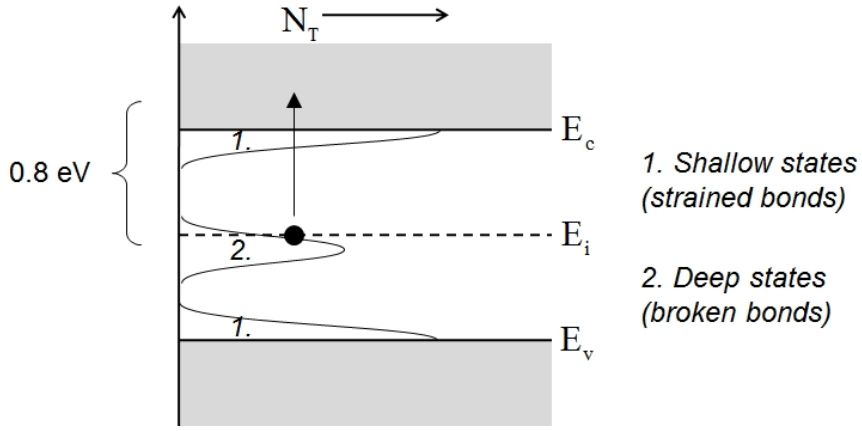


Figure 6.2: Schematic of the energy band gap picture for polycrystalline silicon, following [25]. Bonds can be strained, smearing out the band edge (1), or completely broken, creating a distribution slightly below mid-gap (2).

6.3 Fabrication

We design photodetectors with an integrated PIN diode to sweep out generated carriers and a ring resonator geometry to reduce the footprint. The fabrication is similar to that in Section 5.3 with a summary as follows. We use 3 µm oxide as a lower cladding, deposit 270 nm of high quality amorphous silicon by low pressure chemical vapor deposition (LPCVD), and crystallize the material into polysilicon by a furnace anneal in N_2 at 1100 °C to maximize the grain size (see Fig. 2.2). We perform moderate *n*-type phosphorus doping to an average concentration of $2 \times 10^{17}\,\mathrm{cm}^{-3}$. Many of the dopant ions and donor electrons are trapped at the material grain boundaries [25]. We pattern waveguides and resonators using e-beam lithography (JEOL 9300), etch the devices (PlasmaTherm 770) to leave a 40 nm slab for electrical access, and dope p^+ and n^+ contact regions. We clad the devices in silicon dioxide by plasma enhanced chemical vapor deposition (PECVD) and make electrical contact with nickel silicide and aluminum. The device is shown in Fig. 6.3. The waveguide width is 550 nm and the ring radius is 50 µm to maximize the quality factor Q (minimize the bending and scattering loss) while maintaining a small footprint.

6.4 Experiment

The optical loss through the sample and test setup must be carefully measured to determine accurate values of internal detector responsivity. The experimental setup is shown in Fig. 6.4 and is described as follows. Measurements are performed by coupling light into the waveguide using a tapered lensed fiber and collecting the waveguide output with an objective lens. A polarization

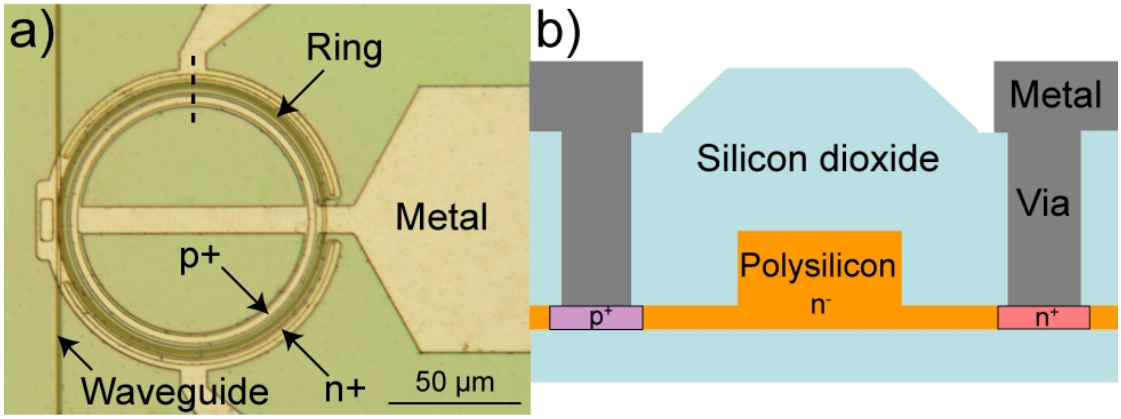


Figure 6.3: (a) Optical microscope image of 50 μm radius polysilicon ring resonator with bus waveguide and metal contacts. (b) Cross-sectional schematic of the electro-optic device region (not to scale). Carriers are generated in the 550 nm wide waveguide region and extracted to the external circuit through the 40 nm slab.

controller is used before the chip to select the TM polarization and a polarization filter is used after the chip. We calculate the waveguide propagation loss to be $\alpha_{wg} = 34.6$ dB/cm by launching light onto the chip from either direction, as follows. Launching from the first facet we find the photocurrent on resonance to be $I_1 = RP_{in1}C_{in}\exp(-\alpha_{wg}L_1)(1 - T_{min})$, and launching from the other facet we find $I_2 = RP_{in2}C_{in}\exp(-\alpha_{wg}L_2)(1 - T_{min})$, where R is the internal responsivity, P_{in1} (P_{in2}) is the power at the fiber tip for facet 1 (facet 2), C_{in} is the fiber to chip coupling efficiency, L_1 (L_2) is the propagation distance from facet 1 (facet 2) to the device, T_{min} is the on-resonance extinction ratio, and $(1 - T_{min})$ is the fraction of power dropped into the ring. The equations reduce to $I_1/I_2 = P_{in1}\exp(-\alpha_{wg}L_1)/P_{in2}\exp(-\alpha_{wg}L_2)$ and we solve for $\alpha_{wg} = 34.6$ dB/cm, which is primarily due to scattering but also includes useful absorption. Then by measuring the total chip insertion loss and subtracting the propagation loss, we find the total chip coupling loss (input facet plus output facet) to be 12.9 dB. We conservatively assume half of this coupling loss to be at the input facet. Ad-

ditionally there is 1.8 dB propagation loss from the input facet to the device, resulting in a total loss of 8.3 dB between the fiber tip and the device for the following measurements.

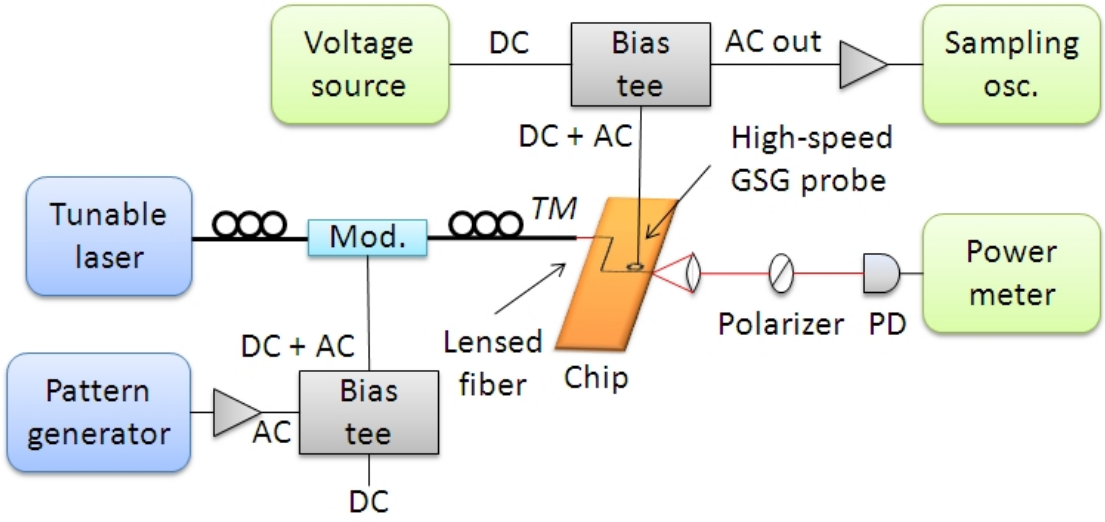


Figure 6.4: Experimental setup for measuring waveguide integrated photodetector. For DC measurements, the modulator and one polarization controller are removed and the high-speed probe is replaced by a DC probe.

We determine the internal responsivity of the photodiode to be as high as 0.15 A/W. Figure 6.5(a) shows the transmission and measured current when we sweep the laser wavelength with a DC reverse bias on the device. When light is on resonance and trapped in the ring, it either scatters away or it is absorbed and generates photocurrent. Figure 6.5(b) shows the resonant photocurrent at -13 V. The optical power in the bus waveguide at the device is P_{wg} = 7.35 μW and the transmission extinction ratio is $(1-T_{min})\times 100\% = 90.5\%$, so $P_{det} = (1-T_{min})\times P_{wg}$ = 6.65 μW is coupled into the resonator. We find a quality factor Q = 10,500 and a maximum photocurrent I = 0.975 μA corresponding to internal responsivity R = 0.15 A/W. The microring device acts as a wavelength-selective photodetector which can both demultiplex and detect one wavelength of a WDM signal. This

combined functionality is not possible in strongly absorbing materials where high loss would prevent the formation of a high-Q resonance.

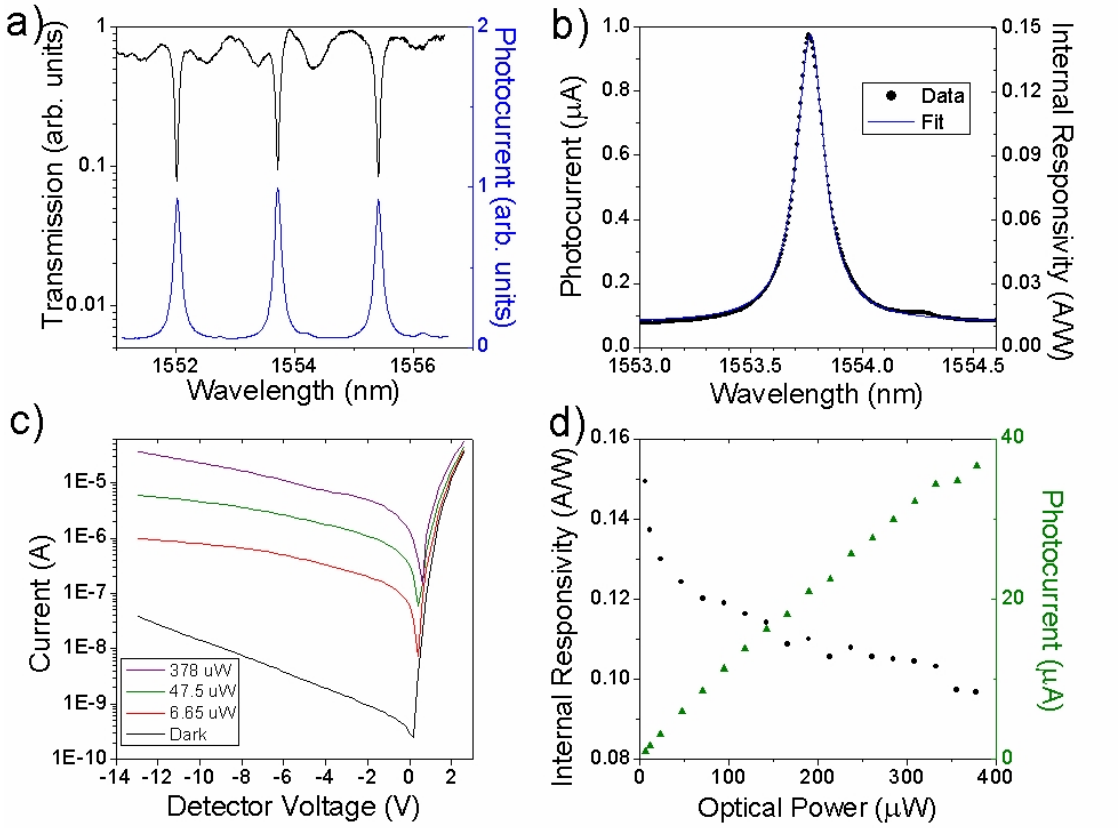


Figure 6.5: (a) Transmission and photocurrent spectra. (b) Close scan of resonance with 6.7 μW optical power coupled into the device at -13 V bias, demonstrating Q = 10,500. Solid line is a Lorentzian fit. (c) Current-voltage characteristics under dark and light conditions, with wavelength set to resonance peak. Legend: optical power coupled into the device. (d) Responsivity (circles) and photocurrent (triangles) at -13 V vs. optical power coupled into the device, with wavelength set to resonance peak.

The responsivity of the photodiode is determined by the efficiency of both carrier generation (given by the ratio of absorption loss to total propagation loss in polysilicon) and carrier extraction. The absorption is due to dangling bonds which produce a distribution of trap states slightly below the mid-bandgap en-

ergy [25, 27], many of which are filled by donor electrons [131]. It is likely that in this device, the photocarrier generation is primarily due to the phosphorus donor electrons being promoted from these trap states to the conduction band.

We measure a low dark current of 40 nA at an operating voltage of -13 V. Figure 6.5 (c) shows IV curves with and without light coupled to the device with the wavelength on resonance. The photocurrent does not plateau but rather continues increasing with reverse bias voltage. This can likely be improved by placing contacts closer to where the carriers are generated, or by tailoring the dopant concentration to ensure full depletion of the waveguide region. Note that we are not operating in an avalanche regime which produces rapidly increasing dark current for voltages less than -14 V. Figure 6.5(d) shows responsivity as a function of the optical power coupled into the device at a bias voltage of -13 V. We find that the internal responsivity decreases from 0.15 A/W to 0.10 A/W as the optical power is increased over nearly two orders of magnitude. This indicates that either the generation or extraction of carriers is suppressed at higher photocarrier densities in the device, and that these effects are larger than any two-photon absorption effect which would increase the responsivity.

We measure the transient response of the photodiode by modulating the c.w. laser with an external modulator. Figure 6.6 (a) shows the direct output of the photodiode operating at a bit rate of 2.5 Gbps. To obtain an eye diagram, we amplify the photodiode output with a low noise amplifier with 1 GHz bandwidth. An open eye diagram at 1 Gbps is shown in Figure 6.6(b). We measure the device S_{11} response using a HP8722ES vector network analyzer and find that the speed of the relatively large device is RC limited. A circuit model and parameter fit is used to de-embed the parasitic contribution of contact pads,

and we find the junction capacitance to be 100 ± 7 fF and series resistance to be 524 ± 25 Ω. From these values, we determine the electrical bandwidth of the device and pads terminated into a 50 Ω load to be 2.6 ± 0.24 GHz, which can be improved by engineering the device structure, reducing the size of the resonator, or integrating directly with a TIA.

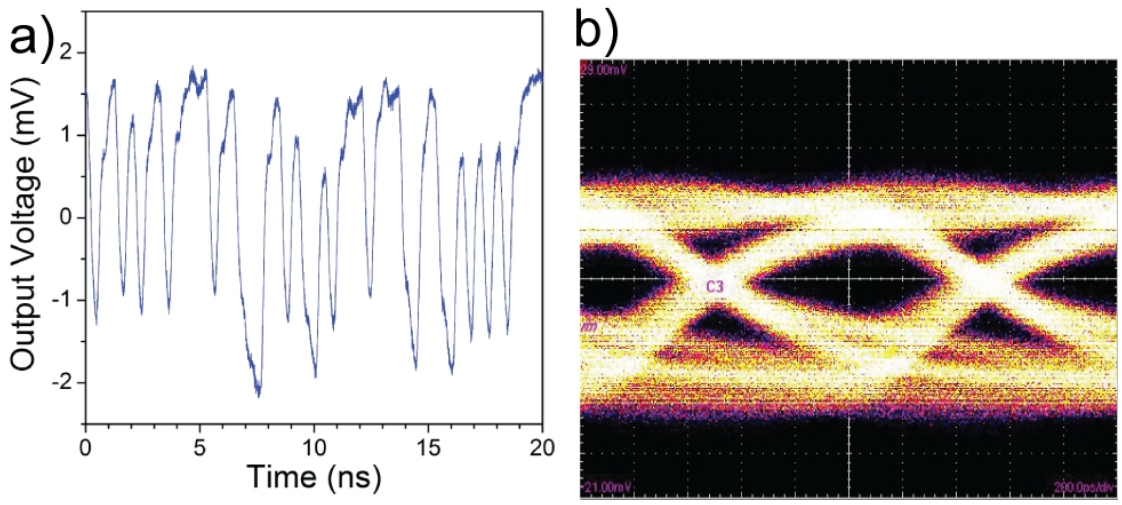


Figure 6.6: (a) Direct AC output of the photodetector on a sampling oscilloscope with a 2.5 Gbps $2^7 - 1$ PRBS input optical signal. (b) Amplified electrical output eye diagram at 1 Gbps. Scale: 200 ps/div, 5 mV/div.

6.5 Discussion

We calculate the absorption coefficient $\alpha_{abs} \geq 6$ dB/cm inside the device. The use of a near critically coupled resonator photodiode is equivalent to a long waveguide photodiode; photons in the cavity which do not scatter away must be absorbed. The internal quantum efficiency is a result of the efficiencies for generation and extraction of the carriers, $QE = \gamma_{gen}\gamma_{extract} = \frac{\alpha_{abs}}{\alpha_{ring}}\gamma_{extract}$. The measured internal quantum efficiency $QE = R\frac{hc}{\lambda}\frac{1}{e} = 12\%$ (for $R = 0.15$ A/W at $\lambda = 1.55$ µm) is therefore a lower bound for $\alpha_{abs}/\alpha_{ring}$, the percent of propa-

gation loss in the ring which is due to absorption. From the Q and extinction ratio, we calculate the total propagation loss in the ring (absorption and scattering) to be α_{ring} = 51.7 dB/cm, and the absorption coefficient is therefore at least 12% of this value, $\alpha_{abs} \geq$ 6.2 dB/cm. We note that the actual absorption value is higher by the percentage of carriers that recombine before being extracted to the external circuit. Additionally, an identical photodiode integrated into a straight waveguide instead of a resonator could have a maximum $QE = \alpha_{abs}/\alpha_{wg}$ = (6.2 dB/cm)/(34.6 dB/cm) = 18%, based on the measured straight waveguide loss. The responsivity can be enhanced by optimizing the background dopant type and concentration.

The polysilicon photodetector presented here can be integrated with CMOS SOI optical components for optical interconnect applications. However, these results also open the door to an integrated optical link which does not require any crystalline SOI material, as discussed in [21], but rather utilizes only silicon-based materials deposited in the CMOS stack. Both the modulator [36] and photodetector can be fabricated from the same polysilicon material. Absorption can be suppressed in the modulator regions by hydrogen passivation [31] and enhanced in the detector by optimizing the dopant type and concentration [143, 131]. Additionally, propagation loss in deposited silicon nitride has been demonstrated as low as 0.1 dB/cm [144], approximately 20 times better than losses in single-mode sub-micron crystalline SOI waveguides. Because of the ultralow optical loss, it may be possible to design optical links or networks whose system-level characteristics outperform the traditional SOI platform [145], even with some degradation in modulator and detector device performance as compared to SOI and crystalline Ge-on-Si.

In conclusion, we have demonstrated an integrated photodiode in polysilicon, a deposited CMOS material. The polysilicon exhibits 6 dB/cm absorption which results in a responsivity of 0.15 A/W. We demonstrated 2.5 Gbps operation of the device and suggest several areas of research for achieving devices with even higher performance.

CHAPTER 7

LOW-TEMPERATURE PROCESSING FOR CMOS INTEGRATION

In this chapter, we show an initial demonstration of integrated optical devices in deposited silicon crystallized at room temperature for 3D photonic integration. These devices can enable electro-optic switching and modulation on low-temperature substrates such as glass, plastic, and post-back-end CMOS wafers. Crystallization of the material is accomplished by excimer laser annealing, where a UV laser pulse heats only the top silicon layer of a material stack over sub-microsecond time scales[1].

7.1 Introduction

Silicon photonic circuits offer the promise of ultra-high bandwidth optical data communication using devices that are monolithically integrated using standard microelectronic fabrication processes [101]. The material system of choice is the silicon-on-insulator (SOI) wafer, which provides a device layer of single-crystalline silicon on top of an undercladding layer of silicon dioxide. Silicon can be used for low-loss waveguides at $\lambda = 1.3$ and 1.55 μm, and free carrier dispersion provides a mechanism for high-speed switching and modulation [104, 9].

In the previous chapters, we used deposited polysilicon as a light guiding material to allow monolithic 3D integration of optical functionality onto a microelectronic chip. We demonstrated that the optical and electrical properties of polysilicon can be sufficient to build optical filters [36] and electro-optic modu-

[1]Portions of this chapter are reproduced with permission from [41].

lators [39]. Ideally such devices would be integrated after the back-end metallization steps of a CMOS process [109, 21] in order to minimize changes to the microelectronic process flow [16]. For the devices in [36, 39], however, we used a high crystallization temperature of 1100 °C in order to maximize the optical and electronic material properties. This is far above the back-end integration limit of 450 °C required to not disturb the metals or doping in the CMOS material stack.

In fact, the thermal budget fundamentally does not allow the formation of polysilicon using steady-state heating. Using chemical vapor deposition, silicon is deposited in its amorphous phase below approximately 580 °C. Above this temperature, there is enough energy in the system for the atoms to rearrange themselves into the preferred crystal lattice, albeit with defects and grain boundaries. In this way the polycrystalline material can either be deposited directly at temperatures above 580 °C, or amorphous material can first be deposited and then crystallized at temperatures above 580 °C as shown in Chapter 2. Instead of steady-state heating, here we will investigate transient heating of amorphous silicon to form polysilicon for integrated optical devices.

7.2 Material Processing

Here we investigate an approach for the crystallization of deposited silicon at low temperatures compatible with back-end CMOS processes. Pulsed laser annealing is used in high-volume manufacturing to produce thin-film polysilicon transistors on glass for the LCD industry [119]. In this method, a near-UV laser pulse is used to locally melt and crystallize a top layer of amorphous silicon [146, 147]. Grain sizes of several microns are achievable in well-optimized

processes [148]. Heating takes place on sub-microsecond time scales and hence the underlying substrate experiences no steady-state heating. Here we use a commercial XeCl excimer laser that generates pulses at $\lambda = 308$ nm with a pulse width ≈ 35 ns. The laser pulse passes through a variable attenuator and is then homogenized in a square glass rod to produce a top-hat spatial profile. This square spot is then focused on the wafer substrate which is mounted on a motorized stage, shown in Fig. 7.1.

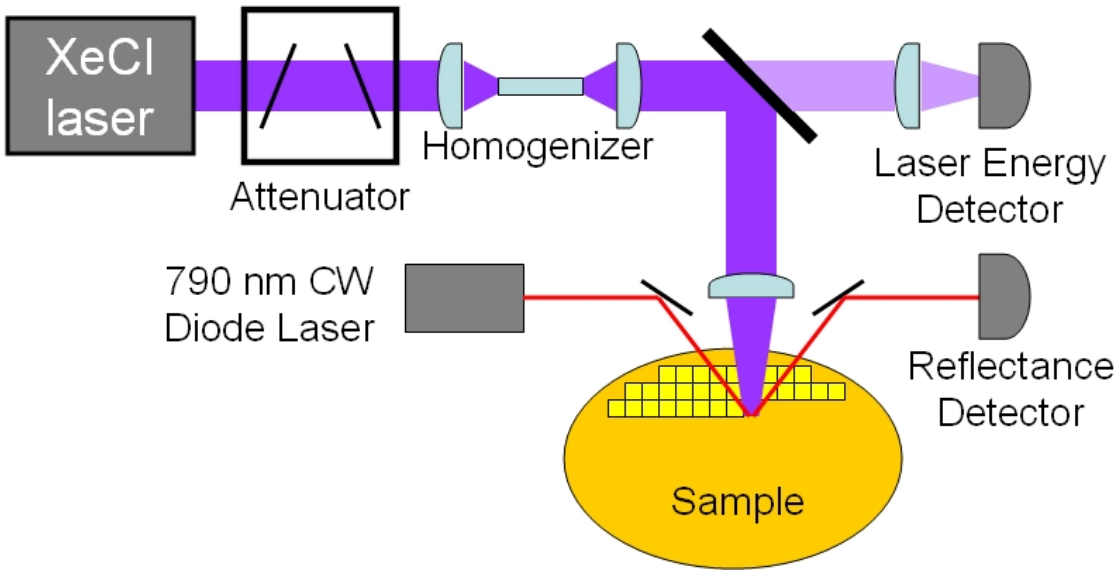


Figure 7.1: Schematic of XeCl excimer laser annealing setup with $\lambda = 308$ nm and pulse width ≈ 35 ns.

Additionally, a red probe laser is focused on the same region of the substrate and its reflection is monitored by a photodetector. In this way the transient material reflectivity, shown in Fig. 7.2, can be monitored in situ to determine melt characteristics since molten silicon is highly reflective. The excimer laser pulse energy is normalized to the melt threshold of a bulk crystalline silicon wafer (which is defined to be at a fluence of 600 mJ/cm^2). The primary method to control the crystallization of polysilicon is to modify the attenuation and hence the pulse fluence (energy density) reaching the substrate.

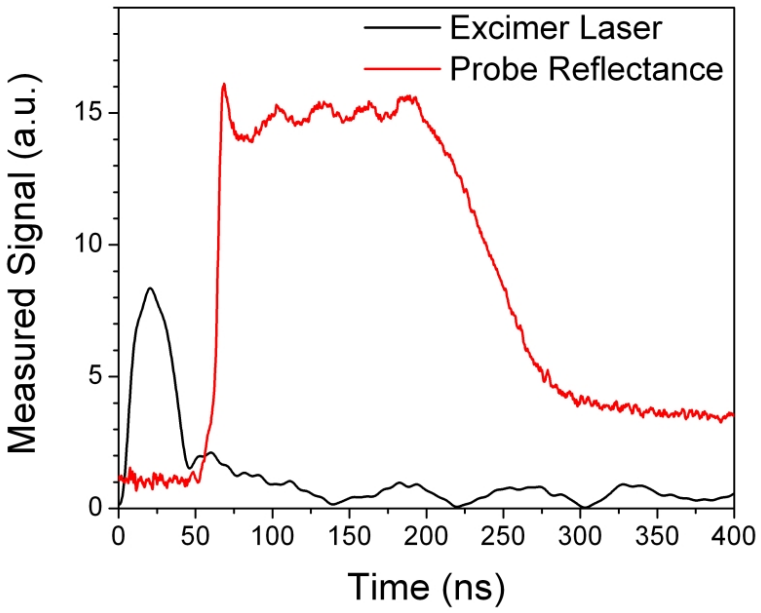


Figure 7.2: Reflectance measurement demonstrating the silicon melt time at 175 mJ/cm^2. Molten silicon is highly reflective, giving an in situ method to monitor the melting process.

The pulse fluence primarily determines the melt depth in the silicon material, which then has a strong effect on the resulting grain size and structure. The absorption depth of 300 nm light in amorphous silicon is about 8 nm, so all of the pulse energy is deposited near the top of the material layer. The silicon then melts down from the top surface to a given depth based on the energy in the pulse. Figure 7.3 shows the different regimes as a function of pulse fluence [147]. Region I is the partial melt regime, where the silicon film melts only partially through its depth. The grain size generally increases as the fluence increases. Note that an amorphous layer can still be present underneath the polycrystalline later. Region II is the near-complete melt regime which provides the largest grains. Here the silicon melts almost completely, leaving only small isolated spots that are unmelted. These act as nucleation sites for grains to grow outwards, with the size only limited by running into another grain. There is a narrow process window for this type of grain growth before Region III, the

complete melt regime with homogeneous nucleation. Grains start to grow from nucleation sites distributed throughout the material, resulting in a small grain size.

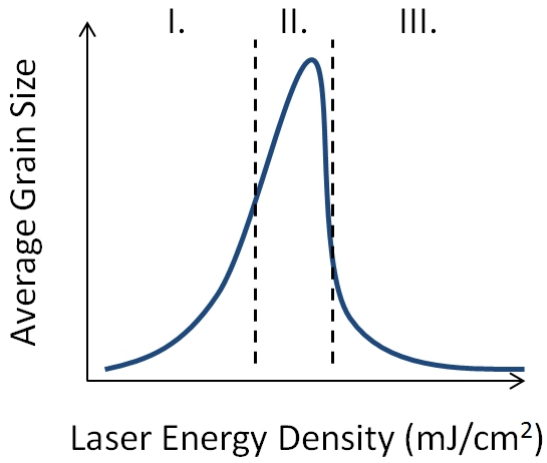


Figure 7.3: Melt regimes for excimer laser annealing. I: Partial melt regime. II. Near-complete melt regime, where only scattered spots of unmelted silicon remain on the bottom surface of the material, acting as nucleation sites for very large grain growth. III Complete melt, where nucleation sites are homogeneously distributed throughout the material, resulting in small grains.

The material processing steps are shown in Fig. 7.4. We begin with a standard 4-inch silicon wafer and grow a layer of thermal silicon dioxide to act as a lower cladding. First we deposit a 160 nm layer of amorphous silicon by electron gun evaporation at room temperature at a pressure of 5×10^{-7} torr. (We have observed that faster deposition rates, up to 100 Å/sec, result in higher quality films that resist ablation at higher ELA fluences.) We then deposit a 150 nm silicon dioxide layer by plasma-enhanced chemical vapor deposition (PECVD). This oxide layer acts as an anti-reflection coating at $\lambda = 308$ nm and reduces silicon surface roughness during the subsequent annealing. Additionally the layer will alter the thermal properties of the material stack. (Note that a 50 nm layer of silicon dioxide would also act as an AR coating, but provides

less mechanical stability to the silicon surface.) The entire wafer is then excimer laser annealed in a manner similar to stepper photolithography: a 3.5 mm × 3.5 mm section is illuminated multiple times for crystallization, the substrate is moved by 3 mm, and the process is repeated. Here we crystallize each region using a sequence of pulses with fluence increasing from 50 to 200 mJ/cm^2. The top oxide layer is then removed in buffered hydrofluoric acid. An atomic force microscope (AFM) measurement of the top surface of the polycrystalline material is shown in Fig. 7.5, with a measured r.m.s roughness of 5 nm. To reduce the surface roughness, we use chemical-mechanical polishing (CMP) to remove about 50 nm of silicon, resulting in a film with thickness ≈ 100 nm and r.m.s roughness < 1 nm. Here we use a hard polishing pad and SS12 slurry, which polishes both silicon and silicon dioxide material to make sure the grain boundaries are polished. Alternate methods could include using a soft pad for more of a fine polishing, or using a slurry that is targeting only at silicon polishing.

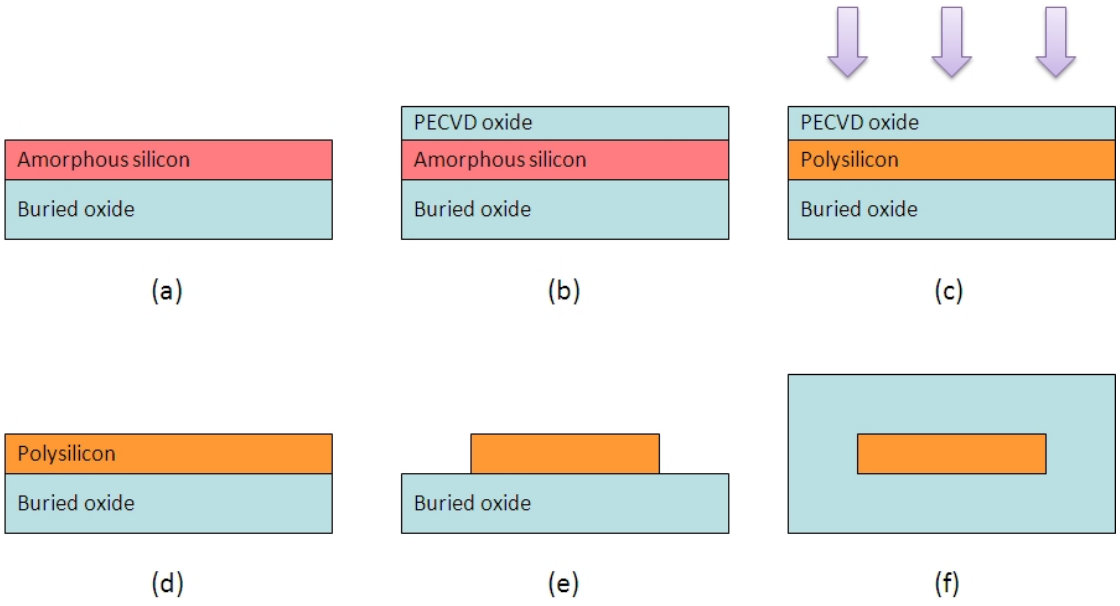


Figure 7.4: Processing steps for excimer laser annealed material.

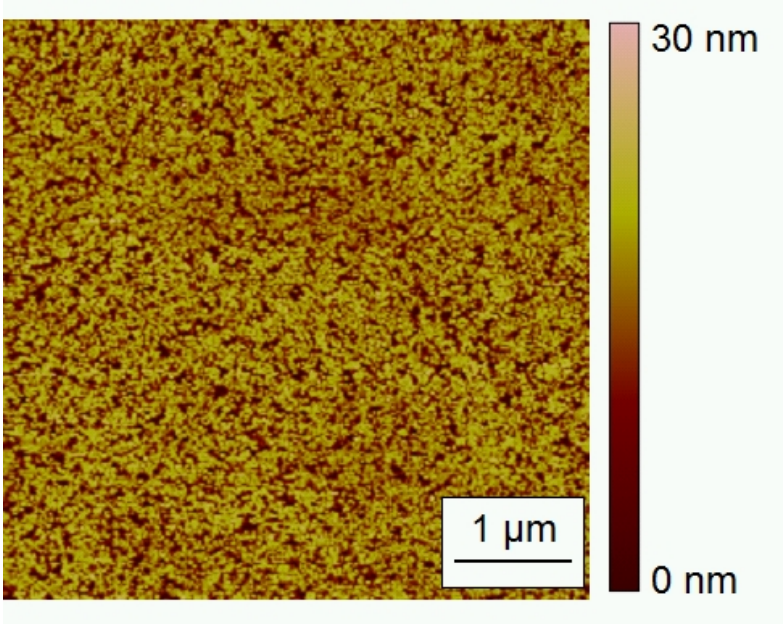
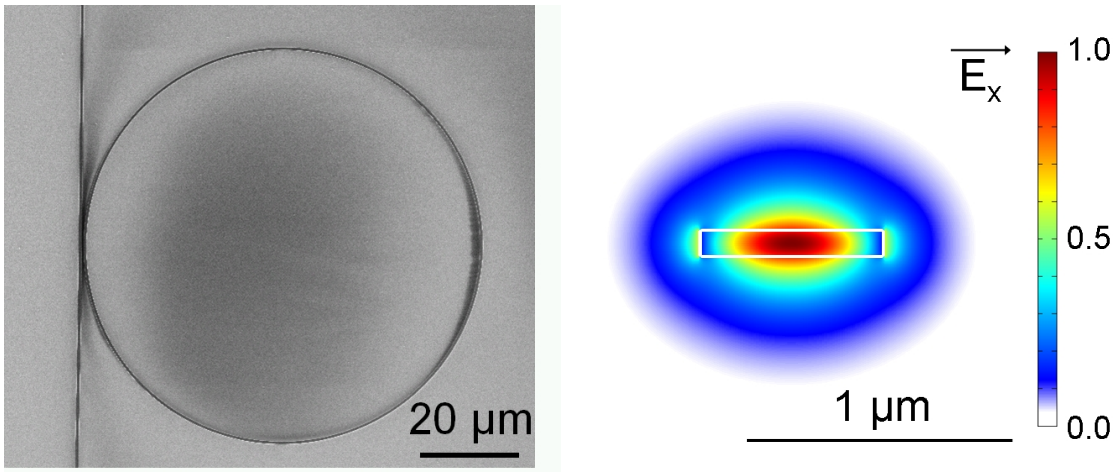


Figure 7.5: AFM image of the polysilicon top surface after crystallization but before CMP. The r.m.s. roughness is 5 nm before CMP and 1 nm after CMP.

7.3 Device Fabrication and Experiment

Optical waveguides and resonators are then patterned in the polysilicon layer using e-beam lithography (JEOL 9300 with XR-1541 6% resist) and chlorine-based reactive ion etching (PlasmaTherm 770). A ring resonator coupled to a bus waveguide is shown in Fig. 7.4(a). The waveguide is 700 nm wide by 100 nm tall. The fundamental quasi-TE (x-polarized) mode is shown in Fig. 7.4(b) as calculated by a finite difference mode solver. The effective index is 1.96. A top oxide cladding is deposited by PECVD, and the chip is diced and the end facets polished for optical testing.

We analyze the optical mode confinement for the 700 nm wide by 100 nm tall waveguide structure. It can be shown [56] that the confinement factor Γ in Eq. 3.1 can be broken into a spatial confinement of the electric field energy



(a) (b)

Figure 7.6: (a) SEM image of the low-temperature polysilicon ring resonator coupled to a bus waveguide. (b) Cross-section modal simulation for the 100 nm × 700 nm polysilicon waveguide with $n_{eff} = 1.96$.

density and a confinement in time due to the group index:

$$\Gamma_A = \frac{n_g}{n_{Si}} \frac{\iint_{Si} \varepsilon |\mathbf{E}|^2 \, dxdy}{\iint_{\infty} \varepsilon |\mathbf{E}|^2 \, dxdy} \equiv \frac{n_g}{n_{Si}} \gamma_{Si} \tag{7.1}$$

where γ_{Si} is the percent of the electric field energy density $\varepsilon|\mathbf{E}|^2$ residing in the silicon region. If the polysilicon is lossy, then we desire a low confinement in order to reduce the modal loss. However, if we wish to use the device in a modulator, then we ultimately require high confinement so that the optical mode interacts with the free carriers in the silicon region. In this case, it is the spatial confinement γ_{Si} that must be maintained, since the resonant wavelength shift goes as $\Delta\lambda = \frac{\lambda_0}{n_g}\Delta n_{eff} = \frac{\lambda_0}{n_g}\Delta n\Gamma = \frac{\lambda_0}{n_g}\Delta n\frac{n_g}{n_{Si}}\gamma_{Si} = \lambda_0\frac{\Delta n}{n_{Si}}\gamma_{Si}$. We use finite difference modesolver simulations to find that $\gamma_{Si} = 0.91$ in a silicon waveguide with a standard 450 nm × 250 nm cross-section. In contrast, the 700 nm × 100 nm waveguide in Fig. 7.6b has $\gamma_{Si} = 0.77$ or only a 15% reduction in spatial confinement while remaining single mode.

For testing, we couple a tunable infrared laser on-chip using a polarization controller and a lensed fiber, and the chip output is focused on a photodetector with a high-NA objective. We design inverse tapers [7] down to a width of 300 nm at the chip facet to improve the coupling. This is different from the typical nanotaper width of around 100 nm because the height of the silicon is only 100 nm here.

We measure resonator quality factors on the order of 3,000 sufficient to support high-speed electro-optic modulation [39]. The transmission spectrum of a 40 µm radius ring resonator is shown in Fig. 7.7 with a loaded quality factor $Q_L = \lambda_0/\Delta\lambda_{FWHM} = 2,900$ at $\lambda_0 = 1555.43$ nm and we measure $n_g = 2.157$ from the free spectral range. By fitting the resonance to Eq. 3.2, we determine the round-trip field transmission coefficient to be $a = 0.788$, corresponding to propagation loss $\alpha = -2\ln(a)/L = 19\,\mathrm{cm}^{-1} = 82\,\mathrm{dB/cm}$. In a practical system, materials with low optical loss and low deposition temperature such as PECVD silicon nitride [21] or amorphous silicon [109] could be used for bus waveguides in combination with electrically controllable polysilicon devices.

7.4 Discussion

Several methods within the excimer laser annealing toolbox remain to be explored as they relate to integrated optics applications.

First and foremost, it is important to establish consistent and measurable connections between the laser fluence, grain size, optical loss, and electrical properties of the material. Grain size can be determined most directly by cross-section TEM analysis, but this is a relatively slow and low-throughput process

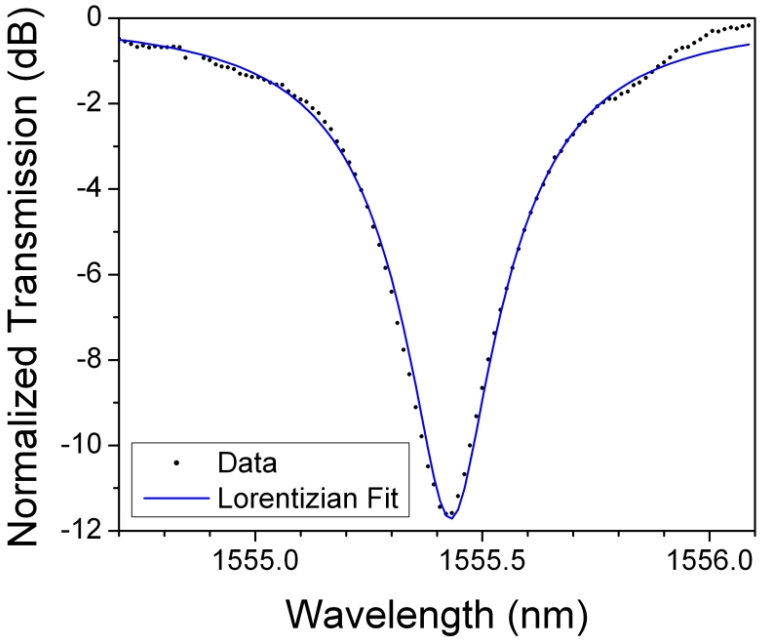


Figure 7.7: Through-port optical response of low-temperature polysilicon resonator for TE polarization.

to analyze the material. Ideally top-surface AFM or SEM microscopy could be used to analyze the grain size, but we have found inconsistent results here due to large surface features that do not correspond to actual grains. It is possible that a simpler approach such as a wafer-level resistance mapping tool could be used to measure the electrical properties of the film, which could then be correlated with grain size. Finally here we measured optical loss in the material by patterning waveguides and resonators and measuring them, which is a relatively slow process. It would be advantageous to investigate ellipsometry or other techniques that could measure optical loss values down to 10's of dB/cm at the wafer scale.

The size and direction of grain growth can be controlled by lithographically patterning an SiO_2 capping layer before the ELA process, causing only some parts of the silicon to melt completely [149, 150]. This regime is called controlled

super-lateral growth and can be used to design the way that the grains interact with a given device. Additionally, the beam can be shaped into a chevron which is stepped across the surface, allowing the growth of large single-crystalline regions [150] which could potentially fit an entire optical device inside.

In this chapter we used a chemical-mechanical polishing (CMP) step to reduce the top surface roughness. This function can actually be carried out as part of the excimer laser annealing process, but illuminating the sample with multiple shots after the initial crystallization [151]. This could be extremely valuable as integrated waveguides are highly sensitive to surface roughness.

It has been shown that the thermal expansion coefficients of the silicon film and the substrate can result in significant stress in the silicon film [152]. This could be important to investigate as it could influence the optical and electro-optic properties of the material.

In conclusion, we have developed a process that produces optical quality polysilicon at low temperatures. Polysilicon is attractive among deposited silicon materials for its electrical properties, which allow for high-speed optical modulators and switches. The maximum steady-state temperature in this process is the PECVD oxide deposition at 400 °C, enabling the polysilicon material to be integrated with a CMOS back-end process to monolithically add optical functionality to a microelectronic chip. Additionally, a similar approach could be used to fabricate photonic integrated circuits on other low thermal budget substrates such as glass or plastic, opening up the advantages of integrated silicon photonics to entirely new platforms.

CHAPTER 8

SUMMARY AND FUTURE WORK

The first chapter introduced the debate regarding which method of silicon photonic integration is most ideal: *chip-scale packaging*, where silicon photonic chips and CMOS chips can be optimized and fabricated separately before integration through traditional microelectronic packaging, or *monolithic front-end integration*, where optical devices and transistors are located in the same layer of crystalline silicon.

In this thesis I investigated materials and devices which could enable a third possible approach, *monolithic back-end integration*, where additional silicon layers can be monolithically integrated on top of a CMOS chip. This approach is at the very early stage of development as compared to the other two. The potential, however, is enormous: monolithic integration of optical links for maximum bandwidth density, with minimal changes to the existing CMOS transistor process flow. I demonstrated microring filters (Chapter 2), slot waveguides for light-emitting devices (Chapter 3), all-optical modulators (Chapter 4), electro-optic modulators (Chapter 5), and infrared photodetectors (Chapter 6) in deposited polysilicon material, and showed initial steps to lowering the processing temperature to back-end CMOS-compatible levels (Chapter 7).

The likely outcome of the integration debate is that every viable approach will be used to meet different goals. In the short term, chip-scale packaging offers the quickest route to integrate silicon photonics with highly optimized CMOS microelectronics. The CMOS chips can be made with absolutely no modifications to the fabrication process, and packaging techniques like wire bonding and flip-chip bonding are already very well developed. The monolithic front-

end approach offers the tightest possible integration of optics and microelectronics. This has already been used by Luxtera to release products for the active optical cable (AOC) market with data rates of 10 Gbps per wavelength channel. They use a modified thick buried oxide SOI wafer on a standard 130 nm CMOS fabrication process. As discussed in the Introduction, the thick buried oxide restricts transistors to gate lengths greater than around 100 nm, which limits the ultimate speed and performance. Monolithic front-end integration on standard thin-oxide SOI or bulk-Si substrates requires significant modifications at the transistor layer [16, 17, 18, 19, 20] which is a major hurdle for commercial adoption.

The potential advantages of the proposed monolithic back-end approach are significant, but significant work remains to prove a level of viability that competes with the other two approaches. The primary challenge is to demonstrate electro-optic device fabrication at temperatures below 450 °C, as discussed in Chapter 7. Once the optical properties of the material have been optimized, the next step is to investigate the appropriate dopant levels to optimize the electrical properties of the device without significantly increasing the optical losses. Once the devices have been demonstrated independently, then a critical demonstration would be to fabricate optical devices and interconnects on top of a CMOS chip and demonstrate the chip performance before and after optical fabrication. This would set the foundation for the viability of the process which would justify further development to improve the devices and fabrication.

Additionally, the high-temperature devices in Chapters 5 and 6 are significant in their own right as they demonstrate a break from the traditional single-layer SOI platform. Polysilicon electro-optic modulators and photodetectors

could be combined with low-loss silicon nitride waveguides in optical links and networks. Even with the device performance shown here which is degraded compared to the best SOI devices, there can still be system-level advantages because the loss in silicon nitride can be as low as 0.1 dB/cm, about 20 times lower than typical losses in SOI. A system-level analysis [145] finds that an especially important advantage to multi-layer systems is that waveguide crossing losses can be eliminated completely, and these crossing losses are a primary limitation for large-scale networks and architectures. Overall, multi-layer integration of optical devices can provide significant advantages at the system level.

In particular, the polysilicon infrared photodetector in Chapter 6 is an important development with room for more improvement. In principle these devices can remove the need for germanium integration, which could significantly decrease the cost and complexity of device integration. The next step in improving these devices would be to identify the dopant type and concentration that maximizes the useful absorption inside the material. Additionally, by engineering smaller devices with contacts placed close to the waveguide absorbing region, the speed and carrier extraction efficiency of the devices could ideally be improved to levels competitive with germanium-based devices.

Silicon photonics has a tremendous potential to revolutionize the connectivity of the world around us. It is my hope that this thesis contributes to the spirit of leaving no stone unturned in the ongoing development of silicon photonic materials, devices, and systems.

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