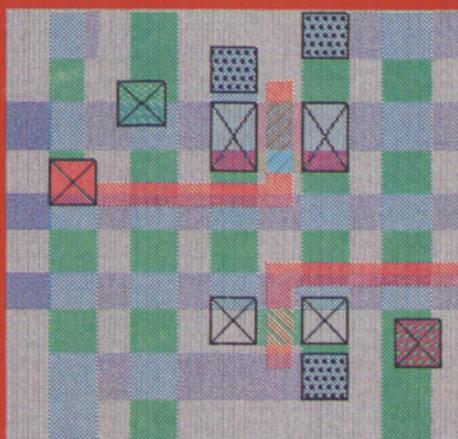
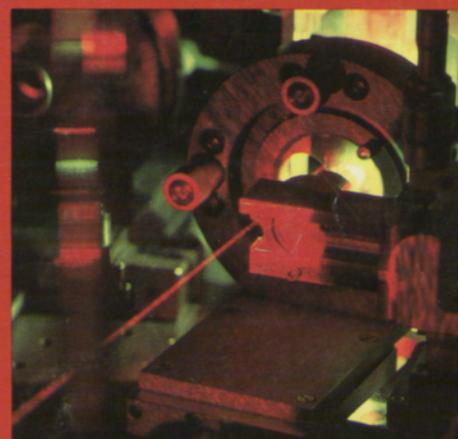
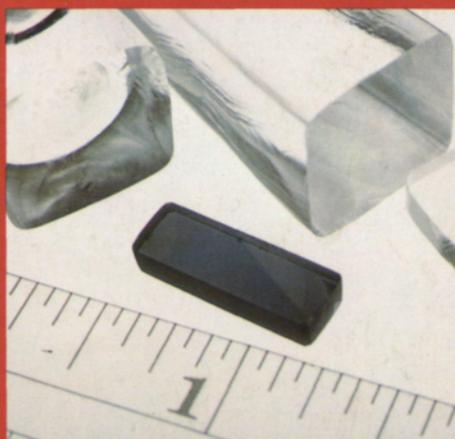
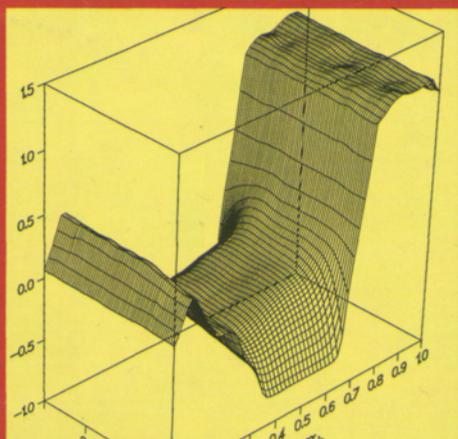


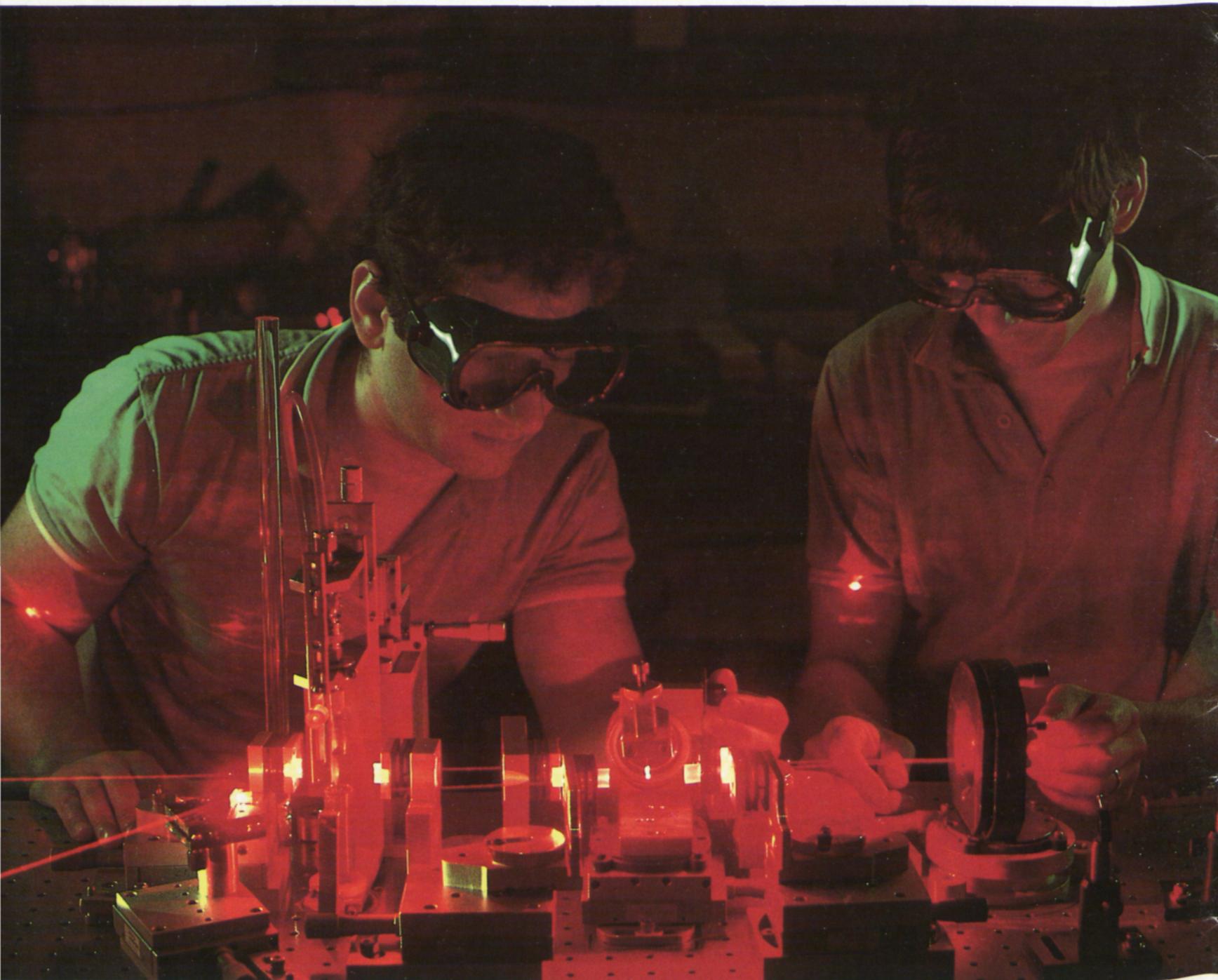
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A NEW THRUST
IN ELECTRONICS
RESEARCH



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Cover illustrations (left to right, top to bottom): (1) A simulation showing electrostatic potential energy as a function of position in a VFET device (see page 12). Here the applied voltage is 0.8 volt and distance is in micrometers. (2) The basis of a color-center laser (see page 31): NaCl crystals grown in a boule, sliced, and infused with sodium vapor to create an impurity that imparts color to the crystal. (3) Part of an ultraviolet femtosecond laser (see page 22). (4) A portion of an arithmetic barrel-shifter cell, part of a custom signal-processing chip (see page 16). (5) An optical micrograph showing a red semiconductor laser composed of an ultrathin (100Å) structure grown in a crystal-growth reactor (see page 4).

Opposite: Graduate students Dan Edelman (at left) and Elliot Wachman work with the ultraviolet femtosecond laser in C. L. Tang's laboratory. This ring-cavity dye laser generates the shortest ultraviolet pulses ever obtained.



Shealy



Weinzierl and Krusius



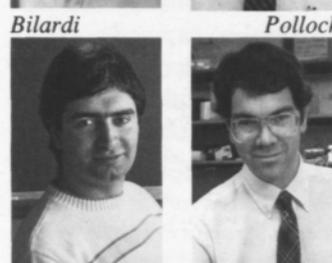
Luk

Schimmel



Torng

Tang



Bilardi

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CORNELL AND JSEP

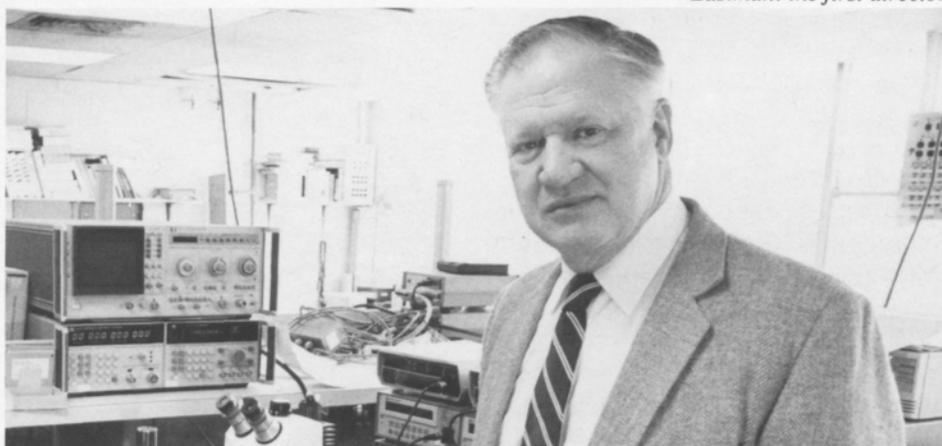
A New Thrust in a Major Program of Electronics Research

A celebration and symposium at the National Academy of Sciences in Washington in September 1986 marked the fortieth anniversary of an unusual national research effort—the Joint Services Electronics Program (JSEP). Researchers from a number of leading universities, including Cornell, were there as representatives of institutions that are participants in the program.

The symposium celebrated the initiation of JSEP in 1946, soon after the end of World War II. As noted in the symposium proceedings*, forward-looking scientists and administrative leaders at universities and military agencies established the program for two reasons: to maintain research and development capabilities that were created during the war, and to promote new university research of interest to all three branches of the military. Today JSEP is the oldest university research program supported by the federal government.

Measured by any criteria, JSEP has been extremely successful. Significant,

*D. Robb and A. Shostak, eds. 1986. *Proceedings of the Fortieth Anniversary Symposium of the Joint Services Electronics Program*. Washington, DC: ANSER.



Eastman: the first director

often pioneering research has been achieved in such areas as atomic clocks, masers, lasers, communication theory and practice, microelectronics, and high-speed electronic digital circuitry and computation. Obviously, the benefits have extended well beyond the military.

The first universities participating in JSEP were the Massachusetts Institute of Technology, Columbia University, Harvard University, and the Polytechnic Institute of Brooklyn. Later they were joined by other institutions, including Stanford University, the University of California at

Berkeley, the University of Illinois, the University of Southern California, the University of Texas, Ohio State University, and Cornell University. Twelve institutions are now participating.

CORNELL ACHIEVEMENTS WITH SUPPORT FROM JSEP

At Cornell, JSEP-supported research was begun in the spring of 1977 under the direction of Lester F. Eastman, the John L. Given Professor in the School of Electrical Engineering. (Eastman is also an alumnus, holding three Cornell degrees.)

“Significant, often pioneering research has been achieved. . .”

During the first decade, the focus was on microwave semiconductors—the preparation of compound semiconductor materials, and the development of electronic devices and circuits. The achievements included many innovations in molecular-beam epitaxy and organometallic vapor-phase epitaxy, both of which are sophisticated techniques for growing compound semiconductor heterostructures. A number of new device concepts were developed, and speed records for electronic devices were broken several times. Research results were presented in 175 refereed publications and 113 conference papers.

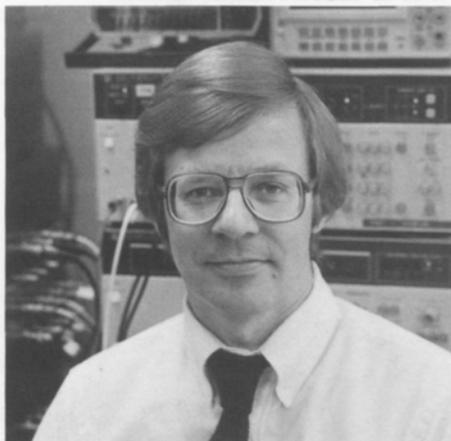
Equally important was the education of young researchers who became leaders in their field. Thirty-nine Ph.D. and fifteen M.S. degrees were awarded during that first decade.

Throughout this period, Cornell hosted the biennial IEEE–Cornell Conference on Microwave Semiconductors, which was initiated by Eastman.

THE CURRENT EMPHASIS ON HIGH-SPEED SYSTEMS

A new thrust in JSEP research at Cornell was started in May 1988 under the direc-

Krusius: the current JSEP director



tion of Professor J. Peter Krusius. Current work is organized around two complementary and synergistic areas: high-speed devices based on ultra-high-speed compound semiconductors, and high-speed signal processing. The Cornell program is monitored by the Air Force Office of Scientific Research; the Cornell group works with Dr. Horst Wittmann and Dr. Gerald Witt.

Six faculty members and their students are involved in the program. Five are electrical engineering professors: in addition to Krusius, they are Franklin T. Luk, Clifford R. Pollock, J. Richard Shealy, C. L. Tang,

and H. C. Torng. The sixth participant, Gianfranco Bilardi, is on the computer science faculty. The articles in this issue are written by these investigators and some of their associates. (Some of the ongoing research by Eastman's group was described in the Spring 1988 issue of this magazine.) These articles give a good idea of the current lines of JSEP-sponsored research and suggest the significance of past, present, and potential accomplishments.

All the work carried out in JSEP is part of the participants' overall research programs, which often have additional support from the National Science Foundation and from industry. The programs benefit from the presence on campus of the National Nanofabrication Facility, with its capabilities for device fabrication, and a national supercomputer center, with its facilities for computer simulation.

The research is rooted in basic scientific investigation, and has important general applicability in many areas of electronics technology. At Cornell it continues as a major component of the research and graduate-study program at the College of Engineering.

GROWING CRYSTALLINE LAYERS FOR NEW HIGH-SPEED ELECTRON DEVICES

By J. Richard Shealy

With a technique pioneered at Cornell, structures consisting of semiconductor materials in layers that can be almost as thin as the diameter of an atom can be grown by deposition from chemical vapors. Materials of this kind provide the characteristics needed for making the ultra-high-speed transistors of the future.

The technique, called *organometallic vapor phase epitaxy* (OMVPE), has been under development over the past six years at the School of Electrical Engineering as part of the government-sponsored Joint Services Electronics Program (JSEP). The thrust of the JSEP research is to design and fabricate structures that will improve electron velocities—a necessity for the higher-speed electronic devices.

The materials under study are the so-called III-V compound semiconductors, in which electrons can travel up to ten times faster than in silicon. With the epitaxial growth technique, a series of deposited layers of different compositions can be used to confine electrons to narrow regions in space and so alter their properties. The energy of the electrons in such regions can be raised above the energy that is characteristic of the bulk semiconducting material.

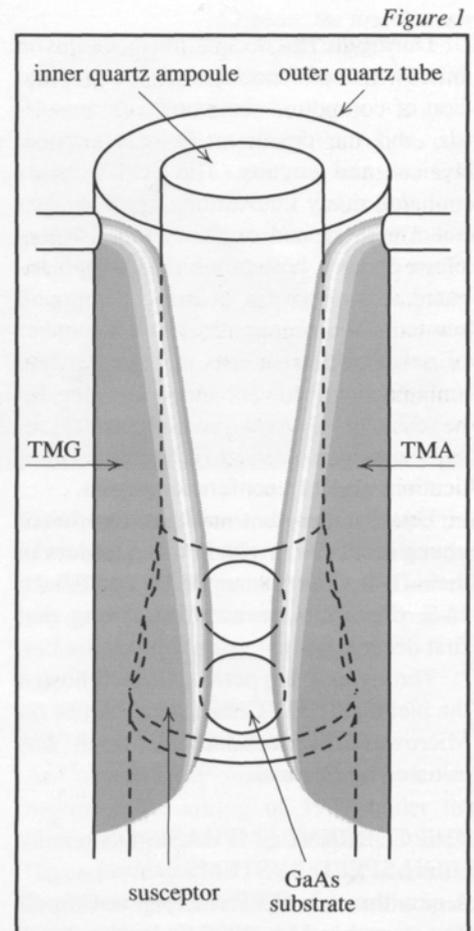
A CRYSTAL-GROWTH REACTOR DEVELOPED AT CORNELL

A novel type of crystal-growth apparatus now under development is shown in Figure 1. Because of its geometry, this reactor is referred to as a *vertical barrel*, a type that was originally used in the vapor deposition of silicon. In this cell the substrates are held by gravity to an induction-heated graphite susceptor, which is supported by an evacuated quartz ampoule.

The unique property of this design is the localization of different combinations of reactants, as is shown in the figure. The reactants in this case are trimethyl gallium (TMG), trimethyl aluminum (TMA), and arsine (AsH_3). These vapors are suspended in a hydrogen carrier gas and by careful control of the fluid dynamics the TMG and TMA are separated and contained in the re-

Figure 1. The "vertical barrel" crystal-growth apparatus under development at Cornell.

In this case the reactants are arsine, which is dispersed throughout the reactor, and trimethyl gallium (TMG) and trimethyl aluminum (TMA), which are separated into different regions. A superlattice is formed by condensation of the vapors on a rotating substrate.



“... semiconductor materials in layers that can be almost as thin as the diameter of an atom can be grown by deposition from chemical vapors.”

gions shown. These regions extend down through the cell with the gases flowing from top to bottom, and as a substrate is rotated through them, different crystalline layers—in this case, GaAs and AlAs—condense from the vapor on each side of the cell. The result is a periodic structure often referred to as a *superlattice* (see Figure 2).

If the superlattice contains high- and low-bandgap semiconductors, the electrons that are present in the structure will be contained in the lower bandgap regions. In the case of GaAs/AlAs structures, the lower-bandgap material is the GaAs. This kind of apparatus has produced films with transitional regions (interfaces) between the semiconductors that are a single atomic layer—less than 2.8 Å or 2.8×10^{-10} meter—in thickness.

Figure 2. A transmission electron micrograph of a semiconductor superlattice grown by chemical vapor deposition in a special crystal-growth reactor. The layers, which have the appearance of rows, are about 2.8 Å apart, about the thickness of a single atomic layer, and are about two atomic diameters thick.

The micrograph was prepared by Professor Barry Carter at Cornell's Materials Science Center.

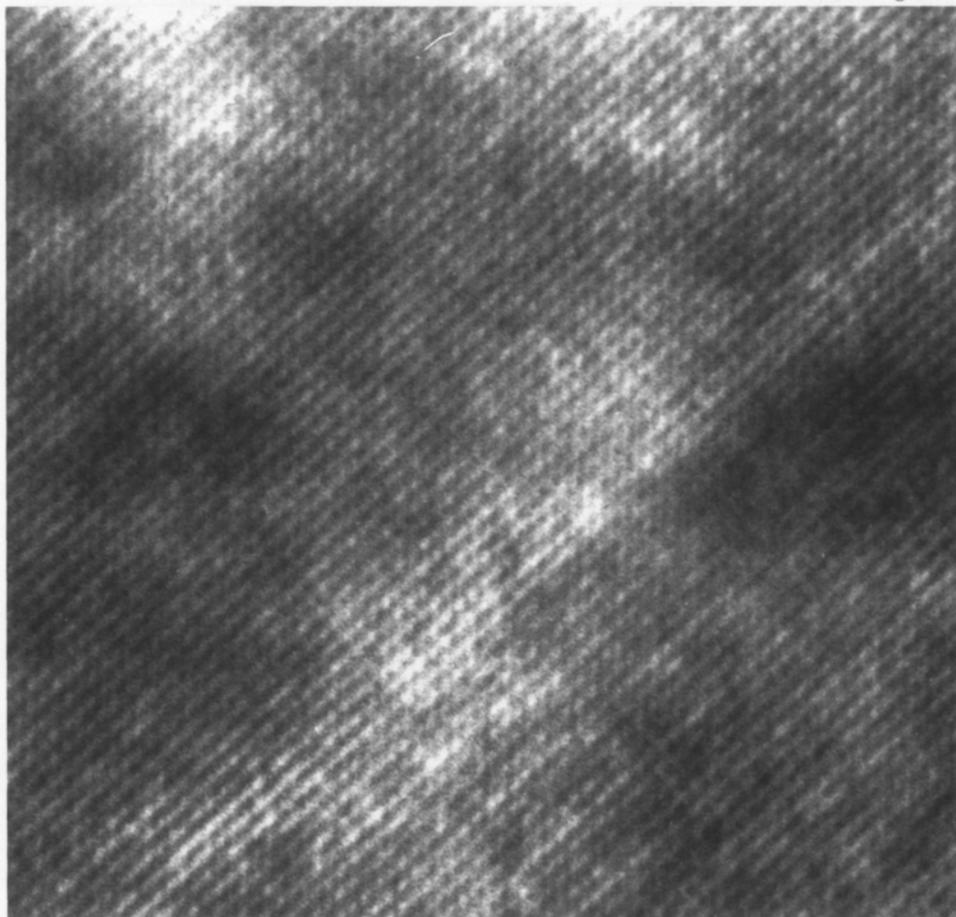


Figure 2

Figure 3

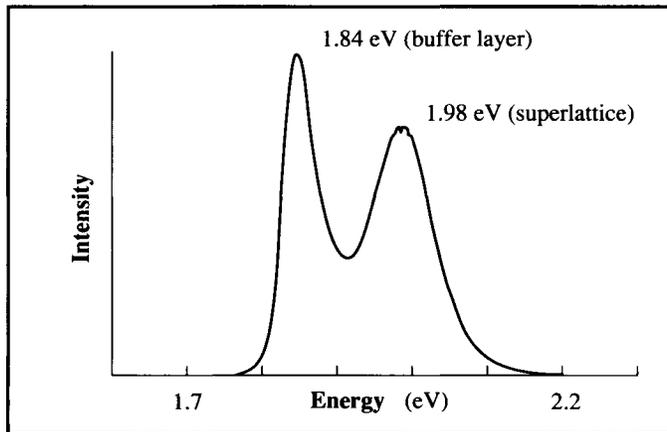


Figure 3. The photoluminescence spectrum of a superlattice structure.

Incident laser radiation causes the emission of photons of different energy (and therefore wavelength) from different parts of the structure. The peak at 1.84 eV corresponds to the relatively thick buffer, which is $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$. The peak at 1.98 eV corresponds to the ultrathin layers of $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$ in the superlattice. The higher energy is the result of confinement of electrons in the layer.

The temperature is 300 K.

Figure 4

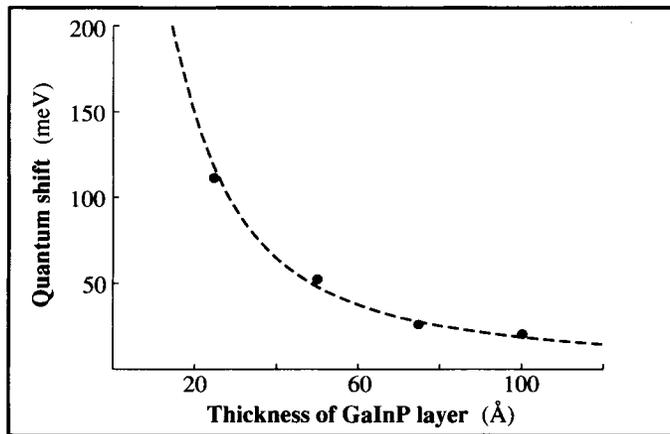


Figure 4. Shifts in the energy of electrons as a result of confinement in a narrow region—the narrower the region, the higher the energy. The structures represented here are superlattices of $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}/\text{Al}_{0.5}\text{In}_{0.5}\text{P}$ in which the $\text{Al}_{0.5}\text{In}_{0.5}\text{P}$ layer is 100 Å thick and the $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$ layers are of different thicknesses. Theoretical (dashed curve) and experimental results are shown.

CHARACTERIZING THE ELECTRON ENERGY IN THE SUPERLATTICES

With reasonably simple analysis techniques, one can observe the elevated energy of electrons that results from their spatial confinement in superlattices.

One such technique is called *photoluminescence*. Typically, the semiconductor is exposed to a visible (green or blue) laser, which gets absorbed and generates pairs of high-energy electrons and holes in the material. These pairs come into equilibrium with the semiconductor lattice and recombine at an energy that is characteristic

of the energy gap of the semiconductor structure.

Incidentally, a major related activity in the JSEP program is the study of processes that take place during the achievement of thermal equilibrium. They are very rapid, occurring in the range of 10^{-15} second, and generally go unnoticed in ordinary photoluminescence measurements. The recombination process is of interest in the research on semiconductor structures because it results in the efficient generation of photons with energies (or wavelengths) characteristic of the semiconductor.

An example of how the photoluminescence technique is used to analyze epitaxially grown semiconductor structures is illustrated in Figure 3. The photoluminescence spectrum is that of a structure, grown by OMVPE, that consists of a semiconductor buffer layer of $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$ and a superlattice of two ternary (three-component) semiconductors— $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$ and $\text{Al}_{0.5}\text{In}_{0.5}\text{P}$. The two features observable in the spectrum are easily identified with the buffer layer and the superlattice. In both cases, electron-hole pairs are resident in the $\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$, but the environment is different. The buffer layer is hundreds of electron wavelengths in thickness, so that there is no spatial confinement of electrons. In the superlattice, on the other hand, the electrons are contained within layers comparable in thickness to an electron wavelength. (Typically, this wavelength is about 100 Å; in this case it is 25 Å.) As a result of the spatial confinement, the energy of the electron-hole pairs is raised, and when the

electrons and holes recombine, photons with wavelengths shorter than that characteristic of the bulk semiconductor exit the sample. The structure yields red light from the buffer and orange light from the superlattice.

The narrower the region in which electrons are contained, the higher their energy. These energy shifts can be predicted from simple quantum mechanical calculations, as represented by the dashed curve in Figure 4. These energy shifts can also be determined experimentally, simply by taking the difference between the two peaks in the photoluminescence spectrum. The data points shown in Figure 4 were obtained by varying the thickness of the lower-bandgap ($\text{Ga}_{0.5}\text{In}_{0.5}\text{P}$) layers. The agreement of the theoretical curve and the experimental data indicates that this phenomenon is reasonable well understood.

THE USEFULNESS OF CRYSTAL-GROWTH TECHNIQUES

How does this research contribute to the development of improved electronic and optoelectronic devices?

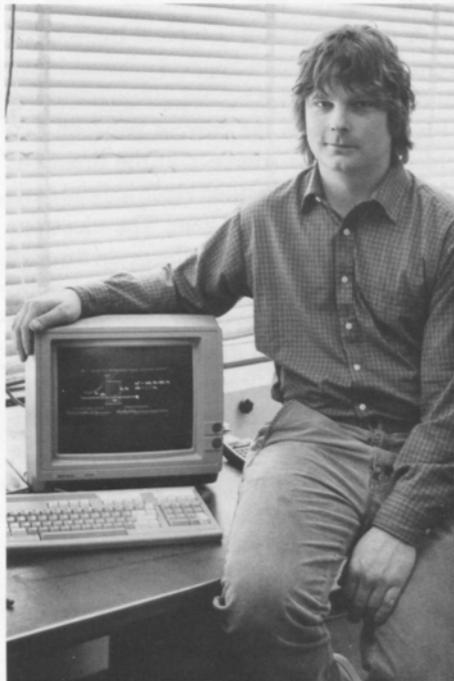
The fabrication of compound semiconductor structures containing ultrathin crystalline layers that can be closely controlled in composition and dimension is the basic capability. By examination with the non-destructive optical technique of photoluminescence, one can identify the bandgaps of bulk semiconductor layers (in our example, the buffer layer) and of semiconductor structures (the superlattice). Then, with knowledge of the materials' bandgap parameters, quantum mechanics can be used to predict the dimensions of the superlattice. This provides important information for more detailed studies of electron relaxation—studies such as those being conducted by Professors C. L. Tang and

Clifford R. Pollock. And once the electron relaxation processes are established, the materials can be employed in specially designed device structures, as in research directed by Professor J. Peter Krusius.

The research provides a way of creating high-velocity channels in electronic devices. The electrons in tomorrow's ultra-high-speed transistors may well travel along pathways prepared in electrical engineering laboratories at Cornell.

J. Richard Shealy, an assistant professor of electrical engineering, joined the Cornell faculty in 1987. He earned his Ph.D. here in 1983, working with Professor Lester F. Eastman, and then continued in that laboratory as a research associate.

His previous degrees are the B.S. in electrical engineering from North Carolina State University and the M.S. in electrophysics from Rensselaer Polytechnic Institute.



“The electrons in tomorrow’s ultra-high-speed transistors may well travel along pathways prepared in electrical engineering laboratories at Cornell.”

SUPERCOMPUTER SIMULATION

for Understanding and Designing Ultra-High-Speed Semiconductor Devices

by J. Peter Krusius, Abdul-Azeez Al-Omar, and Steven R. Weinzierl

All of modern microelectronics rests on semiconductor devices. Two or more such devices are connected together into electronic circuits, which provide logic operations or amplification of analog signals. Large numbers of semiconductor devices are assembled on a single substrate in integrated circuits (ICs) to form the powerful semiconductor chips used in computers and in communication and control systems.

While all large ICs with a high density of devices are made of silicon, small ICs with very high-speed devices are made of gallium arsenide (GaAs) or similar compound semiconductors. The world record for one switching operation (logic inversion) in a compound semiconductor device is 4.8 picoseconds (one picosecond = 10^{-12} second) at liquid nitrogen temperature. In this time light travels a distance of only 480 micrometers in GaAs.

In this article we discuss new concepts being used to make compound semiconductor devices even faster than they are today. The approach we are taking in our research, which is supported by the Joint Service Electronics Program (JSEP) at Cornell, is that of computer simulation on a supercomputer.

HOW ELECTRONS MOVE IN A SEMICONDUCTOR DEVICE

High-speed devices are the result of high-speed electrons in the devices. To increase device speed, it is necessary to understand how electrons behave in a particular structure and how they can be made to move faster.

A micrograph of a typical high-speed compound semiconductor device is shown in Figure 1. This is a field-effect transistor (FET), in which the current between two electrodes—the source and the drain—is modulated by an applied electric field from a third electrode, the gate. The electrons travel from the source to the drain through a sequence of dissimilar compound semiconductor layers—gallium arsenide (GaAs), aluminum gallium arsenide (Al-GaAs), and their alloy $\text{Al}_x\text{Ga}_{1-x}\text{As}$ —which constitute a heterostructure. The device shown in Figure 1 has twelve active fingers; the cross section through two of them is shown in Figure 2.

To obtain the highest possible speed, the device must be designed so that the structure, the geometrical dimensions, and the composition of the materials are optimized. Since a number of complex con-

cepts and tradeoffs are involved, computer simulation is an ideal tool for providing generic understanding and for designing specific devices.

SIMULATING ELECTRON BEHAVIOR IN A DEVICE

The most suitable technique for studying the behavior of the electron ensemble in heterostructure devices is particle simulation by the Monte Carlo method. Because the electrostatic potential is determined by the spatial electron distribution, a self-consistent approach is needed. In such a self-consistent Monte Carlo method, an ensemble of electrons is followed. Electrons are continuously “injected” into the device at the source metal electrode and eventually “collected” at the drain electrode. Inside the device, the electrons of the ensemble interact with the semiconductor crystal lattice, among themselves, and with the externally applied electromagnetic field. These interactions are illustrated in Figure 3.

In order to arrive at a self-consistent solution on the computer, we first advance the electrons for a predefined time interval according to their laws of motion. Next we

Figure 1

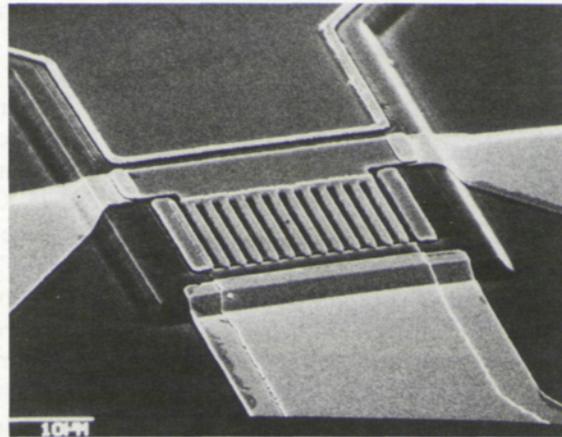


Figure 1. A scanning-electron micrograph of a high-speed vertical field-effect transistor (VFET).

This device has twelve active fingers, each 12 micrometers long. The drain electrode is at the top, the source pads are on the left and right, and the gate electrode is at the bottom. The device was fabricated by Joel R. Wendt, a member of Professor Lester F. Eastman's group at Cornell.

Figure 2

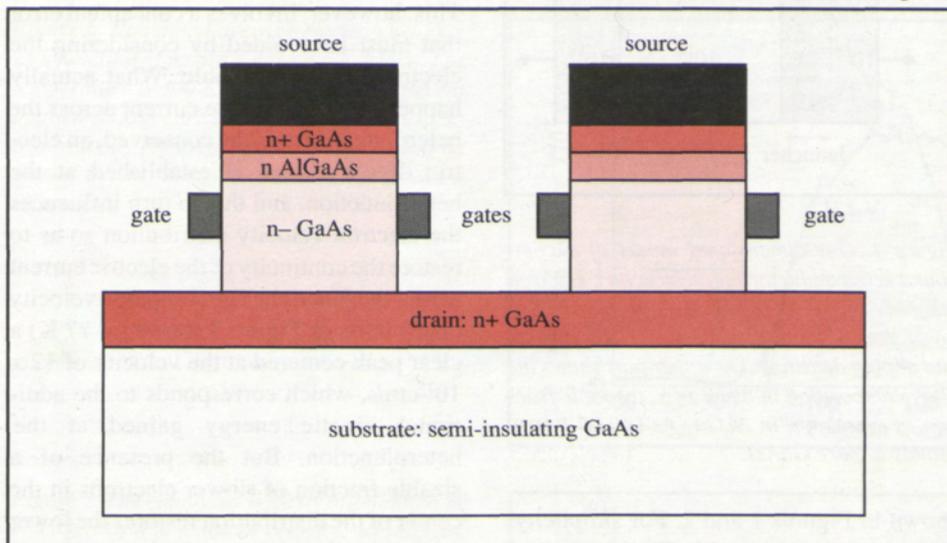


Figure 2. Diagram of the cross section of two active fingers of a heterostructure VFET device such as the one shown in Figure 1.

The source contact is on the top, the gate electrodes are on the sides, and the drain electrode is at the bottom of each active finger. The prefixes n+, n, and n- denote heavy, moderate, and light doping.

Figure 3

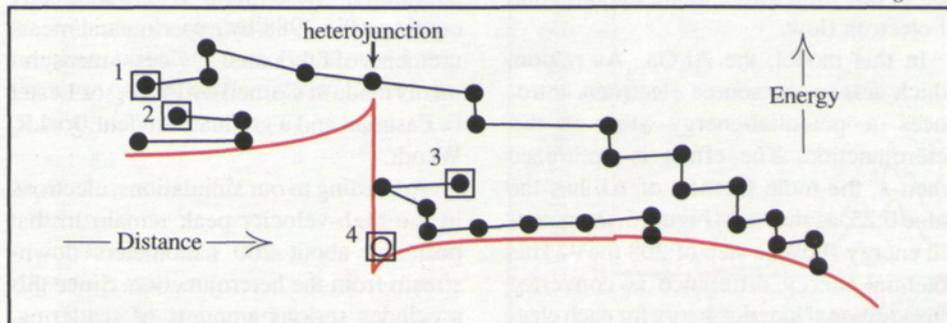


Figure 3. Schematic diagram of electron paths in a heterostructure device in the total energy-distance plane.

The curve in color denotes the minimum potential energy (conduction band edge) for electrons. Electron 1 passes over the heterojunction into the primary downstream direction; electron 2 gets reflected upstream from the heterojunction; electron 3 is reflected downstream from the heterojunction; and electron 4 is trapped in the potential well at the heterojunction. Abrupt vertical energy changes of the electrons signify energy losses, or gains, in interactions with the semiconductor crystal.

Figure 4

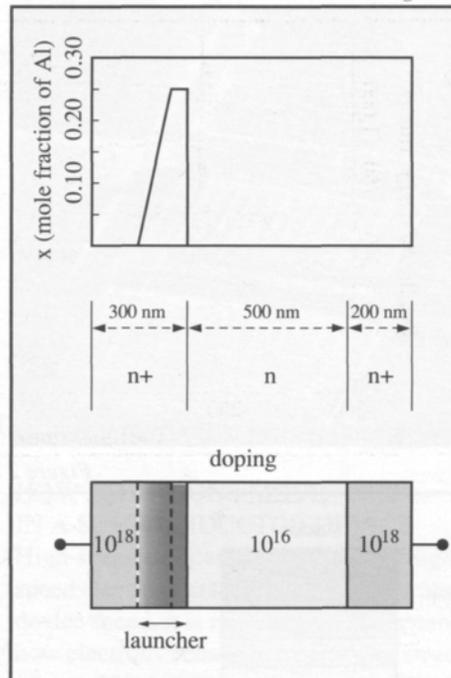


Figure 4. One-dimensional model of a compound semiconductor heterostructure electron launcher made of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and GaAs. The lower part of the figure shows the dimensions and doping densities. The upper part shows the alloy composition in terms of x , the mole fraction of aluminum in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ ($x = 0$ corresponds to pure GaAs).

calculate the charge distribution with the electrons "frozen" in their positions, and using Poisson's equation, we calculate the electric field and the electrostatic potential for many points inside the device. Then we start another time interval, and so on. This method allows us to look at both time-dependent and steady-state phenomena.

In carrying out this kind of simulation, we typically use an ensemble of more than ten thousand electrons, a spatial mesh (needed to discretize the equations to be solved) with a spacing of 3 nanometers (1 nanometer = 10^{-9} meter), and a time interval of 10 femtoseconds (1 femtosecond = 10^{-15} second). One-dimensional steady-state problems such as the one discussed below require (for 15,000 electrons) about one hour of central processing unit (cpu) time on the IBM 3090-600 supercomputer at Cornell's Center for Theory and Simulation in Science and Engineering.

ENHANCED ELECTRON VELOCITY VIA HETEROJUNCTION LAUNCHER

We have used simulation with the supercomputer to study, for example, how electron velocities can be enhanced by the insertion of an $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterojunction into a device such as the one

shown in Figures 1 and 2. For simplicity, the model diagrammed in Figure 4 is limited to one dimension, along the direction of electron flow.

In this model, the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ region, which acts as the source electrode, introduces a potential-energy step at the heterojunction. The effect is optimized when x , the mole fraction of Al, has the value 0.25; as shown in Figure 5, the potential energy shows a step of 208 meV. This potential-energy difference is converted into additional kinetic energy for each elec-

tron that crosses the heterojunction. Because of their higher velocity, the electrons' transit time across the device is shorter, and therefore the device is faster.

According to our simulations in Figure 6, average electron velocities as high as 2.75×10^7 centimeters per second (cm/s) can be reached with this launching technique. This represents an increase in velocity of two and one-half times the maximum drift velocity (about 10^7 cm/s) in a long uniform semiconductor sample.

An even larger enhancement would be expected if the energy conservation principle were applied to the average electron. This, however, involves a conceptual error that must be avoided by considering the electrons as an ensemble. What actually happens is this: because current across the heterojunction must be conserved, an electric dipole charge is established at the heterojunction, and this in turn influences the electron-velocity distribution so as to restore the continuity of the electric current across the junction. The computed velocity distribution in Figure 7 shows (at 77 K) a clear peak centered at the velocity of 12×10^7 cm/s, which corresponds to the additional kinetic energy gained at the heterojunction. But the presence of a sizable fraction of slower electrons in the center of the distribution restores the lower average velocities required for current continuity. These findings were indirectly confirmed in 1988 by experimental measurements of fabricated devices—measurements made at Cornell by Professor Lester F. Eastman and a graduate student, Joel R. Wendt.

According to our simulations, electrons in the high-velocity peak remain in that peak for about 200 nanometers downstream from the heterojunction. Since this precludes serious amounts of scattering,

Figure 5. Computed potential energy of electrons as a function of their position across the device (the Γ valley band edge). The temperature is 300 K. Results for three different voltages applied across the device are shown. The position of the heterojunction is indicated.

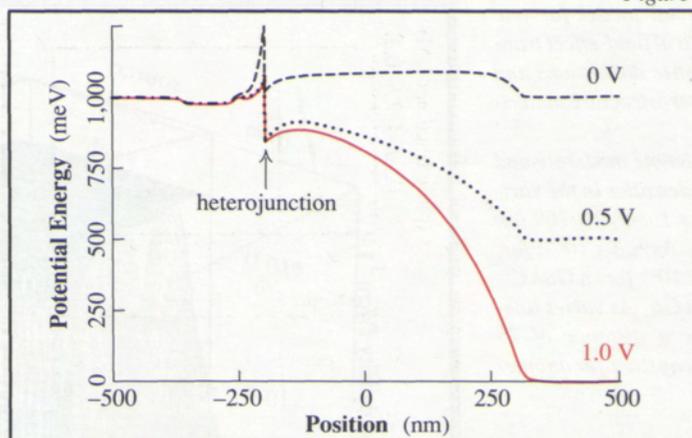


Figure 5

Figure 6. Computed average electron velocity as a function of position across the device. The temperature is 300 K. Results for two different applied voltages are shown. The saturated electron velocity for large electric fields at 300 K, shown by the horizontal line, is given as a reference.

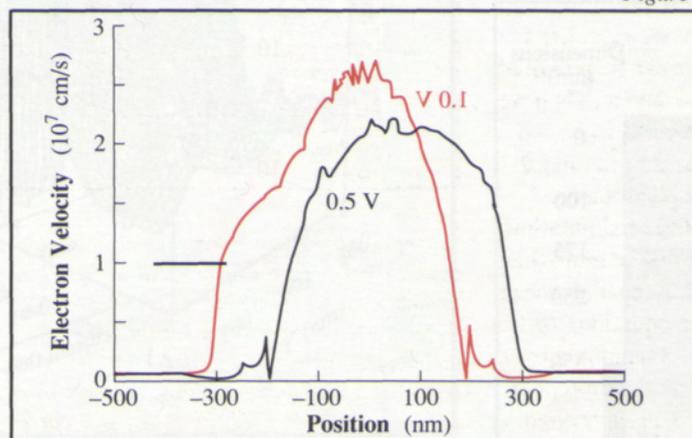


Figure 6

Figure 7. The computed velocity distribution of electrons as a function of velocity. Results for two temperatures are given.

The distributions were calculated for a point 25 nanometers downstream from the heterojunction and for an applied voltage of 1 volt; they have been normalized to unity.

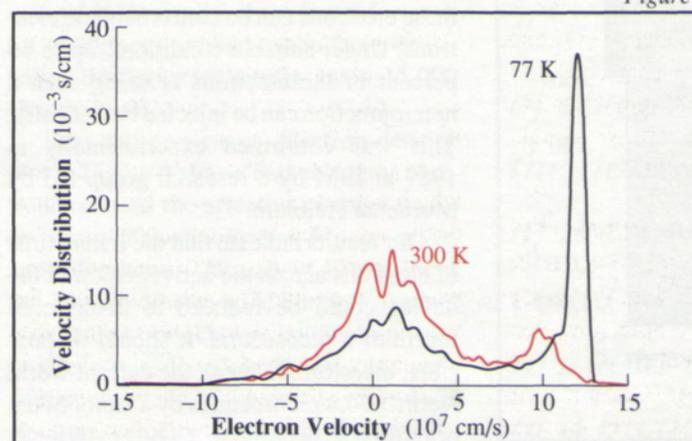
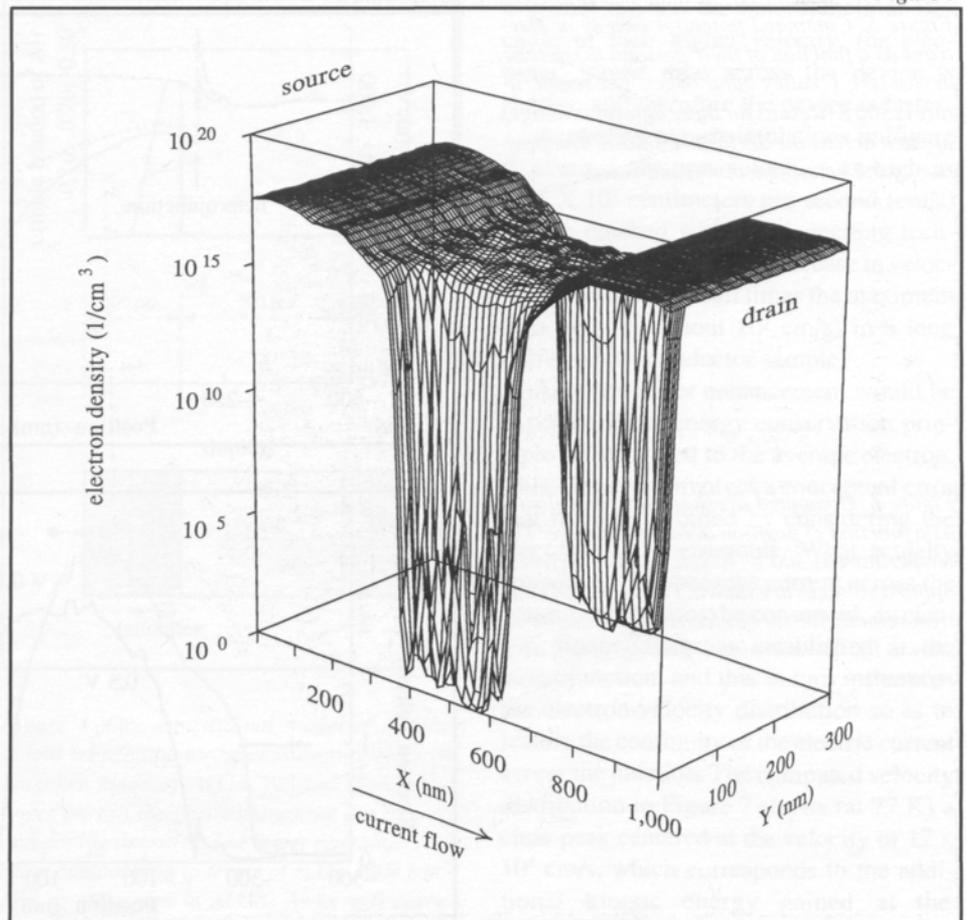
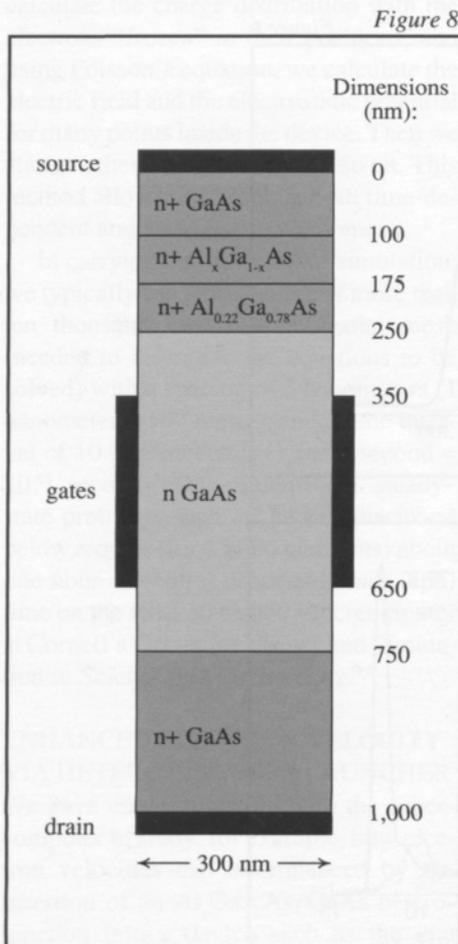


Figure 7

Figure 8. A two-dimensional model for one finger of a high-speed vertical field-effect transistor (VFET). The geometric dimensions and the compositions of the heterostructure materials are shown.

The prefixes *n* and *n+* denote moderate and heavy doping. The doping densities in the various regions are (in units of $1/\text{cm}^3$) 2×10^{18} for *n+*GaAs and *n+* $\text{Al}_x\text{Ga}_{1-x}\text{As}$; 3×10^{17} for *n+* $\text{Al}_{0.22}\text{Ga}_{0.78}\text{As}$; and 2×10^{16} for *n*GaAs.

The Al fraction in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ varies linearly from 0 to 0.22 over a distance of 75 nanometers and then stays constant for another 75 nanometers.



these electrons can be called ballistic electrons. Under suitable conditions, up to 80 percent of the electrons crossing such a heterojunction can be injected ballistically. This was confirmed experimentally in 1987 at IBM by a research group led by Mordehai Heiblum.

Our results indicate that the transit time of electrons across the active region of the device could be reduced to about one-fourth of a picosecond. It should be possible, therefore, to break the current world record of 4.8 picoseconds by a factor of ten or more.

Figure 9. Simulated electron density in the Figure 8 device for an applied voltage of 1 volt. A logarithmic scale has been used for the electron concentration, shown here as a surface over the plane of the device. The gate electrodes introduce a total repulsive potential of 0.8 volt from both electrodes.

TWO-DIMENSIONAL SPACE-CHARGE PHENOMENA

Currently, we are exploring two-dimensional phenomena by computer simulation, using a two-dimensional version of our computer code.

An example is shown in Figure 8. The

Figure 10

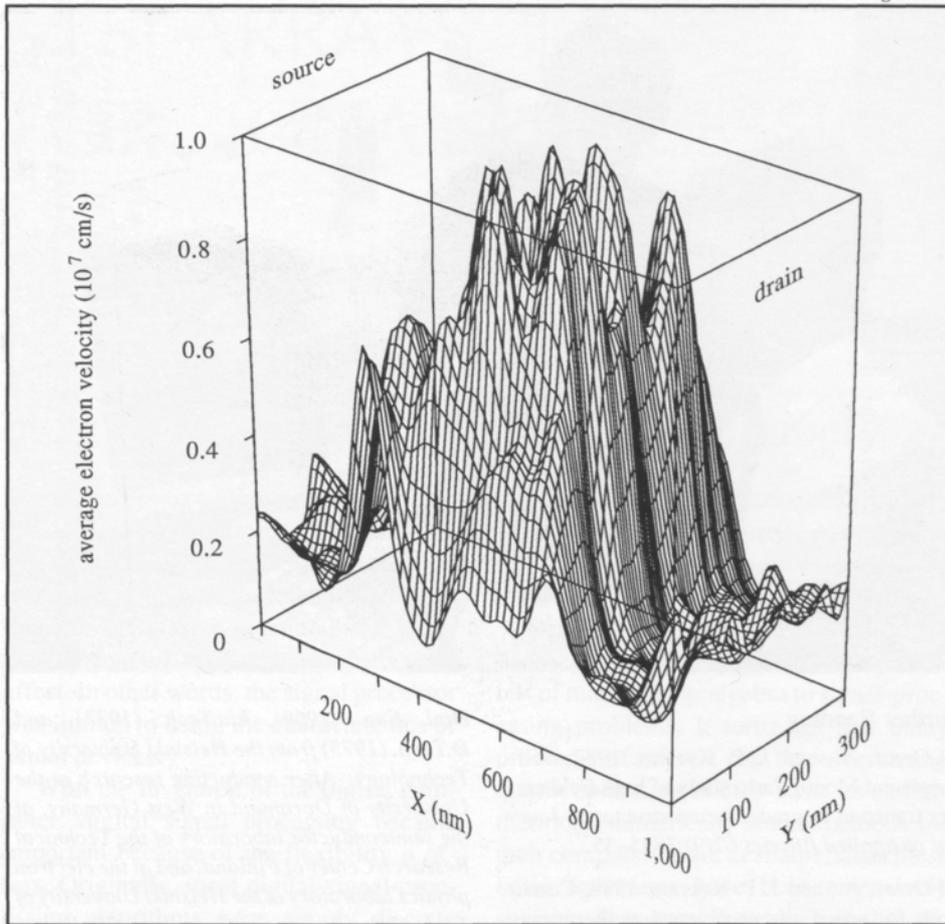


Figure 10. Simulated magnitude of the average electron velocity in the device illustrated in Figure 8 for the voltages given for Figure 9. The resolution is limited by the statistics; the number of electrons assumed is 25,000.

entire lateral cross section of the active finger, including the gate electrodes, is modeled. The lateral gate electrodes modulate, via the field effect, the width of the active channel; electrons are pushed into the interior of the channel in accordance with Coulomb repulsion. A steady-state computer solution on the IBM 3090-600

now takes, typically, three hours for each set of voltages applied to the three terminals of the device (assuming, again, 15,000 electrons).

The self-consistent electron-density plot in Figure 9 shows that each gate electrode reduced the effective channel width by about 600 nanometers for the given applied voltage. Thus, about 40 percent of the 300-nanometer-wide vertical channel is excluded from current conduction.

Clear two-dimensional velocity phenomena are seen in the profile of average electron velocity shown in Figure 10.

“... the transit time of electrons across the active region of the device could be reduced to about one-fourth of a picosecond.”

Right: J. Peter Krusius (at right) and Steven R. Weinzierl use computer simulation in the work they describe here. The third author of this article, Abdul-Azeez Al-Omar, had already left Cornell for Kuwait at the time the photograph was taken.

These phenomena appear to be due to domain formation and lateral contact effects.

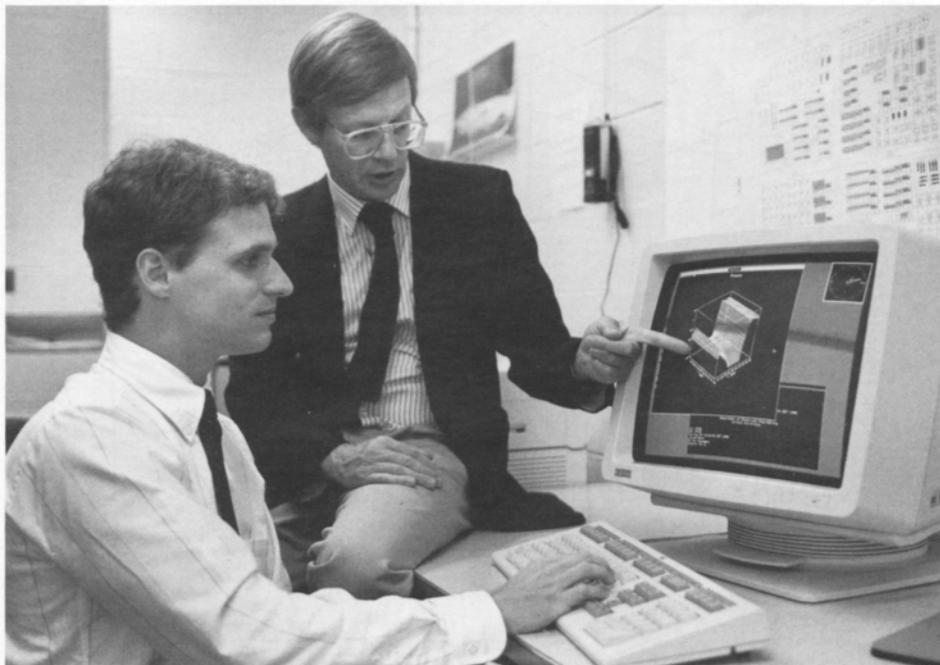
Currently we are mapping out other important two-dimensional phenomena.

WHY SUPERCOMPUTER SIMULATION IS VALUABLE

We have given two examples of how the physical phenomena that occur in high-speed compound semiconductor devices can be studied using self-consistent particle simulations.

Even though a supercomputer is needed to perform the extensive numerical computations, the simulations are well worth the cost and effort. Simulation is orders of magnitude cheaper for exploratory work than the fabrication and measurement of actual devices. In addition, it provides information that cannot be obtained experimentally. (Microscopic electron behavior on a time scale of less than one picosecond can be probed experimentally using femtosecond optics—see articles by C. L. Tang and Clifford R. Pollock in this issue—but this can be done only in semiconductor structures much larger than the nanometer devices we have discussed.) A further advantage of simulation is that it gives us insight into electron behavior and how it can be influenced.

Equipped with a supercomputer, we are prepared to explore the physics of a new generation of subpicosecond, nanometer-scale semiconductor devices.



Further Reading

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J. Peter Krusius, a professor of electrical engineering, is director of the Joint Services Electronics Program at Cornell. Formerly he served as associate director of the National Research and Resource Facility for Submicron Structures (now the National Nanofabrication Facility) at the university. He holds the degrees

Dipl. Eng. (1969), Lic.Tech. (1972), and D.Tech. (1975) from the Helsinki University of Technology. After conducting research at the University of Dortmund in West Germany, at the semiconductor laboratory of the Technical Research Center of Finland, and at the electron physics laboratory at the Helsinki University of Technology, he came to Cornell as a Fulbright fellow in 1979 and joined the faculty in 1981.

Abdul-Azeez Al-Omar, a native of Kuwait, received his Cornell Ph.D. in electrical engineering this past August and is now teaching at Kuwait University. Previously he studied at the University of Wisconsin at Madison, earning B.S. degrees in electrical engineering and in mathematics—both with distinction—in 1980 and the M.S. in 1983.

Steven R. Weinzierl is a Ph.D. candidate in electrical engineering at Cornell. He received the A.B. degree in physics and mathematics/computer science from Vassar College in 1986. At Vassar he helped develop real-time graphics simulations as part of a software package used for teaching introductory physics.

VLSI ARRAYS FOR SIGNAL PROCESSING

by Franklin T. Luk and David E. Schimmel

Signal processing evolved in the domain of the analog circuit designer. To transform and analyze signals, the designer used circuits whose impulse response (in the time domain) or transfer function (in the frequency domain) approximated the desired effect. In other words, the signal processor was limited to using the characteristics of actual devices.

With the invention of the digital computer, digital signal processing became important because of the flexibility it offers. Originally, most digital-signal-processing algorithms were simply discrete simulations of analog circuits that the designers already knew how to make. Their primary advantage was that the desired response could be varied simply by changing the program's parameters. But this approach takes little advantage of the potential of digital methods. In the digital world, almost any function one can imagine can be approximated.

There are problems, however. Like the analog designer, the digital designer needs to consider the stability of the systems, but in addition must take into account the effects of rounding errors. Problems of this kind have been studied extensively by

means of numerical linear algebra. It is also very useful to look at signals and systems in matrix terms; much insight can be gained by proceeding in this systematic way.

Recently, our group and others have been studying the application of the methods of matrix linear algebra to signal-processing problems. It turns out that many problems of interest can be solved using matrix operations at their basic level. Furthermore, numerically stable methods for their computation are available, since these basic operations have been extensively studied. The stumbling block is that the time complexity of many of these methods is unacceptably large. The answer is very-large-scale integration (VLSI).

USING ADVANCED COMPUTING TECHNOLOGY

VLSI has provided the means to put a million or so devices on a single chip, and that number should grow by at least two orders of magnitude. This potential computing power is what we plan to exploit to solve complex signal-processing problems in acceptably short periods of time.

The basic idea is to perform the necessary calculations *in parallel*, and therefore

more quickly. The first task is to find a suitable algorithm—one that will reveal all the possible parallelism. This objective may not always be attainable: some algorithms are inherently sequential and cannot be expressed in parallel form.

We must also consider several architectural criteria in our design process. The computations should map on to a regular array of processor modules, and they should be distributed among those processors so that the load is balanced and the utilization is high. We would like the inter-processor communications to be regular and, preferably, to require only simple connectivity, such as a nearest-neighbor mesh. The data should flow smoothly in and out of the array, which means that the time required to move data in and out should be comparable to the time needed for actually carrying out the computations.

In addition, we should consider the effects of errors in some modules of the array. We ask: Is it possible to provide some form of redundancy within our scheme, so that if an element of a given class of faults occurs during the computation, the effect will be masked and the array will be *fault-tolerant*?

Figure 1. A portion of the layout of a prototype integrated circuit. Linewidths are 3 micrometers in this silicon complementary metal-oxide-semiconductor (CMOS) technology.

Figure 2. A processor architecture to compute a singular-value decomposition of a $m \times n$ matrix using order n -fold parallelism. Each processor is composed of one or several of the multiply-and-add cells shown in Figure 1.

The rows of the matrix are input to the top of the array in staggered fashion. The processors in the top, unshaded row apply orthogonal transformations to the matrix so that its columns become orthogonal. The processors in the bottom, shaded row compute the column and inner product parameters needed to compute the next set of transformations. These are supplied to the pipelined unit at the bottom right, where the transformations are actually computed. The entire sequence repeats on the order of n times, until convergence is achieved.

Figure 3. An array that uses about $n^2/4$ processors to compute the decomposition in time of order n .

The data enter along one edge of the array and each 2×2 submatrix is mapped to a processor in the obvious way. The shaded processors diagonalize their submatrices using orthogonal transformations from both the left and the right. These transformations are sent along the corresponding row and column of processors and applied there as well. Finally, the matrix is permuted by exchanging elements along the diagonal links between each processor. This sequence of steps takes constant time independent of the size of the array, and is repeated on the order of n times, until convergence is achieved.

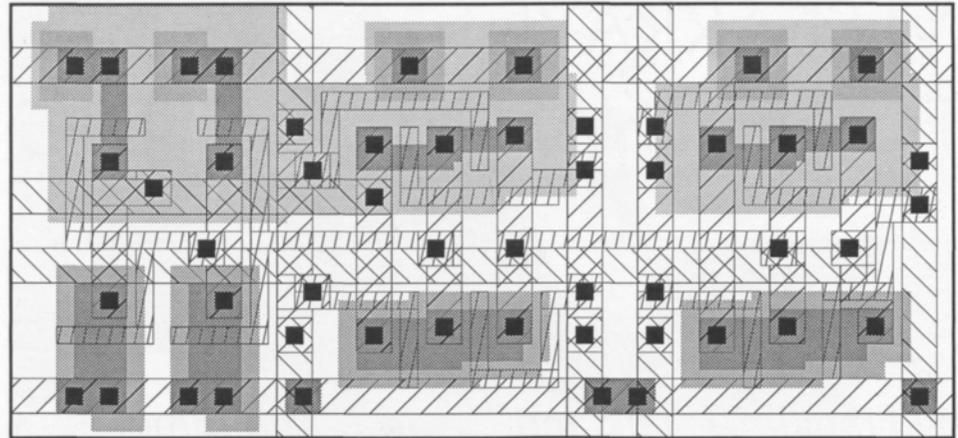


Figure 1

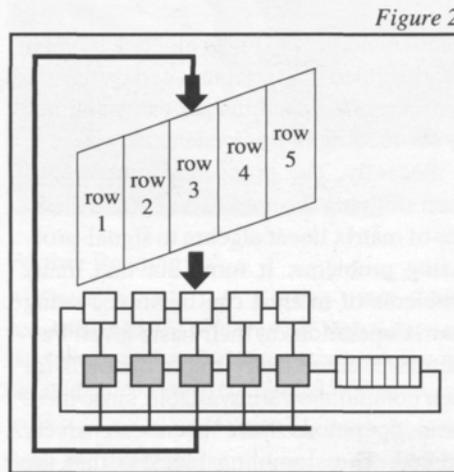


Figure 2

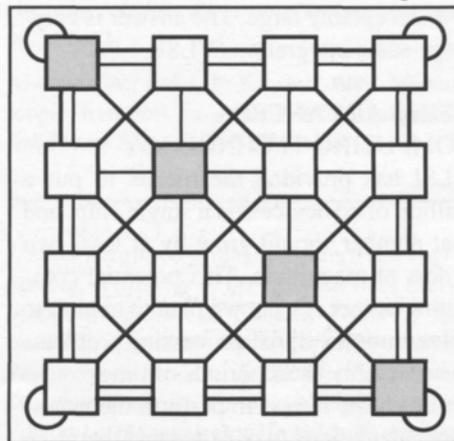


Figure 3

THE USEFULNESS OF PARALLEL PROCESSING

Many algorithms of interest, it turns out, have as their basic computation element a simple multiply-and-accumulate cell. The partial layout of such a cell is illustrated in Figure 1.

The significance of the use of basic cells in designing electronic devices is that these cells may be replicated in one or two dimensions along with some control logic, vastly simplifying the design process. In addition, there may be constraints on the operands—such as their occurrence within a given interval—that can be exploited, allowing the basic cell to be smaller, or the process faster, or the design more elegant.

A cursory glance at the literature shows thousands of different algorithms, but a closer look reveals that at their core, many solve the same few basic problems over and over again. These tasks include finding eigenvalues and eigenvectors, computing Fourier transforms, solving linear systems of equations, and multiplying matrices together. Parallel processing could greatly reduce the time required to obtain the solutions.

Here is an example. Often it is desired to 16

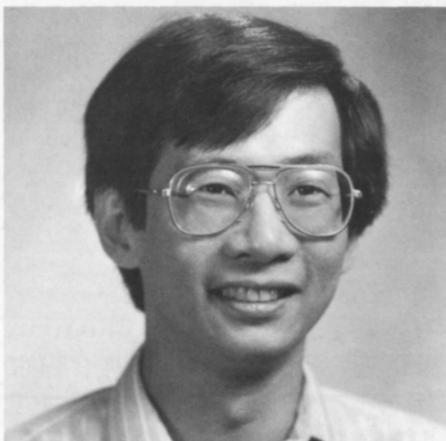
“The basic idea is to perform the necessary calculations in parallel, and therefore more quickly.”

find the eigenvalues of the autocorrelation matrix $A^T A$. But for numerical precision, it is better to find, instead, what are known as the *singular values* of A directly. This singular-value decomposition is also useful for related problems, such as finding the solutions to linear systems of equations. We have studied several solutions to this problem. The architectures include linear, triangular, and square arrays of mesh-connected processing elements.

Figure 2 shows a design for a one-dimensional array of processors for computing the singular values and vectors. This computation would normally take time proportional to n^3 on a single processor (where the matrix is of dimension $n \times n$). Here we utilize on the order of n processors to achieve an n -fold speedup. Since there are many applications in which $n \geq 1,000$, this speedup can be quite significant. Because there are n^2 elements in the matrix, the time required to transfer the data to or from a single memory system will also be proportional to n^2 . This satisfies our restriction that the data-transfer and computation times be well matched.

If the data can be transferred with n -fold parallelism—from multiple memory

Luk



Schimmel



banks, say, or from a phased array of radar antennae or sonar transducers—then the two-dimensional architecture in Figure 3 might be more appropriate. This design solves the problem in linear (order n) time. Of course, the tradeoff is that the processor area is now proportional to n^2 .

Architectures such as these are appropriate for VLSI implementation. The regular and repetitive structure is easy to design and understand, and it is powerful because of the enormous speedups that can be attained.

In this article we have only touched upon the potential of our area of research. Yet we hope we have conveyed a sense of its fascination and excitement.

Franklin T. Luk joined the Cornell computer science faculty in 1978 and later transferred to the School of Electrical Engineering, where he is an associate professor. He received the B.S. degree from the California Institute of Technology in 1972, and did his graduate work at Stanford University, earning the Ph.D. in 1978.

David E. Schimmel is a Ph.D. candidate in electrical engineering. He received the B.S. degree from Cornell in 1984.

INNOVATIONS IN COMPUTER ARCHITECTURE

for Real-Time Signal Processing and Other Applications

by H. C. Torng

Real-time signal processing and many other applications impose stringent requirements on computing systems. To meet these demands, processor designers relentlessly pursue performance enhancements.

Enhancement is measured by numerical comparison of the performance of the improved system with that of a reference system. For example, a recently announced microprocessor can operate at a rate of 7.5 million instructions per second (MIPS); if the rate were increased to 15 MIPS, we would say that its performance had been enhanced by a factor of two.

One way to achieve higher performance is to reduce the machine's cycle time—that is, to make it run faster. Advances in the technologies of silicon and gallium-arsenide integrated circuits have been making this possible; cycle times for processors of all ranges have been dropping. Physical limitations will make cycle-time reduction increasingly difficult, however.

Another approach, taken by CRAY, Floating Point Systems, and other high-end computer systems, is to incorporate multiple arithmetic and logic units into the processor. With the advances in integrated circuit technology, this type of arrange-

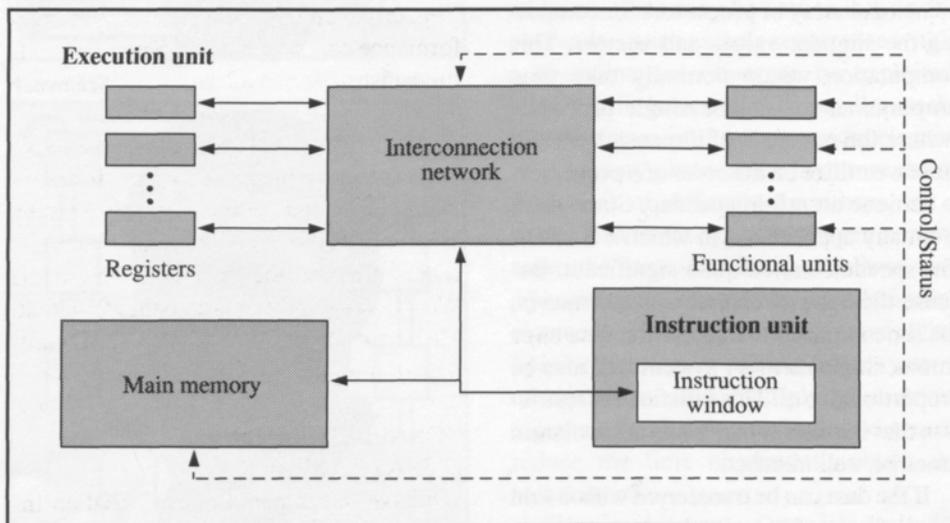
ment has been extended to newly announced reduced-instruction-set computers (RISC): Intel 80960 and Motorola 88000. These RISC processors have two arithmetic units: one for integer operations and one for floating-point operations. Furthermore, it is reported that six additional functional units can be added to the Motorola processor.

This new generation of microprocessors and the well established CRAY machines implement a *register-to-register*

(RR) architecture. They provide banks of fast registers to interact with functional units and the main memory. The configuration of these processors with multiple functional units (from now on simply called *processors*) is depicted in Figure 1.

But although these processors already yield impressive results, we have demonstrated that more can be achieved.

Figure 1. The general architecture of RISC processors with multiple functional units.



AN EXAMPLE OF PERFORMANCE ENHANCEMENT

In the expression:

$$\text{SUM} = A_0 + A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 \quad (1)$$

it is assumed that the eight operands, A_0 to A_7 , have been loaded into general-purpose registers, R0 to R7.

We use the instruction format adopted in CRAY and most RISC processors:

$$i: \text{OP}, S1, S2, D \quad (2)$$

where i is the instruction label, OP specifies the operation code of instruction i , Registers S1 and S2 provide the operands, and D receives the result.

The computation specified in (1) can be coded into the program sequence:

i_0	AD	R0	R1	R0	(3)
i_1	AD	R2	R3	R2	
i_2	AD	R0	R2	R0	
i_3	AD	R4	R5	R4	
i_4	AD	R6	R7	R6	
i_5	AD	R4	R6	R4	
i_6	AD	R0	R4	R0	

Let us consider that four functional units are available to perform additions, and that an addition takes only one cycle to complete. If the conventional mode of instruction issuance is used, it will issue one instruction at a time and take seven cycles to issue and complete this sequence. Only one of the four available functional units is busy at any time.

However, an examination of (3) reveals that i_0 can be issued immediately, as there is an arithmetic unit available to perform addition; Registers R0 and R1 are ready with operands; and Register R0 is free to accept the sum. The same conclusion can be reached about i_1 , i_3 , and i_4 . At the first clock cycle, four instructions— i_0 , i_1 , i_3 , and i_4 —can be issued concurrently.

On the other hand, i_2 presents some interesting problems. One of its source registers, R0, is the destination of a preceding instruction, i_0 ; in other words, i_2 uses

the result of i_0 as one of its operands. If i_0 is not completed, i_2 does not have a valid operand in R0 to operate on. Instruction i_2 should certainly be withheld until the completion of i_0 . The same dependency relationship exists between i_1 and i_2 .

There is another dependency which dictates that i_0 and i_2 not be executed concurrently: both deposit their results into the same sink, R0. If i_0 does this after i_2 , R0 will contain the result produced by i_0 to be used by instructions following i_2 in the instruction stream; this will most likely invalidate the result of the computation.

At the completion of the four instructions issued so far, i_2 and i_5 can be issued at the beginning of the second clock cycle. Similarly, i_7 can be issued at the beginning of the third cycle. Instead of seven cycles, the sequence can be completed in three.

AN OPPORTUNITY FOR ENHANCEMENT

Most, if not all, of the processors now in use issue instructions for execution according to their order of appearance in the instruction stream and at a rate AT MOST of one instruction per machine cycle. The processor performance or equivalent throughput is bounded by the clock rate. For example, if the clock of a processor runs at 20 MHz, there are 20 million cycles in one second, and at most 20 million instructions can be processed in one second. In many cycles, *no* instruction can be issued; the throughput, therefore, is much less than 20 MIPS.

This "at-most-one-per-cycle" mode of issuance leaves some of the functional

units starved for executable instructions. This offers an opportunity: processor performance can be greatly enhanced if multiple instructions can be issued at every machine cycle and out of sequence.

The example outlined in the box above illustrates this important point. It shows that with the conventional issuance mode, only one of four available functional units is busy at a time; the other three remain idle. We should—and can—do better than that. The sequence in the example can be completed in three rather than seven cycles.

CORNELL'S PATENTED DISPATCH STACK

We have developed and evaluated an instruction-dispatching mechanism, called

the *Dispatch Stack* (DS), that enhances the performance of these processors by factors ranging from 2.08 to 2.87, without raising their clock speed.*

The DS examines instruction segments and identifies those that are free of data dependencies. Each stack cell stores one instruction. When the instructions are completed, they are removed from the DS, new instructions are brought in, and entries in the stack are appropriately updated.

Accordingly, three operations have to be carried out during each machine cycle:

*This work has received support through the Joint Services Electronics Program (JSEP) at Cornell, and also from General Electric's Space and Defense Division and from IBM.

Table I. COMPARISON OF DYNAMIC INSTRUCTION-ISSUING SCHEMES

Approach	Issue order	Maximum instruction per cycle	Issue criteria		
			Functional unit	Source register	Destination register
Thornton's Scoreboard (CDC 6600)	sequential	one	busy / free	busy / free	free
Tomasulo's Reservation Stations, Common Data Bus (IBM 360/91)	sequential	one	busy / free	busy / free	busy / free
CRAY-1	sequential	one	free	free	free
Cornell's Dispatch Stack	nonsequential	one or more	free	free	free

fetch, issue, and update. The fetch operation loads new instructions, with appropriate coefficients attached, into the DS. The issue operation identifies instructions in the DS that are free of data dependencies. The update operation removes completed instructions and modifies the coefficients of the remaining instructions in the DS.

All these operations take time, and it is essential that the machine cycle not be lengthened to accommodate them. For RISC processors with a cycle time of 50 nanoseconds or longer, straightforward implementation of the various components will do. For computer systems with cycle times less than 10 nanoseconds, innovative designs with heavy expenditures of logic

circuits (or, equivalently, chip areas) must be used. Our recent work* has included the development of such designs.

A summary comparison between the DS and several existing schemes is given in Table I.

In order to establish the effectiveness of the DS scheme, we have performed extensive simulations. The benchmarks chosen consist of seven Livermore loops, which have large loop bodies, and three search-and-sort programs. As shown in

*Dwyer, H., and H. C. Torng. 1987. *A fast instruction dispatch unit for multiple and out-of-sequence issuances*. Technical report EE-CEG-87-15. Ithaca, NY: School of Electrical Engineering, Cornell University.

Table II. SPEEDUP OF THE DISPATCH STACK RELATIVE TO CRAY-1

Configuration	DS=16, fetch=4	DS=32, fetch=8
Uniprocessing	0.91	0.91
CRAY mode	1.00	1.00
1P	1.18	1.18
2P	2.08	2.09
4P	2.73	2.81
6P	2.73	2.85
8P	2.73	2.87
Full parallel	2.73	2.87

In the Configuration column, a figure before P indicates the maximum number of instructions that can be issued per machine cycle.

Table II, significant speedups were realized for various configurations. The results shown in the table are for two sizes of the DS—16 cells and 32 cells. Since a larger DS affords a bigger window with which one can examine a segment of the instructions, a somewhat larger speedup is expected and realized.

The number of instructions fetched from memory was another parameter we paid attention to. Each fetch produces four instructions with the 16-cell DS and eight instructions with the 32-cell DS. The best results were obtained under "full parallel" conditions, which means that all instructions free of data dependencies are issued. There was almost as much improvement, though, when at most four instructions per

“Our Dispatch Stack demonstrates what can be achieved. . . .”

cycle (4P in the table) were issued; this level realizes most of the concurrency that is available. But even at 2P we can achieve a speedup of 2.08. The benefit derived exclusively from out-of-sequence issuance (without concurrency) is indicated in 1P.

Elements of this dispatching mechanism have been implemented in an announced processor with gratifying results.

A complete description of the DS is available in our patent application, technical reports, and published articles.*

CONTINUING RESEARCH ON PERFORMANCE ENHANCEMENT

We are now investigating architectural issues: how to effectively deal with conditional branching and interrupts; how to construct compilers to maximize concurrencies that can be extracted by the DS; how to provide adequate data paths to sustain highly concurrent operations.

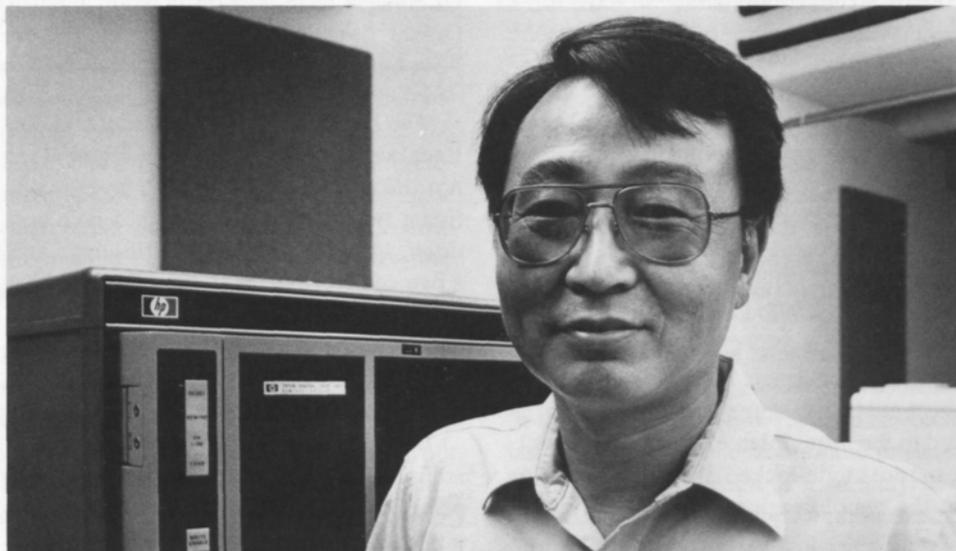
We are also working on identifying the most cost-effective processor configura-

tions for real-time signal processing tasks, and on developing programming aids for making the best use of these processors.

The implementation of concurrent processing has the capacity to greatly increase the efficiency of computing. Our Dispatch Stack demonstrates what can be achieved, and we expect adaptations of it to be incorporated into many processor configurations.

H. C. Torng, a professor of electrical engineering, joined the faculty in 1960 immediately after earning his Cornell Ph.D. He received his undergraduate degree from National Taiwan University in 1955.

Torng has spent sabbatical leaves at Bell Laboratories, and has served as a consultant to a number of industrial organizations. He was a distinguished visitor of the Computer Society of the Institute of Electrical and Electronics Engineers from 1983 to 1986, and is currently an editor of the IEEE Transactions on Computers.



*Acosta, R., J. Kjelstrup, and H. C. Torng. 1986. An instruction issuing approach to enhancing performance in multiple functional unit processors. *IEEE Transactions on Computers*

MEASURING THE UNIMAGINABLY FAST

Femtosecond Spectroscopy of Semiconductors and Large Molecules

by C. L. Tang

Photonic and electronic semiconductor devices operating in the subnanosecond (10^{-9} second) time domain were considered unimaginably fast not too long ago. Today there are subpicosecond (10^{-12} second) semiconductor devices. As such devices become faster and faster, the question that naturally arises is: What is the ultimate limiting speed of semiconductor devices?

Recently developed femtosecond lasers (1 femtosecond = 10^{-15} second) and related optical techniques help to answer this question—and many others as well. These systems, operating in the range of 10^{-15} to 10^{-13} second, can be used to study a wide variety of very fast physical and chemical processes; for example, molecular vibrations have been observed directly in the time domain for the first time with the help of the new technology.

FEMTOSECOND LASERS FROM NEAR-IR TO UV

Femtosecond lasers are now available in the wavelength range from the near-infrared to the ultraviolet. The most commonly used are mode-locked dye lasers operating in the visible region, around 620 to 630 nanometers.

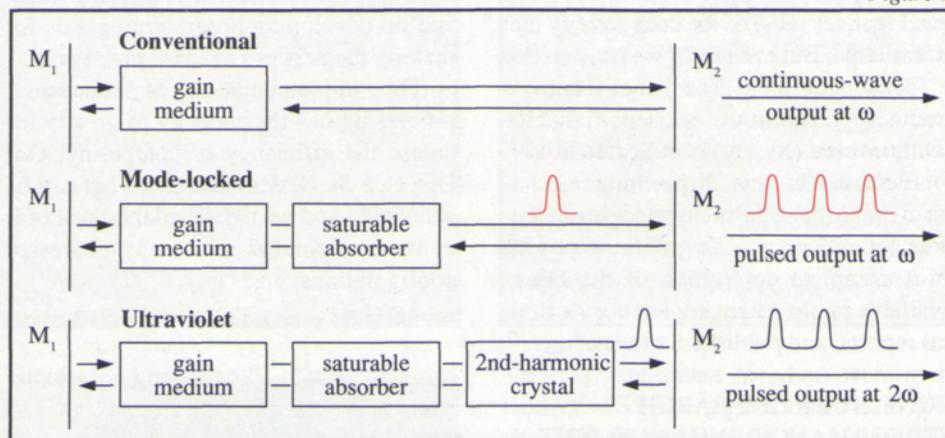


Figure 1

The basic idea of the femtosecond dye laser, shown schematically in Figure 1, is not difficult to understand. The conventional type of laser consists of a *gain medium*, which emits and amplifies light, and a pair of *laser-cavity mirrors* (M_1 and M_2) facing each other, which feed the light repeatedly back into the laser medium for amplification. The output is, generally, a continuous wave.

In the mode-locked dye laser there is, in addition to the gain medium, a nonlinear *saturable absorber*, which has the unusual nonlinear property that its optical loss is

Figure 1. Three types of dye lasers.

The new ultraviolet laser, shown at the bottom, has a nonlinear second-harmonic crystal. It has a power level comparable to that of visible dye lasers. Its pulsed output has a frequency (2ω) twice that of the conventional or mode-locked lasers.

In the diagrams, M_1 and M_2 are laser-cavity mirrors.

less for higher light intensity than for weaker light. As the emitted light, which is initially in the form of random noise spikes, circulates in the laser cavity, the highest

“... the question that naturally arises is:
What is the ultimate limiting speed
of semiconductor devices?”

spike gains at the expense of the others and eventually becomes the sole survivor. As this single high-intensity spike circulates in the cavity and impinges periodically on the output mirror (M_2) of the laser, the laser emits a periodic train of short pulses. This explains how the pulses are formed, but it does not explain why the pulses can be as short as, for example, 35 femtoseconds. This short pulse duration is a result of a delicate balance of the gain, nonlinear saturation, loss, and dispersion in all the various components in the cavity.

Typically, 35 femtoseconds at 10^8 pulses per second at 620–630 nanometers is what one can readily obtain for experimental purposes in the laboratory. It is possible to further compress the pulses external to the laser. In fact, pulses as short as 6 femtoseconds, corresponding to three optical cycles, have been reported by workers in the field. However, for such ultrashort pulses, the pulse repetition rate is often relatively low, down to a few thousand hertz. Since each pulse potentially can be used to obtain information, losing a factor of 10^4 to 10^5 may not always be beneficial. Whether or not to compress the pulse in order to improve time resolution

depends upon the kind of experiment one is trying to do. We usually opt for high pulse-repetition rate rather than for the shortest possible pulse duration.

Because of the easy availability of femtosecond dye lasers operating in the visible, most of the experiments done in the femtosecond time domain are in the visible or longer wavelength range. But recently we developed, for the first time in any laboratory, a femtosecond laser that operates in the ultraviolet. The scheme is shown in the bottom part of Figure 1. Incorporated into the laser is an additional *second-harmonic crystal* that doubles the frequency (or halves the wavelength) of the light. The output with this laser is, therefore, at 310–315 nanometers. We have achieved a pulse duration of 43 femtoseconds at the rate of 10^8 hertz—the shortest ultraviolet pulse ever generated.

The important thing is that the power level of the ultraviolet laser is comparable to the commonly used visible femtosecond laser because of the new nonlinear optical crystal, β -BaB₂O₄, which was grown in our laboratory. Thus, the available femtosecond laser sources have now been extended to the ultraviolet region. This

should enable new ultrafast physical and chemical processes to be studied.

MEASURING ULTRAFAST CARRIERS IN SEMICONDUCTORS

The ultimate speed of semiconductor devices depends upon the lifetime of the electrons in the conduction-band states. In gallium arsenide (GaAs) and related compounds—some of the most commonly used materials for such devices—the lifetimes of electrons are generally in the sub-picosecond time domain. Before the advent of the femtosecond lasers, there had been many theoretical studies and indirect measurements, but only femtosecond optical techniques have good enough time resolution to measure directly the lifetimes of the electron carriers in such compound semiconductors. The basic methods used are the so-called *pump-probe* and *optical correlation* techniques.

In the pump-probe technique, carriers are first excited from the valence band of the semiconductor to some excited conduction-band state by a femtosecond laser pulse. The transmission of a suitably delayed femtosecond pulse probes the states affected. If the carriers still occupy the

Figure 2. A typical transmission correlation trace of GaAs. The semiconductor has been exposed to two femtosecond pulses, the second following the first after a variable delay. Electrons have been excited to 0.5 eV above the conduction band edge.

The curve in black shows the autocorrelation of the femtosecond pulse used for the measurement. The points in color indicate the measured relaxation dynamics of the electrons. The factors of 10 and 100 indicate a change in scale to demonstrate the absence of noise in the data.

Figure 3. A transmission-correlation trace of malachite green, a triphenyl methane dye molecule, showing an oscillatory relaxation process corresponding to coherent vibrations of the molecules in the time domain.

The trace in 3b is an enlargement of the region of interest.

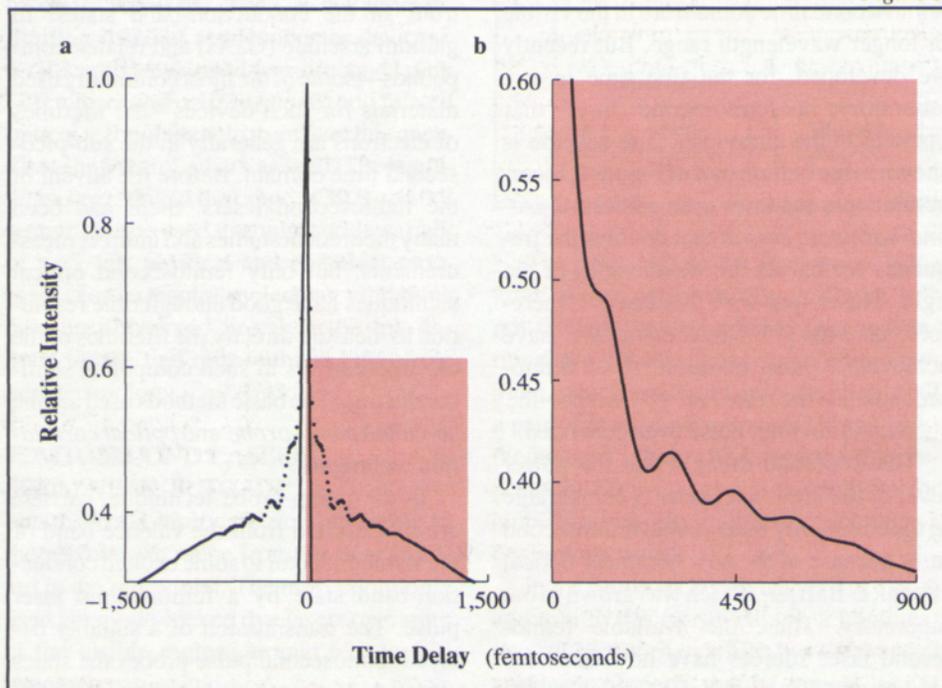


Figure 2

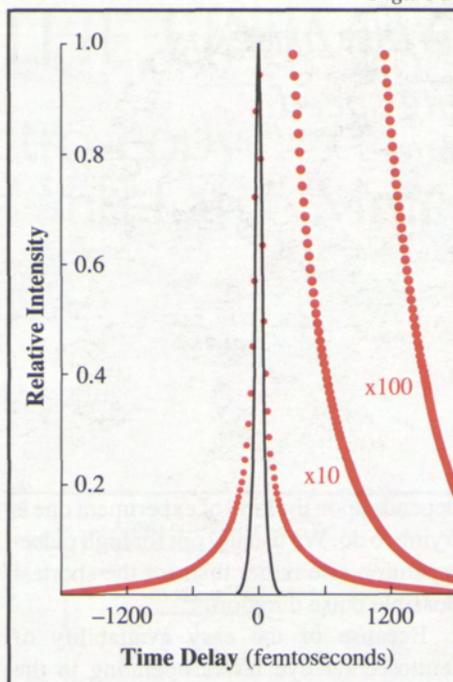


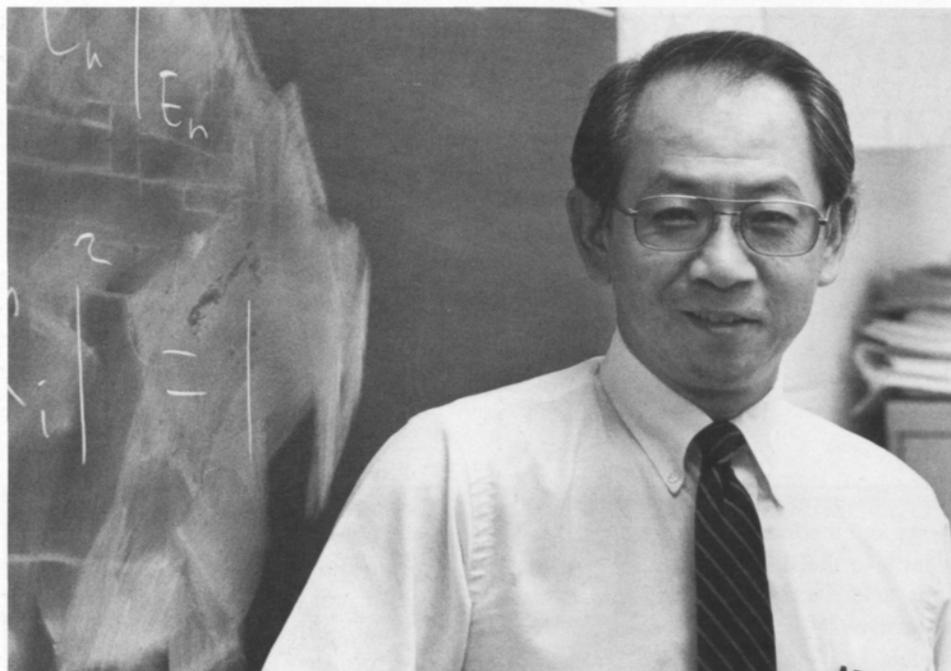
Figure 3

initially excited states, the transmission of the probe pulse through the sample is higher than it would be if the carriers had already left those states through various relaxation processes. Thus, by successively delaying the probe pulses, the lifetime of the carriers in the initially excited states can be measured.

In the optical correlation spectroscopic technique, the total transmission of two femtosecond pulses, with a suitable time delay between them, is measured. If the excitations due to the two pulses do not "see" each other, the transmissions or absorptions of the two pulses will be independent of each other. But if the excitations due to one pulse are still present when the second pulse arrives, then the total transmission is reduced because of an absorption-saturation effect; the transmissions of the two pulses are correlated. By measuring the transmission correlation of the two pulses, one can again measure the lifetime of the carriers. Figure 2 shows a typical transmission correlation curve.

Through such schemes, we have studied the ultrafast relaxation dynamics of hot (high-energy) carriers in a variety of semiconductors and structures such as quantum wells and superlattices.

The ultimate speed of electronic devices is limited by the time it takes the electrons to travel between two electrodes. For the greatest possible speed, semiconductor devices will have to be smaller than the mean free path of the electrons. Our studies indicate that in GaAs electrons with an initial velocity of, for example, 1.5×10^8 centimeters per second (or with a kinetic energy of about 0.5 eV) have a mean free path of only about 75 nanometers, which means that the size of the fastest electronic devices will have to be about 75 nanometers or smaller. We also concluded that about 65



C. L. Tang, the Spencer T. Olin Professor of Engineering at Cornell, has been a member of the electrical engineering faculty since 1964.

He holds the B.S.E.E. degree from the University of Washington, the M.S. from the California Institute of Technology, and the Ph.D. from Harvard University. He also studied at the Technical University in Aachen, Germany, and spent four years as a principal research scientist with the Raytheon Research Division.

Tang is a member of the National Academy of Engineering and a fellow of the Optical Society of America, the Institute of Electrical and Electronics Engineers, and the American Physical Society.

time domain. Such vibrations are usually inferred from measurements in the frequency domain.

WORKING IN THE ULTRAFAST: NEW METHODS, NEW POSSIBILITIES

The purpose of our research, which is part of the Joint Services Electronics Program (JSEP) at Cornell and is also partially supported by the National Science Foundation, is to develop new optical sources and techniques and apply them to specific materials and structures. For example, the femtosecond lasers and related techniques that I have described can be used to measure the lifetime of hot carriers in semiconductors—time constants that are of fundamental importance for understanding and designing all kinds of ultrafast photonic and electronic devices.

The sources and techniques we are developing are capable of measuring processes that are too fast for other available methods. They open up a promising region for exploration in science and technology.

percent of the initial excited carriers would be scattered out within the first 50 femtoseconds, which means that regardless of the type or design, such devices can have an ultimate speed on the order of 50 femtoseconds. Of course, the practical limit of the devices would probably be far from this ultimate limit.

MOLECULAR VIBRATIONS IN ORGANIC DYE MOLECULES

We have obtained a rather surprising result using the femtosecond optical transmission correlation spectroscopic technique in a study of large organic dye molecules. A damped sinusoidal type of relaxation curve, such as the one in Figure 3, was seen for a number of the molecules.

After extensive tests, we ascertained that the oscillations are due to the normal-mode vibrations of the molecules. When the molecules are suddenly excited from

the ground electronic state to an excited electronic state, the electronic charge distributions can change instantaneously, but the relative positions of the atoms cannot adjust as fast. As a consequence, the molecules are left in a nonequilibrium vibrational state and proceed to oscillate coherently. Because the relaxation time of the molecular coherent vibrations is long compared with the pump and probe pulse widths, the molecular vibrational motion is actually resolved as the molecules are probed by suitably delayed femtosecond pulses.

This type of oscillation is known as *quantum beats*. Recent Raman spectroscopic studies carried out at MIT and Brown University on the same molecules have confirmed our observations of quantum beats in the femtosecond time domain. This appears to be the first direct observation of coherent molecular vibrations in the

AREA VS. TIME: A TRADEOFF IN A VLSI COMPUTER

by Gianfranco Bilardi

Running time is the usual measure of performance in solving problems on a traditional computer. The faster the results are obtained, the more efficient the *algorithm* (or method of solution) is considered to be. But if a very-large-scale integrated (VLSI) circuit is used for the computation, an additional factor becomes important. A dedicated VLSI circuit contains a large number of processing elements, and performance depends not only on the algorithm, but also on the architecture of the circuit.

Designing the architecture together with the algorithm allows us to trade architectural complexity for algorithmic complexity—that is, area for time. To appraise the design, one needs measures for both. Because the processing elements (transistors) and the communications elements (wires) are fabricated in the same medium (the silicon chip), a natural measure of architectural complexity is *silicon area*. Reducing this area increases efficiency and, in addition, lowers the cost of fabrication.

This is a field in which part of my research group at Cornell is working. We are studying VLSI structures and their performance in a *complexity-theoretic* frame-

work. We apply algorithm design methodology and theories of computational complexity to the development of VLSI circuits, and we analyze the design mathematically by means of computational models.

It is important to characterize the *area-time complexity* of a problem—determining, for any achievable computation time, the minimum area of a VLSI circuit that can solve the problem within that time.

VLSI CIRCUITS FOR THE DISCRETE FOURIER TRANSFORM

A concrete example is the design of a VLSI circuit for the computation of the Discrete Fourier Transform (DFT), a fundamental operation in many areas of applied mathematics. The architecture, based on orthogonal trees, is illustrated in Figure 1 (in the box opposite) and the method of calculation is outlined. With a suitable implementation of the details, the design results in a circuit that has an area proportional to $n^2 \log^2 n$, where n is the length of the vector to be transformed. The time required to compute a single transform is proportional to $\log n$.

The question is: Can the area be de-

creased while maintaining the same computation time? The answer is yes, as I have shown in joint work with M. Sarrafzadeh at Northwestern University.*

The algorithm we adopt is based on a known property of the DFT and can be outlined as described in the box on page 28. The blocks in Figure 2 labeled column DFTs, row DFTs, and multipliers represent stages of the computation. Figure 3 shows the inner structure of the row DFTs block. Figure 4 illustrates the transposer, a set of wires that route the data to the appropriate place without performing any processing. In spite of its apparently accessory role, the transposer occupies most of the chip area. I shall have more to say on this point.

Once the details of the design are filled in, it turns out that the computation time is $T = O(\log n)$, as required by the orthogonal-trees algorithm of Figure 1. The area, though, is $A = O(n^2)$, smaller by a factor

*Bilardi, G., and M. Sarrafzadeh. 1987. Optimal VLSI circuits for the discrete Fourier transform. In *Advances in computing*, vol. 4, pp. 87–101. Greenwich, CT: JAI Press.

“... performance depends not only on the algorithm, but also on the architecture of the circuit.”

THE DESIGN OF A CIRCUIT FOR COMPUTING THE DISCRETE FOURIER TRANSFORM (DFT)

In a ring endowed with an n -th primitive root of unity ω , the DFT of a vector $(x_0, x_1, \dots, x_{n-1})$ of elements of the ring is the vector $(X_0, X_1, \dots, X_{n-1})$ defined by:

$$X_i = \sum_{j=0}^{n-1} x_j \omega^{-ij} \quad (i = 0, 1, \dots, n-1).$$

An interesting architecture suitable to the computation of the DFT by a direct application of the definition is that of $n \times n$ orthogonal trees (OT). Two families each of n fully balanced binary trees, respectively called the *row trees* and the *column trees*, are interconnected so that the j -th leaf of the i -th row tree coincides with the i -th leaf of the j -th column tree. An n -point DFT can be computed by an $n \times n$ OT with the following procedure (illustrated in Figure 1):

- (1) Input x_j at the root of the j -th column tree and, using the internal nodes of the tree as repeaters, broadcast it to all leaves.
- (2) Multiply x_j by ω^{-ij} at the leaf common to the j -th column tree and the i -th row tree.
- (3) Add $x_j \omega^{-ij}$ ($j=0, 1, \dots, n-1$) using adders located at the internal nodes of the i -th row tree, and output the result X_i at the root.

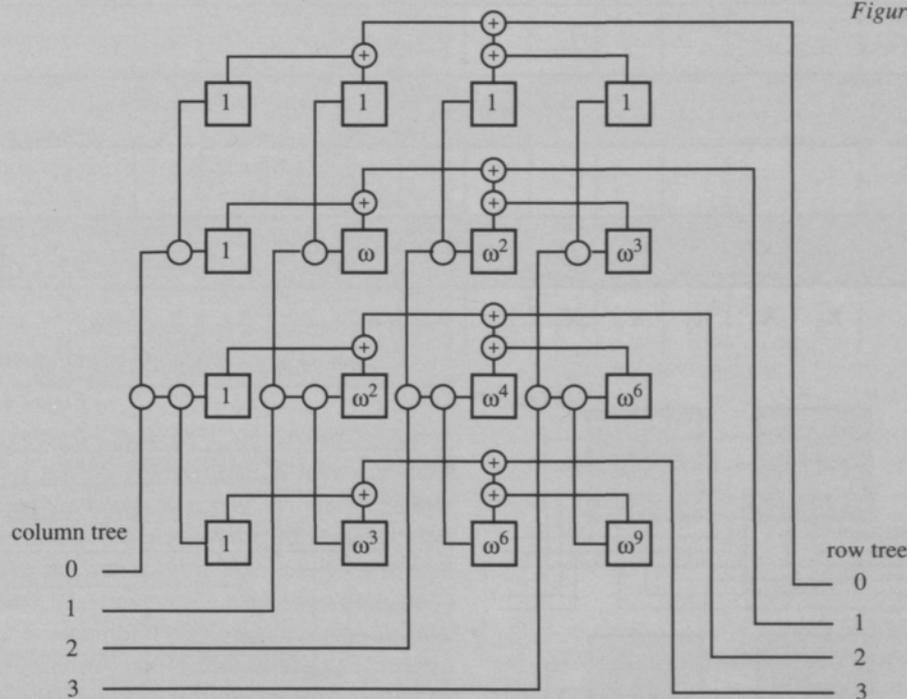


Figure 1

The designed circuit has an area $A = O(n^2 \log^2 n)$. A single transform is computed in time $T = O(\log n)$, during which data propagate up and down the trees.

Figure 1 shows a design of a VLSI circuit for computing the DFT. The architectural type is that of $n \times n$ orthogonal trees, with $n = 4$.

A REDUCED-AREA VLSI CIRCUIT FOR COMPUTING THE DISCRETE FOURIER TRANSFORM (DFT)



Figure 2

Figure 2 shows a high-level diagram for a circuit that was designed to implement an algorithm based on a known property of the Discrete Fourier Transform (DFT).

The algorithm is outlined as follows:

- (1) Let n factor as $n = pq$. Then the components of the vector to be transformed can be (conceptually) arranged into a $p \times q$ array, with the first q components in the first row, the next q components in the second row, and so on.
- (2) Replace each column of the array by its DFT.
- (3) Multiply the (h, k) component of the array by ω^{-hk} .
- (4) Replace each row of the array by its DFT.
- (5) Obtain the transformed vector by concatenating the columns of the resulting array.

In Figure 2 the *column DFTs* block implements stage (2), the *multipliers* block implements stage (3), and the *row DFTs* block implements stage (4). Some rearrangement of data between stages is performed by the two *transposer* blocks.

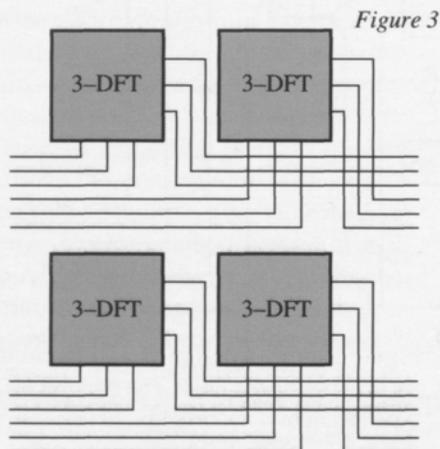


Figure 3

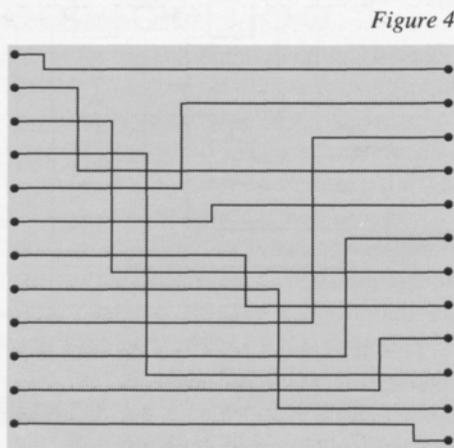


Figure 4

Figure 3 shows the inner structure of the *column DFTs* block (The structure of the *row DFTs* is similar.) The individual DFTs of the columns are carried out by orthogonal-tree architectures of the type illustrated in Figure 1.

Figure 4, representing the *transposer* block, shows how wires route the data. Although they do not have a processing function, transposers occupy most of the area of a silicon chip.

THE ARGUMENT FOR A LOWER LIMIT ON PERFORMANCE

For simplicity, we assume that the layout of a circuit C is a rectangle of base b and height h .

Associated with C is a protocol (chosen by the designer) that specifies, for each variable, a place and time for input or output. If C is swept from left to right by a straight line perpendicular to the base, there will be a position such that (approximately) $n/2$ input variables enter on either side of the line. Let us say that the number of variables output at the right of this line is no less than the number of those output at the left (the argument in the other case is similar). Thus, at least $n/2$ variables are input on the left side, and at least $n/2$ are output on the right side.

At this point we have to invoke a technical result stating that, given $n/2$ input components and $n/2$ output components of the Fourier transform, one can always choose from them $n/4$ input components and $n/4$ output components related by an invertible law (when all the remaining inputs are set to zero).

In our setup, the information on the

value of the $n/4$ inputs enters at the left of the straight line and, because of the invertibility of the relation, exits, encoded by the $n/4$ outputs, at the right of the same line. Clearly, this information must cross the line during the course of the computation. Let us call I the amount of information, measured in bits, needed to specify $n/4$ input elements. A technical argument omitted here shows that at least $\log n$ bits are needed to represent an element of a ring supporting an n -point DFT. Hence, $I \geq (n \log n)/4$.

To relate information to area and time, we observe that (1) transmission time cannot exceed the total computation time T and (2) transmission bandwidth is proportional to the number of wires across the section, which in turn is at most proportional to the width b of the section. We conclude that b is at least proportional to I/T . A similar argument applies to h . Then $A = bh$ is at least proportional to $(I/T)^2$.

Recalling the lower limit established for I , we find that A is at least proportional to $[(n \log n)/T]^2$, as claimed.

proportional to $\log^2 n$. This achieves our goal of reducing area without increasing the running time.

Conversely, our DFT design can be modified to trade time for area. For any computation time in the range $\log n \leq T \leq (n \log n)^{1/2}$, we can design a circuit that fits in an area $A = O[(n \log n)^2/T^2]$. The basic idea is to decrease the number of column (or row) DFT units, but have each unit process more than one column (or row). The design of the transposer becomes somewhat delicate, but everything can be made to work out with the stated performance.

LOWER LIMITS

ON AREA-TIME PERFORMANCE

Can the performance of the circuit represented in Figures 2–4 be improved upon? The answer is no in the following sense: Any VLSI circuit that computes the DFT of a vector of n elements occupies an area at least proportional to $(n \log n)^2/T^2$. This lower limit is a consequence of the bandwidth requirements posed by the information flow. The proof of the lower limit was given by C. D. Thompson in a 1980 Ph.D. thesis at Carnegie-Mellon University; the main ideas are sketched in the box above.

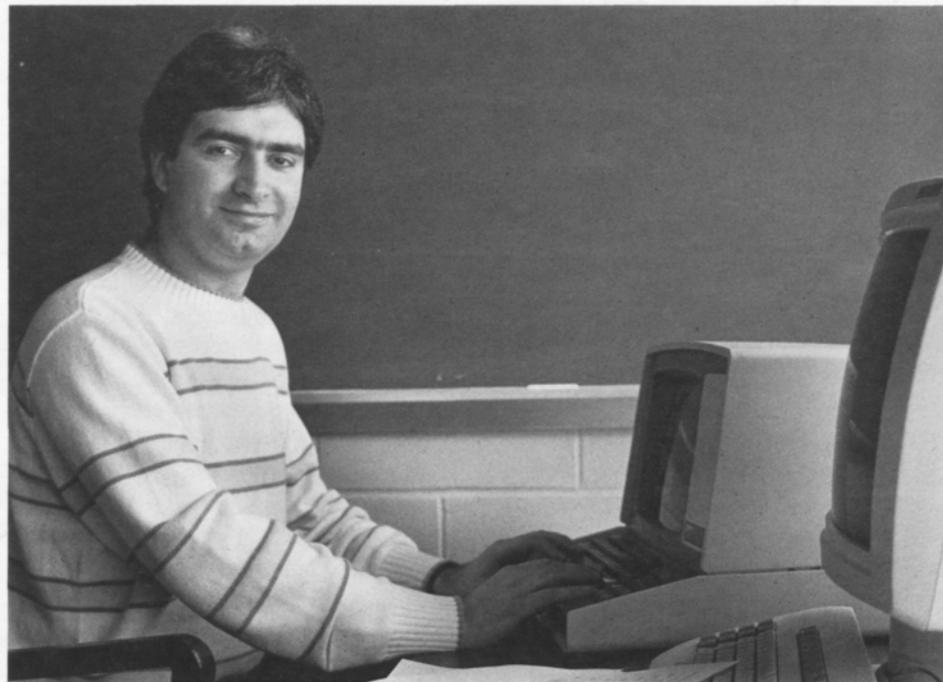
*“Can the performance
of [our circuit]
be improved upon?
The answer is no”*

In view of this result, we can say the DFT design we have described has an area-time performance optimal to within a factor that is independent of the input size n . The fact, perhaps surprising at first, that a substantial part of the area of the DFT circuit is taken up by the transposer, a mere router of data, is the manifestation of what the proof of the lower limit tells us: that performance is essentially constrained by the transfer of information between different regions of the circuit.

FURTHER WORK IN A GROWING RESEARCH AREA

VLSI complexity theory, which had its beginning only eight years ago, has developed in several directions. Algorithms, architectures, layout, and lower-bound techniques are among the tools and methods that have been incorporated.

We have actively participated in this exciting area of research by investigating questions of modeling (how should a VLSI structure be formally described within a computational model?), proposing circuit constructions for various fundamental problems such as sorting, Fourier transform, integer multiplication, and prefix



computation, and developing techniques to derive lower bounds for the area-time tradeoff. This research is supported by the Joint Services Electronics Program (JSEP) and the National Science Foundation.

Currently we are investigating digital filtering, an important special-purpose computation that is at the core of many signal-processing operations. The idea is that since input and output of a filter are infinite sequences (at least conceptually), the speed of the filter is not measured by the computation time, but by the data rate—the number of input samples processed per unit of time.

Perhaps the most interesting outcome of our work so far is that it shows that a complete characterization of the area-data rate tradeoff will be obtained only by combining ideas and techniques from different fields, such as computational com-

plexity, information theory, dynamical system theory, and numerical analysis.

Working in VLSI complexity theory is particularly challenging and rewarding because of the correlation of theory with real devices and the ultimate usefulness of the results.

Gianfranco Bilardi has been an assistant professor of computer science at Cornell since 1984.

He earned his undergraduate degree in 1978 at the University of Padova, Italy, and stayed on for a year to conduct research in statistical communications. He did his graduate work at the University of Illinois, receiving the M.S. degree in 1982 and the Ph.D. in 1985.

He is a member of the Institute of Electrical and Electronics Engineers and the Association for Computing Machinery.

ULTRAFAST SAMPLING WITH A SOLITON LASER

by Clifford R. Pollock

The speed of many compound semiconductor transistors is too fast to be measured by conventional electronic instrumentation. Extremely fast events occurring within semiconductor materials are also unmeasurable by conventional techniques. But in our laboratory we have devised a way to make such measurements.

Using ultrashort pulses in the infrared, we can optically probe the operation of devices and materials with resolution in the femtosecond (10^{-15} second) range. Such measurements enable circuit and device designers to characterize the speed and distortion of their creations, providing the necessary feedback for enhanced designs.

In this article I describe our ultrafast laser system and discuss how it will be applied to the study of fast electronic devices and materials.

MEASURING EVENTS WITH ULTRAFAST PULSES

In our technique, we make stroboscopic measurements of events using ultrashort pulses. The particular event being measured dictates the kind of pulse needed. Two basic conditions must be met: (1) the probe pulse must be shorter in temporal duration

than the process under investigation; and (2) the wavelength of the pulse must interact with the system.

The first condition is illustrated by an analogy with the timing of a race. Imagine trying to time a 100-meter dash with a stopwatch that records seconds, but not tenths or hundredths of a second. There would be no distinction, for example, between a contestant who ran in 10.2 seconds and one who ran in 10.7 seconds. The resolution of the stopwatch would not be good enough.

A similar picture appears when we try to measure physical processes with optical pulses. Suppose we try to determine the speed at which a transistor turns on. By using two successive pulses, one to start the transistor and the second to determine its state after some delay, it should be possible to determine the speed of the device. However, if the transistor can turn on in less time than the duration of the starting or probe pulse, the resolution is lost and the measurement will be imprecise.

How short must the probe pulse be? It depends on the system under measurement. Consider the transistors built here at Cornell by Professor Lester F. Eastman's group. These devices have switching times

of approximately 5 picoseconds (a picosecond is 10^{-12} second). Obtaining an accurate measurement of the switching process requires pulses of much shorter duration.

The second criterion for the probe pulse—that it must interact with the system—is fairly obvious. Returning to the track-meet analogy, we note that the starting signal is a gunshot, a signal the runners can hear; a radio wave, for instance, would not work because the runners simply could not sense it. To optically study the electronic motion in a device, we must use an incident photon with a suitable wavelength—one that will enable the photon to lift an electron into the conduction band or across an energy barrier, or to interact with the system in some other detectable manner.

OUR SOLITON LASER FOR ULTRASHORT PULSES

We have developed a source of ultrashort pulses in the infrared that meets the two criteria. It is based on our NaCl color-center laser*, which tunes across the 1.4-

*See Pollack, C. R. 1984. Tunable infrared lasers based on color centers. *Engineering: Cornell Quarterly* 19(1):12-17.

“The basis of the laser is the optical soliton, which is simply a wave that propagates without distortion.”

1.9-micrometer spectral region—a range that is ideal for studying narrow-bandgap semiconductors such as gallium indium arsenide (GaInAs). Figure 1 shows the tuning range for our laser.

When a substantial portion of this bandwidth is locked together, an extremely short pulse can be generated; the trick is to convince a large portion of the bandwidth to coherently lock together. We have succeeded in accomplishing this by using a nonlinear optical fiber to form what is called a *soliton laser*. This laser was first demonstrated by a Cornell graduate, Linn F. Mollenauer, at Bell Laboratories in 1984; ours is the second laboratory in the world to create such a laser.

The basis of the laser is the optical soliton, which is simply a wave that propagates without distortion. The definition covers all types of waves, ranging from water waves to plasma waves to optical pulses. Most materials display dispersion, in which different wavelengths travel at slightly different velocities. A pulse, which can be viewed as a superposition of a number of different wavelengths, generally distorts by spreading out in time and space when traveling in a dispersive medium. Solitons occur when a special nonlinearity exists in a system that counteracts the dispersion. In glass optical fibers, this nonlinear effect is called *self phase modulation*.

Self phase modulation arises because the index of refraction of the glass fiber increases slightly in the presence of intense optical fields. This modulated index leads to phase shifts and new frequencies, as illustrated in Figure 2. At low power levels, where the self-phase-modulation effect is negligible, the dispersion of the fiber simply causes the pulse to spread out in time and space. However, as the optical power is

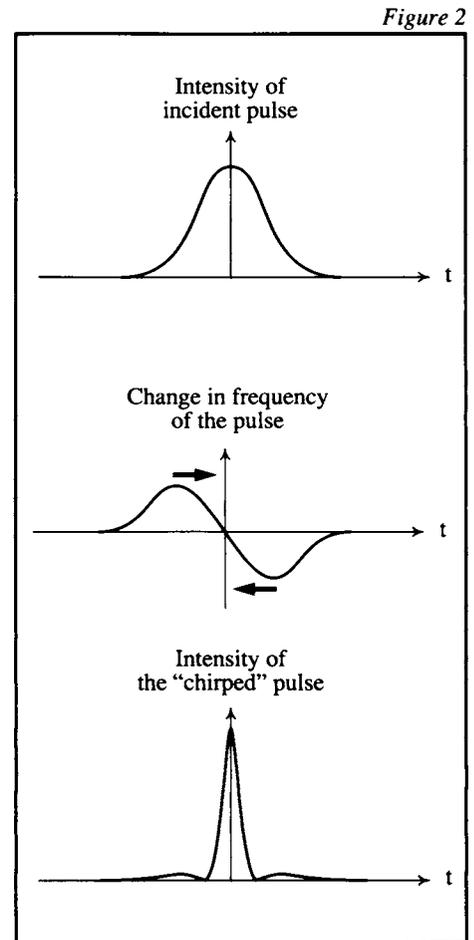
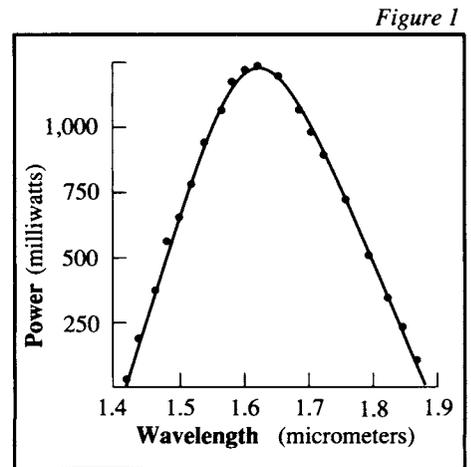


Figure 1. The tuning range for the NaCl color-center laser.

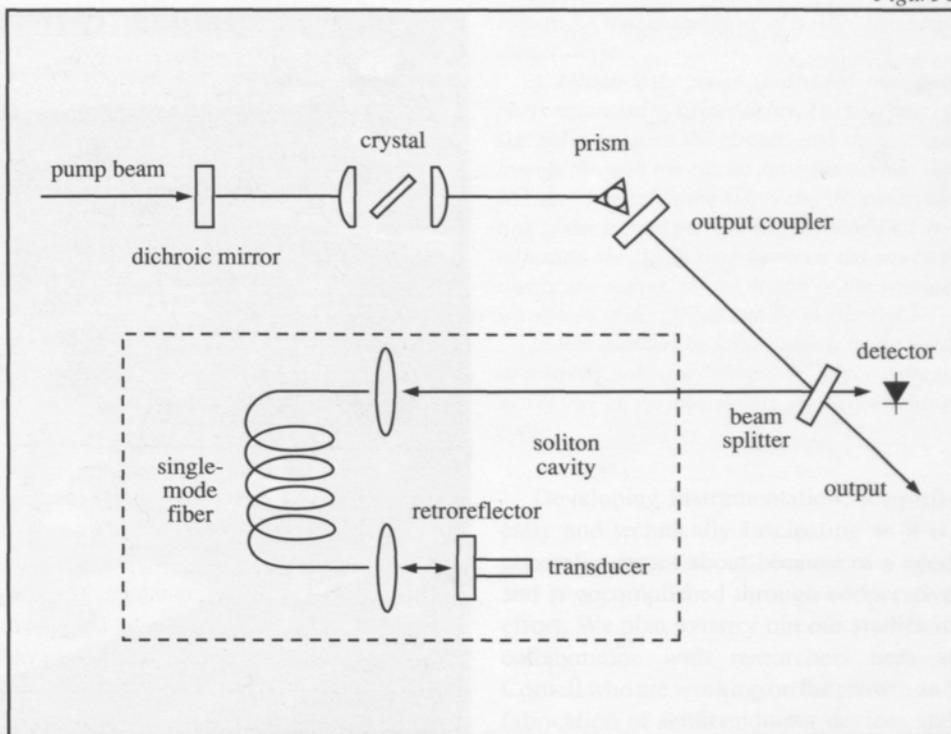
Figure 2. Phase shifts and new frequencies that occur when an intense laser pulse propagates in a glass fiber. The cause is a change in the refractive index of the glass.

The top sketch illustrates the time-varying intensity profile of the incident laser pulse. The index of refraction of the fiber is maximum at the peak of the pulse. The leading edge of the pulse, seeing an increasing index of refraction, is frequency-downshifted by self phase modulation, while the trailing edge is frequency-upshifted.

The middle trace shows the frequency shift of the pulse. The resulting pulse is "chirped": the optical frequency of the pulse increases from the front to the end. In glass fibers at wavelengths longer than 1.3 micrometers, dispersion causes the lower-frequency light, which is at the leading edge of the pulse, to travel more slowly than the higher-frequency light, which is at the back of the pulse. As the chirped pulse travels down the fiber, the leading and trailing edges compress toward the middle, forming a temporally shortened pulse. This is shown in the bottom trace.

Figure 3. The soliton laser, which is a color-center laser coupled to an optical fiber. The laser consists of a color-center crystal between two lenses; a prism; and two mirrors. A portion of the output is fed into the soliton cavity, which is simply a short length (0.3 meter) of optical fiber.

When the intense pulse enters the fiber, it experiences a self phase modulation and is compressed. This compressed pulse is reflected back into the laser, where it is amplified and regenerated. This process is repeated every time the pulse makes a round trip in the cavity, and the result is the formation of extremely short optical pulses. When the pulse width reaches what is called the $N=2$ soliton in the fiber, the returning pulse is exactly the same as the launched pulse, and no further pulse compression occurs. At this point we have a soliton laser.



increased to a certain level, the dispersive pulse-spreading is exactly compensated by a pulse-compression effect of the fiber (see Figure 2), and the pulse displays no distortion as it propagates. This is the regime of the soliton. At even higher powers, actual pulse compression can be observed. A diagram of our laser is shown in Figure 3.

The pulses from the soliton laser are truly impressive. Our soliton laser has generated pulses as short as 70 femtoseconds; Figure 4 shows an example of the output. In contrast to current ultrafast dye-laser systems, the central wavelength of the soliton laser is tunable, allowing the operator to adjust the wavelength of the pulse for optimum interaction with the system of interest.

In making measurements with the soliton laser, one pulse is generally used to

Figure 4. An autocorrelation trace of the output of the soliton laser. The pulse time was 80 femtoseconds, the central wavelength was 1.52 micrometers, and the peak power was several kilowatts.

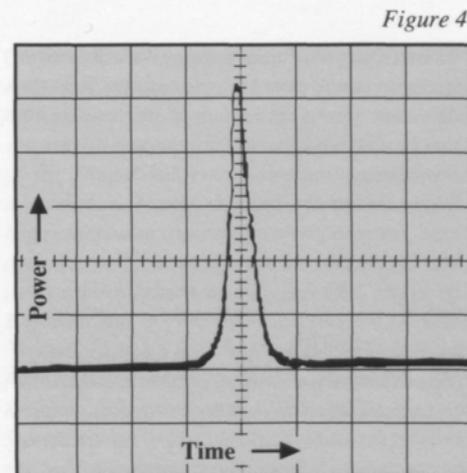


Figure 4

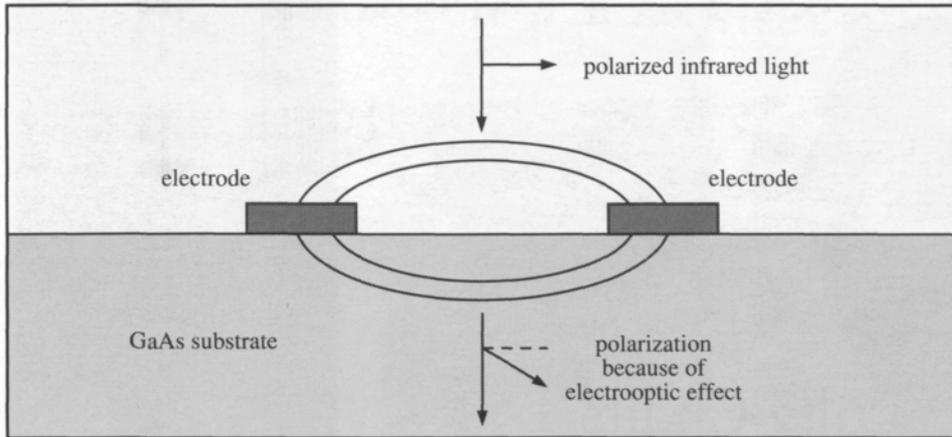


In his laboratory, Pollock shows the equipment he uses to probe extremely fast events that take place during the operation of semiconductor devices. The basis is a color-center laser that is formed into a soliton laser beam.

The beam (not visible because it is in the infrared) travels from the lower right corner of the photograph to a partially reflecting mirror (off to the left) that divides the beam into two pulses—one to excite the sample and one to probe it. The large spools in the foreground hold a kilometer of the optical fiber used to form the soliton laser. The long rectangular component just in front of Pollock is a laser that pumps the color-center laser.



Figure 5



both initiate and observe an effect. The pulse is split into two parts by using a partially reflecting mirror and a variable path arm. The first pulse, called the *pump pulse*, excites or starts the system; the second, the *probe pulse*, samples the system after a fixed delay. By systematically adjusting the relative path difference between the two pulses, the evolution of the probed system can be mapped out.

Figure 5 shows a schematic diagram of the variable delay optics. The two pulses are recombined after one has traveled a longer path; this creates the delay. By varying the path length, the time difference can be adjusted. A path difference of 30 centimeters will cause a 1-nanosecond (10^{-9} second) delay in pulse time. For relaxation rates in the subpicosecond range, a thousand times shorter, path differences on the order of millimeters are usually used.

THE USEFULNESS OF OUR LASER

We are planning to use these soliton laser pulses in several ways. One is for the measurement of the relaxation mechanisms of hot electrons in narrow-bandgap semiconductors. A good description of this

kind of work is given in C. L. Tang's article in this issue of the *Quarterly*. We plan to initiate similar studies in GaInAs.

Another planned use is for determining the speed of discrete devices once they have been built. Many microwave transistors are already so fast that their speeds cannot be directly observed with conventional electronic circuitry. This causes problems because the designer cannot observe the operation of a circuit to see whether there is excess distortion, or whether the speed of the device is sufficient. Designers usually rely on indirect measurements for such information. But now, with ultrafast optical pulses, we can directly observe the voltage waveform in compound semiconductor devices. Compound semiconductors are electrooptic, meaning that the index of refraction can be changed slightly by applying an electric field, and such a change can be monitored by observing the polarization of a transmitted beam, as described in the Figure 5 caption. With our soliton laser, it will be possible to resolve switching speeds down to 100 femtoseconds, which is a good deal faster than present semiconductor devices can operate.

Figure 5. Optical sampling of a III-V semiconductor device.

A soliton-laser pulse is divided into two parts separated by a fixed delay. The first part of the pulse triggers the circuit, and the second travels through the circuit substrate. When the voltage changes in the substrate, the polarization of the second pulse is slightly modified. By adjusting the delay time between the starting and probe pulses, the evolution of the voltage waveform of the circuit can be monitored.

In this manner the laser pulse is being used as a strobe, taking a "snapshot" of the voltage waveform at various points in the switching cycle.

Developing instrumentation, scientifically and technically fascinating as it is, generally comes about because of a need and is accomplished through cooperative effort. We plan to carry out our studies in collaboration with researchers here at Cornell who are working on the growth and fabrication of semiconductor devices and materials.

Clifford R. Pollock, an associate professor of electrical engineering at Cornell, has received recognition for both teaching and research since he joined the faculty in 1983. He was one of the first Presidential Young Investigators named by the National Science Foundation and has research support under that program. This spring he was chosen for the annual Excellence in Teaching Award at the Cornell College of Engineering.

Pollock holds B.S., M.S., and Ph.D. degrees from Rice University. Before coming to Cornell, he spent two years at the National Bureau of Standards on a postdoctoral fellowship from the National Research Council.



Five Appointed to Faculty Chairs

The appointments of five engineering faculty members to chaired professorships were announced at separate receptions at the recipients' schools or departments on the afternoon of September 9. The appointments, approved by the university board of trustees the previous day, had been kept as a surprise to the honorees until the announcements were made.

■ *Toby Berger*, named the J. Preston Levis Professor of Engineering, joined the faculty of the School of Electrical Engineering in 1968. He served as acting director of the school in 1987–88.

Berger was recognized for outstanding contributions in both teaching and research. Regarded as one of the world's leading authorities on information and communication theory, he is a recipient of the Frederick E. Terman Award of the American Society for Engineering Education. His publications include a widely used text.

Berger holds the B.S. degree from Yale University and the M.S. and Ph.D. from Harvard University. He was a Guggenheim fellow in 1976, a Japan Society for the Promotion of Science fellow in 1980, and a

fellow of the People's Republic of China Ministry of Education in 1981.

He is a fellow of the Institute of Electrical and Electronics Engineers and is currently editor-in-chief of the *IEEE Transactions on Information Theory*.

At Cornell he is also associated with the Center for Applied Mathematics and the graduate Field of Statistics.

■ *Edward J. Kramer* is the first Samuel B. Eckert Professor of Materials Science and Engineering. A Cornell B.Ch.E. degree graduate, he received the Ph.D. from Carnegie-Mellon University in 1966 and spent a year as a NATO postdoctoral fellow at Oxford University before joining the Cornell faculty in 1967.

A specialist in superconductivity and high-polymer physics, Kramer has pioneered in the study of microscopic aspects of fracture and diffusion in polymers—work that has led to new methods for improving the toughness and strength of these materials. He has held visiting professorships at the Akademie der Wissenschaften in Göttingen, West Germany, and at the Ecole Polytechnique Fédérale de Lausanne in Switzerland. In 1985 he was co-recipient

of the American Physical Society's High Polymer Physics Prize, generally considered the world's most prestigious award in polymer physics. In 1987–88 he held a Guggenheim fellowship and received a U.S. Senior Scientist Award from the Alexander von Humboldt Foundation of West Germany.

He is a fellow of the American Physical Society. At Cornell he is active in the Materials Science Center.

■ *John Silcox* was named the first David E. Burr Professor of Engineering. He was cited for outstanding accomplishments in all three majors areas of faculty activity—teaching, research, and administration.

He served twice as director of the School of Applied and Engineering Physics. A specialist in electron microscopy and spectroscopy, he was a principal developer of the technique of energy-loss spectroscopy. He has played key roles in two of Cornell's national centers, the Materials Science Center and the National Nanofabrication Facility. In 1987 he received the college's Excellence in Teaching Award.

Silcox was educated in England, earning the B.Sc. degree from Bristol Univer-

Kramer



Silcox



Todd



White



sity and the Ph.D. from Cambridge University. He came to Cornell in 1961. He has spent sabbatical leaves as a Guggenheim fellow in France and England, at Bell Laboratories, and at Arizona State University.

He is a past president of the Electron Microscopy Society of America and a fellow of the American Physical Society. He serves on the Solid State Sciences Committee of the National Academy of Sciences, and the Materials Advisory Committee of the National Science Foundation.

■ *Michael J. Todd*, who was appointed the Leon C. Welch Professor of Engineering, is a member of the School of Operations Research and Industrial Engineering and the director of the Center for Applied Mathematics.

He also received an important professional honor this summer: the George B. Dantzig Prize, which is awarded every three years by the Society for Industrial and Applied Mathematics and the Mathematical Programming Society. For the Dantzig, Todd was cited for his research on optimization methods, particularly linear programming and techniques for computing equilibria in complex systems. His work

has found application not only in engineering, but in economics, for problems such as the effects of tariffs, quotas, and export subsidies on trade balances, and the impact on revenues of changes in the tax code.

Todd earned the B.A. degree at Cambridge University, England, and the Ph.D. at Yale University. Before joining the Cornell faculty in 1973, he taught at the University of Ottawa for two years.

He received a Sloan Foundation research grant in 1980 and a Guggenheim fellowship the following year. He is editor-in-chief of *Mathematical Programming*.

■ *Richard N. White*, who has been named the first James A. Friend Family Professor of Engineering, has earned an international reputation in structural engineering research and has served the college and the School of Civil and Environmental Engineering as educator and administrator. He has been director of his school and is now the college's associate dean for undergraduate programs.

He joined the Cornell faculty in 1961 after earning three degrees at the University of Wisconsin. He also worked for a consulting engineering firm in Madison

and served in the U.S. Army Corps of Engineers. He is a registered professional engineer in the State of New York.

White has conducted research in structural concrete, steel, and timber, and he is a co-author of five books. His specialties include the modeling of structures; frames and concrete structures under severe loading; concrete containment structures for nuclear reactors; concrete structures under seismic loading; connections in tubular steel structures; and shell structures.

He has spent leaves at Gulf General Atomic and at the University of California at Berkeley, and he has traveled to many parts of the world as an educational and professional consultant. He serves on many national and international professional committees.

White is a fellow of the American Concrete Institute and the American Society of Civil Engineers. He was awarded the Collingwood Prize of the American Society of Civil Engineers and has twice received the Professor of the Year award from the national honorary society Chi Epsilon.

At the college White was chosen for the 1965 Excellence in Teaching Award.

THE ENDOWED CHAIRS

The five endowed chairs to which Cornell engineering professors were recently appointed (see the story on the preceding pages) commemorate outstanding Cornell alumni in mechanical engineering.

• **J. Preston Levis '06** spent his career in the glass industry, ultimately becoming president and chairman of the board of Owens-Illinois. He was one of the first members of the Cornell University Council, and was a trustee for eleven years.

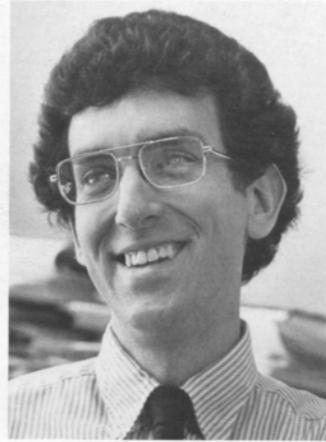
• **Samuel B. Eckert '08** was executive vice president of the Sun Oil Company and director of the Sun Shipbuilding and Dry Dock Company. His legacy will endow up to three engineering professorships; the one announced this year is the first.

• **David E. Burr '03** served as an officer in the Corps of Engineers and in the Army Reserves. He was president of a building construction firm and later, with his brother, organized the Burr Foundry and Machine Company in Keene, New Hampshire.

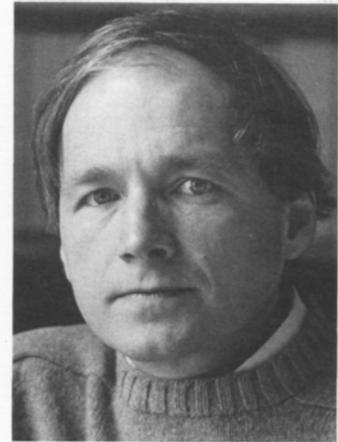
• **Leon C. Welch '06** was vice president of the Standard Oil Company of Illinois. He was active in the Cornell University Council.

• **James A. Friend '16** was chairman of Nordberg Manufacturing Company (later renamed Rexnord, Inc.) in Madison, Wisconsin. The professorship is named for the Friend family; at least seven other members are Cornell graduates.

Craighead



Isacks



Directors Named in Centers and Schools

■ *Harold G. Craighead*, currently a technical manager at Bell Communications Research, has been named director of Cornell's National Nanofabrication Facility (NNF) and professor of applied and engineering physics.

The appointment, effective January 1, was announced by Joseph Ballantyne, vice president for research and advanced studies.

The current NNF director, Edward D. Wolf, is resigning that position but will continue as a professor of electrical engineering and a user of the facility. Wolf came to Cornell in 1978 as director of the newly established center, then called the National Research and Resource Facility for Submicron Structures. Previously he had been at Hughes Research Laboratories.

In commenting on the appointment, Ballantyne said that Craighead will be "very effective in collaborating with a wide range of university, industry, and government users." Craighead cited the NNF as "a unique and successful center for research in the exciting and important area of ultra-small dimensions," and said he is looking

forward to continuing the facility's "extraordinary record of progress."

The NNF provides Cornell and visiting scientists with facilities for fabricating ultrasmall devices for experiments in physics and biology and for future generations of computers. Housed in special clean space in Knight Laboratory, the NNF has some thirty machines for building, testing, and observing small structures, and an expert support staff of twenty-five. Some sixty Cornell professors from fourteen departments conduct research at the facility.

Craighead holds B.S., M.S., and Ph.D. degrees in physics from the University of Maryland. He joined Bell Laboratories in 1979, and after creation of Bell Communications Research in 1984, became district manager in the Solid State Science and Technology Laboratory.

His research has included studies of the optical properties of gallium arsenide semiconductors, high-energy electron-beam lithography, compound semiconductor processing, electron microscopy, and optical properties of thin films.

Meyburg



Buhrman



Blakely



Karig



■ *Bryan L. Isacks*, the William and Katherine Snee Professor of Geological Sciences, has begun a three-year term as director of the Institute for the Study of the Continents (INSTOC).

INSTOC coordinates research on the structure of the continental crust. It includes the Cornell Program for the Study of the Continents (COPSTOC), for industrial associates; the Consortium for Continental Reflection Profiling (COCORP), for which Cornell is the operating institution; the Cornell Andes Project, a multidisciplinary study of continents and mountain-building; and other projects involving individual principal investigators.

Currently, ten faculty members, about thirty-five graduate students, and thirteen staff scientists conduct research under INSTOC sponsorship. The plans are to broaden and strengthen the activities, especially in international cooperative programs using both the seismic reflection profiling technique and satellite imagery to provide three-dimensional images of continental crust.

Isacks's predecessor as INSTOC director was Jack E. Oliver, the Irving Porter Church Professor in Engineering.

■ The School of Civil and Environmental Engineering has been reorganized and *Arnim Meyburg* has been named director. The school no longer has constituent departments and the college now has no schools with multiple departments.

Meyburg succeeds Peter Gergely, who was serving as both director of the school and chairman of the structural engineering department. Christine Shoemaker has just completed a term as chairman of the environmental engineering department.

Meyburg, a specialist in transportation engineering and planning, earned his doctorate at Northwestern University and came to Cornell in 1969. He served as chairman of the environmental engineering department from 1980 to 1985.

■ The School of Applied and Engineering Physics also has a new director, *Robert A. Buhrman*, who began his five-year term on July 1. He succeeds Watt W. Webb.

Buhrman joined the faculty in 1973 after receiving his Cornell Ph.D. A specialist in superconducting devices and sub-micron lithography, he has served as associate director of what is now the National Nanofabrication Facility at Cornell.

■ *Jack M. Blakely* was appointed director of the Department of Materials Science and Engineering. He succeeds Arthur L. Ruoff, the Class of 1912 Professor of Engineering, who served ten years as director.

A specialist in surface science and catalysis, Blakely joined the Cornell faculty in 1963 after completing Ph.D. studies at the University of Glasgow and serving as a research fellow at Harvard University. He is a fellow of the American Physical Society and the Institute of Physics (United Kingdom).

■ *Daniel E. Karig* has been appointed to the new position of associate chairman of the Department of Geological Sciences.

A Ph.D. from the Scripps Institute of Oceanography, he has been at Cornell since 1973. His specialties are marine geology and geophysics, structural geology of orogenic belts, marginal basins, and geomechanics.

He is a fellow of the Geological Society of America and an honorary foreign fellow of the Geological Society of London. He received the Edmond C. van Diest Medal of the Colorado School of Mines, where he studied as an undergraduate.

College Welcomes New Faculty Members

During 1988, newcomers joined the faculties in nine schools or departments and in the recently established Writing Program in Engineering.

■ New to the School of Applied and Engineering Physics is Assistant Professor *Frank Wise*, who recently completed a doctorate in applied physics at Cornell. His specialty is ultrafast transient phenomena in condensed matter. His previous degrees are the B.S. from Princeton University and the M.S. in electrical engineering from the University of California at Berkeley.

■ *Daniel A. Hammer* became an assistant professor in the School of Chemical Engineering in January. His degrees are the B.S. from Princeton University, and the M.S. and Ph.D. from the University of Pennsylvania. His research is concerned with fundamental biochemical and biophysical interactions between cells and their environment.

■ *Gregory G. Deierlein*, a 1981 Cornell graduate, joined the faculty of the School of Civil and Environmental Engineering as an assistant professor. A specialist in

structural engineering, he holds an M.S. degree from the University of California at Berkeley and a Ph.D. from the University of Texas at Austin. He has been a structural engineer with Robertson, Fowler and Associates of New York City.

■ A new member of the Department of Computer Science is Assistant Professor *Daniel P. Huttenlocher*. His degrees are the B.S. from the University of Michigan and the M.Sc. and Ph.D. from the Massachusetts Institute of Technology. He has served as a consultant, researcher, or visiting scientist at several industrial research laboratories. His research interests are computer vision, speech recognition, computational geometry, and artificial intelligence.

■ The School of Electrical Engineering gained four assistant professors: *Richard C. Compton*, *Max W. Hauser*, *Miriam E. Leeser*, and *Niels F. Otani*. Also, *John C. Belina*, who had been serving as an assistant dean and the director of admissions and advising at the college, became assistant director for instruction and a lecturer at the electrical engineering school.

Compton, a specialist in infrared, millimeter, and microwave engineering, received his doctorate from the California Institute of Technology in 1987 and joined the Cornell faculty early in 1988. He received the B.Sc. degree with honors from the University of Sydney; as an undergraduate, he won the Sydney University Medal and an award from the Australian Institute of Physics. Also, he was a Fulbright Scholar and a Sydney University Travelling Scholar. *Compton's* experience includes a year of research in Australia before he began graduate study, and consulting for the Hughes Aircraft Company and TRW.

Hauser, a specialist in integrated circuits, joined the faculty this fall. He received his undergraduate degree from the University of California at Berkeley and was named the outstanding electrical engineering student in the United States by the honor society Eta Kappa Nu. After earning the S.M. degree at the Massachusetts Institute of Technology, he returned to Berkeley, where he recently completed his doctorate. *Hauser* held a Hertz Foundation fellowship at Berkeley and now holds an American Electronics Association devel-

opment fellowship. He has worked as an engineer for a number of electronics firms, most recently North American Philips.

Leeser, who joined the faculty this fall, studied at Cornell for a 1980 B.S. degree in electrical engineering and did her graduate work at Cambridge University, England, where she earned the Ph.D. in 1988. While at Cambridge, she served as an undergraduate tutor in computer science. Her research area is the application of mathematical theorem-proving techniques to hardware verification.

Otani, a specialist in computer simulation of space and fusion plasmas, became an assistant professor in January. He graduated from the University of Chicago in 1977 as a Phi Beta Kappa physics major, and he received the Ph.D. in physics from the University of California at Berkeley in 1986. He spent a year in postdoctoral research at the Courant Institute of Mathematical Sciences, New York University.

Belina received B.S. and M.Eng. degrees in electrical engineering at Cornell in 1974 and 1975 and has been a doctoral student and lecturer at the school.

■ *Yogesh Kamar Vohra*, formerly a senior research associate in the Department of Materials Science and Engineering, was appointed assistant professor this fall. He received B.S. and M.S. degrees from Delhi University, India, in 1972 and 1974, and the Ph.D. from Bombay University in 1979. His research is in optical and structural properties of materials at ultrahigh pressure.

■ Three assistant professors—*Anastasios S. Lyrantzis*, *Jim M. Papadopoulos*, and *G. Gustavo Weber*—joined the Sibley School of Mechanical and Aerospace Engineering this fall.

Lyrantzis, a specialist in fluid mechanics and acoustics, earned a Diploma at the Technical University of Athens, Greece, and M.S. and Ph.D. degrees at Cornell. He was an assistant professor last year at Syracuse University.

Papadopoulos, who was a visiting scientist in the Department of Theoretical and Applied Mechanics last year, uses mechanics for technological innovation. He earned the S.B. degree at the Massachusetts Institute of Technology, the M.Sc. at the Johns Hopkins University, and the Ph.D. at MIT.

Weber holds a License in Physics from the Universidad de Buenos Aires, Argentina, and M.S. and Ph.D. degrees from the Massachusetts Institute of Technology. His specialty fields are solid mechanics and manufacturing.

■ *Gennady Samorodnitsky* joined the School of Operations Research and Industrial Engineering as an assistant professor. He received a B.S. degree from the Moscow Steel and Alloys Institute in 1978, and M.S. and D.Sc. degrees from Technion-Israel Institute of Technology. Before coming to Cornell, he was a visiting assistant professor at Boston University. He specializes in probability and stochastic processes.

■ Faculty newcomers to the Department of Theoretical and Applied Mechanics are *Phoebus Rosakis* and *Alan Zehnder*.

Rosakis attended Brown University as an undergraduate, received the M.S. degree from the California Institute of Technology, and is completing a doctorate there. A specialist in finite elasticity and continuum mechanics, he is currently an acting assistant professor.

Zehnder, an assistant professor, also comes from the California Institute of

Technology, where he earned M.S. and Ph.D. degrees and then served as a research fellow. His B.S. degree is from the University of California at Berkeley. His specialties are experimental mechanics and nonlinear and dynamic fracture mechanics.

■ A new member of the Writing Program in Engineering is *Susan Hubbard*. The program, begun last year, has a faculty of three who collaborate with engineering professors to incorporate writing and speaking into course assignments. They also work with individual students. In addition, Hubbard teaches a new course, Engineering Communications, which focuses on oral and writing skills necessary in technical professions.

Hubbard has taught in the writing programs at Syracuse University and the State University of New York, and she has worked as a journalist for newspapers in Binghamton, Syracuse, and New Haven, and as an editor and writing consultant. She also writes short fiction; some of her work will appear in forthcoming issues of *The Albany Review*. She holds the B.A. degree in communications and the M.A. in writing and literature from Syracuse.

Kudos for Colleagues

■ Two college faculty members have received Senior U.S. Scientist Awards from the Alexander von Humboldt Foundation of West Germany.

Gerard Salton, a professor in the Department of Computer Science, received the honor last fall. His specialty fields are information organization and retrieval, and language processing.

A recent recipient is *Yih-Hsing Pao*, the Joseph C. Ford Professor, who was recognized for both research and teaching. He specializes in studies of wave propagation in solids, magnetoelasticity, vibrations, and earthquake engineering.

■ *Gerald E. Rehkgler*, chairman of the Department of Agricultural Engineering, was elected a fellow of the American Society of Agricultural Engineers. He was cited for his work in the development of implements, including devices for handling eggs and harvesting cabbage, and for research on the dynamics of agricultural vehicles.

■ Three bicyclists who were outstanding competitors at the Empire State Games in Syracuse this spring are also associates at the Cornell College of Engineering.



Representing the central New York region were *P. C. Tobias deBoer* and *S. Leigh Phoenix*, both professors in the Sibley School of Mechanical and Aerospace Engineering, and *Glenn Swan*, a research technician in the Department of Materials Science and Engineering.

Phoenix and Swan were among the ten cyclists who qualified for the regional men's team, made up of racers from an area that includes Syracuse and Binghamton as well as Ithaca. Swan is coach of the team. DeBoer, who has been a competitive cyclist for many years, participated in the master's class this year.

The central region competitors took both first and second place in the 100-kilometer men's team time trials, one of the four men's cycling events during the four-day games. The central region's first team, led by Swan, came in first, and the second team, led by Phoenix, came in second, only 14 seconds behind.

The team members also did exceptionally well in the main event, the 50-kilometer men's open road race. They took seven of the top eleven places, including first, second, third, and fifth. Swan, who has been a dominant figure in cycling in the

Leigh Phoenix is second in line as his team gets water during the men's team time trials. Another team is heading the other way on the loop.

region for seven or eight years and has won many medals, was fifth-place finisher this year. According to his teammates, the strategy was for Swan to stay near the back of the pack for most of the race, keeping competitors from other teams off guard.

Phoenix, who had given up the sport for several years, made a comeback for this year's games. In addition to helping win in the team time trials, he came in fifteenth in the men's open.

Swan won a bronze medal in the 22-kilometer criterium, or points race, an "around the block" sprint event in which contestants get points for their times at five-lap intervals. Swan's medal was the first ever won in this event by someone from the central region.

DeBoer won a silver medal in the master's class road race. A long-time leader of cycling in the upstate region (he was president of the Finger Lakes Cycling Club for a number of years), he is already planning routes for next year's games, which will be held in Ithaca.

FACULTY PUBLICATIONS

Current research activities at the Cornell University College of Engineering are represented by the following publications and conference papers that appeared or were presented during the three-month period April through June 1988. (Earlier entries omitted from previous Quarterly listings are included here with the year of publication in parentheses.) The names of Cornell personnel are in italics.

■ AGRICULTURAL ENGINEERING

Ahmed, I., W. G. Chesbro, and J. B. Hunter. 1988. Dependence of product distribution on growth rates in recycle culture of solventogenic *clostridia*. Paper read at Annual Meeting, Northeast Microbial Physiologists, Ecologists, and Taxonomists (NEMPET), 22–24 June 1988, in Amherst, MA.

Albright, L. D., A. N. Rousseau, and B. L. Brockett. 1988. A method to quantify the suitability of mechanical ventilation to provide desired indoor conditions. In *Proceedings, 3rd International Symposium on Livestock Environment*, ed. E. Barber, pp. 195–202. St. Joseph, MI: American Society of Agricultural Engineers.

Aneshansley, D. J., G. E. Rehkgler, J. A. Throop, J. Naugle, and S. Berlow. 1988. Beef, apples and grapevines: Machine vision developments in agricultural engineering. In *Robots 12 and vision '88*, ed. R. Potter and E. Abott, vol. 2, pp. 11.15–.25. Dearborn, MI: Society of Manufacturing Engineers.

Datta, A. K. (1987.) Sensor needs and their development for on-line control of food processing operations. Paper read at Winter Meeting, American Society of Agricultural Engineers, 15–18 December, 1987, in Chicago, IL.

Datta, A. K., and A. A. Teixeira. 1988. Numerical modeling of natural convection heating in canned

liquid foods. *Transactions of the American Society of Agricultural Engineers* 30(5):1542–51.

Galton, D. M., D. J. Aneshansley, L. G. Petersson, C. S. Czarniecki, and N. R. Scott. 1988. Pressure gradients across the teat canal during machine milking. In *Milking systems and milking management*, ed. R. E. Graves, pp. 114–21. Ithaca, NY: Northern Regional Agricultural Engineering Service, Cornell University.

Glass, R. J., T. S. Steenhuis, G. H. Oosting, and J.-Y. Parlange. 1988. Uncertainty in model calibration and validation for the convection-dispersion process in the layered vadose zone. Paper read at conference, Validation of Flow and Transport Models for the Unsaturated Zone, 23–26 May 1988, in Ruidoso, NM.

Griffin, K. C. 1988. *Small highway department management.* Cornell Local Roads Program report no. 88–5. Ithaca, NY: Cornell University.

Hunter, J. B. 1988. Protein concentration profiles in counteracting chromatographic electrophoresis. Paper read at 195th National Meeting, American Chemical Society, 5–11 June 1988, in Toronto, Ontario, Canada.

Hunter, J. B., and J. A. Asenjo. 1988. A structured mechanistic model of the kinetics of enzymatic lysis and disruption of yeast cells. *Biotechnology and Bioengineering* 31(9):929–43.

Irwin, L. H. (1987.) *Significance of maintenance on aggregate-surfaced roads: Final report.* Cornell Local Roads Program report no. 87–5. Ithaca, NY: Cornell University.

Leibensperger, R. Y., and R. E. Pitt. 1988. Modeling the effects of formic acid and molasses on ensilage. *Journal of Dairy Science* 71:1220–31.

Petersson, L. G., D. M. Galton, D. J. Aneshansley, and C. S. Czarniecki. 1988. Method of measuring air

pressure during machine milking using electronic pressure transducers. In *Milking systems and milking management*, ed. R. E. Graves, pp. 122–26. Ithaca, NY: Northern Regional Agricultural Engineering Service, Cornell University.

Rousseau, A. N., and L. D. Albright. 1988. A comparison of steady-state and transient analysis of the thermal behavior of agricultural buildings. Paper read at Annual Meeting, American Society of Agricultural Engineers, 26–29 June 1988, in Rapid City, SD.

Skelton, K. 1988. *Communication with your board and the public.* Cornell Local Roads Program report no. 88–4. Ithaca, NY: Cornell University.

Staubitz, W. W., J. M. Surface, T. S. Steenhuis, M. J. Lavine, N. C. Weeks, W. E. Sanford, and R. J. Kopka. 1988. Potential use of constructed wetlands to treat landfill leachate. Paper read at International Conference on the Use of Constructed Wetlands for the Treatment of Wastewater, 12–16 June 1988, in Chattanooga, TN.

Steenhuis, T. S., and R. E. Muck. 1988. Preferred movement of nonadsorbed chemicals on wet, shallow, sloping soils. *Journal of Environmental Quality* 17:376–84.

Steenhuis, T. S., and J.-Y. Parlange. 1988. Simulating preferential flow of water and solutes on hillslopes. Paper read at conference, Validation of Flow and Transport Models for the Unsaturated Zone, 23–26 May 1988, in Ruidoso, NM.

Van Wicklen, G., and L. D. Albright. 1988. Removal mechanisms for calf barn aerosol particles. *Transactions of the American Society of Agricultural Engineers* 30(6):1758–63.

Yang, W.-S., and L. H. Irwin. 1988. *Mechanistic analysis of nondestructive pavement deflection data.* Cornell Local Roads Program report no. 88–1. Ithaca, NY: Cornell University.

■ APPLIED AND ENGINEERING PHYSICS

Farmer, K. R., R. Saletti, and R. A. Buhrman. 1988. Current fluctuations and silicon oxide wear-out in metal-oxide-semiconductor tunnel diodes. *Applied Physics Letters* 52:1749-51.

Millard, P. J., D. Gross, W. W. Webb, and C. Fawcett. 1988. Imaging asynchronous changes in intracellular Ca^{2+} in individual stimulated tumor mast cells. *Proceedings, National Academy of Sciences* 85:1854-58.

Nelson, S. A., H. D. Hallen, and R. A. Buhrman. 1988. A structural and electrical comparison of thin SiO₂ films grown on silicon by plasma anodization and rapid thermal processing to furnace oxidation. *Journal of Applied Physics* 63:5027-35.

O'Brien, W. L., T. N. Rhodin, and L. C. Rathbun. 1988. Gas phase recombination of ionic molecules for ion-induced surface emission. *Surface Science* 201:75-86.

Ralls, K. S., and R. A. Buhrman. 1988. Defect interactions and noise in metallic nanoconstrictions. *Physical Review Letters* 60:2434-37.

■ CHEMICAL ENGINEERING

Aven, M. R., and C. Cohen. 1988. Properties of poly(dimethyl siloxane) chains and gels in toluene and in toluene/methanol mixtures. *Die Makromolekulare Chemie* 189:881-98.

Hammers, R. J., P. L. Houston, and R. P. Merrill. 1988. Competition between direct-inelastic and trapping desorption channels in the scattering of NO(v=O,J) from Ir(111). *Journal of Chemical Physics* 88:6548-55.

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Koch, D. L., and J. F. Brady. 1988. Anomalous diffusion in heterogeneous porous media. *Physics of Fluids* 31(5):965-73.

Lee, S. Y., and M. L. Shuler. 1988. Microbial growth model based on carbon material balance and carbon dioxide evolution rate. Paper read at 3rd Chemical Congress of North America, 5-11 June 1988, in Toronto, Canada.

Panagiotopoulos, A. Z. 1988. Gibbs-Ensemble Monte Carlo simulations of high pressure phase equilibria. Paper read at the International Symposium on Thermodynamics in Chemical Engineering and Industry, 30 May-2 June 1988, in Beijing, China.

Panagiotopoulos, A. Z., R. C. Wilson, and R. C. Reid. 1988. Phase equilibria in ternary systems with carbon dioxide, water and carboxylic acids at elevated pressures. *Journal of Chemical Engineering Data* 33:321-27.

Payne, G. F., N. N. Payne, and M. L. Shuler. 1988.

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Payne, G. F., N. N. Payne, M. L. Shuler, and M. Asada. 1988. *In situ* adsorption for enhanced alkaloid production by *Catharanthus roseus*. *Biotechnology Letters* 10(3):187-92.

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Shaqfeh, E. S. G., and D. L. Koch. 1988. The effect of hydrodynamic interactions on the orientation of axisymmetric particles flowing through a fixed bed of spheres or fibers. *Physics of Fluids* 31(4):728-43.

Shuler, M. L. 1988. Immobilized biocatalysts and reactors. Paper read at Engineering Foundation Conference: Chemical Engineering Education in a Changing Environment, 17-22 January 1988, in Santa Barbara, CA.

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Arita, M., and G. H. Jirka. 1988. Two-layer model of the saline wedge. I: Entrainment and interfacial friction. II: Prediction of mean properties. *Journal of Hydraulic Engineering* 113(10):1229-63.

Bierck, B. R., S. A. Wells, and R. I. Dick. 1988. Compressible cake filtration: Monitoring cake formation and shrinkage using synchrotron x-rays. *Journal of the Water Pollution Control Federation* 60:645-50.

Bisogni, J. J., Jr., and S. A. Kishbaugh. 1988. Alkalinity destruction by sediment organic matter dissolution during neutralization of acidified lakes. *Water, Air, and Soil Pollution* 38:85-95.

Blewitt, J. R., A. R. Ingrassia, T. D. O'Rourke, and H. E. Stewart. (1987.) *Analytical study of stresses in transmission and distribution pipelines beneath railroads*. Report no. GRI-87/0234. Chicago, IL: Gas Research Institute.

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