# HIGH-PERFORMANCE SINGLE-PHASE LINE-INTERFACED POWER CONVERTERS

A Dissertation

Presented to the Faculty of the Graduate School

of Cornell University

In Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

Danish Shahzad

August 2021

# HIGH-PERFORMANCE SINGLE-PHASE LINE-INTERFACED POWER CONVERTERS

Danish Shahzad, Ph.D.

Cornell University 2021

The use of single-phase line-interfaced power converters in electrical power systems is rapidly growing due to the changing nature and power quality requirements of electrical loads. Most applications require these single-phase line-interfaced power converters to be compact and efficient, and depending on application meet additional performance, cost, and reliability targets. This thesis presents innovative system architectures, circuit topologies, design methodologies, and control strategies for highly compact and efficient single-phase ac-dc and ac-ac line-interfaced power converters. First, a comprehensive design methodology for step-down isolated two-stage ac-dc converters is presented which compares various designs and operating modes and selects the optimal design based on overall volume and efficiency. Additionally, a new control strategy is presented for a compact front-end soft-switched power-factor correction (PFC) stage to ensure compliance with strict electromagnetic interference (EMI) regulations. A 1-kW universal-input to 28V-output isolated ac-dc prototype converter is built to showcase performance benefits of proposed design and control strategies. This prototype achieves a high-power-density of 84W/in$^3$ and maintains greater than 93% efficiency across a wide output power range. Next, the functionality of the proposed ac-dc converter is further enhanced by incorporating a new droop control strategy for parallel operation of multiple similar ac-dc converter modules. The proposed control strategy uses the input current of the secondary dc-dc stage of two-stage ac-dc converters in conjunction with variable droop

resistance to achieve near-perfect parallel operation. A multi-module ac-dc conversion system is built to validate the proposed droop control strategy. The parallel modules achieve a current distribution error of less than 2% near their maximum output power. Multiple ac-ac conversion applications are also addressed in this thesis. For highly cost-sensitive applications, two compact and efficient single-stage ac-ac converters are presented which utilize a comprehensive design methodology centered around minimizing the total cost of components. Moreover, innovative control strategies are presented for both ac-ac converters to enable output voltage regulation under input voltage and output load fluctuations. Both single-stage ac-ac prototype converters, utilizing the proposed design and control strategies, are built and tested. The 600-W $480V_{rms}$-to-$264V_{rms}$ prototypes achieve power densities exceeding $40W/in^3$ while maintaining conversion efficiencies of greater than 96% across majority of the output load. Finally, a much more feature-rich ac-dc-ac converter is also proposed for advanced ac-ac conversion applications, such as data center online uninterruptible power supplies (UPS). The proposed transformer-less two-stage ac-ac converter is based on a new circuit topology which can operate at high switching frequencies (up to several MHz) and utilize 50% lower dc-bus capacitance than conventional split-dc-bus topologies. A 1-kVA $120V_{rms}$ prototype ac-dc-ac converter is built and extensively tested to showcase performance improvements. This prototype achieves high peak conversion efficiency of greater than 95% and high power density of $26.4W/in^3$ while utilizing long-life but relatively bulky film dc-bus capacitors.

# BIOGRAPHICAL SKETCH

Danish Shahzad received the B.S. degree in electrical engineering from the School of Science and Engineering at Lahore University of Management Sciences, Lahore, Pakistan in 2016, the M.S. degree in electrical engineering from Cornell University, Ithaca, NY, USA in 2020, and the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, USA in 2021. His research interests include design and control of high-efficiency high-power-density single-phase ac-dc and ac-ac power electronic converters. He was awarded an NMF Gold Medal for being the top B.S. electrical engineering graduate and has received two conference registration awards based on paper quality at IEEE COMPEL 2020 and IEEE ECCE 2021.

In the name of Allah, the Most Gracious, the Most Merciful

“He has taught man which he knew not.” (Al-Quran 96:5)

*Dedicated to my parents*

# ACKNOWLEDGEMENTS

One of the greatest pleasures of my journey through this doctorate has been working with Professor Khurram Afridi. His infectious energy, incredible knowledge of scientific principles, and ability to ask all the right questions, greatly inspired me and helped me prosper as a power electronics engineer. He believed in me when I was uncertain, gave me abundant room to flourish independently, and taught me countless academic and non-academic lessons from his own life's journey. His mentorship and guidance have been crucial in defining my professional image, and for all this and much more, I would like to thank Professor Afridi. I would also like to extend my deepest gratitude to my thesis committee members: Professor Alyosha Molnar and Professor Debdeep Jena for their continuous support and guidance throughout my doctorate, and their valuable suggestions in shaping this thesis.

In retrospect, none of this journey would have been possible without the support and guidance of two individuals: my undergraduate advisor - Professor Nauman Zaffar and my elder sister – Hafsah Shahzad who is also an electrical engineer. Both instilled in me the love for electrical engineering and were crucial in motivating me to pursue a doctorate with Professor Afridi. I would also like to thank my teachers and mentors at my undergraduate institution (LUMS-SSE) and my high-school (Beaconhouse Defence Lahore) for their support and guidance. I would also like to take this opportunity to acknowledge Aegis Power Systems, GRE-Alpha, and Schneider Electric for financially supporting my doctoral work and to express my gratitude to the teams at these companies for enlightening me with numerous practical aspects of power electronics converter design.

I also would like to thank my friends and colleagues at CoPEC and Cornell for making this journey wonderful, especially Saad Pervaiz, Ashish Kumar, Brandon Regensburger, Vivek Sankaranarayanan, Sreyam Sinha, Mausamjeet Khatua, Firehiwot Gurara, Maida Farooq, Yuetao Hou, and Sounak Maji. I would also like to thank my friends in Boulder, Colorado and Ithaca, New York for filling my Ph.D. journey with joy and laughter, especially Muneeb Khan, Saad Ansari, Yasir Shah, Uzair Butt, Ali Sair,

Hassan Ilyas, Hassnain Asgar, Awais Rana, and Taha Jamshed. I will forever cherish those fun-filled hiking excursions and laughter sessions in and around Ithaca.

I would like to thank my family members: Bilal Shafiq (my uncle) and Ahmed Sanaullah (my brother-in-law) for their support throughout my time in the US. Last but not the least, I would like to thank my parents, to whom I dedicate my successes, for their unconditional love and unwavering support. Their prayers, wishes, and wisdom have had a profound impact on my personality and have made my life all the more fulfilling - Alhamdulillah.

# TABLE OF CONTENTS

CHAPTER

# LIST OF TABLES

# LIST OF FIGURES

# CHAPTER 1

# INTRODUCTION

With global electricity demand continually increasing, energy sustainability has become a critical metric in the design of future electrical power systems [1]. The new energy sustainability goals are being met by utilization of renewable sources of energy, more efficient distribution of electrical energy and its more effective end-use. Renewable sources of energy, such as wind and solar, as well as more effective electrical-energy end-users, such as LED lighting and electric vehicles (EVs), require the use of power electronics to interface with the electric grid; these power electronic converters are also referred to as line-interfaced power converters. Additionally, with the rapid growth of data centers, there is a growing need for high-quality power, which is also enabled by line-interfaced power converters.

This thesis covers line-interfaced power converters which draw energy from the electric grid to power electrical loads (i.e., provide an interface between the electric grid and electrical-energy end-users), as opposed to line-interfaced power converters that deliver power to the electric grid from power generation sources. A large fraction of line-interfaced power converters used to power electrical loads operate from single-phase electric grid, also referred to as single-phase ac-line. Hence, the focus of this thesis is on single-phase line-interfaced power converters.

## 1.1 MOTIVATION

Over the last 30 years, the need for increased use of power electronics in electrical power systems is mainly driven by the rapidly changing nature and power quality requirements of electrical loads [2]. In the past, most loads used to operate directly from the ac-line and there was no need for an intermediate power conversion stage. However, with the increased use of new loads that cannot operate directly from the ac-line, power electronic converters that act as an interface (also referred to as line-interfaced power converters) have gained immense value. This development is largely motivated by the enormous growth

in applications such as consumer electronics, lighting, telecommunication, data centers, energy storage, aerospace, and electric vehicles, to name a few [2],[3]. For instance, global electricity usage in information-communication technology (ICT) space, which heavily relies on single-phase line-interfaced power converters, has grown from roughly 12.5TWh/year in early 1990s to 242TWh/year in 2015 [4],[5]. Similarly, lighting industry previously dominated by incandescent bulbs driven directly from ac-line is now transitioning toward using LEDs which require an intermediate line-interfaced power converter (offline LED drivers) for operation. Such evolving nature of loads is presenting new opportunities for advancement in line-interfaced power converters.

Owing to the vast application space of single-phase line-interfaced power converters, further development in this area can drastically enhance the capability of modern electronics. For instance, data centers rely on single-phase ac-dc converters to power various computing and storage systems. Moreover, sensitive data storage equipment in data server racks can malfunction due to power outages or line disturbances which can result in data loss. Therefore, single-phase online uninterruptible power supplies (UPS), comprising an ac-dc-ac converter, are used in data centers to ensure an undisrupted supply of ac power to data servers [6]. Reducing the size of such ac-dc and ac-dc-ac power converters can provide extra space for data storage equipment in server racks thereby enhancing the storage capability of data centers. Similarly, electric vehicles (EV), which are rapidly emerging as the future of land transportation, heavily rely on single-phase ac-dc converters for on-board and off-board (level-1) battery chargers [7], [8]. Reducing the volume of on-board battery chargers can provide more space for energy storage and therefore enhance the range of EV [8]. Since compactness of single-phase power converters is essential in many applications, it is often quantified by power density which is an important performance metric for single-phase line-interfaced power converters.

Advancement in single phase line interfaced power converters can also help reduce costs and make new technology more affordable. As an example, LED lighting relies on offline LED drivers (ac-dc converters) to operate. Reducing the volume of LED drivers can help reduce manufacturing, packaging,

and shipping costs, which can lower the overall cost of adoption of LED technology [9]. Another opportunity to reduce cost is by encouraging increased modularity and integration. Such single-phase line-interfaced power converters can be operated in parallel to support an enormous range of applications and power levels. This can facilitate mass production which can ensure substantial savings in manufacturing costs through economies of scale [10]. Another aspect of performance is conversion efficiency of the single-phase power converters. Efficiency improvements in such converters can reduce the operational costs associated with electricity usage. In long-term this can result in substantial reduction in costs through energy saving.

Efficiency of single phase line interfaced power converters can also promote global sustainability initiatives set to reduce carbon emissions and achieve a greener future. Emerging certification standards require higher conversion efficiencies than ever before. As an example, 80-Plus Titanium certification introduced for desktop computers' power supplies in 2015 requires full-load efficiency of $115V_{rms}$ ac-dc converters to be greater than 90%, substantially higher than 80% in standard 80-Plus certification first established in 2004 [11]. Similar efficiency targets are being introduced by other certification agencies such as Energy Star which is backed by US government [12]. It is clear from such initiatives that the power converters of the future need to achieve even higher conversion efficiencies. Furthermore, the desire to make converters more compact requires them to be more efficient as there is less surface area for heat removal. Therefore, on-going research in single-phase line-interfaced power converters needs to focus on efficiency as another key performance metric.

To explore opportunities for performance enhancement of single-phase line-interfaced power converters that draw energy from ac line, three strategic applications have been selected in this thesis which achieve a broad coverage of the entire application space. These applications include ac-dc converters for electronic equipment, ac-ac converters for lighting applications, and ac-dc-ac converters for data-center online UPS.

## 1.2 STATE OF THE ART

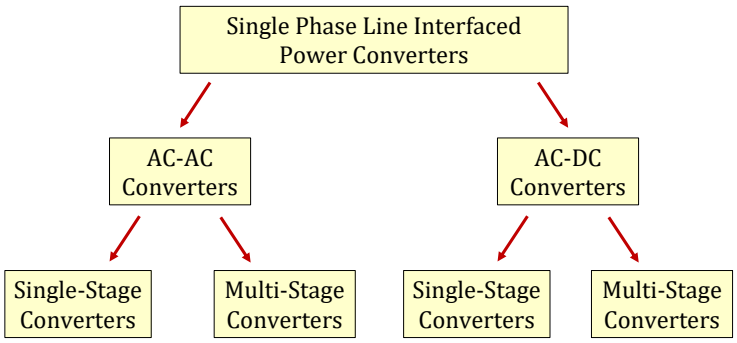
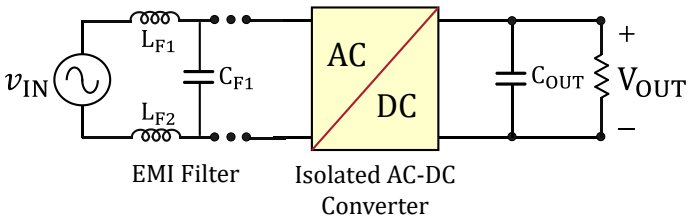



Fig. 1.1: Architectures of single-phase line-interfaced power conversion systems.

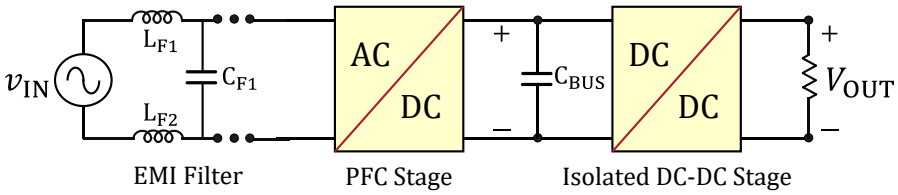
Several single-phase line-interfaced power converters have been proposed by various researchers that draw energy from the ac-line. These power converters can be broadly divided into two types: ac-dc converters and ac-ac converters. Each type can be further divided into single-stage or multi-stage architectures to accommodate application specific requirements. These requirements can include need for galvanic isolation (or common-neutral in certain ac-ac converters) and need for energy storage (prevalent in ac-dc but optional in ac-ac converters). Fig. 1.1 summarizes the different types of single-phase line-interfaced power converters and their architectures.

Regardless of the type of line interfaced power converters, researchers have focused on two aspects of power electronics for performance enhancement: design of power stage and control of power stage. In design innovations, several new architectures, topologies, and component-selection strategies are explored which can result in better performance. On the other hand, innovative control methodologies are presented in literature which focus on efficiency improvement by enabling loss reduction (in certain cases through soft-switching) and power density improvement by operating at high switching frequencies, while adhering to application specific requirements. Specific details about the applications addressed in this thesis and a comprehensive assessment of state-of-the-art power converters for those applications is highlighted below:

### 1.2.1 AC-DC Converters for Electronic Equipment




(a)




(b)

Fig. 1.2: Single-phase isolated ac-dc converter architectures: (a) single-stage ac-dc converter, (b) two-stage ac-dc converter.

Step-down isolated ac-dc power converters are extensively utilized in electronics equipment [13]. In such application, an isolated ac-dc converter needs to satisfy multiple performance specifications, including stringent EMI requirements [14]. Additionally, ever-increasing space and energy utilization constraints in modern applications have made power density and efficiency a key performance requirement for such power converters [15],[16]. Existing state-of-the-art isolated ac-dc power converters can be broadly categorized into single-stage or two-stage architectures, as shown in Fig. 1.2 [17],[18]. Single-stage ac-dc converters typically utilize a line-frequency bridge rectifier followed by an isolated dc-dc converter, such as isolated pulse-width modulated (PWM) converters [19]-[23] or isolated resonant converters [24]-[28]. In such architectures, the isolated dc-dc converter performs multiple functions including input power factor correction (PFC) and output dc-voltage regulation. Single-stage low-output-voltage ac-dc converter architectures have potential for lower component count and higher efficiencies but often suffer from lower power densities. The reason stems from the fact that in such architectures, the twice-line-frequency energy buffering capacitor is placed at the output of the converter. Thus, a very large output capacitor is required to keep the twice-line-frequency voltage ripple within the tight output voltage regulation requirements. On the contrary, in two stage ac-dc converters,

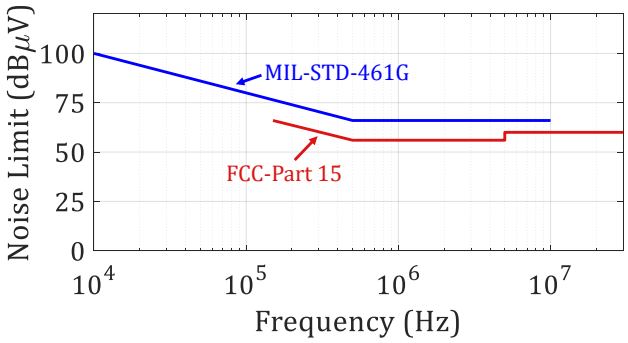



Fig. 1.3: EMI limits imposed on ac-dc converters by FCC-Part 15 and MIL-STD 461G.

the PFC function is performed by a front-end ac-dc stage and the output voltage regulation function is accomplished by the isolated dc-dc stage [18]. An intermediate dc-bus is utilized between the two conversion stages for twice-line-frequency energy buffering. This decouples the energy buffering and output voltage regulation functions, resulting in reduction in overall capacitance requirement. As a result, the two-stage architectures can often achieve high power densities exceeding 50W/in$^3$ [29]-[34].

Extensive research has been reported in the literature to enhance the performance of two-stage ac-dc converters by proposing rigorous design and optimization methodologies in [31],[35],[38], by devising new topological innovations in [37]-[41], and by utilizing new soft-switching techniques in [27]-[30],[32],[34]-[45]. However, such performance benefits often come at the cost of higher overall switch-count, which increases design complexity and/or require complex control strategies. Additionally, telecommunication equipment is extensively utilized in defense applications which makes compliance with MIL-STD specifications essential for such power converters. However, very limited research is available to evaluate the performance of two-stage ac-dc converter architectures for compliance with the more stringent MIL-STD-461G EMI requirements, which impose regulations starting at a lower frequency (10kHz) as compared to 150kHz in FCC-Part 15 or CISPR regulations, as shown in Fig. 1.3 [46],[47].

Paralleled converter operation is also preferred in many high power applications as it enables modularity and improved fault tolerance and reliability due to redundancy, while lowering

manufacturing costs through economies of scale [48],[49]. Recently, various paralleling strategies have been proposed which utilize either centralized or decentralized control architectures to enable equal load current distribution among paralleled converter modules [50]-[59]. Centralized (or master-slave) control architectures allow high conversion efficiency and tight output voltage regulation [50],[51]. However, they suffer from lower overall system reliability due to a single master controller which in case of a fault acts as a single point of failure hence rendering the whole system inoperable. On the contrary, decentralized architectures utilize multiple autonomous power converter modules to ensure equal load current distribution. Such system architectures are beneficial as they do not result in full system failure in case of a single fault in an individual module. Popular decentralized control architectures for power conversion systems utilizing multiple paralleled modules mainly comprise of a droop controller which varies the output voltage of a converter module based on the magnitude of its output current. Several output current based droop control strategies are presented in literature that ensure equal output load current distribution while maintaining a stable output dc voltage [52]-[59]. However, these control strategies require output current sensing, which is challenging in isolated low output voltage high-power converters where large magnitudes of output currents are involved. Furthermore, limited research is available to evaluate the performance of droop controller in two-stage isolated ac-dc conversion architectures, especially in low output voltage (under 48V) applications.

### 1.2.2 AC-AC CONVERTERS FOR LED LIGHTING APPLICATION

Lighting application is another important area of research for single-phase line-interfaced power converters. Rapid shift towards LEDs, especially in industrial lighting, has driven advancements in LED driver technology resulting in more efficient and compact LED drivers. These LED drivers are typically designed to operate across universal ac-line voltage ($85V_{rms}$ to $264V_{rms}$). However, many industrial workspaces are powered by three-phase distribution network comprising $480V_{rms}$ line-to-line ac voltage. To power the universal-input single-phase LED drivers in these workspaces, there is a need for $480V_{rms}$ to $264V_{rms}$ ac-ac voltage conversion. This is typically achieved using low-cost wire-wound line-

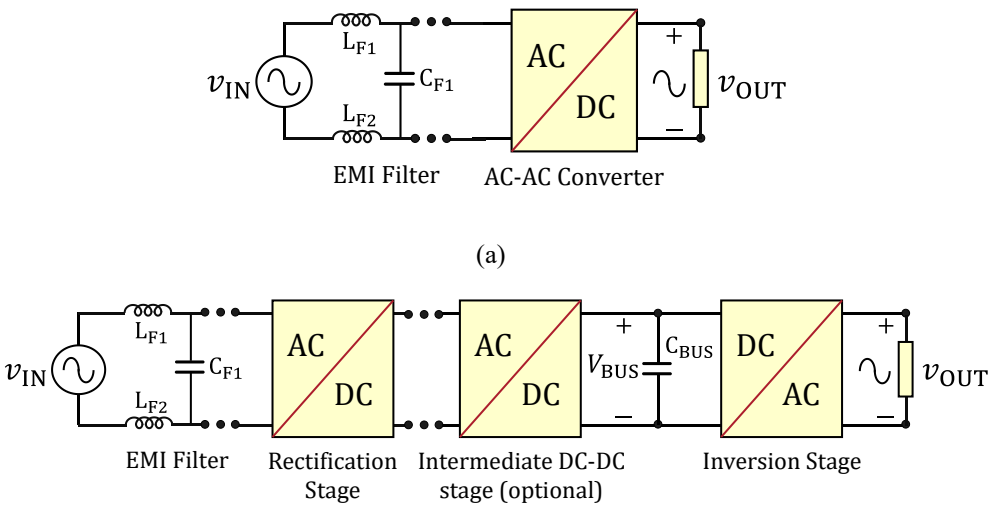



Fig. 1.4: Architectures of single phase ac-ac converters: (a) single-stage ac-ac converter, (b) multi-stage ac-ac converters.

frequency auto-transformers. Although these auto-transformers provide an efficient and cost-effective solution, they have low power density (less than 15W/in$^3$), fixed conversion ratio, and poor output voltage regulation. These limitations in conventional auto-transformers can be overcome by utilizing single-phase ac-ac converters [60]-[66]. Single phase ac-ac converters can be classified in two broad categories: single-stage architectures and multi-stage (typically two-stage) architectures, as shown in Fig. 1.4. Single stage architectures [60]-[64] generally provide low-cost and simple solution to ac-voltage conversion needs but offer limited capability in terms of control and output voltage regulation. Multi-stage architectures typically consist of a front-end ac-dc rectification stage which is followed by an optional intermediate dc-dc regulation stage(s) and an output inversion stage. Such architectures exhibit superior performance in terms of output voltage regulation but have higher number of components, complex control, and higher cost. Further assessment of multi-stage ac-ac converters is presented in the next sub-section. Owing to the lower component count in single-stage architectures, such architectures can be explored for use in such low-cost ac-ac conversion applications. Majority of the single-phase ac-ac converters presented in the literature are focused on high-power high-voltage

utility and grid applications and very few lower-power/voltage ac-ac converters are presented. In addition, little work has been presented on cost reduction of these low-power ac-ac converters which is a crucial design parameter in the LED lighting application space.

### 1.2.3 AC-DC-AC Converters for Data Center Online Uninterruptible Power Supplies

Uninterruptible power supplies (UPS), which are another type of single-phase line-interfaced ac-ac power converters, provide essential backup power to critical electrical loads during grid outages and disturbances [67]. UPS can be divided into three categories depending on their architecture, as shown in Fig. 1.5. These three categories, namely offline UPS, line-interactive UPS, and online UPS, exhibit distinct characteristics in terms of their normal-to-backup mode change-over time (also called transfer time) and their ability to reject input voltage disturbances [68], [69]. Offline UPS (also known as standby UPS) typically comprises a battery charger (ac-dc converter) and an inverter (dc-ac converter). At each point in time, only one of the mentioned power stages operates. In the normal operation, the input directly connects to the output using a static switch and battery charger maintains the state-of-charge (SOC) of the back-up battery. In case of a grid failure, the static switch is turned off to disconnect the input from the output and then the back-up battery powers the load through an inverter. Offline UPSs have a high change-over time and provide the least protection against input voltage disturbances during normal operation since the inverter operates only during backup mode [70]. This limits their usage to common household applications where brief disturbances in input voltage do not harm the load or its operation, and where high-quality grid voltage is normally available. However, in environments where the grid is more prone to disturbances or where higher power quality is desired, e.g., large industrial settings, a line-interactive UPS is preferred over offline UPS. The operation of line interactive UPS is shown in Fig. 1.5(b). This type of UPS typically comprises a bidirectional ac-dc converter. In the normal mode, the grid is connected to the load through a passive regulation stage and the ac-dc converter maintains the SOC of backup battery. The passive regulation stage filters most of the line disturbances

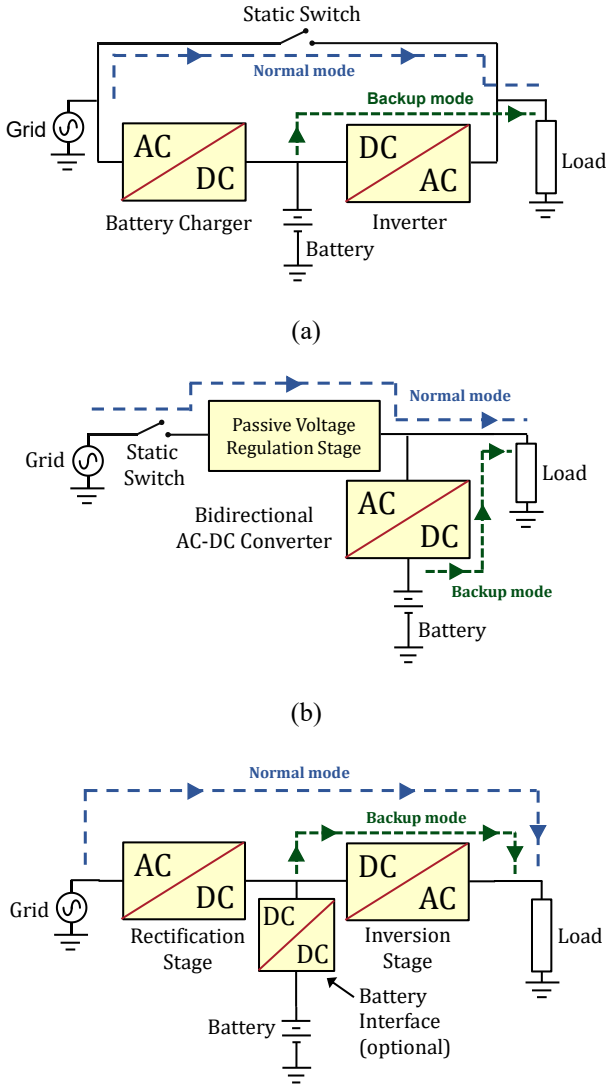



Fig. 1.5: Types of uninterruptible power supply (UPS) architectures with their power flow direction specified in normal and back-up modes of operation: (a) offline UPS, (b) line-interactive UPS, and (c) online UPS.

and hence a line interactive UPS have better line disturbance rejection compared to offline UPS. However, since this architecture also utilizes a series switch to disconnect the grid before the inverter (dc-ac converter) can start operation in case of grid failure, the change-over time is in the order of few milliseconds which is still significant [71]-[73]. Substantial work has been presented in literature to reduce change-over time of such UPS topologies [74]-[76]. However, the proposed topologies and/or control methodologies still have limitations, especially in terms of ensuring output voltage/frequency

regulation in the face of noise in the grid voltage or fluctuations in grid voltage/frequency. For applications where availability of undisrupted input voltage is vital for safety and operation of critical electrical loads, an online UPS is employed [77]-[79]. An online UPS (also known as a double-conversion UPS) comprises a rectification stage (ac-dc converter) followed by an inversion stage (dc-ac converter). In normal mode, the rectification stage first converts the grid voltage to a dc voltage across an intermediate dc-bus and the inversion stage then converts that dc-bus voltage into an ac voltage of the desired amplitude and frequency across the critical load at the output, as shown in Fig. 1.5(c). Since the load is always powered by the dc-ac inversion stage, the online UPS provides a high degree of immunity from input voltage disturbances and eliminates any change-over time which ensures an undisrupted ac voltage across the output load [77]. The intermediate dc-bus is powered from a battery either through a direct connection (when using a high voltage battery) or through a fast response dc-dc converter to minimize the droop in the dc-bus voltage in case of grid-failure. An online UPS can also change the line frequency. The frequency changing capability is especially useful in scenarios where the online UPS is required to maintain a fixed output frequency while the input line frequency may be varying. Owing to these benefits, online UPSs are most commonly utilized in data-center applications, where supply of a stable ac voltage is crucial for safety of sensitive electronic equipment and continual operation of data servers [78]. However, increasing user data and rising IT rack power densities in data centers are putting additional constraints on the space available for power conversion. Consequently, the volume (and hence the power density) of online UPS systems has become a key performance metric [80].

Several online UPSs have been presented in the literature which are either based on transformer isolated topologies or non-isolated topologies. Transformer isolated topologies utilize high frequency operation and a single dc-bus [81]-[89]. Such topologies most commonly utilize an isolated PFC rectification stage to meet isolation requirements [81]-[87]. Three-stage isolated online UPS are also presented, which utilize an additional dc-dc conversion stage either prior to the PFC rectification stage

(in [88]) or after the PFC rectification stage (in [89]), to satisfy the isolation requirements. In all above topologies, the presence of a transformer rated for peak AC output-power limits their efficiency (which is typically below 90%) and also adversely affects their power density. Non-isolated online UPS topologies can be sub-categorized into two groups based on whether they have a common-neutral between the input and output ac ports. The non-isolated topologies that do not have a common-neutral between their input and output ports [90]-[97] do not satisfy various safety related grounding requirements imposed by regulatory bodies, such as NEC and TIA [98]-[101]. To ensure compliance with the grounding requirements, these non-isolated topologies require an external line-frequency transformer which significantly impacts their power density. Various non-isolated online UPS topologies, that do have a common-neutral between input and output ac ports, have also been reported in literature [102]-[111]. However, these topologies also have several drawbacks, such as the use of four-quadrant switches that limits their operating frequency [102]-[104], the presence of split dc-bus that doubles the capacitance requirement and thus limits their overall power density [103]-[111], or a higher component/switch count that increases their control complexity [110],[112]. A few topologies with a common-neutral and a single dc-bus have also been presented in [113]-[115]. In these topologies, a half-bridge switching-leg is shared between the rectification and inversion stages, which prevents these topologies from generating an output voltage at a frequency/phase other than the input line frequency/phase. Therefore, these topologies cannot be used as an online UPS.

## 1.3 CONTRIBUTIONS OF THE THESIS

This thesis introduces design and control methodologies to enhance performance of single-phase line-interfaced power converters. These methodologies are presented for three strategically selected power conversion applications to achieve a broad coverage of the entire application space. Firstly, a high-power-density high-efficiency soft-switched single-phase universal-input to 28V-output isolated ac-dc converter module is presented for powering electronic loads. The proposed two-stage converter

utilizes a totem-pole bridgeless boost power-factor correction (PFC) ac-dc converter stage followed by an isolated LLC resonant dc-dc converter stage. A comprehensive design and optimization methodology is presented that compares various designs and operating modes for the converter's power stages and selects the optimal design based on overall power density and efficiency. Additionally, a control scheme is presented for the PFC stage to minimize current distortion by accounting for various sensor, control, and gate-drive delays while ensuring zero-voltage switching (ZVS) of the transistors. To validate the proposed design and control strategy, a 1-kW universal-input to 28V-output isolated ac-dc converter module is built and tested. The prototype converter module achieves a high power density of 84W/in$^3$ and a peak efficiency of greater than 93%.

Next, the functionality of the proposed isolated ac-dc converter is further enhanced by introducing a new droop control methodology to achieve parallel operation. The proposed control approach employs the input current of the secondary dc-dc conversion stage (LLC converter) to enable adequate output current distribution between paralleled modules when powering a common output load. The proposed droop control strategy also incorporates a variable droop resistance based on the instantaneous value of the dc-bus voltage to compensate for the effect of the twice-line frequency dc-bus voltage ripple and ensure a stable output dc-voltage. To validate the proposed control strategy, two 1-kW universal input-to-28V ac-dc converter modules are designed, built, and tested. The prototype system achieves a current distribution error of less than 2% at the peak output power of 2kW while maintaining a high conversion efficiency of greater than 91% across a 3:1 output power range.

Next, this thesis presents two low-cost high-efficiency high-power-density single-stage 480V$_{rms}$ to 264V$_{rms}$ ac-ac converters for LED lighting applications. The first ac-ac converter utilizes a 2-level ac-ac buck converter topology and the second ac-ac converter utilizes a 3-level center-point-clamped (CPC) ac-ac buck converter topology. Both topologies demonstrate high performance while minimizing the overall cost. This is achieved through a comprehensive cost and efficiency optimization methodology that helps identify the most appropriate converter designs across a design space comprising various

switch structures, a range of operating frequencies, and different inductance values. Moreover, control strategies are also presented for both ac-ac converters to regulate their output voltage and a switching scheme is introduced that ensures smooth inductor current commutation during switching transitions and reduces zero-crossing distortion in the input. Furthermore, an active voltage balancing scheme is developed for the 3-level CPC ac-ac converter to compensate for any imbalances between the two stacked input capacitors to ensure robust converter operation. Two 600-W ac-ac prototype converters based on the proposed optimization, designed to operate at an input voltage of $480V_{rms}$ and an output voltage of $264V_{rms}$ are built and tested. Both prototyped converters achieve high conversion efficiencies and high power densities, while achieving a comparable overall component cost to the conventional solution of a line-frequency transformer. To validate the proposed design and control strategies and demonstrate the performance of both single-stage ac-ac conversion topologies, two prototype 600-W ac-ac converters designed to operate at an input voltage of $480V_{rms}$ and an output voltage of $264V_{rms}$ are built and tested. The prototype 3-level CPC ac-ac buck converter achieves a peak efficiency of 96% while having a power density of $40W/in^3$ and the prototype 2-level ac-ac buck converter achieves a peak efficiency of 97% while having a power density of $60W/in^3$. Both ac-ac converters achieve overall component cost comparable with a conventional line-frequency transformer.

Finally, this thesis presents a new transformer-less ac-dc-ac converter topology which is suitable for a high-power-density high-efficiency single-phase data-center online uninterruptible power supply (UPS) with a common neutral between the input and output ac ports. The proposed converter comprises an input power factor correction (PFC) rectification (ac-dc) stage which is followed by an inversion (dc-ac) stage. The rectification stage operates in boost mode during the input positive half line cycle and buck-boost mode during the input negative half line cycle, while the inversion stage operates in buck and buck-boost modes in the output positive and negative half line cycles, respectively. The rectification stage utilizes boundary conduction mode (BCM) control enabling soft-switching and allowing high frequency operation. The inversion stage is operated in continuous conduction mode (CCM), wherein a

digital controller regulates the output voltage of the converter across both resistive and reactive loads. The proposed online UPS utilizes a single (non-split) dc-bus between the rectification and inversion stages, resulting in a 50% reduction in dc-bus capacitance requirement compared to conventional split-bus online UPS topologies. Additionally, two battery interface solutions are also investigated which provide a trade-off between passive volume and additional switch-count. To verify the performance and control of the proposed online UPS, a GaN-based electrolytic-free 1-kVA prototype online UPS is designed, built, and tested. The prototype ac-dc-ac converter achieves a peak efficiency of 95.2% and maintains a high efficiency of above 92.3% across the full output power range. This electrolytic-free prototype ac-dc-ac converter for the online UPS achieves a power density of 26.4W/in$^3$.

## 1.4 THESIS ORGANIZATION

This remainder of this thesis is organized as follows: Chapter 2 presents a comprehensive design and control methodology for a single phase two stage universal input to 28V-output isolated ac-dc converter for electronic equipment. Chapter 3 introduces a new droop control strategy for paralleled operation of the isolated ac-dc converters proposed in Chapter 2 and demonstrates its effectiveness through experimental results. Chapter 4 presents the design and control of a single-phase single-stage ac-ac converter for LED lighting applications. Chapter 5 introduces a new two-stage ac-dc-ac converter for a single-phase transformer-less online uninterruptible power supply for use in data center application. Finally, Chapter 6 summarizes and concludes the thesis.

# CHAPTER 2

# TWO-STAGE ISOLATED AC-DC CONVERTER

Two-stage isolated ac-dc converters are used across a range of different applications. They are of particular interest in defense applications where they power a variety of different electronic loads. These loads comprise radars, radios, computing hardware, data storage equipment, etc., and are present in land-based, marine, and air-borne systems. In such systems, a 28-V dc-bus is present to power these electronic loads. This 28-V dc-bus is often regulated by ac-dc converters which draw electrical energy from the ac-line at the output of an electrical grid or ac-generators (in vehicles). In typical applications, the ac line voltage can vary across a range (nominally from $85V_{rms}$ to $260V_{rms}$) while the output of the ac-dc converter is kept stable at 28V.

High power density is essential performance metric for such power converters, mainly due to space and volume constraints. Moreover, reducing volume of a power converter presents thermal management challenges due to a smaller surface area for heat dissipation. Therefore, compact power converters need to be more efficient to prevent excessive increase in operating temperatures and to ensure safe operation. To address these needs, this chapter presents a high-power-density high-efficiency single-phase universal-input ($85V_{rms}$ - $260V_{rms}$) to 28V-output isolated ac-dc converter module. The proposed converter utilizes two-stages: a totem-pole bridgeless boost power-factor correction (PFC) converter stage and an isolated LLC resonant dc-dc converter stage. A comprehensive design methodology is presented, which compares various designs and operating modes for the power stages of the converter module and selects the optimal design based on the overall efficiency and power density. For the selected design, a control scheme is presented for the PFC stage to minimize current distortion by accounting for various sensor, control, and gate-drive delays while ensuring zero-voltage switching (ZVS) of the transistors. To validate the proposed design and control strategy, a 1-kW universal-input to 28-V isolated ac-dc converter module is built and tested. The prototype converter module achieves a high power density of $84W/in^3$ and a peak efficiency of greater than 93%. While the design process, control

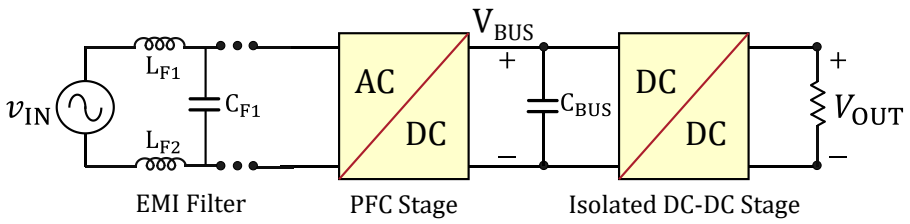



Fig. 2.1: Architecture of a two-stage isolated ac-dc converter.

strategies, and hardware validation in this chapter are presented for a 28V-output power converter, the highlighted challenges, and proposed design and control strategies are also applicable for power converters with output voltages at 48V, 24V, and 12V, which helps address a broad coverage of isolated ac-dc converter application space.

## 2.1 Architecture of a Two-Stage Isolated AC-DC Converter

The architecture of the proposed two stage ac-dc converter is shown in Fig. 2.1. It comprises a front-end totem-pole PFC ac-dc stage which is followed by an isolated dc-dc stage. The PFC stage converts the input ac line voltage to a 400-V dc-bus voltage while ensuring a high input power factor. A totem-pole bridgeless boost PFC stage is used because of its lower twice-line-frequency dc-bus capacitance requirement, which enables reduction in overall converter volume through utilization of high-energy-density electrolytic capacitors. Moreover, a bridgeless topology enables reduction in number of switches in inductor (input) current path, thereby reducing switch conduction losses and enabling high efficiency. The isolated dc-dc stage down-converts the 400-V dc-bus voltage to an output voltage of 28V. For this stage, an LLC resonant dc-dc converter is utilized because of its ability to maintain high conversion efficiency across a wide input voltage and output power range. Finally, an EMI filter is connected at the input of the PFC stage to attenuate switching noise generated by the PFC stage and prevent it from passing into the ac line. This is essential for meeting stringent EMI noise limits imposed by regulatory authorities.

TABLE 2.1: SPECIFICATIONS OF THE ISOLATED AC-DC CONVERTER

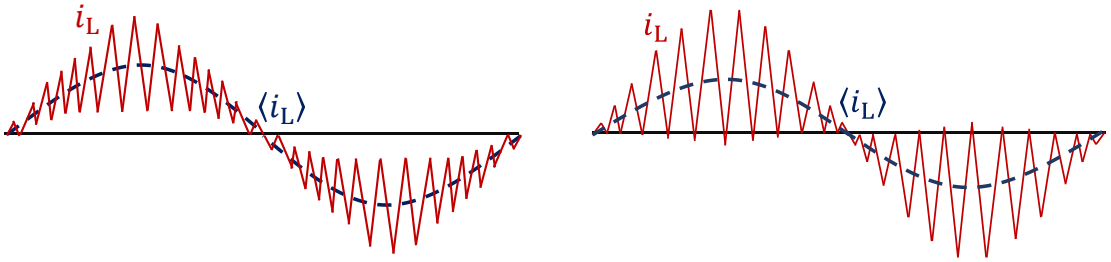
| | |
|---|---|
| Input Voltage | 85-260 $V_{rms}$ |
| Line Frequency | 47-63 Hz |
| Output Voltage | 28 $V_{DC}$ |
| Maximum Output Voltage Ripple | 560 $mV_{pk-pk}$ |
| Output Power | 1 kW |
| EMI Compliance | MIL-STD-461G (see Fig. 1.3) |

## 2.2 SYSTEM DESIGN AND OPTIMIZATION

To obtain a high-power-density and high-efficiency converter, a design and optimization methodology is presented. The design methodology co-optimizes the volume and efficiency of the ac-dc converter by optimally selecting the operating modes of the PFC stage and number of EMI filter stages across various operating modes (CCM vs. BCM) and switching frequencies. Moreover, a design approach for the LLC dc-dc stage is presented to maximize its efficiency by considering various topologies for its inverter and rectifier. For the overall ac-dc conversion system, all design optimizations are performed for the specifications listed in Table 2.1.

### 2.2.1 TOTEM-POLE BOOST PFC STAGE DESIGN:

For the design of the totem-pole boost PFC stage, two operating modes are considered: continuous conduction mode (CCM) and boundary conduction mode (BCM). A time-exaggerated view of the inductor current in both these operating modes is shown in Fig. 2.2. During CCM operation, the inductor current has smaller peak-peak ripple and rms value, but the PFC stage's switches would incur switching losses due to hard-switching. In the case of BCM operation, the PFC stage switches will achieve zero-voltage switching resulting in negligible switching loss, however, the inductor current ripple and its rms value will be higher. Therefore, the PFC stage design strategy accounts for the tradeoffs associated with both operating modes. Moreover, the choice of PFC stage's operating mode also influences the required




(a) (b)

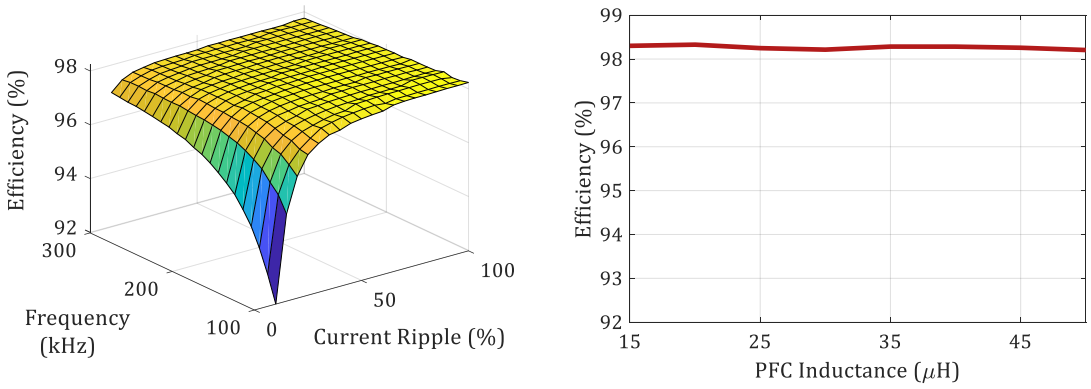
Fig. 2.2: Time exaggerated view of the instantaneous inductor current (solid red line) and average inductor current (dashed blue line) while the PFC stage is operating under (a) Continuous conduction mode (CCM), and (b) Boundary conduction mode (BCM).

attenuation by the input EMI filter and affects its volume and efficiency. Therefore, the design strategy incorporates both the design of the input EMI filter and the PFC stage to achieve the overall optima in terms of efficiency and volume for the EMI filter and the PFC stage. As specified in Table 2.1, the ac-dc converter needs to adhere to MIL-STD 461G EMI regulations. Therefore, the EMI filter design accounts of the noise limits specified in solid-blue line on Fig. 1.3.

For the CCM operation, the optimization is performed across switching frequency and PFC inductor current ripple, which in-turn determines the PFC inductance and the EMI filtering requirements. For BCM operation, the optimization is performed across PFC inductance value, which in-turn determines the operating frequency range of the PFC stage and EMI filtering requirements. For the input EMI filter, single and multi-stage (2, 3, and 4 stage) EMI filters are considered. For the efficiency estimation of the PFC stage, detailed loss models are developed which estimate winding and core losses in the EMI filter

TABLE 2.2: DESIGN SPACE FOR CONTINUOUS CONDUCTION MODE (CCM) AND BOUNDARY CONDUCTION MODE (BCM) OF THE PFC STAGE

| | | |
|---|---|---|
| CCM | Operating Frequency | 100kHz -300kHz |
| | Peak Inductor Current Ripple | 15% - 100% |
| BCM | Inductance | 15µH - 50µH |




(a) (b)

Fig. 2.3: Predicted efficiencies of the PFC stage and EMI filter under (a) Continuous conduction mode (CCM) operation, (b) Boundary conduction mode (BCM) operation.

and PFC inductors, and switching and conduction losses in the PFC switches. Finally, a design space is defined for each of the above-mentioned operating modes and is shown in Table 2.2. To only consider design with inductor volume below a maximum limit, the minimum CCM operating frequency is kept at 100kHz and the maximum PFC inductance for the BCM operation is kept at 50µH. Furthermore, to limit the switching losses in the devices, the maximum CCM operating frequency is limited to 300kHz. Moreover, owing to the limitation of sensing circuitry and digital controller, the maximum operating frequency for BCM operation is limited to 1 MHz, and therefore the minimum inductance in the soft-switched design is kept at 15µH.

The results of the optimization are shown in Fig. 2.3. Fig. 2.3(a) shows the estimated efficiency of the converter for the CCM design across the range of switching frequency and inductor current ripple specified in Table 2.2. As can be seen from Fig. 2.3(a), the CCM designs with lower peak current ripple and operating frequencies have lower efficiencies. This is due to the higher PFC inductance requirement for such low current ripple values which leads to higher winding losses for a given maximum volume limit on the PFC inductor. Fig. 2.3(b) shows the efficiency for the BCM design across the PFC inductance range specified in Table 2.2.

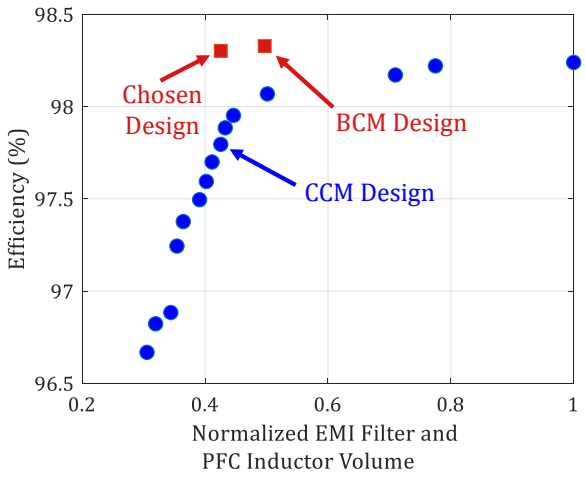



Fig. 2.4: Pareto-optimal designs for the two operating modes of the PFC stage.

The efficiency of the PFC stage remains relatively flat as a function of PFC inductance. This is due to the reason that the optimization process selects a different inductor core for each of the designed inductances while still ensuring that the height of the PFC stage and EMI filter does not exceed the maximum limit (to preserve a high power density). Finally, for each of these operating modes (CCM and BCM), the resultant volumes of the EMI filter and PFC inductance are computed, and the pareto-optimal designs are shown in Fig. 2.4. As can be seen, the pareto-optimal designs exhibit a tradeoff between efficiency and passive volume of the PFC stage and BCM designs tend to have smaller volume and better performance as compared to the CCM designs for the design specifications listed in Table 2.1. Therefore, BCM operation is chosen for final implementation of the PFC stage with a PFC inductance of 15µH.

### 2.2.2 LLC DC-DC Stage Design:

The dc-dc stage of the isolated ac-dc converter needs to step down the 400-V dc-bus voltage to 28V required by the load. For the LLC dc-dc stage optimization, various inverter and rectifier topologies are considered as shown in Fig. 2.5 and 2.6, respectively. For each of these inverter and rectifier combinations, the resonant tank is designed based on the optimization methodology presented in [117]. During the design process, only GaN transistors are considered for the inverter switches owing to their

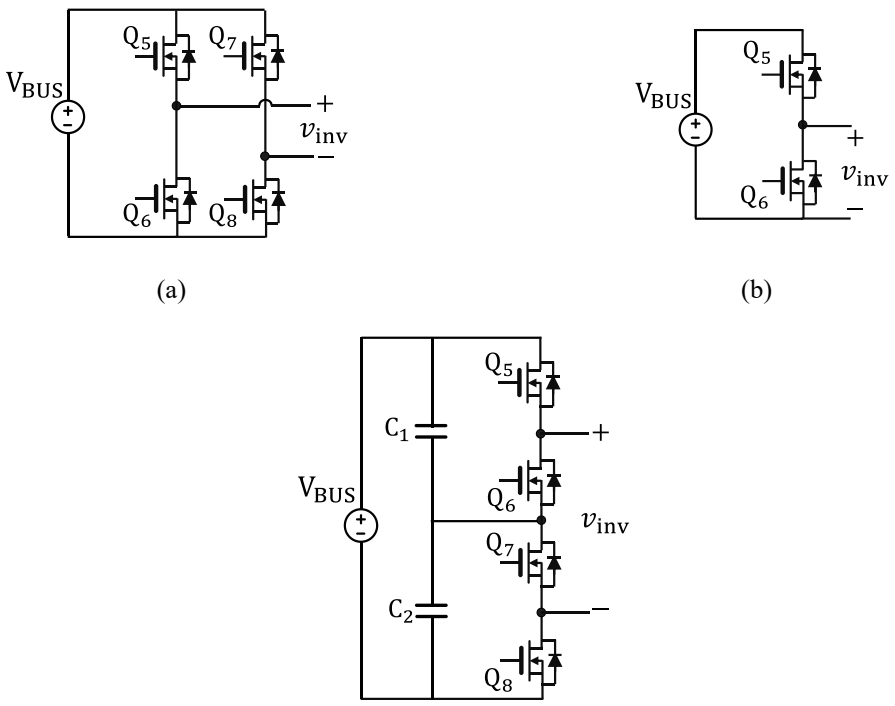



Fig. 2.5: Inverter circuit topologies considered for design of the LLC dc-dc stage: (a) Full-bridge inverter, (b) Half-bridge inverter, and (c) Variable frequency multiplier (VFX).

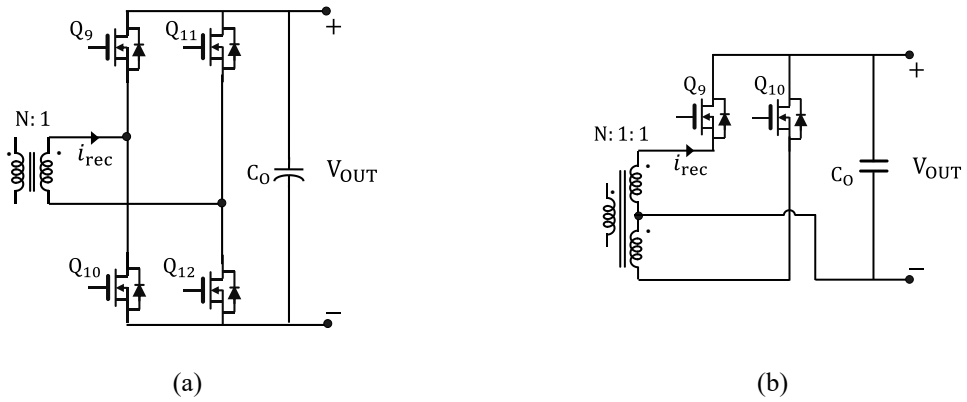
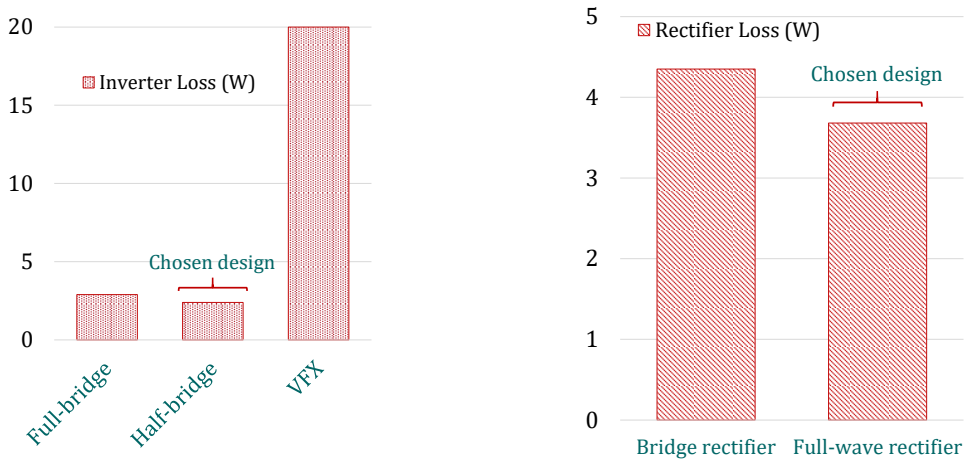



Fig. 2.6: Rectifier circuit topologies considered for design of the LLC dc-dc stage: (a) Bridge rectifier, (b) Full-wave rectifier.

lower output capacitance compared to Si-MOSFETs. This facilitates ZVS with minimal circulating currents, thereby reducing conduction losses in the inverter switches and winding losses in the LLC transformer and resonant inductor. Moreover, this enables higher switching frequency operation of the




(a) (b)

Fig. 2.7: Losses in the LLC resonant dc-dc converter while converting a 400-V dc-bus voltage to 28-V output voltage to power a 1-kW load: (a) Inverter losses, (b) rectifier losses.

LLC dc-dc stage and therefore the LLC dc-dc stage is designed to operate across a switching frequency range of 300kHz to 1MHz.

For the LLC inverter, three topologies were considered as shown in Fig. 2.5. A full-bridge inverter topology is shown in Fig. 2.5(a). Each half-bridge leg in this topology operates at 50% duty ratio and out of phase with each other. This produces a square-wave at the input of the LLC resonant tank with voltage in the range of $+V_{BUS}$ and $-V_{BUS}$. For the converter specifications listed in Table I, a half-bridge inverter can also be utilized and is shown in Fig. 2.5(b). This inverter operates with a 50% duty ratio generating a square-wave voltage in the range of $+V_{BUS}$ and 0 at the input of the resonant tank. This results in a natural step-down of the dc-bus voltage by a factor of two as compared to the full-bridge inverter and reduces the step-down burden on the LLC dc-dc stage. Moreover, this topology has one switch in series with the tank current which can lead to a lower overall conduction loss in the LLC dc-dc stage. Fig. 2.5(c) shows a variable-frequency-multiplier (VFX) topology for LLC inverter [118],[119]. This topology utilizes two stacked capacitors at the input with a half-bridge connected across each capacitor. With appropriate control of the switches, the voltage across each half-bridge is reduced by a factor of two, thereby allowing low voltage rated switches to be used. Moreover, the

inverter topology provides a step-down of the dc-bus voltage by a factor of two as compared to the half-bridge inverter (factor of four if compared with full-bridge inverter). This further reduces the step-down burden on the LLC dc-dc stage and its transformer. However, the topology requires two switches to come in series with the resonant tank current which can increase the overall conduction loss. To estimate the efficiency of the LLC dc-dc stage, conduction losses are computed for each of these inverter implementations and are summarized in Fig. 2.7(a) for the best-in-class commercially available GaN transistors. As can be seen from the figure, the half-bridge inverter results in the lowest overall inverter loss. Therefore, the half-bridge inverter topology is chosen for final LLC dc-dc stage implementation.

Similarly, two topologies are considered for the LLC rectifier as shown in Fig. 2.6. Fig. 2.6(a) shows a bridge rectifier comprising four switches with switches $\mathrm{Q}_9$ and $\mathrm{Q}_{12}$ operating in-phase and switches $\mathrm{Q}_{10}$ and $\mathrm{Q}_{11}$ operating in-phase, depending on the direction of rectifier input current $i_{\mathrm{rec}}$. A full-wave rectifier topology is also considered for the proposed converter and is shown in Fig. 2.7(b). This topology utilizes two switches, each blocking twice the voltage as compared to the switches in full-bridge rectifier. This type of rectifier also requires a dual-secondary center-tapped winding architecture of the LLC transformer where each secondary winding only conducts during a half switching period of the LLC dc-dc stage.

Based on the specifications of the LLC dc-dc stage, the losses for each of these rectifier topologies are then computed and compared. Moreover, while designing the rectifiers, several GaN transistors and Si-MOSFETs were considered and the type of device with the best overall performance was used for loss analysis. Based on this analysis, it is observed that Si-MOSFETs result in better performance because of their lower on-state resistance, lower source-drain forward voltage drop (0.9V vs. 1.5V), and better thermal characteristics for both rectifier topologies. A summary of the losses in both rectifier topologies is shown in Fig. 2.7(b). The full-wave rectifier implementation shown in Fig. 2.6(b) is found to be the most efficient among the two rectifier topologies and is therefore chosen for final LLC

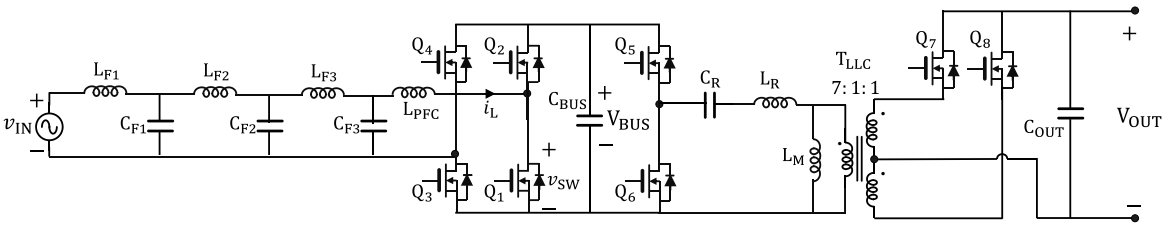



Fig. 2.8: Topology of the isolated ac-dc converter.

implementation. The optimal LLC implementation comprises a half-bridge inverter and a full-wave rectifier. The final topology of the end-to-end isolated ac-dc converter is shown in Fig. 2.8.

## 2.3 PFC CONTROLLER IMPLEMENTATION

A digital controller based boundary conduction (BCM) mode control is utilized for the soft-switched totem-pole boost PFC stage. To ensure BCM operation of the PFC stage, a zero-current detection (ZCD) circuit is utilized which generates a trigger when the inductor current crosses the zero-current mark. The trigger is sensed by the controller to turn-off the synchronous switch ($Q_1$ when input voltage is positive, and $Q_2$ when input voltage is negative, according to circuit illustrated in Fig. 2.8) and start the next switching cycle. In an ideal case, when ZCD sensor, control, and gate drive delays are negligible, the inductor current resembles a waveshape as shown in Fig. 2.2(b). In this case, the PFC stage's high-frequency switches ($Q_1$ and $Q_2$) naturally achieve ZVS when inductor current is brought to zero at the end of the switching period and input voltage $v_{IN}$ satisfies $v_{IN} < V_{BUS}/2$. However, for input voltages greater than $V_{BUS}/2$, the synchronous switch ($Q_2$ when input voltage is positive and $Q_1$ when input voltage is negative) needs to be kept on for an additional duration of time beyond the zero-crossing of the instantaneous inductor current to allow inductor current to build to a minimum value given by:

$$i_{ZVS} \leq -\sqrt{\frac{2C_{OSS}}{L_{PFC}} V_{BUS}(2|v_{IN}| - V_{BUS})}. \tag{2.1}$$

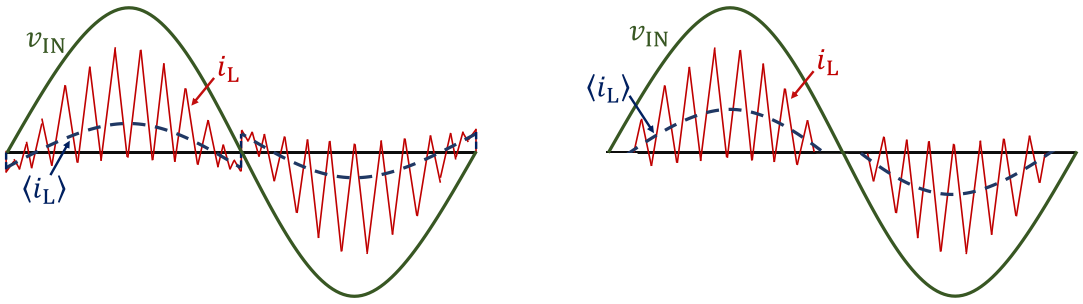
Here, $C_{OSS}$ is the output capacitance of the boost switches, $L_{PFC}$ is the PFC inductance, $V_{BUS}$ is the instantaneous dc-bus voltage, and $v_{IN}$ is the instantaneous input voltage [120],[121]. Given this

constraint, the ZCD circuit trigger is set such that the boost switches achieve full ZVS across the entire input voltage line cycle.

In practice, a delay is also present in the ZCD circuit, digital controller, and gate drive. This delay results in an extra build-up of reverse current flowing through the inductor than is required to achieve ZVS. This extra inductor current is given by:

$$i_{\text{extra}} = -\frac{V_{BUS}-|v_{IN}|}{L_{PFC}}\, T_{\text{delay}}, \tag{2.2}$$

where, $T_{\text{delay}}$ is the cumulative sensor, control, and gate drive delay. As is evident from (2.2), the effect of this delay is most prominent when input voltage is low since the voltage across the PFC inductor is highest. If this delay is ignored during the design of BCM controller, it causes the average inductor current to fall, as illustrated in Fig. 2.9(a) [122]. As can be seen from the figure, at instantaneous input voltage magnitudes below a certain value, the product of input voltage $v_{\text{IN}}$ and input current $\langle i_{\text{L}} \rangle$ is negative and the instantaneous input power is being transferred back towards the input voltage source increasing circulating currents and causing higher conduction losses. To mitigate this effect, the PFC converter is generally switched-off at such low input voltages introducing dead-bands in the inductor current. Fig. 2.9(b) shows the inductor current $i_{\text{L}}$ and its average value $\langle i_{\text{L}} \rangle$ in the presence of such dead-




(a) (b)

Fig. 2.9: Time exaggerated view of PFC stage's inductor current $i_{\text{L}}$ and its average value $\langle i_{\text{L}} \rangle$ while it is operating under boundary conduction mode: (a) in the presence of sensor, control, and gate drive delays, and (b) when dead-bands are introduced at low input voltages causing distortion in the input current waveshape.

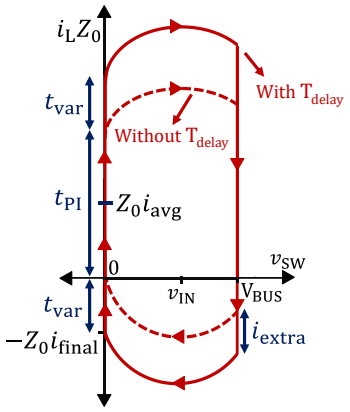



Fig. 2.10: State-plane diagram of a boost converter without any delays $T_{delay}$ (dotted red line) and in the presence of delays $T_{delay}$ with the proposed PFC control strategy (solid red line). Here $Z_0$ is given by $\sqrt{\frac{L_{PFC}}{2C_{OSS}}}$ and $i_L$ and $v_{SW}$ are state parameters.

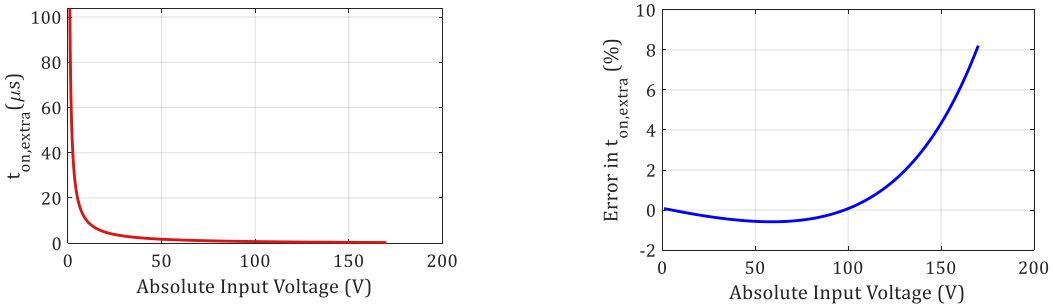
bands. As can be seen, these dead-bands introduce distortion in the input current waveshape and consequently affect the input current THD and power factor.

To preserve a good input current waveshape and to improve the input power factor in the presence of such delays, a new PFC control strategy is also presented. The new PFC control strategy considers the delays and the resultant extra inductor current in the PFC inductance $i_{extra}$ and based on this information, computes the on-time for the boost main switch ($Q_1$ when input voltage is positive and $Q_2$ when input voltage is negative). Fig. 2.10 shows the state plane diagram of the inductor current and the switch-node voltage for a boost converter. As can be seen, in the presence of delays $T_{delay}$, an additional on-time given by $t_{on,extra} = 2 \times t_{var}$ is needed to maintain the average inductor current at its required value. This additional time ($t_{on,extra}$) is a function of input and dc-bus voltages as well as PFC circuit resonant parameters and is given by:

$$t_{on,extra} = \frac{2\sqrt{2L_{PFC}C_{OSS}}}{|v_{IN}|}\sqrt{V_{BUS}^2 - 2V_{BUS}|v_{IN}| + \frac{i_{min,B}^2 L_{PFC}}{2C_{OSS}}}, \tag{2.3}$$

where $i_{min,B}$ is given by:

$$i_{min,B} = |i_{extra}| + |i_{ZCD}|, \tag{2.4}$$




(a) (b)

Fig. 2.11: Compensation needed to mitigate the effect of sensor, control, and gate drive delay, $T_{delay}$ , when operating at an input voltage of $120V_{rms}$ and a dc-bus voltage of 400V: (a) Extra on-time required to restore input current waveshape, (b) Percentage error between the exact and curve-fitted extra on-time for the PFC stage for $\alpha = 104\mu Vs$ and $\beta = 327ns$.

where, $i_{ZCD}$ is the current level at which the ZCD circuit is configured to generate a trigger. Fig. 2.11(a) shows the extra on-time $t_{on,extra}$ required to maintain the input current waveshape, while the PFC stage is operating at $120V_{rms}$ and the dc-bus is regulated at 400V. As can be seen from the figure, $t_{on,extra}$ varies inversely with the input voltage. Accurately computing this additional on-time $t_{on,extra}$ based on equation (2.3) will substantially increase the controller computational overhead which will affect the control complexity.

To overcome this hurdle, this sub-section presents a simpler implementation for this additional on-time based on a curve-fit approximation. The curve-fit utilized is of the form $t_{on,extra} \approx \alpha/v_{IN} + \beta$, where the constants $\alpha$ and $\beta$ can be found by curve fitting the on-time plot of Fig. 2.12(a). Fig. 2.12(b) shows the error between the actual and curve-fitted $t_{on,extra}$ values. As can be seen, the percentage error remains below 8.5% across the full input voltage line cycle. Also, the error remains below 1% at low voltage values (near zero crossing of the input voltage where the effect of delay $T_{delay}$ is most prominent), resulting in negligible difference between actual and curve fitted $t_{on,extra}$ values. The overall control architecture of the PFC stage is summarized in Fig. 2.12. As can be seen, the effective

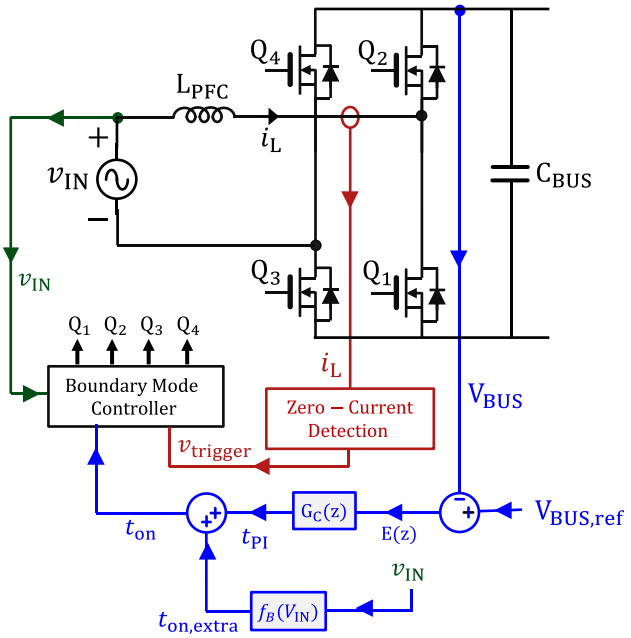


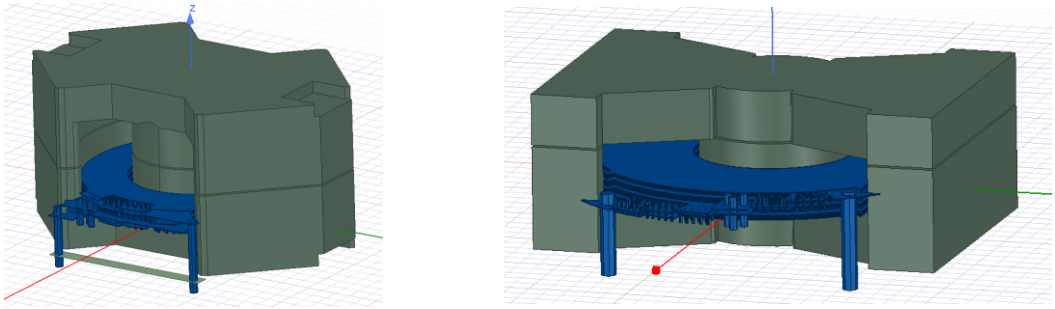

Fig. 2.12: Proposed control architecture for the totem-pole boost PFC stage.

on-time of the main switch is given by $t_{\text{on}} = t_{\text{PI}} + t_{\text{on,extra}}$. Here, $t_{\text{PI}}$ regulates the output power of the PFC stage and is generated by a low-bandwidth dc-bus voltage control loop and $t_{\text{on,extra}}$ helps maintain the waveshape of the average input current by compensating for sensor, control, and gate drive delay ($T_{\text{delay}}$).

## 2.4 Prototype Design and Experimental Results

A 1-kW prototype ac-dc converter, based on the specifications of Table 2.1, utilizing the optimized design and proposed control schemes is built and tested. A photograph of the prototype is shown in Fig. 2.13. The prototype converter achieves an overall power density of 84W/in$^3$. The converter utilizes low-profile magnetic cores with planar winding to implement the PFC inductor and LLC transformer as shown in Fig. 2.14. The magnetics design is optimized in a 3D finite-element-modelling (FEM) software (Ansys HFSS) to maximize efficiency. The PCB stack-up for the planar magnetics is shown in Fig. 2.15. A 4 oz. copper eight-layer PCB is utilized to implement 7 turns of the PFC inductor and two 4 oz. copper eight-layer PCBs are used to implement the interleaved primary and secondary turns of the LLC


Fig. 2.13: Photograph of the prototype 1-kW universal-input to 28V-output isolated soft-switched ac-dc converter which achieves a power density of 84W/in$^3$.



(a) (b)

Fig. 2.14: 3-D images of magnetics used in the proposed ac-dc converter: (a) PFC inductor utilizing a planar RM core, (b) LLC transformer utilizing a modified PQ core.

transformer as shown in Fig 2.15(a) and Fig. 2.15(b), respectively. A 200-MHz 32-bit digital controller is utilized to implement the closed-loop control in the PFC and the LLC dc-dc stage of the converter. The ZCD circuitry used to ensure BCM operation in PFC controller is shown in Fig. 2.16. The circuit utilizes a current sense resistor in series with the PFC inductor. The voltage drop across this resistor is amplified using a high-bandwidth voltage amplifier circuit and the output of the amplifier is fed to high-speed comparators to generate two triggers when the inductor current crosses zero. Each trigger is

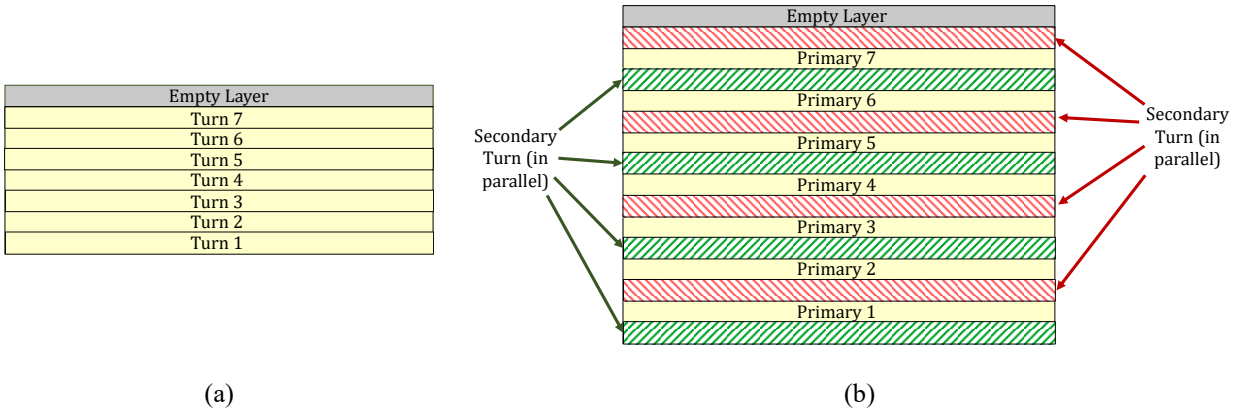



Fig. 2.15: PCB stack-up for the planar magnetics: (a) Planar PCB to implement 7 turns of PFC inductor, (b) Planar PCB to implement 7:1:1 turns ratio in LLC transformer.

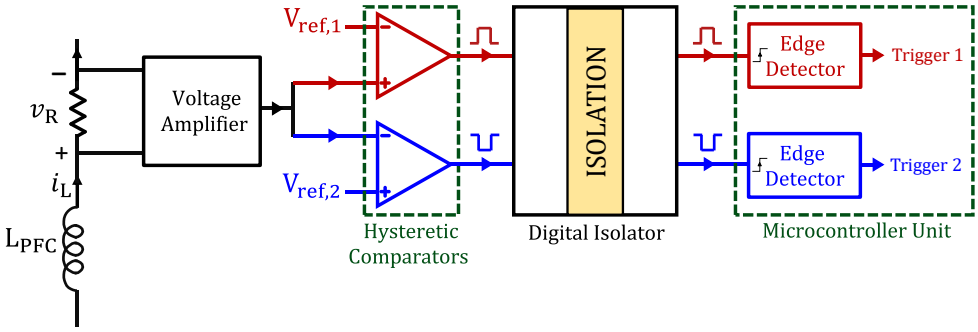



Fig. 2.16: Zero-current detection circuit used to ensure BCM operation of the PFC stage.

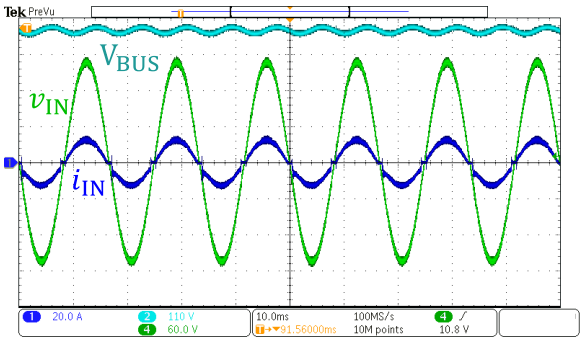
utilized in either the positive or negative half-line cycle of the input ac voltage and resets the PWM counter in the digital controller. Further details about the components used in the prototype ac-dc converter are listed in Table 2.3.

Fig. 2.17 shows the experimentally measured steady-state waveforms of the ac-dc converter. As can be seen from Fig. 2.17(a), the input current is sinusoidal and in-phase with the input voltage and dc-bus voltage is regulated at 400V validating the operation of the PFC controller. Figure 2.17(b) shows the zoomed-in steady-state waveform of the ac-dc converter. As can be seen in the figure, the inductor current crosses zero in each switching cycle verifying BCM operation of the PFC stage. Moreover, the output voltage of the LLC dc-dc stage is regulated at 28V validating the end-to-end operation of the ac-dc converter.

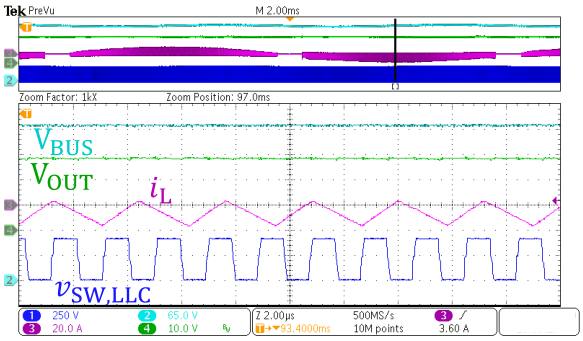
TABLE 2.3: COMPONENTS USED IN THE PROTOTYPE ISOLATED AC-DC CONVERTER

| Component | Value | Description |
|---|---|---|
| $C_{F1}, C_{F2}, C_{F3}$ | 1μF | 275-V Polypropylene X2 film capacitor |
| $L_{F1}, L_{F2}, L_{F3}$ | 11μH | Magnetics Inc.<br>125u core, 20 turns |
| $S_1, S_2, S_5, S_6$ | – | 650-V, 60-A<br>GaN E-HEMT |
| $S_3, S_4$ | – | 600-V, 75-A<br>Si MOSFET |
| $S_7, S_8$ | – | 80-V, 300-A<br>Si MOSFET |
| $L_{PFC}$ | 15μH | RM-14 EPCOS N49<br>(7 turns) |
| $L_R$ | 3.1μH | RM-10 EPCOS N49<br>(3 turns) |
| $L_{LLC}$ | 31μH | LLC transformer magnetizing inductance ($T_{LLC}$) |
| $T_{LLC}$ | 7:1:1 | PQ-32/20 EPCOS N49 |
| $C_{BUS}$ | 390μF | 450-V Aluminum electrolytic capacitor |
| $C_R$ | 33nF | 630-V C0G/NP0 Ceramic capacitor |
| $C_{OUT}$ | 220μF | 50-V Aluminum electrolytic capacitor |

Fig. 2.18 shows the experimentally measured efficiencies of the proposed ac-dc converter as a function of output power. Fig. 2.18(a) shows the efficiency of the PFC stage when it is converting a 120-Vrms, 60-Hz input ac voltage to a 400-V dc-bus voltage across the dc-bus capacitor while utilizing the proposed PFC control strategy. As can be seen, the PFC stage maintains a high conversion efficiency




(a)




(b)

Fig. 2.17: Experimentally measured steady-state waveforms of the converter: (a) Input voltage (60V/div), input current (20A/div), and dc-bus voltage of the PFC stage (110V/div), (b) DC-bus voltage (65V/div), PFC inductor current (20A/div), LLC switch-node voltage (250V/div), and LLC output voltage (10V/div), when a $120V_{rms}$ ac voltage is applied at the input of the converter.

of greater than 97% across a wide output power range and achieves a peak efficiency 97.4%. Fig. 2.18(b) shows the efficiency of the LLC dc-dc stage while it is converting a 400-V dc-bus voltage to a 28-V output voltage. The LLC dc-dc stage maintains an efficiency of greater than 96% across the majority of output power range and achieves a peak efficiency of 97%. The end-to-end efficiency of the proposed ac-dc converter is given in Fig. 2.18(c). As can be seen from the figure, the prototype converter maintains a high conversion efficiency of greater than 90% across 3:1 output power range and achieves a high peak efficiency of 93.3%.

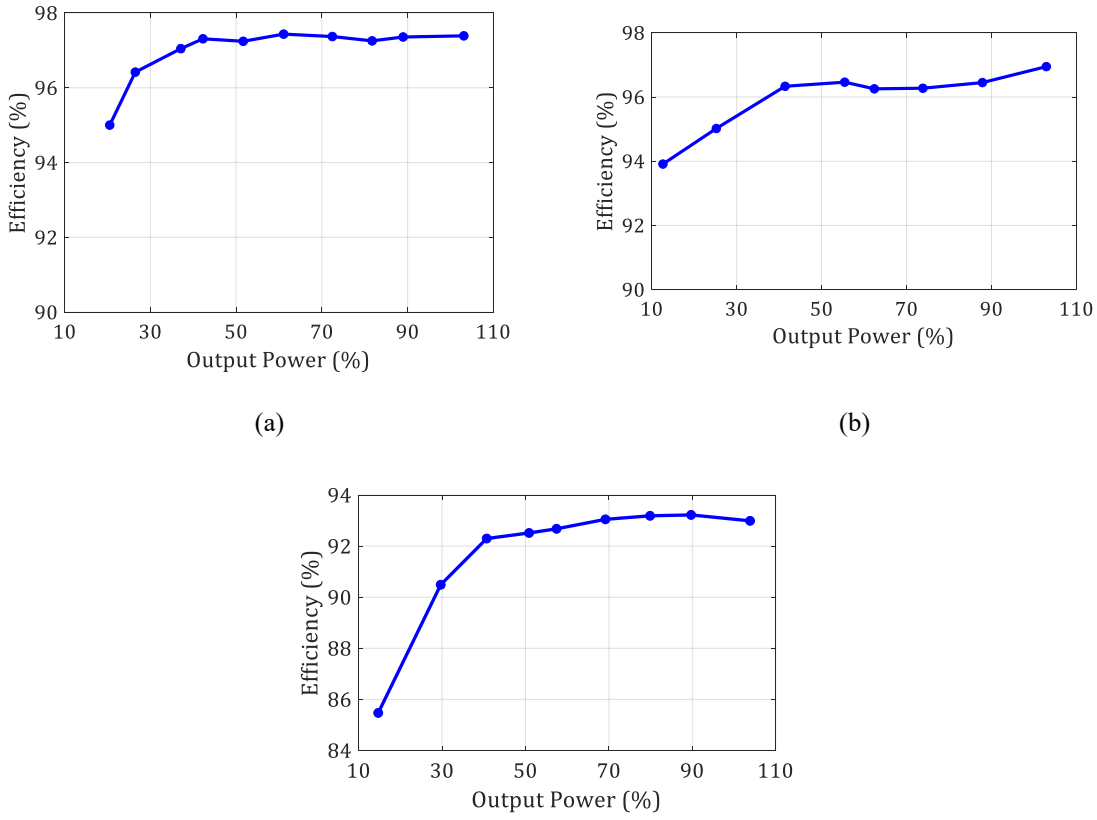
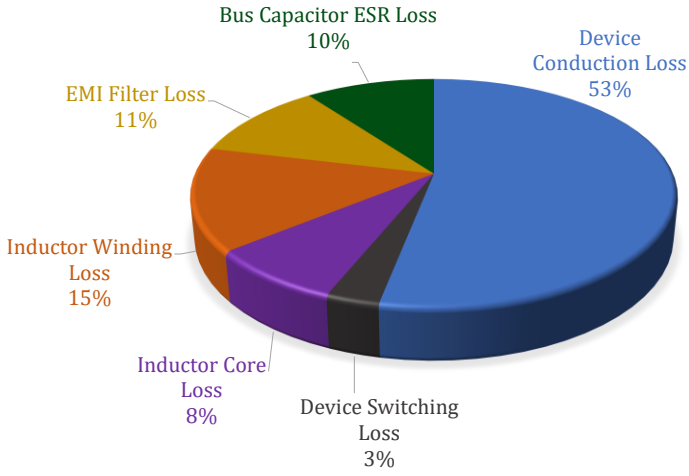
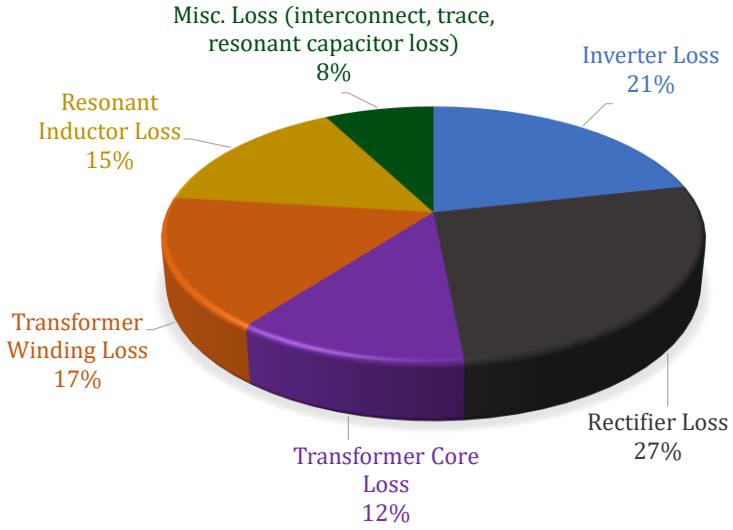



Fig. 2.18: Experimentally measured efficiencies of the proposed ac-dc converter as a function of output load: (a) PFC stage converting 120-$V_{rms}$, 60-Hz ac input voltage to a 400-V dc-bus voltage across capacitor $C_{BUS}$, (b) LLC dc-dc stage converting the 400-V dc-bus voltage to 28-V output voltage across the output load, (c) full end-to-end isolated ac-dc converter converting the 120-$V_{rms}$, 60-Hz ac input voltage to a 28-V output voltage across the load.

The power loss distribution of the PFC stage and LLC dc-dc stage while the proposed ac-dc converter is operating at an input ac voltage of 120$V_{rms}$, nominal dc-bus voltage of 400V, output dc voltage of 28V, and output power of 1kW is shown in Fig. 2.19(a) and Fig. 2.19(b), respectively. As can be seen, the dominant loss mechanism of PFC stage operating in BCM is the device conduction loss in switches $Q_1 - Q_4$. The other dominant loss mechanisms are winding and core losses in PFC inductor, losses in the EMI filter, and ESR losses in the dc-bus capacitor, in decreasing order. There is also a




(a)




(b)

Fig. 2.19: Detailed loss breakdowns of: (a) PFC stage, and (b) LLC dc-dc stage based on the theoretical loss models when the proposed ac-dc converter is operating at an input ac voltage of $120V_{rms}$, nominal dc-bus voltage of 400V, output dc voltage of 28V, and output power of 1kW.

slight turn-off loss in the PFC stage switches which results in some device switching loss. In the LLC dc-dc stage, the dominant loss mechanisms are the winding and core losses in the transformer. This is followed by the losses in rectifier switches $Q_7 - Q_8$, and inverter switches $Q_5 - Q_6$, winding and core

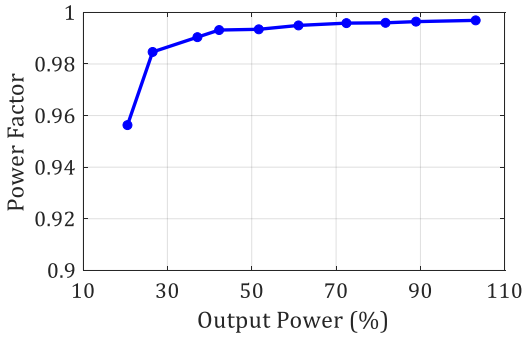



Fig. 2.20: Experimentally measured input power factor of the proposed ac-dc converter as a function of output power when a 120-$V_{rms}$ 60-Hz ac input voltage is converted to a 28-V dc output voltage.

losses in the resonant inductor, and losses in planar PCB interconnects, PCB traces, and the resonant capacitor, in decreasing order.

The input power factor of the ac-dc converter is also measured experimentally and is shown in Fig. 2.20. The converter maintains a high input power factor above 0.98 across 4:1 output power range and achieves a near-unity input power factor of 0.997 at the rated output power of 1kW. Hence, the experimental data validates the efficacy of the proposed control strategy and verifies the PFC operation of the ac-dc converter.

## 2.5 Chapter Summary

This chapter presents a high-power-density high-efficiency soft-switched single-phase universal-input to 28V-output isolated ac-dc converter module. The proposed two-stage converter utilizes a totem-pole bridgeless boost power-factor correction stage followed by an isolated LLC resonant dc-dc stage. A new comprehensive design methodology is presented which compares various designs and operating modes for the converter modules' power stage and selects the optimal design based on overall power density and efficiency. For the selected design, a control scheme is presented for the PFC stage to minimize current distortion by accounting for various sensor, control, and gate-drive delays while ensuring zero-voltage switching (ZVS) of the transistors. To validate the proposed design and control

strategy, a 1-kW universal-input to 28V-output isolated ac-dc converter is built and tested. The prototype converter achieves a high power density of 84W/in$^3$ and a peak efficiency of greater than 93%.

# CHAPTER 3

# PARALLELED AC-DC CONVERTERS

As power conversion applications continue to evolve, the power requirements for each application also vary. A power converter design approach focusing on meeting a certain power level for one specific application though results in high system-level performance but consumes substantial engineering resources. Moreover, producing such power supplies in low volume often increases component costs and introduces manufacturing complexities. An alternate design approach for power converter design is to develop modular power converters, which can be operated together to meet higher-than-rated output power. In this design approach, a single module (represented as a block) is designed to operate in parallel with other similar modules to power a common output load, as shown in Fig. 3.1. This allows for a single module design to be used across a range of different power levels (and applications) which encourages high-volume design and achieves substantial reduction in manufacturing costs through economies of scale. Moreover, it also decreases design effort to meet each specific application requirement individually, which minimizes engineering and manufacturing times.

Apart from its benefits in manufacturing, modular systems also result in improved fault tolerance and reliability due to higher system redundancy [48],[49]. In such systems, if a single module fails, the

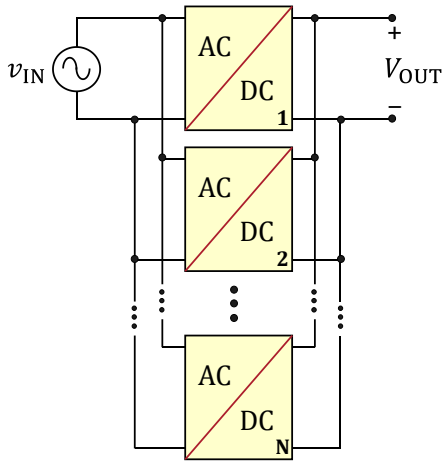



Fig. 3.1: A modular ac-dc conversion system comprising N identical ac-dc converter modules.

output power delivery is undisrupted because other modules can still operate normally. This is essential in critical applications i.e., medical, defense, emergency lighting, etc., where uninterrupted operation of the system is vital.

To achieve parallel operation, the output current of each module needs to be identical to achieve even distribution of stresses across the whole power conversion system. Parallel control architectures are broadly categorized into centralized control architectures and decentralized control architectures, as shown in Fig. 3.2. Centralized control architectures utilize a master controller which monitors the output power of each converter module to enable equal output current distribution, as shown in Fig. 3,2(a). Due to presence of a single master controller in centralized control architectures, a single fault in sensing or control circuitry in the master controller can disrupt the operation of the whole system which lowers the overall system reliability. Moreover, as each paralleled module needs to relay its sensor data to the master controller, the system design and control complexity increases with the number of paralleled modules, which introduces further challenges.

On the contrary, decentralized control architectures (shown in Fig. 3.2(b)) utilize autonomous power converter modules which are programmed to automatically achieve equal output current distribution without any master controller, when operated in parallel. Decentralized control architectures utilize droop control approach which vary the output voltage of each converter module based on its instantaneous output current. Though, the decentralized control approach results in slight variation in output voltage, its advantages in terms of better system robustness and ability for a 'plug-and-play' design approach makes it a popular control strategy for paralleled systems.

This chapter presents two decentralized (droop) control strategies for the secondary (LLC) dc-dc conversion stage of a two-stage isolated ac-dc converter, to enable equal output current distribution when powering a common output load. The control strategies are evaluated on the ac-dc converter discussed in Chapter 2. The first droop control strategy utilizes a conventional output current based control law while the second droop control strategy utilizes a new input-current-based control approach.

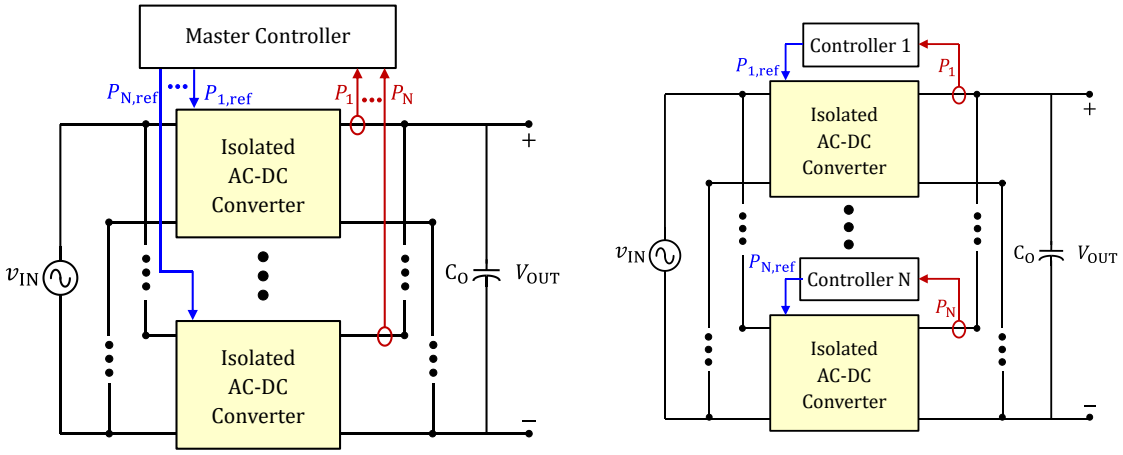



Fig. 3.2: Types of parallel control architectures: (a) Centralized control architecture, (b) Decentralized control architecture.

Based on the implementation challenges associated with conventional (output-current-based) droop control, the new input-current-based droop control approach is shown to be more suited for use in isolated high-output-current converters. To validate the new droop control approach, two 1-kW universal input to 28V-output isolated ac-dc converter modules are designed, built, and tested. The prototype system achieves a current distribution error of less than 2% near the peak output power of 2kW while maintaining a high conversion efficiency of greater than 91% across a 3:1 output power range.

## 3.1 Conventional Output-Current-Based Droop Control Strategy

The architecture for the output-based control strategy is shown in Fig. 3.3. It comprises two control loops: an output-current-based droop control loop and an output voltage control loop. The output voltage control loop is designed to regulate the voltage across the load at the reference value fed into it by the droop control loop. The bandwidth of the voltage control loop is designed to meet the output voltage regulation requirements set by the application. Such requirements include the allowable voltage overshoot (and undershoot) during load step-down (and step-up), and the settling time. The output-current-based droop

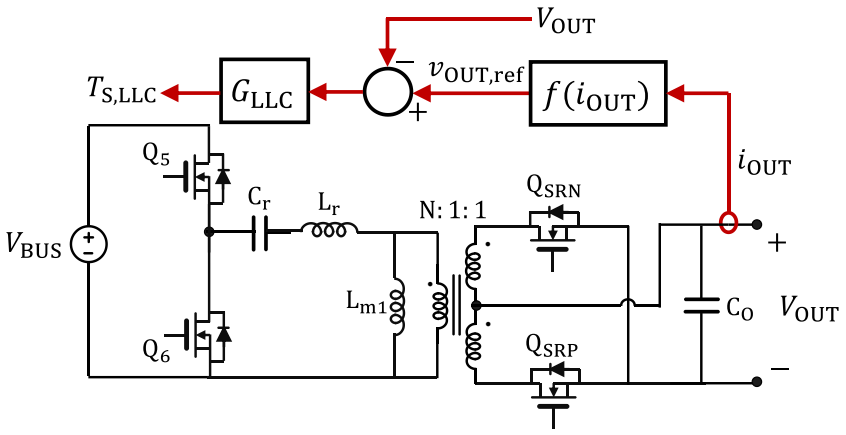



Fig. 3.3: Control architecture for output-current-based droop control strategy for use in LLC dc-dc converter.

control loop senses the output current of the converter module and generates a reference for the output voltage $v_{\mathrm{OUT,ref}}$ by utilizing the following control law:

$$v_{\mathrm{OUT,ref}}(t) = \mathrm{V_{OUT,max}} - i_{\mathrm{OUT}}(t)\mathrm{R_{droop}}, \tag{3.1}$$

where, $\mathrm{V_{OUT,max}}$ is the maximum output voltage corresponding to no-load at the output port, $i_{\mathrm{OUT}}(t)$ is the instantaneous output current, and $\mathrm{R_{droop}}$ is the virtual droop resistance given by:

$$\mathrm{R_{droop}} = \Delta\mathrm{V_{OUT}}/\Delta\mathrm{I_{OUT}}, \tag{3.2}$$

where, $\Delta\mathrm{V_{OUT}}$ is the maximum allowable variation in the output voltage (set by the application requirements), and $\Delta\mathrm{I_{OUT}}$ is the maximum variation in output current across the full output power range of a converter module. As can be seen from (3.1), if a module is delivering higher output current $i_{\mathrm{OUT}}$ than other modules in its parallel, its droop controller will reduce the voltage reference $v_{\mathrm{OUT,ref}}$ to its voltage control loop thereby limiting the amount of power being processed by the module. This shifts the power delivery burden to other parallel modules, which increases their output currents eventually enabling equal current (and output power) distribution in the system.

To implement this control strategy, an additional output current sensor is required. In high-power step-down isolated ac-dc power converters, the high output current is often challenging to sense. This is because of the power losses in the sensing circuitry, e.g., sensing resistor used in current-shunt monitors or primary

conductor present in hall effect sensors. To reduce these power losses, the resistance of current sense resistor or primary conductor is kept low which impacts the sensitivity of the sensor (in mV/A) [123]. Several techniques are employed to restore the sensitivity of the sensor while incurring low power losses, however, such techniques require additional amplification circuitry which increases cost of the sensor and its circuit complexity [123]-[126]. Moreover, to implement an output current based droop control using a digital controller on the primary side of the LLC transformer, the sensed output current information needs to be conveyed to the primary side. Therefore, an isolated current sensor is required which needs to meet the same isolation rating as the LLC transformer. This is especially pertinent if the isolated ac-dc converter is being designed for certain military or medical applications which require reinforced isolation, e.g., up to $5000V_{rms}$ in UL 1577. Therefore, using an isolated current sensor for output current based droop control in such applications further introduces implementation challenges and cost concerns for high-volume design.

### 3.2 Improved Input-Current-Based Droop Control Strategy

To overcome these challenges, a new LLC input-current based droop control strategy is proposed in this paper which estimates the magnitude of the output current of the LLC dc-dc stage by instead sensing its input current. This is beneficial as the input current is much lower in magnitude than the output current and therefore simpler current sensing techniques can be leveraged [123]. Also, the input current of the LLC dc-dc stage can be sensed with respect to the controller ground (located at the primary side of the LLC isolation transformer) by either using a simple current shunt sensor or low current hall effect sensor. Therefore, it does not interfere with above-specified isolation constraints. The control architecture for the proposed LLC input-current based droop control strategy is shown in Fig. 3.4. Based on this architecture, the output current of the LLC dc-dc stage is given by:

$$i_{\mathrm{OUT}}(t) = \frac{i_{\mathrm{IN,LLC}}(\mathrm{t})\eta_{\mathrm{LLC}}}{\mathrm{H}_{\mathrm{LLC}}}, \tag{3.3}$$

where $i_{\mathrm{IN,LLC}}(t)$ is the instantaneous input current, $\eta_{\mathrm{LLC}}$ is the efficiency, and $\mathrm{H}_{\mathrm{LLC}}$ is the conversion ratio of the LLC dc-dc stage given by $\mathrm{V}_{\mathrm{OUT,nominal}}/\mathrm{V}_{\mathrm{BUS,nominal}}$. The control law for the input current based

droop controller is given by:

$$v_{\mathrm{OUT,ref}}(t) = \mathrm{V_{OUT,max}} - \frac{i_{\mathrm{IN,LLC}}(\mathrm{t})\eta_{\mathrm{LLC}}}{\mathrm{H_{LLC}}} \cdot \mathrm{R_{droop}}. \tag{3.4}$$

The above-mentioned control law is adequate if the LLC dc-dc stage exhibits a constant conversion ratio i.e., if LLC is connected to a constant dc-bus voltage. However, in two-stage ac-dc converters a twice-line frequency voltage ripple appears across the dc-bus due to the PFC operation performed by the front-end PFC stage, as shown in Fig. 3.5(a). Since the LLC dc-dc stage is regulating its output voltage, its output power and hence its input power will be constant given the load impedance is unchanged. Consequently, any increase (or decrease) in the LLC dc-dc stage's input voltage (i.e., the dc-bus voltage $v_{\mathrm{BUS}}$) will result in a decrease (or increase) in the input current of the LLC dc-dc stage ($i_{\mathrm{IN,LLC}}$), as shown in Fig. 3.5(b). Since, the output voltage reference $v_{\mathrm{OUT,ref}}$, as given in (3.4), depends on the instantaneous value of the LLC input current $i_{\mathrm{IN,LLC}}$, any variation in $i_{\mathrm{IN,LLC}}$ will cause a similar variation in $v_{\mathrm{OUT,ref}}$. This phenomenon is shown in Fig. 3.5(c) in solid red line. The ripple in $v_{\mathrm{OUT,ref}}$ observed in Fig. 3.5(c) will also appear in the output dc voltage $\mathrm{V_{OUT}}$. Such a ripple is unacceptable in many point-of-load converters as most applications demand a stable output dc voltage with very small steady-state ripple. Moreover, in parallel operation, such a ripple in output voltage can cause currents to flow between modules resulting in

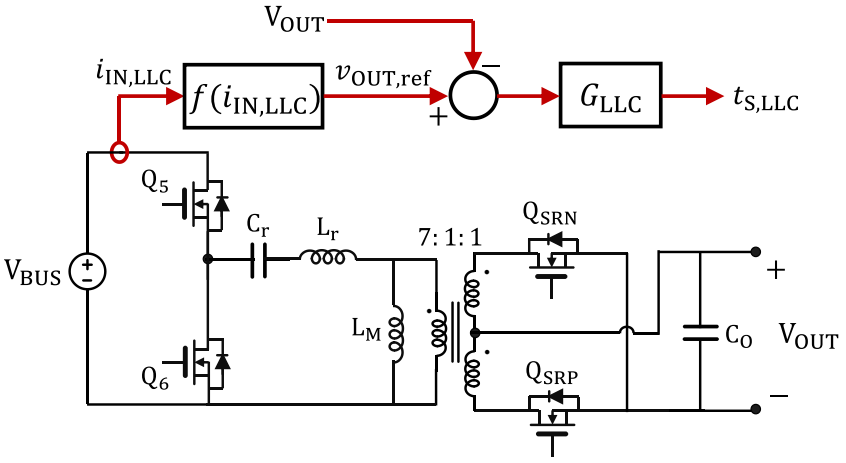



Fig. 3.4: Control architecture for input-current-based droop control strategy for use in LLC dc-dc converter.

increased circulating currents and related losses. To overcome this constraint, a variable droop resistance is utilized which varies in magnitude based on the instantaneous conversion ratio of the LLC dc-dc stage. This compensates for the twice-line frequency ripple in the input current of the LLC dc-dc stage and helps ensure a stable output dc-voltage. The variable droop resistance is given as follows:

$$r_{\mathrm{droop,var}}(t) = \frac{\eta_{\mathrm{LLC}} \mathrm{R}_{\mathrm{droop}} v_{\mathrm{BUS}}(t)}{v_{\mathrm{OUT}}(t)}, \tag{3.5}$$

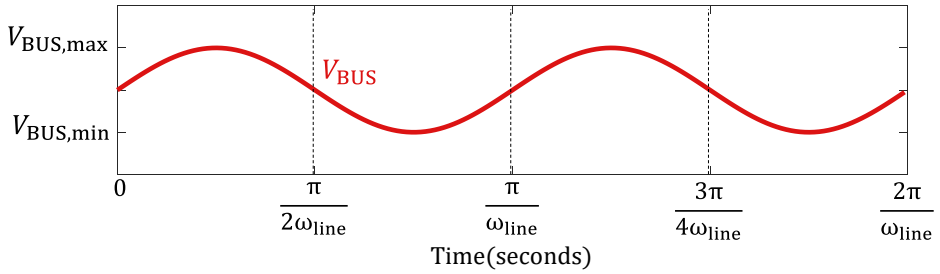
and the control law for the proposed droop control method is given below:

$$v_{\mathrm{OUT,ref}}(t) = \mathrm{V}_{\mathrm{OUT,max}} - i_{\mathrm{IN,LLC}}(t) \cdot r_{\mathrm{droop,var}}(t). \tag{3.6}$$

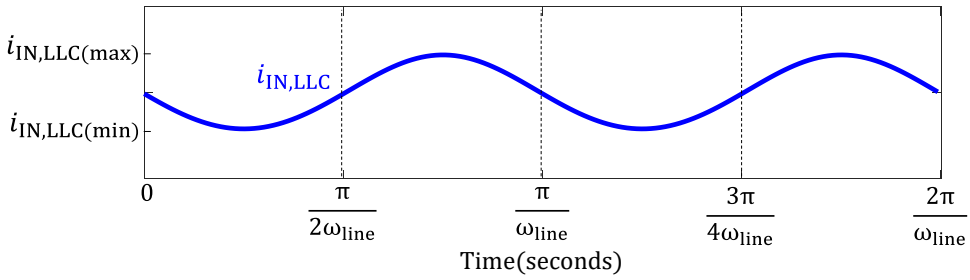
With the LLC dc-dc stage regulating the dc output voltage, any increase in the instantaneous dc-bus voltage will result in a decrease in the instantaneous input current of the LLC dc-dc stage. In such a case, with the proposed control law, the variable droop resistance will be increased by the same factor to cancel the effect of the reduced input current and result in a constant output voltage reference for the LLC output voltage control loop. On the contrary, a decrease in the dc-bus voltage will result in an increase in input current of the LLC dc-dc stage and a decrease in the variable droop resistance again leading to a constant output voltage reference. The dotted blue line in Fig. 3.5(c) shows the output voltage reference of the LLC dc-dc stage with the proposed variable droop resistance based control in the presence of the twice-line frequency ripple in the dc-bus voltage. As can be seen from Fig. 3.5(c), the proposed control strategy results in a constant voltage reference for the LLC output voltage control loop and hence eliminates the effect of the twice-line-frequency dc-bus voltage ripple to ensure a stable output voltage across the load.

## 3.3 Simulation of Droop Control Strategies

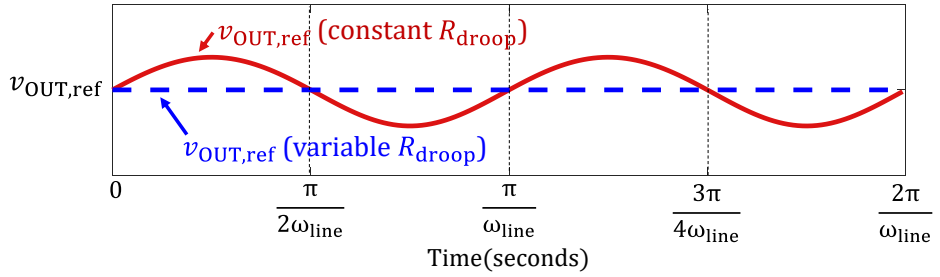
In order to validate the droop control strategies presented in the previous two sections, a simulation model of the power converter modules is built in PLECS. The simulation model verifies the operation of the paralleled modules by emulating component tolerances and temperature differences among




(a)




(b)




(c)

Fig. 3.5: Effect of twice-line-frequency dc-bus voltage ripple on the output voltage reference of the LLC dc-dc stage's input current based droop controller: (a) dc-bus voltage, (b) second-stage input current, and (c) output voltage reference with constant droop resistance (solid red line) and with proposed variable droop resistance (dotted blue line).

paralleled modules. Component tolerances are incorporated in simulation by varying circuit parameters i.e., capacitances, inductances, etc. in the simulation model, while the temperature differences are incorporated by varying on-resistances of the semiconductor switches. Fig. 3.6 shows the complete circuit diagram of the two-stage ac-dc converter (similar to one presented in Chapter 2) and Table 3.1

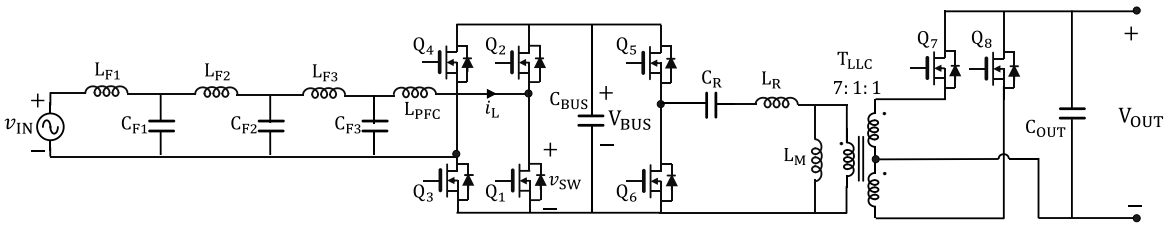



Fig. 3.6: Circuit model of the 1-kW two-stage ac-dc converter.

TABLE 3.1: PARAMETERS VARIED IN THE SIMULATION

| Parameter | Nominal Value | Tolerance |
|---|---|---|
| $L_{PFC}$ | 15μH | ±7% |
| $Q_{1,R_{DS},ON}$, $Q_{2,R_{DS},ON}$ | 25mΩ | ±10% |
| $Q_{3,R_{DS},ON}$, $Q_{4,R_{DS},ON}$ | 28mΩ | ±10% |
| $C_{BUS}$ | 440μF | ±10% |
| $Q_{5,R_{DS},ON}$, $Q_{6,R_{DS},ON}$ | 25mΩ | ±10% |
| $L_R$ | 3.1μH | ±5% |
| $C_R$ | 33nF | ±5% |
| $Q_{7,R_{DS},ON}$, $Q_{8,R_{DS},ON}$ | 1.4mΩ | ±10% |

shows the parameters varied in the simulation, their nominal values, and their tolerances. It is important to note that the transformer turns ratio is not accounted for in the simulation. This is because the transformer is built using a planar PCB which has very little tolerance associated with it. This is also experimentally verified, where two transformers are built, and their magnetizing inductance is measured. The measurements show the exact same magnetizing inductance of (32.3μH) as expected.

To verify the effect of connecting the LLC dc-dc converters in parallel, three simulation models are developed. In each simulation model three converters are connected in parallel to deliver a total

TABLE 3.2: PARAMETER VARIATION AMONG THREE LLC CONVERTERS TESTED IN SIMULATION

| Parameter | Parameter Value | | |
|---|---|---|---|
| | Converter 1 | Converter 2 | Converter 3 |
| $Q_{5,R_{DS,ON}}$, $Q_{6,R_{DS,ON}}$ | +10% | Nominal | -10% |
| $L_R$ | -5% | Nominal | +5% |
| $C_R$ | -5% | Nominal | +5% |
| $Q_{7,R_{DS,ON}}$, $Q_{8,R_{DS,ON}}$ | +10% | Nominal | -10% |

TABLE 3.3: RESULTS OBTAINED FROM SIMULATION OF THREE LLC CONVERTER IN PARALLEL

| Parameter | RMS Output Current $I_{OUT,rms}$ ($A_{rms}$) | | |
|---|---|---|---|
| | Converter 1 | Converter 2 | Converter 3 |
| Without Droop Control | 56.5 | 31.7 | 18.3 |
| With Output-Current-Based Droop Control | 35.5 | 35.5 | 35.5 |
| With Input-Current-Based Droop Control | 35.5 | 35.5 | 35.5 |

output power of 3kW. The LLC converter parameters listed in Table 3.1 (namely $Q_{5,R_{DS,ON}}$, $Q_{6,R_{DS,ON}}$, $L_R$, $C_R$, $Q_{7,R_{DS,ON}}$, and $Q_{8,R_{DS,ON}}$) are varied across all three converters. In the first simulation model, no paralleling (droop) controller is active and the output voltage loop of all three converters is configured to maintain an output voltage of 28V. Several simulation tests are performed and the highest imbalance in output current in the first simulation model is seen for parameter variations listed in Table 3.2. Given the worst case parameter values, the subsequent two simulation models are configured similar to the first simulation model. However, in the second simulation model, an output-current-based droop controller is implemented and in the third simulation model an input-current-based droop controller is incorporated, alongside the output voltage control loop. Finally, steady-state rms output currents of all

TABLE 3.4: PARAMETER VARIATION AMONG THREE AC-DC CONVERTERS TESTED IN SIMULATION

| Parameter | Parameter Value | | |
|---|---|---|---|
| | Converter 1 | Converter 2 | Converter 3 |
| $L_{PFC}$ | +7% | Nominal | -7% |
| $Q_{1,R_{DS,ON}}$, $Q_{2,R_{DS,ON}}$ | +10% | Nominal | -10% |
| $Q_{3,R_{DS,ON}}$, $Q_{4,R_{DS,ON}}$ | +10% | Nominal | -10% |
| $C_{BUS}$ | -10% | Nominal | +10% |
| $Q_{5,R_{DS,ON}}$, $Q_{6,R_{DS,ON}}$ | +10% | Nominal | -10% |
| $L_R$ | -5% | Nominal | +5% |
| $C_R$ | -5% | Nominal | +5% |
| $Q_{7,R_{DS,ON}}$, $Q_{8,R_{DS,ON}}$ | +10% | Nominal | -10% |

three parallel converter modules in all three simulation models are measured and the results are listed in Table 3.3. As can be seen, without any droop controller, all three converters have highly imbalanced output currents and majority of the output current is being delivered by the converter 1. However, with the droop controllers active in simulation models 2 and 3, the power converters achieve near-perfect output current distribution with all three converters sharing equal output power.

Once the worst case converter configuration is identified based on above simulations, a similar simulation setup is built for the entire ac-dc converter. In this simulation setup, three ac-dc converters are operated in parallel to power a 3-kW load. The converter parameters in each ac-dc converter are varied and their values are listed in Table 3.4. Finally, rms currents with and without the droop control are measured in steady-state and the results are listed in Table 3.5. As can be seen, without droop controller, converter 1 still delivers majority of the output current. However, when any of the droop

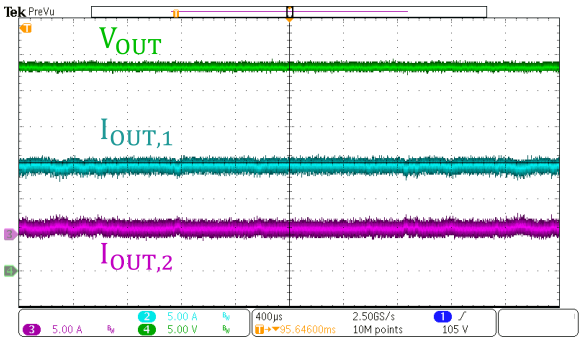
TABLE 3.5: RESULTS OBTAINED FROM SIMULATION OF THREE AC-DC CONVERTERS IN PARALLEL

| Parameter | RMS Output Currents $I_{OUT,rms}$ ($A_{rms}$) | | |
|---|---|---|---|
| | Converter 1 | Converter 2 | Converter 3 |
| Without Droop Control | 61.7 | 24.6 | 21.1 |
| With Output-Current-Based Droop Control | 35.5 | 35.5 | 35.5 |
| With Input-Current-Based Droop Control | 35.5 | 35.5 | 35.5 |

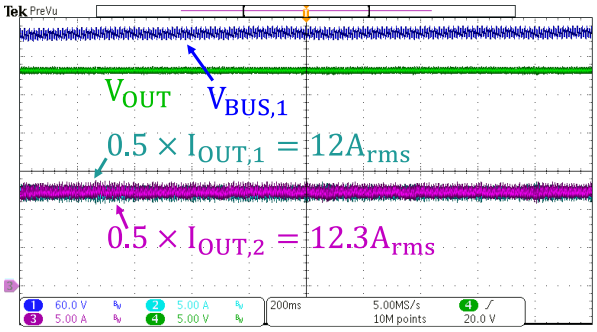
controller is activated, all converters achieve near-perfect current distribution.

## 3.4 EXPERIMENTAL VALIDATION OF INPUT-CURRENT-BASED DROOP CONTROLLER

To validate the control scheme discussed in the previous section, two 1-kW ac-dc converters (similar to the ac-dc converter presented in Chapter 2) are built and tested. For the hardware validation, the input-current-based droop control strategy is utilized because of its advantages as highlighted in Section 3.2. Fig. 3.7 shows the experimentally measured steady-state waveforms of two ac-dc converters operating in parallel. Fig. 3.7(a) shows the output voltage (across the shared load) and output currents of both ac-dc converters with the voltage control loop active and with the current sharing controller deactivated (without any droop control). It can be seen that with just the voltage control loop operating in each converter, the output currents are highly imbalanced with the converter 1 delivering the entire load current, and the two converters do not naturally share any output current. Fig. 3.7(b) shows the output voltage (across the shared load), output current of both converters, and dc-bus voltage of converter 1 with the LLC input current based droop control active. As can be seen, the output currents of both converter modules are well balanced, while the output voltage is regulated at 28V and dc-bus voltage of the converter 1 is regulated at 400V.




(a)




(b)

Fig. 3.7: Experimentally measured steady-state waveforms of two converters connected in parallel: (a) output currents of converter 1 and 2 (5A/div), and output voltage across the load with the current-sharing controller turned-off (5V/div), (b) output currents of converter 1 and 2 (5A/div), dc-bus voltage of converter 1 (60V/div), and output voltage across the load with the proposed current sharing controller turned-on (5V/div).

Fig. 3.8 shows the experimentally measured output voltage as a function of output power when two 1-kW rated ac-dc converters are connected in parallel. It can be seen that the output voltage drops with output load. Based on this drop in output voltage, the virtual droop resistance $R_{droop}$ is measured to be 12.4mΩ. Fig. 3.8 also shows the percentage current distribution error (CDE) between the two ac-dc converter modules connected in parallel. The CDE is defined as $\max\left(\left|\frac{I_{OUT1}-I_{OUT,ideal}}{I_{OUT,ideal}}\right|, \left|\frac{I_{OUT2}-I_{OUT,ideal}}{I_{OUT,ideal}}\right|\right)$ and is the deviation of output current of each parallel-connected module (i.e., $I_{OUT,1}$, $I_{OUT,2}$) from the nominal output current of each module (under perfect current

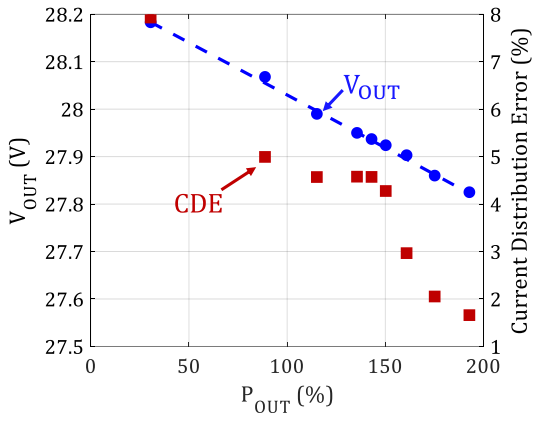



Fig. 3.8: Experimentally measured output voltage and current distribution error of the paralleled converter modules powering a common output load while utilizing the proposed droop control strategy. Here 100% load represents 1kW which is the maximum power rating of a single ac-dc converter module.

distribution) $I_{OUT,ideal}$. As can be seen from Fig. 3.8, the CDE remains below 8% for the entire test range and below 5% for power levels exceeding 900W. Moreover, the measured CDE is below 2% near the maximum total output power of 2kW thereby validating the efficacy of the proposed LLC input current based droop controller.

## 3.5 Chapter Summary

This chapter presents paralleling strategies for a single-phase universal-input to 28-V ac-dc conversion system comprising multiple paralleled two-stage ac-dc converters. Two droop control strategies are presented. The first strategy utilizes an output-current-based droop control to enable parallel operation. Challenges associated with sensing output current in an isolated high-power low-output-voltage ac-dc converter are discussed. To overcome such challenges, a new droop control strategy is presented which employs the input current of the LLC dc-dc conversion stage to enable adequate output current distribution between paralleled modules when powering a common output load. The presented input-current-based droop control strategy also incorporates a variable droop resistance based on the instantaneous value of the dc-bus voltage to ensure a stable output dc voltage in the

presence of the twice-line frequency dc-bus voltage ripple. To validate the input-current-based droop control strategy, two 1-kW universal input to 28V-output isolated ac-dc converter modules are built and tested. The prototype system achieves a current distribution error of less than 2% at the maximum output power of 2kW and maintains a current distribution error of less than 8% across an 8:1 output power range.

# CHAPTER 4

# SINGLE STAGE AC-AC TRANSFORMER-LESS CONVERTER

The power converters presented in Chapters 2 and 3 convert an ac-line voltage to a dc output voltage. While there is immense utility for ac-dc power converters, a substantial range of applications require an ac-ac power conversion. The most common strategy to address this need is to utilize a line-frequency transformer. Line-frequency transformers provide a low-cost solution to ac-ac power conversion and often have high efficiencies (in excess of 95%). However, such transformers have limitations. Firstly, they have large volume and are heavy. The size (and weight) of a transformer is dependent on the volt-seconds applied on its primary (or secondary) winding. This makes a transformer unsuitable for use in applications involving high amplitude or low frequency ac voltages and requiring smaller form-factor. Secondly, since a transformer is a passive component, it does not provide any output voltage regulation. Therefore, a transformer is not appropriate for use in applications which require a stable ac-voltage in the face of input voltage disturbances. Regardless of these drawbacks, transformers are a popular choice because of their lower manufacturing cost.

However, growth in semiconductor technologies, higher need for active power conversion, and newer power electronics topologies and control strategies, are rapidly bridging the gap between widespread use of passive elements like transformers and their active replacements i.e., ac-ac power electronic converters. As specified in Chapter 1, a key application for line-frequency transformers is in industrial lighting where they are used to convert a $480V_{rms}$ ac-line voltage to $264V_{rms}$ ac voltage, compatible with universal input offline LED drivers. To actively replace line-frequency transformers with more efficient, compact (high power density), and lightweight power electronic converters, a low-cost solution needs to be devised. Therefore, there is a need for research in a new design and control methodology for ac-ac power converters, that focuses on their cost as a key design metric while achieving efficiency and power density benefits.

This chapter presents two low-cost high-efficiency high power density single-stage $480V_{rms}$ to $264V_{rms}$

ac-ac converters for lighting applications. The first ac-ac converter utilizes a 2-level ac-ac buck converter topology and the second ac-ac converter utilizes a 3-level center-point-clamped (CPC) ac-ac buck converter topology. Both topologies demonstrate high performance while minimizing the overall cost. This is achieved through a comprehensive cost and efficiency optimization methodology that helps identify the most appropriate converter designs across a design space comprising various switch structures, a range of operating frequencies, and different inductance values. Moreover, control strategies are also presented for both ac-ac converters to regulate their output voltage and a switching scheme is introduced that ensures smooth inductor current commutation during switching transitions and reduces zero-crossing distortion in the input. Furthermore, an active voltage balancing scheme is developed for the 3-level CPC ac-ac converter to compensate for any imbalances between the two stacked input capacitors to ensure robust converter operation. Two 600-W ac-ac prototype converters based on the proposed optimization, designed to operate at an input voltage of $480V_{rms}$ and an output voltage of $264V_{rms}$ are built and tested. Both prototyped converters achieve high conversion efficiencies and high power densities, while achieving a comparable overall component cost to the conventional solution (line-frequency transformer).

## 4.1 Architectures of the Single-Stage AC-AC Power Converters

The topologies of the single-stage ac-ac power converters are presented in Fig. 4.1. Fig. 4.1(a) shows a standard ac-ac buck converter. It comprises a single inverter consisting of 2 switches where each switch needs to be implemented by a four-quadrant switch. In this topology, each four-quadrant switch needs to block the peak input voltage. The inverter chops the input ac-line voltage at high frequency and the L-C tank (comprising $L_{OUT}$ and $C_{OUT}$) filters the high frequency ripple in the chopped voltage to generate a line-frequency sinusoid at the output. The amplitude of output voltage is controlled by the duty cycle of the switch $S_1$.

The topology of the center-point-clamped (CPC) buck-type ac-ac converter is shown in Fig. 4.1(b).

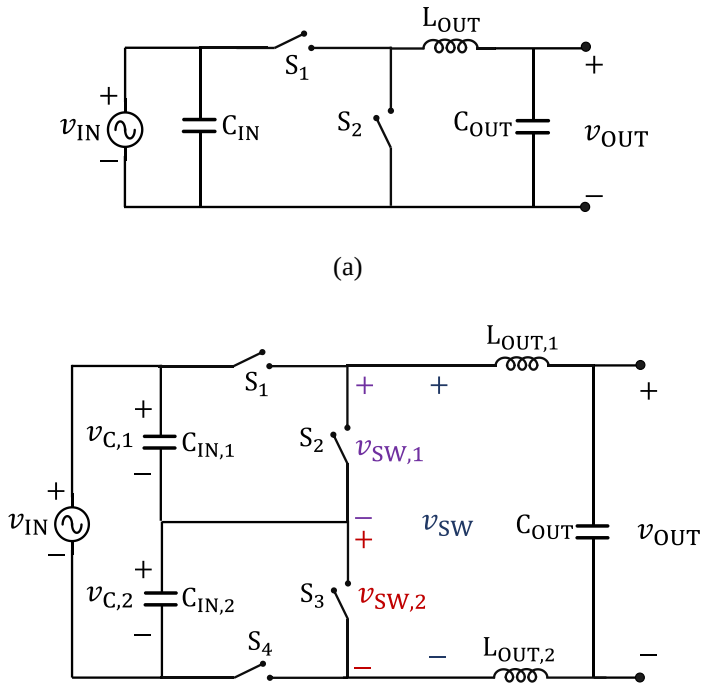
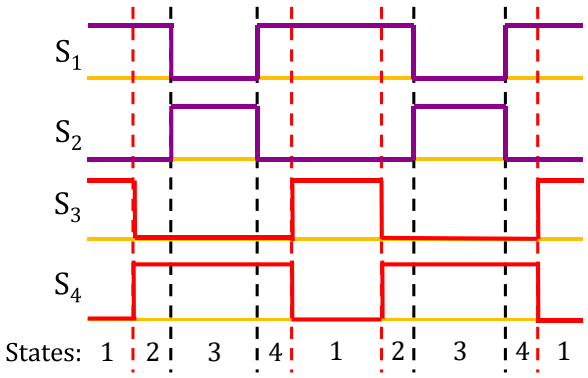


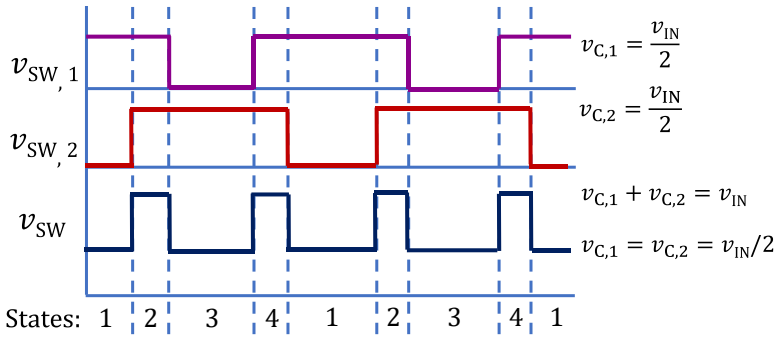

Fig. 4.1: Topologies of the single-stage ac-ac power converters: (a) 2-level ac-ac buck converter, (b) 3-level center-point clamped (CPC) ac-ac buck converter.

The converter comprises two stacked inverters (switches $S_1 - S_4$), where each switch is required to be a four-quadrant switch. This topology is chosen because it reduces the voltage stress across the switching devices by a factor of two compared to a standard ac-ac buck converter. The inverter gating signals for the CPC ac-ac buck converter are shown in Fig. 4.2(a). The inverter switches are operated at a fixed switching frequency with a 180° phase shift between the two inverters. The corresponding switch-node waveforms are shown in Fig. 4.2(b). It is seen that the voltage across the L-C tank ($v_{SN}$) has double the frequency as compared to the switching frequency of the inverter switches. This reduces the switching losses of the inverter while enabling the inductor and output filter capacitor to be designed for a higher switching frequency, potentially reducing their size and cost.

## 4.2 Switch and Gate Drive Implementations




(a)

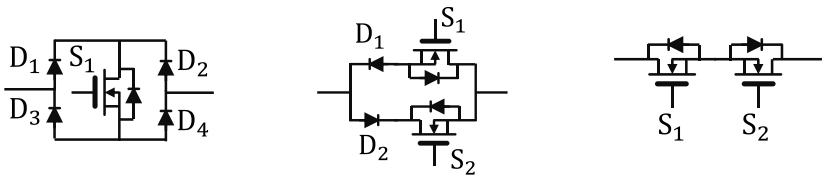



(b)

Fig. 4.2: Operation of the CPC ac-ac buck converter: (a) PWM timing diagram for inverter switches, (b) Switch node voltage waveforms.

For the four-quadrant switches in the two ac-ac converters, three switch implementations are considered, as shown in Fig. 4.3. Switch implementation I (see Fig. 4.3(a)) presents least gate drive complexity, as it has only one MOSFET, but it always has two diodes in the conduction path. Switch implementation II (see Fig 4.3(b)) reduces the total number of devices by using one additional MOSFET. Switch implementation III (see Fig. 4.3(c)) uses only two MOSFETs and has the least component count. In switch implementations I and II, Schottky diodes can be utilized to reduce reverse recovery losses associated with hard switching, but switch implementation III always suffers from reverse recovery losses since it utilizes the body diode of the MOSFETs for current commutation.

Various gate drive circuitry are considered to operate the switches in both ac-ac converter. These include isolated gate drives, self-powering gate drives [127],[128], and transformer-isolated gate




(a) (b) (c)

Fig. 4.3: Topologies of the four-quadrant switches.

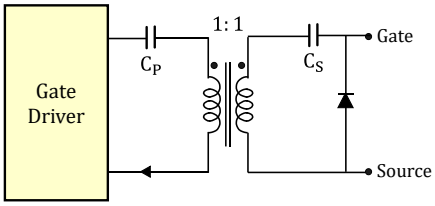



Fig. 4.4: Transformer-isolated gate drive implementation.

drive. Isolated gate drivers require isolated dc-dc converters to power their secondary side and result in much higher cost. Self-powering gate drivers require the use of additional high-power and high-voltage devices and result in increased cost. Transformer-isolated gate drive, shown in Fig. 4.4, provide a low cost and robust solution which can be implemented using a single dc supply and low-power and low-voltage devices. This methodology is chosen for driving the four-quadrant switches in the ac-ac converters.

## 4.3 Cost and Efficiency Optimization

For the cost optimization of the ac-ac converters, four converter implementations are considered for each ac-ac converter topology, as shown in Fig. 4.5 and 4.6 respectively. Switch implementation I (Fig. 4.3(a)) cannot be used for all four switches since it does not allow smooth switching transitions and results in discontinuity in inductor currents during the dead-times. Hence this implementation is used in conjunction with either switch implementation II (Fig. 4(b)) or implementation III (Fig. 4(c)). For each of these converter implementations, detailed loss models are developed that include switching and conduction losses for the semiconductor devices and winding and core losses for the inductors. For

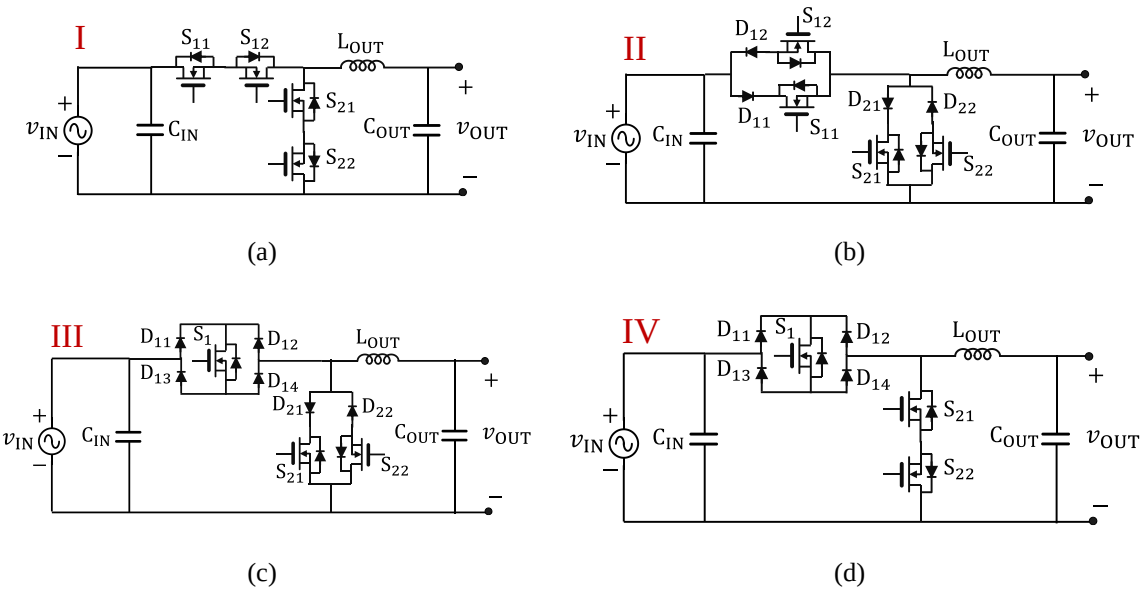



Fig. 4.5: Different implementations of 2-level ac-ac buck converter considered for cost and efficiency optimization.

design of each converter implementation, switching frequency and inductance values are swept across wide range and the design with the maximum efficiency is selected.

For cost computations, the cost of all major components in the converter, including power semiconductor devices (MOSFETs and diodes), gate driver chip and transformer, input and output film capacitors, inductors, microcontrollers and various passive components is considered. For accurate price models, quotations from various manufacturers and large volume pricing are obtained. Results of the proposed optimization are shown in Fig. 4.7, which comprises cost vs. efficiency comparison for the four implementations considered for each ac-ac converter topology (see Fig. 4.5 and 4.6). It can be seen that implementation I (Fig. 4.5(a) and 4.6(a)) results in the lowest cost for the proposed SST, while implementation II (Fig. 4.5(b) and 4.6(b)) has the highest efficiency. This difference between the performances of these two designs is due to the fact that implementation II uses Schottky diodes which help reduce the switching losses associated with reverse recovery; however, addition of these diodes results in an increase in the converter cost. Since the proposed application is focused on lowest cost designs, implementation I is chosen as the topology of choice for the SST. For the selected converter

topology, the cost breakdown is given in Fig. 4.8, which shows the cost of all major components in each

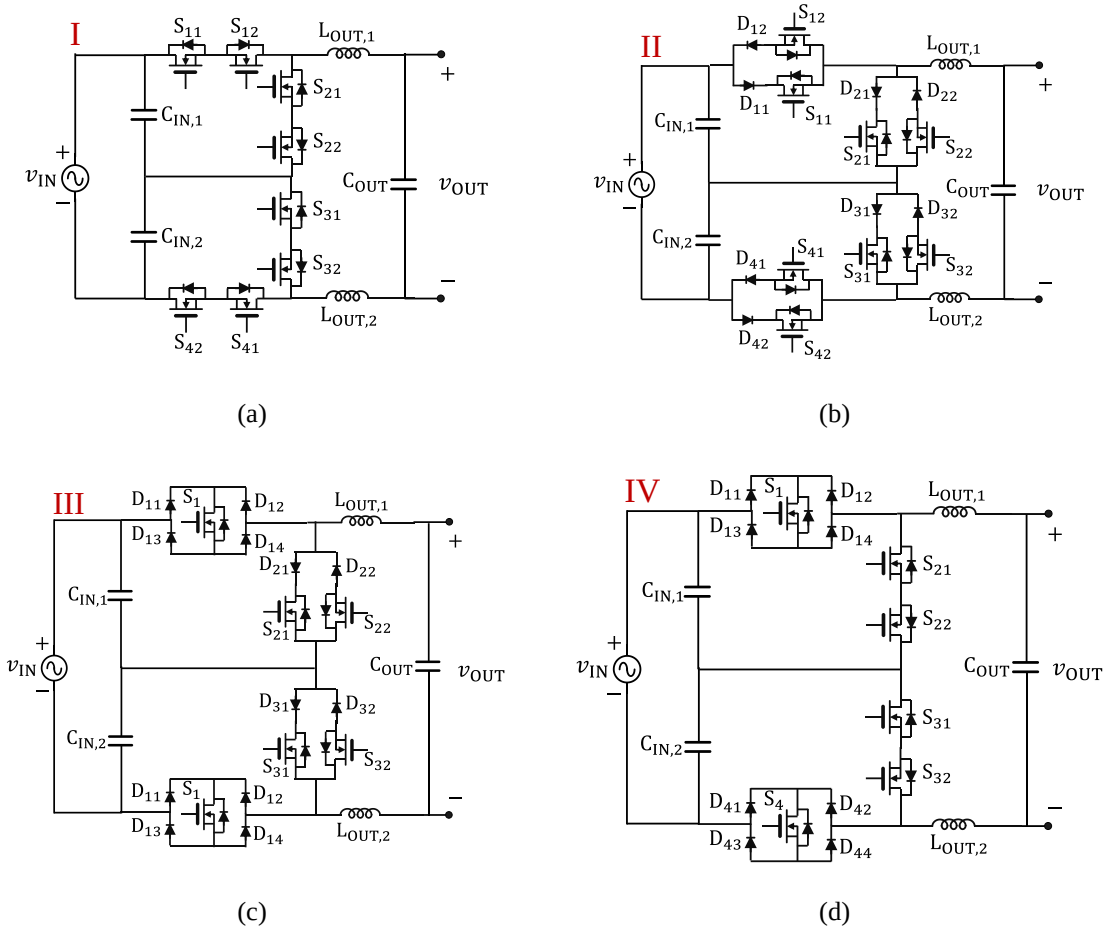



Fig. 4.6: Different implementations of 3-level ac-ac buck converter considered for cost and efficiency optimization.

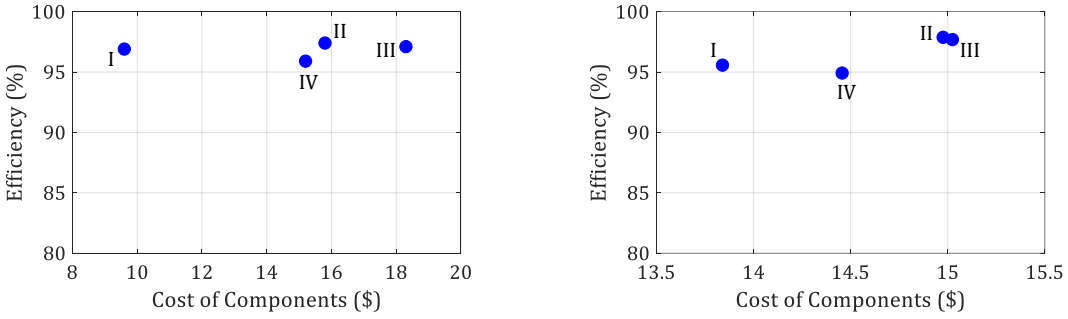
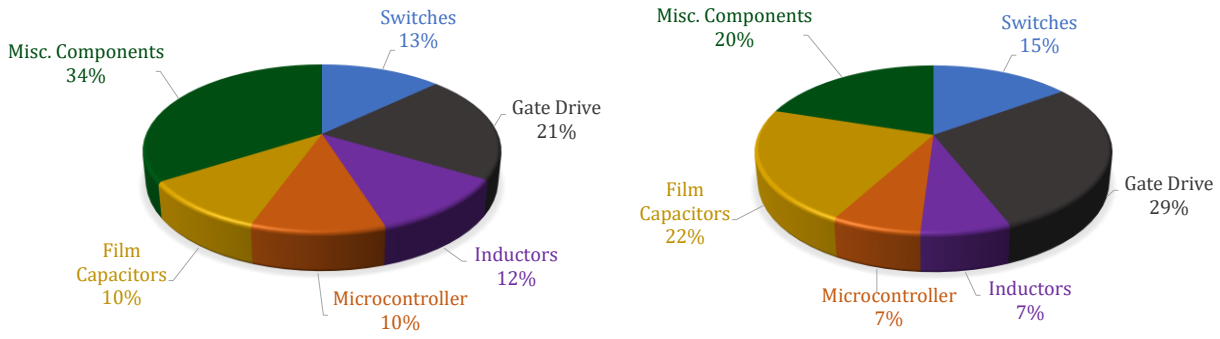



Fig. 4.7: Comparison of cost and efficiency of four different ac-ac converter implementations: (a) 2-level ac-ac buck converter, (b) 3-level center-point clamped (CPC) ac-ac buck converter.




(a) (b)

Fig. 4.8: Cost breakdown of the two ac-ac converters: (a) 2-level ac-ac buck converter, (b) 3-level center-point clamped (CPC) ac-ac buck converter.

ac-ac converter.

## 4.4 Control Strategy

This section discusses the control strategies for both ac-ac converters. Three elements of control are discussed: four-quadrant switch control to ensure smooth inductor current, voltage-loop control, and input capacitor voltage control for 3-level CPC ac-ac buck converter. Following sub-sections address each of these in detail.

### 4.4.1 Four-Quadrant Switch Control

The use of four quadrant switches in the two ac-ac converters requires a control mechanism to ensure a continuous current path for the inductor current, during the dead-times. In addition, delays and inaccuracies in the sensing of the input voltage zero crossings introduce additional challenges to prevent impulse discharge of the input capacitors. Therefore, a switch commutation scheme is presented that ensures smooth transitions of the inductor current during dead-times and near line zero-crossings. For the sake of brevity, a single state transition in 3-level CPC ac-ac buck converter is highlighted as follows. Fig. 4.9 shows the commutation scheme, when the 3-level CPC ac-ac buck converter is transitioning from state 4 to state 1 (see Fig. 4.2(a)). This is shown for the case when positive inductor current is flowing as labelled in Fig. 4.9(a). Even though this transition only addresses the 3-level CPC ac-ac converter, it is also applicable to the standard ac-ac buck converter. Just before turning off $S_4$, $S_{42}$ is

turned off enabling current to commutate from the body of $S_{42}$ to its diode (see Fig. 4.9(b)). Now switch $S_{32}$ is turned on to create a path for inductor current before the next step of switch transition (see Fig. 4.9(c)). Once switch $S_{32}$ is turned-on, switch $S_{41}$ is safely turned off allowing inductor current to commutate from switch $S_4$ ($S_{41}$ and $S_{42}$), to switch $S_3$, as shown in Fig. 4.9(d). During this interval, the inductor current is flowing through the body diode of $S_{31}$ and the channel of $S_{32}$. This switch transition is necessary because it prevent impulse discharge of capacitor $C_{IN,2}$. Lastly, switch $S_{31}$ is also turned on and the current starts flowing through its channel (Fig. 4.9(e)), finishing the state transition from state 4 to state 1. Switching transition from state 1 to state 4 is simply the reverse of this. Similarly, for all other state transitions in both ac-ac converters, additional sub-states are introduced to ensure inductor current commutation during dead-time. This control scheme also prevents the build-up in inductor current due to delays and inaccuracies in zero crossing detection, reducing zero-crossing distortion in the input current. During this brief interval, the inductor current is brought safely to zero before the microcontroller senses the change in input voltage polarity and provides the correct gate pulses.

### 4.4.2 OUTPUT VOLTAGE CONTROL

For both ac-ac converters, output ac-voltage regulation is required to ensure the amplitude of the output voltage is maintained during input voltage and output load variations. To accomplish this, a feedback controller is designed for both ac-ac converters, as shown in Fig. 4.10. In both ac-ac converters, the output voltage is sensed and compared with a reference ac voltage to generate error for the voltage compensator. The compensator generates duty cycle for switches in the converter. The four-quadrant switch control describe in the previous section is implemented in the digital controller to generate suitable gate drive signals with sufficient dead-times. A key consideration while implementing the control strategy lies in the controller computational limitations since a low-cost controller is utilized in the design. Such controllers do not have floating point computation capability and have limited PWM resolution and ADC sampling frequency. The compensator for both converters is therefore designed to have low bandwidth PI compensator to track the 60Hz reference sine-wave. Fixed point computation is

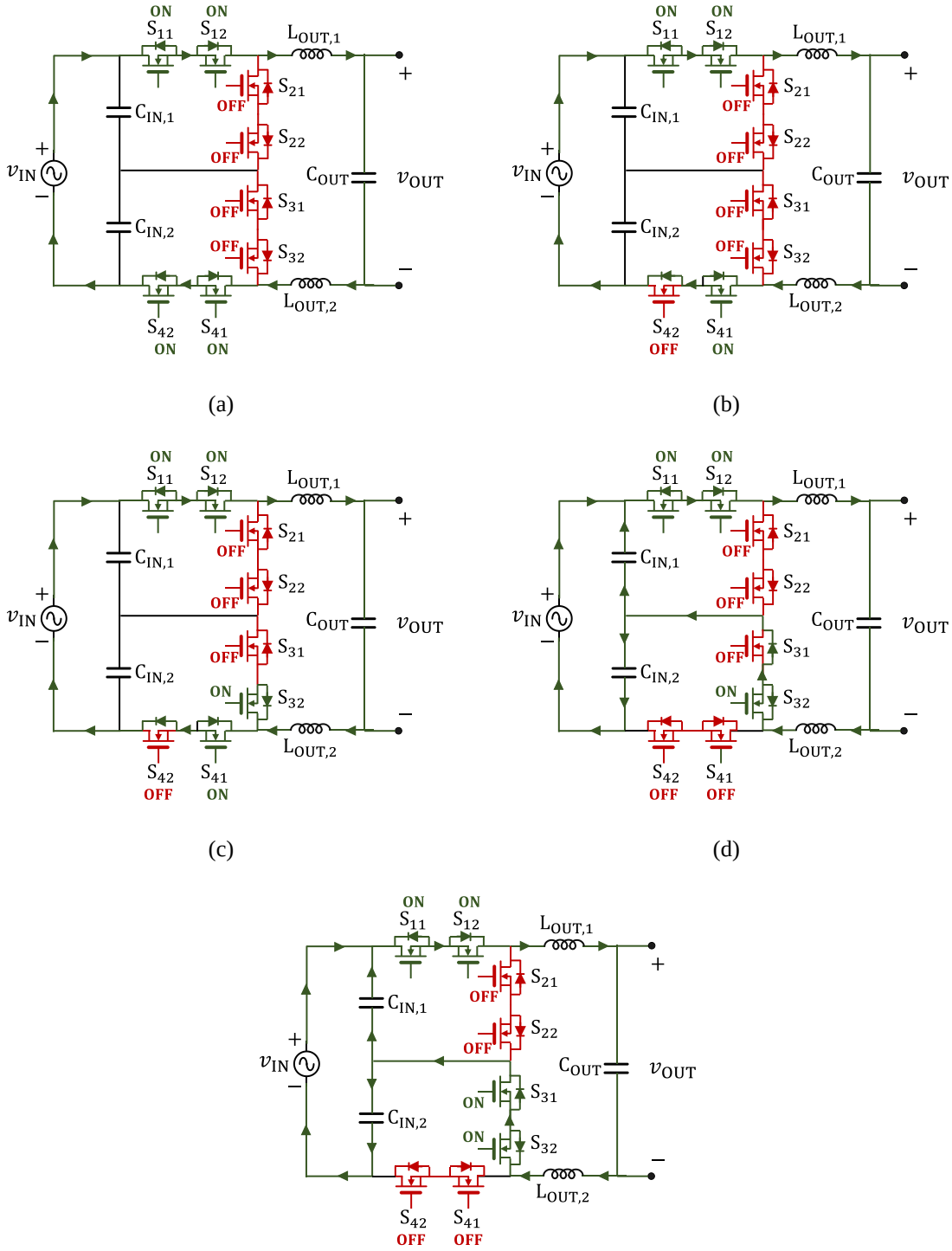
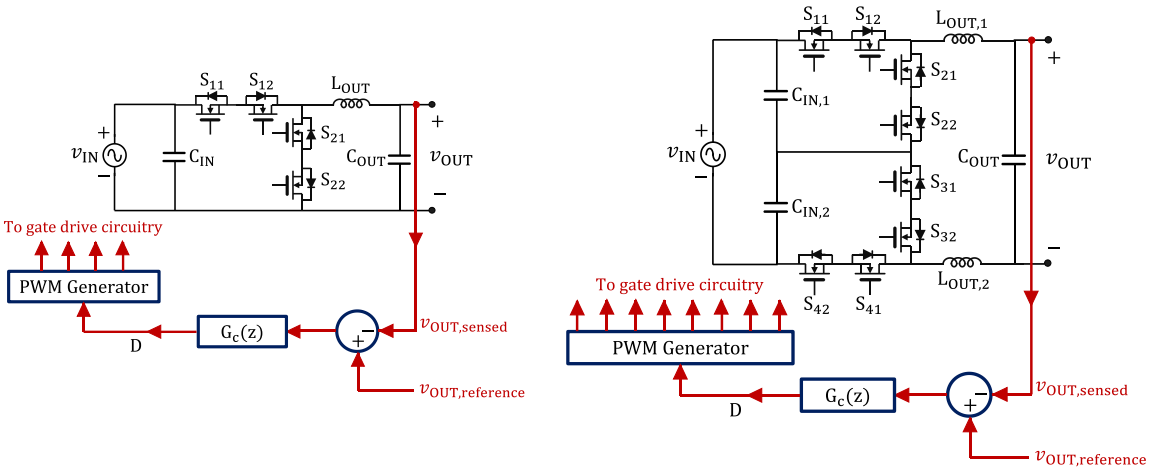



Fig. 4.9: Current commutation scheme when the 3-level CPC ac-ac buck converter is transitioning from state 4 to state 1. This is shown for the case when $v_{IN}$ is positive.

implemented using addition, subtraction, and simple bit operations to multiply compensator parameters. Details about fixed point implementation can be seen in [129].

### 4.4.3 Capacitor Voltage Balancing Control for 3-Level CPC AC-AC Buck Converter

A control methodology to balance the voltages across input capacitors of 3-level CPC ac-ac buck converter is also presented. In normal converter operation, these voltages diverge due to tolerances in capacitances of the input capacitors and differences in the effective on and off times of switches due to differences in the control signals and individual gate drivers. This imbalance results in increased voltage stress and increased losses in the bridge with the higher voltage. Fig. 2.11 shows the PWM timing diagram for the voltage balancing methodology utilized for this converter. This PWM scheme is shown for the case when the voltage across capacitor $C_{IN,1}$ is greater than voltage across capacitor $C_{IN,2}$. To balance the voltages across the two capacitors, the duty cycle of the top inverter is increased by $2\Delta D$ while the duty cycle of bottom inverter is decreased by the same proportion. This causes the time duration of state 1 to increase by $\frac{2\Delta D}{f_s}$ while the time duration of state 3 decreases by the same amount.




(a) (b)

Fig. 4.10: Output voltage control architecture for ac-ac converters: (a) 2-level ac-ac buck converter, (b) 3-level center-point clamped (CPC) ac-ac buck converter.

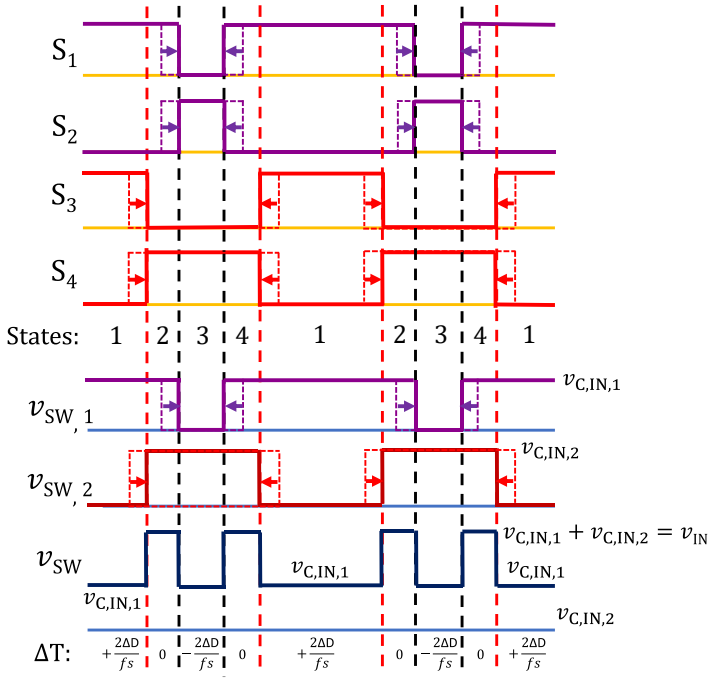



Fig. 4.11: Proposed inverter PWM timing diagram for input capacitor voltage balancing. This shown for the case when $v_{C,IN,1} > v_{C,IN,2}$ .

Here $f_s$ is the switching frequency of the converter. The duration of state 2 and state 4 is not affected by this change in the duty cycle. This causes the capacitor $C_{IN,1}$ to discharge for a longer period than capacitor $C_{IN,2}$ allowing the average voltage across $C_{IN,1}$ to decrease, resulting in a corresponding increase in the capacitor $C_{IN,2}$ voltage, since both the capacitors are connected in series. Similarly, a negative value of ΔD will have the opposite effect and cause voltage across $C_{IN,2}$ to decrease. By varying value of ΔD, the average voltage across $C_{IN,1}$ and $C_{IN,2}$ can be controlled and any imbalances in their voltages can be eliminated. This control scheme can be easily implemented using symmetric pulse-width modulation functionality present in most microcontrollers with phase-shifted carriers to produce the required gate pulses.

Another aspect to consider in a low-cost implementation is the ability of microcontroller to produce high resolution PWM signals. Low-cost microcontrollers have low clock speeds which limits the PWM frequency and its resolution. For higher output loads, the value of ΔD needs to be reduced as the

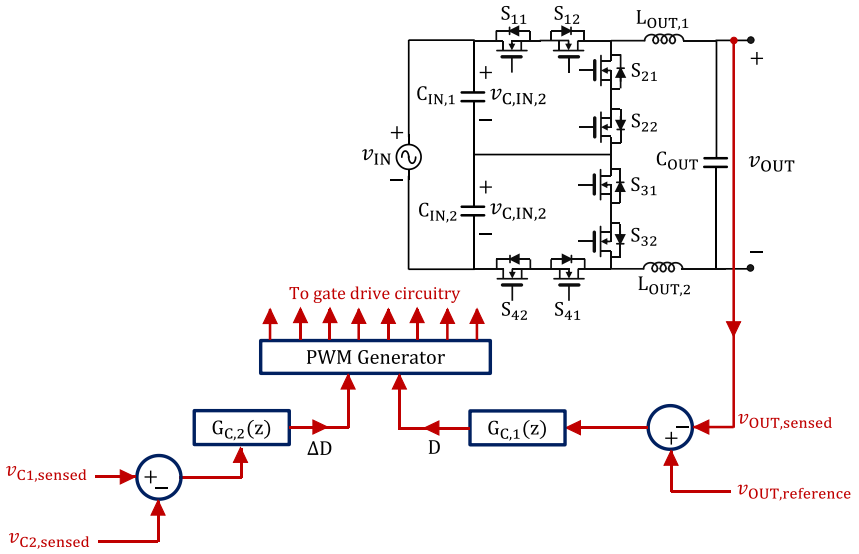
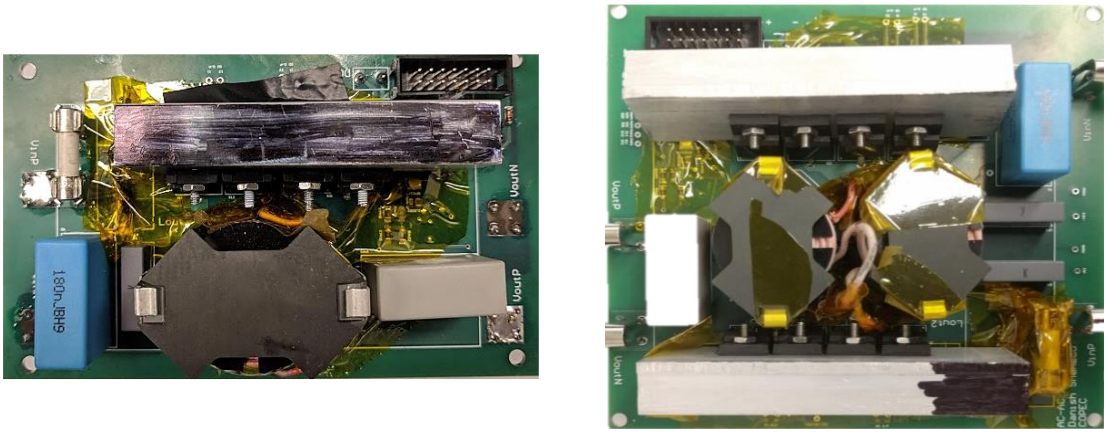



Fig. 4.12: Final control architecture for the 3-level CPC ac-ac buck converter including the input capacitor voltage balancing block.

increased output current draws charge out of one capacitor and into the other capacitor at higher rate causing larger variation in the voltages. The discrete nature of ΔD and its low resolution limits the ability to control capacitor voltages at higher output load values. To solve this issue, an innovative modulation scheme to increase the effective resolution of ΔD is used in this low-cost solid-state transformer implementation. To illustrate the proposed scheme, consider an example in which the microcontroller can only achieve a step size of 1 in ΔD but the required ΔD for voltage balancing is 0.5. To overcome this limitation, the ΔD is modulated between 0 and 1 with a modulation index of 50 %. This will have an effective ΔD of 0.5 which will help obtain the required change in the capacitor voltages. This technique is utilized to achieve precise voltage balance across input capacitors and the control architecture for 3-level CPC ac-ac buck converter is shown in Fig. 4.12.

## 4.5 Prototype Design and Experimental Results

To validate the design and performance of the ac-ac converters, two 600W 480$V_{rms}$-to-264$V_{rms}$ ac-ac converter are built and tested. Photographs of the prototype converters are shown in Fig. 4.13. The 2-



(a) (b)

Fig. 4.13: Photographs of the 600W 480$V_{rms}$-to-277$V_{rms}$ ac-ac converter: (a) 2-level ac-ac buck converter, (b) 3-level CPC ac-ac buck converter.

level ac-ac buck converter achieves a power density of 60W/$in^3$ and the 3-level CPC ac-ac buck converter achieves a power density of 40W/$in^3$. Based on the optimization performed in Section 4.3, the switching frequency for both 2-level buck converter and 3-level CPC buck converter was chosen to be at 50kHz. The 2-level buck converter utilizes four 900-V Si MOSFETs (IPA90R340C3) and the 3-level buck converter utilizes eight 600-V Si MOSFETs (IPA60R400CE). Both ac-ac converters utilize dual low-side gate drivers by IXYS and 1:1 toroid core gate-drive transformers to drive the MOSFETs. The inductors are built using Litz wire wound on RM cores. A single RM14 core is used in the 2-level buck converter and two RM12 cores are used in 3-level buck converter. The choice of using split-inductor design in 3-level buck converter is made to reduce common-mode noise at the input of the converter. The prototype ac-ac converters are controlled using a TI MSP430F5510 microcontroller.

Experimentally measured steady-state waveforms of the 2-level ac-ac buck converter are shown in Fig. 4.14. As can be seen, the output voltage is regulated at 264$V_{rms}$ validating operation of the converter. The steady-state operating waveforms for the 3-level CPC ac-ac buck converter are shown in Fig. 4.14. As can be seen from Fig. 4.15(a), the output voltage is regulated at 264$V_{rms}$. The input capacitor voltages

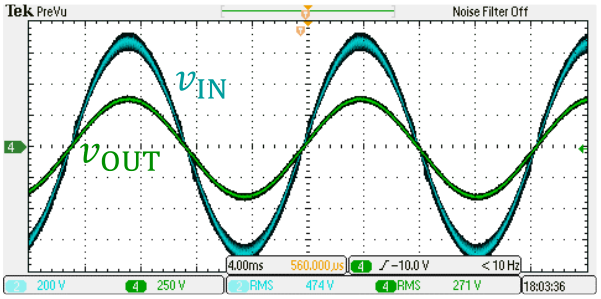
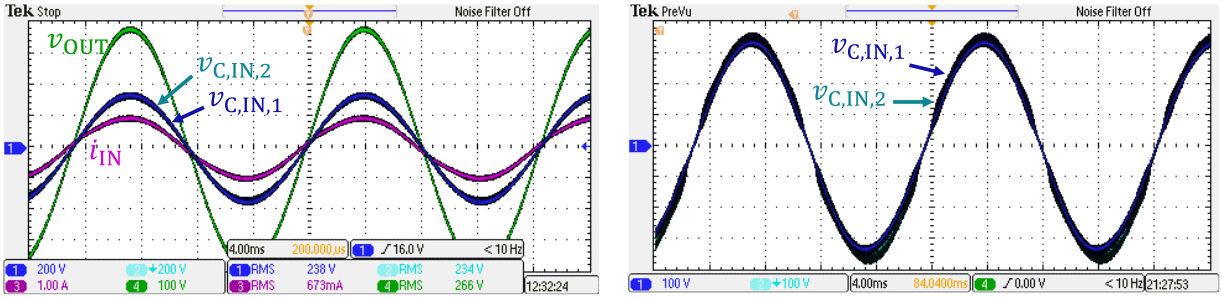



Fig. 4.14: Steady-state input voltage (200V/div) and output voltage (250V/div) of the 2-level ac-ac buck converter while converting a 480$V_{rms}$ input ac-voltage to a 277$V_{rms}$ output ac-voltage.



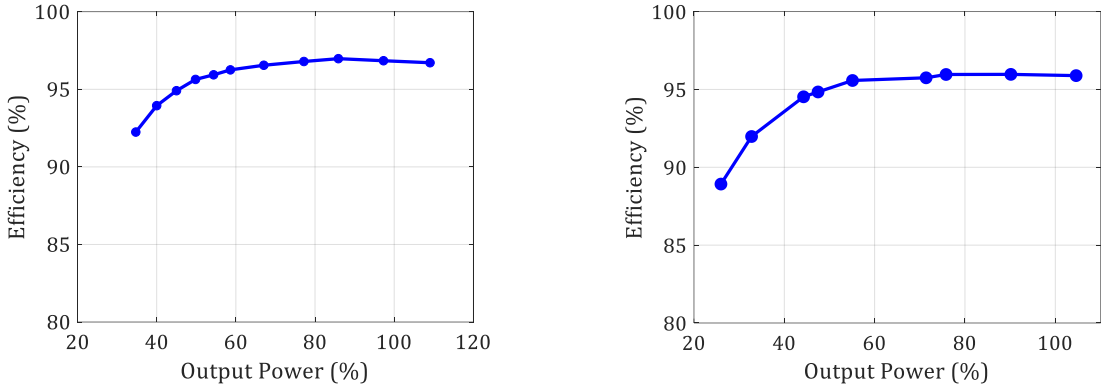

(a) (b)

Fig. 4.15: Steady-state operating waveforms of the 3-level CPC ac-ac buck converter: (a) Input capacitor voltages $v_{C,IN,1}$ and $v_{C,IN,2}$ (200V/div), input current (1A/div), and output voltage (100V/div), (b) Input capacitor voltages $v_{C,IN,1}$ and $v_{C,IN,2}$ (100V/div).

are also shown in Fig. 4.15(a) and Fig. 4.15(b). In both the waveforms, the capacitor voltages are balanced verifying the efficacy of the capacitor voltage balancing methodology.

The experimentally measured efficiencies of both prototype ac-ac converters as a function of output power are shown in Fig. 4.16. It can be seen from Fig. 4.16(a) that the 2-level ac-ac buck converter achieves a peak efficiency of 97% and maintains an efficiency of above 90% over a 3:1 output power range. Similarly, as can be seen from Fig. 4.16(b), the peak efficiency of the 3-level CPC ac-ac buck converter is 96% and it also maintains a high conversion efficiency of greater than 90% across a 3:1 output power range.

It is evident from the results, that the standard ac-ac buck converter achieves superior performance in terms of all three parameters: efficiency, power density, and cost. The reason for higher efficiency of 2-




(a) (b)

Fig. 4.16: Efficiencies as function of output power of the ac-ac converters: (a) 2-level ac-ac buck converter, (b) 3-level CPC ac-ac buck converter.

level ac-ac buck converter is that the commercially available lowest-cost 900-V MOSFETs exhibit superior performance in terms of $R_{DS,ON}$ as compared to lowest-cost 600-V MOSFET (340mΩ vs 400mΩ). Since, conduction loss was the most dominant loss mechanism (especially since both converters operated at relatively low switching frequency of 50kHz), the effect of $R_{DS,ON}$ was substantial. Moreover, the number of devices in series path of current were also double in 3-level ac-ac buck converter which further affected the overall losses in the converter. In terms of cost, even though the cost-per-MOSFET in 3-level CPC ac-ac buck converter was 16% lower than the cost-per-MOSFET in 2-level ac-ac buck converter, the number of devices in 3-level converter was twice which substantially increased the total cost of the converter. Furthermore, the gate-drive circuitry associated with the eight devices in 3-level converter was double the cost of gate-drive circuitry in 2-level converter.

In practice, 2-level ac-ac buck converter has further advantages as compared to the 3-level ac-ac buck converter. The primary advantage being the presence of a common-neutral which makes it a suitable replacement of auto-transformers, commonly used in lighting applications. The common-neutral configuration helps in achieving appropriate system-level grounding often required by regulatory bodies

(to be discussed further in next chapter). Moreover, it provides a plug-and-play replacement for step-down transformers which are currently used to operate LED drivers from $480V_{rms}$ ac-line.

Having discussed practical benefits of 2-level ac-ac buck converter, the 3-level CPC ac-ac buck converter also has its fair share of advantages. Such a topology is suitable for use in high-voltage applications where conventional devices are not readily available and substantial cost saving can be achieved by using lower voltage devices. Moreover, this topology effectively doubles the frequency of the inductor current and imposes lower volt-seconds on the filter inductor (advantages of any multi-level converter topology) which helps reduce the volume of the filter inductor.

## 4.6 CHAPTER SUMMARY

This chapter presented a low-cost high-efficiency high-power-density single-stage $480V_{rms}$-to-$264V_{rms}$ ac-ac converters for use in lighting applications. The two ac-ac converters utilize a standard 2-level ac-ac buck converter topology and a 3-level center-point-clamped (CPC) ac-ac buck converter topology. A comprehensive cost and efficiency optimization methodology is developed to help identify the most appropriate converter designs across a design space comprising various switch structures, a range of operating frequencies, and different inductance values. For the selected implementation, a switching scheme is introduced that ensures smooth inductor current commutation during switching transitions, and also reduces zero-crossing distortion in the input current. Furthermore, an active voltage balancing scheme is developed to compensate for any imbalances between the two stacked input capacitors in 3-level CPC ac-ac buck converter, to ensure its robust converter operation. Two prototype 600-W ac-ac converter based on the proposed optimization, designed to operate at an input voltage of $480V_{rms}$ and an output voltage of $264V_{rms}$ are built and tested. The prototype 3-level CPC ac-ac buck converter achieves a peak efficiency of 96% while having a power density of $40W/in^3$ and the prototype 2-level ac-ac buck converter achieves a peak efficiency of 97% while having a power density of $60W/in^3$. Both converters are shown to achieve substantially higher performance while having a similar total cost,

as compared to line-frequency transformers commonly used in industrial lighting applications. Lastly, given the advantages of standard 2-level ac-ac buck converter in terms of cost, efficiency, power density, and presence of a common-neutral, it is found to be the better replacement for the line-frequency transformer in lighting applications.

# CHAPTER 5

# TWO-STAGE AC-AC TRANSFORMER-LESS CONVERTER

The previous chapter discussed several aspects of design of a single-stage ac-ac converter. Such converters though are suitable for replacing conventional transformers and have high conversion efficiencies, they have several drawbacks. Firstly, single-stage ac-ac converters do not have any energy buffering element in their architectures. This makes them unsuitable for use in applications where input and output ac voltages have different phase or frequencies. This feature is a key requirement in several applications, for example online uninterruptible power supplies (UPS), to be explored in detail in this chapter. Secondly, single-stage ac-ac converters cannot fully attenuate high-frequency input voltage disturbances/noise. This is often due to bandwidth limitations of the output voltage control loop. The presence of a perfect output ac voltage, unperturbed by any disturbance in the input voltage, is often necessary when an ac-ac converter is required to power critical/sensitive ac loads e.g., data storage equipment, medical imaging systems, etc., where such irregularities in voltage can impede operation or damage electronic circuitry.

Two-stage ac-ac converters can effectively address all the above-mentioned needs. An architecture for a two-stage ac-ac converter is shown in Fig. 5.1. It comprises a rectification stage followed by an inversion stage. The rectification stage converts the ac input voltage to a dc voltage across dc-bus. The inversion stage then converts the dc-bus voltage to an ac output voltage across the load. Since, there is an energy buffer across the dc-bus, this architecture can support an ac output voltage with different frequency/phase as compared to the ac input voltage. Furthermore, as the ac output voltage is not

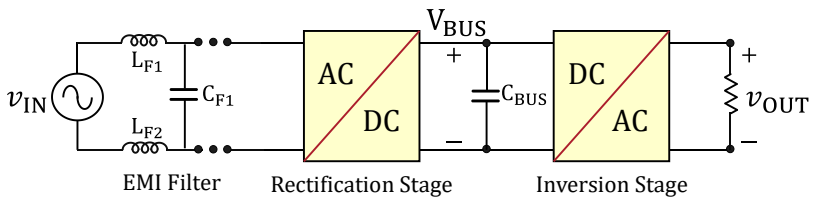



Fig. 5.1: Architecture of a two-stage ac-ac converter.

generated directly from the ac input voltage, any disturbance in the ac input voltage does not appear in the ac output voltage. This satisfies the need for a well-regulated noise-free ac output voltage as discussed earlier.

As elaborated in Chapter 1, several applications of ac-ac converters have certain grounding requirements which influence the choice of converter topology. One such requirement is the ability to connect input and output neutrals. This requirement, which is imposed on online UPS (a two-stage ac-ac converter) in data centers, can be fulfilled by either utilizing a common-neutral topology or by providing galvanic isolation in the converter. A galvanically isolated (transformer-based) online UPS either has low power density resulting from the presence of a bulky transformer or has low conversion efficiency emerging from losses due to a high-frequency transformer. On the contrary, common-neutral (transformer-less) topologies can simultaneously achieve high conversion efficiencies and high power densities because of the absence of a bulky and/or lossy transformer.

A commonly utilized topology for non-isolated online UPS, with a common neutral between input and output ports, is shown in Fig. 5.2. This topology is similar to the online UPS presented in [103] and [111]. The rectification stage is derived from a three-level bridgeless boost converter topology comprising a four-quadrant active switch (implemented using $S_1$ and $S_2$) and synchronous boost switches ($S_3$ and $S_4$) [116]. The buck-type inversion stage is a time-reversed dual of the rectification stage, which produces a sinusoidal output voltage for the load by appropriately switching $S_5$ - $S_8$. The presence of four-quadrant switches in this topology results in relatively large high-frequency-loop inductances, which limits the switching frequency. Furthermore, the split dc-bus introduces challenges

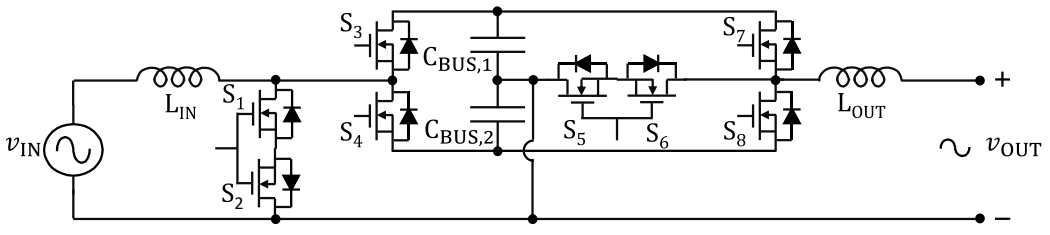



Fig. 5.2: Conventional transformer-less online UPS topology with a split dc-bus and four-quadrant switches.

in terms of capacitor voltage balancing, specifically while delivering power to loads that draw different amounts of power in positive and negative half line cycles. Moreover, if the UPS is being designed to support reactive loads or the frequency of the output voltage is desired to be different from the input voltage, the volume of the split dc-bus capacitors becomes a significant portion of the overall volume, thus negatively impacting the overall power density. The dc-bus capacitance requirement in such cases will be elaborated in section 5.2 of this chapter.

This chapter introduces a new two-stage transformer-less ac-ac converter topology suitable for a high-power-density high-frequency single-phase online uninterruptible power supply (UPS) with a common neutral between the input and output ac ports and a single dc-bus. This proposed topology consists of an input power factor correction (PFC) rectification stage followed by a voltage-mode inversion stage. Both the rectification and inversion stages operate in buck-boost mode for negative input/output voltage polarity and in a boost/buck mode for the positive input/output voltage polarity, respectively. The proposed online UPS utilizes a single dc-bus between the rectification and inversion stages, resulting in a 50% reduction in dc-bus capacitance requirement as compared to conventional split dc-bus online UPS topologies. A detailed analysis of dc-bus capacitance requirement for a single dc-bus and a split dc-bus based online UPS is also presented. This paper also presents the appropriate control techniques that ensure a unity power factor for the input rectification stage and a sinusoidal output ac voltage for the output inversion stage. In the proposed control scheme, the input rectification stage of the UPS, utilizes boundary conduction mode (BCM) control enabling soft-switching and allowing high frequency operation. The inversion (dc-ac) stage is operated in continuous conduction mode (CCM), wherein a digital controller regulates the output voltage of the converter across both resistive and reactive loads. The proposed topology also lends itself to an integrated battery charging/discharging interface. The battery interface utilizes the main power stage during discharge operation (backup mode) eliminating the need for a peak power rated discharge stage. For charging, a lower power rating buck converter is utilized. To verify the performance and control of the proposed online UPS a GaN-based 1-

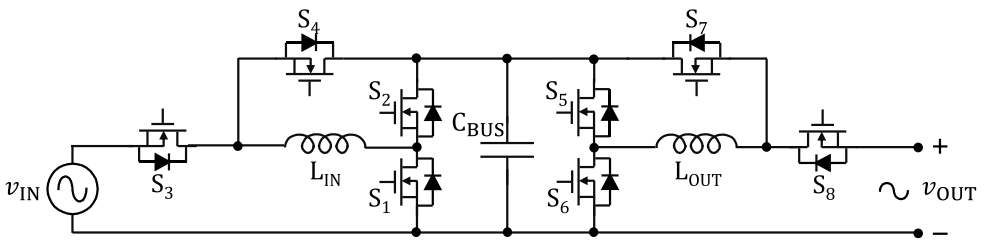



Fig. 5.3: Proposed transformer-less online UPS topology with a single dc-bus and half-bridge switch structures.

kVA electrolytic-free prototype online UPS, is designed, built, and tested. This electrolytic-free prototype ac-dc-ac converter for the UPS achieves a peak efficiency of 95.2% and maintains a high efficiency of above 92% across the full output power range while having a power density of 26.4 W/in$^3$.

## 5.1 PROPOSED ONLINE UPS TOPOLOGY

The topology of the proposed online UPS with a common neutral between the input and the output is shown in Fig. 5.3. It consists of a front-end power factor correction (PFC) rectification stage followed by a voltage-mode inversion stage with a single energy buffering capacitor ($C_{BUS}$) connected across the intermediate dc-bus. The rectification stage comprises two half-bridges with switches $S_1$, $S_2$ forming a boost converter and switches $S_3$, $S_4$ forming an inverting buck-boost converter. Similarly, switches $S_5$, $S_6$ form a buck converter and switches, $S_7$, $S_8$ form an inverting buck-boost converter for the inversion stage.

The operation of the rectification stage is shown in Fig. 5.4. Depending on the polarity of the input voltage ($v_{IN}$), the rectification stage operates in either boost or buck-boost mode. In the positive half line cycle of the input voltage, the rectification stage operates in the boost mode by keeping the switch $S_3$ closed and the switch $S_4$ open, while switching $S_1$ and $S_2$ at a high frequency, as shown in Fig. 5.4(a). On the other hand, during the negative half line cycle, the rectification stage operates in the buck-boost mode by keeping the switch $S_1$ closed and the switch $S_2$ open, while switching $S_3$ and $S_4$ at a high frequency, as shown in Fig. 5.4(b). For lower power applications, the synchronous switches ($S_2$ and $S_4$) can be replaced by diodes, in favor of reduced gate drive complexity and simplified operation. The boost and the buck-boost operating

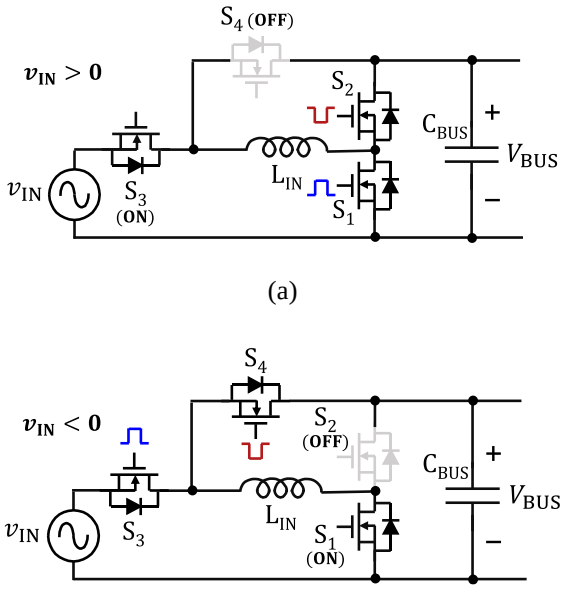
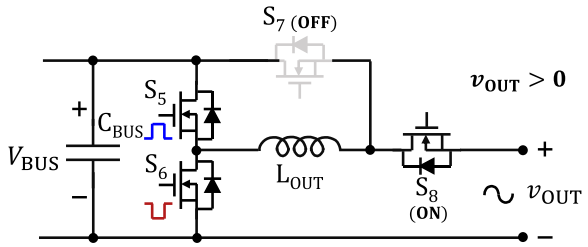


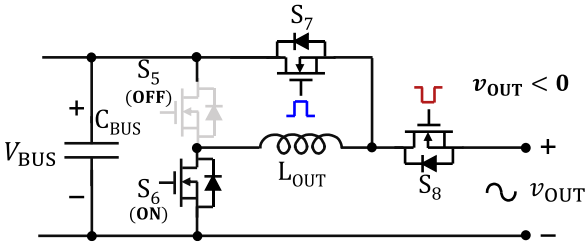

Fig. 5.4: Operating modes of the rectification stage: (a) for positive input voltage, and (b) for negative input voltage.

modes of the rectification stage are appropriately controlled in their respective half line cycles to draw a sinusoidal current from the input at unity power factor while regulating the dc-bus voltage.

The operation of the inversion stage is shown in Fig. 5.5. To produce a positive output voltage, the inversion stage operates in buck mode by keeping the switch $S_8$ closed and the switch $S_7$ open, while switching switches $S_5$ and $S_6$ at a high frequency, as shown in Fig. 5.5(a). A negative output voltage is generated by operating the inversion stage in buck-boost mode, where the switch $S_6$ is kept closed and switch $S_5$ is kept open, and switches $S_7$ and $S_8$ are switched at high frequency, as shown in Fig. 5.5(b). Both operating modes of the inversion stage (buck and the buck-boost modes) are appropriately controlled to generate the desired positive and negative output voltages at the output ac port of the inversion stage. To achieve this, the inversion stage is controlled using voltage mode control, which regulates the output ac voltage amplitude, frequency, and waveshape, with the magnitude and the phase of the output current being determined by the load. Additionally, the phase and frequency of the output ac voltage ($v_{\mathrm{OUT}}$) can be independent of the input ac voltage ($v_{\mathrm{IN}}$), providing flexibility of operation depending on the load




(a)




(b)

Fig. 5.5: Operating modes of the inversion stage: (a) for positive output voltage, and (b) for negative output voltage.

requirements and allowing out-of-phase and out-of-frequency operation at the output.

## 5.2 DC-BUS CAPACITANCE REQUIREMENT

The dc-bus capacitance needed in the proposed online UPS depends on the reactive power that the UPS is required to supply to the load while maintaining a unity power factor at the input. To better understand this energy storage requirement, consider the example operating waveforms for the proposed UPS shown in Fig. 5.6. Fig. 5.6(a) shows the instantaneous voltage and current at the input port of the UPS, and the associated instantaneous input power. Fig. 5.6(b) and 5.6(c) show the instantaneous output voltage, output current, and output power when the UPS is delivering power to two different types of loads: a resistive load and a reactive load, respectively. As can be seen from Fig. 5.6(a) and 5.6(b), for the case of a resistive load and with the output voltage at the same frequency and phase as the input voltage, the instantaneous input and output power are equal, and therefore no twice-line-frequency energy storage is required from the converter. In practice, some minimum bus capacitance is still

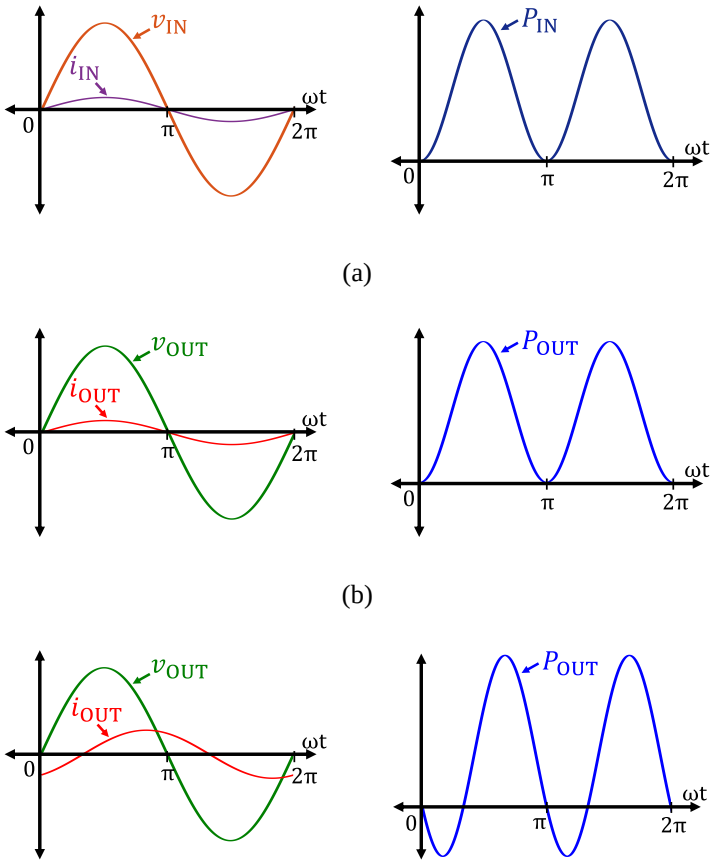



Fig. 5.6: Operating waveforms for the proposed UPS (a) instantaneous input voltage, input current, and input power of the rectification stage, (b) instantaneous output voltage, output current, and output power of the inversion stage powering a resistive load, at the same frequency and phase as the input voltage, and (c) instantaneous output voltage, output current, and output power of the inversion stage powering a reactive load at the same frequency and phase as the input voltage.

required for high frequency energy buffering at the switching frequency of the rectification and inversion stages. For the case of a reactive load even with the output voltage at the same frequency and phase as the input voltage (Fig. 5.6(c)), it can be seen that there is a difference between the instantaneous input and output powers; hence warranting a need for an intermediate energy storage element. Assuming that the output voltage has the same frequency and phase as the input voltage, the energy that the intermediate dc-bus capacitor must store and release is given by:

$$E_S = \frac{V_{OUT,rms} I_{OUT,rms} \sin(\theta)}{\omega_{line}}, \tag{5.1}$$

where, $V_{OUT,rms}$ is the rms output voltage, $I_{OUT,rms}$ is the rms output current, $\theta$ is the phase angle between the output voltage and the output current, and $\omega_{line}$ is the line frequency.

With a nominal dc-bus voltage of $V_{BUS}$ and a maximum allowed peak-to-peak bus voltage ripple of ($\Delta V_{BUS,pk-pk}$), the required dc-bus capacitance is given by:

$$C_{BUS} = \frac{V_{OUT,rms} I_{OUT,rms} \sin(\theta)}{\omega_{line} V_{BUS} \Delta V_{BUS,pk-pk}}. \tag{5.2}$$

A derivation of (5.1) and (5.2) is provided in Appendix A. As can be seen from (5.2) for a given nominal dc-bus voltage ($V_{BUS}$), the required capacitance is directly proportional to the reactive power drawn by the load (i.e.,$V_{OUT,rms} I_{OUT,rms} \sin(\theta)$) and inversely proportional to the allowed dc-bus voltage ripple ($\Delta V_{BUS,pk-pk}$). In the above analysis it is assumed that the size of the dc-bus capacitor is not dictated by the rms current requirement. By allowing a larger dc-bus voltage ripple the dc-bus capacitance requirement can be reduced, but this may decrease the efficiency and increase the control complexity of the rectification and inversion stages.

The conventional online UPS topology of Fig. 5.2 utilizes two capacitors ($C_{BUS,1}$ and $C_{BUS,2}$) of equal capacitance and voltage rating between the rectification and inversion stages. The energy storage and capacitance requirement for each of these capacitors is the same as that of the single capacitor in the proposed single dc-bus UPS topology. This is because $C_{BUS,1}$ buffers the full required reactive power during the positive half line cycle, while $C_{BUS,2}$ buffers the full required reactive power during the negative half line cycle, and both capacitors operate with the same nominal dc-bus voltage as the single dc-bus capacitor in the proposed online UPS, which buffers the reactive power in both the positive and the negative half line cycles. Hence, for any non-zero reactive power requirement the proposed topology results in a factor of two reduction in energy storage requirement and dc-bus capacitor volume compared to the conventional split dc-bus topology. This factor of two advantage in dc-bus capacitor volume also

exists for the proposed UPS topology if the phase and/or frequency of the output ac voltage is different from that of the input ac voltage.

The energy storage requirement for the proposed online UPS in case of different input and output line frequencies is also derived in this paper and is given by:

$$E_{S,\max} = \frac{P_{OUT}(\omega_{OUT}+\omega_{IN})}{\omega_{OUT}\omega_{IN}} \times \left|\sin\left(\frac{\pi\omega_{OUT}}{\omega_{OUT}+\omega_{IN}}\right)\cos\left(\frac{(2m_A-1)\pi\omega_{OUT}}{\omega_{OUT}+\omega_{IN}}\right)\right|, \quad (5.3)$$

where $P_{OUT}$ is the output power of the online UPS, $\omega_{IN}$ is the frequency of the input ac voltage, $\omega_{OUT}$ is the frequency of the output ac voltage, and $m_A$ can be computed by the following ceiling function:

$$m_A = \left\lceil \frac{(\omega_{OUT}+\omega_{IN})}{2|\omega_{OUT}-\omega_{IN}|} \right\rceil. \quad (5.4)$$

With a nominal dc-bus voltage of $V_{BUS}$ and a maximum allowed peak-to-peak bus voltage ripple of ($\Delta V_{BUS,pk-pk}$), the required dc-bus capacitance is given by:

$$C_{BUS} = \frac{P_{OUT}(\omega_{OUT}+\omega_{IN})}{V_{BUS}\Delta V_{BUS,pk-pk}\omega_{OUT}\omega_{IN}} \times \left|\sin\left(\frac{\pi\omega_{OUT}}{\omega_{OUT}+\omega_{IN}}\right)\cos\left(\frac{(2m_A-1)\pi\omega_{OUT}}{\omega_{OUT}+\omega_{IN}}\right)\right|. \quad (5.5)$$

A derivation of (5.3) and (5.5) is provided in the Appendix B.

## 5.3 CONTROL STRATEGY

The proposed online UPS comprises a PFC rectification stage and a voltage-mode inversion stage. The control strategy and controller design for each of these stages is described below.

### 5.3.1 RECTIFICATION STAGE CONTROL

The rectification stage of the online UPS is designed to operate at high frequency in both the boost and the buck-boost modes of operation in order to reduce the size of the input inductor ($L_{IN}$). To maintain high efficiency at high switching frequencies, the rectification stage is operated in boundary conduction mode (BCM) to enable zero-voltage switching (ZVS). Fig. 5.7 shows a time-exaggerated view of the

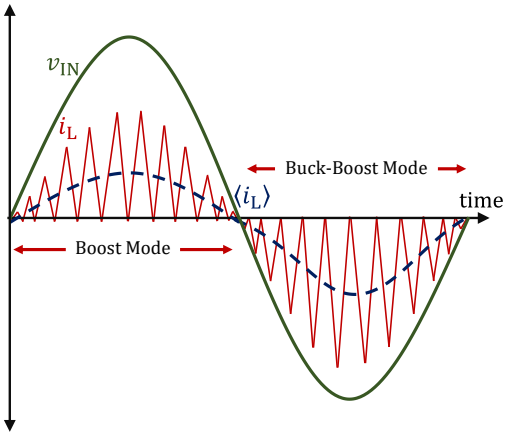



Fig. 5.7: Time-exaggerated view of inductor current $i_L$ (solid red line) and its average value $\langle i_L \rangle$ (dotted blue line) shown relative to the input voltage $v_{IN}$ (solid green line).

rectification stage's inductor current ($i_L$) under BCM operation. The average value of the inductor current $\langle i_L \rangle$ is also shown in Fig. 5.7. During the positive half line cycle, the rectification stage operates in boost mode and naturally achieves ZVS for both its switches when the instantaneous input voltage ($v_{IN}(t)$) is less than half the dc-bus voltage ($v_{IN}(t) < V_{BUS}/2$ ). However, for input voltage greater than $V_{BUS}/2$, ZVS is achieved only when the inductor current at the end of each switching cycle is less than certain negative value $i_{boost(min)}$ given as:

$$i_{boost(min)} \leq -\sqrt{\frac{2C_{OSS}}{L_{IN}} V_{BUS}(2v_{IN} - V_{BUS})}\,. \tag{5.6}$$

Here, $C_{OSS}$ is the capacitance of the boost switches ($S_1$ or $S_2$). For this purpose, the synchronous boost switch ($S_2$) is kept on for additional time after the inductor current zero-crossing to build up the required negative inductor current and ensure the ZVS turn-on of switch $S_1$ [120], [121]. During the negative half line cycle when the rectification stage is operating in buck-boost mode, the buck-boost switches $S_3$ and $S_4$ naturally achieve ZVS for $|v_{IN}| < V_{BUS}$. Since the buck-boost converter always operates in a step-up mode (i.e., $|v_{IN}| < V_{BUS}$), no additional synchronous switch $S_4$ on-time is required for switch $S_3$ to achieve ZVS turn-on during this operating mode (see Fig. 5.8(c)).

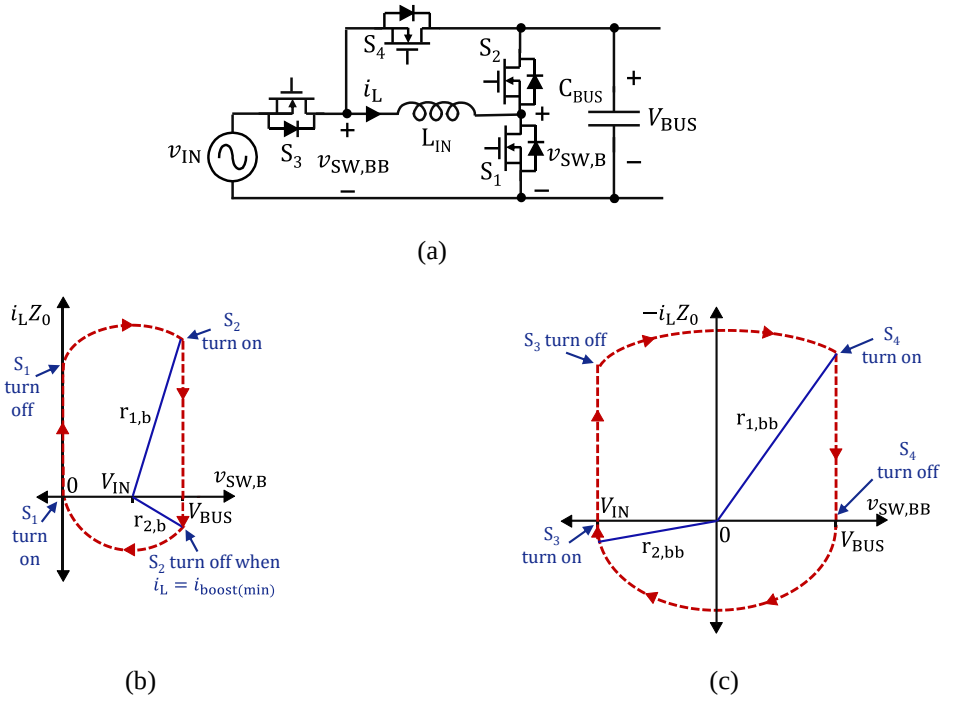



Fig. 5.8: Zero voltage switching (ZVS) of the transistors in the rectification stage: (a) rectification stage circuit, (b) state plane diagram for boost-mode operation, (c) state plane diagram for buck-boost-mode operation. Here $Z_0$ is the characteristic impedance given by $\sqrt{\frac{L_{IN}}{2C_{OSS}}}$ and the state variables $i_L$, $v_{SW,B}$, and $v_{SW,BB}$ are as labelled in (a).

As discussed in Chapter 2, the presence of sensor, control, and gate-drive delays can substantially affect the input current waveshape and performance of the BCM controlled rectification stage. Fig. 5.9(a) illustrates a time-exaggerated view of the rectifier stage's inductor current ($i_L$) and its average value $\langle i_L \rangle$, when the rectifier is operated in BCM. However, in practical scenarios, sensor, control, and gate-drive delays in the ZCD circuit will result in a time delay between the moment the inductor current crosses zero and the moment a trigger is produced at the output of the ZCD circuit. These delays can cause the synchronous switch ($S_2$ during boost mode and $S_4$ during buck-boost mode) to stay on for an extended period of time causing the average inductor current amplitude to fall. Figure 3(b) shows the inductor current ($i_L$) and its average value $\langle i_L \rangle$ in the presence of a sensor, control, and gate-drive delays ($t_{delay}$) in the ZCD circuit. As can be seen, in the boost mode, the minimum value of inductor current

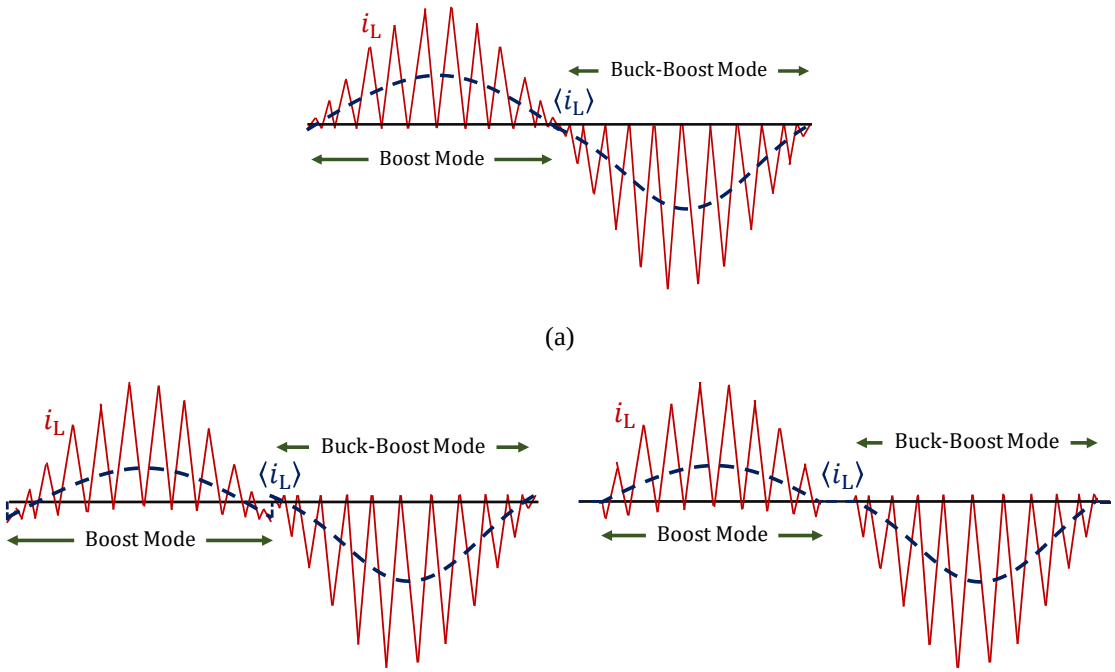



Fig. 5.9: Time exaggerated view of the inductor current ($i_L$) and its average value $\langle i_L \rangle$ when rectifier is operating in boundary conduction mode: (a) when sensor, control, and gate-drive delays are negligible, (b) when sensor, control, and gate-drive are significant, (c) when dead bands are introduced at low input voltages introducing distortion in average inductor current waveshape.

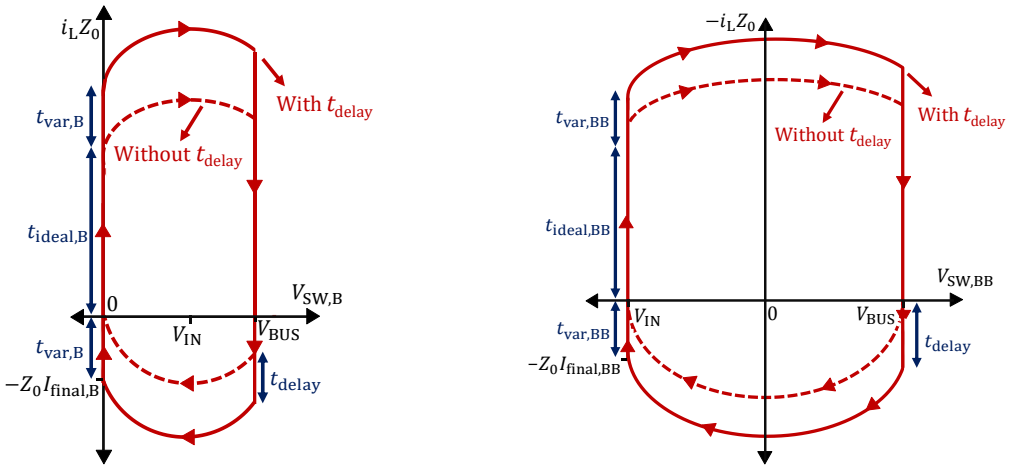
in a switching cycle becomes more negative and its value varies across the input voltage half-cycle. The decrease in the minimum inductor current value is given by:

$$\Delta I_{\mathrm{min,boost}} = \frac{(\mathrm{V_{BUS}} - v_{\mathrm{IN}})}{\mathrm{L_{IN}}} \mathrm{t_{delay}}, \tag{5.6}$$

Furthermore, in buck-boost mode the maximum inductor current in the presence of the sensor, control, and gate-drive delays will remain constant during the input voltage half-cycle and it will increase by the following value:

$$\Delta I_{\mathrm{max,buckboost}} = \frac{\mathrm{V_{BUS}}}{\mathrm{L_{IN}}} \mathrm{t_{delay}}, \tag{5.7}$$

The higher magnitudes of $\Delta I_{\mathrm{min,boost}}$ and $\Delta I_{\mathrm{max,buckboost}}$ will cause a decrease in the average inductor




(a) (b)

Fig. 5.10: Zero voltage switching (ZVS) of the transistors in the rectification stage in the presence of sensor, control, and gate-drive delays $t_{delay}$: (a) rectification stage circuit, (b) state plane diagram for boost-mode operation, (c) state plane diagram for buck-boost-mode operation.

current causing it to become more negative in boost mode and more positive in buck-boost mode at low input voltage magnitudes. As a result, at low input voltages, instantaneous power will be transferred back towards the input voltage source, thereby increasing circulating currents and causing a higher conduction loss. To prevent this, the converter is conventionally switched off at such low voltages introducing dead bands in the inductor current waveform. Fig. 5.9(c) shows the inductor current ($i_L$) and its average value $\langle i_L \rangle$ in the presence of such dead bands. As can be seen, the presence of dead bands introduces distortion in the input current wave shape, consequently, affecting the input current THD and power factor.

To improve the input current wave shape, an additional on-time value is required which compensates for the fall in average inductor current due to the sensing delay. Fig. 5.10 shows the state-plane diagram of inductor current and switch-node voltage in boost mode and buck-boost mode of the rectifier stage. As can be seen, additional on-time (in both modes) is required to maintain the average input current at its nominal value. These additional on-times for both operating modes are given by:

$$t_{extra,boost} = 2 \times t_{var,B}, \tag{5.8}$$

$$t_{\text{extra,buckboost}} = 2 \times t_{\text{var,BB}}, \tag{5.9}$$

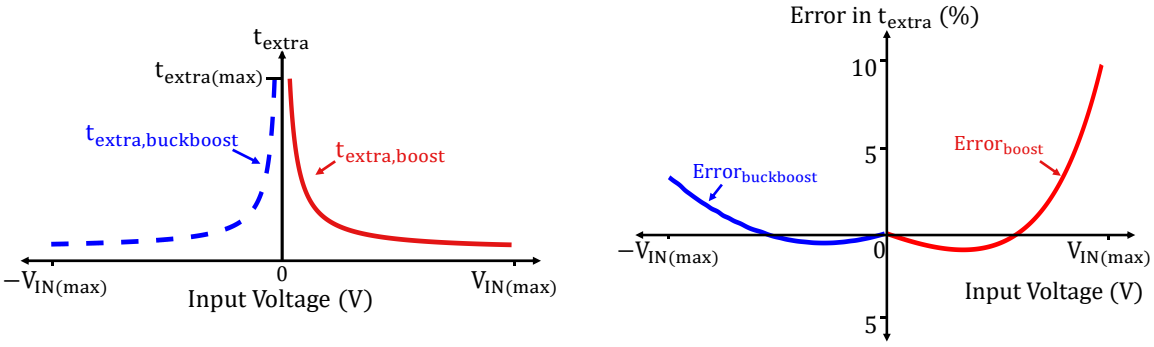
Where, $t_{\text{var,B}}$ is the time required for inductor current to increase from $-I_{\text{final,B}}$ to zero and $t_{\text{var,BB}}$ is the time required for inductor current to decrease from $I_{\text{final,BB}}$ to zero.

Fig. 5.11(a) shows the required $t_{\text{extra,boost}}$ and $t_{\text{extra,buckboost}}$ for a given value of switch-node capacitance, inductance, and dead-time in boost switches ($S_1$ and $S_2$) and buck-boost switches ($S_3$ and $S_4$), as input voltage magnitude is varied. The required extra on-times can be approximated in the form of following expressions:

$$t_{\text{extra,boost}} \approx \frac{\alpha_{\text{boost}}}{v_{\text{IN}}} + \beta_{\text{boost}}, \tag{5.10}$$

$$t_{\text{extra,buckboost}} \approx \frac{\alpha_{\text{buckboost}}}{|v_{\text{IN}}|} + \beta_{\text{buckboost}}, \tag{5.11}$$

Where, $\alpha_{\text{boost}}$, $\alpha_{\text{buckboost}}$, $\beta_{\text{boost}}$, and $\beta_{\text{buckboost}}$ can be found by curve fitting the on-time plot given in Fig. 5.11(a). Figure 5.11(b) shows the percentage error between the actual and the curve fitted on-time values. As can be seen, the error remains under 10% across the full input voltage range and the error is below 1% at low input voltage magnitudes where the impact of sensing delay is most prominent.




(a) (b)

Fig. 5.11: Compensation needed to mitigate the effect of sensor, control, and gate drive delay, $t_{\text{delay}}$ , when operating at an input voltage of $120V_{\text{rms}}$ and a dc-bus voltage of 225V: (a) Extra on-time required to restore input current waveshape, (b) Percentage error between the exact and curve-fitted extra on-time for the rectification stage.

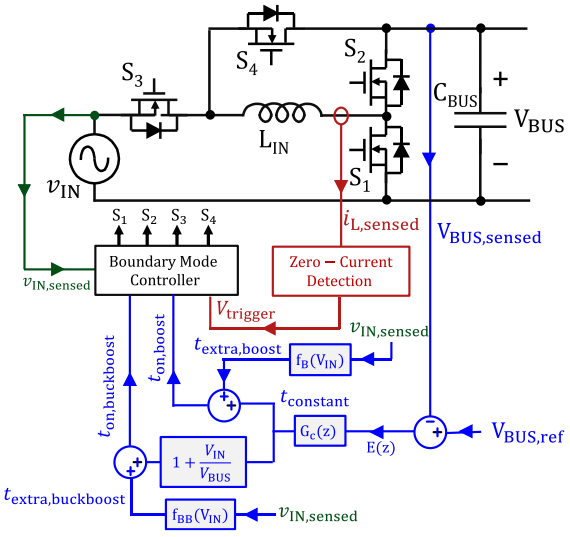



Fig. 5.12: Control architecture for the rectification stage.

The overall control architecture for the rectification stage of the proposed online UPS is shown in Fig. 5.12. In the proposed control, the output voltage of the rectification stage (i.e., the dc-bus voltage $V_{BUS}$) is regulated using a low bandwidth voltage loop comprising a PI compensator. The output of this compensator a dc-bus voltage loop $t_{constant}$ is fed into the on-time controller which generates the on-times for the boost and buck-boost mode of the rectifier stage, as given below:

$$t_{on,boost} = t_{constant} + t_{extra,boost}, \tag{5.12}$$

$$t_{on,buckboost} = t_{constant}\left(1 + \frac{|v_{in}|}{V_{BUS}}\right) + t_{extra,buckboost}, \tag{5.13}$$

A boundary mode controller utilizes these on-times to generate the gate-drive signals for all switches ($S_1$-$S_4$) based on the sensed input voltage polarity. For a positive input voltage, the boost switch $S_1$ is turned on for a given on-time $t_{on,boost}$. After that, the synchronous boost switch $S_2$ is turned on until the inductor current falls below $i_{boost(min)}$. For a negative input voltage, the buck-boost switch $S_3$ is turned on for a given on-time $t_{on,buckboost}$. After that, the synchronous buck-boost switch $S_4$ is turned on until the inductor current reaches zero. A zero-current detection (ZCD) circuit is implemented for that purpose (see Fig. 5.13). This ZCD circuit senses the inductor current and utilizes two hysteretic

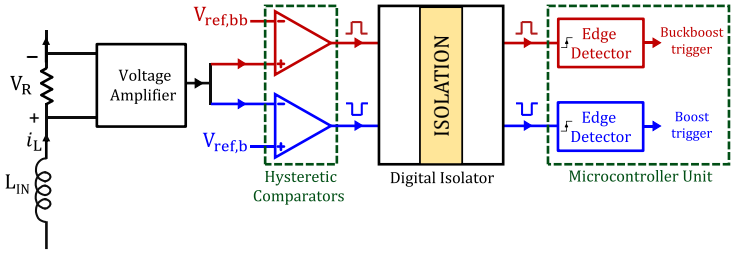
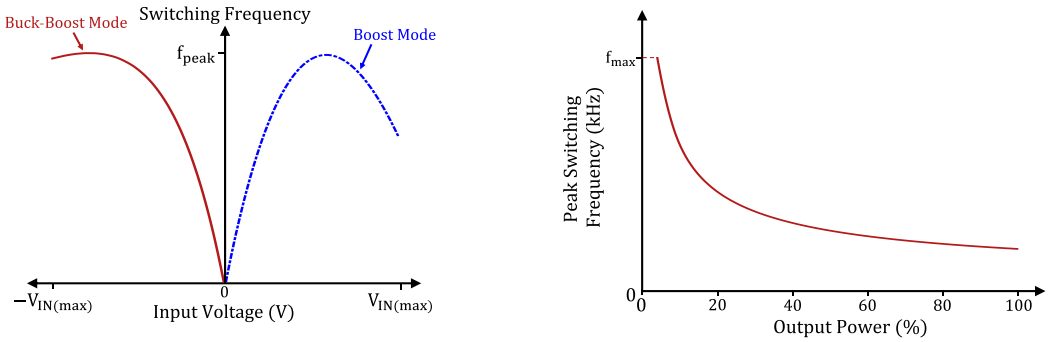



Fig. 5.13: Zero current detection (ZCD) circuitry utilized in the control of the rectification stage.

comparators, one for each input voltage half line cycle. For the positive half line cycle (in boost mode), the hysteretic comparator generates a trigger when the inductor current falls below $i_{\text{boost(min)}}$. Similarly, in the negative half line cycle (in buck-boost mode), the hysteretic comparator generates a trigger when inductor current reaches zero. The trigger in each half line cycle is detected by the microcontroller which resets the PWM counter and starts the next switching cycle.

The variation in switching frequency across the line cycle covering both modes of operation of the converter is shown in Fig. 5.14(a). The peak value of the switching frequency during the boost and the buck-boost modes of operation is a function of output power as shown in Fig 5.14(b). As can be seen from Fig. 5.14(b), the peak value of the switching frequency increases as output power is reduced. In practical designs, the maximum and minimum values of the switching frequency are typically limited




(a) (b)

Fig. 5.14: Switching frequency of the rectification stage: (a) variation in switching frequency as a function of input voltage reaching a peak value during both buck-boost and boost modes of operations, and (b) variation in peak value of switching frequency with output power.

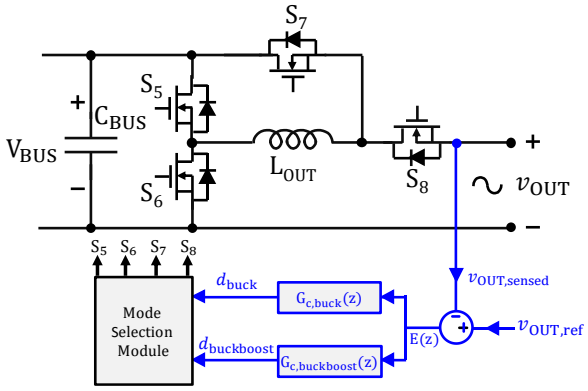



Fig. 5.15: Controller architecture for the inversion stage.

to limit losses and avoid saturation of the magnetics. The maximum switching frequency can be limited by operating the converter in discontinuous conduction mode (DCM), or the converter can continue to operate in BCM at the maximum frequency limit $f_{max}$ but with a somewhat distorted line current (resulting in increased THD) [130]. Similarly, for the lower frequency limit, the converter can be either turned off or operated at the fixed minimum switching frequency limit $f_{min}$ at the expense of increased input current THD.

### 5.3.2 INVERSION STAGE CONTROL

The inversion stage is designed to produce a sinusoidal ac voltage at the output of the online UPS. A voltage mode controller is utilized to regulate the output voltage for both real and reactive loads. In the proposed converter, the inversion stage is operated in CCM with a fixed switching frequency. BCM operation can also be utilized in inversion stage to achieve soft switching and reduce losses at the expense of increased sensing and control complexity. Additionally, output current control can be utilized for the inversion stage to enable other features including over current protection and current sharing in case of paralleled operation.

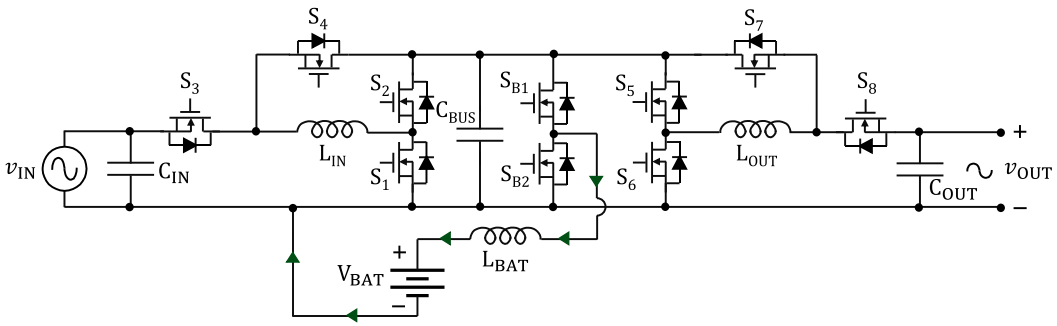
The control architecture for the inversion stage of the proposed online UPS is shown in Fig. 5.15. A sinusoidal voltage reference $v_{OUT,ref}$ is compared with the sensed output voltage $v_{OUT}$ to generate an error for the voltage-mode controller. The voltage-mode controller utilizes two voltage compensators

$G_{c,buck}$ and $G_{c,buckboost}$. For the positive output voltage half line cycle (in buck mode), the buck compensator $G_{c,buck}$ is activated to generate duty cycle for the buck switch $S_5$. In this operating mode, the output of buck-boost compensator is ignored and buck-boost switch $S_8$ is kept on. For the negative output voltage half line cycle (in buck-boost mode), the buck-boost compensator $G_{c,buckboost}$ is activated to generate duty cycle for buck-boost switch $S_7$. In this operating mode, the output of buck compensator is ignored and buck switch $S_6$ is kept on. The voltage-mode compensators for both operating modes are designed based on the duty-cycle-to-output voltage transfer functions and voltage mode controller design methodology of buck and buck-boost converters as explained in [131].

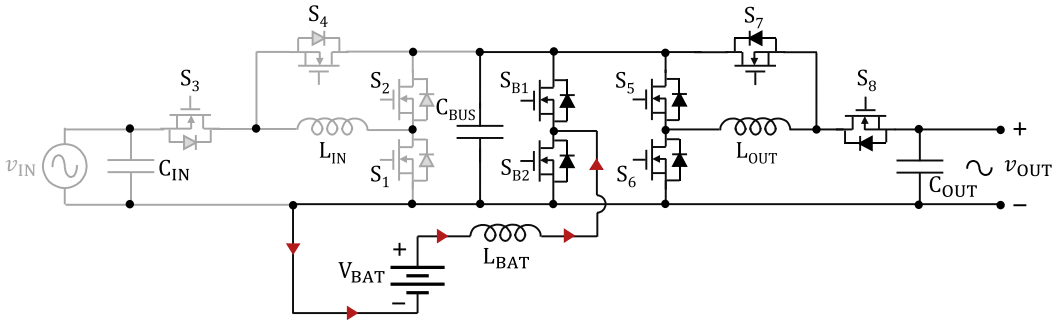
## 5.4 BATTERY INTERFACE

The proposed online UPS topology lends itself to multiple battery interface options to support the load in case of a grid outage. One possible battery interface is shown in Fig. 5.16. This approach utilizes a bi-directional dc-dc converter, comprising switches $S_{B1}$, $S_{B2}$, and inductor $L_{BAT}$ to interface the battery with the intermediate dc-bus. When the grid is stable, i.e., in the normal operation mode, and when the battery is not fully charged, the battery interface converter operates in buck mode (since $V_{BAT} < V_{BUS}$) and charges the battery from the intermediate dc-bus, as shown in Fig. 5.16(a). In case of a grid outage, the bi-directional dc-dc converter operates in boost mode and regulates the dc-bus voltage at its nominal value, thus ensuring an uninterrupted flow of power to the load, as shown in Fig. 5.16(b). A drawback of this battery interface architecture is that the bi-directional dc-dc converter must be rated for the peak output power of the UPS which reduces the overall power density of the online UPS.

To increase the overall power density of the UPS, a different battery interface architecture is proposed here that reduces the power processing requirement of the additional dc-dc converter, as shown in Fig. 5.17. This battery interface includes a dc-dc (buck) converter (comprising switches $S_{B1}$ and $S_{B2}$



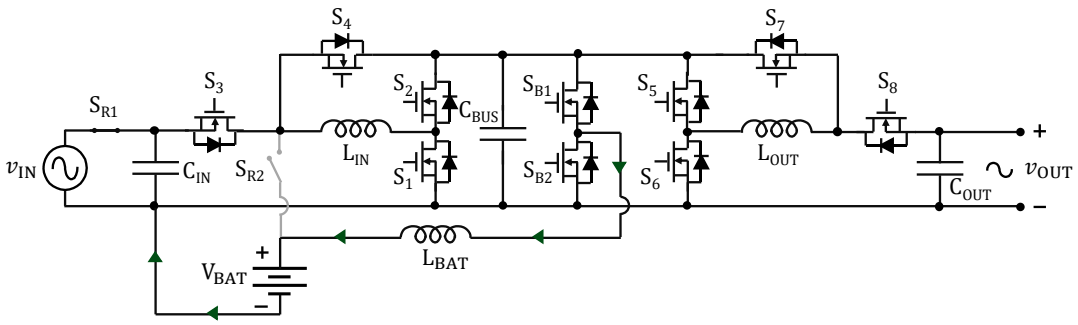

(a)



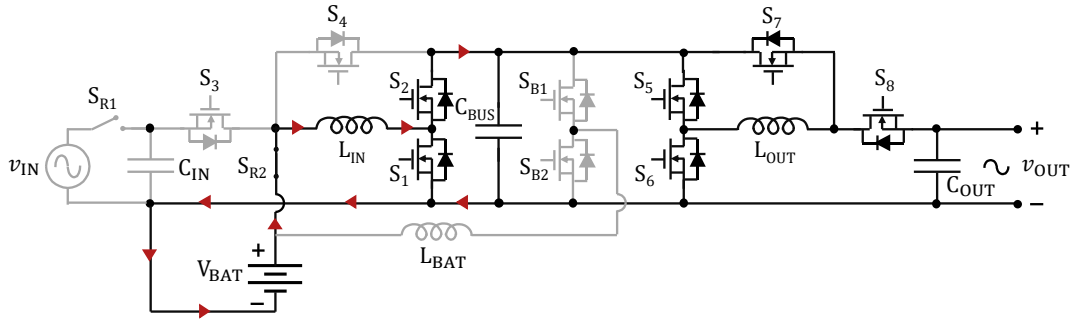

(b)

Fig. 5.16: Traditional battery interface architecture showing (a) the battery charging path in normal mode of operation, and (b) battery discharging path in backup mode of operation.

and inductor $L_{BAT}$) and two fast relays ($S_{R1}$ and $S_{R2}$) which can be implemented using back-to-back MOSFETs. The proposed architecture uses different paths for charging and discharging the battery. In the normal mode of operation when the battery is being charged, relay $S_{R1}$ is on and $S_{R2}$ is off and both the rectification and inversion stages are operating normally as discussed in Section 5.2. During this mode, the battery is charged from the dc-bus utilizing the dc-dc converter formed by switches $S_{B1}$ and $S_{B2}$ and inductor $L_{BAT}$ as shown in Fig. 5.17(a). Since this dc-dc converter is not used to power the load in case of a grid-outage, it is not rated for the full output power of the online UPS, instead it is rated based on the required charging rate of the battery. Typically, the power rating of the charger is substantially smaller than the power rating of the online UPS. In the case of a grid outage, relay $S_{R1}$ is turned off and $S_{R2}$ is turned on, connecting the battery to the input of an effective boost converter




(a)




(b)

Fig. 5.17: Proposed battery interface architecture showing (a) the battery charging path in normal mode of operation, and (b) battery discharging path in backup mode of operation.

comprising switches $S_1$ and $S_2$, and inductor $L_{IN}$ of the rectification stage as shown in Fig. 5.17(b). This rectification stage's boost converter, which is already rated for the peak output power of the online UPS, delivers power to the dc-bus and hence ensures continued power delivery to the load via the inversion stage. This proposed battery interface replaces a peak-power rated bi-directional dc-dc converter with a reduced power rating buck converter at the expense of two relays.

Typically, the battery charger power rating is under 15% of the online UPS power rating [132]-[134]. The proposed online UPS is also designed to have a similar ratio between the power rating of the battery charger and the UPS, resulting in a 150-W battery charger for the 1-kVA online UPS. If the proposed online UPS did not have the ability to utilize the main power stage to power the load in backup mode, it would have required a 1-kW bi-directional dc-dc converter between the battery and its dc-bus.

Hence, the proposed online UPS topology reduces the power rating of the additional battery interface by 85%, resulting in a significant reduction in the overall volume of the proposed online UPS.

## 5.5 PROTOTYPE DESIGN AND OPTIMIZATION

An online UPS based on the proposed topology of Fig. 3 is designed to deliver up to 1 kVA of power to loads with power factor ranging from -0.5 to +0.5 and able to operate with an input voltage of 120 $V_{rms}$ at 50-60 Hz line frequency and an ac output voltage of 120 $V_{rms}$ at 60 Hz. The complete specifications for the designed system, including the nominal dc-bus voltage, are given in Table 5.1. To optimize the power density of the proposed online UPS, a design methodology is developed to find a reasonable trade-off between its passive volume and efficiency for the given specifications. To estimate the system efficiency, a loss model is developed that incorporates switching and conduction losses in the switches $S_1$-$S_8$, winding and core losses in the inductors $L_{IN}$ and $L_{OUT}$, and ESR losses in the dc-bus capacitor.

The rectification stage is designed to operate in BCM with the peak inductor current given as follows:

TABLE 5.1: SPECIFICATIONS OF THE ONLINE UPS

| | |
|---|---|
| Input Voltage | 120 $V_{rms}$ |
| Line Frequency | 50-60 Hz |
| Output Voltage | 120 $V_{rms}$ |
| Output Frequency | 60 Hz |
| Nominal DC-Bus Voltage | 225 V |
| Peak Output Power | 1 kVA |

$$i_{\mathrm{LIN,BCM,peak}} = \max\left\{\begin{matrix}\frac{4P_{\mathrm{IN}}}{V_{\mathrm{IN,peak}}} + \sqrt{\frac{2C_{\mathrm{OSS}}}{L_{\mathrm{IN}}}V_{\mathrm{BUS}}\left(2V_{\mathrm{IN,peak}} - V_{\mathrm{BUS}}\right)}, \\ \frac{4P_{\mathrm{IN}}}{V_{\mathrm{IN,peak}}}\left(1 + \frac{V_{\mathrm{IN,peak}}}{V_{\mathrm{BUS}}}\right)\end{matrix}\right\}, \tag{5.14}$$

where, $P_{\mathrm{IN}}$ is the input power of the online UPS and $V_{\mathrm{IN,peak}}$ is the peak input voltage. Since the rectification stage operates in BCM with ZVS across the full operating range, the switching losses for all its devices are negligible and the dominant loss mechanism is conduction loss in the switches $S_1 - S_4$ and the inductor $L_{\mathrm{IN}}$. The maximum switching frequency of the rectification stage is designed to be 500 kHz, which is reached when the output power drops to below 10% of the rated output power. This results in an inductance requirement of 38 µH for the rectification stage.

Similarly, the peak inductor current for the inversion stage operating in CCM can be found as:

$$i_{\mathrm{LOUT,CCM,peak}} = \max\left\{\begin{matrix}\frac{2P_{\mathrm{OUT}}}{V_{\mathrm{OUT,peak}}} + \frac{V_{\mathrm{OUT,peak}}}{2L_{\mathrm{OUT}}f_{\mathrm{SW}}}\left(1 - \frac{V_{\mathrm{OUT,peak}}}{V_{\mathrm{BUS}}}\right), \\ \frac{2P_{\mathrm{OUT}}}{V_{\mathrm{OUT,peak}}}\left(1 + \frac{V_{\mathrm{OUT,peak}}}{V_{\mathrm{BUS}}}\right) + \frac{V_{\mathrm{OUT,peak}}V_{\mathrm{BUS}}}{2L_{\mathrm{OUT}}f_{\mathrm{SW}}(V_{\mathrm{OUT,peak}}+V_{\mathrm{BUS}})}\end{matrix}\right\}, \tag{5.15}$$

where, $V_{\mathrm{OUT,peak}}$ is the peak output voltage, $L_{\mathrm{OUT}}$ is the inductance, and $f_{\mathrm{SW}}$ is the switching frequency of the inversion stage. The inversion stage is designed to operate in CCM at a fixed switching frequency.

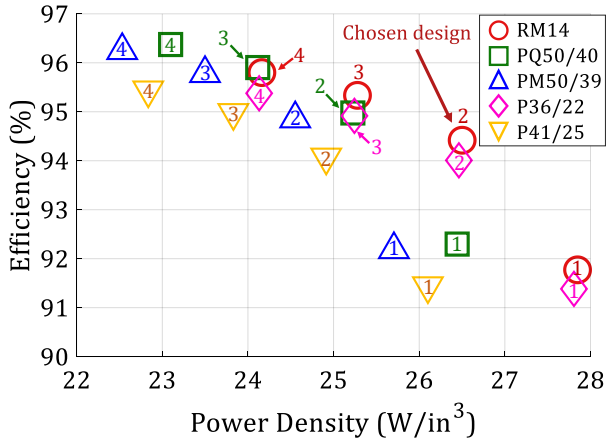



Fig. 5.18: Efficiency and power density of various design options for the online UPS, utilizing different number of paralleled transistors and different inductor cores. The numeric label on each design option represents the number of paralleled transistors used to implement each switch of the UPS.

Since the inversion stage does not achieve ZVS for most of the operating range, both the switching and conduction losses need to be account ed for. To obtain a reasonable tradeoff between the conduction and switching losses, an operating frequency of 100 kHz is selected for the inversion stage along with an inductance of 40 μH.

With these design specifications, the efficiency and power density (as a proxy for volume) of the proposed online UPS are determined for different number of paralleled transistors (ranging from 1 to 4), and different inductor cores (RM14, PQ50/40, PM50/39, P36/22, P41/25). The calculated efficiency and power density of the designs using different number of paralleled transistors and different cores are shown in Fig. 5.18. As can be seen from Fig. 5.18, designs that utilize lower number of paralleled transistors have better power density, because of the reduced board area taken by the transistors and the associated gate drive circuitry but result in lower efficiencies as the designs are conduction loss dominated. As a reasonable trade-off between power density and efficiency, a design option with two paralleled GaN transistors is chosen, as shown in Fig. 5.18. This design utilizes an RM-14 core with N49 magnetic material for both inductors $L_{IN}$ and $L_{OUT}$.

For the design of the intermediate dc-bus capacitance, the maximum allowed peak-to-peak voltage ripple is limited to 15%. This results in a minimum required capacitance of 300 μF for the specifications given in Table 5.1. To achieve a long lifetime, no electrolytic capacitors were utilized. Instead, lower energy density film capacitors were used in the prototype online UPS. The components used in the prototype online UPS are listed in Table 5.2.

## 5.6 EXPERIMENTAL RESULTS

A 1-kVA prototype online UPS based on the optimized design of Section 5.5 is designed, built, and tested. A photograph of the prototype is shown in Fig. 5.19. The eight switches in the converter are realized using 650-V 30-A eGaN transistors (GaN Systems GS66508T). For the closed loop control, a

TABLE 5.2: COMPONENTS USED IN THE PROTOTYPE ONLINE UPS

| Component | Value | Description |
|---|---|---|
| $C_{IN}$ | 6 x 2.2μF | 450-V X6S Ceramic Capacitors |
| $C_{OUT}$ | 12 x 2.2μF | 450-V X6S Ceramic Capacitors |
| $S_1 - S_8$ | – | 650-V, 30-A GaN E-HEMT |
| $L_{IN}$ | 38μH | RM-14 EPCOS N49 (20 turns) |
| $C_{BUS}$ | 3 x 100μF | 450-V Polypropylene film capacitor |
| $L_{OUT}$ | 40μH | RM-14 EPCOS N49 (22 turns) |

200-MHz, 32-bit digital controller (Texas Instruments TMS320F28379D) in conjunction with the inductor current zero crossing detection (ZCD) circuit of Fig. 5.13 are utilized. The electrolytic-capacitor-free prototype online UPS has a box volume of 37.8 $in^3$ and achieves a power density of 26.4 $W/in^3$.

Fig. 5.20 shows the experimentally measured waveforms of the online UPS while it is operating in normal mode. Fig. 5.20(a) shows the ac input voltage, filtered ac input current, the inductor current, and the dc-bus voltage with the rectification stage operating in boundary conduction mode. It can be seen that the peak inductor current in the positive half line cycle (boost mode) is smaller than the peak inductor current in the negative half line cycle (buck-boost mode). This is expected since volt-seconds across the inductor $L_{IN}$ are higher in buck-boost mode as compared to the boost mode. Thereby, the inductor current has higher peak-to-peak ripple and therefore, higher peak currents in buck-boost mode. The sinusoidal input current is in-phase with the input voltage, verifying the rectification stage's PFC operation. Fig. 5.20(b) shows the steady state ac output voltage and output current of the inversion stage

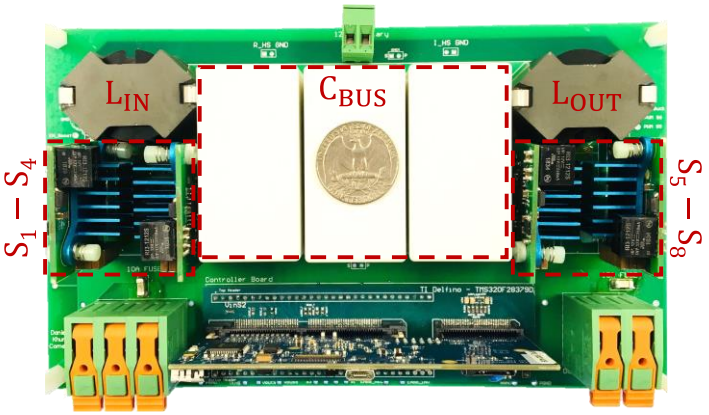
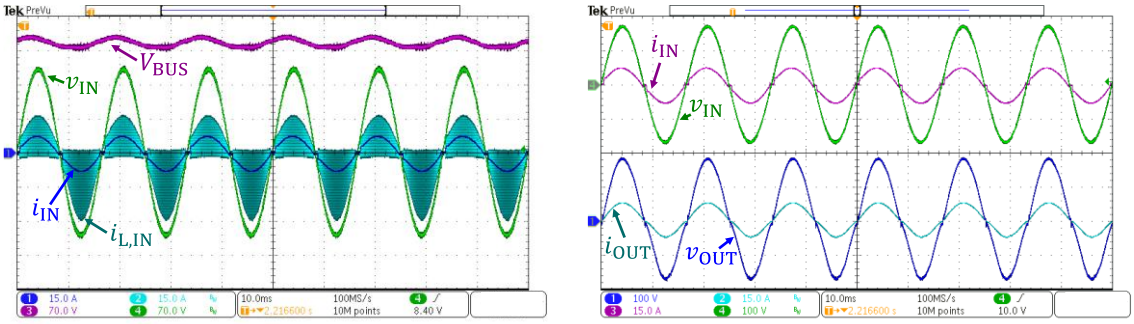



Fig. 5.19: Photograph of the 1-kVA electrolytic-free prototype online UPS which achieves a power density of 26.4 W/in$^3$. The prototype exhibits this power density despite utilizing lower energy density, but longer life, film capacitors instead of high energy density electrolytic capacitors for energy buffering.

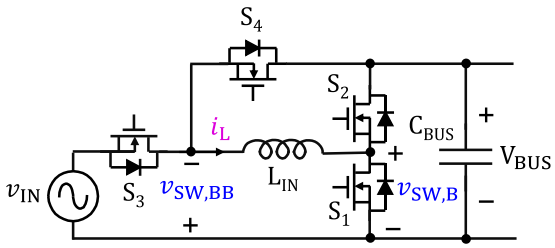



(a) (b)

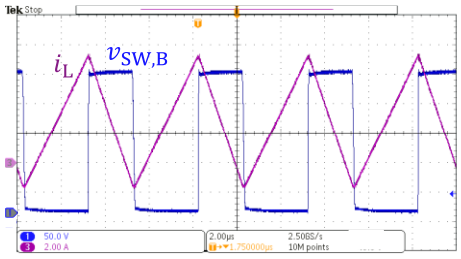
Fig. 5.20: Steady-state operating waveforms of the proposed online UPS in normal mode. (a) Input voltage (70V/div), input current (15A/div), inductor current (15A/div), and dc-bus voltage (70V/div) of the rectification stage demonstrating boundary conduction mode control, (b) Input voltage (100V/div), input current (15A/div), output voltage (100V/div), and output current (15A/div) of the online UPS while it is operating in normal mode.

along with the ac input voltage and input current of the rectification stage. The inversion stage generates a 120$V_{rms}$ sinusoidal output voltage, validating the output voltage mode control and operation of online UPS under normal mode.

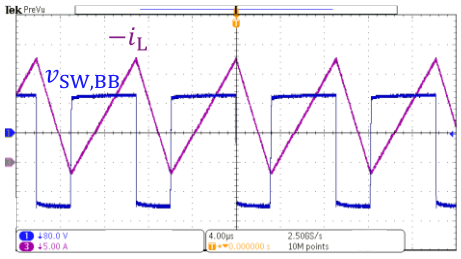
Fig. 5.21(b) and 5.21(c) show zoomed-in waveforms for the rectification stage's inductor current and the boost and buck-boost switch-node voltages, respectively. The polarity of the measured




(a)




(b)

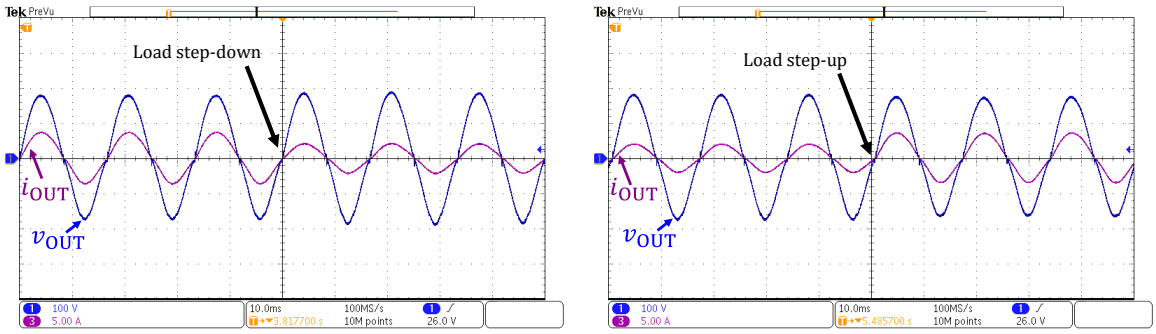



(c)

Fig. 5.21: Steady-state operating waveforms of the rectification stage: (a) rectification stage circuit, (b) zoomed-in waveforms of the inductor current $i_L$ (2A/div) and boost switch-node voltage $v_{SW,B}$ (50V/div) while the rectification stage is operating in boost mode, (c) zoomed-in waveforms of the inductor current $i_L$ (5A/div) and buck-boost switch-node voltage $v_{SW,BB}$ (80V/div) while the rectification stage is operating in buck-boost mode.

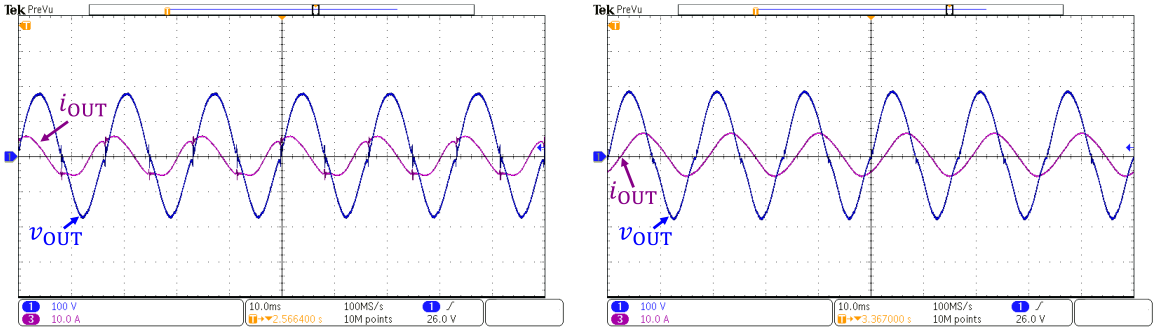
waveforms is indicated in schematic of Fig. 5.21(a). It can be seen that the converter is operating in BCM and ZVS is achieved for switches $S_1$ and $S_2$ in boost mode, and switches $S_3$ and $S_4$ in buck-boost mode of the rectification stage. Some additional negative and positive current was observed in boost and buck-boost modes respectively due to ZCD sensor and gate-driver propagation delays, which were compensated for by appropriately modifying the thresholds of the ZCD hysteretic comparators (see Fig. 5.13).

Fig. 5.22 shows the output voltage and current waveforms of the inversion stage during a 300W to 150W step-down load transient (see Fig. 5.22(a)) and 150W to 300W step-up load transient (see Fig. 5.22(b)). Fig. 5.23 shows the output voltage and current waveforms of the online UPS for reactive loads. Fig. 5.23(a) shows the output voltage and output current of the inversion stage for a 0.5 power-factor




(a) (b)

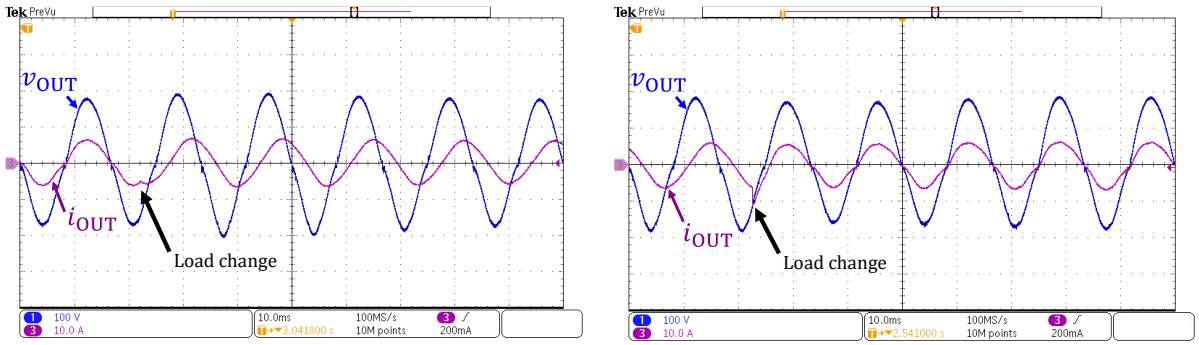
Fig. 5.22: Operating waveforms of the online UPS during load step transients at the output. Output voltage (100V/div) and output current (5A/div) during: (a) load step-down transient from 300W to 150W, (b) load step-up transient from 150W to 300W.




(a) (b)

Fig. 5.23: Steady-state operating waveforms of the proposed online UPS while powering non-unity power factor (reactive) load. Output voltage (100V/div) and output current (10A/div) while powering: (a) 0.5 power factor capacitive load, (b) 0.5 power factor inductive load.

capacitive load and Fig. 5.23(b) shows the output voltage and output current of the inversion stage for a 0.5 power-factor inductive load. Fig. 5.24(a) shows the output ac voltage and output ac current for a step change in load from 500W (resistive) load to 500VA 0.5 power-factor (reactive) load. Similarly, Fig. 5.24(b) shows the output ac voltage and output ac current for a step change in load from 500VA 0.5 power-factor (reactive) load to 500W (resistive) load. As can be seen, for all these operating conditions and load transients, the output ac voltage amplitude and waveshape is well regulated by the voltage-mode controller in the inversion stage.




(a) (b)

Fig. 5.24: Operating waveforms of the online UPS during load step at the output. Output voltage (100V/div) and output current (10A/div) during: (a) load step change from 500W resistive load to 500VA 0.5 power-factor reactive load. (b) load step change from 500VA 0.5 power-factor reactive load to 500W resistive load.

Experimentally measured efficiencies of the rectification and inversion stages are shown in Fig. 5.25(a) and Fig. 5.25(b), respectively. The rectification stage achieves a peak efficiency of 98.4% and the inversion stage achieves a peak efficiency of 97.3%. Fig. 5.25(a) and Fig. 5.25(b) also shows the predicted efficiencies for both stages based on the loss models used for optimization. A notch is observed in the efficiency of the inversion stage at around 500W output power. This is because below this power level, the switch turn-off currents for the inversion stage start going negative. As a result, the inversion stage achieves either partial or full zero-voltage switching leading to reduced losses and improved efficiency. The measured efficiencies match well with the theoretically predicted efficiencies. The end-to-end (ac-dc-ac) efficiency of the prototype online UPS is shown in Fig. 5.25(c). The online UPS achieves a peak efficiency of 95.4% and a full load efficiency of 92.6%. The input power factor and input current THD of the online UPS while it is operating in normal mode is shown in Fig. 5.26. The converter achieves a high input power factor across the full load range, validating the PFC operation of the rectification stage.

The modelled power loss distribution of the online UPS rectification and inversion stages are shown in Fig. 5.27. Fig. 5.27(a) shows the loss distribution in the rectification stage while it is operating in boost and buck-boost modes, and Fig. 5.27(b) shows the loss distribution in the inversion stage while it is

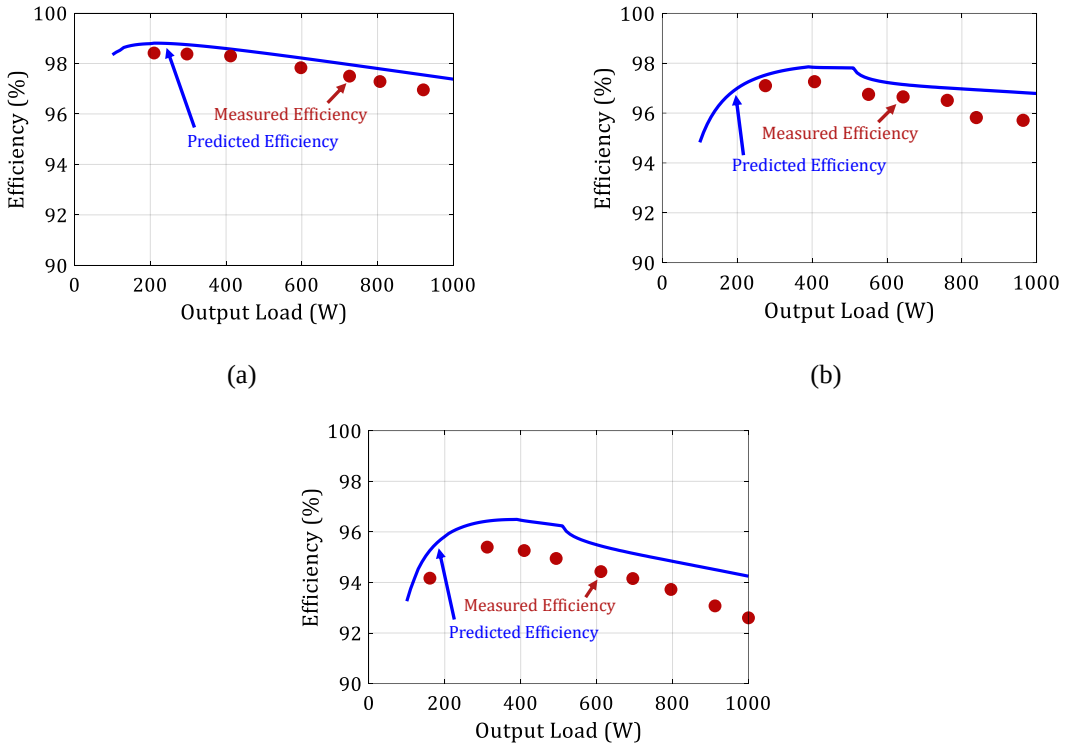



Fig. 5.25: Experimentally measured and theoretically predicted efficiencies of: (a) rectification stage operating as a PFC stage converting 120-$V_{rms}$, 60-Hz ac input voltage to a 225-V dc bus voltage across capacitor $C_{BUS}$, (b) inversion stage converting the 225-V dc-bus voltage to 120-$V_{rms}$, 60-Hz ac output voltage across a resistive load, (c) full online UPS converting the 120-$V_{rms}$, 60-Hz ac input voltage to 120-$V_{rms}$, 60-Hz ac output voltage in normal mode of operation.

operating in buck and buck-boost modes. As can be seen, in both the rectification and inversion stages, the largest fraction of losses is due to device conduction losses in the buck-boost mode. These are followed by the inductor losses in the buck-boost mode. It is also observed that in each stage of the online UPS, 72% of the losses occur while operating in the buck-boost mode and only 28% of the losses occur while operating in boost or buck modes.

The battery interface proposed in Section 5.4 is also experimentally validated using a 72-V battery. Fig. 5.28 shows the measured waveforms while the battery interface is operating in backup mode (see Fig. 5.17(b)). As can be seen, the dc-bus voltage is being regulated at its the nominal value (225 V)

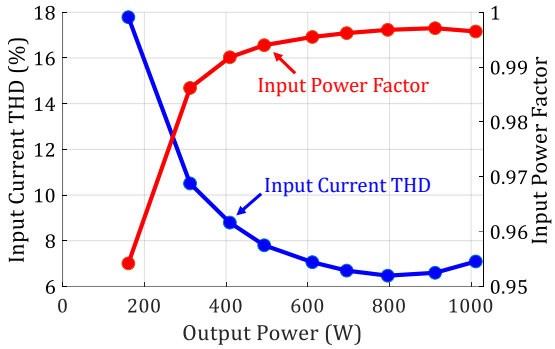
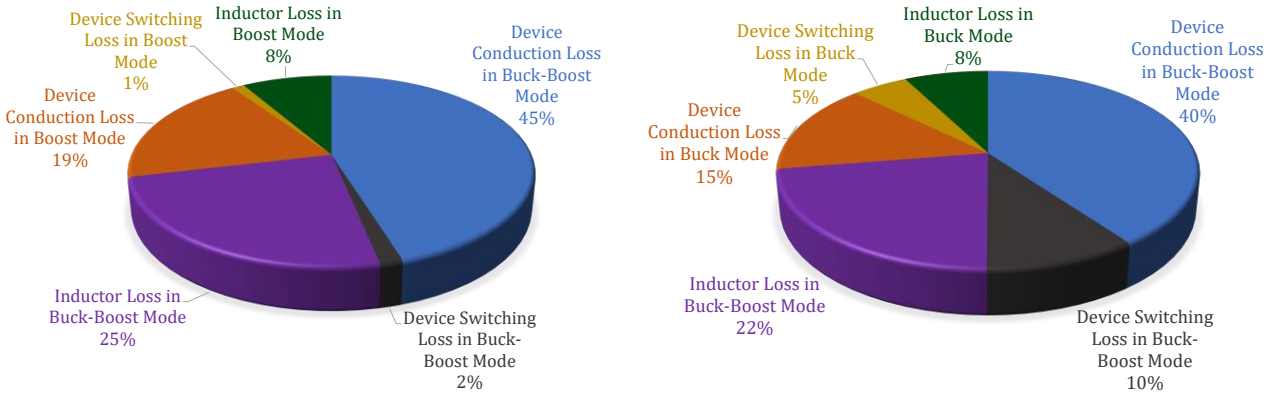



Fig. 5.26: Experimentally measured input power factor and input current THD as a function of output power with online UPS operating to convert 120-$V_{rms}$, 60-Hz ac input voltage to 120-$V_{rms}$, 60-Hz ac output voltage in normal mode of operation.




(a) (b)

Fig. 5.27: Power loss distribution in: (a) rectification stage, and (b) inversion stage based on theoretical models when the online UPS is operating at an ac input voltage of 120$V_{rms}$, nominal dc-bus voltage of 225V, output ac voltage of 120$V_{rms}$, and output power of 1kW.

while boost stage comprising switches $S_1$ and $S_2$, and inductor $L_{IN}$ is operating in BCM. Fig. 5.29 shows the operating waveforms of the online UPS when the UPS transitions from the normal mode to backup mode while utilizing the proposed battery interface. It can be seen that the dc-bus falls briefly after the input ac supply is disconnected. However, the battery discharge controller stabilizes the dc-bus voltage (at its nominal value of 225V) shortly after the UPS transitions to backup mode. Moreover, negligible distortion is seen in the output voltage due to the mode transition, and the output voltage amplitude and

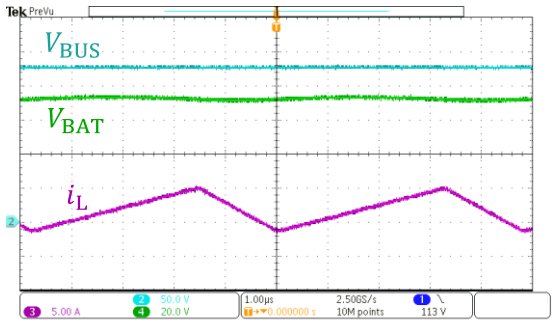



Fig. 5.28: Steady-state operating waveform of battery voltage $V_{BAT}$ (20V/div), inductor current $i_L$ (5A/div), and dc-bus voltage $V_{BUS}$ (50V/div) when a 72-V battery connected to the online UPS is discharged (in backup mode).

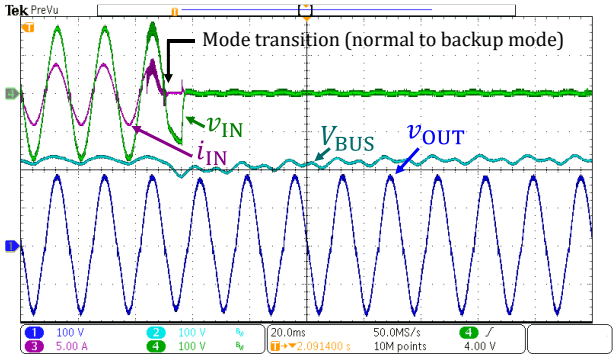



Fig. 5.29: Operating waveforms of the input voltage (100V/div), input current (5A/div), dc-bus voltage (100V/div), and output voltage (100V/div) of the online UPS when the UPS transitions from the normal mode to backup mode.

waveshape is well regulated by the voltage mode controller of the inversion stage. The experimentally measured efficiency of the battery interface is shown in Fig. 5.30. The battery interface achieves a peak efficiency of 98.9% and maintains an efficiency of above 97% across a wide output power range.

Table 5.3 shows a comparison of the prototype online UPS with state-of-the-art online UPS from literature. It can be seen that the proposed online UPS has much better efficiency as compared to the existing designs with similar input/output voltages and output power rating.

TABLE 5.3: PERFORMANCE COMPARISON WITH STATE OF THE ART ONLINE UPS OF SIMILAR SPECIFICATIONS

| Reference | Output Power | Input Voltage ($V_{rms}$) | Output Voltage ($V_{rms}$) | Topological Configuration | Type of Devices Used | Operating Frequency (kHz) | Peak Efficiency | Input Power Factor at Full Load | Input Current THD at Full Load |
|---|---|---|---|---|---|---|---|---|---|
| This work | 1kVA /1kW | 120 | 120 | Non-isolated | GaN MOSFET | 50 – 500 | 95.4% at 310W | 0.997 | 7.43% |
| [87] | 1kVA /700W | 220 | 110 | Isolated | Si (IGBT + MOSFET) | 20 – 50 | 85% at 300W | 0.99 | Not Provided |
| [88] | 2kVA | 110/220 | 110 | Isolated | Si MOSFET | 50 | 89.5% at 550W | > 0.99 | Not Provided |
| [89] | 1kVA /700W | 80-120 | 100 | Isolated | Si MOSFET | 60 | 83% at 400W | Unity | < 3% |
| [106] | 1.3kVA | 127 | 127 | Non-isolated | Si IGBT | 50 | 88% at 1.1kW | 0.99 at 500W | 3.4% at 500W |
| [107] | 600VA /500W | 120 | 120 | Non-isolated | Si IGBT | 10 | 93.9% at 500W | Unity | 0.74% |
| [109] | 2kVA /1.5kW | 127 | 127 | Non-isolated | Si IGBT | 10 | 92.3% at 1.15kW | Unity | 1.77% |

## 5.7 CHAPTER SUMMARY

This chapter presents a new transformer-less ac-dc-ac converter topology suitable for a high-power-density high-frequency single-phase online uninterruptible power supply (UPS) with a common neutral between the input and output ac ports. The proposed converter comprises an input power factor correction (PFC) rectification (ac-dc) stage which is followed by a voltage-mode inversion (dc-ac) stage. The rectification stage operates either in a boost or a buck-boost mode depending on the polarity of the line voltage. Similarly, the inversion stage operates in either a buck or a buck-boost mode depending on the desired polarity of its output voltage. The rectification stage utilizes boundary conduction mode (BCM) control, enabling soft-switching and allowing high frequency operation. The inversion stage is operated in continuous conduction mode (CCM), and a digital controller regulates the output voltage of the online UPS across both resistive and reactive loads. The proposed online UPS topology utilizes a single dc-bus between its rectification and inversion stages, resulting in a 50% reduction in dc-bus capacitance requirement compared to conventional split dc-bus online UPS topologies. Additionally, two battery interface solutions are considered which provide an opportunity to trade-off between passive volume and switch-count. To verify the performance and control of the proposed online UPS, a GaN-based electrolytic-free 1-kVA prototype online UPS is designed, built, and tested. The prototype UPS achieves a peak efficiency of 95.2% and maintains a high efficiency of above 92.3% across the entire output power range. The electrolytic-free prototype online UPS achieves a power density of 26.4 W/in$^3$.

# CHAPTER 6

# SUMMARY AND CONCLUSIONS

Single-phase line-interfaced power converters are widely utilized in several applications, including consumer electronics, lighting, telecommunications, data centers, electrified transportation, medical, and defense. Their use is rapidly increasing due to rising global electricity demands, need for higher power quality, and the evolving nature of electrical loads. Consequently, there is greater focus on the performance of single-phase line-interfaced power converters. In most applications, these converters are required to achieve high power density and high conversion efficiencies to meet space and power loss constraints. To achieve these objectives, this thesis has explored several opportunities to reduce the power converter volume while enhancing its overall conversion efficiency.

## 6.1 THESIS SUMMARY AND CONCLUSIONS

This thesis presents the design and control strategies aimed at enhancing power density and conversion efficiencies of single-phase line-interfaced power converters that draw electrical power from ac-line. Such converters comprise ac-dc and ac-ac converters. To achieve a broad coverage of the entire application space, three strategic applications have been addressed encompassing ac-dc converters for electronic equipment, ac-ac converters for lighting applications, and ac-dc-ac converters for data-center online UPS.

Chapter 2 presents a high-power-density high-efficiency soft-switched single-phase universal-input to 28V-output isolated ac-dc converter module for use in electronic equipment. The proposed two-stage converter utilizes a totem-pole bridgeless boost power-factor correction stage followed by an isolated LLC resonant dc-dc stage [135]. A new comprehensive design methodology is presented which compares various designs and operating modes for the converter modules' power stage and selects the optimal design based on overall power density and efficiency. For the selected design, a control scheme

is presented for the PFC stage to minimize current distortion by accounting for various sensor, control, and gate-drive delays while ensuring zero-voltage switching (ZVS) of the transistors. To validate the proposed design and control strategy, a 1-kW universal-input to 28V-output isolated ac-dc converter is built and tested. The prototype converter achieves a high power density of 84W/in$^3$ and a peak efficiency of greater than 93%.

Next, in chapter 3, the functionality of the above-mentioned isolated ac-dc converter module is further enhanced by introducing a new droop control methodology to achieve parallel operation [136]. By achieving parallel operation, the ac-dc converter module can be used to meet several ac-dc converter applications spanning a wide range of power levels while providing manufacturing cost reduction through economies of scale and increased system reliability through redundancy. The proposed control approach employs the input current of the secondary dc-dc conversion stage (LLC converter) to estimate the output current of the converter module, thereby eliminating need for costly and complex isolated sensing circuitry to measure high output current. The proposed input-current based droop control strategy achieves adequate output current distribution between paralleled modules when powering a common output load. The proposed droop control strategy also incorporates a variable droop resistance based on the instantaneous value of the dc-bus voltage to compensate for the effect of the twice-line frequency dc-bus voltage ripple and ensure a stable output dc-voltage. To validate the proposed control strategy, two 1-kW universal input to 28V-output isolated ac-dc converter modules are designed, built, and tested. The prototype system achieves a current distribution error of less than 2% at the peak output power of 2kW while maintaining a high conversion efficiency of greater than 91% across a 3:1 output power range.

Next chapter 4 presents two low-cost high-efficiency high-power-density single-stage 480V$_{rms}$ to 264V$_{rms}$ ac-ac converters for LED lighting applications. The first ac-ac converter utilizes a 2-level ac-ac buck converter topology and the second ac-ac converter utilizes a 3-level center-point-clamped (CPC) ac-ac buck converter topology. The first topology is chosen owing to its lower overall component count

potentially allowing lower component cost, while the second topology is chosen based on its ability to utilize lower-voltage switches and multi-level operation potentially saving switch cost and inductor volume. Both topologies demonstrate high performance while achieving overall component cost comparable with the conventional ac-ac conversion solution -- a line-frequency transformer. This is achieved through a comprehensive cost and efficiency optimization methodology that helps identify the most appropriate converter designs across a design space comprising various switch structures, a range of operating frequencies, and different inductance values. Moreover, control strategies are also presented for both ac-ac converters to regulate their output voltage and a switching scheme is introduced that ensures smooth inductor current commutation during switching transitions and reduces zero-crossing distortion in the input. Furthermore, an active voltage balancing scheme is developed for the 3-level CPC ac-ac converter to compensate for any imbalances between the two stacked input capacitors to ensure robust converter operation [137]. Two 600-W ac-ac prototype converters based on the proposed optimization, designed to operate at an input voltage of $480V_{rms}$ and an output voltage of $264V_{rms}$ are built and tested. Both prototyped converters achieve high conversion efficiencies exceeding 96% and high power densities of greater than $40W/in^3$.

Finally, chapter 5 presents a new feature-rich transformer-less ac-dc-ac converter topology which is suitable for a high-power-density high-efficiency single-phase data-center online uninterruptible power supply (UPS) with a common neutral between the input and output ac ports [138]. The proposed converter comprises an input power factor correction (PFC) rectification (ac-dc) stage which is followed by an inversion (dc-ac) stage. The rectification stage operates in boost mode during the input positive half line cycle and buck-boost mode during the input negative half line cycle, while the inversion stage operates in buck and buck-boost modes in the output positive and negative half line cycles, respectively. The rectification stage utilizes boundary conduction mode (BCM) control enabling soft-switching and allowing high frequency operation [139], [122]. The inversion stage is operated in continuous conduction mode (CCM), wherein a digital controller regulates the output voltage of the converter across

both resistive and reactive loads. The proposed online UPS utilizes a single (non-split) dc-bus between the rectification and inversion stages, resulting in a 50% reduction in dc-bus capacitance requirement compared to conventional split-bus online UPS topologies. Additionally, two battery interface solutions are also investigated which provide a trade-off between passive volume and additional switch-count. To verify the performance and control of the proposed online UPS, a GaN-based electrolytic-free 1-kVA prototype online UPS is designed, built, and tested. The prototype ac-dc-ac converter achieves a peak efficiency of 95.2% and maintains a high efficiency of above 92.3% across the full output power range. This electrolytic-free prototype ac-dc-ac converter for the online UPS achieves a power density of 26.4W/in$^3$ [140].

## 6.2 Recommendations for Future Work

While this work demonstrates a substantial improvement in performance of single-phase line-interfaced power converters, there are still few unexplored opportunities to further enhance performance. For ac-dc applications, this work addressed the need to co-optimize the design of PFC stage and EMI filter to enhance overall power density and efficiency while the isolated dc-dc stage was designed as a standalone converter. However, the optimization methodology can be further extended to the design of isolated dc-dc converter where the dc-bus voltage ripple can become a design variable. Trade-offs between power density and efficiency can be evaluated by increasing dc-bus voltage ripple (reducing dc-bus capacitance) which would reduce dc-bus capacitor volume but increase power losses in LLC dc-dc stage. Similarly, other design variables can also be explored to evaluate possible tradeoffs in power density and efficiency.

For ac-ac converter applications, a multilevel variant of the proposed two-stage ac-ac converter topology can be explored which can provide reduction in magnetics volume. Thereby, enabling further improvement in power density. Moreover, advanced control techniques can be explored for the new topology both for rectification and inversion stages. The rectification stage operates at variable switching

frequency which add complications to the design process for the EMI filter. A constant frequency but soft-switched control technique would add substantial value for practicing engineers and EMI filter designers. Similarly, soft-switching techniques can also be explored for the inversion stage (currently operating under CCM operation with partial soft-switching only at low loads). Such techniques can help enhance power density of the online UPS by lowering power stage and output filter volume. A comprehensive design methodology can also be explored for the online UPS which considers the design of the input and output EMI filters in the power stage design process by utilizing similar co-optimization strategy as presented in chapter 2. Lastly, paralleling techniques can also be explored for the proposed online UPS. Paralleled online UPS can adhere to N+1 redundancy needs and can also enable cost reduction through economies of scale. Therefore, developing paralleling techniques suitable for the new online UPS topology can further enhance its utility for UPS designers, manufacturers, and consumers.

Lastly, the research proposed in this work can also be explored for three-phase applications. A substantial amount of electrical power is delivered and processed using three-phase line-interfaced power converters. In three-phase ac-dc converters, a similar design strategy as the one presented in chapter 2 can be explored which can enhance power density and efficiency by evaluating several conversion architectures, control strategies, and design parameters, while adhering to pertinent EMI regulations. Moreover, three-phase ac-ac converters can also be evaluated. Owing to the benefits of proposed ac-dc-ac converter topology in single-phase applications, a three-phase variant can also be explored and evaluated for performance comparison with the state-of-the-art. Furthermore, while SiC is increasingly being utilized for use in three-phase applications, GaN transistors are not as prominent in this application space. Therefore, there is an opportunity to evaluate GaN technology and compare its performance in three-phase ac-dc and ac-ac conversion systems.

# BIBLIOGRAPHY


[1] Hannah Ritchie and Max Roser (2020) - "Energy". Our World in Data.

[2] W. Kramer, S. Chakraborty, B. Kroposki, and H. Thomas, Advanced Power Electronic Interfaces for Distributed Energy Systems Part 1: Systems and Topologies. National Renewable Energy Laboratory, March 2008.

[3] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," *IEEE Transactions on Industrial Informatics*, vol. 7, no. 4, pp. 540-556, November 2011.

[4] IEA (2019), World Energy Outlook 2019, IEA, Paris. Available: https://www.iea.org/reports/world-energy-outlook-2019.

[5] J. Spitaels, "The Different Types of AC Power Connectors in North America", Schneider Electric.

[6] P. T. Krein, "Data center challenges and their power electronics," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 1, pp. 39-46, July 2017.

[7] W. Su, H. Eichi, W. Zeng, and M. Chow, "A Survey on the Electrification of Transportation in a Smart Grid Environment," in *IEEE Transactions on Industrial Informatics*, vol. 8, no. 1, pp. 1-10, February 2012.

[8] D. Patil and V. Agarwal, "Compact Onboard Single-Phase EV Battery Charger With Novel Low-Frequency Ripple Compensator and Optimum Filter Design," in *IEEE Transactions on Vehicular Technology*, vol. 65, no. 4, pp. 1948-1956, April 2016.

[9] J. Morroni and P. Shenoy, "Understanding the Trade-offs and Technologies to Increase Power Density", Texas Instruments, 2020.

[10] F. Guo and J. K. Gershenson, "Discovering Relationships Between Modularity and Cost", in *Journal of Intelligent Manufacturing 18*, pp. 143-157, April 2007.

[11] "Program Details: What is 80 PLUS certified?," CLEAResult: 80 Plus. [Online]. Available: https://www.clearesult.com/80plus/program-details.

[12] "What is ENERGY STAR," About ENERGY STAR | ENERGY STAR. [Online]. Available: https://www.energystar.gov/about.

[13] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," *IEEE Transactions on Industrial Informatics*, vol. 7, no. 4, pp. 540-556, November 2011.

[14] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962-981, October 2003.

[15] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, S. D. Round, "PWM Converter Power Density Barriers," *Proceedings of the Power Conversion Conference*, Nagoya, Japan, April 2007.

[16] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Washington, DC, February 2009.

[17] G. Moschopoulos and P. Jain, "Single-phase single-stage power-factor-corrected converter topologies," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 23-35, February 2005.

[18] B. Koushki, A. Safaee, P. Jain, and A. Bakhshai, "Review and comparison of bi-directional AC-DC converters with V2G capability for on-board EV and HEV," *Proceedings of the IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, June 2014.

[19] M. J. Kocher and R. L. Steigerwald, "An AC-to-DC Converter with High Quality Input Waveforms," *IEEE Transactions on Industry Applications*, vol. IA-19, no. 4, pp. 586-599, July 1983.

[20] Yim-Shu Lee and Bo-Tao Lin, "Adding active clamping and soft switching to boost-flyback single-stage isolated power-factor-corrected power supplies," *IEEE Transactions on Power Electronics*, vol. 12, no. 6, pp. 1017-1027, November 1997.

[21] Shiguo Luo, Weihong Qiu, Wenkai Wu, and I. Batarseh, "Flyboost power factor correction cell and a new family of single-stage AC/DC converters," *IEEE Transactions on Power Electronics*, vol. 20, no. 1, pp. 25-34, January 2005.

[22] Jong-Lick Lin, Ming-Zhi Chang, and Sung-Pei Yang, "Synthesis and analysis for a novel single-stage isolated high power factor correction converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 9, pp. 1928-1939, September 2005.

[23] S. Narula, B. Singh, and G. Bhuvaneswari, "Power Factor Corrected Welding Power Supply Using Modified Zeta Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 617-625, June 2016.

[24] P. M. Barbosa, F. Canales, J. M. Burdio, and F. C. Lee, "A three-level converter and its application to power factor correction," *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1319-1327, November 2005.

[25] M. Khatua, A. Kumar, S. Pervaiz, S. Chakraborty, and K. K. Afridi, "A Single-Stage Isolated AC-DC Converter Based on the Impedance Control Network Architecture," *IEEE Transactions on Power Electronics*, Early Access.

[26] S. Chen, Z. R. Li, and C. Chen, "Analysis and Design of Single-Stage AC/DC LLC Resonant Converter," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 3, pp. 1538-1544, March 2012.

[27] F. Jauch and J. Biela, "Combined Phase-Shift and Frequency Modulation of a Dual-Active-Bridge AC–DC Converter With PFC," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8387-8397, December 2016.

[28] N. D. Weise, G. Castelino, K. Basu, and N. Mohan, "A Single-Stage Dual-Active-Bridge-Based Soft Switched AC–DC Converter With Open-Loop Power Factor Correction and Other Advanced Features," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4007-4016, August 2014.

[29] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, T. McNutt, and A. B. Lostetter, "High-frequency AC-DC conversion with a silicon carbide power module to achieve high-efficiency and greatly improved power density," *Proceedings of the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Rogers , AR , July 2013.

[30] B. Whitaker et al., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2606-2617, May 2014.

[31] M. Kasper, D. Bortis, J. W. Kolar, and G. Deboy, "Hyper-efficient (98%) and super-compact (3.3kW/dm$^3$) isolated AC/DC telecom power supply module based on multi-cell converter approach," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh , PA , September 2014.

[32] S. Lim, D. M. Otten, and D. J. Perreault, "New AC–DC Power Factor Correction Architecture Suitable for High-Frequency Operation," *IEEE Transactions on Power Electronics,* vol. 31, no. 4, pp. 2937-2949, April 2016.

[33] M. Khatua, D. Shahzad, S. Pervaiz, and K. K. Afridi, "A High-Power-Density Electrolytic-Free Offline LED Driver Utilizing a Merged Energy Buffer Architecture," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim , CA , March 2019.

[34] Z. Zhang, C. Liu, M. Wang, Y. Si, Y. Liu, and Q. Lei, "High-Efficiency High-Power-Density CLLC Resonant Converter With Low-Stray-Capacitance and Well-Heat-Dissipated Planar Transformer for EV On-Board Charger," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10831-10851, Oct. 2020.

[35] J. Biela, D. Hassler, J. Miniböck, and J. W. Kolar, "Optimal design of a 5 kW/dm$^3$ / 98.3% efficient TCM resonant transition single-phase PFC rectifier," *Proceedings of the IEEE International Power Electronics Conf. (IPEC-ECCE Asia)*, Sapporo , Japan , June 2010.

[36] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," *Proceedings of the 7th International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg , Germany , March 2012.

[37] M. K. H. Cheung, M. H. L. Chow, and C. K. Tse, "Practical Design and Evaluation of a 1 kW PFC Power Supply Based on Reduced Redundant Power Processing Principle," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 2, pp. 665-673, February 2008.

[38] H. Nakao et al., "2.5-kW power supply unit with semi-bridgeless PFC designed for GaN-HEMT," *Proceedings of the Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach , CA, March 2013.

[39] C. Shi, A. Khaligh, and H. Wang, "Interleaved SEPIC Power Factor Preregulator Using Coupled Inductors In Discontinuous Conduction Mode With Wide Output Voltage," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3461-3471, July-August 2016.

[40] W. Konrad, G. Deboy, and A. Muetze, "A Power Supply Achieving Titanium Level Efficiency for a Wide Range of Input Voltages," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 117-127, January 2017.

[41] S. Pervaiz, A. Kumar, and K. K. Afridi, "GaN-Based High-Power-Density Electrolytic-Free Universal Input LED Driver," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3890-3901, July-August 2018.

[42] C. A. Gallo, F. L. Tofoli, E. A. A. Coelho, L. C. de Freitas, V. J. Farias, and J. B. Vieira Jr., "A switched-mode power supply using a boost-flyback converter and an interleaved soft-switching forward topology," *Proceedings of the IEEE Power Electronics Specialists Conference*, Rhodes , Greece , June 2008.

[43] J. Lee and H. Chae, "6.6-kW Onboard Charger Design Using DCM PFC Converter With Harmonic Modulation Technique and Two-Stage DC/DC Converter," *IEEE Transactions on Industrial Electronics,* vol. 61, no. 3, pp. 1243-1252, March 2014.

[44] C. Shi, H. Wang, S. Dusmez, and A. Khaligh, "A SiC-Based High-Efficiency Isolated Onboard PEV Charger With Ultrawide DC-Link Voltage Range," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 501-511, January-February 2017.

[45] Z. Liu, B. Li, F. C. Lee, and Q. Li, "High-Efficiency High-Density Critical Mode Rectifier/Inverter for WBG-Device-Based On-Board Charger," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9114-9123, November 2017.

[46] MIL-STD-461G, Department of Defense Interface Standard: Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment, 2015

[47] Part 15: Radio Frequency Devices, Federal Commununications Commission, Electronic Code of Federal Regulations, Title 47: Telecommunications (47CFR15), 2017.

[48] V. J. Thottuvelil and G. C. Verghese, "Analysis and control design of paralleled DC/DC converters with current sharing," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 635-644, July 1998.

[49] D. J. Perreault, K. Sato, R. L. Selders, and J. G. Kassakian, "Switching-ripple-based current sharing for paralleled power converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 10, pp. 1264-1274, October 1999.

[50] X. Zhang, L. Corradini, and D. Maksimovic, "Digitally controlled distributed multiphase DC-DC converters," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, San Jose, CA, September 2009.

[51] S. Zong, H. Luo, W. Li, X. He, and C. Xia, "Theoretical Evaluation of Stability Improvement Brought by Resonant Current Loop for Paralleled LLC Converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4170-4180, July 2015.

[52] F. Chen, R. Burgos, D. Boroyevich, and W. Zhang, "A nonlinear droop method to improve voltage regulation and load sharing in DC systems," *Proceedings of the IEEE First International Conference on DC Microgrids (ICDCM)*, Atlanta, GA, June 2015.

[53] H. Wang, M. Han, R. Han, J. M. Guerrero, and J. C. Vasquez, "A Decentralized Current-Sharing Controller Endows Fast Transient Response to Parallel DC–DC Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4362-4372, May 2018.

[54] Y. Wang, X. Ren, Z. Zhang, and Q. Chen, "Research on current sharing strategy of parallel LLC resonant converter," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim*, CA, USA, March 2019.

[55] S. S. Shah, S. K. Rastogi, and S. Bhattacharya, "Paralleling of LLC Resonant Converters," *IEEE Transactions on Power Electronics*, November 2020.

[56] H. Wang, M. Han, R. Han, J. M. Guerrero, and J. C. Vasquez, "A Decentralized Current-Sharing Controller Endows Fast Transient Response to Parallel DC–DC Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4362-4372, May 2018.

[57] G. Liu and P. Mattavelli, "Hysteresis Droop Controller with One Sample Delay for DC-DC Converters in DC Microgrids," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, September 2019.

[58] G. Xu, D. Sha, and X. Liao, "Decentralized Inverse-Droop Control for Input-Series–Output-Parallel DC–DC Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4621-4625, September 2015.

[59] M. Davari and Y. A. I. Mohamed, "Robust Droop and DC-Bus Voltage Control for Effective Stabilization and Power Sharing in VSC Multiterminal DC Grids," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4373-4395, May 2018.

[60] B.H. Kwon, B.D. Min and J.H. Kim, "Novel Topologies of AC Choppers," *IEE Proceedings - Electric Power Applications*, vol. 143, no. 4, pp. 323-330, July 1996.

[61] S. Srinivasan and G. Venkataramanan, "Comparative Evaluation of PWM AC-AC Converters," *Proceedings of the Power Electronics Specialists Conference (PESC)*, Atlanta, GA, June 1995.

[62] A.V. Sidorov, "AC Voltage Regulators Review," *International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM)*, Erlagol, Russia, June 2016.

[63] H. Shin, H. Cha, H.G. Kim and D.W. Yoo, "A Novel Single-Phase PWM AC-AC Converters without Commutation Problem," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Denver, CO, September 2013.

[64] B. Glod, L. Parvulescu and D. Floricau, "Multilevel Direct PWM AC-AC Converters," *Proceedings of the International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, Bucharest, Romania, March 2017.

[65] P.K. Bhowmik, S. Yellapragada and M. Manjrekar, "Dynamic Analysis and Controller Design for a Center-Point-Clamped AC-AC Converter," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, March 2015.

[66] J. Ramos-Ruiz, A. Morsy and P. Enjeti, "Medium Voltage AC-AC Adapter using Multilevel Capacitor Clamped Buck Converter," *Proceedings of the International Conference on Power Electronics (CIEP)*, Guanajuato, Mexico, June 2016.

[67] N. Rasmussen, "The Different Types of UPS Systems," Schneider Electric, 2011.

[68] S. Karve, "Three of a Kind," *IEE Review*, vol. 46, no. 2, pp. 27-31, March 2000.

[69] International Electrotechnical Commission, "Uninterruptible Power Systems (UPS) - Part 3: Method of Specifying the Performance and Test Requirements," IEC 62040-3, 2011.

[70] J. M. Guerrero, L. Garcia De Vicuna, and J. Uceda, "Uninterruptible Power Supply Systems Provide Protection," *IEEE Industrial Electronics Magazine*, vol. 1, no. 1, pp. 28-38, Spring 2007.

[71] M. T. Tsai and C. H. Liu, "Design and Implementation of a Cost-Effective Quasi Line-Interactive UPS with Novel Topology," *IEEE Transactions on Power Electronics*, vol. 18, no. 4, pp. 1002-

1011, July 2003.

[72] M. A. P. Azpeitia, A. Fernandez, D. G. Lamar, M. Rodriguez, and M. M. Hernando, “Simplified Voltage-Sag Filler for Line-Interactive Uninterruptible Power Supplies,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 3005-3011, August 2008.

[73] S. S. H. Bukhari and J. Ro, “A Single-Phase Line-Interactive UPS System for Transformer-Coupled Loading Conditions,” in IEEE Access, vol. 8, pp. 23143-23153, January 2020.

[74] Y. Chen and P. Cheng, “An Inrush Current Mitigation Technique for the Line-Interactive Uninterruptible Power Supply Systems,” *IEEE Transactions on Industry Applications*, vol. 46, no. 4, pp. 1498-1508, July 2010.

[75] M. Arias, M. M. Hernando, D. G. Lamar, J. Sebastián, and A. Fernández, “Elimination of the Transfer-Time Effects in Line-Interactive and Passive Standby UPSs by Means of a Small-Size Inverter,” *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1468-1478, March 2012.

[76] M. Tsai, Y. Shen, J. Zhou and P. Cheng, "A Forced Commutation Method of the Solid-State Transfer Switch in the Uninterrupted Power Supply Applications," in IEEE Transactions on Industry Applications, vol. 56, no. 2, pp. 1609-1617, March-April 2020.

[77] “IEEE Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications,” in IEEE Std 446-1995, vol., no., pp.1-320, July 1996.

[78] J. Seymour, “The Seven Types of Power Problems,” Schneider Electric, 2011.

[79] R. E. Cosse, D. G. Dunn, and R. M. Spiewak, “Is My UPS Distribution System Coordinated?,” *IEEE Transactions on Industry Applications*, vol. 42, no. 6, pp. 1565-1573, November 2006.

[80] N. Rasmussen, “Guidelines for Specification of Data Center Power Density,” Schneider Electric, 2011.

[81] E. Rodriguez, N. Vazquez, C. Hernandez, and J. Correa, “A Novel AC UPS With High Power Factor and Fast Dynamic Response,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8,

pp. 2963-2973, August 2008.

[82] H. Pinheiro and P. K. Jain, "Series-Parallel Resonant UPS With Capacitive Output DC Bus Filter for Powering HFC Networks," *IEEE Transactions on Power Electronics*, vol. 17, no. 6, pp. 971-979, November 2002.

[83] N. Vazquez, C. Aguilar, J. Arau, R. O. Caceres, I. Barbi, and J. A. Gallegos, "A Novel Uninterruptible Power Supply System With Active Power Factor Correction," *IEEE Transactions on Power Electronics*, vol. 17, no. 3, pp. 405-412, May 2002.

[84] M. A. De Rooij, J. A. Ferreira, and D. Van Wyk, "A Novel Unity Power Factor Low-EMI Uninterruptible Power Supply," *IEEE Transactions on Industry Applications*, vol. 34, no. 4, pp. 870-877, July 1998.

[85] N. Vazquez, J. Villegas-Saucillo, C. Hernandez, E. Rodriguez, and J. Arau, "Two-Stage Uninterruptible Power Supply With High Power Factor," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2954-2962, August 2008.

[86] K. Hirachi, J. Yoshitsugu, K. Nishimura, A. Chibani, and M. Nakaoka, "Switched-Mode PFC Rectifier With High-Frequency Transformer Link for High-Power Density Single Phase UPS," *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, Saint Louis, MO, June 1997.

[87] R. P. Torrico-Bascope, L. D. Bezerra, G. V. Torrico-Bascope, D. de S. Oliveira, C. G. C. Branco, and L. H. C. Barreto, "High Frequency Isolation On-Line UPS System for Low Power Applications," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Austin, TX, February 2008.

[88] R. P. Torrico-Bascopé, D. S. Oliveira, C. G. C. Branco, and F. L. M. Antunes, "A UPS With 110-V/220-V Input Voltage and High-Frequency Transformer Isolation," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2984-2996, August 2008.

[89] J. Y. Lee, Y. M. Chang, and F. Y. Liu, "A New UPS Topology Employing a PFC Boost Rectifier

Cascaded High-Frequency Tri-Port Converter," *IEEE Transactions on Industrial Electronics*, vol. 46, no. 4, pp. 803-813, August 1999.

[90] L. Schuch, C. Rech, H. L. Hey, and J. R. Pinheiro, "Integrated ZVT Auxiliary Commutation Circuit for Input Stage of Double-Conversion UPSs," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1486-1497, November 2004.

[91] C. G. C. Branco, C. M. T. Cruz, R. P. T. Bascope, and F. L. M. Antunes, "A Nonisolated Single-Phase UPS Topology With 110-V/220-V Input–Output Voltage Ratings," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2974-2983, August 2008.

[92] B. Zhao, Q. Song, W. Liu, and Y. Xiao, "Next-Generation Multi-Functional Modular Intelligent UPS System for Smart Grid," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3602-3618, September 2013.

[93] R. S. Maciel, A. M. Costa, B. V. João, E. A. A. Coelho, G. B. Lima, and L. C. G. Freitas, "Renewable Uninterruptible Power Supply System Deploying a Single-Phase Front-End Converter With Integrated PFC and DC-DC Functions," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, Canada, September 2015.

[94] M. Aamir and S. Mekhilef, "An Online Transformerless Uninterruptible Power Supply (UPS) System With a Smaller Battery Bank for Low-Power Applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 233-247, January 2017.

[95] N. B. de Freitas, C. B. Jacobina, and R. P. de Lacerda, "Single-Phase AC-DC-AC Topology for Grid Voltage Compensation," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, October 2017.

[96] N. B. de Freitas, C. B. Jacobina, B. S. Gehrke, and M. F. Cunha, "Transformer-Based Single-Phase AC–DC–AC Topology for Grid Issues Mitigation," *IEEE Transactions on Industry Applications*, vol. 55, no. 4, pp. 4001-4011, July, 2019.

[97] M. F. Alsolami, K. A. Potty and J. Wang, "Mitigation of Double-Line-Frequency Current Ripple

in Switched Capacitor Based UPS System," in *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4042-4051, April 2021.

[98] E. S. Thomas, J. B. Dagenhart, R. A. Barber, and A. L. Clapp, "Distribution System Grounding Fundamentals," *IEEE Industry Applications Magazine*, vol. 11, no. 5, pp. 67-76, September 2005.

[99] N. Rasmussen, "The Role of Isolation Transformers in Data Center UPS Systems," Schneider Electric, 2010.

[100] Telecommunications Industry Association, "Generic Telecommunications Bonding and Grounding (Earthing) for Customer Premises," TIA 607-C, 2015.

[101] National Fire Protection Association, "Chapter 2: Wiring and Protection," National Electrical Code (NEC), 2017.

[102] C. Wang and C. Su, "A Novel Common-Neutral Single-Stage Single-Phase AC/DC/AC Converter With High Input Power Factor," *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, Jeju, South Korea, June 2006.

[103] Gui-Jia Su and T. Ohno, "A New Topology for Single Phase UPS Systems," *Proceedings of the Power Conversion Conference (PCC)*, Nagaoka, Japan, August 1997.

[104] O. Kwon, J. Kwon, and B. Kwon, "Highly Efficient Single-Phase Three-Level Three-Leg Converter Using SiC mosfets for AC–AC Applications," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 9, pp. 7015-7024, September 2018.

[105] S. B. Bekiarov, A. Nasiri, and A. Emadi, "A New Reduced Parts On-Line Single-Phase UPS System," *Proceedings of the Conference of the IEEE Industrial Electronics Society (IECON)*, Roanoke, VA, November 2003.

[106] M. R. Reinert, C. Rech, M. Mezaroba, and L. Michels, "Transformerless Double-Conversion UPS Using a Regenerative Snubber Circuit," *Proceedings of the Brazilian Power Electronics Conference*, Bonito, Mato Grosso do Sul, Brazil, September 2009.

[107] R. P. R. de Sousa, N. S. de Moraes Lima Marinus, C. B. Jacobina, and N. Rocha, "A Unidirectional

Single-Phase AC–DC–AC Three-Level Three-Leg Converter," *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1708-1716, March 2019.

[108] A. Costa, N. Rocha, C. B. Jacobina, and E. L. L. Fabricio, "Single-Phase AC-DC-AC Three-Level Three-leg Converter with Reduced Switch Count," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2295-2307, March 2020.

[109] A. Costa, C. Jacobina, N. Rocha, E. Silva and A. V. Filho, "A Single-Phase AC-DC-AC Unidirectional Three-leg Converter," in *IEEE Transactions on Industrial Electronics*, April 2020.

[110] I. S. de Freitas, C. B. Jacobina, E. R. C. da Silva, and T. M. Oliveira, "Single-Phase AC–DC–AC Three-Level Three-Leg Converter," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 12, pp. 4075-4084, December 2010.

[111] R. Ghosh, M. Lipare, and D. Klikic, "Single-Battery Power Topologies for Online UPS Systems," United States Patent US9024476B2, July 28, 2011.

[112] B. R. Lin and C. H. Huang, "Single-Phase AC/DC/AC Converter Based on Capacitor Clamped Topology," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 3, pp. 464-472, May 2005.

[113] J. H. Choi, J. M. Kwon, J. H. Jung, and B. H. Kwon, "High-Performance Online UPS Using Three-Leg-Type Converter," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 889-897, June 2005.

[114] C. Yeh and M. D. Manjrekar, "A Reconfigurable Uninterruptible Power Supply System for Multiple Power Quality Applications," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1361-1372, July 2007.

[115] J. Park, J. Kwon, E. Kim, and B. Kwon, "High-Performance Transformerless Online UPS," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2943-2953, August 2008.

[116] C. M. T. Cruz and I. Barbi, "Unit Power Factor Active Clamping Single Phase Three Level Rectifier," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition*

*(APEC),* Anaheim, CA, March 2001.

[117] S. De Simone, C. Adragna, C. Spini and G. Gattavari, "Design-oriented steady-state analysis of LLC resonant converters based on FHA,"*Proceedings of the International Symposium on Power Electronics*, Electrical Drives, Automation and Motion ( SPEEDAM)., Taormina, May 2006.

[118] L. Gu, W. Liang, M. Praglin, S. Chakraborty, and J. Rivas-Davila, "A Wide-Input-Range High-Efficiency Step-Down Power Factor Correction Converter Using a Variable Frequency Multiplier Technique," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9399-9411, November 2018.

[119] W. Inam, K. K. Afridi, and D. J. Perreault, "Variable Frequency Multiplier Technique for High-Efficiency Conversion Over a Wide Operating Range," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 335-343, June 2016.

[120] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 873-882, February 2014.

[121] Z. Huang, Z. Liu, Q. Li, and F. C. Lee, "Microcontroller-Based MHz Totem-Pole PFC With Critical Mode Control," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, September 2016.

[122] D. Shahzad, N. Zaffar, and K. K. Afridi, "Power Factor Enhancement of a Soft-Switched Common-Neutral Single-DC-Bus Power Converter,"*Proceedings of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aalborg, Denmark, November 2020.

[123] S. Ziegler, R. C. Woodward, H. H. Iu and L. J. Borle, "Current Sensing Techniques: A Review," *IEEE Sensors Journal,* vol. 9, no. 4, pp. 354-376, April 2009.

[124] R. P. Singh and A. M. Khambadkone, "Giant Magneto Resistive (GMR) Effect Based Current Sensing Technique for Low Voltage/High Current Voltage Regulator Modules," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 915-925, March 2008.

[125] B. Liu, R. Ren, Z. Zhang, B. Guo, F. Wang, and D. Costinett, "Impacts of high frequency, high di/dt, dv/dt environment on sensing quality of GaN based converters and their mitigation," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 4, pp. 301-312, December 2018.

[126] Michael A.Wu , "A Common Platform for Current Sensor Evaluation in Industrial Automation Applications," M.S. thesis, Electrical Engineering and Computer Science, Massachusetts Institute of Technology, February 2016.

[127] J.C. Crebier and B.D. Nguyen, "Gate Driver Supplies and Dead Time Management Circuits for AC to AC Converters," *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 168-177, January 2010.

[128] L. Ghossein, F. Morel, H. Morel and P. Dworakowski, "State of the Art of Gate-Drive Power Supplies for Medium and High Voltage Applications," *Proceedings of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, Nuremberg, Germany, May 2016.

[129] L. Corradini, Maksimović Dragan, P. Mattavelli, and R. Zane, "Digital control of high-frequency switched-mode power converters," Hoboken: Wiley, 2015.

[130] K. Yao, Y. Wang, J. Guo, and K. Chen, "Critical Conduction Mode Boost PFC Converter With Fixed Switching Frequency Control," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6845-6857, August 2018.

[131] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed. New York, NY, USA: Springer, 2001.

[132] Apc.com. 2021. APC Smart-UPS SRT 1000VA RM 120V - APC USA.

[133] Apc.com. 2021. APC Smart-UPS SRT 72V 2.2kVA Battery Pack - APC USA.

[134] Lithium-ion-ups.com. 2021. N1C.L1000 (1kVA, 120V) – N1C USA.

[135] D. Shahzad, S. Pervaiz and K. K. Afridi, "A High-Power-Density High-Efficiency Single-Phase Universal-Input to 28V Isolated AC-DC Converter Designed to Meet MIL-STD EMI

Specifications," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, June 2021.

[136] D. Shahzad and K. K. Afridi, "Paralleled Two-Stage Single-Phase AC-DC Converter Modules utilizing a Second-Stage Input-Current based Droop Control Strategy," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Vancouver, Canada, October 2021.

[137] D. Shahzad, S. Pervaiz and K. K. Afridi, "Low-Cost High-Efficiency Single-Stage Solid-State Transformer for Lighting Applications," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, September 2018.

[138] D. Shahzad, N. A. Zaffar, and K. K. Afridi, "High-Power-Density GaN-Based Single-Phase Online Uninterruptible Power Supply," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, September 2019.

[139] D. Shahzad, S. Pervaiz, N. Zaffar and K. K. Afridi, "Control of a GaN-Based High-Power-Density Single-Phase Online Uninterruptible Power Supply," *Proceedings of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, ON, Canada, June 2019.

[140] D. Shahzad, S. Pervaiz, N. Zaffar and K. K. Afridi, "GaN-Based High-Power-Density AC-DC-AC Converter for Single-Phase Transformer-Less Online Uninterruptible Power Supply," *IEEE Transactions of Power Electronics*.

# APPENDIX A

# DC-BUS CAPACITANCE REQUIREMENT OF SINGLE-DC-BUS AC-DC-AC CONVERTER

This appendix derives the closed-form expressions for the proposed online UPS' dc-bus capacitor's energy storage requirement and capacitance value. These expressions are derived assuming that the UPS' output voltage has the same frequency and phase as its input voltage, and the losses in the UPS are negligible. The instantaneous input power $p_{\mathrm{IN}}(t)$ of the online UPS is given by:

$$p_{\mathrm{IN}}(t) = 2\mathrm{V}_{\mathrm{IN,rms}}\mathrm{I}_{\mathrm{IN,rms}}\sin^2(\omega_{\mathrm{line}}t) = \mathrm{P}_{\mathrm{OUT}}(1-\cos(2\omega_{\mathrm{line}}t)), \tag{A.1}$$

where $\mathrm{V}_{\mathrm{IN,rms}}$ and $\mathrm{I}_{\mathrm{IN,rms}}$ are the rms values of the sinusoidal input voltage and current, respectively, $\omega_{\mathrm{line}}$ is the line frequency, and $\mathrm{P}_{\mathrm{OUT}}$ is the average output power delivered by the UPS. The instantaneous output power of the online UPS is given by:

$$p_{\mathrm{OUT}}(t) = 2\mathrm{V}_{\mathrm{OUT,rms}}\mathrm{I}_{\mathrm{OUT,rms}}\sin(\omega_{\mathrm{line}}t)\sin(\omega_{\mathrm{line}}t-\theta), \tag{A.2}$$

where $\mathrm{V}_{\mathrm{OUT,rms}}$ and $\mathrm{I}_{\mathrm{OUT,rms}}$ are the rms values of the sinusoidal output voltage and current, respectively, and $\theta$ is the phase difference between the output voltage and output current; note $\mathrm{V}_{\mathrm{OUT,rms}}\mathrm{I}_{\mathrm{OUT,rms}}\cos(\theta) = \mathrm{P}_{\mathrm{OUT}}$, where $\cos(\theta)$ is the output power factor of the UPS. The instantaneous difference between the input and output powers must be buffered by the dc-bus capacitor. Therefore, the energy that must be received and released by the dc-bus capacitor, i.e., the energy storage requirement, is given by:

$$E_{\mathrm{S}} = \int_{t_1}^{t_2}[p_{\mathrm{IN}}(t) - p_{\mathrm{OUT}}(t)]\,\mathrm{dt}, \tag{A.3}$$

where the times $t_1$ and $t_2$ correspond to adjacent zero crossings of the power going into the dc-bus capacitor $p_{\mathrm{C}}(t)\big(= p_{\mathrm{IN}}(t) - p_{\mathrm{OUT}}(t)\big)$, such as:

$$t_1 = 0, \tag{A.4}$$

$$t_2 = \frac{\pi}{2\omega_{\text{line}}}. \tag{A.5}$$

Substituting (A.1), (A.2), (A.4), and (A.5) into (A.4) gives the following as the energy storage requirement for the dc-bus capacitor:

$$E_{\text{S}} = \frac{\text{V}_{\text{OUT,rms}}\text{I}_{\text{OUT,rms}}\sin(\theta)}{\omega_{\text{line}}}, \tag{A.6}$$

which is the same as (1).

The maximum energy that the dc-bus capacitor can receive and release is given by:

$$E_{\text{C}} = \frac{1}{2}\text{C}_{\text{BUS}}\left(\text{V}_{\text{BUS,max}}^2 - \text{V}_{\text{BUS,min}}^2\right), \tag{A.7}$$

where, $\text{C}_{\text{BUS}}$ is the capacitance of the dc-bus capacitor, and $\text{V}_{\text{BUS,max}}$ and $\text{V}_{\text{BUS,min}}$ are the maximum and minimum allowed values of the dc-bus voltage, respectively. This can be expressed in terms of the nominal dc-bus voltage ($\text{V}_{\text{BUS}}$) and the allowed peak-to-peak dc-bus voltage ripple ($\Delta\text{V}_{\text{BUS,pk-pk}}$) as below:

$$E_{\text{C}} = \text{C}_{\text{BUS}}\text{V}_{\text{BUS}}\Delta\text{V}_{\text{BUS,pk-pk}} \tag{A.8}$$

Equating (A.6) and (A.8) gives the required dc-bus capacitance value:

$$\text{C}_{\text{BUS}} = \frac{\text{V}_{\text{OUT,rms}}\text{I}_{\text{OUT,rms}}\sin(\theta)}{\omega_{\text{line}}\text{V}_{\text{BUS}}\Delta\text{V}_{\text{BUS,pk-pk}}}, \tag{A.9}$$

# APPENDIX B

# DC-BUS CAPACITANCE REQUIREMENT FOR SINGLE-DC-BUS AC-DC-AC CONVERTER FOR DIFFERENT INPUT AND OUTPUT AC VOLTAGE FREQUENCIES

This appendix derives the closed-form expressions for the proposed online UPS' dc-bus capacitor's energy storage requirement and capacitance value when the input ac voltage and output ac voltage have different frequencies. These expressions are derived assuming that the losses in the UPS are negligible and a resistive load is connected at the output of the online UPS. The instantaneous input power $p_{\mathrm{IN}}(t)$ of the online UPS is given by:

$$p_{\mathrm{IN}}(t) = 2\mathrm{V}_{\mathrm{IN,rms}}\mathrm{I}_{\mathrm{IN,rms}}\sin^2(\omega_{\mathrm{IN}}t) = \mathrm{P}_{\mathrm{OUT}}(1-\cos(2\omega_{\mathrm{IN}}t)), \tag{B.1}$$

where $\mathrm{V}_{\mathrm{IN,rms}}$ and $\mathrm{I}_{\mathrm{IN,rms}}$ are the rms values of the sinusoidal input voltage and current, respectively, $\omega_{\mathrm{IN}}$ is the input line frequency, and $\mathrm{P}_{\mathrm{OUT}}$ is the average output power delivered by the UPS. Similarly, the instantaneous output power of the online UPS is given by:

$$p_{\mathrm{OUT}}(t) = 2\mathrm{V}_{\mathrm{OUT,rms}}\mathrm{I}_{\mathrm{OUT,rms}}\sin^2(\omega_{\mathrm{OUT}}t) = \mathrm{P}_{\mathrm{OUT}}(1-\cos(2\omega_{\mathrm{OUT}}t)), \tag{B.2}$$

where $\mathrm{V}_{\mathrm{OUT,rms}}$ and $\mathrm{I}_{\mathrm{OUT,rms}}$ are the rms values of the sinusoidal input voltage and current, respectively, and $\omega_{\mathrm{OUT}}$ is the output line frequency. The instantaneous difference between the input and output powers must be buffered by the dc-bus capacitor. Therefore, the energy storage requirement for the capacitor is given by:

$$E_{\mathrm{S}}(t) = \int_{t_1}^{t_2}\left(p_{\mathrm{IN}}(\tau) - p_{\mathrm{OUT}}(\tau)\right)\mathrm{d}\tau = \frac{\mathrm{P}_{\mathrm{OUT}}}{2}\left|\frac{\sin(2\omega_{\mathrm{OUT}}\tau)}{\omega_{\mathrm{OUT}}} - \frac{\sin(2\omega_{\mathrm{IN}}\tau)}{\omega_{\mathrm{IN}}}\right|_{t_1}^{t_2} \tag{B.3}$$

where the times $t_1$ and $t_2$ correspond to adjacent zero crossings of the power going into the dc-bus capacitor $p_{\mathrm{C}}(t)\left(= p_{\mathrm{IN}}(t) - p_{\mathrm{OUT}}(t)\right)$. These values of $t_1$ and $t_2$ are given by:

$$t_1 = \frac{(\mathrm{m}-1)\pi}{\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}}}, \tag{B.4}$$

$$t_2 = \frac{\mathrm{m}\pi}{\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}}}, \tag{B.5}$$

Here, m is an integer between zero and infinity. As can be inferred from (B.4) and (B.5), there are several local minima and maxima of $E_{\mathrm{S}}(t)$ at integer multiples of $t = \frac{\pi}{\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}}}$. For given input and output frequencies ($\omega_{\mathrm{OUT}}$ and $\omega_{\mathrm{IN}}$), the global maxima and minima of $E_{\mathrm{S}}(t)$ can be found by substituting the following value of m ($= \mathrm{m_A}$) in (B.4) and (B.5):

$$\mathrm{m_A} = \left\lceil \frac{(\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}})}{2|\omega_{\mathrm{OUT}}-\omega_{\mathrm{IN}}|} \right\rceil, \tag{B.6}$$

The above expression uses a ceiling function $\lceil x \rceil$ (which returns the least integer greater than or equal to its argument $x$). Substituting the expression of $\mathrm{m_A}$ given by (B.6) in (B.4) and (B.5), and replacing the resultant values of $\mathrm{t_1}$ and $\mathrm{t_2}$ in (B.3) results in the following expression for peak energy stored in the dc-bus capacitor:

$$E_{\mathrm{S,max}} = \frac{\mathrm{P_{OUT}}(\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}})}{\omega_{\mathrm{OUT}}\omega_{\mathrm{IN}}} \times \left| \sin\left(\frac{\pi\omega_{\mathrm{OUT}}}{\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}}}\right) \cos\left(\frac{(2\mathrm{m_A}-1)\pi\omega_{\mathrm{OUT}}}{\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}}}\right) \right|. \tag{B.7}$$

The maximum energy that the dc-bus capacitor can receive and release is given by:

$$E_{\mathrm{S,max}} = \frac{1}{2}\mathrm{C_{BUS}}\left(\mathrm{V_{BUS,max}^2} - \mathrm{V_{BUS,min}^2}\right), \tag{B.8}$$

where, $\mathrm{C_{BUS}}$ is the dc-bus capacitance, and $\mathrm{V_{BUS,max}}$ and $\mathrm{V_{BUS,min}}$ are the maximum and minimum values of the dc-bus voltage, respectively. This can be expressed in terms of the nominal dc-bus voltage ($\mathrm{V_{BUS}}$) and peak-to-peak dc-bus voltage ripple ($\Delta\mathrm{V_{BUS,pk-pk}}$) as below:

$$E_{\mathrm{S,max}} = \mathrm{C_{BUS}V_{BUS}}\Delta\mathrm{V_{BUS,pk-pk}}. \tag{B.9}$$

Equating (B.7) and (B.9) results in the required dc-bus capacitance value:

$$\mathrm{C_{BUS}} = \frac{\mathrm{P_{OUT}}(\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}})}{\mathrm{V_{BUS}}\Delta\mathrm{V_{BUS,pk-pk}}\omega_{\mathrm{OUT}}\omega_{\mathrm{IN}}} \times \left| \sin\left(\frac{\pi\omega_{\mathrm{OUT}}}{\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}}}\right) \cos\left(\frac{(2\mathrm{m_A}-1)\pi\omega_{\mathrm{OUT}}}{\omega_{\mathrm{OUT}}+\omega_{\mathrm{IN}}}\right) \right|, \tag{B.10}$$