# LOCAL OSCILLATOR GENERATION AND MIXER CORE DESIGN FOR MILLIMETER-WAVE N-PATH RECEIVERS

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Robin Cherng-En Ying

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# LOCAL OSCILLATOR GENERATION AND MIXER CORE DESIGN FOR MILLIMETER-WAVE N-PATH RECEIVERS

Robin Cherng-En Ying, Ph. D.

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As the RF spectrum becomes increasingly crowded, demands on receiver flexibility and interference-tolerance are becoming more stringent. At the same time, while higher frequency bands are becoming available, they often exceed the upper frequency limits of state-of-the-art software defined receiver circuits and architectures. Thus, to make effective use of the entire available spectrum, receivers must be capable of mixing at these higher frequencies while remaining both resistant to interferers at other frequencies and instantly tunable across a wide frequency and bandwidth.

In this dissertation we introduce a receiver architecture which is resistant to blockers, tunable across a wide frequency range, and capable of mixing up to and beyond 100 GHz. The development of such a solution comes across three generations of the HBT-based N-path receiver and this dissertation will cover each of these iterations as well as the underlying theory that establishes fundamental limits for its performance metrics. Finally, we will conclude with a summary that provides guidance for the further HBT-based N-path receiver designer.

# BIOGRAPHICAL SKETCH

The author was born in Woodland Hills, CA in 1992. He graduated from Cornell University, Ithaca, NY, USA with a Bachelor of Science degree in both Electrical and Computer Engineering (ECE) and Mechanical and Aerospace Engineering (MAE) in 2014. Since then, he has been working toward his Ph.D. at Cornell University in the department of ECE where he focuses on the design, theoretical analysis, and implementation of a new class of N-path receivers implemented with HBTs. He was also the recipient of the 2019 Outstanding ECE TA Award and has since lectured and instructed Cornell's cumulative design course in Digital VLSI Circuit Design.

To my wife, family, and the Vineyard Church of Ithaca

for their unrelenting love and support

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In addition to faculty I must also acknowledge mentors and collegues who built my foundational skills for conducting research. In particular, Ben Johnson and Changhyuk Lee were extremely patient and supportive as I began exploring research in the summer of 2013. Through their encouragement and guidance, I acquired skills in the lab that have been with me until this day. Dong Yang also provided instruction and mentorship in regard to PCB design which has been indispensable.

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Of course, this work would not have been possible without the love, food, friendship, and fellowship of numerous brothers and sisters in Christ who encouraged me, strengthened me, and served me in my times of weakness and exhaustion. My wife, Josephine, fed me, prayed for me, and supported me through all the ups and downs of the process. Friends such as Ryan Kwak, Frank Lin, Charles Qian, and many others cared for me in ways that made my dedication to this work possible. Special thanks to Kevin Zong for proofreading this dissertation. And of course, my in-laws who constantly cooked nutritious and delicious meals when I was particularly busy and even made special trips just to take care of Jo and myself. None of this would be possible without their support.

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CHAPTER 1

# INTRODUCTION

## 1.1 Background

As the RF spectrum becomes increasingly crowded, demands on receiver flexibility and interference-tolerance are becoming more stringent. At the same time, while higher frequency bands are becoming available, they often exceed the upper frequency limits of state-of-the-art software defined receiver circuits and architectures [1,2]. Thus, to make effective use of the entire available spectrum, receivers must be capable of mixing at these higher frequencies while remaining both resistant to interferers at other frequencies and instantly tunable across a wide frequency and bandwidth.

While SAW filters can precede a receiver LNA to provide a high-Q impedance match and a high tolerance for blockers out-of-band, a bank of SAW filters with series switches must be used to tune across a range of RF frequencies as seen in Fig. 1.1. Thus, one of the more promising RF circuit topologies for such a front-end is the multi-phase passive mixer, or N-path filter. The key features of such N-path receivers are:

1) widely-tunable, instantly-reconfigurable RF input impedance and bandwidth

2) high RF port power handling and high blocker/interference tolerance.

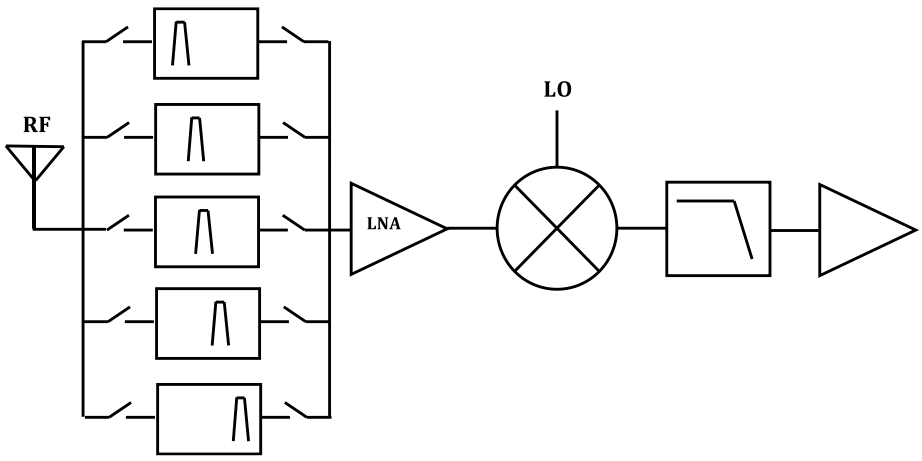


Figure 1.1 Receiver architecture with switched-bank of SAW filters

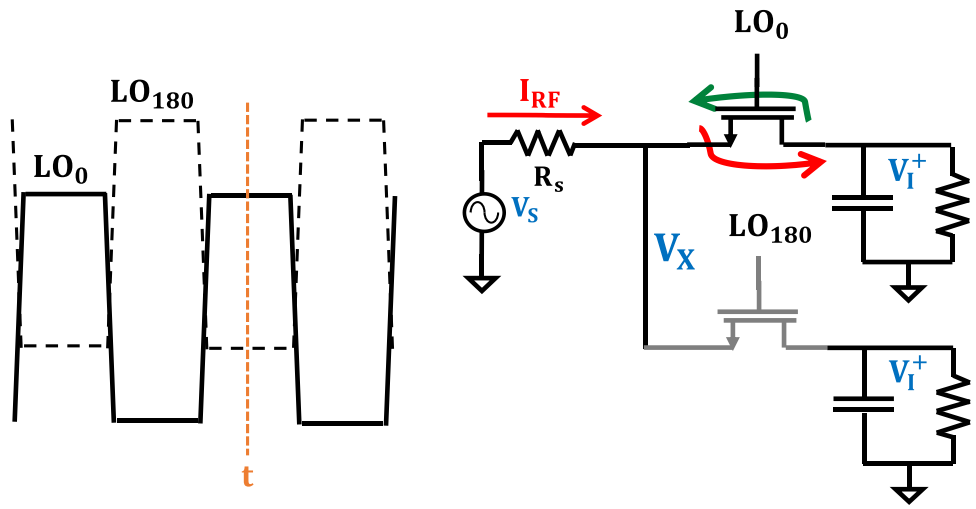


Figure 1.2 Bidirectionality of MOS N-path mixer switch

## 1.2 Bidirectionality and Impedance Transparency

The key property of MOS N-path filters is the bidirectional flow of current across the low impedance switch which is not inherent to BJTs. In Fig. 1.2, for MOS under the hard-switched condition given on the left, the switch corresponding to $LO_0$ presents very low impedance to both the source and drain. While $V_S$ generates a current across $R_S$ which charges up the capacitor on $V_I^+$, the voltage held on the drain is sampled back onto $V_X$ as long as the switch presents a very low impedance. Conversely, when $LO_{180}$ becomes large, the same becomes true for $V_I^-$. Thus, for ideal complementary 50% duty cycle LO pulses, the differential drain current is always proportional to $V_S$ x $\text{sgn}(LO_0 - LO_{180})$ and simultaneously, the voltage $V_X$ is always proportional to the baseband voltage, $V_I$ x $\text{sgn}(LO_0 - LO_{180})$ .

From an impedance perspective $I_{RF}$ generated across $R_S$ induces proportional baseband current which interacts with baseband impedance to generate baseband

voltage. Because of bidirectionality, baseband voltages are simultaneously re-upconverted to the RF port. Since the ratio of $V_X$ to $I_{RF}$ is dependent on baseband impedance, it can be said that an N-path mixer is transparent to impedance as depicted in Fig. 1.3. Provided that $R_{SW} \ll R_S$, impedance transparency means that in-band impedance can be controlled such that $Z_{inRF} \cong R_S$ for impedance matching with low noise figure, while out-of-band, the low impedance of baseband capacitance means that $Z_{inRF} \ll R_S$ attenuates out-of-band signals for improved OOB linearity.

In the case of a BJT differential pair, the collector current is again always proportional to $V_S$*sgn($LO_0 - LO_{180}$) because the emitters see a very low impedance; but the emitter voltage is given by

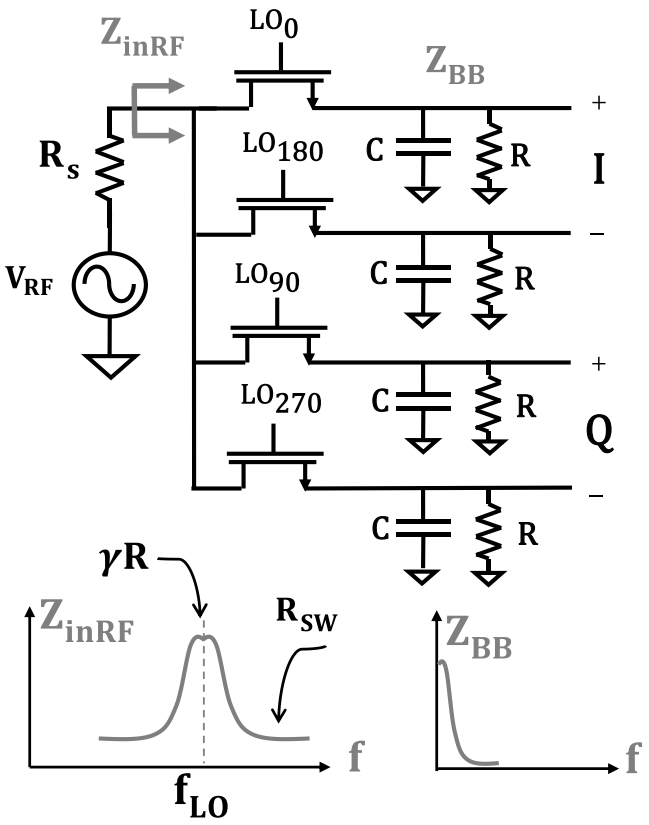


Figure 1.3 MOS N-path mixer with low pass baseband impedance and tunable bandpass on the RF port

$$V_{RF} = \max(V_{LO}) - v_T * \ln\left(\frac{I_{RF}}{I_{Sat}} + 1\right) \quad (1.1)$$

where $I_{RF}$ is the current flowing across $R_S$ from $V_S$ and $I_{Sat}$ is the reverse saturation current of the base-emitter junction. What is important to note here is that the emitter voltage is entirely independent of the collector voltage and tracks the maximum base voltage at any given time. Thus, there is no way for the baseband impedance to control the amplitude and phase of the RF port as is necessary for impedance transparency.

## 1.3 Limitations of Traditional MOS N-Path Filters

Prior work [3] highlighted three properties of LO generation for high-performance N-path filters which together make LO generation at mm-wave frequencies non-trivial:

1) large LO swing

2) non-overlapping quadrature-phase pulses

3) logic switching speed.

While in this section these effects will be described qualitatively, parameters related to these effects will be derived in Chapter 3.

1. Large LO swing: In MOSFET N-path designs, LO signals on the gate should be driven to the maximum allowable $V_{GS}$ to maximize linearity and minimize $R_{sw}$, the on-resistance of the MOS switches which sets both linearity and noise figure.
2. Non-overlapping quadrature-phase pulses: Under the condition of overlapping

pulses shown in Fig.1.1 where the orange box highlights the time window of interest, the FET switched fully by $LO_0$ presents very low impedance while the FET switched by $LO_{90}$ becomes increasingly low impedance. During this overlap, charge leaks between adjacent baseband nodes through the two low impedance switches leading to loss from their corresponding baseband signals.

3. Logic switching speed: In state-of-the-art high-speed flip-flops, MOS-based current mode logic achieves a 100 mV eye-opening at 30 GHz [4]. Since an N/2-stage Johnson counter would be used to generate N-phase 50% duty-cycle square waves, this corresponds to an upper limit on LO generation of about 15 GHz for an N=4 implementation.

## 1.4 Organization of Dissertation

Combining the observations that:

1) blocker tolerance is necessary to handle the crowded spectrum

2) high $f_T$ HBTs are not inherently bidirectional

3) 25 % duty-cycle non-overlapping pulse generation is difficult at mm-wave,

this thesis demonstrates a new class of N-path filters which utilize inherently non-bidirectional HBTs for high power handling at mm-wave RF frequencies while driven by less-demanding and lower-power LO generation architectures. The rest of the dissertation is organized into the following chapters:

**Chapter 2** discusses the implementation of an HBT ECL Johnson-counter divider used to drive FETs both in standard 130 nm CMOS as well as with Raytheon's proprietary 150nm GaAs pHEMT.

**Chapter 3** introduces impedance transparency with inherently non-bidirectional HBTs and characterizes the theoretical boundaries of key performance metrics for the proposed receiver architecture.

**Chapter 4** demonstrates our proof-of-concept implementation of the 1st generation HBT-based N-path mixer with LTI resistor in feedback and Johnson-counter divider for LO generation.

**Chapter 5** builds on our proof-of-concept implementation with the 2nd generation HBT-based N-path mixer utilizing LPTV emitter follower in feedback and a much lower-power, dual-resonant LO buffer. A technique for noise-cancellation to compensate for the non-retimed LO is also introduced.

**Chapter 6** looks forward to the to-be-tested 3rd generation HBT-based N-path mixer with sinusoidal LO signals coupled to inductors in feedback. To improve noise figure, series $\lambda/4$ transmission lines mitigate the loss due to overlap from pure sinusoids.

**Chapter 7** summarizes the challenges of mm-wave layout and modelling and endeavors to guide any designer who looks to implement an HBT N-path receiver.

CHAPTER 2

# QUADRATURE NON-OVERLAPPING PULSE GENERATION FOR THE RF SAMPLER

## 2.1 Architecture Overview

As part of the DARPA ACT program, the RF Sampler provides frequency down conversion from a digitally-selected portion of several octaves of operational bandwidth [5]. This is accomplished with a passive switch network providing frequency conversion, a digitally-reconfigurable feedback amplifier, and high-speed logic and timing circuits to control the passive switch network as shown in Figure 2.1. While there is a challenge posed by fabricating four well-matched GaAs switches for the mixer core, the bulk of the design challenges come from the local oscillator logic and timing circuits.

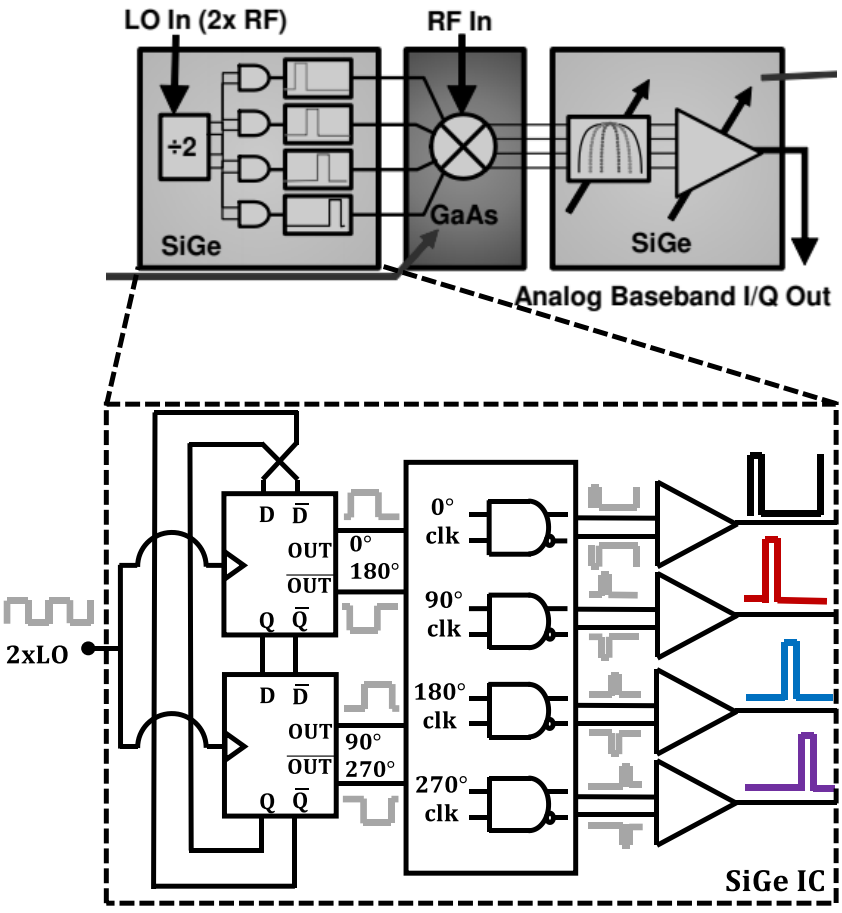


Figure 2.1 Block diagram from the RF sampler with block diagram from logic/timing control circuits

In particular, Raytheon pHEMTs require greater than 2V of swing, driving a 400 pH+9Ω+ 200fF load. To generate quadrature non-overlapping 25% duty-cycle pulses which control these GaAs switches, LO input must be at twice the desired switching frequency (2 x $f_{LO}$) and then:

1) divided down to generate 50% duty-cycle quadrature square waves at $f_{LO}$

2) retimed to generate 25 % duty-cycle pulses

3) buffered to drive the GaAs switch load.

Each of these aforementioned functions is performed by a dedicated circuit block and depicted in Figure 2.1. The remainder of this chapter describes the circuit topology utilized in each block.

## 2.2 LO Buffer

In order to drive the GaAs switch with ~ 2.5V swing, a two-stage push-pull buffer is employed. The first stage maintains sufficient voltage swing without excessive loading on the preceding AND gate while the 2nd stage boosts current drive to mixer gates. Both

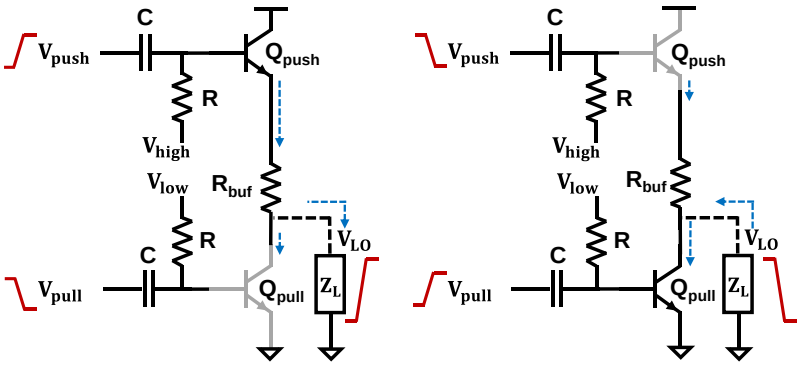


Figure 2.2 Push-pull buffer

stages are comprised of push-pull amplifiers, as demonstrated in Figure 2.2. Because PNPs are slow, traditional inverter-style buffers or complimentary push-pull amplifiers cannot be employed. Instead, if the PNP is replaced by an NPN which is driven by a complimentary signal on the base, we now have a differential-to-single-ended push-pull amplifier providing high-speed buffering and pulse generation. When $V_{push}$ is high, $V_{pull}$ is low, causing $Q_{push}$ to turn on and $Q_{pull}$ to turn off. $Q_{push}$ functions like an emitter follower loaded by a large output impedance from $Q_{pull}$ in parallel with the mixer load, $Z_L$, which ultimately drives current from $Q_{push}$ into $Z_L$ causing $V_{LO}$ to rise. Conversely, when $V_{push}$ is low then $V_{pull}$ is high, causing $Q_{push}$ to turn off and $Q_{pull}$ to turn on. $Q_{push}$ provides no current, but $Q_{pull}$ wants current and thus pulls current from the load $Z_L$ causing $V_{LO}$ to drop. $V_{high}$ and $V_{low}$ set the DC biasing for $Q_{push}$ and $Q_{pull}$, respectively, providing a tuning knob for power consumption and current drive to the mixer load.

Since $Q_{push}$ behaves as an emitter follower with maximum gain of ~1, $Q_{pull}$ is a common emitter amplifier loaded by $1/g_{m,push}$, yielding a gain of approximately $-1$. Since $V_{push}$ and $V_{pull}$ are complimentary, the total gain of the buffer stage is approximately 2. $R_{buf}$ is selected to provide a stable output impedance regardless of whether the buffer is operating in the pushing or pulling regime. With the output of the AND gate being complimentary 625 mV swing pulses, the 1st stage is sized and biased to provide 1.25V swing to the load presented by the 2nd stage buffer while the 2nd stage buffer is sized to provide current drive to generate 2.5V swing on the gate of the GaAs switch up to 20 GHz. As expected, with $V_{CC}$ ranging from 3.3V to 4V and current drive

of up to 80 mA for 2.5V pulses at 20 GHz, the buffer consumes significant power and demands significant layout area. Layout considerations will be discussed in Chapter 7.

## 2.3 Retiming ECL-AND Gate

To generate the needed complimentary 25% duty cycle pulses with approximately 625 mV swing, an emitter-coupled-logic (ECL) AND gate is used. ECL is a BJT-based logic family which is generally considered the fastest logic available, but its high-speed relies on BJTs never entering saturation. Turning off a saturated BJT involves removing and/or recombining carriers generated in the base region such that during a high to low transition, the output won't change until the base charge is first removed. For the ECL AND gate in Figure 2.3, this means providing a supply voltage high enough to sustain the desired voltage swing and biases on all base signals that ensure no device sees a collector-emitter voltage dropping near 200 mV. Under current steering, the collector current for a differential pair with $I_{bias}$ on the shared emitter node and $\Delta V_b$ as the

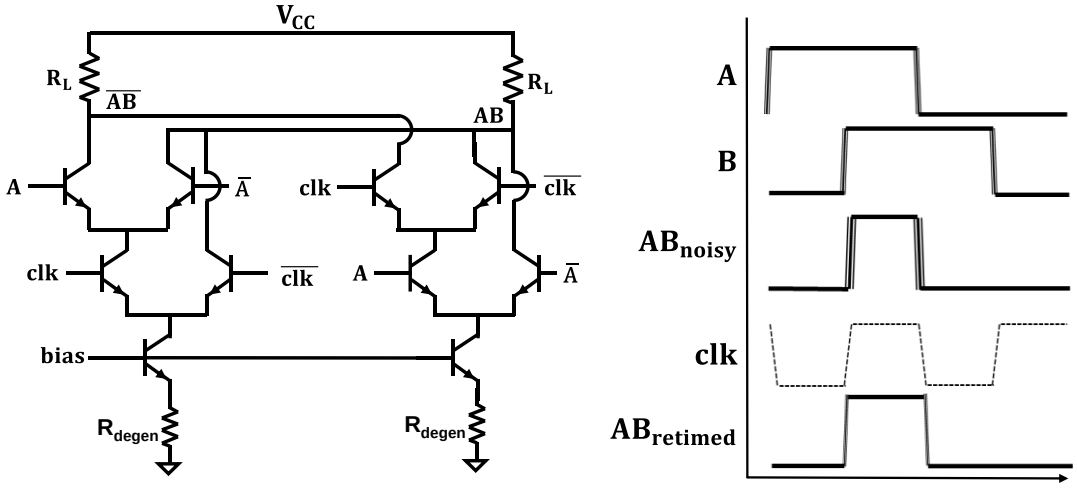


Figure 2.3 Retiming AND gate

difference in base voltages can be predicted by

$$I_C = \frac{I_{bias}}{1 + e^{\Delta V_b / v_T}} \tag{2.1}$$

For as little as 256 mV voltage difference between bases, 22,000 times more current is pulled into one branch than the other such that ECL is inverting and fully-differential, with logic level "0" corresponding to $V_{CC} - I_{bias}R$ and logic level "1" corresponding to $V_{CC}$.

As can be seen in Fig. 2.3, noise captured in the edges of the quadrature-shifted 50% duty-cycle square waves would show up if two quadrature shifted signals were combined with an AND gate. However, if A were instead AND'd with the clean clock signal, the resulting pulse would no longer capture the noise from A. Given this, the quadrature shifted square waves would each see a single AND gate, but the clock signal would see 4 times the load. Thus, while one half of the utilized circuit would be sufficient to perform the desired AND function, the double-balanced implementation ensures that AB and $\overline{AB}$ are truly complimentary.

## 2.4 ECL Divider

The generation of 25% duty-cycle quadrature LO pulses begins with a frequency divide-by-2 consisting of a pair of cross-coupled latches in a Johnson-counter configuration clocked by differential LO inputs. Here we again employ ECL to overcome the frequency limitation of traditional CMOS latches. Since loading of the divider with

capacitance would limit its maximum frequency of operation, we also use a common-base buffer to bring out the quadrature phase square waves which drive the retiming AND gates. HBTs are sized to achieve high $f_T$ at the desired current bias and 4-bit tunable currents enable lower-power operation for lower frequencies of operation.

## 2.5 Measurements in 130 nm CMOS and Raytheon GaAs

Measurements of the RF sampler were taken at Raytheon by Raytheon. Two main versions of the RF sampler were created: one that uses GaAs sampling switches to achieve higher linearity and a second that uses standard CMOS switches for lower cost and reduced linearity. The GaAs/SiGe RF sampler features three chips that are wirebonded chip-to-chip with potentiometers on a low-cost evaluation board for

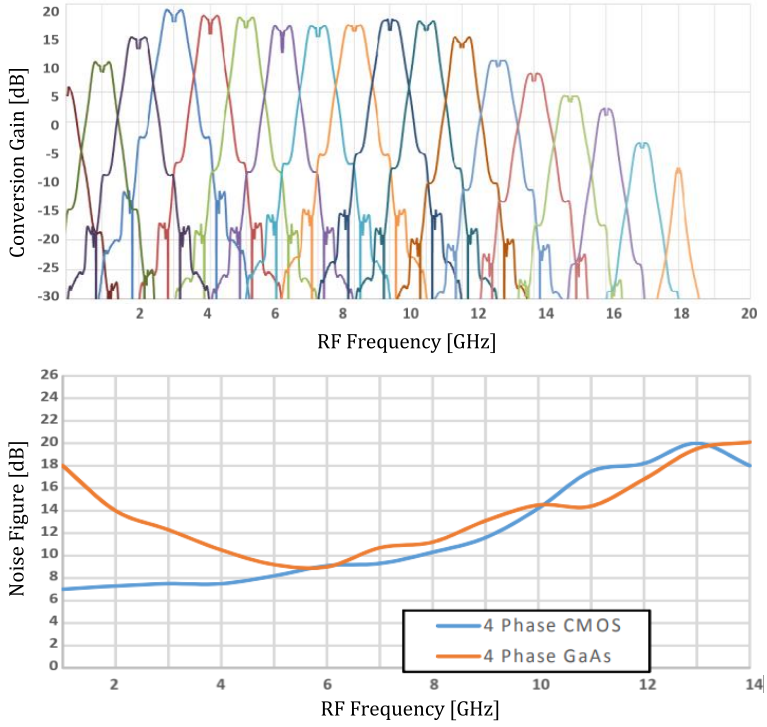


Figure 2.4 The GaAs RF sampler demonstrates multi-octave frequency coverage [5]

producing all necessary bias voltages and currents. In order to ensure the proper negative potential for switching of the GaAs FET, DC blocking capacitors also cause a roll-off in conversion gain (and NF) below 4 GHz as shown in Fig. 2.4. Aside from the loss incurred by the roll-off, NF between the GaAs/SiGe and the BiCMOS remain about equal. However, because of the low $R_{on}$, high $g_m$, and high current handling of the GaAs switch, 1 dB compression due to an out-of-band blocker occurs at much higher input RF power. Measurements show that while B1dB for the 130 nm MOS occurred at around 7 dB, B1dB for Raytheon's 150nm GaAs pHEMT process occurred at 19 dB.

Including the baseband amplifiers, the GaAs/SiGe RF sampler consumed 1.8W while the SiGe-only RF sampler still consumed 1.7W. A large majority of this power consumption comes from the ECL divider, retiming-AND gate, and the 2-stage buffer for driving 25% duty-cycle non-overlapping quadrature pulses to the mixer load up to 20 GHz. Such power consumption ,though considered "low" for III-V technologies, is an order of magnitude larger than would be desired for driving traditional MOS N-path mixers. It is with this in mind that we examine alternate methods for LO generation and alternate N-path topologies which can handle less design-intensive and power-hungry LO generation in the remainder of this dissertation.

CHAPTER 3

# HBT N-PATH IMPEDANCE TRANSPARENCY AND PERFORMANCE METRICS

## 3.1 Motivation

Recent developments in 5G new radio (NR) have expanded the frequencies of interest from sub-6 GHz into the mm-wave range [1,2]. While hardware to make use of this new available spectrum is beginning to be developed [5-9], in the sub-6 GHz range software-defined radios (SDRs) have made dynamic spectrum access to any band possible, tuned to a channel of any bandwidth [10-12]. Mobile devices in close proximity, though now able to hop into unused bands with SDRs, result in potentially strong mutual inference. Thus, for SDRs to make effective use of dynamic spectrum access, tunable filters are needed for blocker suppression.

While state-of-the-art tunable filters are capable of simultaneous center frequency and bandwidth tuning, the former is limited to an octave and the latter is not trivial to achieve [13-16]. To meet the demand for a widely tunable RF band-pass filter which tracks the capabilities of SDRs, N-path filters, which allow for an instantly-reconfigurable RF center frequency – set by the LO – and tunable bandwidth – set by the baseband impedance – have gained popularity in both academia and industry [3,5-6,8-10,17-18].

The key property of these N-path filters which allows for this flexibility is impedance transparency, characterized by the simultaneous down-conversion of the RF current to baseband and re-upconversion of the baseband voltage to the RF port. This two-way frequency translation, or bidirectionality, characteristic to MOS transistors in triode is not inherent to HBTs which often have higher $f_T$ [6,19-20]. However, in our proof-of-concept work, we achieved impedance transparency with HBTs and

demonstrated a new topology of N-path mixer with moderate NF and high linearity at mm-wave frequencies, but with comparable power consumption to that reported in Chapter 2. Additionally, while novel MOS-type devices with high $f_T$ would also enable translation of N-path properties and performance to millimeter wave, in this chapter we will examine the fundamental limits of HBT N-path mixers in comparison to their MOS counterparts to show that HBT N-path mixers exhibit a better full-system power versus performance trade-off.

This chapter is organized as follows: Section 3.2 highlights the differences between MOS and BJT transistors which necessitates HBT-based N-path filters [6]. Section 3.3 builds upon these key properties of BJTs to derive the LTI model for the HBT-based N-path mixer using the process parameters and design variables presented in [3] in order to provide a meaningful comparison between traditional MOS implementations of N-path mixers and the proposed HBT-based topology. Section 3.4 continues in the language of [3] using this LTI model to show how these process parameters and design variables, once organized into dimensionless variables, impact key receiver performance metrics and compare with MOS implementations. Finally, section 3.5 synthesizes our analysis from sections 3.3 and 3.4 to provide a methodology for HBT N-path receiver design and optimization.

## 3.2 MOS vs. BJT Behavior

While state-of-the-art MOS N-path receivers have been demonstrated in the mm-wave frequency range, they often make use of resonant EM structures for sinusoidal LO drive

to novel, short-channel FETs [21-23]. Such designs can consume less power than lower frequency designs, which use high bandwidth digital circuitry as seen in Chapter 2 to generate non-overlapping LO pulses; however, the overlap from the sinusoidal LO drive degrades both linearity and noise. In this section we will examine the demands of high-performance MOS N-path filters which lead to this performance degradation, demonstrate that current-steering HBTs can overcome these limitations but cannot inherently provide impedance transparency, and then conclude with a summary of how we achieve impedance transparency with inherently non-bidirectional HBTs to attain high-performance mm-wave N-path filters.

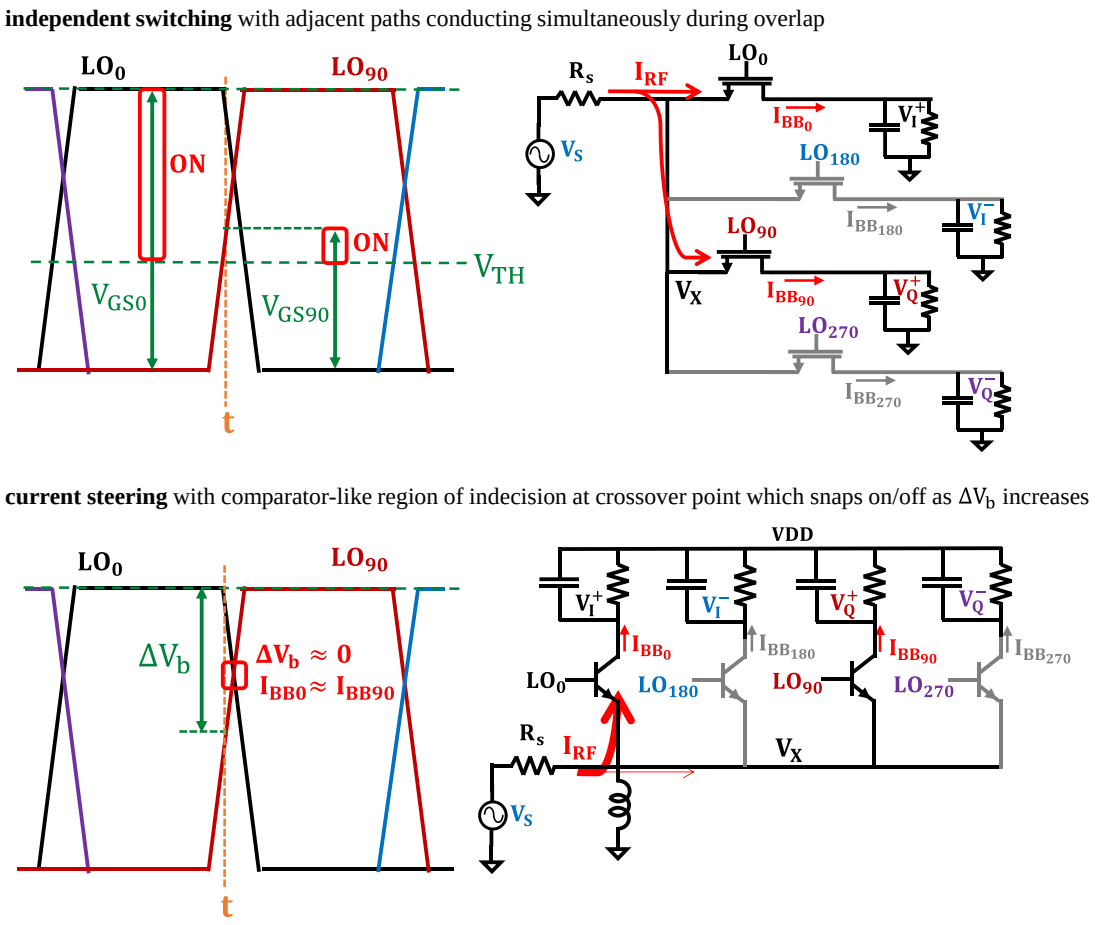


Fig. 3.1 Summary of the key differences between MOS and BJTs

### *3.2.1 HBT Current Steering*

If we simply replace the MOSFETs in Fig. 3.1 with BJTs as well as provide a pull-up supply and an RF choke for biasing, the bottom of Fig. 3.1 illustrates key differences in the behavior of this new topology. To understand this nuanced behavior, consider a differential pair of BJTs with a constant current source shared by their emitters. Here, the ratio of currents between the two collectors is given by

$$\frac{I_{C1}}{I_{C2}} = e^{\frac{\Delta V_b}{v_T}} \tag{3.1}$$

where $\Delta V_b$ is the difference between the base voltages and $v_T$ is the thermal voltage. For as little as a 256 mV ($=10v_T$) difference between the two bases, 22,000 times more current will be pulled to one branch relative to the other effectively turning on one switch and turning off the other. Under the condition of overlap where again the dashed orange line highlights the time of interest, the ratio of currents between the phase adjacent branches follows (3.1). Thus, under current steering, $V_{be}$ of a given transistor is of less concern than $\Delta V_b$ between adjacent bases. Because the switch on-resistance for a BJT is approximately $v_T/I_{Cn}$, (3.1) also governs the impedance a given switch presents to $I_{RF}$ on the shared emitter node. Thus, the switching mechanism for CMOS switches can be viewed as independent switching contingent only on $V_{GS}$, the voltage on a gate relative to a common source node, allowing for adjacent switches to conduct simultaneously, whereas the switching mechanism for BJTs can be likened to that of a comparator where there is a region of indecision during overlap which quickly snaps high or low as $\Delta V_b$, the difference between base voltages, increases.

### 3.2.2 *Impedance Transparency with HBTs*

Given the high-frequency capabilities of BJTs, they would be preferable to FETs for use in mm-wave N-path mixers; unfortunately, given the non-bidirectionality described in Chapter 1, they are not a viable option as is. However, if a signal path were formed between the collector and the base such that the baseband voltage could be re-upconverted to the RF port by the LO, then impedance transparency could be achieved using non-bidirectional devices.

Fig. 3.2 shows the proposed topology and the key waveforms that demonstrate

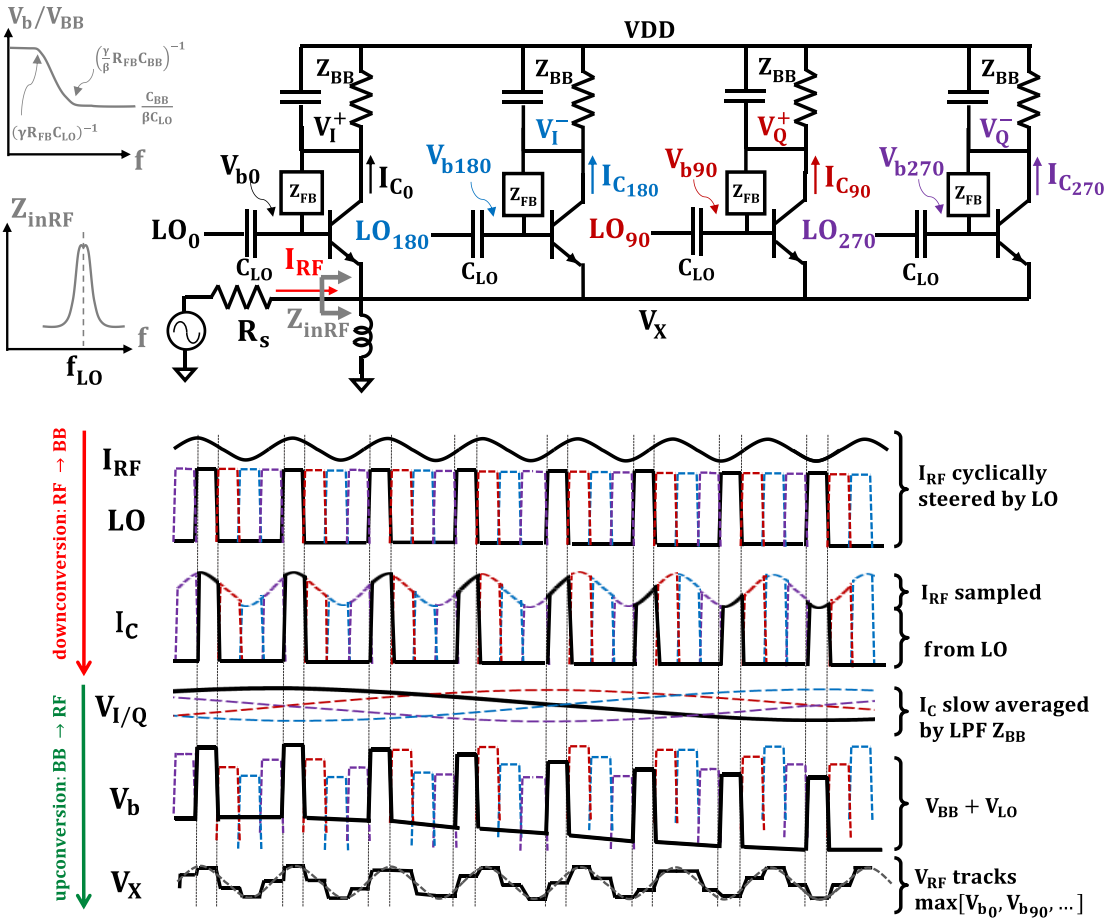


Fig. 3.2 Voltages and currents of proposed topology to demonstrate impedance transparency

how the baseband impedance can be used to set the amplitude and phase of the ratio of voltage and currents on the RF port. When $I_{RF}$ is generated across the antenna port, it is cyclically steered by quadrature-phase, non-overlapping pulses into four identical low-pass baseband loads $Z_{BB}$ which slow-average the fast-varying baseband current to complete the process of down-conversion. $Z_{FB}$ then provides a feedback path from collector to base for baseband signals. If the high-pass filter corner formed by the feedback impedance $Z_{FB}$ and the AC coupling capacitor $C_{LO}$ is sufficiently far from the low-pass corner of the baseband filter $Z_{BB}$ ,then the voltage on the bases of the BJTs will be the superposition of LO pulses sitting on top of the bias-like slow-varying quadrature baseband voltages. Since the peaks of the baseband coupled pulses carry quadrature amplitude information from the baseband, the combined peaks of these pulses are the cyclically sampled form of $I_{RF} \times Z_{BB}$. Finally, because $V_X$, the voltage of the common emitter port, tracks the maximum base voltage at any given time (as described in section IIC), the amplitude and phase of the RF voltage on the RF port can now be set by the easily tunable baseband impedance.

## 3.3 LTI Model of HBT-based N-Path Mixer

For MOS N-path mixers, an elegant LTI model has been developed which captures the dependence of impedance tuning, noise, linearity, and power on various process and design parameters yielding an exhaustive design guide for any given process node [3]. In this section we adopt similar terminology to present a point-by-point dimensionless comparison between MOS and HBT-based N-path mixer limits and performance.

### *3.3.1 HBT-based Equivalent ρ*

If we define $R_{SW}$ as the resistance seen by the RF port when the baseband is shorted to ground, as shown in Fig. 3.3, then we define ρ to be $R_{SW}/R_S$ . Under the comparator-like behavior described in section IIB, the LPTV model on the left of Fig. 3.3 can be simplified to a single transistor with $\gamma$-scaled impedances where $\gamma$ captures the effect of sampling. For N=4, $\gamma \sim 0.2$. When looking out of band, the model consists of a single transistor with $\gamma Z_{AC}$ and $\gamma Z_{FB}$ in shunt from base to ground and the collector tied to ground. Since the equivalent impedance seen by the emitter for an impedance on the base is simply scaled by $1/(\beta + 1)$, the equivalent $R_{SW}$ for the proposed HBT-based N-path filter is

$$R_{SW} = \frac{1}{g_m} + \frac{\gamma Z_{FB} || \gamma Z_{AC}}{\beta + 1} \tag{3.2}$$

where $Z_{AC}$ is the eqvivalent impedance of the series combination of $R_{buf}$ and $C_{LO}$. In band, one of the benefits of impedance transparency is the ability to provide a perfect match to the antenna impedance, or other well-controlled RF impedance. From Fig. 3.3,

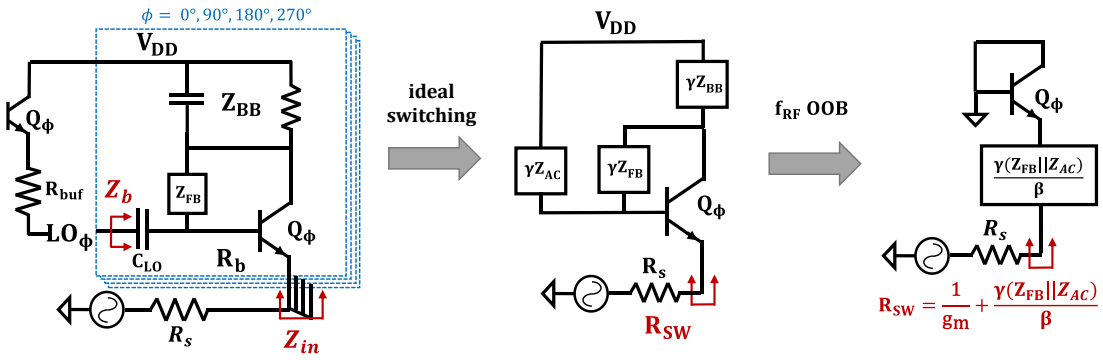


Fig. 3.3 Under ideal switching, the N-phase circuit can be modelled with gamma-scaled impedances and a single mixer-core transistor.

this is equivalent to saying that $R_S = Z_{in}$ when the signal is within the passband on the RF port, $f_{RF} = f_{LO} \pm f_{BB}$. Again, under the assumption of comparator-like behavior of perfect current steering, the small signal equivalent can be used to compute $Z_{in}$.

$$Z_{in} = \frac{1}{g_m} + \frac{\gamma[(\beta+1)Z_{BB}(\omega_{RF} - \omega_{LO}) + Z_{FB}]||\gamma Z_{AC}}{\beta + 1} \tag{3.3}$$

In band, the real part of the second term can be tuned to match the antenna. Out of band, $Z_{BB}(\omega_{RF} - \omega_{LO}) = 0$ and (3.3) becomes equivalent to (3.2). Unlike the CMOS N-path filter where $R_{SW}$ is minimized by larger LO swing, because of the comparator-like behavior of HBT N-path filters, minimal swing is needed to steer the entirety of user-determined current to generate the low $R_{SW}$ which is proportional to $1/I_C$.

### *3.3.2 HBT-based Equivalent $Z_{sh}$*

As was described in [3], mixer input capacitance not only shunts high frequency in-band signals (inductive resonance is often employed to address this) but also shunts re-upconverted power of harmonic images of the original RF signal which are much more difficult to compensate. This effect reduces the impedance seen by those harmonics and $Z_{sh}$ captures the infinite sum of these harmonic losses in a lumped-element LTI impedance.

If we define the mixer cutoff frequency $\omega_m$ to be the frequency at which the mixer shunts as much current through its input capacitance as it downconverts, $Z_{sh}$ can be described as a function of $\omega_{LO}/\omega_m$ and

$$\omega_m = (R_{in}C_{in})^{-1} \tag{3.4}$$

where $R_{in}$ is the real impedance seen looking into the mixer at the RF port and $C_{in}$ is the parasitic capacitance of the RF port due to the mixer and loads. To provide an accurate comparison, we will likewise focus only on the parasitics of the mixers. Under the conditions of proper current steering, we can assume a strong forward-bias on the base-emitter junction of a single p-n junction. Therefore, the non-linear input capacitance is $C_\pi || C_{off}$ : the diffusion and base charging capacitance of a single forward-biased base-emitter junction in parallel with N-1 depletion capacitances. The input capacitance then can be defined in terms of design and process parameters according to

$$C_{in} \cong \frac{I_C}{V_T \omega_T} + (N-1) * C_{j0} \tag{3.5}$$

where $I_C$ is the user-selected collector current, $v_T$ is the thermal voltage, and $C_{j0}$ the depletion capacitance under 0V reverse bias. Since $C_{off}$ drops slightly for larger reverse bias conditions and can increase if LO swing is insufficient to cause reverse-bias across the base-emitter junction, $\omega_m$ increases with LO swing. For a SiGe HBT with its bias (13 mA/$\mu m^2$) and sizing ($W_E$x $L_E$ = 0.17 x 3.6 $\mu m^2$) optimized for $f_{T,max}$= 220 GHz, the depletion capacitance of the base-emitter junction was measured to be 8.9 fF [24]. Using (3.5), $C_{in}$ is computed to be 248 fF with 89.1% of $C_{in}$ coming from the diffusion capacitance of the forward-biased path. Assuming that the impedance looking up the forward-biased base-emitter junction, $R_{in}$ , is $1/g_m$, $\omega_{mHBT}$ for N=4 would yield approximately $0.9\omega_T$. In comparison, for a shallow-trench-isolation MOS process,

$\omega_{m,MOS} \cong \omega_T/(N+1)$ [17].

Harmonic re-upconversion and dissipation in the HBT N-path filter follows from the same sampling mechanism described in [3], so the same harmonic loss shunt resistance approximation can be used

$$Z_{sh}\left(\frac{\omega_{LO}}{\omega_m}, \rho, N, R_S\right) \cong \rho \frac{sinc^2\left(\frac{\pi}{N}\right)}{1 - sinc^2\left(\frac{\pi}{N}\right)}\left(1 + \frac{1}{N\frac{\omega_{LO}}{\omega_m} + \rho}\right) R_S \tag{3.6}$$

What is important to note is that regardless of topology, for any 4-phase N-path filter and antenna impedance operating at the same $R_{SW}$ & $\omega_{LO}$, $Z_{sh}$ is only dependent on $\omega_m$, with a larger $\omega_m$ presenting a larger shunt resistance. This suggests that for a 4-phase HBT-based N-path filter, harmonic re-reradiation effects of the high-frequency LTI model can be pushed out by $4.5 \times (f_{T,HBT}/f_{T,MOS})$ compared to the traditional MOS implementation.

### *3.3.3 HBT-based Equivalent $R_{OL}$*

Lastly, to complete the LTI model we must see how the system performance is affected by leakage between phase-adjacent baseband paths during LO overlap. Since the baseband is slow-varying compared to the LO, baseband voltages can be considered constant during the window of interest in Fig. 3.4. Additionally, with the mechanism for switching for MOS N-path filters being independent switching, the leakage current can be computed by Ohm's law with a time-dependent resistance. Taking into consideration that the lowest power LO drive with a peak swing of $V_{LO}$ is 50% duty-

cycle triangle waves with rise and fall time equal to $V_{LO}/\tau$ as seen in Fig. 3.4, the leakage current during the nth transition is

$$I_{OLn,MOS}(t) = \frac{1}{2R_{SW}}\left(\frac{t}{\tau}\right)\left(1-\frac{t}{\tau}\right)\left(V_{BB_n} - V_{BB_{n-1}}\right) \tag{3.7}$$

In the case of the BJT-based N-path filter with current steering, (3.7) is a severe over-estimation. Since $R_{on}(t)$ for MOSFETs in triode is linear with respect to $LO_n(t)$ while $R_{on}(t)$ for BJTs is proportional to $\exp(\Delta V_b(t))$, the effective duration of leakage is significantly less than $\tau$. For a BJT-based N-path filter, the resistance presented by the "on" branch is given as

$$R_{on}(t) \cong \frac{v_T}{I_C}\left(1 + e^{\frac{-\Delta V_b(t)}{v_T}}\right) \tag{3.8}$$

where $I_C$ is the total current of all N paths and $\Delta V_b$ is the difference between the nth and

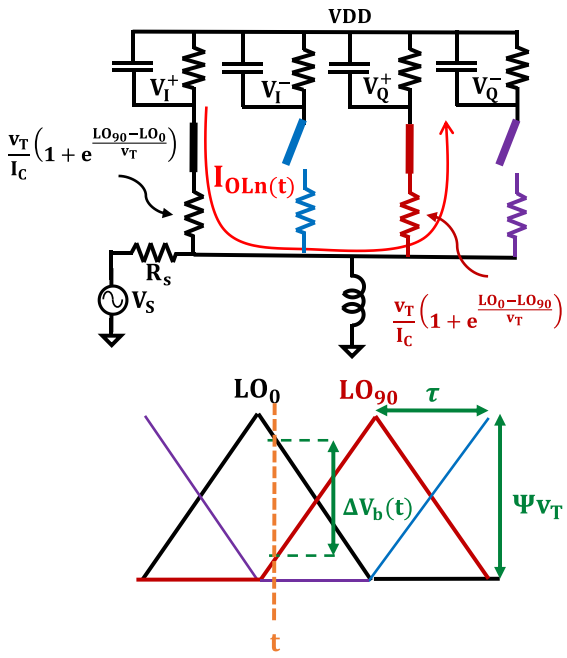


Fig. 3.4 Schematic of mixer switches driven by triangular LO pulses with rise and fall time of $V_{LO}/\tau$.

(n-1)th base voltages. If we define $\Psi = V_{LO}/v_T$ , then the total overlap current between adjacent baseband voltages is

$$I_{OLn}(t) = \frac{V_{BB_n} - V_{BB_{n-1}}}{\frac{1}{g_m}\left(2 + e^{\Psi\left(1-\frac{2t}{\tau}\right)} + e^{\Psi\left(\frac{2t}{\tau}-1\right)}\right) + \frac{2\gamma Z_{FB}}{\beta}} \tag{3.9}$$

The total charge leaking from the nth baseband path during an LO cycle can then be computed by integrating (3.9) from 0 to $\tau$ and combining the nth and the (n+1)th transitions. By noting that when $2\gamma Z_{FB}/\beta$ is small it can be neglected from (10) and when it is large, $I_{OLn}(t)$ decreases

$$Q_n(t) \leq \frac{\tau g_m}{\Psi}\left(2V_{BB_n} - V_{BB_{n-1}} - V_{BB_{n+1}}\right) \tag{3.10}$$

The effect of this leakage current can be approximated as a shunt resistance in our LTI model by Ohm's law for the slow-varying baseband voltage over the average leakage current

$$R_{OL,BJT} = \frac{\gamma T_{LO} V_{BB_n}}{Q_n} \geq \frac{\Psi}{2\pi}\frac{\rho N R_S}{\omega_{LO}\tau} = \frac{\Psi}{6} R_{OL,MOS} \tag{3.11}$$

Under the piece-wise linear model for the triangular 50% duty cycle pulses with slope $V_{LO}/\tau$ and N=4, $R_{OL,MOS} \cong 2.4\ R_{SW}$. For the same $R_{SW}$ and a small value of $V_{LO}$= 256 mV, where 22,000 times more current is steered into one branch relative than the other, $R_{OL,BJT}$ is already 67% larger than $R_{OL,MOS}$. Note also that because $\rho_{MOS}$ is a function of $V_{LO}$, a large $V_{LO}$ would decrease both $\rho$ and $R_{OL}$, but because $\rho_{BJT}$ is a function of $I_C$ and independent of $V_{LO}$, a large $R_{OL,BJT}$ can be achieved independently of small $\rho_{BJT}$ by increasing $V_{LO}$.

## 3.4 Implications for Fundamental Limits of Performance Metrics

Combining all of the effects described in section 3.3, the LTI model in Fig. 3.5 can be used to show how various process and design parameters impact performance metrics.

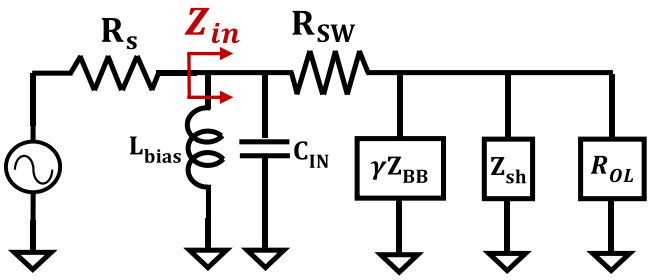


Fig. 3.5 The complete LTI model for the HBT-based n-path mixer.

### *3.4.1 Implications for Conversion Gain*

Although this is an active mixer topology with a constant current consumption, the need for an in-band match reduces its effectiveness as an amplifier. Fig. 3.6 depicts the small-signal model for both the feed-forward and feedback paths and the accompany block diagram for computing the closed-loop gain under the assumption that $\beta \gg 1$ . In the

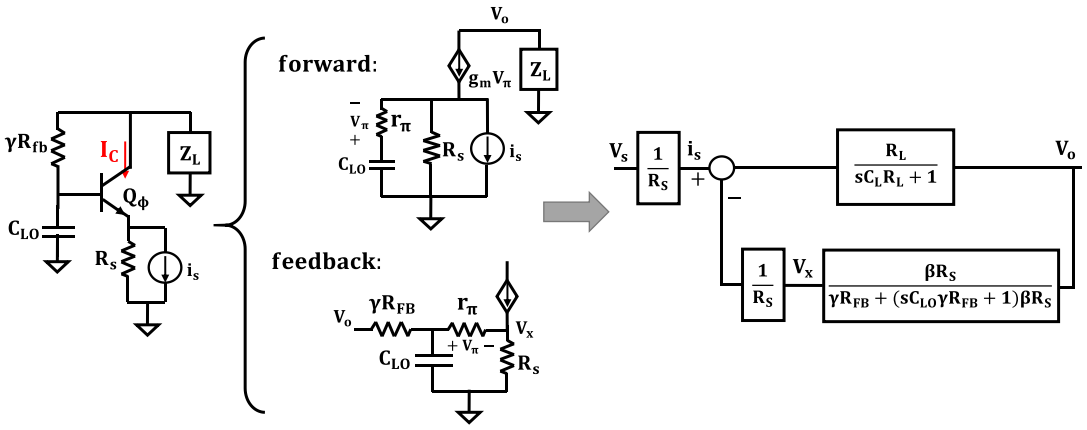


Fig. 3.6 The small signal model and the block diagram representation of the mixer core

feed-forward path, RF current, $i_S$ passes through a common base buffer degenerated by the source impedance, $R_S$, into the load impedance, $Z_L$, such that the transfer function is given by

$$V_o \cong i_s \frac{R_L}{sC_L R_L + 1} \tag{3.12}$$

In the feedback path, we note that perturbations on $V_X$ will generate a current across $R_S$ flowing against $i_S$. Thus, we are interested in the transfer function $V_X/V_o$. From the small signal model in Fig. 3.6 and assuming $\rho \ll 1$,

$$V_x \cong V_o \frac{\beta R_S}{sC_{LO}\gamma\beta R_s R_{FB} + (\beta R_s + \gamma R_{FB})} \tag{3.13}$$

Combining (3.12) and (3.13) in the block diagram from Fig. 3.6 the closed-loop transfer function simplifies to

$$\frac{V_o}{V_s} = \frac{s(\gamma\beta C_{LO} R_S R_{FB} R_L) + (\beta R_S R_L + \gamma R_{FB} R_L)}{s^2(\gamma\beta C_L C_{LO} R_L R_{FB} R_S^2) + sR_S(\gamma\beta C_{LO} R_{FB} R_S + \beta C_L R_L R_S + \gamma C_L R_L R_{FB}) + R_S(\beta R_S + \gamma R_{FB} + \beta R_L)} \tag{3.14}$$

whose dimensionless expression with $\Lambda = R_L/R_S$ and $\chi = \gamma R_{FB}/r_\pi$ gives

$$\lim_{s\to 0}\left(\frac{(sC_{LO}\gamma R_{FB} + 1 + \chi\rho)}{\Lambda^{-1}(sC_L R_L + 1)(sC_{LO}\gamma R_{FB} + 1 + \chi\rho) + 1}\right) = \frac{\Lambda(\chi\rho + 1)}{\Lambda + \chi\rho + 1} \tag{3.15}$$

Since we can minimize both $\rho$ and $\chi$, the maximum conversion gain $R_L/(R_L + R_S)$ resembles that of a voltage divider between $R_S$ and $R_L$, just as is the case for MOS implementations of N-path filters. Additionally, because the loop gain $AB = \Lambda \leq 1$ for

impedance match and there are two poles in the transfer function, the system with feedback is stable.

### *3.4.2 Input Impedance Tuning Range*

From Fig. 3.5, it is evident that while (3.3) would suggest that $Z_{in}$ could reach any real and imaginary values depending on the tunable baseband impedance, accounting for $Z_{sh}$ sets an upper bound on $Z_{in}$. In [3] it was also demonstrated that the reachable complex-valued $Z_{in}$ is confined to a circle centered at ½ $(Z_{sh} + R_{sw})$ with radius ½ $(Z_{sh} - R_{sw})$ and up to a 50Ω match could be achieved at 5 GHz with inductive resonance. In comparison, for the $f_T = 220$ GHz device in [24], $\omega_m \approx 200$ GHz and a 50Ω match can be achieved up to 80 GHz. Fig. 3.7 shows the circles ($R_L \to \infty$, $C_L$ swept from $-\infty \to \infty$) which confine the reachable input impedance for $\omega_{LO}/\omega_m$ = 0.0005, 0.005, 0.05, and 0.5.

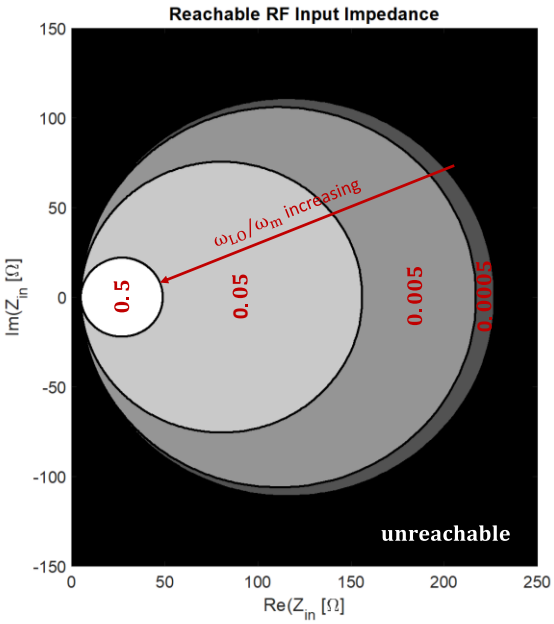


Fig. 3.7 Reachable input impedance swept from $\omega_{LO}/\omega_m$ = .0005 to .5

### *3.4.3 Implications for Noise*

Although BJTs are known to contribute less noise ($2kT/g_m$) than FETs ($\sim 4kTR_{SW}$), the presence of a conduction path between the collector and base for the HBT implementation of impedance transparency introduces some non-intuitive noise behavior:

1) the feedback impedance is not positioned directly between the output (collector) and the input (emitter)
2) the common base description becomes incomplete because the base node is no longer grounded.

Summing the uncorrelated noise contributions of each of the noise sources in Fig. 3.8, the noise factor is

$$F = 1 + \frac{\gamma R_{FB}}{R_S} + \frac{\gamma^2 R_{FB}^2}{2r_\pi R_S} + \frac{(r_\pi + \gamma R_{FB})^2}{r_\pi R_S \beta} + \frac{(r_\pi + \gamma R_{FB} + \beta R_S)^2}{\beta^2 R_L R_S} \tag{3.16}$$

where $R_{FB}$ is the real part of the impedance in feedback and $R_L$ is the parallel

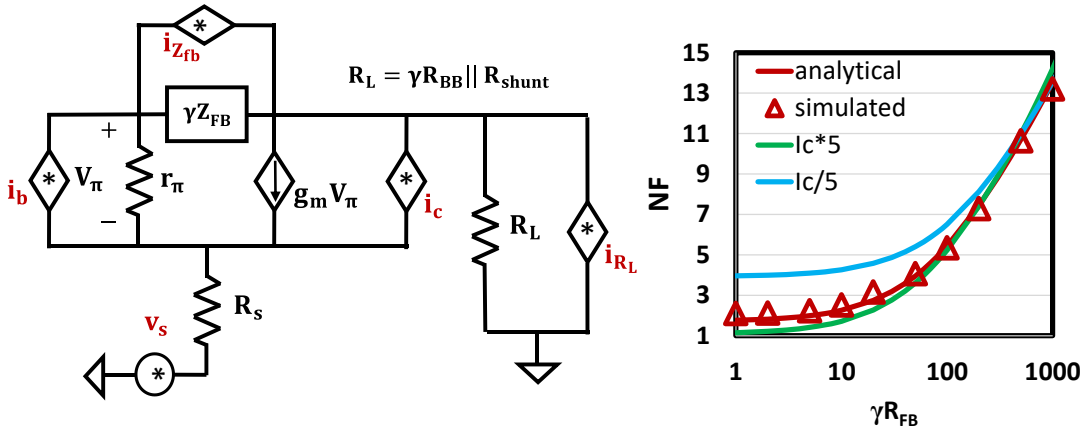


Fig. 3.8 Small signal model for noise analysis and plot of NF vs. $R_{FB}$

combination of baseband load scaled by gamma and the loss mechanisms derived in section III. Two important observations with regard to optimizing for noise can be made from (3.16). First, while a lumped element resistor can be used to provide the impedance match in $R_L$ , the match can also be provided by a $A_{BB}$ times larger resistor in feedback around an amplifier of gain $A_{BB}$ such that the baseband noise resistance is scaled by $1/A_{BB}$. Secondly, there is a strong dependence on $R_{FB}$, which is a free design parameter that can be minimized. Thus, if we assume that $\chi \ll 1$, (3.16) can be simplified and expressed in dimensionless variables as

$$F \cong 1 + \rho(1 + \chi\beta) + \frac{(1+\rho)^2}{\Lambda} \tag{3.17}$$

What can be observed is that by minimizing both $\chi$ and $\rho$ which are both user-selected design parameters, (18) simplifies to $1+\Lambda^{-1}$, which for an impedance match from a discrete load resistor yields $\Lambda_{max}$=1 and $NF_{min} = 3dB$. Taking into consideration all user-selected design parameters as well as process defined parameters, $\Lambda^{-1}$ can be written as

$$\Lambda^{-1} = \frac{1}{\rho}\left[\frac{2\pi\omega_{LO}\tau}{N\Psi} + \frac{1}{sinc^2\left(\frac{\pi}{N}\right)}\left(\frac{1 - sinc^2\left(\frac{\pi}{N}\right)}{1 + \left(\frac{N\omega_{LO}}{\omega_m} + \rho\right)^{-1}} + \frac{\rho N R_S}{R_{BB}}\right)\right] \tag{3.18}$$

where the three terms correspond to the effects of overlap, harmonic loss, and the discrete, noise-contributing baseband load impedance, respectively. Note that even for $\omega_{LO}/\omega_T \ll \rho/N$, $Z_{sh,max} \cong 4.2\,(R_S + R_{SW})$. Thus, while the effects of $R_{Sh}$ are pushed out by the higher $\omega_m$ and $R_{OL}$ is significantly increased, these LTI loss models are still

only hundreds of ohms in parallel with $R_{BB}$ making each term in (3.18) significant.

By utilizing baseband techniques that eliminate the need for a discrete load resistor, the NF limit drops below 3dB with a heavy dependence on both $I_C$ and $R_{FB}$. Fig. 3.8 shows the effect of $R_{FB}$ on the noise figure both analytically – assuming $Z_{sh}$ and $R_{OL}$ are maximized and the noise contribution of $Z_{BB}$ is ignored – and in simulation with ideal 25% duty-cycle non-overlapping pulses at $\omega_{LO}/\omega_T = .001$. As predicted, with large $R_{shunt} = Z_{sh}||R_{OL}$, $\chi \ll 1$ , antenna impedance of 50Ω, and moderate current bias of 2.6 mA, the minimum achievable noise figure is about 1.7 dB with 1 dB degradation from $R_{FB}$ rising to 20Ω. However, $\chi \ll 1$ needed to attain minimal NF comes at a cost: small $R_{FB}$ both presents a resistive load to the LO and necessitates a large AC-coupling capacitor increasing the power consumption of the LO buffer.

Additionally, because one of the key differences between the CMOS and BJT implementation is the current bias, the model also predicts the trade-off between power and NF through ρ and $Z_{sh}$ when the noise contribution of $Z_{BB}$ is ignored. Fig. 3.8 also shows that for 5 times larger mixer bias current the best-case NF improves by 0.9 dB and for 5 times less, the NF degrades by 3.6 dB. A more thorough examination of the trade-off between NF and power due to both ρ and $R_{FB}$ is presented in section 3.5.

### *3.4.4 Implications for Out-of-Band Linearity*

Intrinsically, BJTs are known to be more non-linear than MOSFETs. For a BJT in a common-base configuration, the collector current is an exponential function of the input voltage and can described by its 3rd order Taylor series expansion as:

$$I_C = I_{DC} + g_m V_{in} + \frac{g_m}{2v_T} V_{in}^2 + \frac{g_m}{6{v_T}^2} V_{in}^3 + O(V_{in}^4) \tag{3.19}$$

If we perform the same expansion on the topology given in Fig. 3.9, the collector current sees an additional degeneration resistance ($R_{degen}$) comprised of the source impedance in series with the beta-scaled $\gamma R_{FB} || \gamma R_{buf}$ such that

$$I_C = \frac{g_m}{1 + g_m R_{degen}} V_{in} + \frac{g_m(1 - 2g_m R_{degen})}{6v_T^2\left(1 + g_m R_{degen}\right)^5} V_{in}^3 + O(V_{in}^5) \tag{3.20}$$

where for an N-path filter with an even number of phases and N>2, all even order terms are cancelled, simplifying the differential collector current to its odd terms. For a weak in-band signal $A\cos(\omega_{ib}t)$ and a strong out-of-band blocker $B\cos(\omega_{bl}t)$, (3.19) can be expanded such that the terms which carry signal at the fundamental are

$$I_C = \left(a_1 A + a_3 A B^2 \frac{3}{2}\right) cos(\omega_{ib} t) + \cdots \tag{3.21}$$

Since $a_3 < 0$, there is a value of B such that the output swing of the in-band tone, nominally $a_1 A$, will compress by 1 dB. This out-of-band cross-compression, B1dB, as

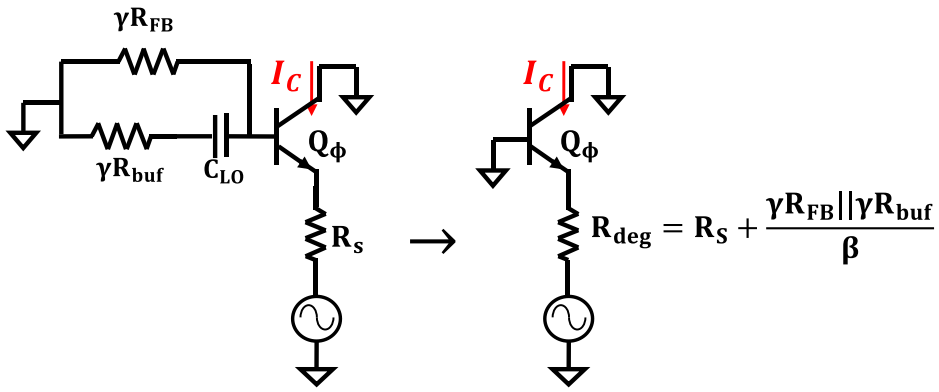


Fig. 3.9 The single transistor model used to compute OOB linearity

well as IIP3 are proportional to the coefficients of (3.20)

$$B1dB, IIP3 = C\sqrt{\frac{a_1}{a_3}} = C\ v_T \frac{\sqrt{6}\left(1 + g_m R_{degen}\right)^2}{\sqrt{|1 - 2g_m R_{degen}|}} \tag{3.22}$$

where C is the coefficient corresponding to the metric of interest. Thus, although BJTs are known for their exponential, non-linear behavior, the out-of-band linearity of the proposed HBT-based N-path filter benefits from increasing the product $g_m R_{degen}$ where the potentially high $g_m$ enhances the effect of degeneration coming from the characteristic impedance of the antenna. If this product is sufficiently larger than 1 and assuming both $\gamma R_{FB}/\beta \ll R_s$ and $\gamma R_{FB}/\beta \ll 1/g_m$, then $g_m R_{degen}$ can be approximated to be $1/\rho$ such that (3.22) simplifies to

$$B1dB, IIP3 \cong C\frac{v_T\sqrt{3}}{\rho^{3/2}} \tag{3.23}$$

Similar to the derivation in [17], it can be seen that the out of band linearity is set by the device parameter $v_T$ and a free design parameter $\rho$ with a dependency of $\rho^{-3/2}$, which is also predicted for MOS implementations of N-path filters where $\rho \ll 1$. Although $v_T$ is small, requiring smaller $\rho$ to achieve the same B1dB or IIP3 as their MOS counterparts, this can easily be achieved by increasing $I_C$. In section 3.5, it is shown that further decrease in $\rho$ can further increase B1dB but at the expense of NF degradation.

### *3.4.5 Implications for Power Consumption*

When using BJTs, power consumption is inevitable and often cause for concern. The two main sources of power consumption, the mixer core and LO generation, exhibit classic trade-offs between power and performance. It can be easily derived for $\gamma R_{FB}/\beta \ll 1/g_m$ that

$$P_{mix} = \frac{v_T VDD_{mix}}{\rho R_S} \tag{3.24}$$

While from (3.23) and (3.24) it can be seen that ρ has a monotonically decreasing relationship with both power and linearity, combining (3.17) and (3.18) reveals that there is also an optimal ρ for minimizing NF at every frequency.

With regard to LO generation, while the exact power consumption depends on the buffer topology utilized, generally the power is proportional to the load capacitance, frequency, and voltage squared. For the same triangular waveforms from Fig. 3.4 and pulse height of $V_{LO}$

$$P_{buf} = 2NV_{LO}^2 C_{mix} f_{LO} = \Psi^2 \frac{\omega_{LO}}{\omega_T} \frac{N v_T^2}{\pi \rho R_S} \tag{3.25}$$

While (3.25) does not represent the generation of ideal quadrature 25% duty-cycle non-overlapping pulses, given our analysis in sections 3.3 and 3.4, it is evident that the HBT-based N-path filter can tolerate overlap without significant degradation in performance. Thus, power does not need to be burned to achieve large-swing, non-overlapping pulses and this will be explored further in the subsequent section.

## 3.5 Optimization and Design Trade-Offs

Having considered the fundamental limits associated with free design parameters as well as process defined parameters, we now turn out attention to making use of our analysis from sections 3.3 and 3.4 to inform design decisions and optimization. In particular, we will examine the classic design-space spanning power, noise, and linearity and present a methodology for the simultaneous optimization of all three. Following this we present considerations for LO generation in HBT N-path receivers which ultimately establishes a better trade-off between performance and power than for MOS N-path receivers. Finally, because

1) these metrics depend on $\rho$
2) the designer's control over $\rho$ is different for HBT N-path receiver
3) a whole range of $\rho$ can be utilized for a given device size

we conclude this chapter with our recommended design methodology for establishing the proper emitter length for a given power budget and target performance specifications.

### *3.5.1 Designing for NF, Linearity, and Power Simultaneously*

To optimize for maximal out-of-band B1dB and minimal NF simultaneously, we define dynamic range to be their difference (DR = OOB B1dB-NF). Since B1dB, which is proportional to $\rho^{-3/2}$, decreases monotonically, there is no $\rho_{optimal}$ for DR. However,

since there is a $\rho$ that optimizes NF, we weigh NF more heavily in determining $\rho$ for optimal DR by limiting the allowable degradation in NF to +1dB. Fig. 3.10 shows that an HBT N-path mixer operating at $\omega_{LO}/\omega_m \sim 0.05$ and driven by LO as weak as 400 mV demonstrates > 8 dB improvement in dynamic range at the expense of ~1 dB degradation in NF from $NF_{opt}$. As expected, ρ optimized for DR is smaller than for NF, and thus requires more power.

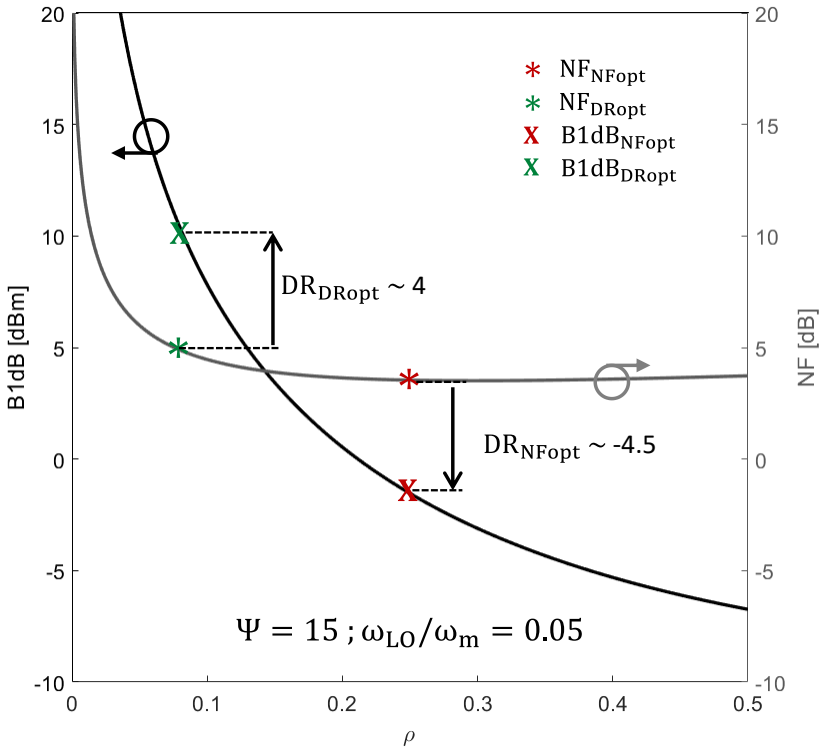


Fig. 3.10 OOB B1dB and NF with associated dynamic range

## *3.5.2 LO Generation Considerations*

While for both MOS and HBT N-path mixer cores there is an evident trade-off between power and performance, for HBTs significant power reduction can be obtained by

relaxing and/or eliminating elements of the LO generation chain with minimal impact on performance. By combining our brief analysis on LO generation power with our understanding of the effects of LO overlap and the difficulty of non-overlapping pulse generation at mm-wave frequencies, we suggest 3 techniques that significantly save power and only slightly reduce performance:

1. Reducing $V_{LO}$: Reducing LO swing reduces power consumption of the LO buffer with minimal impact on NF and linearity which are both primarily set by ρ. Fig. 3.11 shows NF, dynamic range, and power consumption of the buffer while sweeping pulse size across the x-axis and frequency across the family of curves.

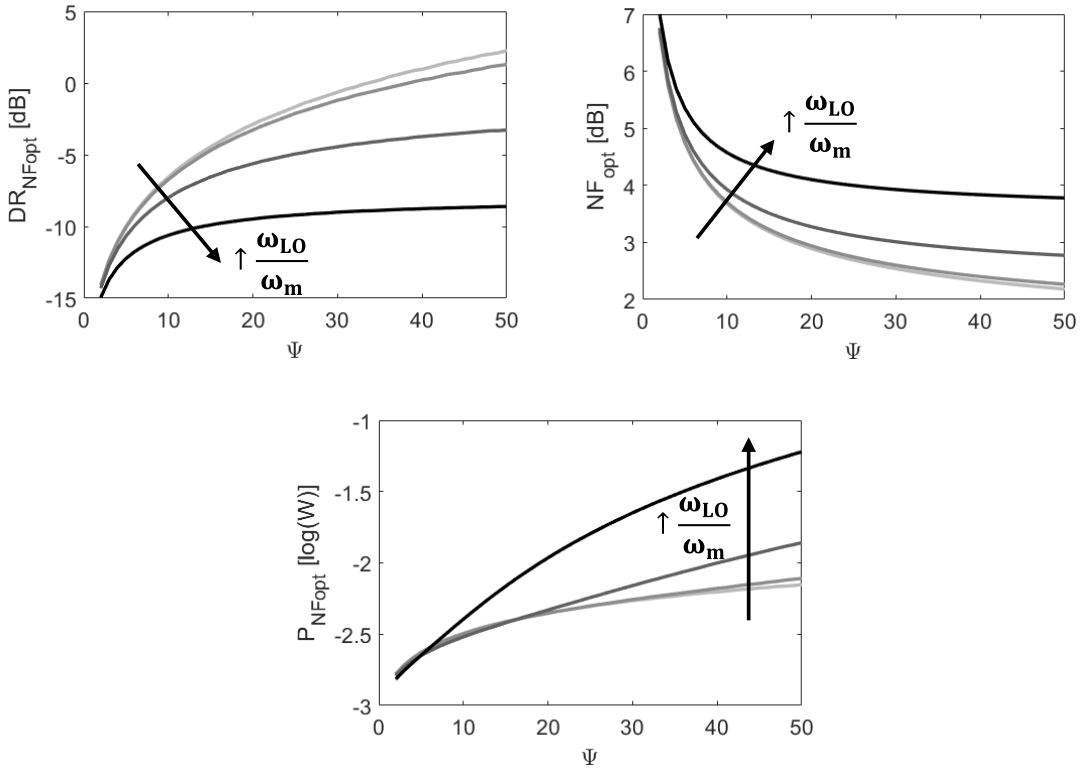


Fig. 3.11 Theoretical minimum noise figure, maximum dynamic range, and the associated power consumption

Because $Z_{sh}$ and $R_{SW}$ impact NF in opposite directions, plots display performance metrics at the $\rho_{optimal}$ that corresponds with each frequency and pulse size. As expected from (3.25), power is quadratically proportional to $\Psi$ and linearly proportional to $\omega_{LO}/\omega_m$. But more importantly , for large $\omega_{LO}$, the NF improvement from further increase in $\Psi$ beyond ~15 is minimal while power consumption increases by nearly an order of magnitude from 15 (~0.4V) to 50 (~1.3V, the nominal $V_{LO}$ needed for MOS N-path mixers).

2. Utilizing non- 25% duty-cycle overlapping quadrature pulses: Because the key parameter in $R_{on,HBT}$ is $\Delta V_b$ (not the absolute value of $V_b$), the same $R_{OL}$ and mixer power can be achieved by the non-overlapping 25% duty cycle pulses with rise and fall times $(2Nf_{LO})^{-1}$ and overlapping 50 % duty cycle pulses with rise and fall times $(Nf_{LO})^{-1}$ in Fig. 3.12. Thus, while high-performance 4 phase MOS N-path mixers

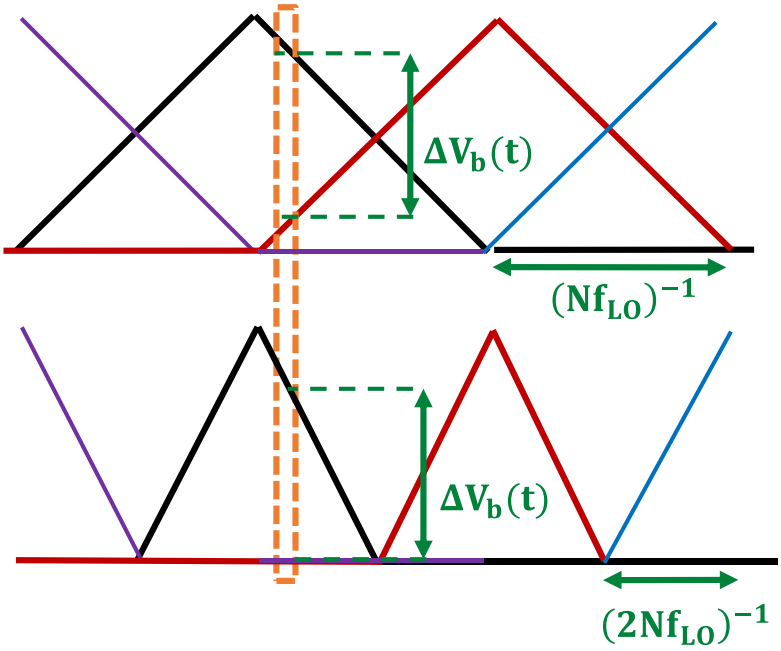


Fig. 3.12 Comparison of $\Delta V_b(t)$ for 25% and 50% duty cycle triangle waves

must be driven by quadrature non-overlapping 25% duty cycle pulses (often generated by high-bandwidth digital logic gates), their HBT counterparts can be driven by less design-intensive and less power-consumptive 50% duty cycle pulses while maintaining high performance.

3. Generating LO with resonant EM structures : As demonstrated in [20,22], quadrature sinusoids can be used for low-power mm-wave MOS N-path mixers but either at the expense of linearity or noise such that DR ~ -10. Because the assumption of comparator-like switching behavior for HBT N-path mixers does not hold when $\Delta V_b$ changes slowly relative to the period of the waveform, the ratio of emitter currents does not remain constant with increasing $I_{RF}$ as illustrated in Fig. 3.13. While (3.1) does hold for emitter currents under current steering, $\Delta V_b$ must now also account for voltage drops across the HBT base resistance, $r_b$. Because $I_{e0} >> I_{e90}$, the voltage drop across $r_{b0}$ is much larger than that across $r_{b90}$. For simplicity, one could assume that $\Delta V_{be90}$ is negligible, then conclude that owing to

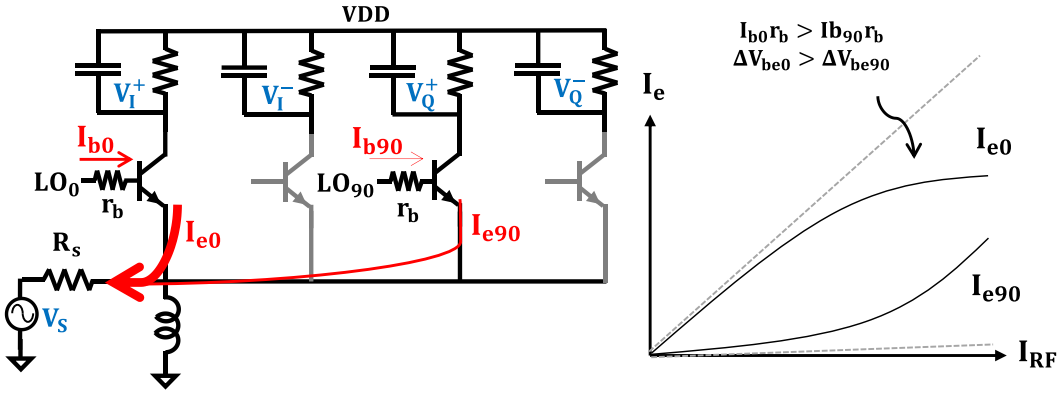


Fig. 3.13 Mechanism for input compression when ideal current steering assumption does not hold

the smaller $\Delta V_b$ in (3.1), the ratio of currents drops. As $I_{RF}$ increases, $\Delta V_b$ drops more and effectively compresses the signal on the RF port. Note that such an effect only presents itself when $\Delta V_b = LO_0 - LO_{90}$ is small, as would be the case under sinusoidal drive or extremely low $\Psi$. Measurements show that under such a phenomenon, OOB B1dB for a $\rho$ selected for ~9 dBm drops to ~6 dBm [3]. Combining this effect with the NF degradation of ~ 2dB estimated for low $\Psi$ in Fig. 3.11, it can be estimated that DR degrades by approximately 5 dB. With $\rho$ optimized for DR as in Fig. 3.10 this would give $DR = -1$ dBm which is still 9 dB better than reported values for mm-wave MOS N-path mixers [20,22].

In summary, given that for $\omega_{LO}$ approaching $\omega_m$,

1) dropping $V_{LO}$ from 1.3V to 400 mV corresponds to less than 1 dB of NF degradation
2) HBT N-path mixers can achieve high performance with 50% duty-cycle pulses
3) much lower-power and less design-intensive sinusoidal LO drive can be employed for a slight performance degradation,

HBT N-path receivers exhibit a different and arguably better power versus performance trade-off than their MOS counterparts. This is especially true for higher center frequencies. Thus, it is left to the designer to determine how much design effort and power budget must be dedicated to LO generation and/or whether to compromise on target performance specifications in favor of a simpler, low-power LO generation chain.

### *3.5.3 Recommended Design Methodology*

Unlike MOS N-path mixers whose ρ is set by device sizing during design and fabrication, the HBT N-path mixer $R_{FB}, v_T,$ and β are set, but ρ remains variable by adjusting $I_C$. For a given range of desired $I_C$, there is a corresponding emitter length that will maximize $f_T$. Thus, we suggest the following process for designing HBT N-path mixers:

1. use equations in Table I to establish target specifications
2. determine range of desired $\rho_{opt}$ and associated range of $I_C$
3. determine $V_{LO}$ and LO generation architecture that will simultaneously meet power budget and target specifications
4. iterate steps 1-3 until both power budget and target specifications are met
5. select $L_{emitter}$ that maximizes $f_T$ across desired range of $I_C$

CHAPTER 4

# FIRST GENERATION HBT N-PATH RECEIVER FOR < 12 GHz

## 4.1 Introduction

The first generation of the HBT N-path receiver had one main goal: to demonstrate that impedance transparency could be achieved using inherently unidirectional bipolar-type transistors. Having acknowledged that InP HBTs are capable of much higher $f_T$ than most, if not all, MOS-type transistors [25] and that the maximum operation frequency for N-path mixers is proportional to $f_T$, demonstrating impedance transparency with bipolar-type transistors would enable N-path mixer performance – moderate noise with reconfigurable impedance match and high out-of-band linearity with low out-of-band impedance – at much higher frequencies than traditional MOS N-path filters could cover. While many different impedances could be used in feedback, we demonstrated impedance transparency with the simplest element: a resistor.

In this chapter, the limitations on performance set by using a lumped-element resistor in feedback will be examined and the relationship between loading of the LO buffer, area utilized to couple the LO to the mixer, and noise figure will be explored. Section 4.2 will provide the analysis for the minimum achievable noise for a given value of the feedback resistor. While this proof-of-concept work utilized a high-power Johnson counter divider with ECL blocks like those presented in chapter 2, section 4.3 will describe the key differences between the LO generation chains for the GaAs mixer and the HBT mixer load. Finally, section 4.4 will provide measurement results for conversion gain, impedance transparency, linearity, and noise figure which all serve to prove that HBTs can be used for N-path receiver architectures and that their performance can be well-predicted by our proposed theory and models.

## 4.2 Mixer Core: LTI Resistor in Feedback

According to the analyses performed in section 3.4, three main user-defined dimensionless variables (ratios) determine the performance of the HBT-base N-path filter: $\Lambda = R_L/R_S$ (which should be maximized), $\rho = 1/g_m R_S$, and $\chi = \gamma R_{fb}/r_\pi$ (which so far have been assumed to be minimized).

$\Lambda$ can be maximized, but to maintain impedance matching a load where $\gamma R_{BB} = R_S$, the maximum remains 1. $\rho$ can generally be minimized for $\omega_{LO}/\omega_m < \rho/N$, but for larger $\omega_{LO}$, $\Lambda$ becomes proportional to $\rho$ leading to the existence of an optimal $\rho$ which varies with $\omega_{LO}/\omega_m$. $\chi$ can be minimized indefinitely to reduce NF, but as $R_{FB}$ decreases, LO buffer power consumption increases to drive the smaller input impedance. This means that an adjustment must be made to our simplified expression for (17) to determine how small $R_{FB}$ should be. Assuming no simplifications, but translating all terms of (17) into dimensionless ratios we arrive at

$$F = 1 + \rho\left[(1+\chi)^2 + \chi\beta\left(1+\frac{\chi}{2}\right)\right] + \frac{[1+\rho(1+\chi)]^2}{\Lambda} \tag{4.1}$$

For $\gamma R_{FB} = R_S = R_L$ such that $\chi\beta\rho = 1$ and assuming that $\beta \gg 1/\rho$, (4.1) achieves a minimum of F= 3 (~4.8 dB NF) with a strong dependence on $\rho_{opt}$ given by

$$F \cong 3 + \frac{1}{2\beta\rho_{opt}} + \rho_{opt} \tag{4.2}$$

Additionally, when capacitor area and AC coupling corner are of concern, a larger $R_{FB}$ may be necessary such that $\chi \geq 1$. Note that large capacitors can significantly increase

route length and introduce bends in critical RF routing. Under this condition, (3.16) simplifies to

$$F \cong 1 + \frac{\chi^2 \beta \rho}{2} + \frac{(1 + \rho\chi)^2}{\Lambda} \tag{4.3}$$

Because the implemented HBT-based N-path mixer is loaded by lumped element pull-up resistors for impedance matching to a 50Ω source, $\Lambda = 1$. Again, assuming that $\beta \gg 1/\rho$, (4.3) simplifies to

$$F \cong 2 + \frac{\chi^2 \beta \rho}{2} \tag{4.3}$$

For small values of $\chi$, (4.3) predicts a larger NF than is shown in the plot from Fig. 3.8. However, as $\chi$ increases and dominates the term from $\Lambda = 1$, (4.3) comes into alignment with the plot and validates our assumptions. Measurements which will be presented in section 4.4 are also consistent the theory.

## 4.3 LO Generation: ECL Johnson Counter Divider

Unlike traditional CMOS N-path receiver architectures which require approximately 1.2V of non-overlapping swing to sufficiently drive mixer switches to low $R_{on}$, the HBT-based N-path mixer steers current between core devices with as little as 250 mV. However, larger amplitude is needed to ensure that LO signals strongly dominate over the baseband signals when combined. While a single stage could be sufficient to drive the mixer with this necessary swing, the loading on the AND gate limits the frequency

of operation. Instead, if a very weak pre-amplifier buffers the AND gate from the mixer-driver, higher frequency operation can be attained for a slight cost in area and power. To minimize the power consumption of this pre-amplifier we recognize that it can run off a separate power supply from the mixer driver. Additionally, as compared to the buffer utilized in chapter 2, the pull-up and pull-down signal paths are designed to minimize area and power as demonstrated in Fig. 4.1. All resistors are sized to minimize noise while providing a sufficient AC coupling corner of 200 MHz with $C_{AC}$. To reduce the number of pads, pull-up bias is tied to the collector supply and $V_{amp}$ and $V_{bias1}$ is shared. Lastly, to significantly reduce area, output resistance to present a stable output impedance is removed and transistor width is adjusted for less current. All other elements of high-bandwidth ECL logic are reused.

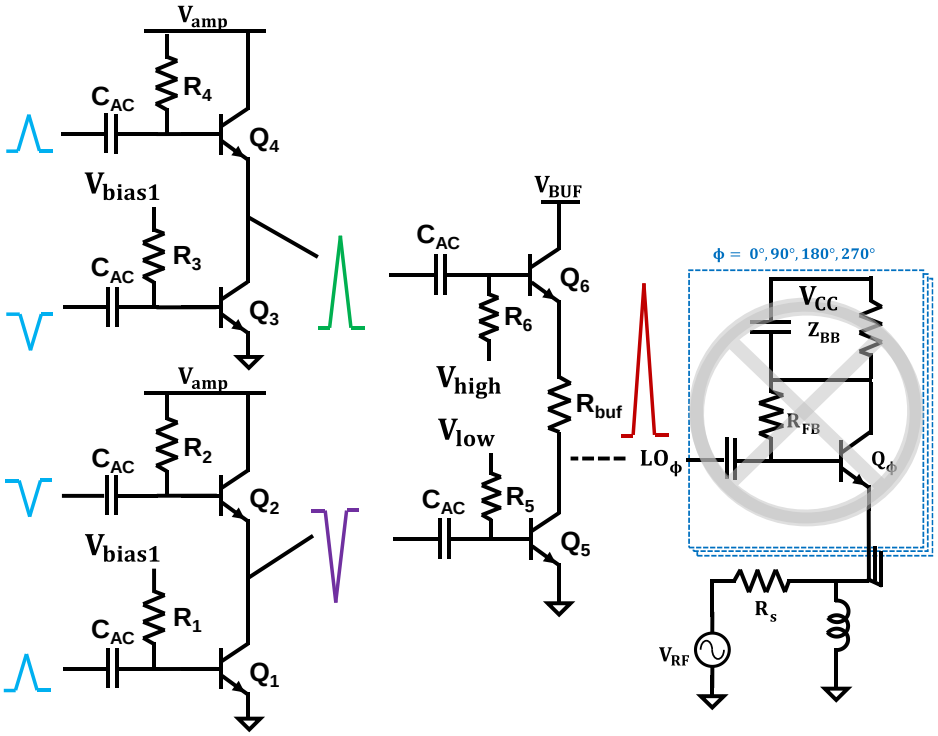


Fig. 4.1 Modified 2-stage buffer for 1st Gen HBT N-path mixer

## 4.4 Measurements Consistent with Theory

The 1st generation of the HBT-based N-path mixer designed to be tunable from 0.3-12 GHz was fabricated in GlobalFoundries BiCMOS 8HP with an active area of 0.81 $mm^2$. Die photo is given in Fig. 4.2. Because the LO generation was implemented by Johnson-counter dividers, the lower end of the tuning range was set by the size of $C_{LO}$ and $R_{FB}$ that optimized the available area.

All measurements, unless otherwise noted, were done with baseband impedance set by off-chip $R_{BB}$ = 300 Ω and $C_{BB}$ = 1nF with a baseband BW approximately 800 kHz. On PCB, I and Q baseband signals were recombined by poly-phase filter and subsequently fed into a differential-to-single-ended amplifier with tunable gain. Gain of off-chip amplifier was determined by the gain-setting where noise from the mixer was distinguishable from the noise floor of the sampling ADC.

PCB was produced on impedance-controlled laminate with all routing for LO and RF on impedance matched 50Ω coplanar waveguides. All pads of the SiGe chip were directly wirebonded to ENIG pads on the PCB. All reported results have cable losses and board losses de-embedded and LO power delivered to the LO pads is 10 dBm.

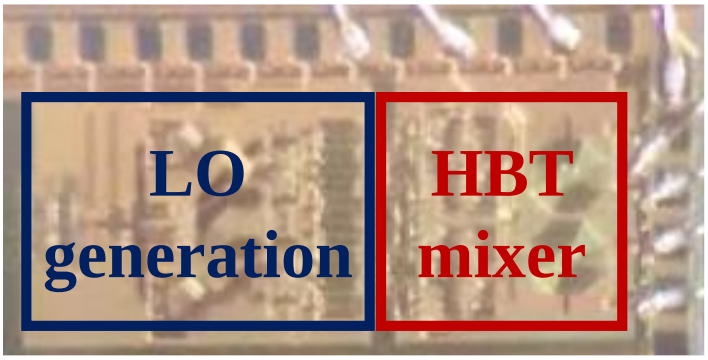


Fig. 4.2 1st generation HBT N-path mixer die photo

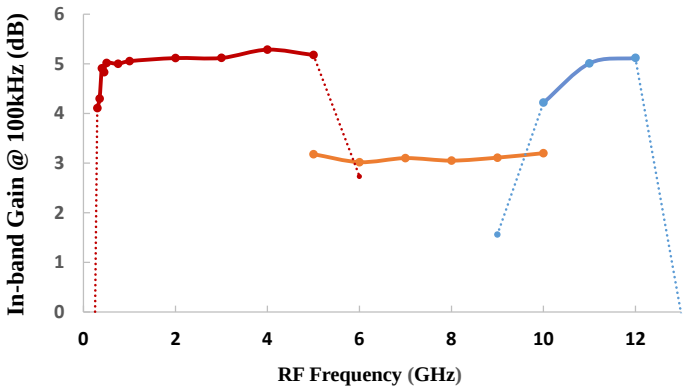


Fig. 4.3 Conversion gain for 1st gen HBT N-path mixer

### *4.4.1 Measured Conversion Gain*

Fig. 4.3 shows the measured in-band voltage gain across the entire tested LO range from 500MHz to 26 GHz which translates to RF input range from 250MHz to 13 GHz. In band, the gain was between 3dB and 5 dB depending on whether it was in the low (< 5 GHz), mid (5 GHz to 10 GHz), or high (>10GHz) frequency range of operation. Note that for ideal single balanced mixing with $R_s = 50\Omega$ and $R_{BB} = 300\Omega$ values followed by an off-chip 10 dB amplifier, a gain of 4 dB is expected. The in-band gain dropped by 3 dB below 300MHz and above 12GHz, so we consider the full operating range of the receiver to be from 300 MHz to 12 GHz. Although the LO pulse buffer was designed to provide sufficient current drive for high frequency operation, it proved difficult to find a single bias state that worked well for all frequencies. We boosted LO pulse amplitude for higher frequency operation by increasing $V_{low}$ in Fig. 4.1. Here, we present gain from three overlapping ranges, each with a distinct bias which would be held in a lookup table for real-time receiver operation.

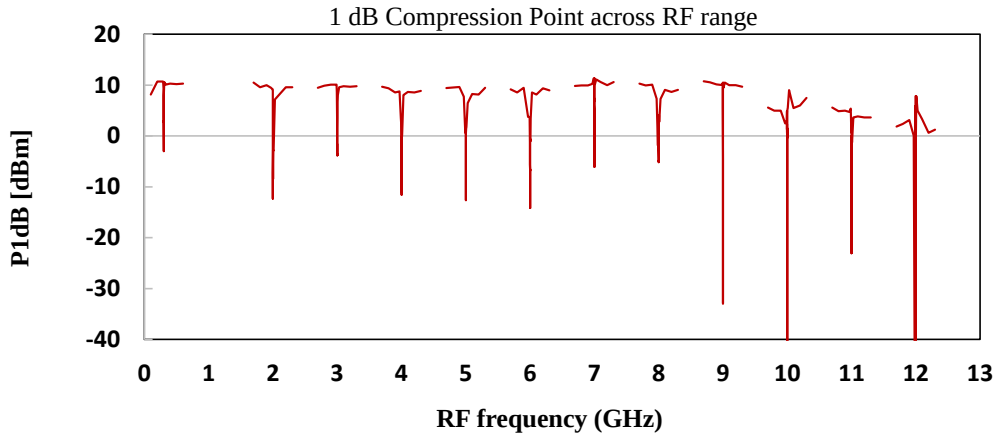


Fig. 4.4 B1dB for 1st gen HBT N-path mixer

### *4.4.2 Measured Out-of-Band Linearity*

According to (3.22) with $g_m$ boosted by the antenna impedance as degeneration, the model for $\rho = 0.087$ predicts 9.5 dBm. Agreement between the model and measurements have been verified with our chip yielding OOB B1dB of 9.4 dBm up to 9 GHz as shown in Fig. 4.4. In-band compression is set primarily by the off-chip amplifier.

However, as the assumption of non-overlapping pulses breaks down at higher frequencies, the effect described in section 3.5.2 kicks in and causes input compression earlier than (3.22) predicts. This can be seen in Fig 4.4 where above 9 GHz the out-of-band B1dB drops more as overlap increases. While input power delivered to the LO pads of the chip remained at 10 dBm and conversion gain from Fig. 4.3 did not drop, likely the pulse shape degraded such that overlap duration increased.

### *4.4.3 Verification of Impedance Transparency*

As a proof-of-concept work, one of the key pieces of evidence of N-path filter behavior is impedance transparency as described in sections 1.2 and 3.2.2. To demonstrate impedance transparency, S11 in Fig. 4.5 shows that in-band impedance match is set by the baseband load while out-of-band impedance is set by the on resistance.

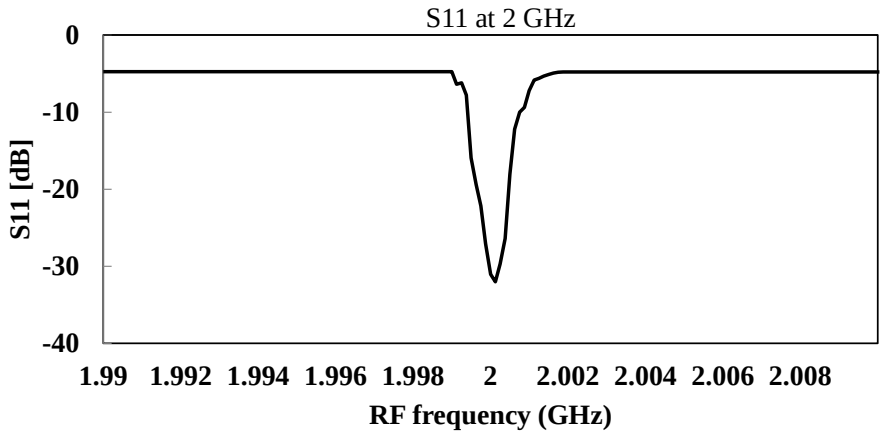


Fig. 4.5 S11 @ 2GHz for 1st gen HBT N-path mixer

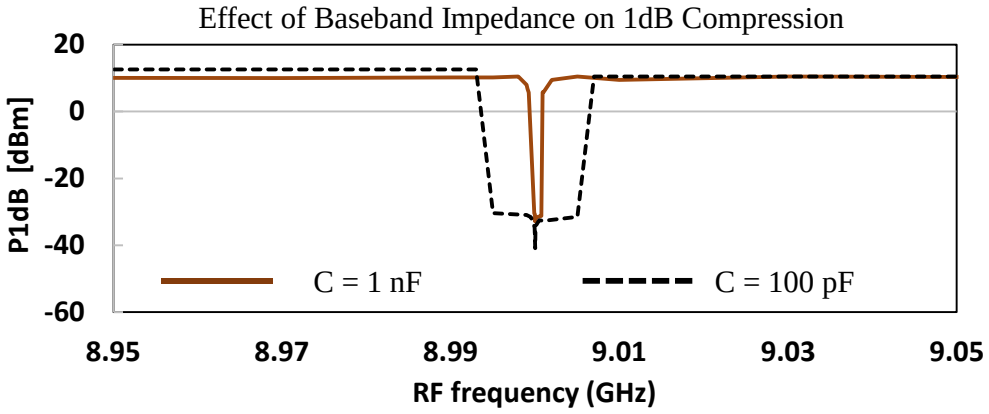


Fig. 4.6 Effect of baseband capacitance

Additionally, a key feature of N-path filters is the reconfigurable RF port impedance bandwidth. For a larger baseband low-pass-filter bandwidth there should be a proportionally wider filter behavior at the antenna. Given this, one would expect the transition band to high out-of-band linearity to be pushed out further from the center frequency as shown in Fig. 4.6.

### *4.4.4 Measured Noise Figure*

We measured noise figure with a 4 GHz LO and 2.0005 GHz RF input. With ρ= 0.087, $\beta \approx 300$, and $\chi$ = 1, (4.3) predicts 11.67 dB and our measurements yielded NF of 12.74 dB at 2 GHz. Since poor noise performance is associated with the large $R_{FB}$, subsequent chapters look at alternate mixer core topologies to reduce NF.

CHAPTER 5

# SECOND GENERATION HBT N-PATH RECEIVER FOR 20 – 40 GHz

## 5.1 Introduction

N-path-based software-defined radios in the sub-6 GHz regime have been shown to enable instantly reconfigurable RF center frequency and bandwidth while maintaining high OOB B1dB and moderate in-band noise figure. However, both the relatively large input capacitance of N-path mixers and the need for quadrature non-overlapping (LO) pulses limit performance of such receivers at mm-wave frequencies [6,21,23,26-28]. Approaches using high bandwidth digital circuitry to generate non-overlapping LO pulses consume high power [6,26] while receivers using resonant EM structures and sinusoidal LO drive [21,23,27] consume less power at the cost of reduced performance. Prior work on HBT-based N-path mixers described in chapter 4 showed impedance transparency from 0.3-12 GHz and high OOB B1dB (9 dBm) but suffered from intrinsically high NF (> 12 dB) and extremely high power consumption (> 1W) [6]. This chapter describes a high dynamic range (DR) receiver in a noise-cancelling configuration where an HBT LNTA, loaded by a quadrature mixer, is protected by an HBT N-path filter with linear-periodically-time-varying (LPTV) feedback for impedance transparency. Mixers are driven by 20-40 GHz, tunable dual-resonant LO buffers which generate 25% duty-cycle pseudo-non-overlapping LO pulses at mm-wave frequencies.

In the work described in chapter 4 we demonstrated impedance transparency and high out-of-band linearity, but the receiver suffered from:

1) high power consumption from the ECL Johnson counter divider and buffers which covered ultra-wide tuning range from 0.3 – 12 GHz

2) high noise figure dominated by large $R_{FB}$ to minimize both area of AC-coupling capacitor and loading on LO buffer

which both motivated and framed our goals for the 2nd generation receiver design:

1) consider alternate feedback impedances which could break the NF, LO-loading, and area trade-off
2) lower power consumption by considering resonant, more narrowband structures and techniques for LO generation
3) under the assumption that our new LO generation would not be capable of re-timing, examine alternate methods for reducing the noise of the LO generation chain

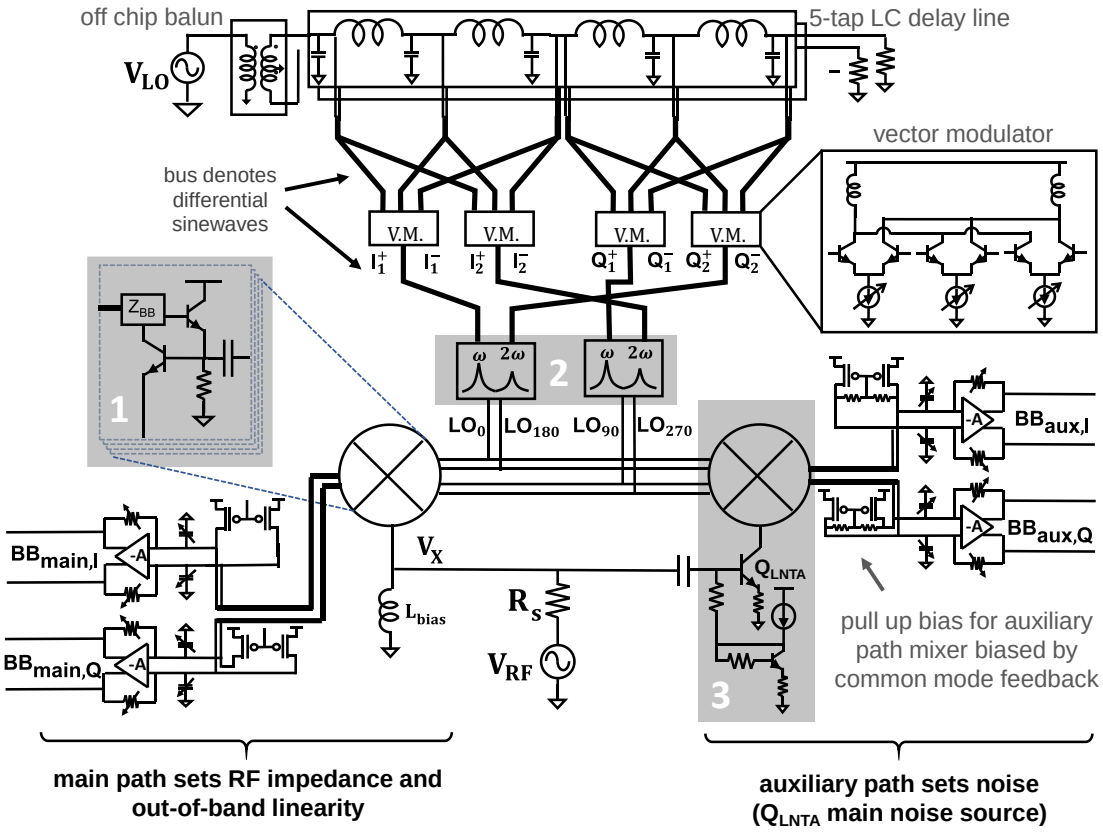


Fig. 5.1 The 2nd gen HBT N-path receiver architecture

In response, the 2nd generation HBT-based N-path receiver is comprised of 3 key techniques in the evolution of HBT-based N-path receivers which each address one of our goals:

1) LPTV feedback impedance for low noise and both reduced LO loading and area
2) Dual-resonant LO buffer for lower-power non-overlapping pulse generation
3) Noise-cancellation for reducing the effect of LO jitter on noise figure

Fig. 5.1 shows the block diagram of implemented single-chip receiver architecture including each of the aforementioned techniques and all auxiliary circuitry. A pair of 5-tap lumped-LC delay lines provide diverse phases which are tunably weighted and combined to generate amplitude and phase balanced quadrature sinusoids across 20-40 GHz. To ensure the proper phase relationship between the necessary currents to generate our pseudo-non-overlapping pulses across the full tuning range, separate vector modulators generate the sinusoids which then generate the fundamental and 2nd harmonic currents from the dual-resonant LO buffer. Finally, mixer basebands are loaded by differential amplifiers of gain A with feedback resistance which can be tuned to provide an impedance match to $R_S$ and cancel out noise generated in the main path. Subsequent sections will cover the theory and implementation details of both the proposed mixer core and LO generation technique, then highlight a use-case of the HBT-base N-path filter as protection for an LNTA, and present measurement results consistent with theory.

## 5.2 Mixer Core: LPTV Emitter Follower in Feedback

Following our analysis in chapter 3, the ideal HBT-based N-path mixer would inject minimal noise from the feedback mechanism ($\chi \ll 1$) while also presenting a large impedance between the collector and base when the LO is driven high ($\chi \geq 1$). For an LTI impedance, such as the lumped-element resistor used in chapter 4, these two requirements are mutually exclusive. However, if we expand our analysis to include linear periodically time-varying (LPTV) impedances, there exists an impedance

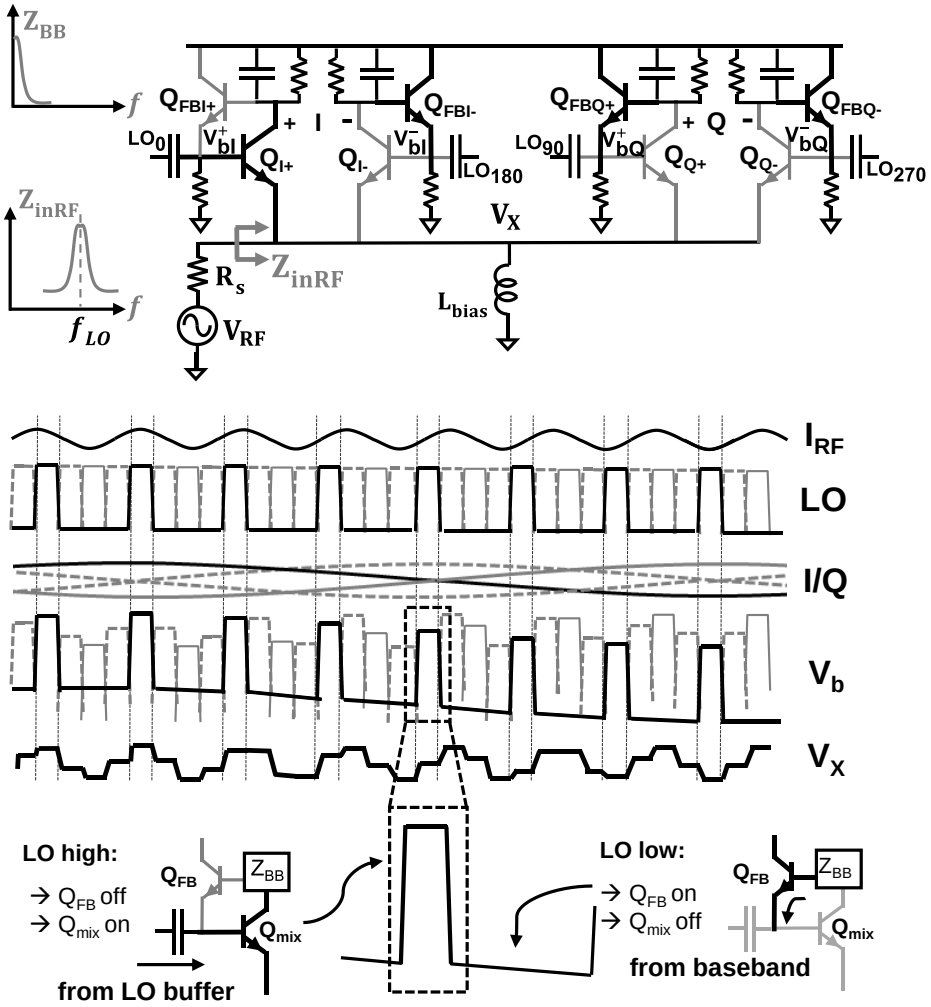


Fig. 5.2 The 2nd gen HBT N-path mixer impedance transparency

which satisfies both of the aforementioned requirements. One such solution, which is the subject of this chapter, is an emitter follower in feedback which would provide a $\sim 1/g_m$ impedance when the base is held low, and a much larger impedance when the LO pulse pulls the base voltage high.

Fig. 5.2 shows the 4-phase HBT N-path mixer driven by wideband non-overlapping quadrature 25% duty-cycle pulses such that the low-pass impedance on the mixer's quadrature baseband port is translated to a band-pass impedance on the RF port suppressing large OOB blockers. The proposed HBT-based N-path mixer utilizes 4 HBTs driven between cutoff (LO low) and forward active (LO high) by this 4-phase pulsed LO.

Prior work [6] in chapter 4 demonstrated that impedance transparency could be achieved in an HBT-based N-path mixer by providing a DC feedback path from the baseband node on the collector to the AC-coupled LO node on the base of each mixer core HBT. However, there was an inherent tradeoff between NF and loading on the LO by the feedback resistor. In this chapter, an LPTV feedback impedance is introduced in the form of an emitter follower. When LO voltage is low, $Q_{FB}$ presents a small resistance between the collector and base such that voltage noise generated by the feedback is negligible and the slow-varying baseband voltage DC-couples to the base. Conversely, when the LO pulses to a high voltage, $V_{BE}$ and $g_m$ of $Q_{FB}$ are small, presenting a large impedance between the collector and base, and the AC-coupled LO pulse is now superposed on the corresponding DC-coupled baseband waveform with minimal loading from $Q_{FB}$. Because $V_x$, the common-emitter voltage on the RF port, tracks the maximum of the mixer's base voltages and the peak of each base voltage tracks the

corresponding DC-coupled baseband waveform, the interaction of the baseband impedance with the down-converted RF current sets the amplitude and phase of $V_X$. Thus, in this work, impedance transparency is achieved while breaking the NF versus LO loading trade-off of the LTI feedback resistance utilized in chapter 4.

## 5.3 LO Generation: Dual-Resonant LO Buffer

### *5.3.1 Theory and Analysis of Dual-Resonance*

Fig. 5.3 shows how combining the fundamental and 2nd harmonic terms of the LO generates quadrature waveforms that much more closely approximate non-overlapping

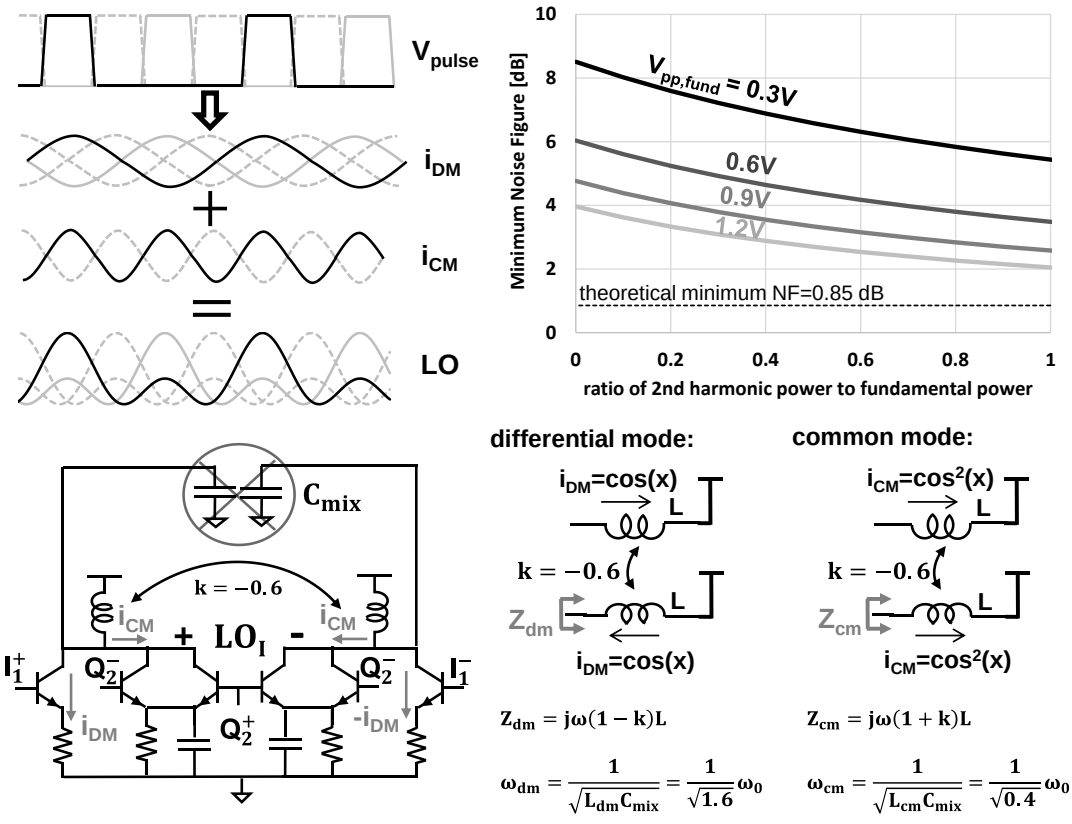


Fig. 5.3 Theory of dual-resonant LO generation

pulses than the fundamental alone. Note that for proper $LO_{I\pm}$ waveforms, $\pm i_{DM}$ at the fundamental are anti-phase while $i_{CM}$ at the 2nd harmonic are in-phase. The plot (upper right) shows theoretical NF curves corresponding to 0.3V steps in fundamental peak-to-peak voltage swing from 0.3V to 1.2V while sweeping the power of the 2nd harmonic demonstrating how the introduction of the 2nd harmonic reduces overlap-induced loss, and consequentially NF. To generate these pseudo-non-overlapping pulses without excessive power consumption, the fundamental and 2nd harmonic must simultaneously resonate with the capacitive mixer load. The bottom of Figure 2 shows the schematic and analysis for the proposed dual-resonant LO generation circuitry. Differential voltages ($I_{1^{\pm}}$) at the fundamental generate differential currents $\pm i_{DM}$ through degenerated common emitter amplifiers. 90°-shifted signals ($Q_{2^{\pm}}$) on the bases of a transistor pair with their collectors shorted generate in-phase currents $i_{CM}$ with a strong 2nd harmonic. To generate LO comprised of both the fundamental and 2nd harmonic, the combined load of the effective inductance and mixer capacitance must resonate differential signals at the fundamental and common mode signals at the 2nd harmonic. Since a pair of coupled inductors has differential mode impedance proportional to 1-k and common mode impedance proportional to 1+k, k=-0.6 yields $\omega_{cm} = 2\omega_{dm}$.

### *5.3.2 Implementation and Layout of Coupled Inductors*

Since the target coupling coefficient is 0.6, the challenge in the coupled inductor design is not achieving the target k, but rather doing so without excessive capacitance which would limit the frequency of operation. Because one side of each inductor pulls up to

supply, two layout configurations were considered. Layouts for equivalent inductance and coupling coefficient are show in Fig. 5.4:

1) Coplanar with via-stitching (left): Because one end of the inductor is tied to supply, a low impedance return path down to the shield allows for the supply end of the inductors to be at the center of concentric spirals. Coplanar spirals allow for via-stitching between two layers of metal in order to reduce the series resistance of the spiral and achieve Q greater than 10. However, due to the multi-turn interwire capacitance necessary for a compact layout and moderately-high coupling, we went with the stacked layout.
2) Stacked (right): The stacked layout depends on the foundry-determined spacing between RF metals to achieve the desired k. With vertical overlap which does not have to be completely overlapping to achieve the desired k, less capacitance between inductor wires allowed for higher frequency performance, but at Q just under 10.

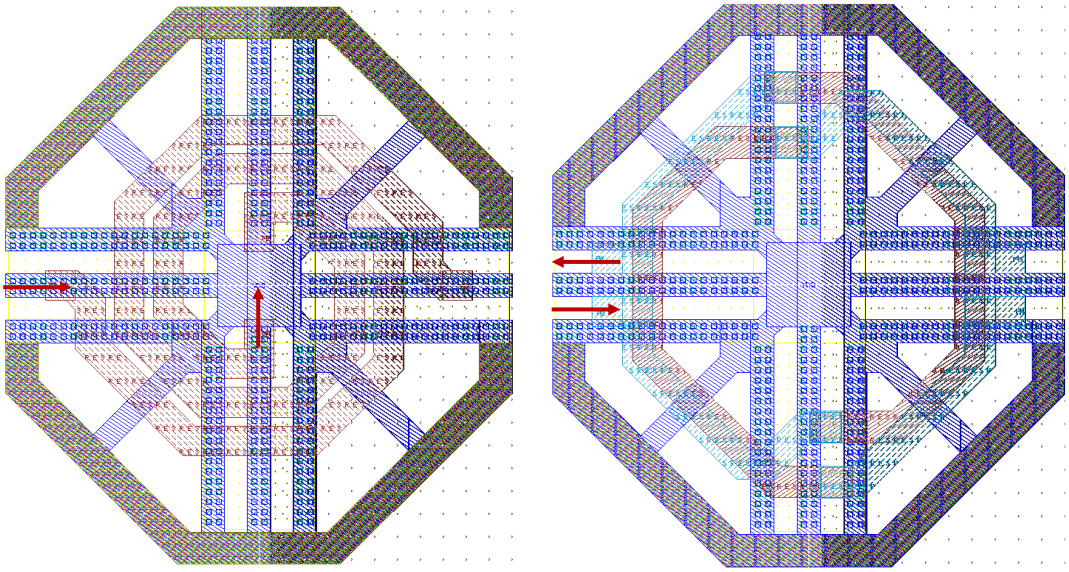

Fig. 5.4 Layout comparison of coupled inductors

For both layouts, the inductor is bottom-shielded with custom metal shielding to prevent eddy-currents and surrounded by isolation walls all modelled with EMX.

### *5.3.3 Quadrature Signal Generation*

To maximize non-overlapping− and thus maximize out-of-band linearity and minimize noise figure as described in chapter 3 − a particular phase relationship is necessary between $I_1^{\pm}$ and $Q_2^{\pm}$ from Fig. 5.3. To ensure such a phase relationship in the routing from quadrature signal generation to the LO buffer, signal for generating fundamental current and signal for generation 2nd harmonic current are generated independently. Differential 5-tap delay lines from Fig 5.1 are sized such that the delay across 4 taps corresponds to 20 GHz while the delay across 2 taps corresponds to 40 GHz. Extra taps provide buffer on both the high frequency and low frequency ends of the tuning range and account for frequency dependent phase shifts between I signals for generating the fundamental and 2nd harmonic currents in the dual-resonant LO buffers.

Additionally, layout considerations also demanded that signals $I_1$,$I_2$,$Q_1$, and $Q_2$ are generated separately. Three sets of routes are critical to LO generation and each comes with critical considerations to ensure proper functionality:

1) from 5-tap delay to vector modulators: imbalance and path-length mismatch in layout affects evenness of tuning range and makes layout difficult, but such an error is not critical
2) from vector modulators to dual-resonant LO buffer: imbalance and path-length mismatch across $I_1$,$I_2$,$Q_1$, and $Q_2$ must be compensated to guarantee

the proper phase relationship for generating quadrature pseudo-non-overlapping pulses

3) from LO buffer to mixer: imbalance and path-length mismatch severely affects pulse shape. Additionally, theory depends on LO buffer seeing a capacitive load, and long routes would present unwanted transmission-line-like-load which distort the wanted signal.

Given the three aforementioned considerations:

1) routing from the LO buffer to mixer must absolutely be minimized
2) imbalance in the routing from delay to vector modulators should be avoided for ease of testing (predicting programming bits for a given $f_{LO}$)
3) routing mismatch from the vector modulators to dual-resonant LO buffer is critical but can be compensated

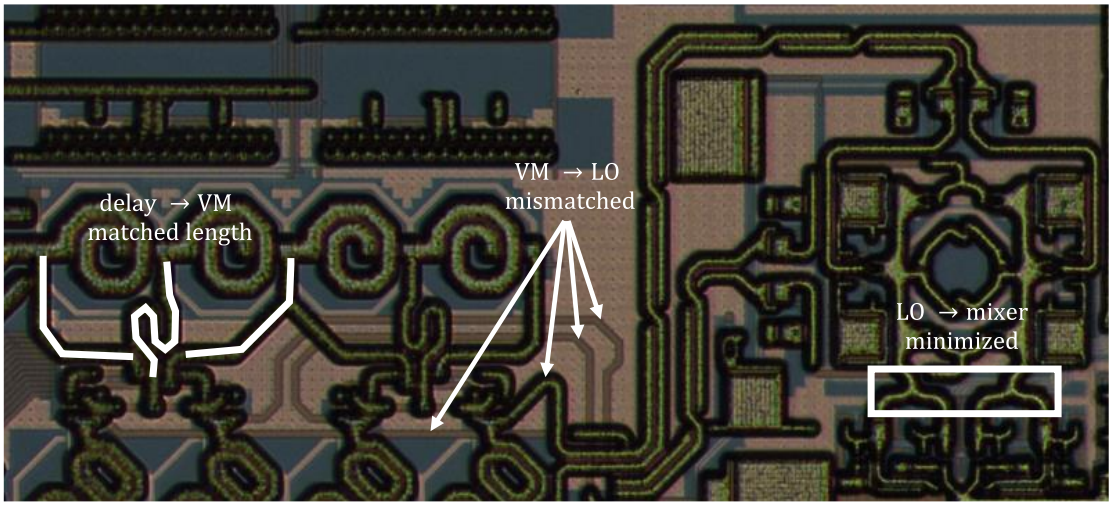


Fig. 5.5 Layout of LO generation chain

As it turns out, to both maintain symmetry of the differential 5-tap transmission lines and minimize routing length in the layout between LO buffers and mixer core transistors, uneven delay across $I_1$,$I_2$,$Q_1$, and $Q_2$ – which each consist of a pair of path-length-matched differential sinusoidal signals– is inevitable. Such uneven signal paths from quadrature generation to LO buffer can be easily visualized in the block diagram in Fig. 5.1 and the layout in Fig. 5.5 and can easily be compensated for by shifting along or interpolating between taps/inputs in the vector modulator. Lastly, because HBT bases load transmission line taps, current also affects capacitive load of each tap in the delay line and must be considered for the proper phase relationship between $I_1$,$I_2$,$Q_1$, and $Q_2$.

## 5.4 HBT N-Path Filter for LNTA Protection

As the name would suggest, N-path filters can be used as tunable filters that replace high-Q SAW filters which sit between the antenna and LNA of a traditional receiver. Since the Q and center frequency of a SAW filter are not tunable but ensure that large out-of-band blockers are suppressed, the benefit of an N-path filter is to likewise protect an LNA but with the added capability of tunable bandwidth and center frequency.

To demonstrate the ability for an N-path filter to protect an LNTA this work also includes a noise-cancelling LNTA and second mixer driven by the same LO as the main mixer which cancels out noise from the main mixer and LO. All noise mechanisms inherent to the main mixer core and from inter-phase jitter and amplitude noise in the LO show up on shared emitter node, $V_X$. As with prior noise-cancellation [28], $V_{RF}$ propagates through the main path and auxiliary path with opposite phases, while the

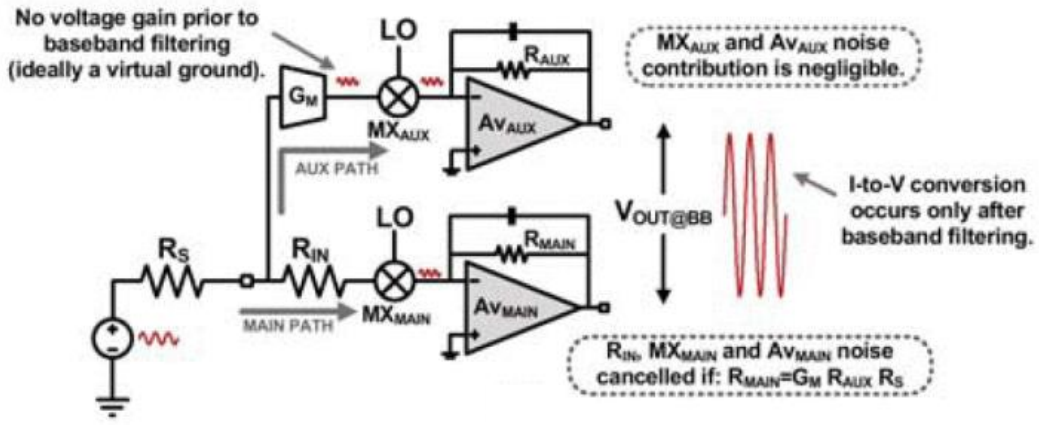


Fig. 5.6 Noise-cancellation theory from [28]

noise generated by the main mixer on $V_X$ propagates in-phase through both paths as seen in Fig. 5.6. $Z_{NC}$ can be tuned such that the total noise of the receiver when both paths are combined comes primarily from the LNTA and residual LO noise that affects the two mixers asymmetrically. Thus, with the HBT N-path filter protecting the LNTA:

1) the linearity of the combined receiver architecture is set by the N-path filter
2) the noise comes primarily from the LNTA (the auxiliary mixer behaves as a non-noise-contributing cascode)

Measurements in section 5.5.3 will show that when the main mixer is turned off, noise will improve slightly because noise from the main path baseband load is eliminated, but linearity degrades to that of an unprotected LNTA. Conversely, when the noise cancellation path is turned off, linearity improves slightly because non-linearity from the LNTA is eliminated, but noise figure degrades significantly because of the aforementioned noise mechanisms.

Given that

1) the two mixers are driven by the same LO
2) the layout of the routing from the LO to the mixers is critical
3) the node $V_X$ of the shared emitter is critical for achieving impedance transparency,

main mixer core devices must be placed as close as possible and noise-cancelling mixer core devices must be placed symmetrically and within close proximity. Layout of symmetry and routing to both mixers is given in Fig. 5.7.

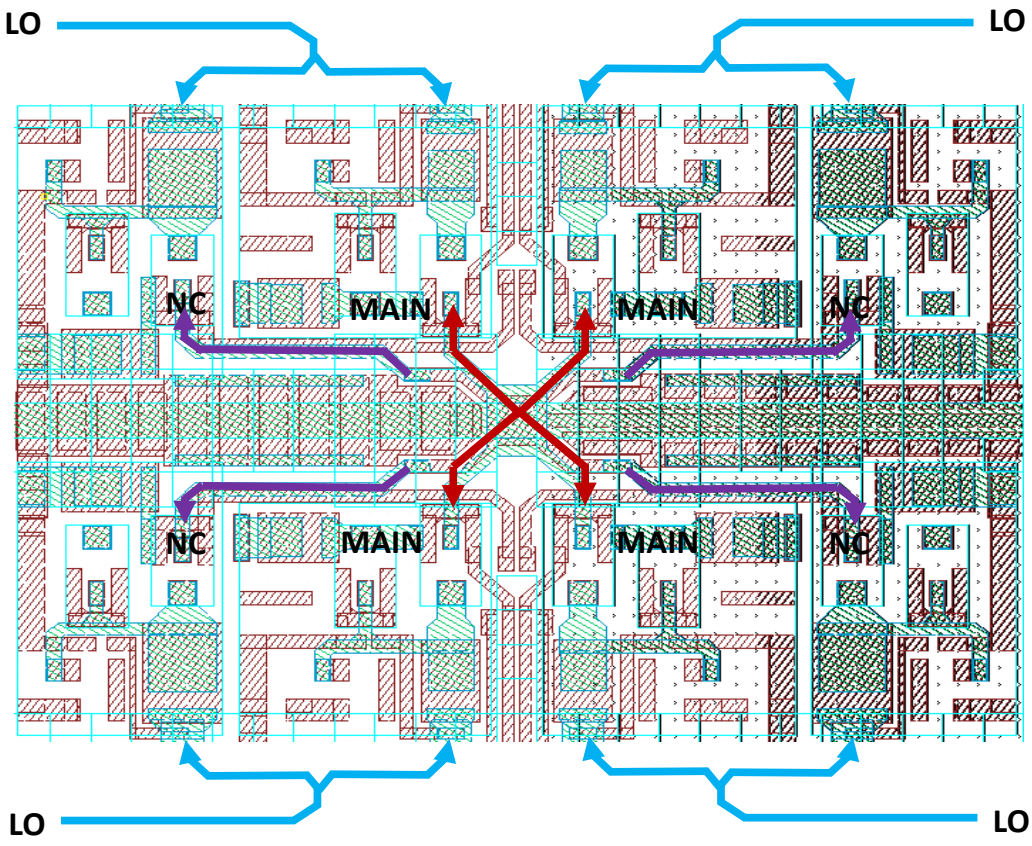


Fig. 5.7 Layout of main and noise-cancelling mixer cores

## 5.5 Measurements Consistent with Theory

The 2nd generation of the HBT-based N-path mixer designed to be tunable from 20-40 GHz was fabricated in GlobalFoundries BiCMOS 8XP with an active area of 2 mm x 1.8 mm, including on-chip baseband amplifers. Die photo is given in Fig. 5.8. All measurements reported in this section have losses associated with the measurement set-up calibrated from 20-40 GHz. Losses up to the probes (GSGSG for LO and GSG for RF) were measured using the Anritsu MA24507 power meter and losses across measurement probes were estimated from data sheets provided by Cascade Microtech.

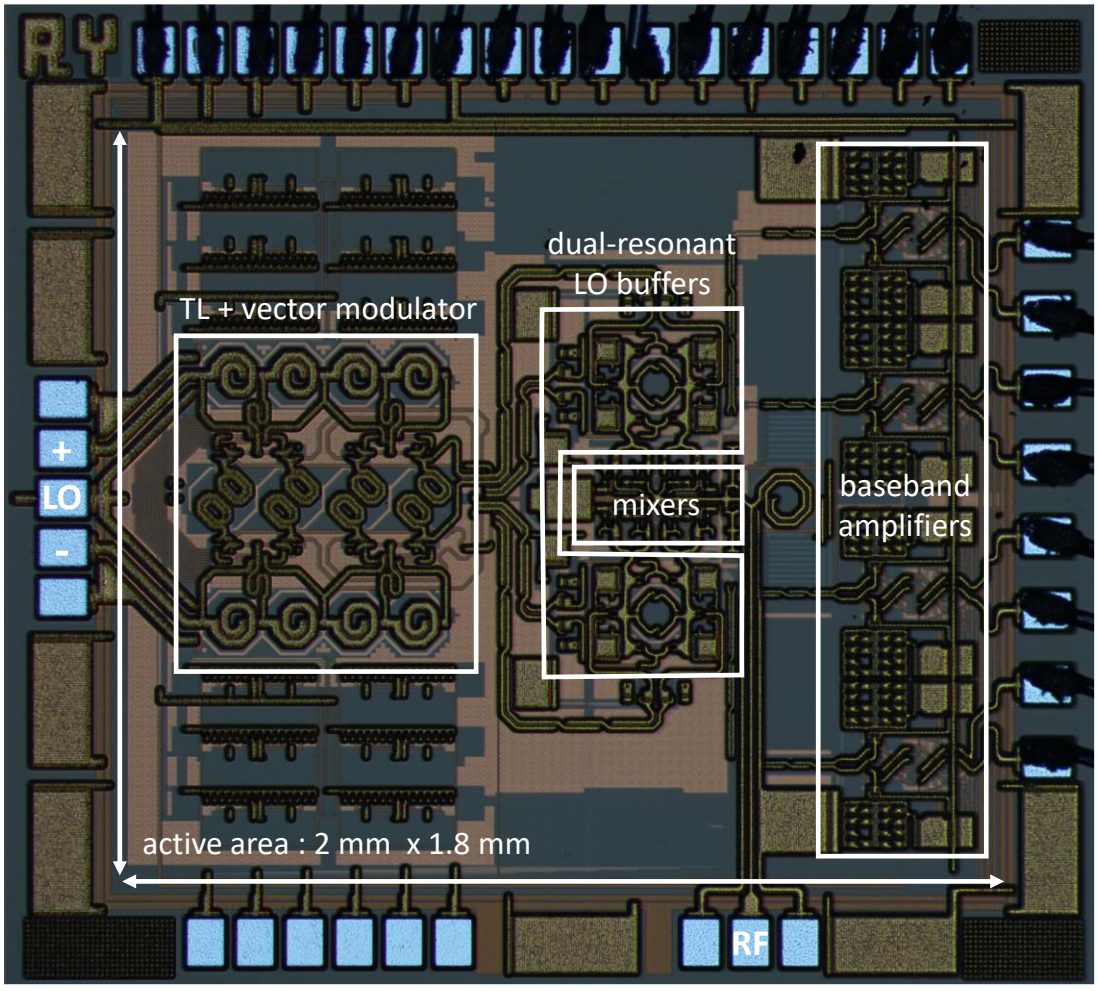


Fig. 5.8 Die photo of 2nd generation HBT N-path receiver

### *5.5.1 Measurement Setup*

Bias and power supplies were brought to PCB through ribbon cable and locally decoupled before bringing DC signals through wirebonds to the chip. A low capacitance surface mount package brings baseband signals to PCB with off-chip baseband amplifiers for generating baseband I/Q for the main and auxiliary paths. Baseband I/Q signals were sampled by a high-speed oscilloscope, Lecroy WaveSurfer 24xs, and scaled/recombined in MATLAB. All measurements were taken with the same gain settings and cable setup so that linearity and noise measurements are consistent. For different power levels, different mV/div settings on the oscilloscope were used. A diagram of the test setup is show in Fig. 5.9.

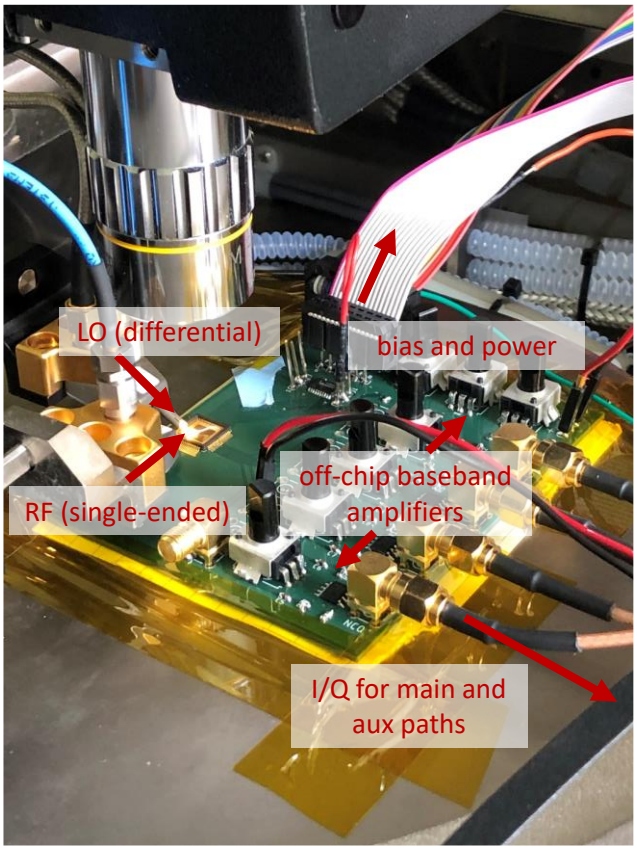


Fig. 5.9 Test setup for 2nd generation HBT N-path receiver

### *5.5.2 Baseline Measurements for Optimal Dynamic Range*

Fig. 5.10 shows a sample measurement of out-of-band linearity at 30 GHz. On the left, B1dB is measured and normalized to the power level when blocker power of a tone with 1 GHz offset is -100 dBm. Up to 5 dBm, there is no compression, and by about 9 dBm, the in-band tone has compressed by 1 dB. On the right, out-of-band IIP3 is given for two out-of-band tones located at 1 GHz and 1.99 GHz offset, dropping an in-band 3rd order term at 10 MHz. The measured OOB IIP3 is about 26 dBm which indicates that the non-linearity in the receiver is not dominated by the 3rd order non-linearities.

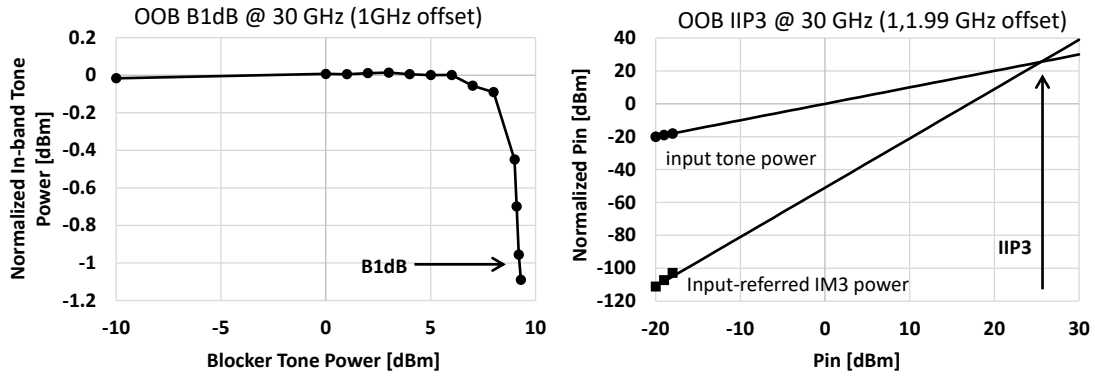


Fig. 5.10 Sample linearity measurements for 2nd gen HBT N-path receiver

Fig. 5.11 shows baseline performance of the proposed receiver when optimizing for blocker-induced DR (defined as OOB B1dB-NF+174) as described in section 3.5.1. B1dB measurements are performed while sweeping both center frequency and offset from center frequency and results are reported for 4 GHz steps with a 4 GHz span around center frequency. Across the tuning range, out-of-band B1dB ranges from 8.2 to 9.4 dBm. In-band, B1dB is dominated by the baseband amplifier. At the same bias settings, NF measured across the entire tuning range ranges from 8.5 to 10.9 dB.

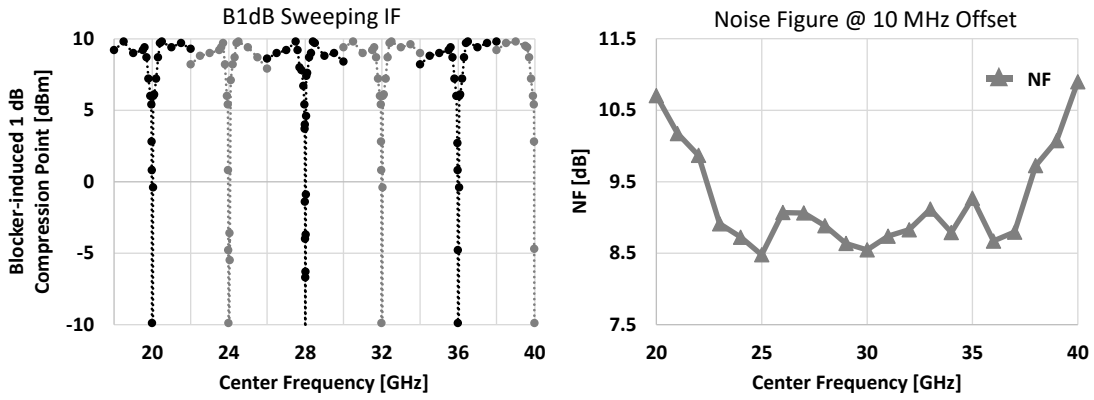


Fig. 5.11 Baseline performance optimizing for DR

### *5.5.3 Efficacy of Proposed Techniques*

Figure 5.12 shows the measured OOB B1dB and NF under 5 conditions to demonstrate the efficacy of the proposed techniques:

1) baseline from Figure 5.8

2) turning off the main mixer

3) turning off noise cancellation

4) turning off the 2$^{nd}$ harmonic in LO

5) optimizing bias for NF.

Turning off the main mixer and measuring the noise-cancellation path alone yields slightly lower NF but significantly worse B1dB (13 dB), indicative of how the main mixer protects the LNTA out-of-band. Turning off the noise cancellation path and measuring the main mixer alone slightly improves OOB B1dB while degrading the NF (by >3 dB), indicative of the efficacy of the noise cancellation technique. Turning off

the 2nd harmonic in the LO generation chain both lowers the OOB B1dB and increases the NF, indicative of how overlap degrades both performance metrics. Additionally, slightly reducing bias current in the mixer core can enhance NF to as low as 7.6 dB but also degrades B1dB by 7dB.

The pie chart in the upper right of Fig. 5.12 shows the power consumption breakdown of the receiver operating at 30 GHz. Total power consumption from 20-40 GHz ranges from 130 to 160 mW where the baseband and noise cancellation path are held constant, but the mixer bias current setting ρ and the power consumption from the DVM in the LO generation chain vary with frequency.

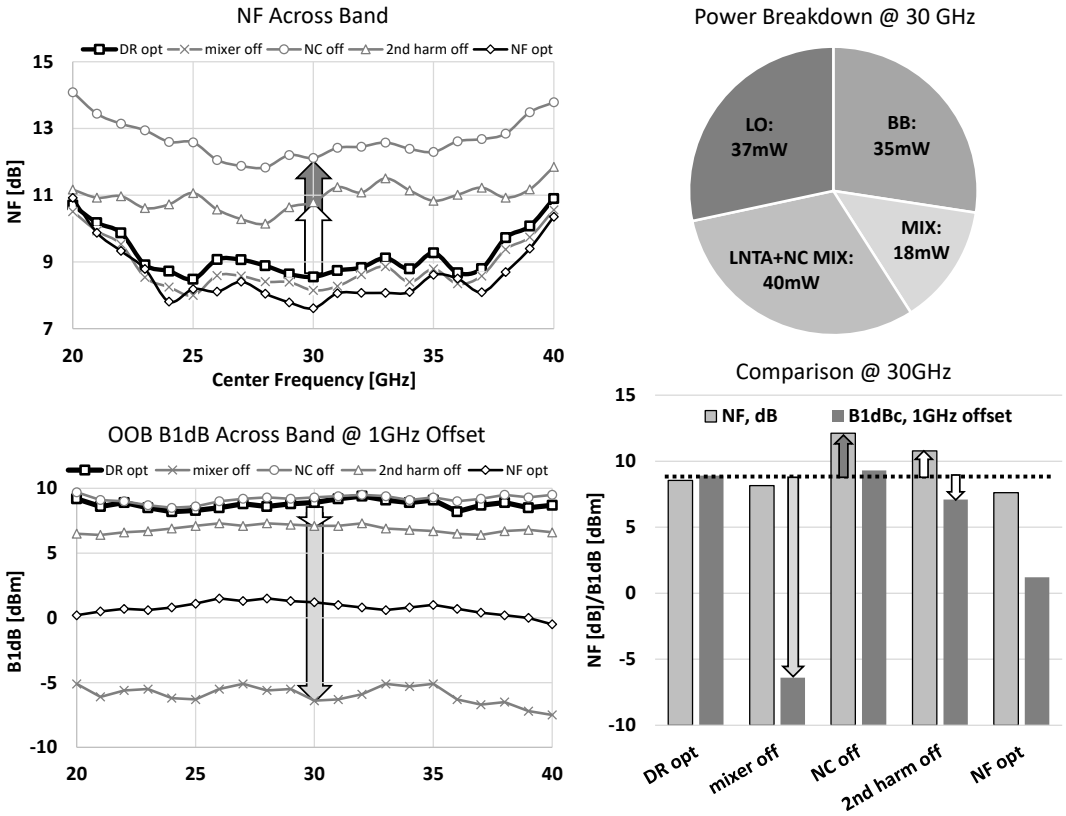


Fig. 5.12 Measurements demonstrate efficacy of proposed techniques

To summarize the performance of the 2nd generation HBT N-path receiver, Table I presents comparison to the state-of-the-art. In comparison to other mixer-first receivers in the 10-50 GHz range, this work achieves comparable or better NF and more than 10 dB larger DR for comparable power.

| | this work | | ESSCIRC '17 [6] | GOMAC '19 [26] | RFIC '20 [21] | RFIC '20 [22] | JSSC '20 [23] | |
|---|---|---|---|---|---|---|---|---|
| | NF-opt | DR-opt | | | | | | |
| RF tuning range | 20-40 | | 0.3-12 | 5-31 | 9-31 | 10-35 | 25-50 | GHz |
| NF | 7.6 | 8.55 | 12.74 | 8 | 12.5→17.5 | 12.5→15.7 | 3.2 → 6.1 | dB |
| OOB B1dB | 1.2 | 8.9 | 10 | -10 | 4 | -3→-5.5* | -7 → -25.5 | dBm |
| OOB B1dB-NF | -6.4 | 0.35 | -2.74 | -18 | -8.5→-13.5 | -15.5→-21.2 * | -10 → -31 | dB |
| DC Power | 118 | 130 | >1000 | 300 | 162 | 60 | 60 | mW |
| LO generation | dual-resonant | | divider | divider | sinusoid | 50% d.c. square | sinusoid | |
| Technology | 130 nm BiCMOS | | 130 nm BiCMOS | 45 nm SOI | 65 nm CMOS | 28 nm CMOS | 45 nm SOI | |

* B1dB estimated from reported P1dB

Table I: Table of comparison for 2nd gen HBT N-path receiver

CHAPTER 6

# THIRD GENERATION HBT N-PATH RECEIVER FOR 60 – 100 GHz

## 6.1 Introduction

One of the key characteristics of 5G NR is the global interest in massive MIMO transceivers utilizing licensed and unlicensed bands above 37 GHz [1,2]. With massive MIMO, while noise averaging across the array reduces the SNR of the system as compared to a single element receiver on the same antenna, matching networks for conventional receiver architectures begin to occupy significant area. Thus, for large arrays, minimizing the per-element area and power consumption becomes integral to designing viable receiver architectures.

As the preceding chapters have described, N-path filters can provide the necessary impedance matching for much less area than traditional receiver architectures because matching is set by the baseband load. While significant power consumption is necessary to drive large, low $R_{on}$ MOS transistors with quadrature phase 25% duty-cycle non-overlapping pulses, overlap-tolerant HBT N-path mixers can maintain high performance with sinusoidal drive, which can be generated with passive EM structures as shown in the block diagram for the 3rd generation HBT N-path receiver in Fig. 6.1.

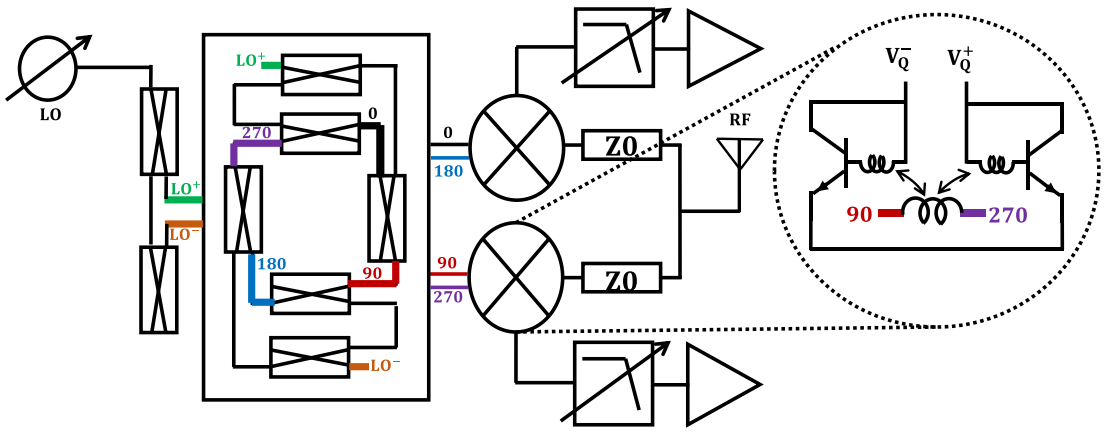


Figure 6.1 Block diagram for 3rd gen HBT N-path receiver

The remainder of this chapter will describe a new mechanism for coupling LO signals to the mixer core with coupled inductors in feedback, an adaptation of the hybrid-coupler-ring for amplitude and phase error correction in the LO, and an adaption of our overlap current choking technique implemented with $\lambda/4$ transmission lines. Following the overview of schematics and techniques we will highlight key simulation results and conclude by looking forward to applying these techniques to novel technologies with even higher $f_T$.

## 6.2 Mixer Core: Coupled Inductor in Feedback

While the emitter-follower described in chapter 5 breaks the trade-off between LO loading and NF from the lumped-element resistor in chapter 4, an even simpler coupling mechanism can be employed when the LO only carries signal at a single frequency.

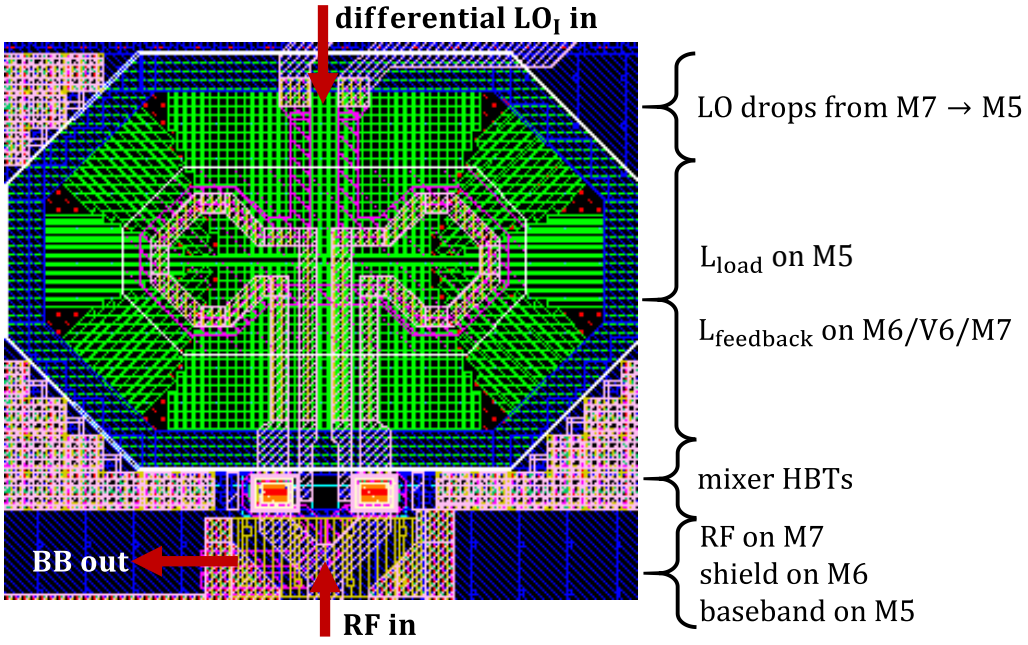


Figure 6.2 Layout of coupled inductor in feedback

Additionally, as will be described in depth in section 6.3, when coupled-line-couplers (CLCs) are loaded by a non-time-varying load, their behavior can be better predicted. Since the emitter-follower and input capacitance to the mixer presents a time-varying impedance, an inductor presents a more stable load across switching. Thus, the load to the coupled-line-coupler is an inductor and signal current from that load inductor is coupled to another inductor in feedback from the HBT's collector to base as shown in Fig. 6.2. From a signal-impedance perspective, the inductor presents a large impedance, but from a noise perspective, the resistance of concern is the parasitic resistance across the wire. To increase the Q, via stitching between 2 layers of metal like that described in section 5.3.2 can be employed to further reduce the effective $R_{FB}$ and $\chi$. Lastly, because mixer core devices can be grouped in differential pairs, coupler load inductance can be differential and bypass shunting to ground.

## 6.3 LO Generation: Coupled-Line Couplers with Error Correction

Because unwanted image signal can mix with noise and severely degrade the noise performance of a receiver, significant effort has been dedicated to attaining quadrature mixing with quadrature LO. Classic methods for generating quadrature include quadrature voltage-controlled oscillators (QVCOs), Johnson counter dividers, RC poly-phase filters (RC-PPFs), and quadrature hybrid couplers. However, each comes with its limitations. QVCOs depend on tunable capacitance to establish its limited tuning range; Johnson counter dividers require an input frequency of 2x the desired frequency; RC-PPFs are comprised of resistors which are lossy and suffer from device variation; and

quadrature hybrid couplers are physically large because branches are sized $\lambda/4$. At mm-wave, hybrid-couplers can become compact, but due to the $\lambda/4$ being defined for a specific frequency, cannot maintain amplitude and phase balance over a wide frequency range. The s-parameter matrix for a (CLC) at the frequency where there is no reflected power at the input is given by

$$S = \begin{bmatrix} 0 & -j\beta & \alpha & 0 \\ -j\beta & 0 & 0 & \alpha \\ \alpha & 0 & 0 & -j\beta \\ 0 & \alpha & -j\beta & 0 \end{bmatrix} \tag{6.1}$$

where $\alpha = k$, the coupling coefficient from the input the coupled port and $\beta = \sqrt{1 - k^2}$ for the signal which propagates to the through port. At $f_{center}$, $\alpha = \beta$ and $k = 1/\sqrt{2}$ ensuring that $\Gamma_S = (\alpha^2 - \beta^2)\Gamma_L = 0$, satisfying our assumption.

Quadrature signal generation with insufficient amplitude and phase balance both limits useable frequency range and significantly affects performance through poor image rejection, which is only made worse by errors in differential signals propagating through the hybrid couplers. For differential phase error, $\phi$, and amplitude error, $\epsilon$, coming from imbalanced parasitics, routing in differential baluns, and normalizing to one signal ($1\angle 0$), the differential signal can be described as $-(1+\epsilon)\angle\phi$. For an ideal CLC operating at $f_{center}$ amplitude, phase errors would propagate through and degrade the image rejection.

It is with all this in mind that [29] demonstrates a technique for amplitude and phase correction using a ring of CLCs. Each output node is comprised of signal from the coupled and through ports of CLCs with quadrature-phase shifted signal on their input ports. The transfer function describing the relationship between signals on input

ports and output nodes is

$$\begin{bmatrix} V_{o1} \\ V_{o2} \\ V_{o3} \\ V_{o4} \end{bmatrix} = \begin{bmatrix} \alpha & -j\beta & 0 & 0 \\ 0 & \alpha & -j\beta & 0 \\ 0 & 0 & \alpha & -j\beta \\ -j\beta & 0 & 0 & \alpha \end{bmatrix} \begin{bmatrix} V_{i1} \\ V_{i2} \\ V_{i3} \\ V_{i4} \end{bmatrix} \tag{6.2}$$

and the corresponding schematic is given in Fig. 6.3.

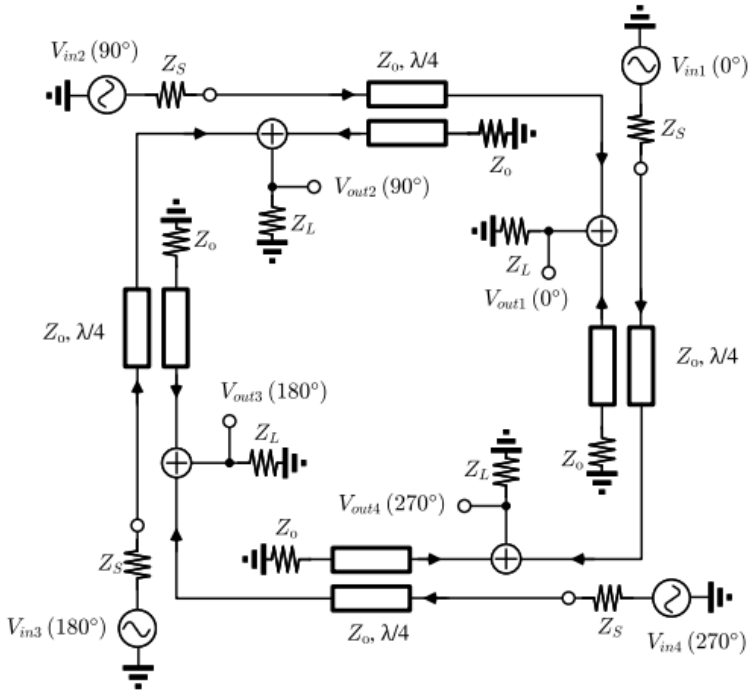


Figure 6.3 Schematic of quadrature-hybrid ring [29]

It is shown in [29] that quadrature signals can be broken down into 4 modes similar to the common mode and differential mode for differential circuits:

1) Quadrature counterclockwise
2) Quadrature clockwise
3) Collinear differential
4) Collinear in-phase

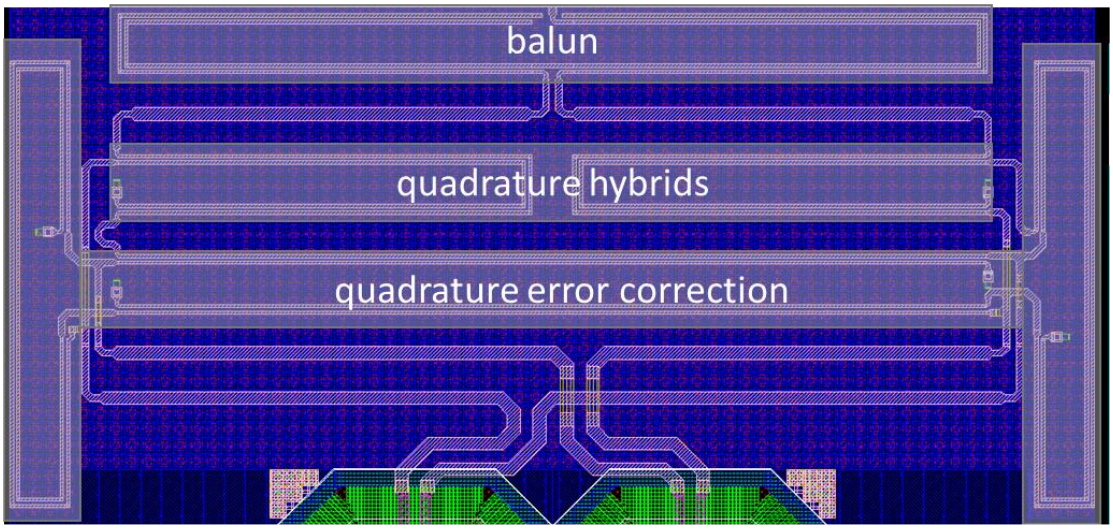


Figure 6.4 Layout of LO generation chain

The quadrature-hybrid ring is also shown to pass quadrature counterclockwise signals, block quadrature clockwise signals, and attenuate both collinear signals, thereby improving the amplitude and phase match. An EM structure comprised of a marchand balun, a pair of CLCs for quadrature generation, a quadrature hybrid ring for error correction, and routing to the inductor loads from Fig 6.2 is shown in Fig. 6.4.

## 6.4 Overlap Current Choking with $\lambda/4$ Transmission Lines

While LO overlap itself does not degrade HBT N-path performance, the slow switching from pure sinusoidal drive degrades performance as described in section 3.5.2. To counter this, we group our 4-phase mixer into a pair of differential mixers and place $\lambda/4$ transmission lines in series such that the impedance seen from one differential pair's emitter to the RF port is inverted by $\lambda/4$. During overlap, because the mixer switch driven by the quadrature-phase shifted LO presents a impedance inversion, no low-

impedance path is presented until the differential LO causes its mixer switch impedance to drop. Such behavior can be expected until the inversion causes the impedance presented by the quadrature-phase shifted mixer to become smaller.

## 6.5 Simulations Consistent with Theory

Combining all the aforementioned techniques, we arrive at the chip layout shown in Fig. 6.5 which utilizes 0.72 $mm^2$, including baseband amplifiers with tunable bank of feedback resistance and shunt capacitance. For simulations, all EM structures have been E&M-modelled together as a continuous signal path rather than individual blocks. An ocean of M1 shield is used to model the ground return path with ground return path ports placed on the M1 shield directly beneath the LO, RF, and BB ports.

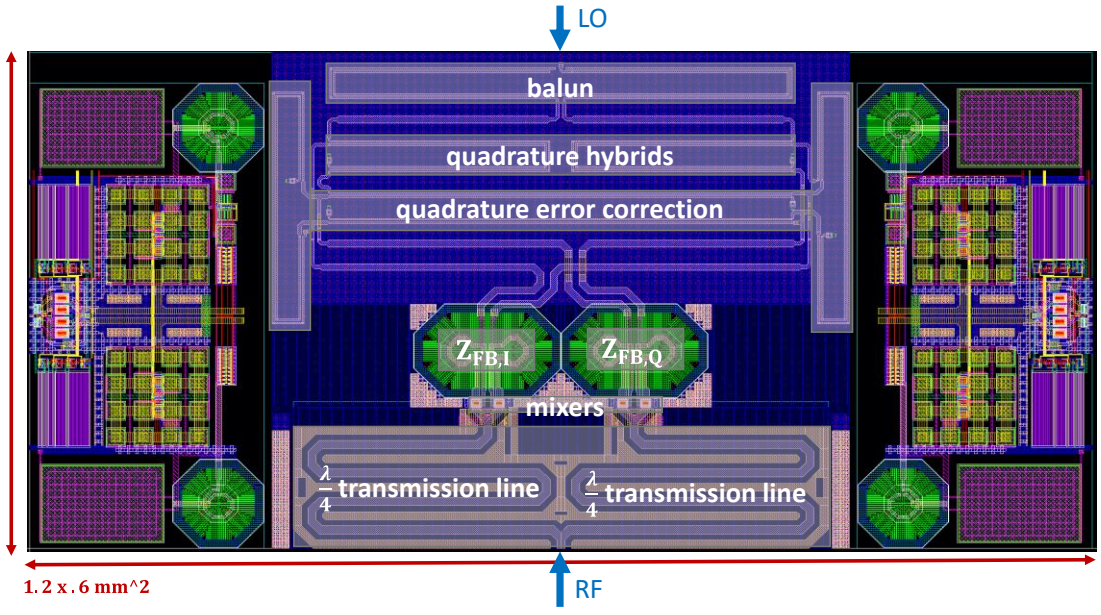


Figure 6.5 Layout of 3rd gen HBT N-path receiver

### *6.5.1 Simulated Quadrature Phase LO*

To verify the technique proposed in [29], we simulated the phase balance from a single-ended LO to ports located at the edge of the coupled-inductor load. Including the loading of an HBT N-path mixer in operation, the simulation results in Fig. 6.6 indicate that less than 1° quadrature phase mismatch can be ensured from 60 – 100 GHz with less than 3° error down to 50 GHz and 10° error down to 40 GHz. Amplitude balance (not shown) is within 1 dB from 60-100 GHz.

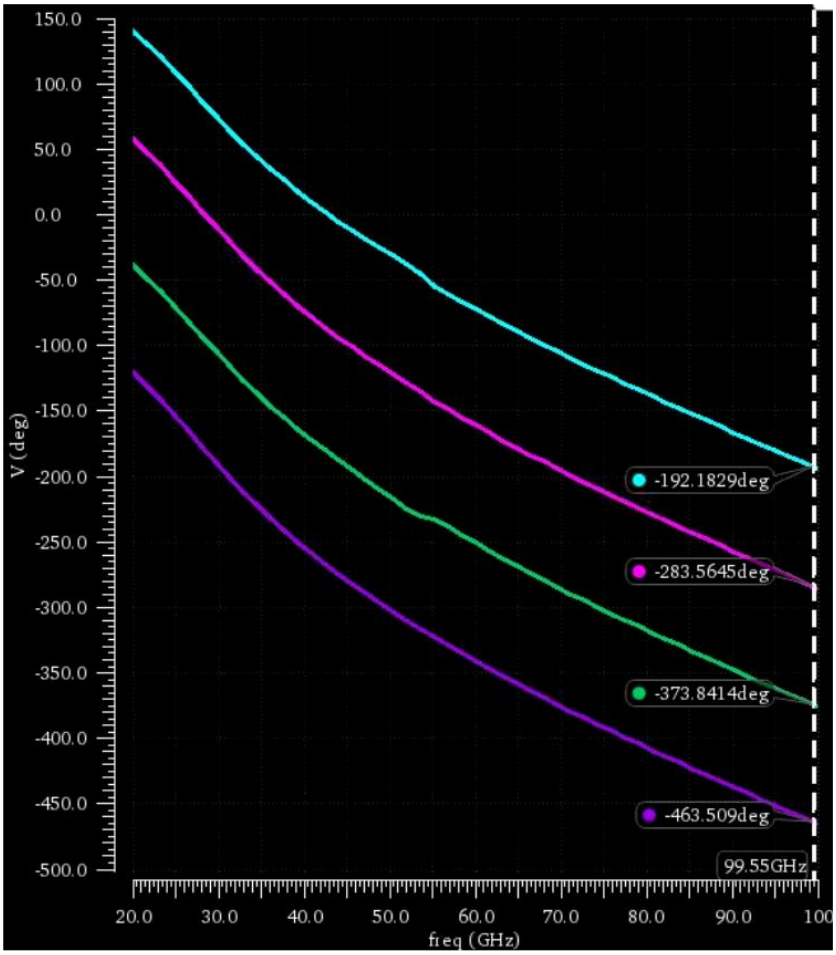


Figure 6.6 Phase at differential inductor load across tuning range

### 6.5.2 *Simulated Noise Figure*

With

1) no re-timing in the LO generation structure
2) overlap current choked by transmission lines
3) baseband amplifiers with resistor in feedback for setting the impedance match,

noise primarily comes from the mixer core and baseband current sources with minimal noise from the series resistance of the inductor placed in feedback for impedance transparency. With 0 dBm input power to the LO input of the marchand balun across the entire tuning range from 50-100 GHz as compared to the 10 dBm input power utilized by the active LO generation chain of the 2nd generation chip in chapter 5, mixers are switched with $V_{LO}$ of approximately 300 mV. With a center frequency of 80 GHz, the simulated noise figure from 50-100 GHz is given in Fig. 6.7 to range from 8 to 10.4

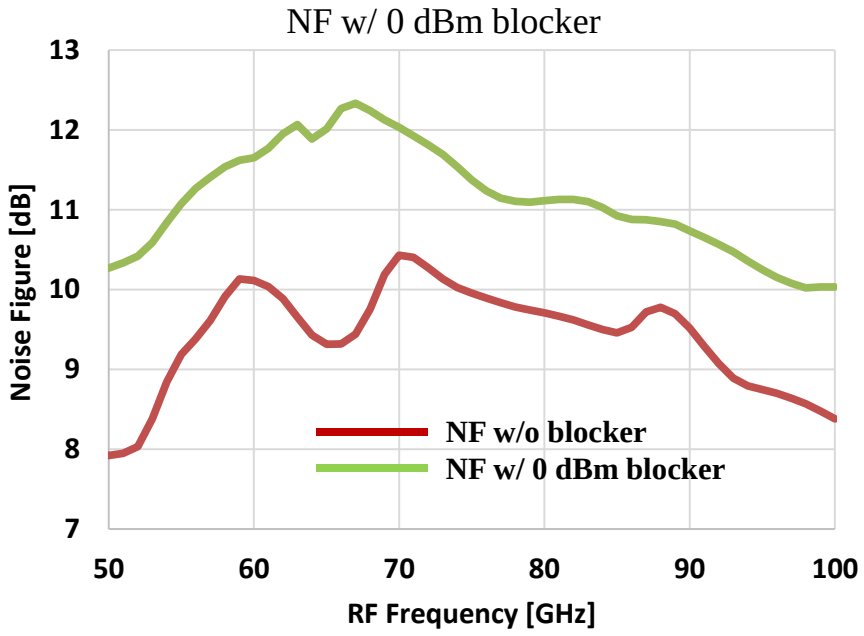


Figure 6.7 NF for 3rd gen HBT N-path receiver

dB. Assuming an additional 1 dB of loss from simulation to measurement, this is consistent with measurements in chapter 5 under the condition where 2nd harmonic was turned off. Note that below 50 GHz the phase and amplitude imbalance begins to severely degrade NF and above 100 GHz, the quadrature phase error quickly collapses such that quadrature phase-shifted signals are coincident.

In chapters 4 and 5, biasing resistors in the LO buffers present bias noise that mixes with even-order harmonics to degrade NF in the presence of a blocker. For the proposed receiver architecture, because the LO generation chain is entirely passive and un-biased, the 0 dBm blocker NF degradation ranges from 1 dB to 2.5 dB across the full tuning range, giving NF that ranges from 10 to 12.2 dB.

### *6.5.3 Simulated Out-of-Band Linearity*

Lastly, with regard to linearity, simulation at 100 GHz in Fig. 6.8 shows OOB B1dB of 5.8 dBm. For a $\rho$ = 0.087 which predicts approximately 9 dBm, the 3 dBm degradation

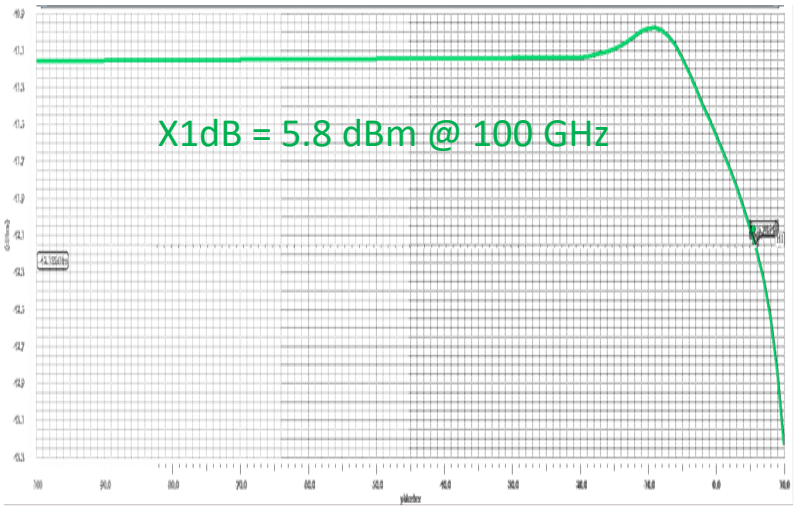


Figure 6.8 OOB B1dB for 3rd gen HBT N-path receiver @ 100 GHz

is consistent with our analysis from section 3.5.2 where compression occurs because of the effectively long duration of crossover. Considering that the full swing of the LO is approximately 300 mV, it is not surprising that the effective $V_{LO}$ would drop low enough to degrade linearity. Considering that the simulated DR at 100 GHz is 5.8-8.4 = -2.6 dB and can be estimated to be closer to -4 dB for real-life measurement, this dynamic range is still better than or comparable to other state-of-the-art receivers at a fraction of the operating frequency.

## 6.6 Future Directions

As we look forward to future work with the 3rd generation HBT-based N-path receiver, two main directions come to mind. First, higher frequency N-path receivers can be implemented in novel III-V technologies. Second, by reducing the area of a single receiver by eliminating various area-hungry, but not critical elements, both the low-area and low-power demands of massive MIMO receivers can be satisfied.

### *6.6.1 Novel Technology Implementations*

Given the extremely high dynamic range, extremely low 0 dBm blocker NF degradation, and the entirely passive LO generation chain, such a topology becomes a viable option for use in mm-wave massive MIMO receiver arrays. Additionally, because the entire receiver architecture:

1) only makes use of 4 transistors which comprise the mixer core

2) has no need for any digital tuning except in the baseband (which would require integrated MOS for digital circuitry)
3) can be routed with only 2 RF metals (or 1 with air-bridges for crossover points)
4) is self-biased by inductors in feedback

the 3rd generation of the HBT-base N-path receiver implemented with novel InP [25] or other high $f_T$ technology could enable highly linear, moderate noise, and low power receiver architectures beyond 100 GHz.

### *6.6.2 Viable Massive MIMO Receiver Block*

Note also that if no series transmission lines are placed between the differential mixer pairs, area could be significantly reduced and tuning range limitations from the transmission lines would be eliminated. In this case, degradations to noise figure and

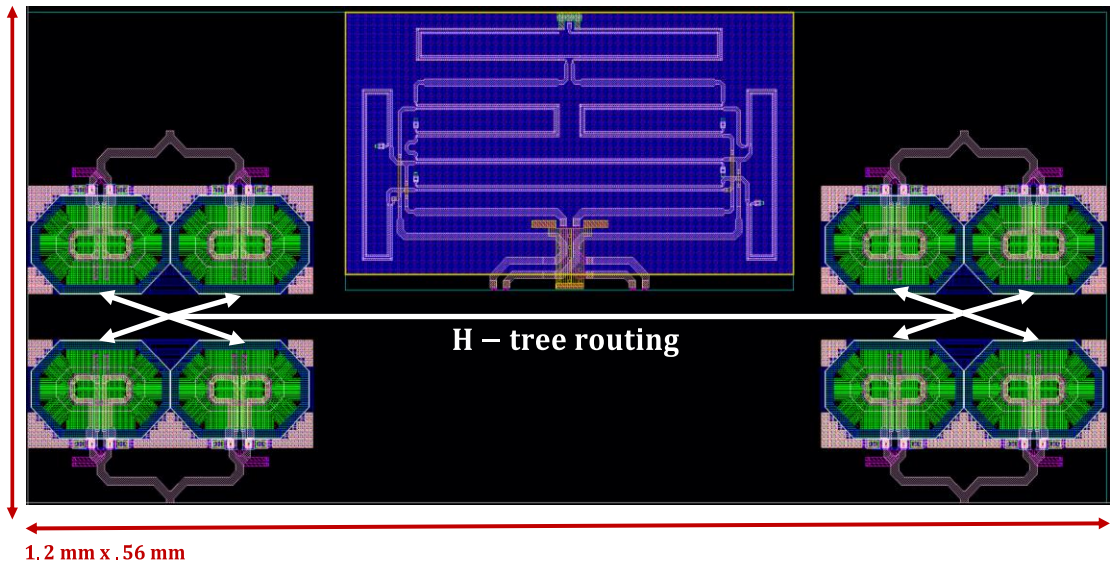


Figure 6.9 Proposed layout for 4-element HBT N-path receiver array

linearity would be incurred to expand the tuning range to that limited by the quadrature hybrid ring's error correction and area would instead be dominated by the coupling inductors. Further area reduction could be attained for receiver arrays where the LO generation structure is shared among M N-path receivers and even further reduction can be attained if baseband amplifier tuning ranges were reduced from 4-bits. As a thought experiment, with some creative H-tree like routing, no series transmission lines, and baseband amplifiers removed as in Fig. 6.9, the total area of a 4-element array sharing a single LO generation chain would take approximately the same area as the receiver architecture in Fig 6.5. Such a receiver would be capable of achieving high blocker tolerance, moderate NF, and all the reconfigurability of N-path receivers with low power and low area, making the 3$^{rd}$ generation HBT-base N-path receiver a viable option for utilization in massive MIMO receivers.

CHAPTER 7

# HBT N-PATH PRACTICAL DESIGN GUIDE

## 7.1 Introduction

Throughout multiple tapeouts we have acquired much wisdom and skill in the art of millimeter wave layout. “All models are wrong, but some are useful” is generally true for circuit design, but at millimeter wave frequencies, careful layout and the accompanying E&M modelling can become critical. In this concluding chapter we will describe two layout techniques utilized in all three generations of the HBT-base N-path receiver or otherwise learned along the way and then conclude by synthesizing this dissertation into a step-by-step guide for the HBT-based N-path receiver designer.

## 7.2 Transistor Routing for optimal $f_T$

One of the key limiters of the performance of HBT N-path mixers is $f_T$ because this cutoff frequency sets the onset of $Z_{sh}$ effects. As shown in Fig 3.7, $Z_{sh}$ sets the upper bound for the reachable impedance of the RF port and thus must be maximized. From a device perspective, the maximum $f_T$ is set by the physics of electron transport; however, layout parasitics can significantly affect both $f_T$ and $f_{max}$. The expression for $f_T$

$$f_T = \left[2\pi(\tau_E + \tau_B + \tau_C + \frac{nkT}{qI_C}(C_{CE} + C_{BC}) + C_{BC}(R_E + R_C)\right]^{-1} \tag{7.1}$$

indicates that:

1) $C_{BC}$ must be minimized
2) $C_{BE}$ can affect $f_T$ but less than $C_{BC}$
3) $C_{CE}$ has no effect on $f_T$
4) $R_E$ & $R_C$ can further reduce the effect of $C_{BC}$ when minimized

Given these observations, great care must be taken to keep routing capacitance on $C_{BC}$ to a minimum. Because most RF and millimeter wave signals need to route up to the top level metals, parasitic extraction is performed on transistors with vias and metal up to pins on top level metals. This technique also reduces layout effort for each individual transistor since separate cellviews can be made for transistor layout variations that will be repeatedly reused.

Because $C_{CE}$ has no effect on $f_T$ and $C_{BE}$ should also be minimized, we route collector and emitter in one direction and base away in the opposite direction. Additionally, as we move up layer by layer toward the thick RF metals, we immediately start moving the vias and metals for routing the collector away from the base stack. With CBEBC structure to minimize $R_C$ and $R_B$, the sample layout for routing up from a transistor is given in Fig. 7.1. In this sample layout metals 1- 5 are standard routing layers and layers 6-7 are 1.52 mm and 4 mm thick, respectively. Base routes down and stitches with vias from M1-M5 while collector routes up and progressively moves outward from the base which is constrained by DRC with the emitter stack.

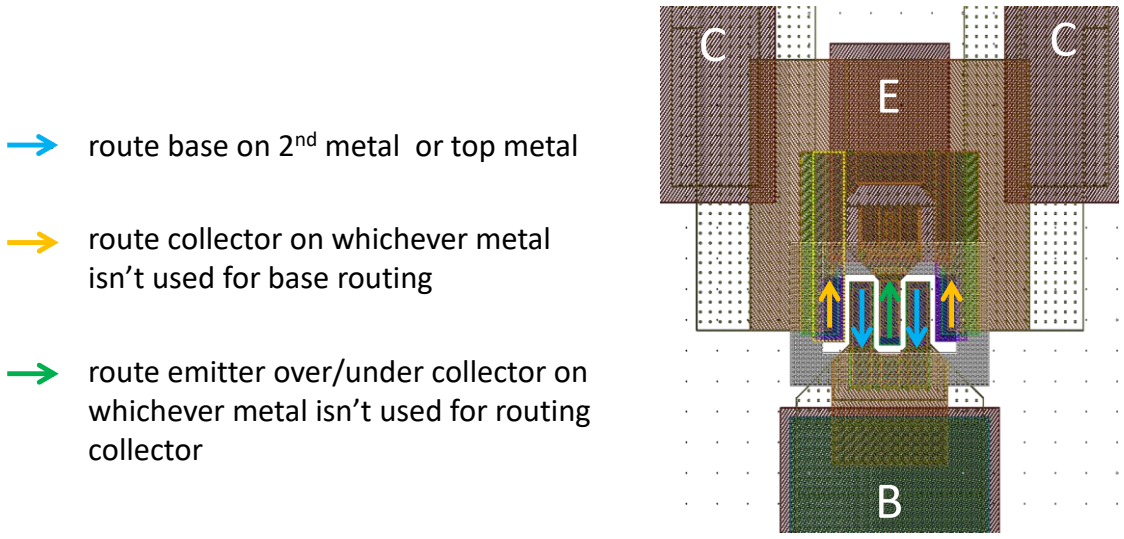


Figure 7.1 Layout of transistor with minimal parasitics

To then make contact with the "rest of the world," base, collector, and emitter must all be accessible by RF routing metals. Because $C_{CE}$ is inconsequential, the routing of collector and emitter is primarily determined by DRC and the critical-ness of the signal being routed. Generally, for long routes carrying critical RF signal (except for those where MIM cap dendrite formation rules discourage the use of the top routing metal), the top level metal should be used to minimize loss and transmission line modelling should be used. Fig. 7.2. shows the layout conventions we used in two cases:

1) (left) collector carries the more critical signal so top metal is used for collector and 2nd metal is used for emitter. Because the collector metal stack must include 2nd metal to reach the top metal, a cutout in the 2nd metal is made for the entry/exit point for the emitter routing. Again, because $C_{CE}$ is inconsequential, minimum spacing (or close to) ensures that routing metal for both the collector and emitter on 2nd metal is as wide as possible.
2) (right) emitter carries the more critical signal so 2nd metal is used for collector and top metal is used for emitter. Because the collector routing does not include the top metal, routing for the emitter can run across the collector and the collector signal can route upward and out or across on 2nd metal.

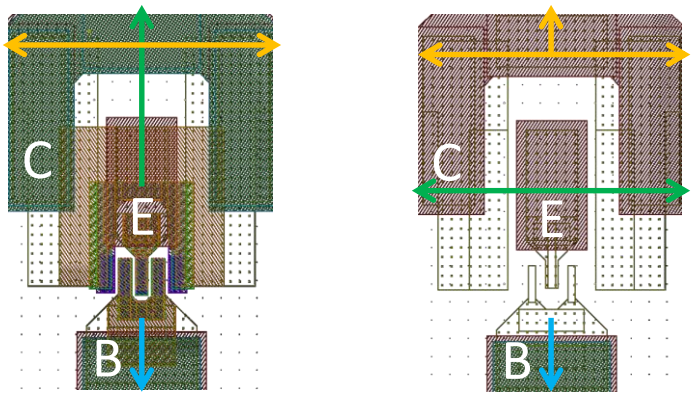


Figure 7.2 Layout of transistor with different routing orientations

## 7.3 Ground Ocean Blocks

With potentially high current producing local heat spots around transistors, ground connection to substrate provides a path for heat to dissipate. Because these local heat spots can reach high enough temperatures for thermal runaway if not carefully considered, transistors pulling large currents should be surrounded by an ocean of ground plane from lower level routing metals down to substrate. Additionally, because millimeter wave routing must be CPW or microstrip modelled, ground plane must surround and run underneath routing paths.

### *7.3.1 The Basic Process*

Apart from DRC this would mean that sheets of solid, uninterrupted metal and via grids would do the trick; however, DRC rules significantly constrain and complicate the implementation of these ground oceans. To streamline this process, we suggest the following process:

1) Determine the maximum current that is expected in the high-current transistors
2) Based on the assumption of current density approximately 1 mA/μm, determine the width of metal needed to carry the signal safely
3) With the established width, determine what the minimum spacing needs to be in order to satisfy DRC at the top level (note that for wider metals on any layer there are different DRC rules for different widths of metal)
4) With metal spacing established, create a subblock of layout stacking up from

substrate to top metal (or lower metals for layout block variations) such that if blocks were tessellated, DRC would not be violated. Squares of 10 µm x 10 µm recommended

5) Place a P&R boundary around your sub-block so that quick-align may be used to quickly copy and snap blocks by edge or corners
6) If desired, create larger blocks for filling large chunks of ocean or create variations with different layers.

A sample layout stack employing this process is given in Fig. 7.3 with a metal stack running from substrate through substrate contacts on the right then going up one layer of via and metal progressing to the left. Note that due to DRC rules related to the density of vias connecting metal 1 to metal 2 over substrate contacts, the use of ground ocean layout blocks bypasses violating this DRC error every time auto-via-generation is used. Additionally, while the auto-via tool can be useful, DRC violations can run rampant and take longer to debug than tessellating ground ocean blocks.

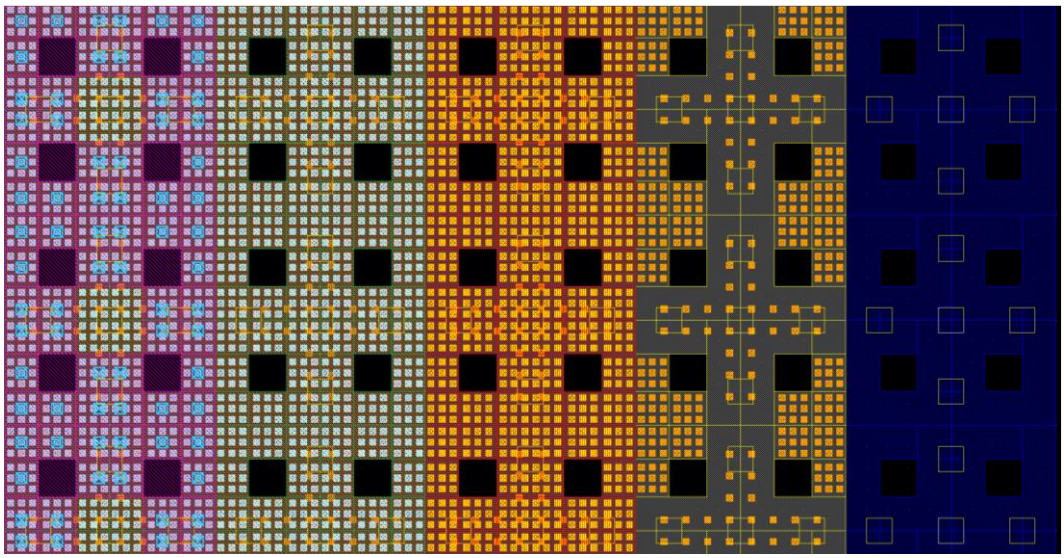

Figure 7.3 Layout of ground ocean from substrate up

### *7.3.2 Ground Ocean for Low Resistance Shield*

Figure 7.3 assumes that RF routing is running over a ground ocean that runs from and fills substrate up through metal 5. However, in practice, there will often be signals that may run underneath the ground shield such as digital blocks or bias/supply wires. In that case, the ground ocean should be used to create a shield that ensures there is still a low resistance path from the ground shield to the substrate. Fig. 7.4 shows the cross-section of a layout of ground ocean surrounding a cavity where digital circuits and a power supply are completely isolated from the RF signal on the top metal. Ground ocean extended outward on the left and right provides the low-resistance path from the shield to the substrate which carries the well-defined "ground" signal. Also, note that because the purpose of a ground shield is to provide the path for return current, the shield must be uninterrupted or else return current will have to travel down the via stack and come back up.

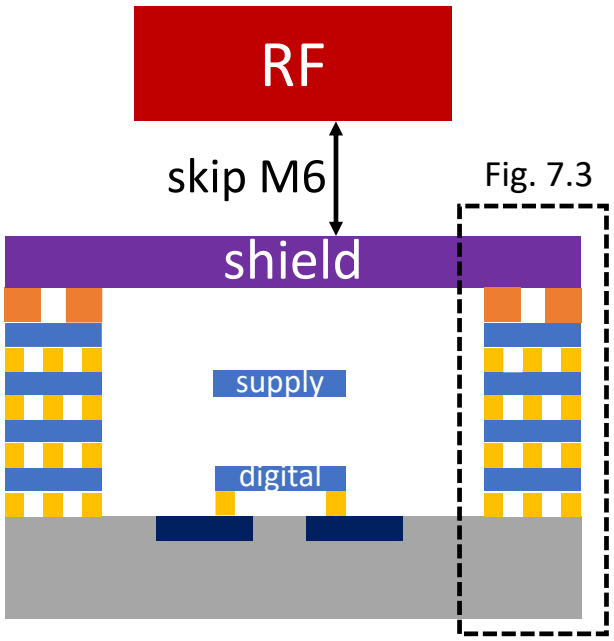


Figure 7.4 Layout cross-section with digital/supply shield and ground ocean

### *7.3.3 Considerations for E&M Modelling*

It is almost guaranteed that for such a ground shield to be useful for RF routing that the interaction of the RF signal and the shield must be modelled as a transmission line. However, since E&M solvers create meshes over which to run, and slots like those in Fig 7.3 require finer meshes, it behooves the designer run E&M modelling tools on solid, uninterrupted ground shields. If an ocean were used even without any supply or digital blocks underneath, the layout for E&M modelling should still only use a solid sheet of the uppermost metal. For this model to be useful, two conditions must hold:

1) the ground shield on this uppermost metal must behave as the ground in the substrate would. This is a valid assumption if the ground ocean is used anywhere and everywhere digital blocks and supply wires do not run.
2) ground ports should be placed on the edge of the modelled region with ports for ground placed directly underneath ports for the input and output of the signal as depicted in Fig. 7.5.

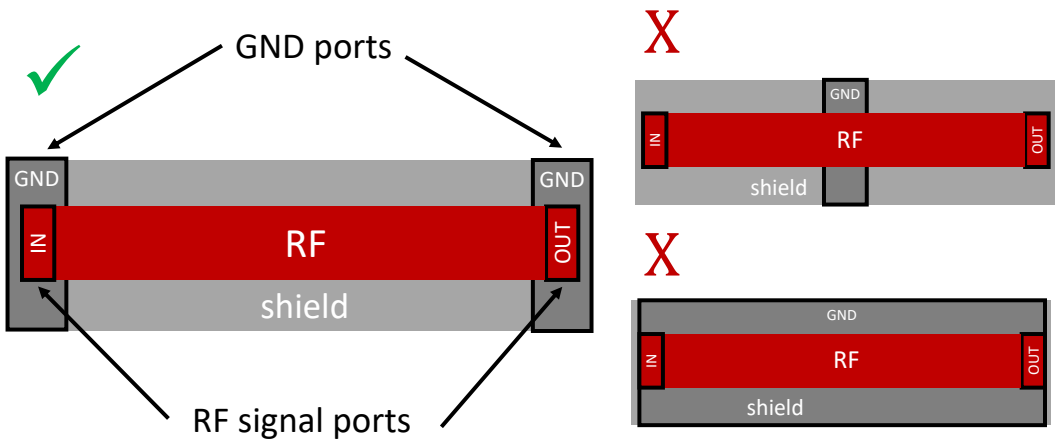


Figure 7.5 Proper pin placement for E&M model of transmission lines

## 7.4 HBT-based N-path Design Guide

### *7.4.1 Summary of HBT-based N-path Design Iterations*

In the first generation HBT-based N-path receiver, we demonstrated that impedance transparency was possible with higher $f_T$ bipolar-style transistors, but such a demonstration utilized a large lumped-element resistor in feedback which exhibited a trade-off between loading on the LO and noise figure. Following suit with the traditional Johnson-counter used to generate LO for traditional MOS implementations of N-path receivers, the first generation HBT-based N-path receiver LO used emitter-coupled-logic for high-speed, fully-wideband, 25% duty-cycle non-overlapping digital pulse generation.

While the first generation HBT-based N-path receiver was able to demonstrate impedance transparency and high out-of-band linearity, it suffered from a high noise figure from $R_{FB}$ and high power consumption from generating quadrature-phase non-overlapping pulses. In the second-generation design, we introduced three techniques which addressed both the high noise and high power. An LPTV emitter follower in feedback instead of an LTI resistor broke the NF versus LO loading trade-off and introduced a method for attaining impedance transparency while presenting both a small noise resistance and a large input impedance to the LO buffer. Additionally, because generating high-bandwidth digital pulses at mm-wave frequencies is both a waste of power and unnecessary for sufficient switching, the second-generation LO generation chain introduced a dual-resonant pseudo-non-overlapping pulse generation technique. Finally, because this LO generation does not include re-timing to reduce the noise

contribution of the LO generation circuitry, a noise-cancellation technique was employed to cancel noise from the LO generation. Measurements of the second-generation receiver demonstrated the efficacy of the HBT-based N-path filter as protection for an LNTA.

Lastly, while the second generation HBT-based N-path receiver demonstrated outstanding dynamic range over an octave tuning range for moderately low power, it did not completely make use of the high $f_T$ that HBTs are known for. In the third-generation HBT-based N-path receiver, we demonstrate an even lower-power technique for LO generation accepting that even dual-resonant LO generation at 100 GHz presents a challenge. We also demonstrate a 3rd impedance-type in feedback for impedance transparency: coupled inductors can be used for coupling pure sinusoids with minimal area and ease of layout (there is no dendrite formation risk as there is for MIM caps in AC-coupling from the 1st and 2nd generation layouts). From our theory and analysis as well as in observations of the second-generation design, overlap due to sinusoidal drive only slightly increases noise figure and reduces out-of-band linearity. By saving the power and area needed for injecting the 2nd harmonic for LO overlap reduction, the third generation simulates 8-10 dB noise figure with 6 dBm out-of-band B1dB from 50-100 GHz. Combining the reduced area, low power, still excellent out-of-band linearity, and moderate noise figure, the 3rd generation of the HBT-based N-path receiver also becomes a viable option for massive MIMO arrays for next-generation communications systems.

Table II summarizes the performance metrics for each of the three generations of the HBT-based N-path receiver and generalizes trends and limitations of each.

| | | 1st Gen | 2nd Gen | | 3rd Gen | |
|---|---|---|---|---|---|---|
| | | | NF-opt | DR-opt | | |
| Measured | RF tuning range | 0.3-12 | 20-40 | | 50-100 | GHz |
| | NF | 12.74 | 7.6 | 8.55 | 8 → 10 | dB |
| | OOB B1dB | 10 | 1.2 | 8.9 | 6 | dBm |
| | OOB B1dB-NF | -2.74 | -6.4 | 0.35 | -2 → -4 | dB |
| | DC Power | >1000 | 118 | 130 | < 50 | mW |
| Generalized | RF tuning range | ↑↑ | ↑ | ↑ | ↑ | |
| | NF | ↓ | ↑ | – | – | |
| | OOB B1dB | ↑↑ | ↑↑ | ↑↑ | ↑ | |
| | OOB B1dB-NF | ↑ | ↑ | ↑↑ | ↑ | |
| | DC Power | ↓↓ | ↑ | ↑ | ↑↑ | |
| | LO generation | divider | dual-resonant | | sinusoid | |

Table II: Summary of performance metrics and generalizations of HBT N-path iterations

Depending on the desired performance metrics and the power budget allotted for the receiver architecture, different LO generation chain techniques may be employed. Table III summarizes the considerations and performance limitations of all techniques demonstrated and described in this dissertation.

| | LO GENERATION | | | FEEDBACK IMPEDANCE ($Z_{FB}$) | | |
|---|---|---|---|---|---|---|
| | ECL Johnson Counter | Dual-resonant buffer | Balun→CLCs →QHR | Resistor | Emitter Follower | Coupled Inductors |
| **BW / tuning range** | ↑↑ digital/non-resonant | ↑ resonance limits tuning | ↑ limited by $\lambda\backslash 4$ transmission lines | ↑↑ AC coupling BB pole separation | ↑↑ AC coupling BB pole separation | ↑ bandwidth can be limited by inductors |
| **NF** | ↑↑ retimer for LO noise | ↑ large $R_{OL}$ not no retimer | – decent NF from sinusoidal overlap | ↓↓ direct impact of $R_{FB}$ | ↑↑ noise resistance $\sim 1/g_m$ | ↑ inductor resistance |
| **OOB B1dB** | ↑↑ digital ensure quick switching | ↑ 2nd harmonic ensures quick switching | ↑ slight linearity degradation due to overlap | no significant impact because $Z_{FB}$ is scaled by β for degeneration term in linearity | | |
| **OOB B1dB-NF** | ↑↑ | ↑ | ↑ | | | |
| **DC Power** | ↓↓ ECL blocks + high current buffer | – resonance lowers buffer power; needs amp/DVM | ↑↑ fully passive LO generation | ↓ $R_{FB}$ loads LO | ↓ follower always pulls current | ↑↑ presents large impedance |

Table III: Summary of performance metrics and generalizations of demonstrated techniques

### *7.4.2 Summary of Design Parameters*

Building upon the design process described in chapter 3 we summarize performance metrics and dimensionless design parameters in Table IV. Alongside the information summarized in Tables II and III, the HBT N-path designer is equipped to establish realizable performance metrics that fall within a prescribed power budget.

TABLE I

HBT-BASED N-PATH MIXER DESIGN SPACE SUMMARY

| Parameter | Symbol | Expression | Effect on Performance | | |
|---|---|---|---|---|---|
| | | | **noise** | **linearity** | **power** |
| Ratio of switch/antenna impedance | $\rho$ | $\rho = \frac{1}{R_S}\left(\frac{1}{g_m} + \frac{\gamma Z_{FB} \| \gamma Z_{AC}}{\beta}\right) \cong \frac{1}{g_m R_S}$ | optimize | $\rho \downarrow$ then $\uparrow$ | $\rho \downarrow$ then $\uparrow$ |
| Ratio of load/antenna impedance | $\Lambda$ | $\frac{1}{\Lambda} = \frac{1}{\rho}\left[\frac{\pi\omega_{LO}\tau}{N\Psi} + \frac{1}{\mathrm{sinc}^2\left(\frac{\pi}{N}\right)}\left(\frac{1-\mathrm{sinc}^2\left(\frac{\pi}{N}\right)}{1+\left(\frac{N\omega_{LO}}{\omega_m}+\rho\right)^{-1}} + \frac{\rho N R_S}{R_{BB}}\right)\right]$ | $\Lambda \uparrow$ then $\downarrow$ | -- | -- |
| Ratio of feedback/internal base-emitter resistance | $\chi$ | $\chi = \frac{\gamma R_{fb}}{r_\pi} = \frac{\gamma I_C R_{fb}}{\beta v_T}$ | $\chi \downarrow$ then $\downarrow$ | -- | $\chi \downarrow$ then$\uparrow$ (LO loading) |
| Ratio of LO swing/thermal voltage | $\Psi$ | $\Psi = \frac{V_{LO}}{v_T}$ | $\Psi \uparrow$ then $\downarrow$ | $\Psi \uparrow$ then $\uparrow$ (overlap $\downarrow$) | $\Psi \uparrow$ then $\uparrow$ |
| NF [dB] | | $10 * \log_{10}\left(1 + \rho\left[(1+\chi)^2 + \chi\beta\left(1+\frac{\chi}{2}\right)\right] + \frac{[1+\rho(1+\chi)]^2}{\Lambda}\right)$ | | | |
| B1dB [dBm] | | $10 * \log_{10}\left[\left(.44\, v_T \frac{\sqrt{6}\left(1+\frac{1}{\rho}\right)^2}{\sqrt{\frac{2}{\rho}-1}}\right)^2 \frac{1000}{2R_S}\right] \cong 10 * \log_{10}\left[\left(.44\, v_T \rho^{-\frac{3}{2}}\right)^2 \frac{1000}{2R_S}\right]$ | | | |
| Power [W] | | $\frac{1}{\rho R_S}\left(\frac{N\Psi^2}{\pi}\frac{\omega_{LO}}{\omega_T} v_T^2 + v_T V_{CC,mixer}\right)$ | | | |

Table IV: Summary of performance metrics and their dependence on dimensionless design variables

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