MILLIMETER WAVE TRANSCEIVER FRONTEND CIRCUITS IN ADVANCED SIGE TECHNOLOGY WITH CONSIDERATIONS FOR ON-CHIP PASSIVE COMPONENT DESIGN AND SIMULATLION

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A novel design approach for implementing millimeter wave wireless transceiver front-end circuits is proposed. The design methodology takes advantage in advances in Silicon Germanium (SiGe) fabrication technology and sophisticated Electro-Magnetic (EM) simulation software to ensure successful implementation of circuits designed to operate in millimeter wave range. The discussion covers basic circuits common in typical transceiver architecture such as low noise amplifier (LNA), active balun, and mixer. The design methodology is not limited to the above circuits. It can be applied to many other situations where operating frequency is high and the dimensions of passive structures are comparable to signal wavelength.

A comprehensive solution to the design of millimeter wave wireless transceiver front-end circuits requires consideration for active devices as well as passive structures. For circuits operating at 94 GHz, 40 GHz and 18 GHz discussed in this dissertation, each design generally has two parts of discussion – one devoted to circuit design and one devoted to passive design. Optimization of circuit performance and reliability is analyzed in each case. Simulation results from both the circuits and the passives are presented and an integrated simulation environment is proposed to simply the design flow. Some measurement results are provided to confirm the validity of the proposed design methodology. Summaries are given at the end of each chapter and future research direction is highlighted at the end of the dissertation.

BIOGRAPHICAL SKETCH

Yanxin Will Wang was born on October 12, 1979 in Dalian, China and came to the United States in 1997. Yanxin graduated from Cottage Grove High School in Cottage Grove, OR in 1998. He received his undergraduate education from Oregon State University in Corvallis, OR and University of California Berkeley (UC Berkeley) in Berkeley, CA. He graduated in August 2002 with a Bachelor of Science in Electrical Engineering and Computer Science from UC Berkeley. In August 2002 he joined the Broadband Communications Research Laboratory at Cornell University to pursue a Ph.D. degree. He spent the fall and winter of 2005 as an intern at LeCroy Corporation located in Chestnut Ridge, New York where he worked on oscilloscope front-end circuit design. Yanxin received a Master of Science in Electrical and Computer Engineering from Cornell University in May of 2005. He completed his Doctor of Philosophy in Electrical and Computer Engineering with a minor in Earth and Atmospheric Science in August 2006.

To My Parents

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I would like to express my gratitude to my dear parents, Xizhang Wang and Chuangling Qu, who have provided me the perfect environment where my character and intellectual curiosity were nurtured and who have sacrificed so much to support my education in the United States. Without all the love and support I have received all these years from my parents, I would never have been able to successfully reach my academic goals.

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Chapter 1: Introduction

1.1 Overview

Over the past ten years wireless communication industry has enjoyed tremendous growth that has been fueled by many factors such as breakthroughs in communication theory, innovations in digital signal processing, advancement of silicon based VLSI technology, proliferation of internet users, heavy investment from governments and industries, and demands from consumers for reliable and convenient mobile voice and data solutions. Compared to the old analog wireless technology, the new digital technology adopts many forms of digital modulation schemes to achieve efficient use of spectrum space, low bit error rate (BER), low power consumption, and low hardware cost. Despite the fact that there are many modulation schemes, wireless transceiver architecture has remained relatively stable. In a generic wireless transceiver system, a received signal from an antenna needs to be filtered and amplified before it is down converted to a signal at much lower frequency than its carrier frequency. The down converted signal then is digitized to be processed by digital signal processor, which gives output to other digital components to translate the signal into information people can recognize. The transmitting side is the roughly the reverse of the receiving process.

A simplified block diagram of a wireless communication system is shown in Figure 1.1. On the receiver side, a radio signal comes in and gets picked up by the antenna. Then the signal is amplified by the low noise amplifier (LNA), which

suppresses system noise for the subsequent stages. The amplified signal then enters the mixer, which down-converts signal from its carrier frequency – usually in the GHz range and thus difficult to process – to a much lower frequency or directly to DC. This could be achieved in more than one step, based on system specifications and technology limitations. The frequency synthesizer provides the exact carrier frequency for the mixer. Because the carrier frequency sometimes varies from one channel to another due to changes in existing transmitting environment, the frequency synthesizer has to be able to switch to the correct frequency within a reasonable amount of time. The down-converted signal then is digitized by the analog-to-digital converter that feeds the digital signal to DSPs. The transmitting side is roughly the reverse of the receiving side. Instead of down converting the modulated signal the mixer in a transmitter up-converts it to the carrier frequency. Then the power amplifier (PA) greatly boosts the signal power while keeping the signal relatively free of distortion. Finally the signal goes out into the air from the transmitting antenna. The general transceiver architecture discussed so far excludes components that interface with digital domain.

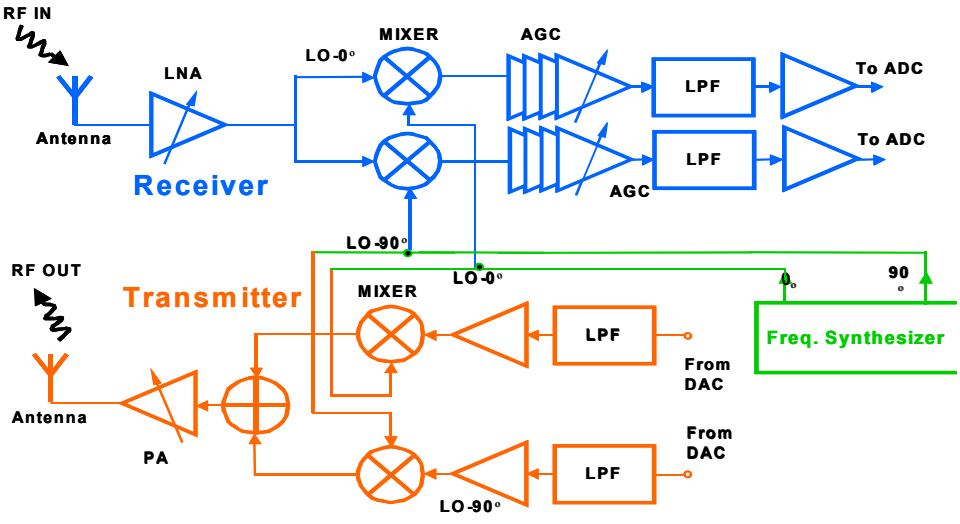

Figure 1.1: Example of a wireless transceiver system

1.2 Motivation

Given the fact that every wireless transceiver has to occupy a part of the radio spectrum, it is not difficult to realize that with ever-increasing number of wireless devices being used every day, radio spectrum becomes a precious resource. Recent spectrum auction price of more than two billion dollars for a total of 120 MHz of spectrum between 1.8 GHz and 1.9 GHz [1] shows how fierce the fight is for the right to have additional spectrum space. Because of the huge cost embedded in getting additional spectrum, many innovative solutions have surfaced to increase spectrum usage efficiency such as Ultra Wide Band, which covers a wide range of spectrum (3.1GHz to 10.6GHz) with very little interference to existing signals within the spectrum [2].

One important factor that contributes to spectrum shortage is that at present commonly used commercial bipolar or CMOS technologies can only handle signals below 10 GHz. Without a more advanced technology the only solution for satisfying increasing demands is to adopt more efficient modulation schemes. However, opportunities arise when FCC opened up spectrum at K and W bands. At such high frequencies allowed bandwidth is significantly higher than that at lower frequencies. Therefore without modifying existing modulation schemes the fact that the carrier frequency is located at higher frequency implies more bandwidth for data transmission. This solves the problem of crowded spectrum usage at below 10 GHz and enables faster wireless data transmission without sacrificing the number of available channels.

Cost and ability to integrate with digital components are important indicators of a successful technology for wireless transceiver chips. The recent development of SiGe technology that claims a maximum f_t of more than 200 GHz at IBM [3] and Infineon [4] makes it possible to have transceiver circuits using Silicon based

technology operating at millimeter wave range. Successful commercial development has been underway for applications in Collision Avoidance Radar (CAR) at 77GHz where transceiver architecture is relatively simple. With the help of sophisticated Electro-Magnetic (EM) wave simulators and state-of-art circuit simulators, it can be expected that millimeter wave wireless transceiver design based on SiGe will eventually achieve the accuracy and predictability that current low frequency design based on SiGe and CMOS enjoys.

1.3 Current Industry Development

1.3.1 Development at IBM

The technology IBM has developed features a 200 GHz f_t and 280 GHz f_{max} [3]. The minimum width of the base for a HBT is 0.12 μm, which reduces capacitive parasitics and base resistance. What sets this technology apart from other high performance SiGe process is its capability to integrate 0.13 μm CMOS process. The presence of CMOS technology makes this BiCMOS process more desirable for system level integration and cost reduction.

Since IBM has developed their SiGe technology with a 200 GHz f_t, IBM T. J. Watson Research Center has used this technology and published several papers that present circuits for collision avoidance radar that operates in the 77 GHz range. The circuits in those published papers include a power amplifier (PA) [5], a voltage controlled oscillator (VCO), and a low noise amplifier (LNA) [6]. The circuits utilize on-chip transmission lines and capacitors for matching networks. Measured results are given to show successful implementation of those components. There are also some LNA's that operate in the 60 GHz range, which is the spectrum for short distance wireless data communication.

In those papers what is remarkable is the low noise performance for the amplifiers (roughly 4.6 dB of noise figure for 60 GHz circuits and 5.6 dB of noise figure for 77 GHz operation). For VCO's the phase noise is measured at –100 dBc/Hz at 1 MHz offset for operations from 53 GHz to 85 GHz. However, the papers do not reveal the design process. They only present the simulated and measured results along with circuit schematics. In those papers, the authors also admit discrepancies between simulation results and measurement results. Some circuits have matching characteristics that deviate from original design targets. In wireless communication, a shift in optimal operating frequency means failure in design. Therefore the importance of accurately predicting the actual performance of a high frequency circuit can never be over-stated.

1.3.2 Development at Infineon

Infineon is another company that has led the commercial development of advanced SiGe technology. At 2004 BCTM Infineon published a paper on its SiGe technology that has 200 GHz f_t [4]. Roughly at the same time period when IBM published its papers on SiGe circuits at V and W bands, Infineon also published a paper on 77 GHz VCO [7]. The circuits that Infineon published include a resonate-tank based oscillator at 77 GHz and a mixer at 77 GHz [8]. The circuits perform roughly at the same level as IBM counterparts.

The technology developed at Infineon features a cut-off frequency of 200 GHz, a maximum oscillation frequency of 275 GHz, and a gate delay of 3.5 ps. The emitter width is shrunk to 0.14 μm in this technology to achieve faster frequency response and smaller base resistance. In addition, deep trench is used throughout the active area to

increase isolation between signal and substrate. The technology also features TaN thin film resistor and MIM capacitor on-chip.

In the descriptions of the circuits mentioned above the authors do not have a comprehensive approach to the design of MM Wave IC. Circuits are considered purely from small signal analysis point of view. There are no discussions of passive structures that affect the outcome of measurement results. There are also little discussions on optimization issues such as choice of circuit topology and device sizes. Without a clear understanding of all the components that play crucial roles in successful implementation of MM Wave IC, the design process can be daunting and full of pitfalls. In the remaining chapters there are detailed discussions dealing with all those issues that are unaccounted for in current research publications.

1.4 Chapters Overview

A novel design approach to the design of integrated circuits for millimeter wave transceiver front-ends is proposed in the following chapters. The new approach considers the effects of device models, circuit topology, passive models, and many other factors that impact actual circuit performance. This design method optimizes parameters that are usually beyond the traditional scope of radio frequency integrated circuits design and the optimization process itself is formulated and enables efficient design flow for some of the key blocks in a transceiver system.

The remaining chapters are organized as the following. Chapter 2 discusses the constraints of basic circuit building blocks such as SiGe fabrication process, device modeling, and passive modeling. Chapter 3 introduces the general design methodology for successful implementation of millimeter wave transceiver front-end circuit design. This chapter discusses in general amplifier and mixer blocks. Chapter

4 discusses a 94 GHz wireless receiver mixer and active balun in SiGe. Detailed design analysis and simulation as well as measurement results are presented. Chapter 5 presents an 18 GHz direct down-conversion double-balanced mixer and an integrated mixer VCO block in SiGe. This chapter is organized similarly as the previous chapter. Chapter 6 discusses a 40 GHz receiver LNA in SiGe. Chapter 7 concludes the dissertation with future research directions.

Chapter 2: Constraints of Millimeter Wave Front-end IC Design

2.1 Overview

In this chapter constraints on the design of millimeter wave front-end integrated circuits are discussed. In the traditional radio frequency integrated circuit design signal wavelength is significantly smaller than device and passive structure dimensions. Therefore research efforts have been concentrated on circuit topology improvement and high Q inductor design. However, in the domain of millimeter wave wavelength becomes comparable to passive structure and device dimensions, thus introducing additional complexity when designing circuits. Furthermore, at high frequency silicon substrate becomes extremely lossy, and isolation between active components is a serious issue for a designer to consider.

This chapter discusses constraints on successful design of millimeter wave transceiver circuits in great detail. In additional to the aforementioned constraints, issues associated with modeling and simulation are also discussed. The goal of this chapter is to present difficulties a designer faces when designing circuits at very high frequencies, which leads to the remaining chapters that propose novel design solutions to overcome these problems along with several design examples to validate the proposed solutions.

2.2 Constraints from SiGe Device

Constraints from SiGe active devices are due to fabrication process and device modeling. Since some key fabrication parameters are protected commercial secrets, the following discussion is based on generic SiGe process. However, the generic SiGe process and device modeling is a good approximate of real data from different foundries mainly because SiGe HBT technologies share the same fundamental principles in active device operation. The conclusions drawn from the generic process therefore is applicable to all SiGe HBT based design.

2.2.1 Lossy Silicon Substrate

One factor that makes some III-V process technologies such as GaAs and InP attractive for millimeter wave IC design is their low-loss substrate. Given the small dimensions of modern processing technology, devices are placed very close to each other even though each has complete different functionality in the whole system. Inevitably cross-talk between adjacent devices becomes a serious issue in analog circuits where each circuit element is assumed to be isolated from one another. In addition, lossy substrate introduces finite resistance to ground, which may attenuate critical signals.

In order to have some appreciation for the difficulties involved in dealing with substrate cross-talk and signal loss, a realistic substrate model is described here. The parameters for the substrate model closely mimics the one used for the designs discussed in this dissertation. According to [9], SiGe substrate resistivity is 20 Ω·cm, and substrate thickness is 300 μm, both of which are important in determining the substrate model for circuit analysis.

A test structure for evaluating the substrate parasitics is shown in Figure 2.1. Substrate coupling between an 80 μm x 260 μm isolation box connected to terminal A

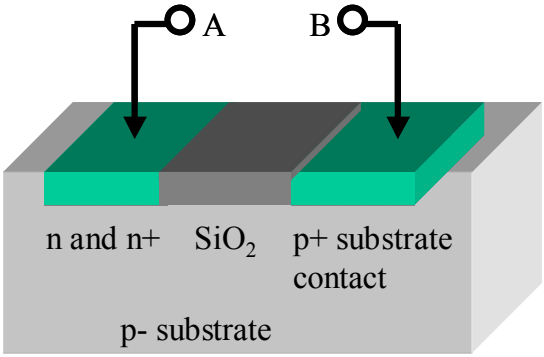

Figure 2.1: Substrate test structure

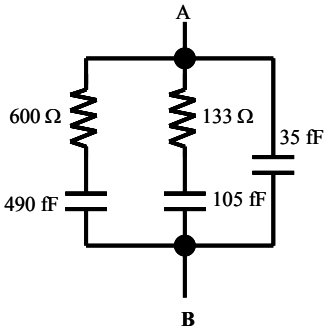

Figure 2.2: Substrate test structure circuit model

and a large substrate contact of size 120 μm x 200 μm connected to terminal B is considered. There is a shallow trench layer between the two terminals that reduces coupling between the two areas. The trench layer material is SiO_2, which has much less conductivity then p- substrate. Figure 2.2 shows a model derived from substrate material parameters. The model is verified through actual measurement. In a more realistic setting, two devices may not occupy such a large area and therefore the RC network used to model coupling between two small devices will have much less capacitance and much more resistance. At low frequencies two devices placed far away from each other may very well be isolated. However, at high frequencies even several fF of capacitance can have some impacts on isolation and matching characteristics of a circuit.

2.2.2 High Frequency Device Modeling

Complexity of active device modeling increases with operating frequency. At high frequency a simple model often fails to consider many secondary physical effects that are critical for design success. In RFIC design, circuits are optimized according to each device's power, noise, linearity and small/large signal parameters. All those parameters are functions of device size, biasing point, temperature, process and frequency. Those dependencies are not always linear and often have to be determined by experimental data to fit original equations that may otherwise predict results deviating from measurement data.

Accurate device modeling is the key to the success of design of integrated circuits at high frequency. However, there is also a speed and accuracy trade-off between modeling and simulation. The best scenario that could be achieved is a simple but accurate model. To this end, there has been much research in the past to perfect models for SiGe HBT at high frequencies. One model presented by [10] is one step closer to the desired solution. The model is described in Figure 2.3.

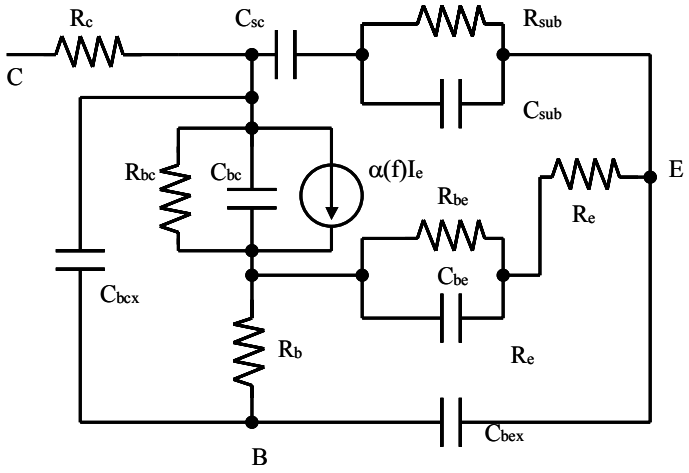

Figure 2.3: SiGe HBT high frequency model

The model depicted in Figure 2.3 derives its parameters from actual tests performed under a stable environment for a single device. For various devices sizes more tests can be run to extrapolate those parameters at a higher level of accuracy. Some parameters are linearly extrapolated and some are not. Extrapolation method depends on both actual data points and device physics, and device physics often dictates relationships between device sizes and device parameters. With all the parameters in place, simulated S-Parameters match measurement results within 10% error at 40 GHz. In addition, there is also a noise model derived from measurement results that predicts noise figures of the device within 0.1 dB at 5GHz. However, the model generates much larger error in predicting noise figure at higher frequencies due to lossy substrate.

At low frequencies, the methods mentioned above can yield a reliable set of parameters for circuit simulation. However, what is noticeable in high frequency modeling is extracted device parameters have a strong dependency on test setup. This is mainly because at high frequencies passive structures that are necessary to connect the test equipment and the device under test contribute to the overall response of parameter extraction. An improperly de-embedded structure will lead to inaccurate modeling parameters. Thus for a circuit designer who does not have control over model parameters it is important to realize limitations imposed by foundry models and avoid situations where critical circuit performance is determined by device parameters that vary a lot with temperature, process, and bias conditions.

2.3 Constraints from Passive Elements

Passive circuit elements are critical components of MM Wave IC design. Due to lossy substrate in SiGe technologies compared to other high resistivity substrates,

passive elements have to shield signals from substrate as much as possible. Process determines backend layer thickness and this in turn limits the vertical dimension of passive structures. Given all these limitations, a combination of microstrip and coplanar transmission line becomes the ideal choice for on-chip transmission line for MM Wave IC design. Figure 2.4 shows the difference between microstrip line, coplanar line, and the combination of both, which is the ideal choice for high frequency applications. For microstrip line it is a convenient choice for monolithic process compared to other forms of transmission lines such as rectangular wave guides or stripline where a fully enclosed shape needs to be formed. However, because microstrip line has no ground shield at the top, the wave propagation on a microstrip line is in hybrid mode, namely TE and TM. This complicates the analysis and model accuracy of microstrip lines. In order to improve on microstrip line, a coplanar structure that introduces additional ground planes to the signal line can be combined to make a semi-enclosed box. The result is EM lines mostly confined by the surrounding ground structures and thus analysis of this structure is simplified and more accurate.

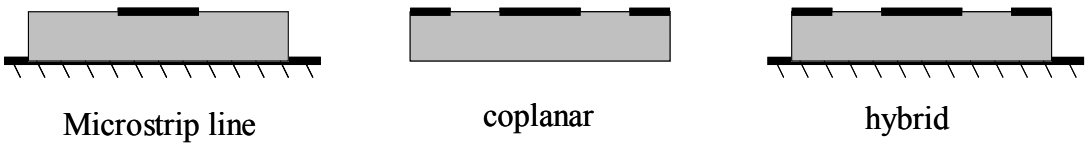

Figure 2.4: Stripline, coplanar, and combination of the two

2.3.1 Electric-Magnetic (EM) Modeling

Choosing the right structure that simplifies analysis is just the first step towards a full solution for designing passive structures. In very high frequencies, transmission lines are extensively used because they provide better isolation and can be controlled very easily by altering their dimensions. Accurate EM modeling plays an important part in determining the robustness of passive structures. The definition of passive structures discussed here needs to include other elements such as filters, capacitors, pads, etc, elements that are located in the back-end layers. Even though resistor constitutes a passive structure, for lack of control by the designer and its resistive property, it is does not need to be simulated by EM software.

For a complex structure, simple models that predict passive structure's frequency response fairly accurately at low frequencies often fail when they try to extrapolate the results for a more complex geometry at higher frequencies. Therefore it is necessary to use mesh-based EM simulation tools to have much more accurate predictions on a specific passive structure. However, running EM numerical simulations takes a lot of resources and usually becomes unrealistic for a large chip where many passive structures are laid out. Another challenge in using EM simulation is the complexity of simulation setup. Even though several EM simulation software vendors have come up with ways to simplify structure import from CAD tools familiar to circuit designers (Ansoftlinks from Ansoft Corporation, for example), the port setup, which is responsible for mimicking the real EM wave excitation, can be complicated and error-prone. Unfortunately, an incorrect port setup usually results in wrong simulation data and renders final circuit simulation results useless.

2.3.2 Parasitic Extraction

In current circuit design environment there are established methods to extract circuit parasitics associated with a particular layout. The extraction part of the simulation flow is facilitated by metal layer dimensions provided by a foundry, which are fed into some predetermined formula to calculate capacitance and resistance corresponding to that specific layout. Inductance extraction is trickier in a sense that it is defined in a loop and the return path needs to be known in order to extract the proper inductance. In addition, inductance is also affected by magnetic coupling between adjacent conductors. Furthermore, inductance is a frequency dependent parameter and an inductor's geometry usually dictates the dependency. Finally, skin effect and proximity effect can also contribute to extracted inductor quality factor. There has been concentrated research on inductance extraction and one of the most efficient and effective is FASTHENRY from MIT [11]. It presents an efficient solution to inductance extraction along with many others that are commercially available. However, all the available methods are not automated at the same level of RC extraction and therefore manual intervention in the design flow is required.

At very high frequency it becomes critical for any extraction method to account for any parasitic component existing in the layout for critical signal paths. In reality, however, extraction methods competent for low frequency extraction often fail at high frequencies. The complexity associated with inductance extraction introduces additional level of uncertainty in back-annotated circuit simulation. A solution is needed for successful implementation of MM Wave IC circuit design, which has to avoid the problems of inaccuracy of regular RLC extraction programs at high frequency, and yet at the same time does not introduce significant increase in simulation time and effort.

2.4 Conclusion

This chapter discusses the limitations that a designer has to face in order to successfully design an MM Wave IC given today's technology. Limitations consist of several aspects in a design cycle. Models of SiGe devices at high frequencies are derived from data extracted from device under test at certain conditions. Those data are extrapolated to fit all sizes and all operating conditions. At high frequencies improper de-embedded test setup can skew device parameters by a large margin, thus making it less reliable. Silicon substrate also presents another problem because of its low resistivity. Therefore signals can easily be coupled to unwanted paths and as a result, actual measurement results will be different from that of simulation if the effect is not modeled. Passive structure is another important aspect of MM Wave IC design. Traditional low frequency extraction tools are not able to account for all the electrical and magnetic interactions but at the same time, more accurate CAD tools demand much longer simulation time and are prone to mistakes in simulation setup.

The following chapters will address issues discussed in this chapter and several design examples are presented to illustrate how optimized design methodology can make designs more robust and design process more efficient.

Chapter 3: Design Methodology for Millimeter Wave Integrated Circuits

3.1 Overview

In this chapter a novel design methodology for millimeter wave integrated circuits is proposed. The chapter first discusses the impact of circuit topology on robustness of MM Wave IC circuit design. Two main blocks (LNA and mixer) in a wireless transceiver system are considered for this purpose. Since matching is closely related to device sizes and bias conditions, optimization is discussed next after topology choice. In addition to circuit elements, there are also layout components that need to be analyzed and optimized. Another area of the design process is simulation. Modeling of passive structures, extraction of substrate coupling as well as interconnects, and integration of simulation environment are all considered and a solution for simplifying the simulation process is proposed. The general discussion of this chapter presents a novel approach that uses numerical and circuit analysis to achieve a design methodology that can be applied to many other LNA and mixer designs that operate in the millimeter wave range in different SiGe Technologies.

3.2 Analysis of Circuit Topology Trade-offs

3.2.1 Topology for Low Noise Amplifiers (LNA)

LNA's are a crucial component in a wireless transceiver system. It is the first block in a system that provides gain to the incoming signal and therefore suppresses

noise. A good LNA must have low noise, high gain, and high linearity and consume as little power as possible. Furthermore, LNA's must achieve good input and output power match so that power transfer is maximized at desired frequencies. Since signals from antenna are single-ended, LNA needs to take single-ended data and output either single-ended or differential signals. Several configurations can be considered for this type of application.

The most common configuration for an amplifier is common-emitter. Figure 3.1 shows an NPN HBT is connected in this configuration. This is the simplest way to amplifier a signal. With its simplicity, there are many serious drawbacks to prevent its use. Consider the small signal equivalent of the common-emitter circuit on its left. For a complete small signal analysis to find the transfer function, it can be shown as

$$\frac{v_{out}}{v_{in}} = \frac{s - \dfrac{g_m}{c_\mu}}{c_\pi r_b [s^2 + s(\dfrac{1}{c_\pi \cdot r_b \,\|\, r_\pi} + \dfrac{1}{(c_\mu + c_\pi)\cdot Z_L \,\|\, r_0} + \dfrac{g_m}{c_\pi}) + (\dfrac{1}{c_\pi \cdot r_b \,\|\, r_\pi \cdot Z_L \,\|\, r_o})]}. \quad (3.1)$$

From this equation the complicated but complete representation of all the major small

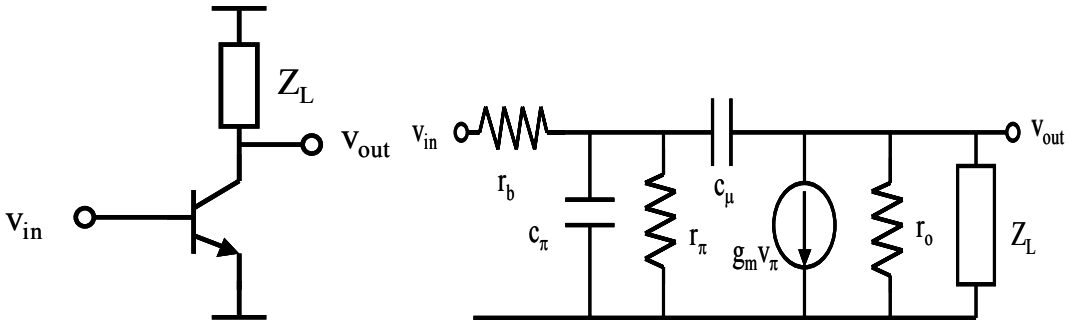

Figure 3.1 Common-emitter configuration and simplified small signal model

signals does not give much insight into the transfer function. However, by lumping the Miller capacitance c_μ to the input, the expression can be simplified to have only the sum of gain adjusted c_μ and c_π as the dominant pole in this circuit. From this pole it is easy to see that the transfer function is dominated by the emitter to collector capacitance c_μ and circuit power gain is significantly affected.

Another problem with this kind of configuration is that the circuit can be potentially unstable at high frequencies. This is due to the fact that the presence of c_μ constitutes a feedback network for the amplifier. The *K* factor, which measures the stability of a given circuit by calculating S-parameters, has a component for S_{12}, which is the reverse gain path for the two port network used in deriving the expression for *K*. *K* is given as follows.

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{11}||S_{12}|}\ , \tag{3.2}$$

where $\Delta = S_{11}\,S_{22} - S_{12}\,S_{21}$. If $K > 1$ and $\Delta < 1$, the circuit is unconditionally stable.

Since this common-emitter configuration has so many drawbacks, it is not realistic to use this simple configuration to design a high frequency circuit. Therefore it is worthwhile to explore other possibilities.

The next circuit configuration under consideration is common-base. Common-base configuration has the benefit of duplicating input current to the output. With the simplified small signal analysis used in the previous common-emitter configuration, the transfer function can be shown to be

$$\frac{v_{out}}{v_{in}} = \frac{g_m z_L}{1 + s c_\mu z_L}, \tag{3.3}$$

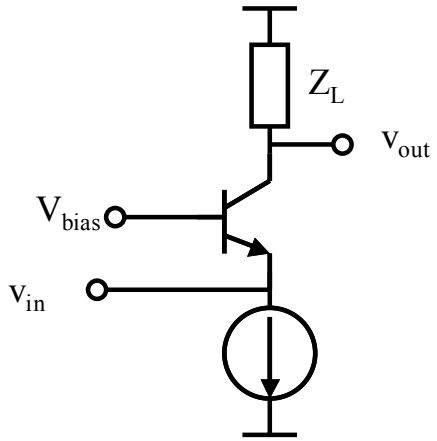

Figure 3.2 Common-base configuration

where resistance between base and emitter and collector to emitter is omitted. What this simplified equation shows is the pole of the transfer function is solely decided by load and c_μ. Compared to the common emitter case, it is obvious that the Miller effect is eliminated. In terms of stability, S_{12} can be seen as an isolation parameter for this configuration and in this case it will be the inverse of the gain transfer function. Isolation degrades with increasing frequency and the corner frequency is proportional to $c_u Z_L$. If Z_L is inductive, there potentially can be a point where inductance and capacitance resonate and isolation is well controlled. The conclusion from this simplified analysis shows that common base configuration is better in high frequency operation in that it does not generate Miller capacitance and the reverse isolation is better than common-emitter configuration.

One transistor configuration is the easiest to analyze. However, in order to further enhance circuit performance, other circuit topology needs to be analyzed to find an optimal solution for amplifier design.

Following the discussion above, it is obvious that in high frequency operation, Miller capacitance needs to be avoided as much as possible. This in turn means the

collector and the base of a transistor cannot see voltage gain. Another type of amplifier topology that avoids voltage swing on the collector-base junction is cascode. For cascode configuration, it can be seen as a combination of a common-emitter or common base stage with common-base stage. Two possible configurations are shown in Figure 3.3.

In Figure 3.3 (a) has common-emitter and common-base configuration. The benefit of this type of configuration is that Q_2 shields any voltage swing seen by Q_1, therefore eliminating Miller effect. In terms of stability, the path from v_{out} to v_{in} is further enhanced by the transistor stack-up. The downside of this topology is reduced linearity due to reduced output swing, which depends on available headroom for a given power supply.

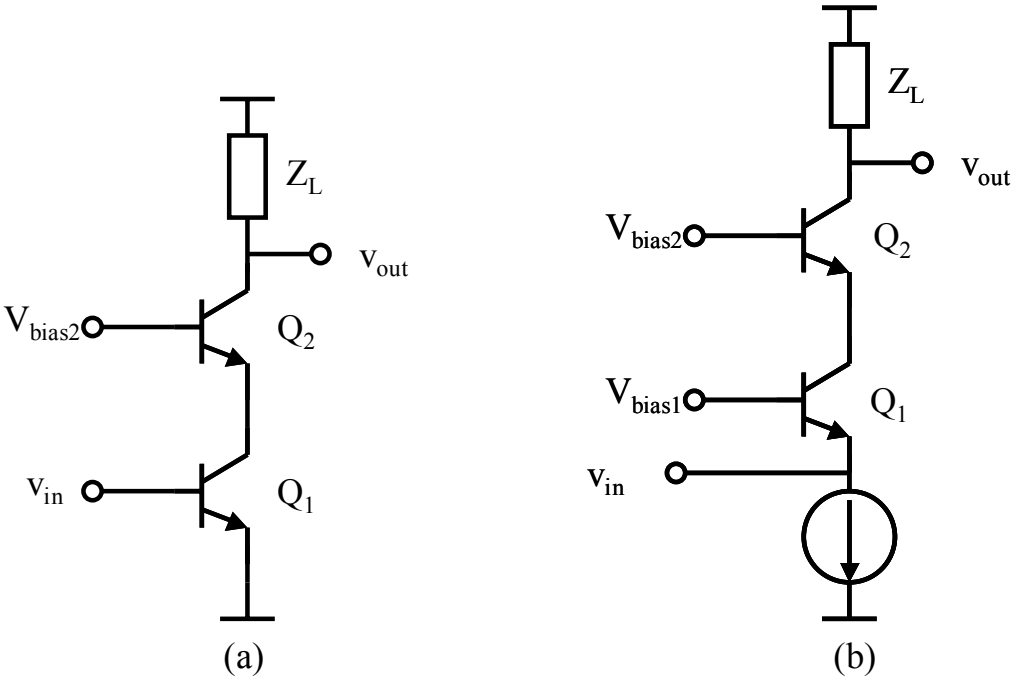

Figure 3.3 Cascode configuration for (a) common-emitter and (b) common-base

A quantitative way of illustrating its advantage is shown below in equation (3.4). Again, transfer function is used to demonstrate the effect of c_μ on its frequency response. In (3.4) many simplifications are taken so that an intuitive equation can be derived to show the fact that one more transistor cascoded with a common-emitter essentially has the same transfer function as the common-base configuration. Therefore Miller effect is avoided and reverse isolation is enhanced.

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} \cdot z_L}{1 + \frac{z_L}{r_{o1}} + sc_{\mu 2} z_L} \tag{3.4}$$

Another configuration is shown in Figure 3.3 (b) where the first input stage is common-base stage instead of a common-emitter stage. The cascode structure makes it have the same benefits enjoyed by (a). However, this is a redundant effort because the first common-base stage by Q_1 already shields the transistor from seeing the collector-base capacitance. The advantage of this type of configuration lies in input matching, which is discussed in the following sections.

3.2.2 Topology for Mixers

Mixer down-converts or up-converts base band signal to the carrier frequency. Some key specs for mixer are conversion gain, linearity, noise figure, and power consumption. A good design practice should consider all aspects of mixer design and balance competing specs. Most commonly seen mixers include single balanced mixer and double balanced mixer. Single balanced mixer takes single-ended input signal and local oscillator signal and output a differential signal. Double-balanced mixer uses differential signal for input and output. The main difference between the choice of single-ended signal and differential signal is linearity. Since single ended signal does

not suppress second order distortion, linearity performance is usually worse than differential operation. For this purpose, double-balanced mixer is always a better choice for linearity purpose. Another advantage represented by double-balanced design is its ability to suppress feed-through. Feed-through is a measure of unwanted signal leakage. Leakage occurs when local oscillator signal can be traced at input or output. Due to local oscillator's large input voltage swing, inevitably it will find a path to input or output. A well-designed mixer needs to suppress this unwanted signal from a topology that is independent of other circuit parameters. A single balanced mixer is shown in Figure 3.4.

In Figure 3.4 v_1 is the input signal and v_2 is the local oscillator signal. v_1 modulates current I_o supplied to transistors Q_1 and Q_2. v_2 also modulates currents in the differential pair i_1 and i_2. The difference in the output currents from the mixer is then given by

$$i_1 = \frac{I_o}{1 + e^{-v_2 / v_T}} \tag{3.5}$$

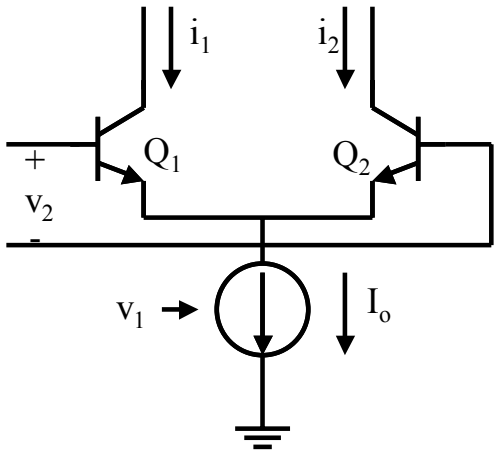

Figure 3.4 Single balanced mixer

$$i_2 = \frac{I_o}{1 + e^{v_2 / v_T}} \tag{3.6}$$

Thus, the difference in the output currents from the mixer is given by

$$i_o = i_1 - i_2 = I_o \left(\frac{1}{1 + e^{-v_2 / v_T}} - \frac{1}{1 + e^{v_2 / v_T}} \right) = I_o \tanh \frac{v_2}{2v_T} \tag{3.7}$$

This can converted to a differential voltage with equal load resistors in the collectors. For small input signals, if $v_2 << v_T$, then

$$i_o \approx I_o \frac{v_2}{2v_T} \tag{3.8}$$

Since it is assumed that the current I_o is modulated by v_1, which can be replaced by $I_o + g_{mc} v_1$, where g_{mc} is the transconductance of the current source, then

$$i_o = \left(I_o + g_{mc} v_1 \right) \tanh \frac{v_2}{2v_T} = I_o \tanh \frac{v_2}{2v_T} + g_{mc} v_1 \tanh \frac{v_2}{2v_T} \tag{3.9}$$

It is obvious to see that the signal representing local oscillator v_2 shows up at the output for this configuration, whereas if output can somehow become differential, the effect will be eliminated structurally.

In Figure 3.5 a double balanced mixer topology is presented. Its differential structure completely eliminates feed-through from local oscillator port. Intuitively, this structure employs four switching transistors instead of two in the single balanced case, which at any moment has at least two transistors combine modulated signals from the differential input. This combination of differential signal can cancel any components that are common to each of the signal path, thus reducing feed-through from the local oscillator port.

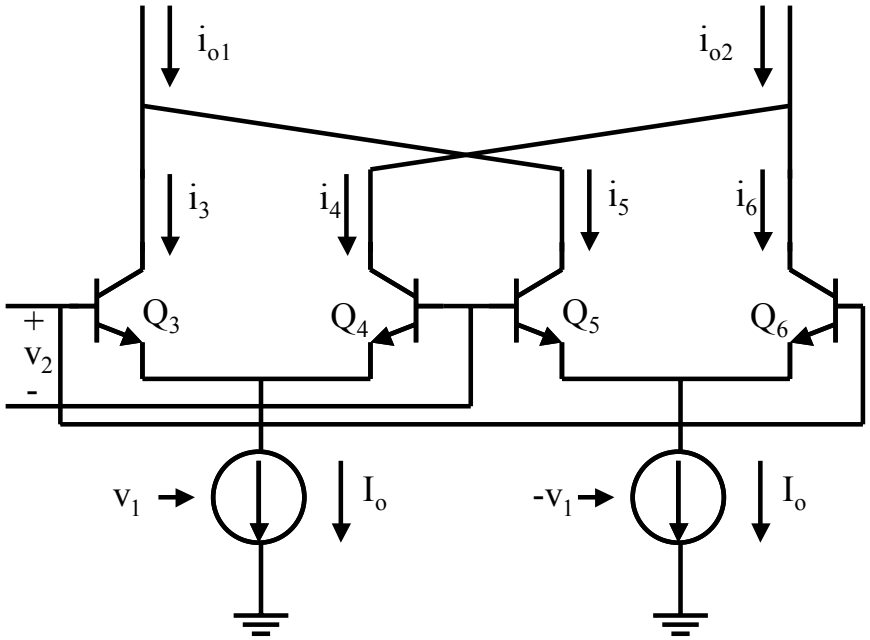

Figure 3.5 Common-base configuration

Following the previous discussion on output current generated by mixing input and local oscillator signals, the output current for double balanced mixer can be derived easily. The output current for the second differential pair is given by

$$i_o^{'} = i_6 - i_5 = I_o \tanh\frac{v_2}{2v_T} - g_{mc}v_1 \tanh\frac{v_2}{2v_T}. \tag{3.10}$$

Therefore the total differential current is

$$i_{out} = i_o - i_o^{'} = 2g_{mc}v_1 \tanh\frac{v_2}{2v_T}. \tag{3.11}$$

This removes the v_2 feed-through term that was present in (3.9).

Another type of mixer is sub-harmonic mixer. Sub-harmonic mixer uses several different topologies such as anti-parallel pair [12], resistive mixer [13], or using passives to achieve 180-degree phase shift for input signal combined with

identical LO signal for sub harmonic mixing [14]. In the past, sub-harmonic mixers are good choice for mixers operating in the millimeter wave range since they use higher harmonic contents to mix with RF signal, thus avoids limitation set by active devices' cut-off frequency. However, the disadvantage of using sub-harmonic mixer is its low conversion gain. This is an intuitive conclusion because the higher harmonics of the mixing function has lower amplitude than the fundamental. Along with lower conversion gain, input noise cannot be effectively suppressed and therefore the SNR of such mixer suffers. With the emergence of new SiGe process that has an f_t of more than 200 GHz, circuits operating in the 60 GHz or the 77 GHz range can be biased such that active devices can still contribute significant current gain. This enables mixer topology to use the switching characteristic of active devices to get better conversion gain and SNR.

3.3 Matching Considerations

The concept of matching comes from the fact that maximum power transfer is achieved when source impedance and load impedance are equal if they are real or conjugate of each other if they have imaginary parts. In a wireless system antenna are designed to have an impedance of 50 Ω and this usually sets the source impedance for LNA. For components that do not have to interface with off-chip signal transfers, an arbitrary impedance can be found. This impedance is usually higher than 50 Ω to reduce the power drain associated with driving low impedance.

3.3.1 Matching Network

In order to match the impedance looking into a circuit to 50 Ω, impedance transformation network is needed. The idea behind impedance transformation is that for a given non-zero impedance, a network of L's and C's at low frequency or a network of stubs (transmission lines terminated to ground or open) connected in series

or in parallel with the given impedance can alter the total impedance looking into the circuit. Since there is a choice between LC matching network and stub matching network, limitations of each need to be discussed to justify the proper use of a particular network.

If an unmatched impedance has a real part, theoretically it can be matched to 50 Ω by any L and C network. For an unmatched impedance $z = x + jy$ ($x \neq 0$ or ∞), there are several possible ways of construction a matching LC network using two elements. The first connection could be series or shunt L/C and the second can be a series or shunt L/C. In Figure 3.6, one particular example is given on Smith Chart. Smith Chart is a convenient way of designing matching network [15]. For every point on the chart, there is a corresponding impedance. The Y circles represent a shunt connection and the Z circles represent a series connection. For an inductor connected in series with a load, the total impedance is moved clockwise on the Z circle. For a capacitor connected in series with a load, the total impedance is moved counter-clockwise. Shunt connected inductor and capacitor follows similar rules to move around Smith

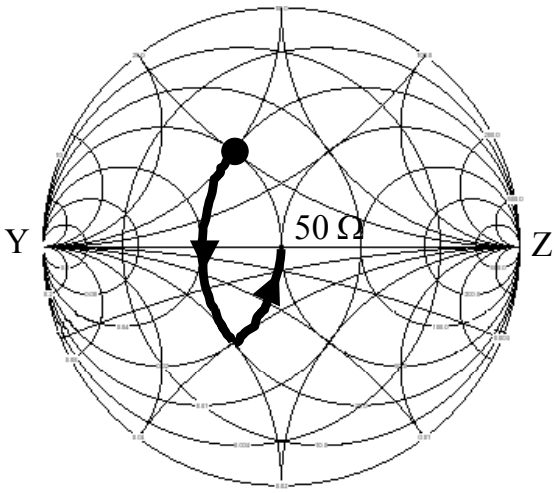

Figure 3.6 Smith Chart with a matching example

Chart. In Figure 3.6, it is easy to see that for any given point, there is always a path to the center of the circle, which represents 50 Ω.

Mathematically it can be proved that for a complex number with a real part, combinations of series and/or shunt connection of $1/j\omega C$ and $j\omega L$ will create a value that has only a real part. However, one limitation of the LC network is that the inductance and capacitance of on-chip components are limited to certain values due to their limited dimensions. [16] gives a mathematical expression on how large an area on Smith Chart covers given a specific source and load impedance and maximum and minimum values of L and C.

For millimeter wave applications, however, simple on-chip inductors and capacitors have many secondary effects and usually those secondary effects cannot be ignored. For spiral inductors typically used in radio frequency applications, an accurate model needs to consider many secondary effects such as skin effect, proximity effect, substrate capacitance, metal resistance, and interline/cross-under coupling capacitance [17]. As its experimental results show, at high frequencies on-chip inductors have diminished inductance due to capacitive coupling. Skin effect also reduces the quality factor (Q) of inductors to a level that is not useful for most of the applications. According to these limitations, spiral inductors are not suited for millimeter wave circuits.

On the other hand, stub matching provides an excellent way of constructing a matching network on-chip. Because operating frequencies for millimeter wave range are in the tens of Gig hertz range, signal wavelength is reduced to dimensions that are comparable to the on-chip device size, which enables on-chip stub matching network to be implemented. In a typical SiGe process, distance between the top layer metal and the bottom layer is roughly in the range of 10's of microns. With a dielectric constant of 4.1 for SiO_2, it is straightforward to calculate the unit inductance and

capacitance for a transmission line that has both side and bottom ground shield. For a transmission line, the wavelength of a signal traveling through is given by

$$\lambda = \frac{2\pi}{\omega\sqrt{LC}}, \tag{3.12}$$

where L and C is unit inductance and capacitance. As frequency increases, signal wavelength is shortened. Experimental data show that for a 100 GHz signal the wavelength on a transmission line can be 1500 μm [18], which is comparable to the chip size and can be conveniently implemented on chip.

With its feasibility established, on-chip transmission line provides many benefits that regular passive devices cannot. As mentioned earlier, the benefit of having transmission line on-chip is its use of shields to reduce coupling to substrate and other components. Furthermore, transmission line offers a flexible way of matching a particular impedance by using a tapered line, which directly transforms one impedance to another without additional matching network. One difficulty associated with on-chip transmission line is the return path. Without a ground plane, the return path goes through substrate and because substrate has frequency dependent parameters that are hard to define precisely, leading to large errors in its modeling behavior [19]. With a ground shield, transmission lines behave mostly the way models predict, proving the usefulness of the shield.

To further enhance the quality of transmission line's Q, other techniques have been reported. One of such techniques is to have a floating bottom shield instead of a connected bottom shield [20]. This technique predicts that by using floating metals to link equally opposing electric field emitting from the passive component and its current-return path, the floating shield stays at 0 V without an explicit ground reference. This overcomes the difficulty of designing a 0 V (explicitly) grounded

shield on silicon-based MM Wave IC. Floating shields for passive devices are physically separated and thereby minimize unwanted coupling between devices.

In order to do stub matching, Smith Chart is an intuitive way to derive stub length. With transmission lines, a load impedance can travel on a constant SWR circle, which is concentric with Smith Chart. For shorted stub, it behaves like an inductor on Smith Chart. As its length increases, it moves along clockwise following the constant reactance circle. Similarly, an open stub resembles a capacitor and it moves along the constant susceptance circle.

3.3.2 Active Device Matching Considerations

Even though matching network can transform almost any given input impedance to match that of the source, there is an additional dimension of issues for designing active devices. As discussed before, the idea of having a properly matched input impedance maximizes power transfer from source to load. In an amplifier or a mixer design, power transfer is not the only spec that determines performance. Noise

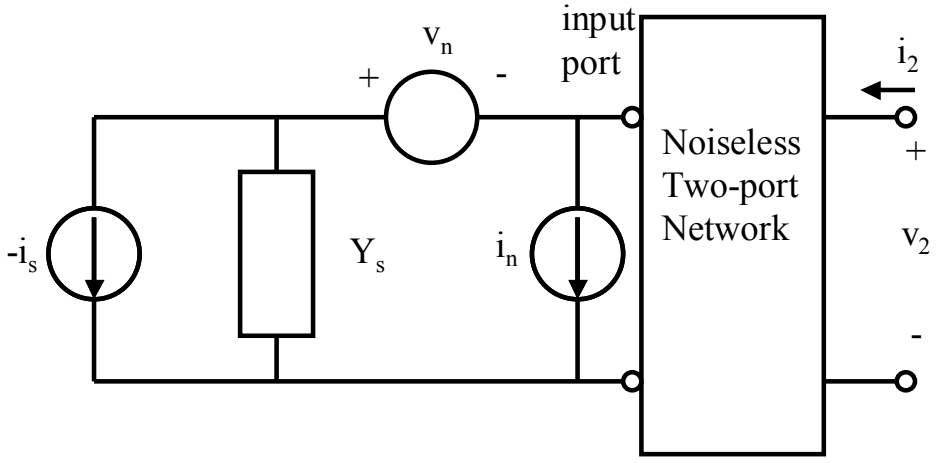

Figure 3.7 Noise model for calculating amplifier's noise figure

consideration is equally important in evaluation of a front-end component. In order to optimize noise performance of a given amplifier, the concept of noise matching needs to be introduced. To define a noise performance parameter, the concept of noise figure (NF) is used. NF is defined as the ratio of the total available noise power at the output of a network to the available noise power at the output due to thermal noise from the input termination resistor.

Figure 3.7 describes a generic noise model for a two-port network. Noise sources are lumped to the input and the two-port network itself is noiseless for simplicity.

The total output noise power is proportional to the mean square of the short-circuit current ($\overline{i_{sc}^2}$) at the input port of the noise free amplifier, while the noise power due to the source alone is proportional to the mean square of the source current $\overline{i_s^2}$. Therefore the NF is given by

$$F = \frac{\overline{i_{sc}^2}}{\overline{i_s^2}}. \tag{3.13}$$

Since

$$i_{sc} = -i_s + i_n + v_n Y_s, \tag{3.14}$$

it follows that the mean square of i_{sc} is given by

$$\overline{i_{sc}^2} = \overline{(-i_s + i_n + v_n Y_s)^2} = \overline{i_s^2} + \overline{(i_n + v_n Y_s)^2} - 2\overline{i_s (i_n + v_n Y_s)} \tag{3.15}$$

Since the noise from the source and the noise from the network are uncorrelated, the term that contains the multiplication of i_n and i_s has to be zero. After shifting some terms around, equation (3.13) becomes

$$F = 1 + \frac{\overline{(i_n + v_n Y_s)^2}}{\overline{i_s^2}} \tag{3.16}$$

There is some correlation between the external source v_n and i_n. So in can be written as a composition of two parts, one correlated to v_n and one that is not. To link in and v_n, another coefficient Y_c can be defined such as the correlated part of in is $Y_c v_n$. Substitute the new expression for in into (3.16). The new expression for F becomes

$$F = 1 + \frac{\overline{(i_{nu} + (Y_c + Y_s)v_n)^2}}{\overline{i_s^2}} \tag{3.17}$$

The noise produced by the source is related to the source conductance by

$$\overline{i_s^w} = 4kT_o G_s B\,, \tag{3.18}$$

where $G_s = \mathrm{Re}[Y_s]$. The noise voltage can be expressed in terms of an equivalent noise resistance R_n as

$$\overline{v_n^2} = 4KT_o R_n B \tag{3.19}$$

and the uncorrelated noise current can be expressed in terms of an equivalent noise conductance G_u, which is

$$\overline{i_{nu}^2} = 4kT_o G_u B \tag{3.20}$$

Substitute (3.18), (3.19), and (3.20) into (3.17) with $Y_c = G_c + jB_c$ and $Y_s = G_s + jB_s$ and the new expression for F is

$$F = 1 + \frac{4kT_o G_u B + |\, G_s + jB + G_c + jB_c\,|^2\, 4kT_o R_n B}{4kT_o G_s B} \tag{3.21}$$

$$= 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}[(G_s + G_c)^2 + (B_s + B_c)^2] \tag{3.22}$$

To minimize noise contribution, B_s needs to be equal to $-B_c$. Furthermore, the expression can be minimized by choosing a G_s that gives the local minimum for the equation. To derive this local minimum, a derivative of F with respect to G_s can be found and the expression for G_s that gives the minimum value of F is

$$G_s = \sqrt{G_c^2 + \frac{G_u}{R_n}} \tag{3.23}$$

In order to satisfy both maximum power transfer and minimum noise figure, the input impedance looking into the active devices needs to be designed in such way that when matching network is attached it can achieve simultaneous power and noise match. Because noise match equations derive optimal values for the source impedance, and source impedance is usually fixed to 50 Ω, the design problem becomes how to find an input impedance for a given circuit that has optimal noise and power impedance located at points symmetrical to the x-axis.

Figure 3.8 demonstrates the ideal case of simultaneous power and noise match. For a two-port network, there exists a value for optimal source reflection coefficient Γ_{opt}. Since this value refers to impedance looking into the matching network from the amplifier, and Γ_{in} refers to the impedance looking into the amplifier, the two values have to be symmetrical around the x-axis on the Smith chart, i.e. $\Gamma_{opt} = \text{conj}(\Gamma_{in})$.

With the goal of achieving simultaneous power and noise match, the next step would be to find the relationship between optimal source reflection coefficient and input impedance. Since both values depend on device size, circuit topology, bias

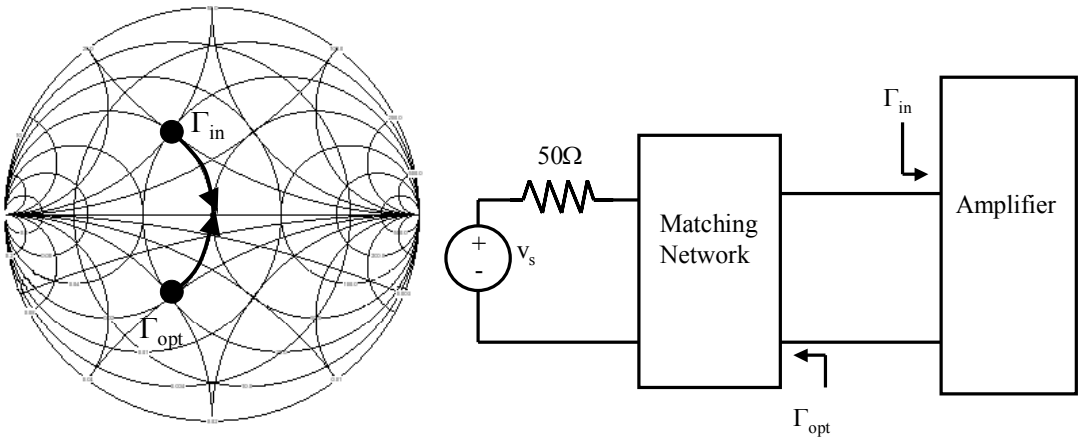

Figure 3.8 Ideal simultaneous noise and power match

conditions, and process technology as well as ambient temperature, and their correlation is not intuitive, it is useful to derive a formula that links both values with all the parameters that a designer has control over. Thus design time and accuracy can be greatly improved.

First, the most important parameter for this type of optimization is circuit topology. Different circuit topology results in changes in the inherent connection between input impedance and optimal source reflection coefficient, given that all other parameters are held constant. Therefore it is imperative to fix the design within a universally applicable topology so that a designer does not need to derive the complex formula every time a design changes.

As mentioned earlier, among many amplifier topologies, common emitter and common base with a cascode device is the most useful topology for MM Wave IC application. Therefore it is useful to formulate the relationship between optimal noise match and power match for those two configurations.

First, it is useful to derive input impedance for a common-emitter with cascode configuration. For the circuit in Figure 3.3 (a), the input impedance Z_{in} looking into the base of Q_1 is

$$\begin{aligned} Z_{in} &= r_{b1} + \frac{r_{\pi 1}}{1 + j\omega r_{\pi 1}[c_{\mu 1}(1 + \frac{g_{m1}}{g_{m2}}) + c_{\pi 1}]} \\ &= r_{b1} + \frac{r_{\pi 1}}{1 + \omega r_{\pi} c_{lump}} - j\frac{r_{\pi}^2 \omega c_{lump}}{1 + \omega^2 r_{\pi}{}^2 c_{lump}^2} \end{aligned} \tag{3.24}$$

where $c_{lump} = c_{u1}(1+g_{m1}/g_{m2})+c_{\pi 1}$. The expression for Z_{in} clearly shows that the effect of cascode has minimum impact on input impedance.

To derive an expression for the optimal source reflection coefficient, there need to be a noise model for SiGe HBT device and an analytical expression for input referred noise. It is possible to include the cascoded device's noise model into the

final equation, however, the cascode transistor Q_2 has a current gain of 1 and this forces the current coming into the emitter of Q_2 to equal the current coming out of the collector of Q_2. Therefore a noise current source between the collector and the emitter does not change output noise [21]. Therefore, the cascode device can be treated as a noiseless network connected to a noise common-base stage.

Figure 3.9 shows the small signal and noise model of a SiGe HBT transistor. This model can be used to derive the minimum noise figure as well as Γ_{opt}. From [22], the theoretical equations for noise related parameters are given below. R_n is noise resistance, Y_{sop} is the optimal source impedance for noise matching, F_{min} is the mininum noise figure, and Y_{xy} is the Y parameter of the noiseless two-port network.

$$R_n = C_{A11} \tag{3.25}$$

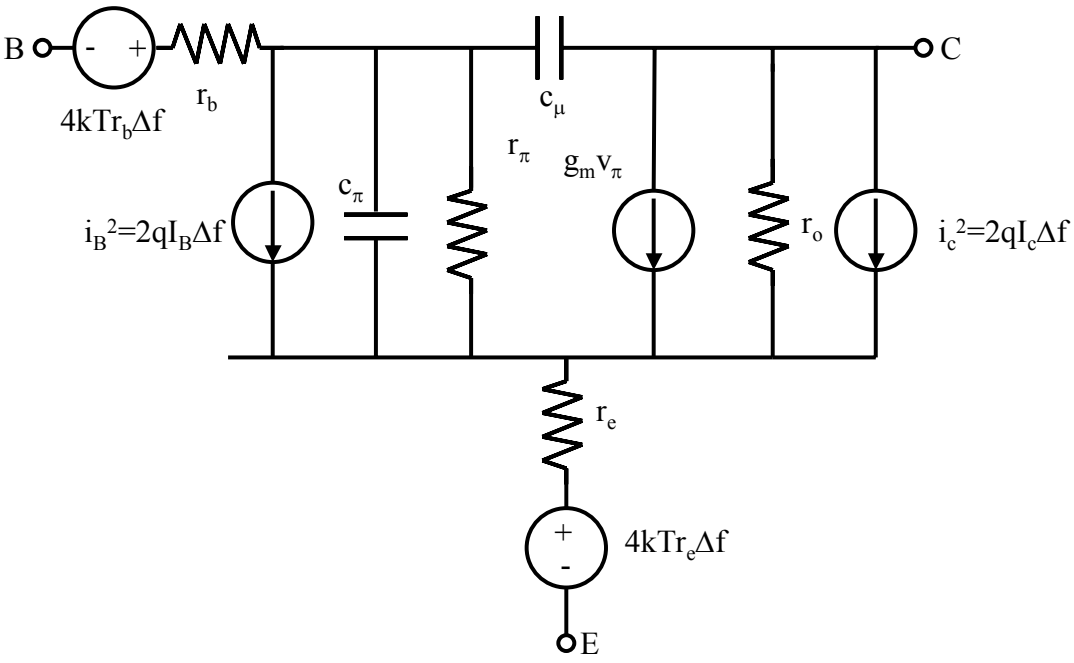

Figure 3.9 Noise model for SiGe HBT

$$Y_{sop} = G_{sop} + jB_{sop} = \sqrt{\frac{C_{A22}}{C_{A11}} - (\frac{\mathrm{Im}\{C_{A12}\}}{C_{A11}})^2} + j\frac{\mathrm{Im}\{C_{A12}\}}{C_{A11}} \tag{3.26}$$

$$F_{MIN} = 1 + 2(\mathrm{Re}\{C_{A12}\} + C_{A11}G_{sop}) \tag{3.27}$$

$$C_{A11} = \frac{\overline{v_n^2}}{4kT\Delta f} = \frac{\overline{i_c^2}}{4kT\Delta f \mid Y_{21} \mid^2} + (r_E + r_B) \tag{3.28}$$

$$C_{A21} = C_{A12}^* = \frac{\overline{v_n^* i_n}}{4kT\Delta f} = \frac{Y_{11}\overline{i_c^2}}{4kT\Delta f \mid Y_{21} \mid^2} \tag{3.29}$$

$$C_{A22} = \frac{\overline{i_n^2}}{4kT\Delta f} = \frac{\mid Y_{11} \mid^2 \overline{i_c^2}}{4kT\Delta f \mid Y_{21} \mid^2} \tag{3.30}$$

In these substitutions, i_{c2} is the shot noise due to collector current and i_{B2} is the shot noise due to base current. r_E and r_B are internal emitter and base resistance respectively. With all the parameters in place, the general equation for Y_{sop} can be derived.

$$\begin{aligned} Y_{sop} = & \sqrt{\frac{I_B \mid Y_{21} \mid^2 + I_C \mid Y_{11} \mid^2}{2V_T \mid Y_{21} \mid^2 (r_E + r_B) + I_C} - \left(\frac{I_c \,\mathrm{Im}\{Y_{11}\}}{2V_T \mid Y_{21} \mid^2 (r_E + r_B) + I_C} \right)^2} \\ & - j\frac{I_C \,\mathrm{Im}\{Y_{11}\}}{2V_T \mid Y_{21} \mid^2 (r_E + r_B) + I_C} \end{aligned} \tag{3.31}$$

$$F_{MIN} = 1 + \frac{I_C}{V_T \mid Y_{21} \mid^2} \left(\sqrt{\left[1 + \frac{2V_T \mid Y_{21} \mid^2 (r_E + r_B)}{I_C} \right] \left[\mid Y_{11} \mid^2 + \frac{I_B \mid Y_{21} \mid^2}{I_C} \right] - \left(\mathrm{Im}\{Y_{11}\} \right)^2} + \mathrm{Re}\{Y_{11}\} \right) \tag{3.32}$$

Equation (3.31) gives the relationship between Y parameters of a two-port network and the optimal source impedance. As discussed earlier, the ideal case is when $Z_{sopt} = Z^*_{in}$. But with the above equation, it is difficult to directly use it to find the optimal

matching point. Y_{sop} can be transformed to Z_{sop} where it consists of a real and imaginary part. The process of this transformation is omitted because it is purely mathematical manipulation. The result of this transformation is that the real part of Z_{sop} scales with the inverse of emitter length and decreases with increase in frequency.

Another observation from this transformation the relationship between the sign of the imaginary part of Z_{in} and Z_{sop} can be derived relative to each other. To have a good noise match, those two imaginary parts need to have opposite signs. Mathematical manipulation of the expressions gives that S_{11} of the two-port network needs to remain in the left half of the Smith chart.

The main problem with (3.31) is that S_{11} of a SiGe HBT device is related to Z_{sop}. From optimization point of view, this is the worst case because with so many variables involved and many circuit specs to meet, completely correlated circuit parameters are difficult to be simulated or solved independently. A designer usually have limited resources on simulation and it is reasonable only if there are two or three variables to be simulated at the same time. Therefore it is important to devise a way so that the two parameters become less correlated or uncorrelated. In this particular case, an emitter degenerated inductance is sought to provide this desired property.

Figure 3.10 shows the input stage modified but an emitter degeneration inductor. Ideally this inductor does not add additional noise, therefore the minimum NF is not affected. With the addition of the degeneration inductor, the new input impedance becomes

$$Z_{in} = r_{b1} + \frac{r_{\pi 1}}{1 + j\omega r_{\pi 1}[c_{\mu 1}(1 + \frac{g_{m1}}{g_{m2}}) + c_{\pi 1}]} + j\omega L_e \qquad (3.33)$$

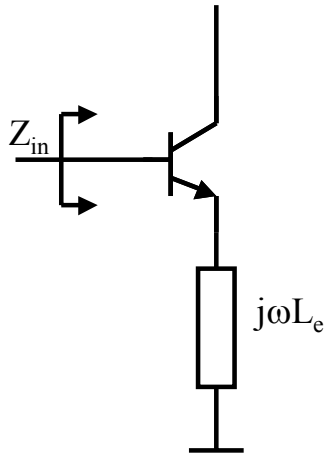

Figure 3.10 Emitter degenerated input stage

L_e directly influences the imaginary part of the input impedance only. It can also be demonstrated that L_e only changes the imaginary part of Z_{sop}, leaving the matching of the real part for other circuit parameters. Given the difficulty in solving the equations for a pure quantitative solution, computer simulation is needed to find the exact solution for optimal bias point and device sizes for low noise operation. The derivation above provides the first qualitative understanding of matching requirements.

(3.31) and (3.32) predict that noise figure is a function of bias current and device size. It is useful then to use a sample device constructed in the cascode configuration to illustrate the influence that those parameters have on device noise performance. Figure 3.11 shows the effect of sweeping L_e, the emitter degeneration inductance from 0 to 1 nH, on Γ_{sop} and Γ_{in} for a transistor biased at 1 mA with emitter length at 0.12 μm and width at 2.4 μm. The circuit is simulated at 40 GHz. As indicated by previous derivation, L_e enables a more flexible matching optimization for Γ_{sop} and Γ_{in}. Γ_{in} changes more rapidly than Γ_{sop}, which facilitates matching.

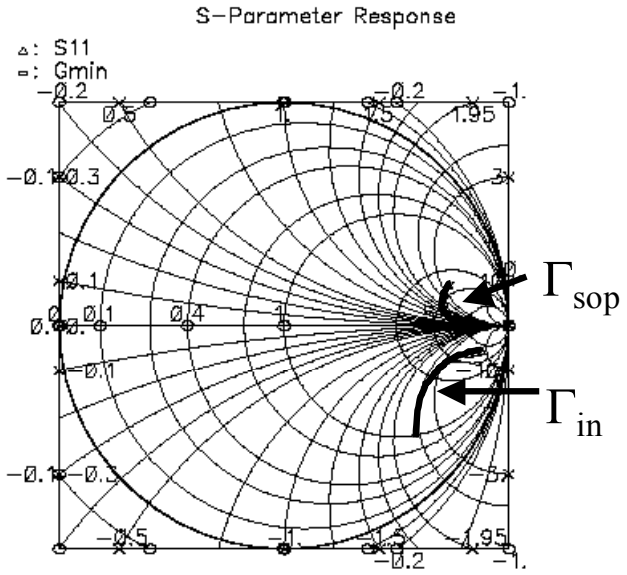

Figure 3.11 Effect of sweeping degeneration inductance

Figure 3.12 shows the effect of device geometry and bias current on minimum

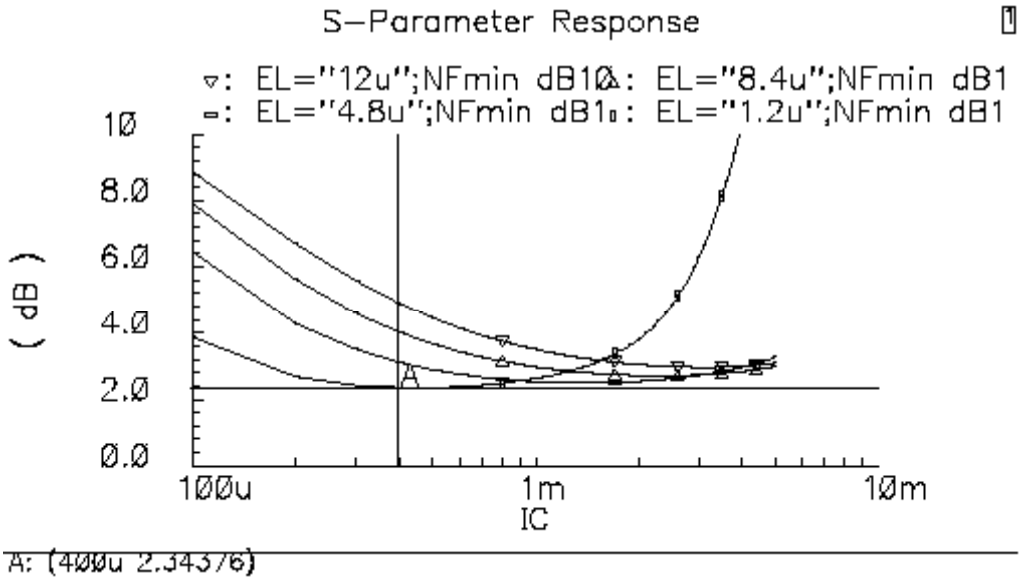

Figure 3. 12 CE stage device size and bias current on NF_{min}

noise figure. Various devices are chosen and the x-axis shows the bias current. It is interesting to note that for each device size, there exists a range for bias current to have a relatively constant minimum noise figure. When bias current is too little, a transistor does not have enough current gain to offset the internal noise. When bias current is too large, base and collector shot noise dominates and noise figure goes up abruptly. Another fact revealed by Figure 3.12 is for this particular process noise due to base resistance is not a dominant noise source. Theoretically base resistance is a function of emitter length. As emitter length increase, base resistance goes down due to larger area to carry current. In this plot, the smallest device has the lowest noise figure, which proves the fact that noise power due to base resistance is small.

The above discussion has concentrated on common-base cascode configuration for low noise amplifier. The other suitable topology which uses common base as the first gain stage can be analyzed in a similar way. For simplicity reasons the equations are not given here. Simulation with the same device size and bias current for minimum noise figure in Figure 3.13, however, shows that for the same device size

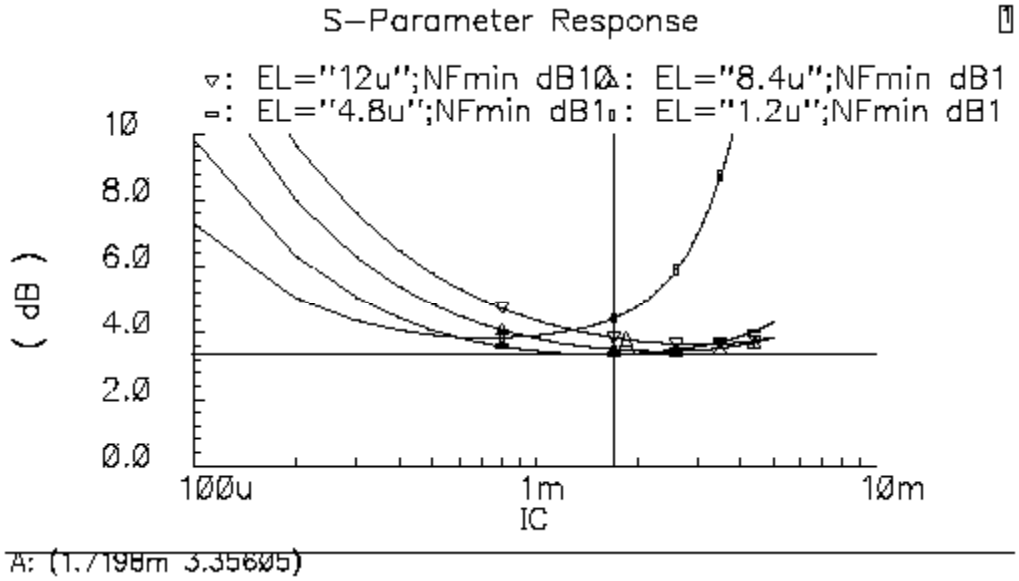

Figure 3.13 CB stage device size and bias current on NF_{min}

and bias current, the common base configuration has a higher minimum noise figure. This is mainly due to the fact that collector shot noise directly appears at the input whereas in the common emitter case, it needs to be transformed to the equivalent noise source. In doing so, the transconductance gain needs to be removed to reflect the fact that the real noise source is not at the input.

In terms of matching for optimal noise and power, the common base configuration is harder to achieve because there is no similar leverage such as L_e in the common emitter case that can change one parameter a lot more effective than others, which simplifies optimization tasks. But given the fact that common base input stage has a low input impedance, matching to 50 Ω is relatively easy.

3.3.3 Circuit Optimization

Given the previous discussions on circuit topology trade-offs and matching considerations, a general procedure for circuit optimization is outlined. A topology is chosen first according to the frequency and specific design requirements. At millimeter frequency range there are not many options since additional devices will add more noise and some topologies that rely on feedback are vulnerable to many parasitic effects that can change the loop dynamics. Once a topology is fixed, the next step would be to adjust device sizes and bias current, as those two parameters have the most dominant effects on noise and power match. In the case of common-base input stage, the use of emitter degeneration inductance decouples otherwise strongly correlated circuit parameters and thus simplifies optimization tasks. However, in the case of common-base configuration, minimum noise figure is higher and optimization is more difficult. This optimization process involves simulation over different device sizes and bias currents until a simultaneous match is found.

3.4 Physical Layout Considerations

In RFIC design, a good circuit on schematic is only the first step. A poorly designed layout can easily ruin a circuit that has good simulation results. In order to have a successful silicon chip, a designer has to pay attention to various components during layout. For MM Wave IC design, many issues are unique because the wavelength of the signal approaches the dimensions of circuit components, thus demanding more rigorous layout disciplines.

Most RF circuitry does not involve many transistors in the design. In addition, the presence of passives requires large space to be dedicated to those space-hungry components such as inductors and transmission lines. As a result, devices from different gain stages tend to be isolated from each other. It is a common practice to have the shortest distant from the input pad to the output pad so that unwanted interference or parasitics can be avoided.

Substrate contacts are very crucial in isolating active devices and reducing cross-talk. There have to be substrate contacts around sensitive components to maintain a good ground. A good practice is to arrange a network of substrate contacts and make a large ground plane that covers as much space as possible on-chip with substrate contacts connected to this large ground.

Vias are also important in that the actual length of a via or vias can approach a large fraction of the wavelength. If unaccounted for, it will change measurement data and make simulation results less accurate. In a typical SiGe process the distance from a top layer metal, usually thick metal with good conductivity and small ground capacitance, to the device is approximately of 10 μm. For a signal at 100GHz a quarter λ on-chip is roughly 400 μm. With both vias needed to get signal up to the top layer metal and down requires 20 μm of distance, 5% of a quarter wavelength. As

signals travel along the path, if vias are not accounted for, the errors in the end will add up and causes simulation to deviate quite significantly from actual results.

Pads are usually designed to be small so that they do not take on too much capacitance to the ground. But in real testing environment, pads are usually de-embedded so that the effect of pads is negligible. However, the section that connects a pad to an actual circuit element usually is not accounted for, because for a de-embed procedure to work properly, pads are arranged in short, open and load positions, which does not require the pad to mimic the real design. Since the extra bridge between pad and a component can be implemented in transmission line a lot of uncertainty can be taken out by trusting robust transmission line modeling.

The next concern is transmission line. With a standard shape (CPW with ground plane), it is fairly easy to produce accurate models for any dimensions of transmission lines. When a bend is needed due to space conservation, it can usually be modeled as a regular straight transmission line with modified length. For a T-junction simulation shows that it is reasonable to assume the transmission line model is accurate for each branch of a T-junction. The grounds of all transmission lines are connected and occupy a large area to reduce resistance and inductance on the return path. Unfortunately this is usually not the case.

Sometimes for MM Wave IC that occupies the lower end of the spectrum, transmission lines may prove to be too costly because wavelengths are increased. In this case, line inductor or even spiral inductors are used. Those components see more open space on-chip and the chances of having magnetic coupling is greatly enhanced. In this case it is a good practice to keep those exposed passives as far away as possible.

3.5 Integrated Simulation Considerations

3.5.1 Proposed Parasitic-aware MM Wave IC Design Flow

The traditional circuit design flow usually starts with circuit simulation, and then schematic is drawn on a layout cell. The layout cell is extracted and compared to the original schematic to make sure all the connections are correct. Extraction also adds parasitics on the interconnect to the netlist. Simulation on the complete netlist will finally verify the circuit performance.

In MM Wave IC design, this flow needs to be modified because parasitics become an important part of matching network and often alter the performance of the schematic by a large margin. A new design flow is proposed here to give full considerations for the effects that parastics have on circuit performance. Figure 3.14 show the new proposed design flow. Schematic design begins with active devices and passives that are part of the chosen topology. Only certain parameters of those elements will be changed over the course of optimization. Since those elements tend to be well defined, i.e., transmission lines and pads that already have an accurate

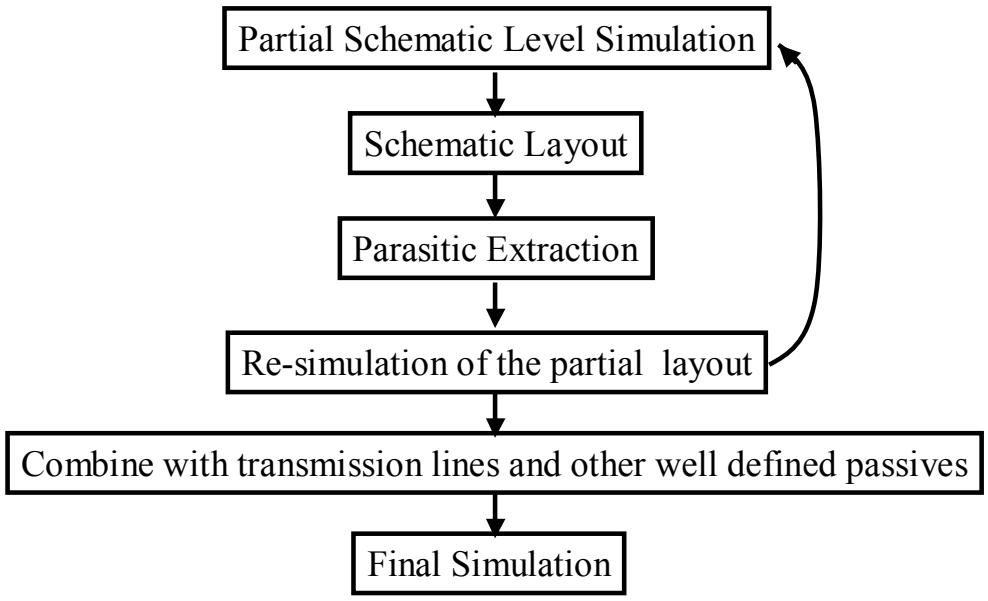

Figure 3.14 Proposed parasitic-aware MM Wave IC design flow

simulation model, they are treated as part of the "known" elements.

The "unknowns" are the interconnects that link the "known" elements. Since interconnects are extracted by the provided extraction deck generated at the foundry, designers do not have much control over the accuracy of the extraction results. However, if the extraction method is reasonably accurate, the design flow emphasizes on the effect of interconnects on schematic simulation by breaking the circuits down to several pieces. Each piece contains some closely placed active elements and interconnects connecting those elements. The extraction deck then extracts the parasitics that exist among the active devices and back annotate them back to the schematic. After all the pieces are laid out and extracted, the schematic simulation now becomes a pseudo-post-layout extraction simulation because parasitic information is already contained in the simulation. With added parasitics, some circuit parameters need to be modified and a new version of the schematic needs to be laid out. This is an iterative process and each time device parameters are altered, layout dimensions may have to change and thus new extraction is needed. However, if the original extraction contains elements that are relatively stable in position relative to each other, the iteration process can be shortened.

While simulation on active device coupled with layout generated parasitics is an iterating process, some foresights into the chip layout process can save tremendous amount of simulation time. For example, in the situation where three transmission lines are to be joined together, thus creating a T junction, given transmission line models do not have a specific model for this particular case. Therefore it is necessary to run some EM simulation to generate some standard P-cells to cover this case. With a T-junction model, whenever 3 transmission lines meet, it can be directly applied to the schematic simulation without ever going to the layout stage to determine its proper S parameter values.

3.5.2 Evaluation of Extraction Deck

Since devices at high frequencies are sensitive to parastics, accurate extraction of those elements is critical to the design process. Well-defined structures such as inductors or transmission lines are not extracted by the extraction deck, since simple extraction rules cannot completely capture the EM wave propagation around the structure. However, [23] gives a uniform approach to high frequency extraction of those well-defined structures. The advantage stated in [23] is that it is formulated with relatively simple forms and if simulation speed is a concern, the use of these models will reduce simulation time.

Extraction deck performs extraction on relatively simple structures such as interconnects. Extracted values include R, C, and sometimes L if it is sophisticated enough. In order to have confidence in the extraction deck, several corner test cases are proposed here to explore the limits of those decks. Since most of the extraction decks are from foundries where information on specific rules are strictly proprietary, the cases proposed here are independent of specific rules and can be applied to any deck.

For resistance extraction, several cases are given below to evaluate the accuracy of the deck. In model silicon process via resistant approaches roughly one

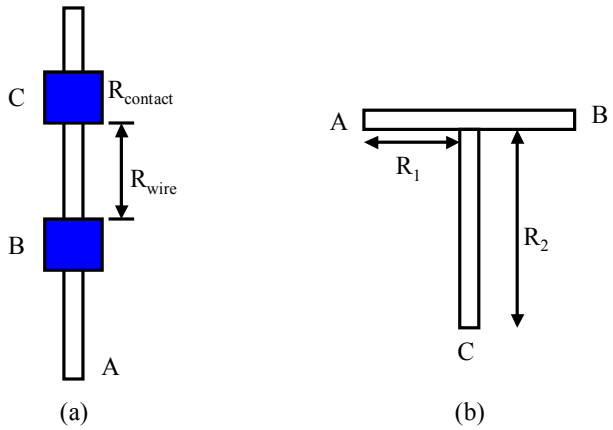

Figure 3.15 Cases to test R extraction deck

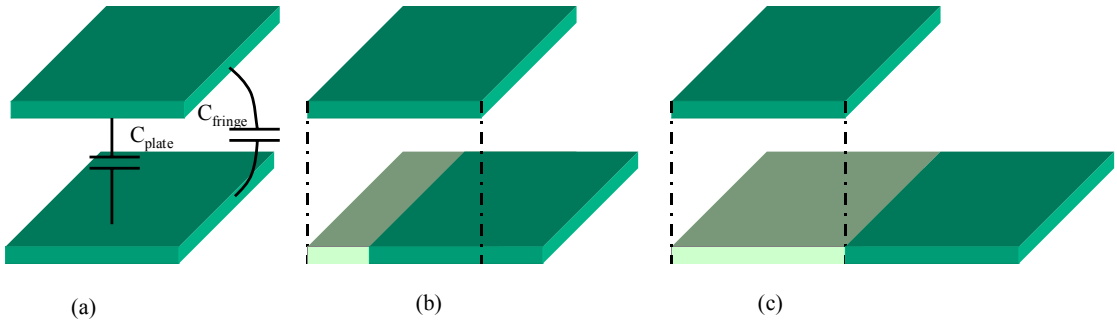

Figure 3.1617 Capacitance extraction evaluation

square metal on the same level. Accurate R extraction must be able to extract via resistance. For the case in Figure 3.15 (a) the resistance from A to C has to include the metal resistance from A to C as well as the via resistance down to C. In Figure 3.15 (b) the extraction deck has to be able to correctly break down the metal resistance from A to B and add R_1 and R_2 for resistance between A and C.

Capacitance extraction is more difficult to evaluate. However, some general principles of capacitance can be used to quickly identify exaggerated capacitance extraction. Consider the case in Figure 3.16. Figure 3.16 (a) shows a perfectly aligned parallel plate structure where there are two well-defined capacitances – the place capacitance C_{plate} and the fringe capacitance C_{fringe}. Figure 3.16(b) shows the two plates are offset by a finite distance where they are partially overlap. In this case the capacitance extracted should still consist of C_{plate} and C_{fringe}, with smaller value for each one. In Figure 3.16(c) there are a complete offset between the two plates and the capacitance should only be the C_{fringe}. When evaluating the extraction deck, case (b) should present a capacitance that is close to be at a mid point between that of (a) and (c) on a first order analysis. However, if there is a large discontinuity for case (b), caution has to be taken to avoid such partially overlapping parallel plate interconnects.

For inductance extraction, it is even more difficult to evaluate since it strongly depends on surrounding structures as well as metal above and below. But

interconnects between closely placed actives devices tend to be short and much less than wavelength, so it can usually be ignored without sacrificing accuracy.

3.5.3 Evaluation of EM Simulation Results

With the emergence of myriads of EM software on the market and ever-powerful functionality, it becomes easier to integrate EM simulation into the overall circuit simulation into the design flow. Products such as HFSS from Ansoft Corporation or Sonnet from Sonnet Software offer a simulation environment that integrates directly into a layout tool in Cadence or ADS.

EM simulation is the ultimate tool to determine a passive structure's response under a wave excitation, but the setup usually is more difficult and error-prone. To evaluate the correctness of a particular setup, basic transmission line structure can be drawn using circuit CAD tools. Then the structure can be imported to the EM tools for S parameter extraction. If the input and output ports are set up correctly, the simulated S parameters should match that of the model coming from the foundry, where not only EM simulation but actually measurement data are used to guarantee the model robustness. With confidence in the EM simulation setup, many structures in the layout environment can be imported for a thorough frequency sweep. Secondary effects such as skin effect and proximity effect will be taken into account, yielding parameters that faithfully reflect reality.

3.6 Conclusion

In this chapter, a general approach to the design of MM Wave IC is discussed. Circuit topology, optimization, matching, layout and simulation issues are presented and a novel approach that incorporates all aspects of high frequency design is proposed. This design approach is illustrated in the following chapters with real design examples.

Chapter 4: 94 GHz Receiver Front-end Circuits in SiGe

4.1 Overview

FCC has recently opened up spectrum from 92 GHz to 95 GHz range [24]. This band is included in the licensed E-band allocation. The small wavelength at this frequency range enables very fine spatial resolution, therefore many commercial applications such as automotive radar, industrial process control, and imaging sensor can be deployed to achieve a level of precision and stability unparalleled by infrared, ultrasonic, video and laser sensors. It also provides an opportunity for various security applications, such as airport screening, provided privacy rights are maintained [25]. In addition, short-range wireless data communication can also use this spectrum to send high bandwidth data, further opening up potential market for technologies targeted at this spectrum. Current research has concentrated on system level and component level radar design in this frequency. [26] presents an FMCW radar operating at 94 GHz in HEMT technology. [27] presents a mono-pulse radar at 94 GHz in GaAs technology. There is also a VCO designed for 77 GHz and 94 GHz applications in InP [28]. Before the breakthrough of SiGe technology with 200 GHz of f_t, MMWIC is dominated by the traditional III-V process. They provide a low loss substrate and higher electron mobility but integration with the rest of the silicon is impossible. The advent of advanced SiGe process enables radars to be designed entirely on Silicon, which enables future integrations with CMOS digital components and lower unit cost. In the future, it can be predicted that demand for cheaper but ultra-fine resolution radar

as well as high bandwidth wireless transceiver will make Silicon based system far more competitive than its III-V counterparts.

Regardless of different type of applications, either radar or wireless data communication system, some components are fundamental building blocks that maintain their functionality from system to system. Such fundamental building blocks include LNA, balun and mixer. Because of their universal presence, this chapter discusses the design of a 94 GHz LNA/Balun and a direct conversion mixer.

Chapter 2 describes the limitations that a designer has to face to successfully design a circuit in MMW range. Chapter 3 proposes some general solutions to solve problems inherent in the design. In this chapter, those general solutions are applied to specific design problems posed by specific design requirements. Simulation as well as some of the measurement results are presented to validate those proposed general design principles.

4.2 94 GHz LNA/Balun

4.2.1 Circuit Design

The LNA/Balun provides signal amplification to suppress noise for subsequent stages. Depending on the next stage, the LNA/Balun structure can have a single-ended or differential output. The Balun is implemented by a passive Marchand balun

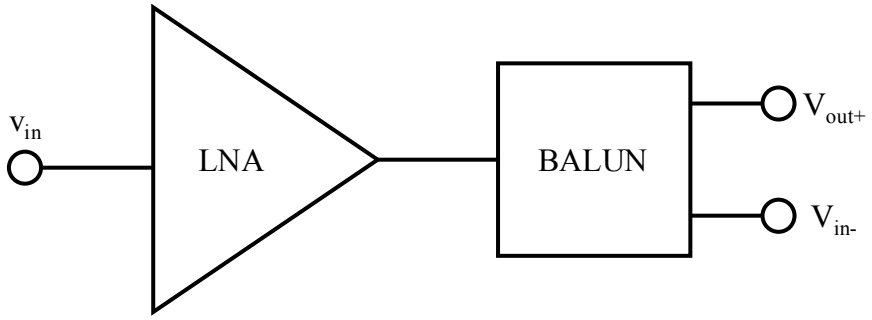

Figure 4.1: LNA and Balun block diagram

structure. Figure 4.1 shows the block diagram of the LNA and the Balun.

Before delving into the details of circuit design, there are some unique properties that 94 GHz band possess for chip design. At 94 GHz, the quarter λ for a 50 Ω transmission line is 430 μm, well within the dimension of a typical chip layout. λ/4 is an important dimension because in microwave theory, a λ/4 section of a transmission can move a point by 180° on a Smith chart. Mathematically the impedance looking into a λ/4 section terminated by a specific load R_L is

$$Z_{in} = Z_1 \frac{R_L + jZ_z \tan \beta l}{Z_1 + jR_L \tan \beta l} \tag{4.1}$$

where Z_1 is the characteristic impedance of the transmission line, $\beta = 2\pi/\lambda$, $\beta_l = \pi/2$ [29]. The resulting input impedance is

$$Z_{in} = Z_1^2 / R_L \tag{4.2}$$

What this implies is for a shorted λ/4 section, the impedance looking into the input of the transmission line is infinity, and for an open λ/4 section it becomes a short. This provides a convenient way of biasing a device and helps with matching.

Even though common-emitter cascode configuration provides a better noise performance over common-base configuration, biasing at 94 GHz is not a trivial task. Common-emitter amplifier needs to be biased at the base, which implies that a high impedance is needed when looking into the bias circuitry at 94 GHz while at DC the impedance drops to zero. For low frequency RFIC this is usually done by inserting a large inductor at the bias line so that at high frequency the bias input impedance is large. At 94 GHz this could be achieved by inserting a 430 μm transmission line at the base and terminate the other end with a large capacitor. However, the internal resistance associated with the transmission line will make the current bias less accurate. For example, for a process where sheet metal resistance is 30 mΩ and transmission line metal width is 2 μm, the total nominal resistance for a 430 μm long

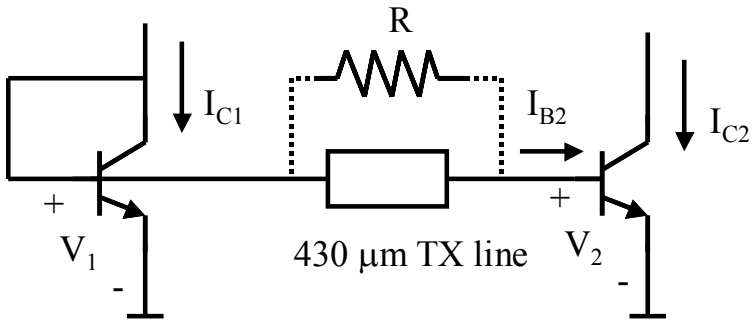

Figure 4.2: Biasing scheme for common emitter configuration.

line is $430/2 \times 30m\Omega = 6.45\Omega$. Figure 4.2 shows a typical biasing configuration with parasitic resistance associated with the transmission line. To calculate the inaccuracy of bias current caused by this extra base resistance R, the ration of two currents I_{C1} and I_{C2} is given as

$$\frac{I_{C1}}{I_{C2}} = e^{\frac{V_1 - V_2}{V_{TH}}} = e^{\frac{6.45\Omega \cdot 0.05mA}{26mV}} = 1.012, \qquad (4.3)$$

assuming I_{C2} = 5 mA and I_{B2} =0.05 mA. This shows a 1.2% of error for a nominal case. If process variation causes metal to deviate its nominal width and temperature of the chip rises, the transmission line can have significant higher resistance and introduces much more error than the nominal case.

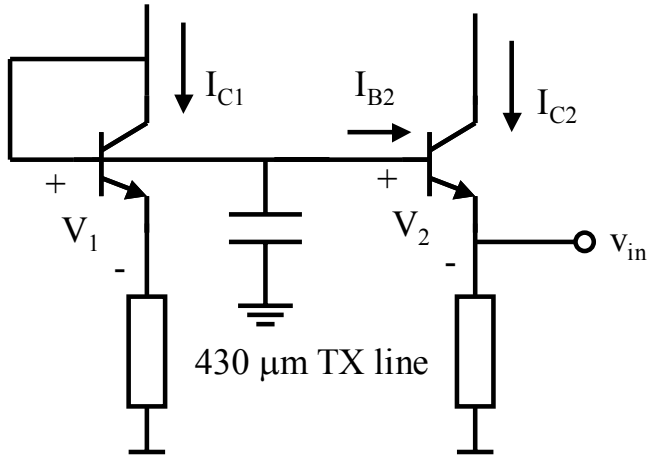

Figure 4.3: Biasing scheme for common-base

To solve this biasing error, common base cascode configuration is used instead as in Figure 4.3. Even though the noise figure a bit higher for similar bias current and device size, this type of circuit topology can have much better current accuracy than the common emitter case. To illustrate this point, Figure 4.3 shows the bias circuitry along with a common base connection. Here I_{C2} fully is decoupled from parasitic resistance.

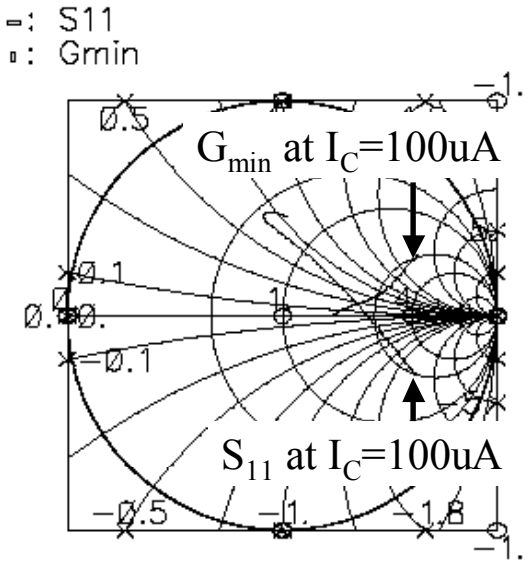

Figure 4.4: G_{min} and S_{11} versus I_c

Since it is difficult to have an exact solution for simultaneous power and noise match, simulation is used to obtain some insight into the connection between different circuit parameters and noise and power match. For a test setup that has common base and cascode connection, bias current and emitter length are swept to obtain optimal source and input reflection coefficient. Figure 4.4 uses 2.4 μm devices and *Ic* is swept from 0.1 mA to 5 mA. At low bias current, G_{min} and S_{11} achieves simultaneous match but as current increases, S_{11} changes more rapidly than G_{min}. This is to be expected because for common base connection the strong noises sources such as collector shot noise can see input directly. Changing current merely changes the power of noise.

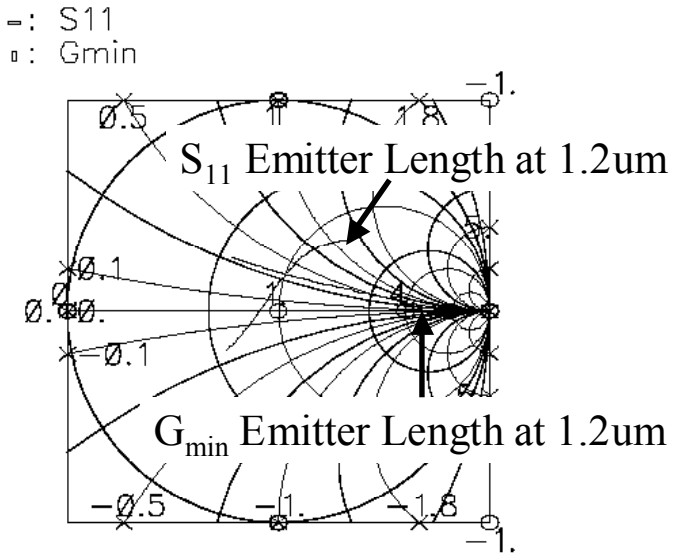

Figure 4.5: G_{min} and S_{11} versus emitter length

Figure 4.2 shows G_{min} and S_{11} when emitter length is swept from 1.2 μm to 12 μm while collector current is fixed at 1mA. When emitter length is at its maximum, it achieves simultaneous noise and power match. When emitter length gets smaller, the match gets worse. The correlation from Figure 4.4 and 4.5 indicates that bias current and emitter length are correlated in terms of noise match. The current density J_C should be used as a parameter to determine noise and power match.

For device emitter length at 2.4 μm, NF_{min} is plotted with I_C. The minimum

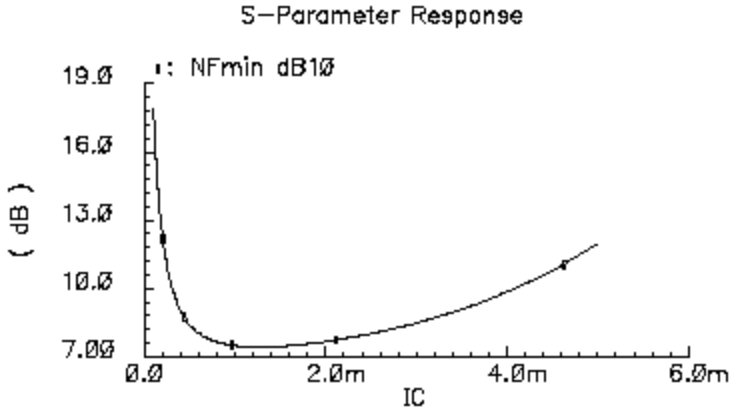

Figure 4.6: NF_{min} verus I_C

NF exists for I_C = 1mA, which corresponds to a current density of 1 mA/2.4 μm = 0.42 mA/μm. However, Figure 4.4 and 4.5 shows a simultaneous power and noise match at current density much lower than 0.42 mA/μm. For this particular example, this means that either simultaneous power and noise match is sacrificed or minimum NF is raised. Since the ultimate goal is to have an overall low NF, further optimization needs to be carried out to find a balance between the two.

Once the optimal device size and bias current is found for noise and power match, according to the design flow discussed in chapter 3, initial layout needs to be carried out so that partially back-annotated parasitic values will join the simulation to make it more realistic and save design iterations later on. In this case, the obvious components for extraction are the two transistors that make the cascode structure. Figure 4.7 indicates the devices are laid out and extracted. Q_1 and Q_2 are closely placed to each other to minimize unwanted parasitics. Vias at the bottom and top are

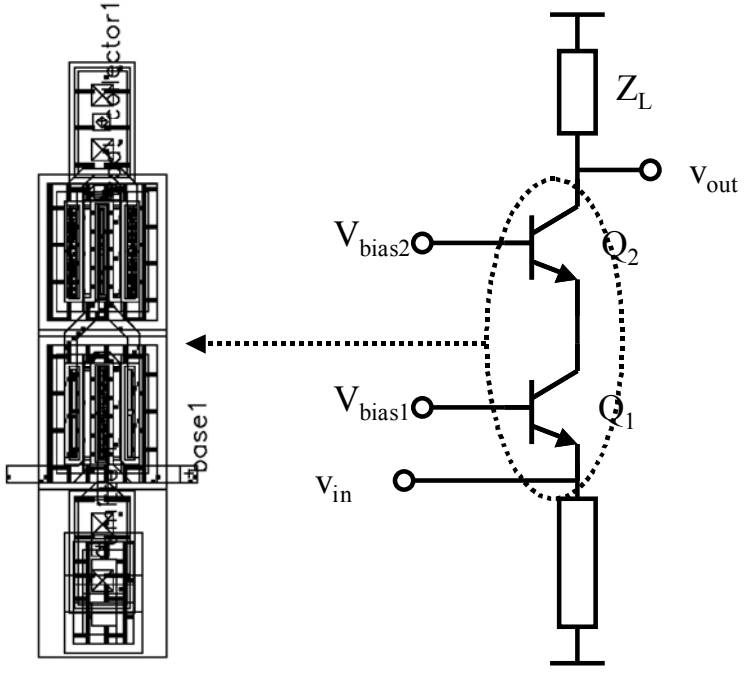

Figure 4.7: Parastic-aware extraction for cascode connection

used to connect to transmission lines at top level metal. This layout is extracted and the back-annotated netlist is sent back to the original schematic to be simulated with other components.

Figure 4.8 shows the complete schematic of the LNA and Balun. Bias network is omitted due to insufficient space. Previous discussions have described one particular bias scheme for the base of a transistor and such scheme is universally used in the design of this LNA.

The LNA consists of two gain stages. The first gain stage includes Q_1 and Q_2. The send stage includes Q_3 and Q_4. C_1 and T_2 are part of the input-matching network to match external 50 Ω resistance. The second stage uses a common emitter cascode configuration because λ/4 transmission line still takes a lot of space and there is no more room for another one. Bias current accuracy may suffer but since it is the second gain stage, less accuracy can be tolerated. $T_{3,4,5,6,}$ and C_2 are part of the inter-stage matching network. Inter-stage matching network does not have to match to specific value as long impedance looking both ways are conjugate of each other. The

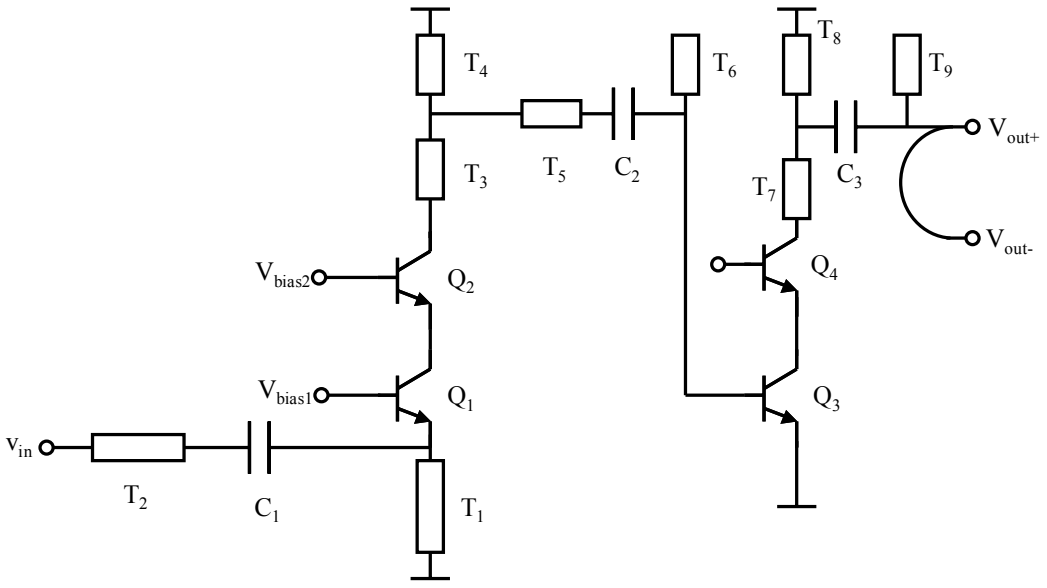

Figure 4.8: Complete schematic of 94 GHz LNA and Balun

placement of $C_{1,2,3}$ also form a DC open to the signal. The whole signal path is AC coupled to avoid DC level change. $T_{7,8,9}$ and C_3 are part of the output matching network that matches to 50 Ω.

Table 4-1 94 GHz LNA device parameters

Device	Parameter and Value
T_1	L=430 μm, W=6 μm
T_2	L=55 μm, W=6 μm
T_3	L=92 μm, W=6 μm
T_4	L=350 μm, W=6 μm
T_5	L=130 μm, W=6 μm
T_6	L=316 μm, W=6 μm
T_7	L=20 μm, W=6 μm
T_8	L=360 μm, W=6 μm
T_9	L=260 μm, W=6 μm
C_1	C=126 fF
C_2	C=126 fF
C_3	C=126 fF
$Q_{1,2,3,4}$	W=0.12 μm, L=5 μm, Ic=3.4 mA

The optimization process for Q_3 and Q_4 is similar to Q_1 and Q_2. The fact that they are at the second stage boosting gain implies optimization target is for high gain but less for noise. That is the reason for no degeneration component at the emitter of Q_3. Devices are biased at the highest f_t for Q_3 and Q_4; therefore the highest possible gain is obtained if properly matched. The design and validation of the passive structures are discussed in later sections.

Marchand Balun is used to split the single-ended signal and output two signals that are equal in amplitude but 180-degree out of phase. The reason to use a passive balun instead of an active one is the difficulty in controlling phase at this frequency. For a common differential pair with one input terminated by a stable ground, if the delay through the transistor whose input is grounded is negligible, then this circuit can achieve a good differential operation. However, every device has intrinsic delay from

input to output. At 94 GHz, the delay for those devices can be significant enough to affect the output phase balance. Another way to look at the unbalance problem is to use common-mode rejection ration (CMRR) to measure signal unbalance [30]. For a perfect balun, if CMRR is infinity, only the differential mode is amplified and the common mode is suppressed. Therefore the output has perfectly balanced signal. However, if CMRR is less than infinity, the differential output will have a common mode component and the balun performance suffers. To link CMRR with gain and phase imbalance, [31] gives the following expression.

$$CMRR(dB) = 10 \cdot \log\left(\frac{1 - \frac{2\alpha}{1+\alpha^2} \cdot \cos(\Delta\varphi)}{1 + \frac{2\alpha}{1+\alpha^2} \cdot \cos(\Delta\varphi)}\right) \tag{4.4}$$

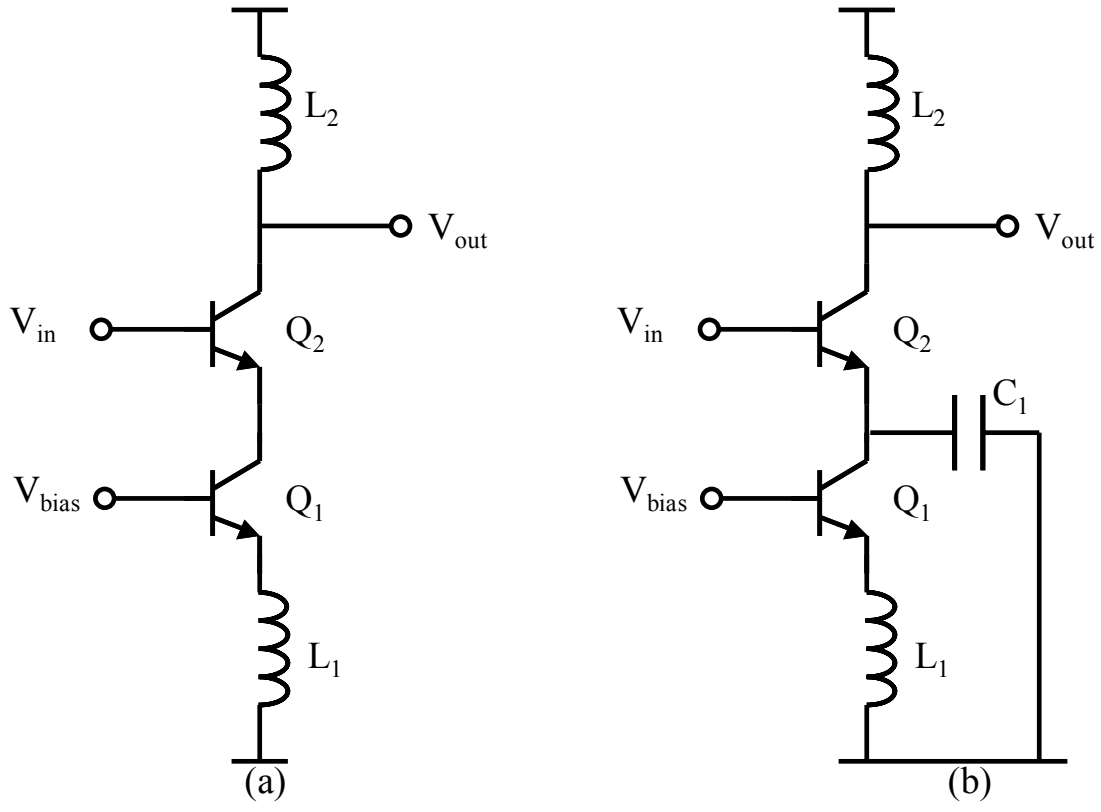

Figure 4.9: CMRR test circuits at 94GHz. (a) CM (b)Differential Mode

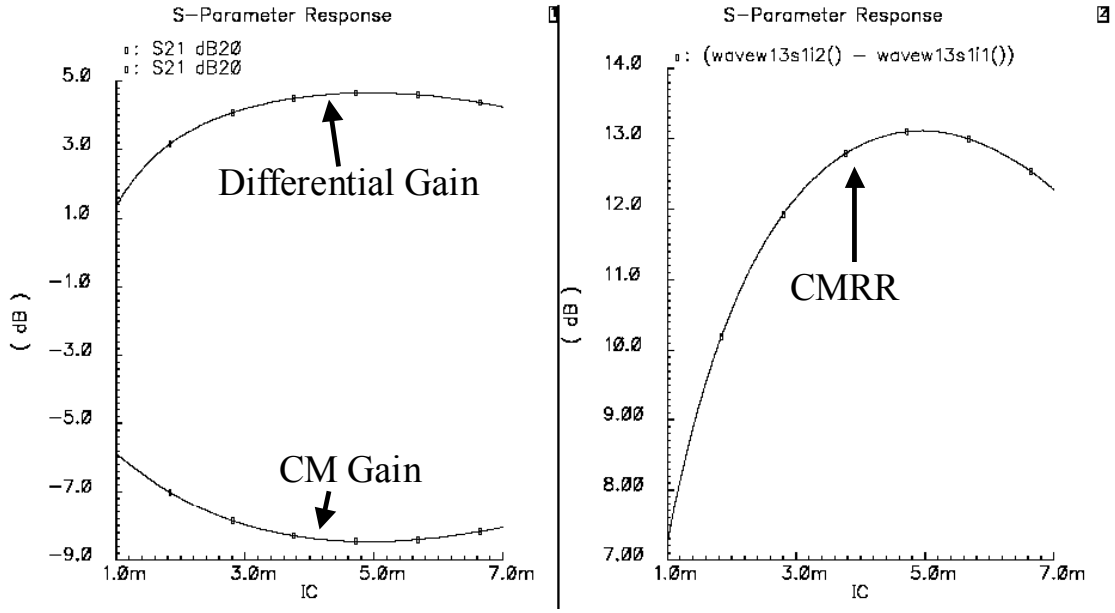

Figure 4.10: CMRR Simulation results

where $\alpha=1+\Delta G/G_1$, and G_1 is one the two single ended gains used as a reference and ΔG is the difference between the two outputs. CMRR at 94 GHz for any differential pair structure is dismal because of various capacitances to the ground and adjacent devices.

To get a rough idea on CMRR for a typical differential pair at 94 GHz, a test circuit is constructed as in Figure 4.9. It uses the half circuit topology of a differential pair to emulate the common mode. For differential mode a large capacitor C_1 (1F) grounds the emitter of Q_2. All the inductors are 1 H to artificially create open nodes. Simulation results are presented in Figure 4.10. Differential gain and CM gain are plotted on the left and the difference – CMRR, is plotted on the right. Figure 4.10 shows a CMRR of less than 13 dB, which is far worse than a low frequency diff pair. A CMRR of 20 dB corresponds to a phase offset of at least 20 degrees [32]. Therefore without going into the actual design, conceptual simulation eliminates the possibility of using active devices as a balun structure. The design of the Marchand Balun is discussed in the following section.

4.2.2 Passive Design

As shown in the schematic in Figure 4.8, there are plenty of transmission lines used in the design. Table 4.1 lists values of all the transmission line dimensions. These transmission lines all have the same characteristic impedance. There are also plenty of T-junctions to join different transmission lines together. In addition, the Balun uses Marchand coupler as a basic structure and the actual S parameters need to be obtained from its layout to accurately reflect its response under wave excitation.

To accurately determine each structure's S parameter response, EM simulation tool HFSS from Ansoft, Inc. is used. HFSS has the capability of transporting layout file from Cadence environment and making it a project file in HFSS, thus saving the trouble of drawing a 3D structure from scratch. In order to understand the layout file from Cadence, a process layer file needs to be defined first. The layer file contains the material and thickness of each metal layer as well as the dielectric in between. Once the 3D structure is drawn in HFSS, input and output ports need to be set up so that waves are correctly excited at each port. The port set up is quite involving and error-prone. A misplaced port can result in a completely erroneous simulation data.

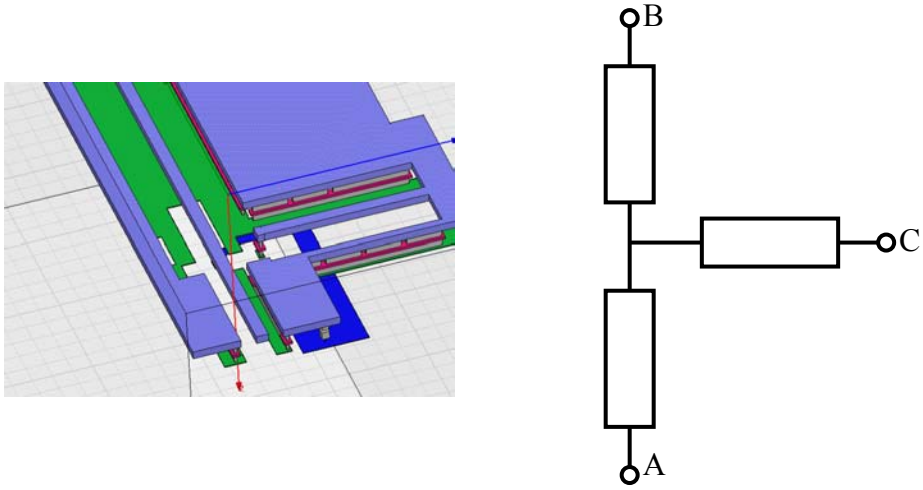

Figure 4.11: T-junction HFSS setup and model

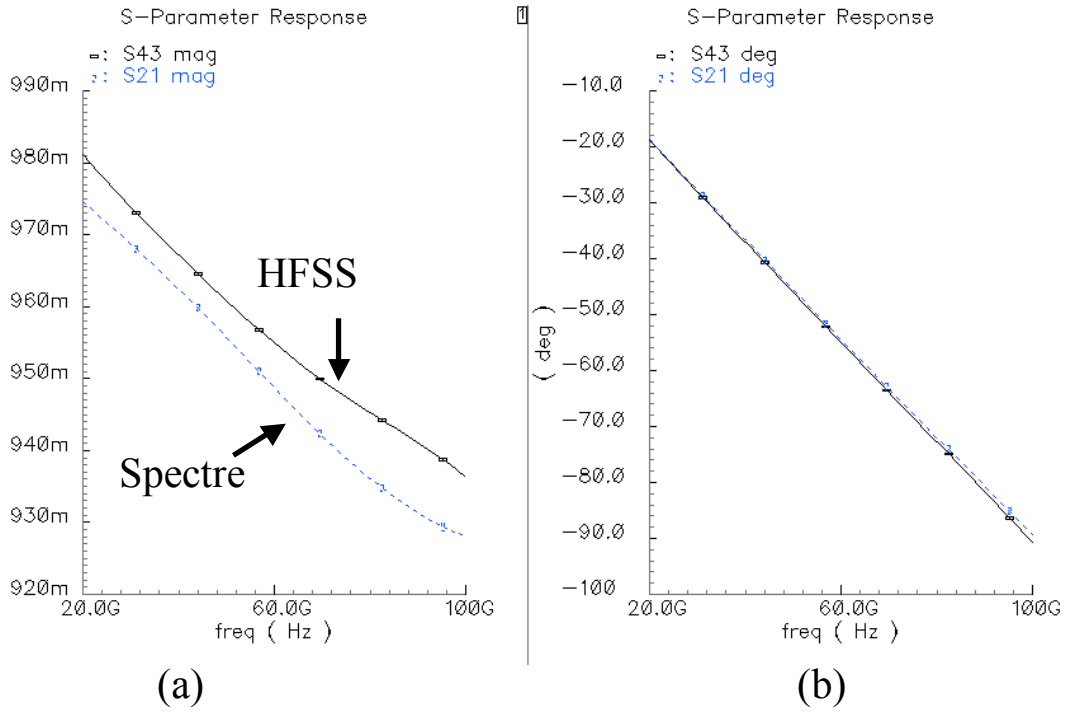

Figure 4.12: Magnitude and phase of S-parameter from HFSS and Spectre

Figure 4.11 gives the T-junction for transmission lines and its equivalent circuit model. The length of each segment of transmission is exactly the same as measured from the intersection point to the edge. Figure 4.12 gives the simulation results for S-parameters from EM and circuit simulation. The results are very close to each other. The notion of S_{21} and S_{43} refers to the same ports. From this simulation it can be safely concluded that T-junction can be modeled as simple transmission lines connected at single point.

Figure 4.13 shows the 3D model of a transmission line in EM simulator. The transmission line is enclosed by a silicon boundary box. The wave excitation port is parallel to the direction of wave propagation and its boundaries touch the ground plane and the center signal line. Effects of vias are also simulated here. Simulation results show that transmission lines are well modeled by the foundry and a single via to the lowest metal introduces 17 pH of inductance.

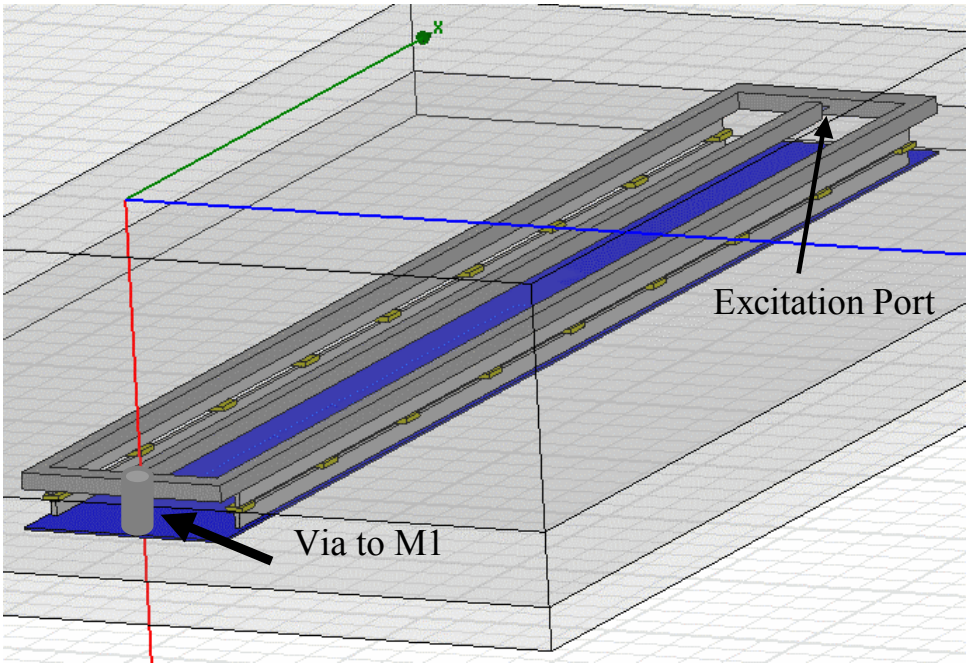

Figure 4.13: Transmission line EM simulation model with vias

Marchand balun is a well-known structure for splitting an unbalanced signal into two balanced ones [33]. The input wave is coupled onto two differently terminated section of transmission lines by which phase is offset by 180 degrees.

Figure 4.13 shows the circuit representation of a Marchand balun. Two segments of differential transmission lines are used. Port 1 is the input port and port 2 and 3 are the output port. The coupling factor C between the two coupled wires can

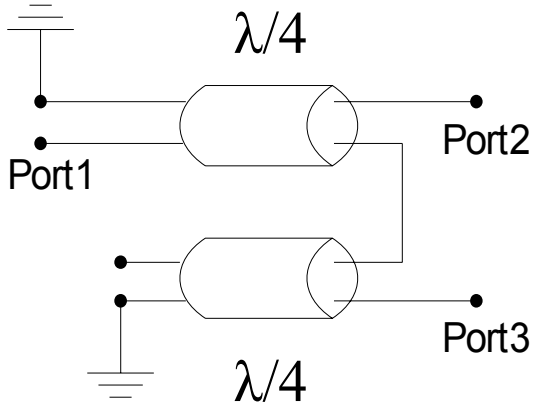

Figure 4.14: Marchand balun circuit model

determine the input and output impedance of the coupler, if simplification is made to assume that the balun is a combination of two identical coupled sections [34]. In order to find the ideal coupling factor C, some mathematically manipulation is needed. The even and odd mode impedance of a coupling line is given by

$$Z_{even} = Z_o\sqrt{\frac{1+C}{1-C}}$$
$$Z_{odd} = Z_o\sqrt{\frac{1-C}{1+C}} \tag{4.5}$$

The optimal C is given by

$$C = \frac{`1}{\sqrt{\frac{2Z_1}{Z_o}+1}} \tag{4.6}$$

where Z_1 is the load impedance to be matched and Z_o is the characteristic impedance of the transmission line coupler. If $Z_1 = Z_o$, the optimal coupling factor C becomes 1/3, which can be achieved by adjusting the distance between the two coupling wires. It has to be noted that a lossless reciprocal three-port network cannot achieve perfect matching on all of its three ports. However, if output port matching is more important, (4.6) provides a simple way of adjusting the coupling factor and achieving satisfactory matching. The layout of the balun is shown in Figure 4.14. Since its transmission line

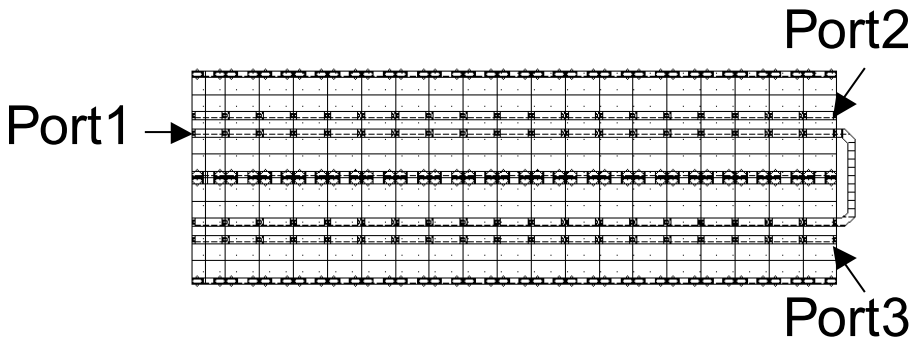

Figure 4.15: Marchand balun circuit model

base coupler and the models are from the foundry, even without HFSS verification the performance of the balun can be accurately estimated.

4.2.3 Layout

There are two gain stages and they are connected by a 150 μm transmission line. The isolation between the two stages should be fairly good given the distance. However, extra caution is taken for each gain stage by padding active devices with deep trench. Deep trench around the devices forms a high impedance guardring . In addition, substrate contacts are extensively used to provide ideal ground in the bulk. The pads are specially designed and have a dimension of 55 μm^2, which is the limit this process technology sets. A smaller pad will introduce less capacitance, and even if de-embedding procedure fails, this added capacitance from the pad should have minimum impact on circuit matching qualities. Figure 4.16 shows the layout with deep trench and substrate contacts strategically placed to reduce noise and crosstalk.

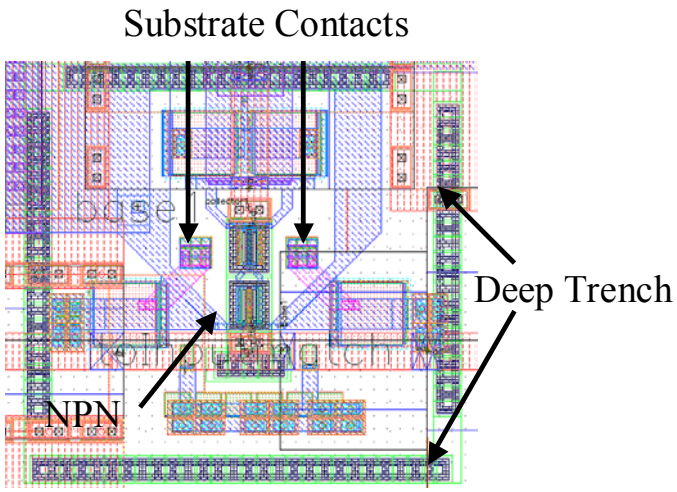

Figure 4.16: Placement of deep trench isolation and substrate contacts

4.3 LNA/Balun Simulation and Measurement Results

The 94 GHz LNA/Balun chip was fabricated in a production SiGe BiCMOS technology with HBT f_t = 200GHz. Most of space is used by transmission lines and the final chip area is 1.1 mm by 0.84 mm. Figure 4.17 shows the die photo. The LNA/balun consumes 8 mA of current with 1.7V of power supply. A current of 8 mA is equally shared by the two gain stages. The simulated S_{11}, S_{21} and S_{31} with magnitude and phase are shown in Figure 4.18. Broadband matching is achieved from 90 GHz to 100 GHz. This is mainly due to some parasitic resistance that reduces the Q of the passive devices. S_{21} and S_{31} have very closely matched input amplitude and near perfect 180-degree phase difference. The circuit also achieves 9.58 dB of noise figure, which is just 0.8 dB above the minimum noise figure in Figure 4.18. Due to testing equipment limitations, only S parameters are measured for this circuit. S_{11} is better than –20 dB and S_{22} is better than –10 dB. However, S_{21} does not show much of a gain and S_{12} is close to 0 dB. One explanation for this could be that some devices

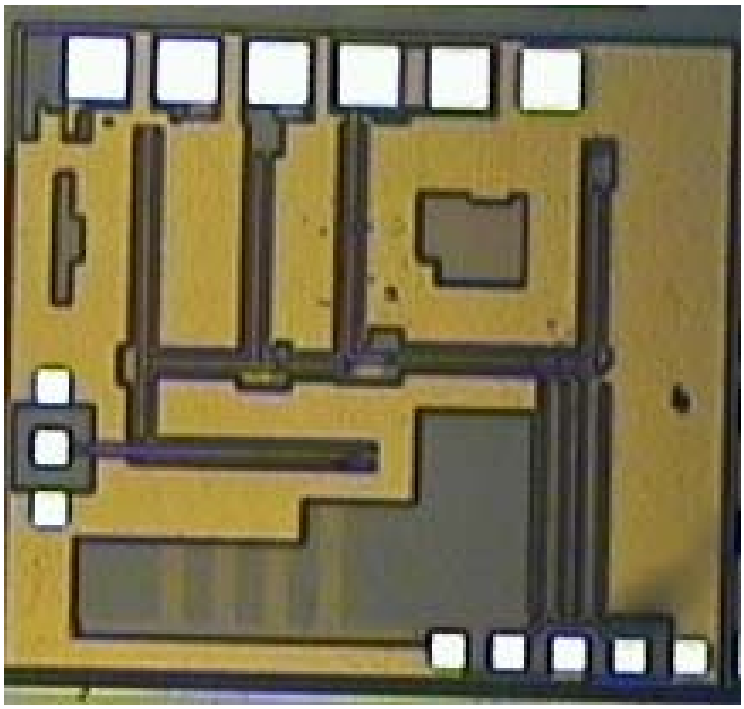

Figure 4.17: LNA/Balun die photo

might not be properly biased.

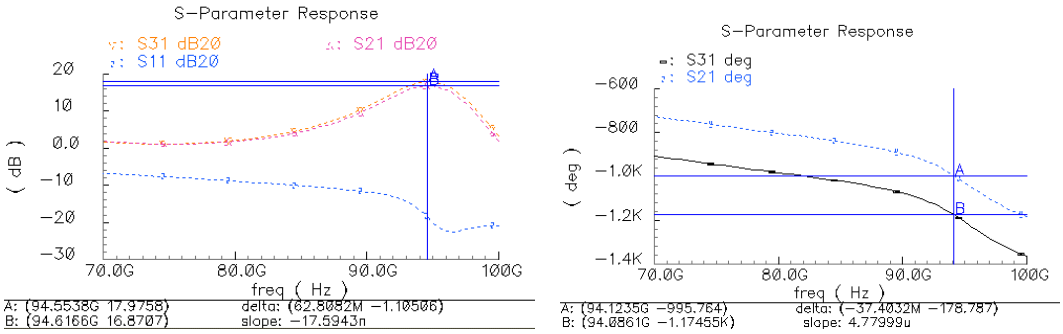

Figure 4.18: S-parameter magnitude and phase

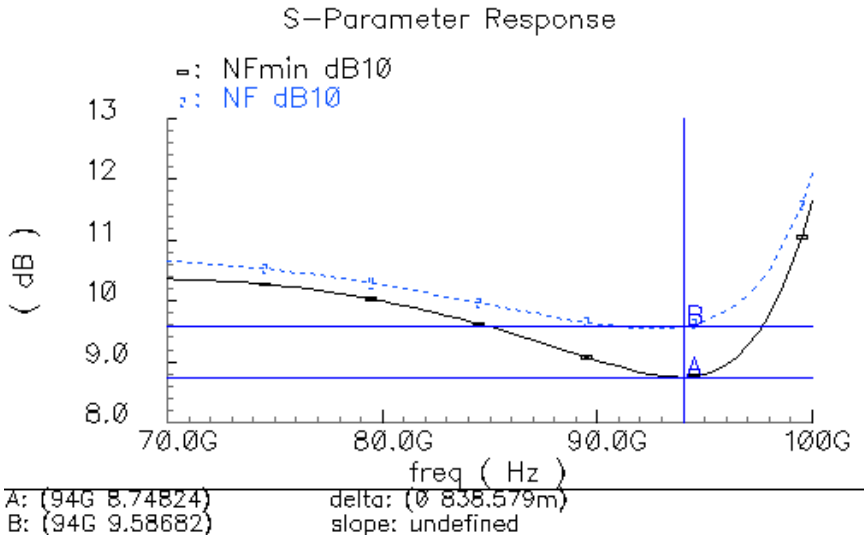

Figure 4.19: 94 GHz LNA NF and NF_{min}

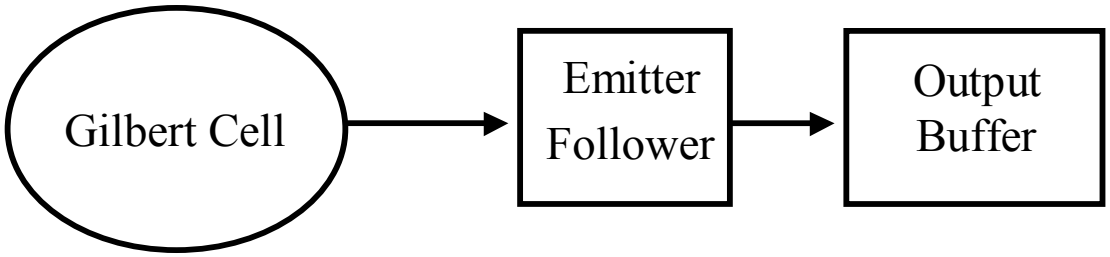

Figure 4.20: Mixer block diagram

4.4 94 GHz Double Balanced IF Down-conversion Mixer

4.4.1 Mixer Circuit Design

This mixer converts RF input signal at 94 GHz and down-convert it to a low RF frequency at 1 GHz. Since direct down-conversion mixers have to deal with DC offset problem, a low IF conversion will maintain simplest system while provide good linearity and high conversion gain. In chapter 3 basic mixer topology is discussed. The Gilbert mixer cell is a robust choice for high linearity and high conversion gain design. Mixer circuit design is composed of the tranconductance stage and the quad stage. In terms of optimization, the transconductance stage can be optimized the same way as an LNA for simultaneous power and noise match. For quad design, matching network is also needed to match the input of the switching quad.

Mixer circuit block diagram is shown in Figure 4.20. It consists of a Gilbert mixer cell with bias networks, an emitter follower as a level shifter, as well as an output buffer that interfaces 50 Ω system for testing purposes.

Figure 4.21 shows the mixer core circuit representation. All bias circuitry is omitted for simplicity reasons. Matching network is also omitted at the RF and LO ports. The mixer core then becomes a standard Gilbert mixer and circuit analysis closely follows one based on a Gilbert cell. This double-balanced mixer can effectively suppress feed-through and makes a high conversion gain possible at an IF of Gig Hertz range.

Mixer core is composed of the transconductance stage, switching quad, load resistor and current bias. The transconductance stage uses 2x transistors with emitter length at 6 μm and width at 0.12 μm. For the switching quad, it uses transistors with emitter length at 2 μm and width at 0.12 μm. The smaller emitter size with the given bias current sets a collector current density optimal for speed. Load resistor R_1 and R_2 are 75 Ω each. The reason for using 75 Ω resistor is that the IF frequency is at 10GHz. The output cannot be bandwidth limited up to at least 10 GHz. Therefore a smaller resistance will not introduce a dominant pole at the mixer output. In addition,

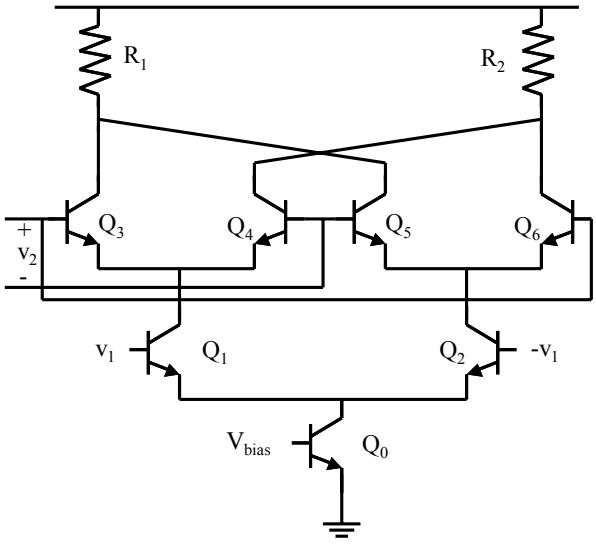

Figure 4.21: Mixer core schematic

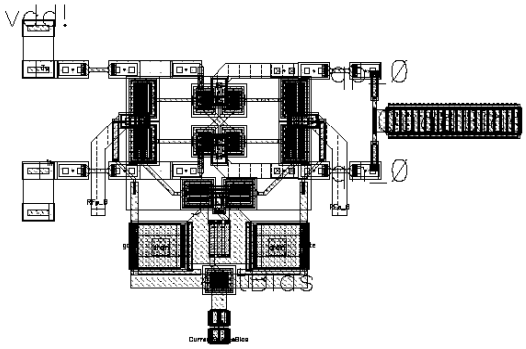

Figure 4.22: Mixer core layout

smaller resistance has small DC voltage drop and thus saving headroom for collector-emitter voltage and helping linearity of the mixer.

Based on the design principles outlined in Chapter 3, the mixer core is laid out before other passive elements. Figure 4.22 gives the layout cell of the mixer core. Since all the active devices are close to each other, signal isolation becomes worse. Large substrate contacts are used subsequently to ground signals traveling in the substrate. Then the mixer core is extracted and back-annotated netlist is generated for re-simulation. In order to interface with transmission lines and other passive elements at top layer metal, vias are also part of the layout and the effect of which is accounted for.

Figure 4.23 shows the subsequent stage after the mixer core. The emitter followers serve as level shifters to the output buffer. $Q_{1,2}$ has an emitter length of 2 μm, $Q_{3,4}$ 10 μm, and Q_5 7 μm with a multiplicity of 2. All transistors have an emitter width of 0.12 μm. $R_{1,2} = 4\ K\Omega$, $R_{3,4} = 150\ \Omega$, and $R_5 = 100\Omega$.

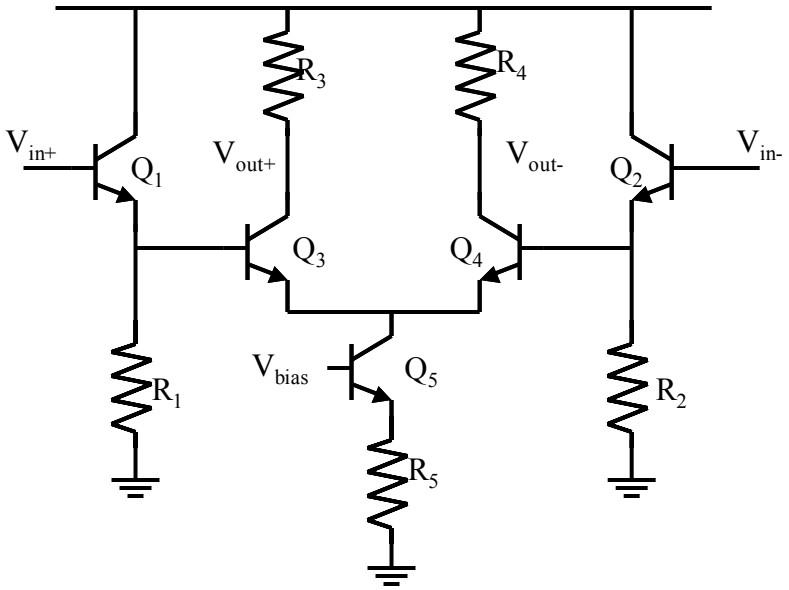

Figure 4.23: Level shifter and output buffer

Mixer layout is provided in Figure 4.24. Transmission lines are used to connect signals in and out of the chip. The layout is symmetric for all the differential signals. Decoupling capacitors are extensively used to eliminate ringing due to low or high frequency resonate parasitics. The chip size is 900 μm by 800 μm, which is compact enough for future system on chip integration.

Figure 4.25 shows the simulated results for linearity measurement. 1dB compression point is at –23 dBm input, and IIP3 is at –9 dBm at input, and conversion gain is 16 dB. The circuit is simulated with 94 GHz RF and 93 GHz LO, which results in 1 GHz IF signal. The noise figure for the mixer is 17 dB, which is reasonable given the minimum NF for a transistor is around 3dB. The chip is under

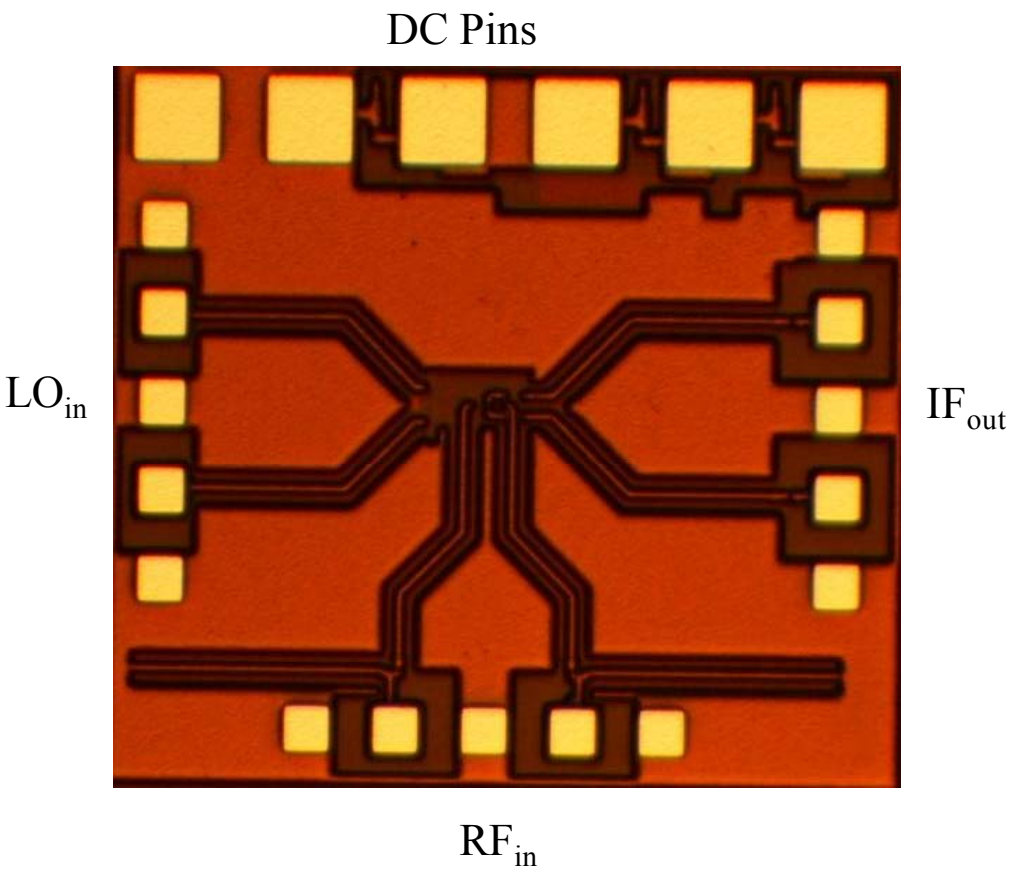

Figure 4.24: Mixer layout view

3.3 V supply and draws 25mA of current. The output buffer is the most power hungry block because it has to drive low impedance node.

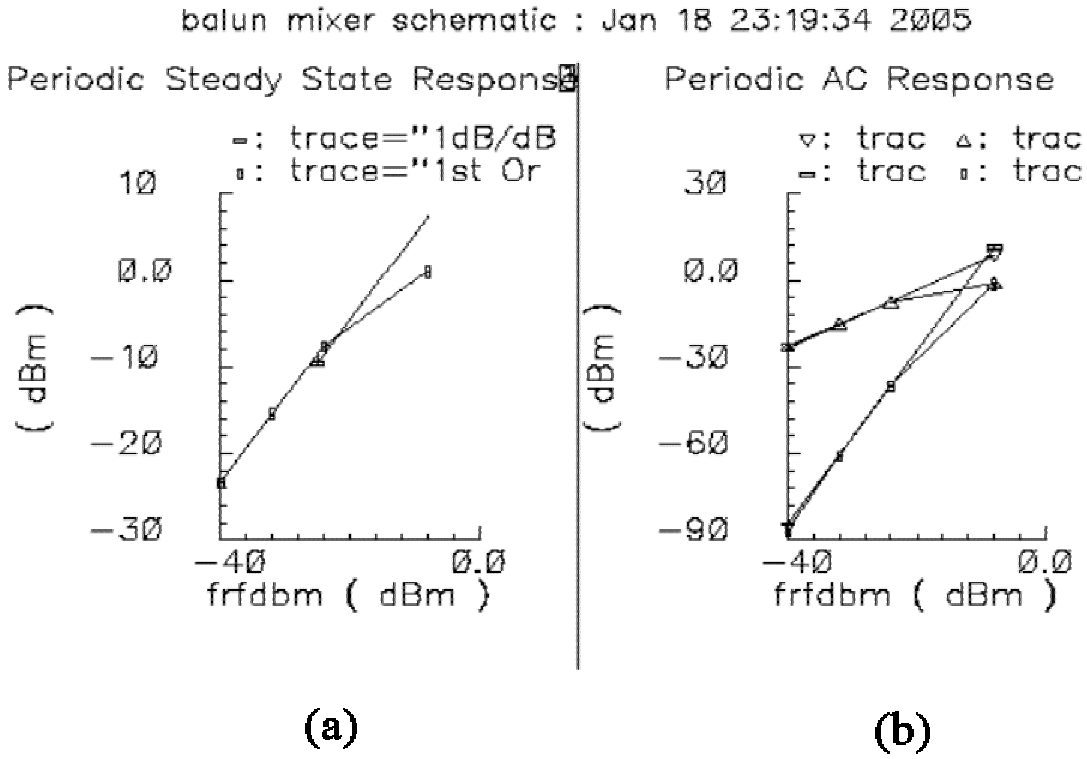

Figure 4.25: Mixer (a) 1dB compression point (b) IIP3

4.5 Conclusion

This chapter goes over in great detail the design process of a 94 GHz low noise amplifier/balun and a double balanced IF mixer. Many design issues are discussed and the parasitic-aware design process proposed in chapter 3 is applied in both designs. Simulation and some of the measurement results are presented as validation to the design process. Due to some test equipment limitations, not all circuit performance metrics can be measured. There was only one opportunity to tape out

this design and several technical difficulties in the design kit also affected the final verification process. Nevertheless, the design of a 94 GHz LNA/balun and a mixer illustrates the effectiveness of the new design methodology and as a result, uncertainties in millimeter wave integrated circuit design are greatly reduced and the design flow is much more transparent to a designer.

Chapter 5: 18 GHz Mixer and Integrated Mixer/VCO in SiGe

5.1 Overview

While 94 GHz band offers ultra short wavelength for high-resolution imaging, the advanced fabrication process that enables such applications is still expensive and limitations on existing testing equipment further make it a very expensive process that tailors to some very specific need, where cost is not a concern. For wireless data communications, however, price is the key driver for growth. Cheap yet reliable and high performance technology is always the ultimate goal for commercial development. At lower frequency spectrum, Ku band has some unlicensed spectrum space at 18 GHz that can be used for future short distance wireless data transmission. This chapter presents an integrated direct-down conversion mixer and quadrature voltage controlled oscillator (VCO) at 18 GHz in 47 GHz f_t SiGe technology, which will be integrated into future 18 GHz transceivers that have the capability of fast data transmission with low cost Si-based technology. The VCO is a collaboration effort from fellow graduate student B. Welch at CBCRL. This chapter will focus mainly on the design of the mixer, with additional discussion on the integrated VCO and mixer combo. Various aspects of circuit design optimization are discussed and measurement results are presented and compared with other previously published results to show the merit of this work. A summary is provided at the end.

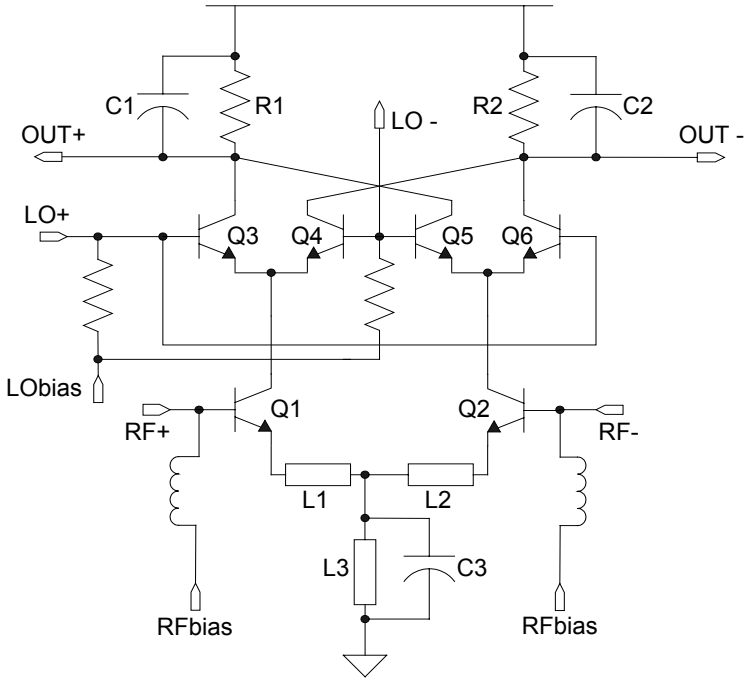

Figure 5.1: Mixer simplified schematic

5.2 Mixer Circuit Design

A double-balanced direct down-conversion mixer for use in a homodyne architecture reduces design complexity and power consumption; produces less even-order distortion; provides a high conversion gain; and offers superior immunity against LO and RF feed-through [35].

A simplified schematic of the mixer core, which is based upon Gilbert cell topology [36], is shown is Figure 5.1. In this schematic Q_1 and Q_2 form the RF transconductance stage and $Q_3 - Q_6$ form the switching quad. The tank, composed of L_3 and C_3, provides common-mode rejection without consuming additional DC voltage headroom. R_1, C_1, R_2, and C_2 form low pass filters at the load that filter the high frequency signals produced by LO and RF leakage and harmonics of the baseband signal. L_1 and L_2 are microstrip line degeneration inductors that enhance the

linearity of the transconductance stage by providing more current efficiency than resistive or capacitive degeneration [36].

5.2.1 Device Geometry on Noise Figure and Gain

The noise figure of the mixer is dominated by the RF transconductance stage, since the LO drive is large and remains fixed. Thus for the RF stage the analysis of noise optimization can be done using a similar approach to that of a common emitter low noise amplifier. The main contributors of bipolar transistor noise are base resistance thermal noise $4kTr_b$, collector shot noise $2qI_C$, and base shot noise $2qI_B$, where r_b, I_C, and I_B are base resistance, collector current and base current respectively. In general, for a fixed SiGe HBT size, NF_{min} has a relatively flat minima when plotted against I_C [38]. This in return leaves some room for optimization. Nevertheless, those minima are still roughly one-eighth of the value at which corresponding f_t peaks for a specific device size, thus the trade-off between gain and NF remains severe. In addition, the constraints of low supply voltage of 3.3 V and low power consumption still maintain an upper bound on the collector current. The requirement of simultaneous power and noise match further limits the range of the collector current for a given geometry size.

The transistor sizes of the mixing quad are carefully chosen to maximize their f_t once the current level for the RF stage is determined, because an imperfect switching quad not only degrades the conversion gain, it also increases its noise contribution to the overall mixer.

5.2.2 Quad Transistors Base DC Bias's Effect on Gain and IIP_3

Once the DC current level and transistor sizes are determined, a reasonable value for load resistors R_1 and R_2 is chosen to provide good gain while maintaining sufficient headroom for the quad and the transconductance stage. Since a higher V_{CB}

increases device f_t mainly due to its effect on base-collector depletion capacitance, the quad transistors and the transconductance stage compete for the limited headroom to achieve a higher f_t. Also since input LO signal is large, inadequate headroom in the quad section will result in severe distortion at the output. To balance the requirement of both the quad and the transconductance stage for optimal gain and linearity, the voltage headroom allocation is optimized by changing the DC bias point at the base of transistors Q_3 - Q_6. Therefore, the total DC current is pinned by the bias input at the RF stage and remains fixed throughout the optimization.

Figure 5.2 shows the simulated conversion gain and IIP3 versus base bias point at the quad for a roughly fixed DC current level, device geometry, and LO drive amplitude. By raising the DC bias level, V_{CB} of the quad transistors is decreased and V_{CB} at the RF stage is increased. The rapid decrease in IIP_3 is due to non-ideal switching at the quad when headroom is limited. The slower increase in gain is partially due to a small increase in DC current and higher f_t of the RF stage. The plot

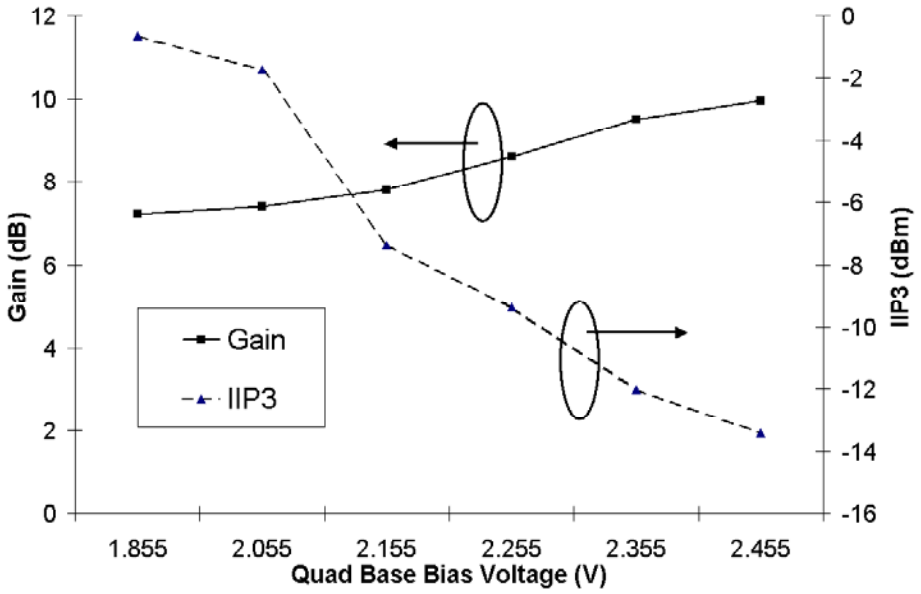

Figure 5.2: Simulated gain and IIP_3 design trade-off with various DC bias at the base of the quad

provides qualitative insight into the effect of device headroom on gain and linearity. It indicates that large headroom in the quad section is desirable for high linearity.

5.2.3 Output Buffer

The output buffer of the mixer shown in Figure 5.3. is a differential pair with 50 Ω terminations (R_1, R_2). The buffer uses two 25 Ω degeneration resistors (R_3, R_4). Most of the published mixers typically use an IF or the baseband amplifier as part of their overall mixer performance; however, the differential pair used in the current design does not provide any gain because the degeneration resistance is the same as load resistance (50 Ω R_1 or R_2 in parallel with 50 Ω termination on test equipment). Hence, the measured results presented in the next section are a true reflection of the mixer's intrinsic performance and can be easily compared with other mixers operating at similar frequencies. A higher baseband gain can be easily obtained by cascading baseband amplifiers after the mixer core.

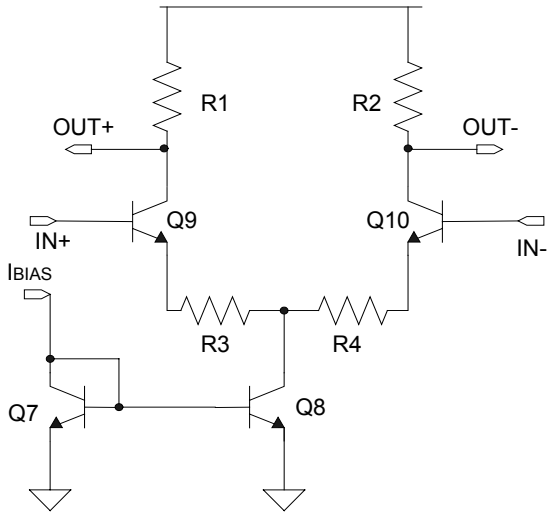

Figure 5.3: Output buffer with 50 Ω termination and 25 Ω degeneration to give 0 dB of gain

5.2.4 Experimental Results

The mixer is designed and simulated using Cadence Spectre and Agilent ADS. The chip is fabricated in IBM 6HP BiCMOS technology featuring an f_t of 45 GHz. A die photo of the chip, which has an area of 1.24mm x 1mm, is shown in Figure 5.4 including input and output pads. For measurements, two GSGSG wafer probes are used for the RF and LO signals and one GSG probe is used for the baseband output.

RF and LO signals are fed through two hybrid couplers to produce differential signals. The RF and LO frequencies are 17.8 GHz and 17.9 GHz respectively, and the LO power is –1 dBm. The mixer core consumes 16.5 mW, while the output buffer consumes 33 mW from a 3.3 V supply including their bias network.

S_{11} of the RF input port is measured with de-embedded data. The measurement is done with single-ended signal. Figure 5.5 shows the measured results. –15.3 dB of S_{11} is obtained at 17.8 GHz.

Accounting for cable and hybrid coupler losses, the conversion gain of the mixer is 4.5 dB at an LO drive of –1 dBm. It is important to note that the gain is

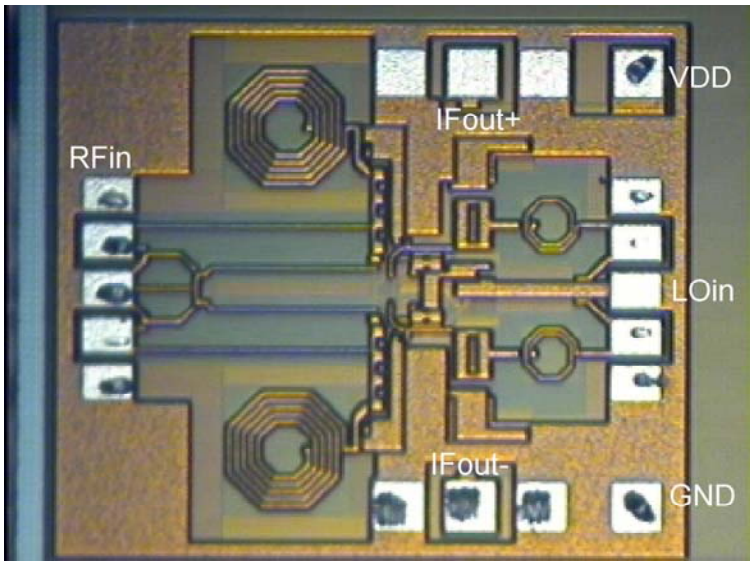

Figure 5.4: Mixer die photo

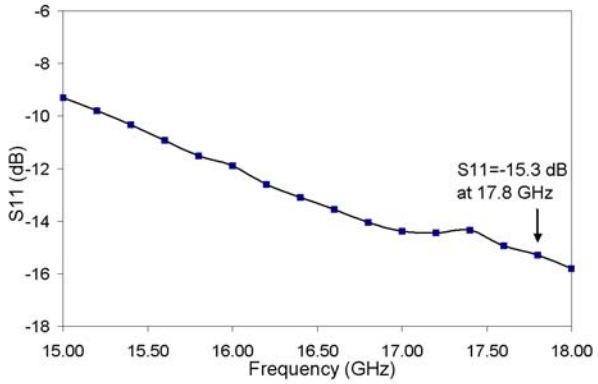

Figure 5.5: Measured S_{11} at RF port

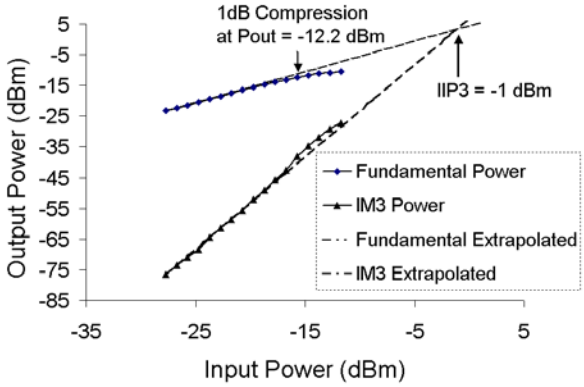

Figure 5.6: Fundamental and third order intermodulation output power verses RF input power

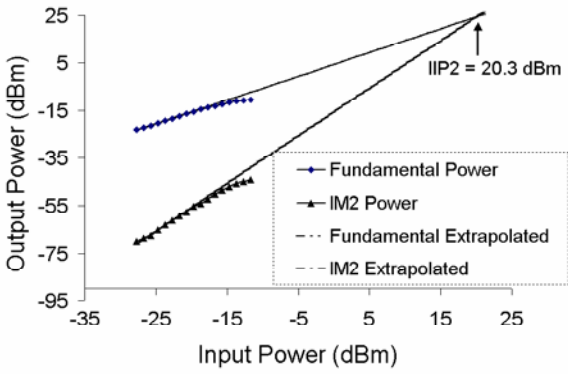

Figure 5.7: Fundamental and second order intermodulation output power verses RF input power

entirely produced from the mixer core without any baseband amplification.

Ideally the NF should be measured differentially. For a single-ended output, the noise contribution from the buffer tail current at IF will leak to the output and greatly increase the NF [6]. However, due to equipment limitations the NF is measured single-ended. A rough estimate of double side band (DSB) NF degradation can be expressed as follows.

$$NF_S - NF_D = 10\log(\frac{N_{totS}}{N_{in} \cdot G_S} \cdot \frac{N_{in} \cdot G_D}{N_{totD}}) \tag{5.1}$$

where NF is the NF, N_{tot} is the total output noise, N_{in} is the input noise, G is the gain, and the subscripts S and D denote singled-ended and differential cases respectively. Since G_D is two times G_S and N_{in} is unchanged, the degradation only depends on the ratio of the total output noise. First, it can be shown that in the differential case the output noise contribution is primarily composed of noise from the input and collector shot noise from $Q_1 - Q_6$. The buffer stage noise can be ignored because of the gain in the first stage and $Q_1 - Q_6$'s base thermal and shot noise is ignored due to small r_b and source impedance. $Q_1 - Q_6$'s shot noise appears symmetrically on the differential mixer outputs. Given I_C = 2.5 mA for Q_1 and Q_2, I_C = 1.25 mA for $Q_3 - Q_6$, the buffer has a voltage gain of 1, and an impedance at the output of the mixer core of 61 Ω, the output noise spectral density due to $Q_1 - Q_6$ is 1.19×10^{-19} (W/Hz). The input noise power spectral density is twice that of the single side band and multiplies the overall gain (4.5 dB) to arrive at an output spectral density of 2.32×10^{-20} (W/Hz). Summing the two together, the total noise spectral density is 1.42×10^{-19} (W/Hz). Then for the single-ended case, the largest noise contribution comes from Q_8 and Q_7, because the common mode noise is no longer rejected and Q_8 amplifies any noise seen at its base. To simplify the analysis, the noise source seen at the base of Q_8 is limited to Q_8's base shot noise and Q_7's base thermal noise and collector shot noise. Given that I_{CQ8} is 10mA, I_{CQ7} is 88mA, and β is 100 for both transistors, it can be shown that Q_8's

collector shot noise can be ignored. And due to Q_8's small r_b and Q_7's small I_B, their base thermal noise and base shot noise can be ignored, too. With r_{bQ7} equal 12 Ω and circuit parameters given above, the total output noise spectral density for the single-ended case is 5.83×10^{-19} (W/Hz). Thus the hand calculation gives a rough estimate of noise degradation of 7 dB, which is close to the simulated 6.7 dB. Simulation also shows that a 10% of output mismatch only increases the NF by 0.4 dB. Therefore from the measured 13.8 dB of DSB NF, it is reasonable to extrapolate the true DSB NF to be 7.1 dB, which is very close to simulated 6.7 dB

The IIP_3 measurement is done by combining two single tone RF signal sources. The two tones are kept 20 MHz apart with the center at 17.8 GHz. The output power spectrum is obtained to construct the IIP_3 plot. Figure 5.6 shows the fundamental tone and third order intermodulation output power verses input power. The data is extrapolated to find IIP_3 point. From the graph the 1dB compression point is at an output power of –12.2 dBm, and IIP_3 point is –1 dBm while an IIP_2 of 20.3 dBm is shown in Figure 5.7.

The measured LO to RF isolation is 31 dB. Since the single-ended output is taken, the LO-to-output leakage is not rejected by the differential structure and therefore not measured.

The summarized performance of the mixer is in Table 5.1 along with other published mixers operating at similar frequencies. It is important to note that many of these mixers include a baseband or IF amplifier to provide a higher conversion gain.

Table 5-1 Mixer performance compared with other published results

Ref	RF Freq. (GHz)	Process	Gain (dB)	DSB NF(dB)	IIP3 (dB)	P_{DC} (mW)	P_{out1dB} (dBm)	FOM (dB)
[39]	**17.5**	**45 GHz f_t SiGe**	**4.5**	**7.1**	**-1.0**	**16.5**	**-12.2**	**-19.3**
[40]	17.35	Same	12.0	11.5	-10.0	17.8	-25	-33.7
[41]	20	80 GHz f_t SiGe	10.0	6.0	-11.3	10.0	-21	-26.0
[41]	17.0	52 GHz f_t SiGe	5.4	8.8	-9.9	7.0	-19	-26.5
[42]	20.0	50 GHz f_t SiGe	10.0	17.0	-1.0	32.0	-9	-33.0

The figure of merit (FOM) given below in the table is used to compare the current mixer to state-of-the-art that appear in publication, and is defined as in [43].

$$FOM = 10\log(\frac{IIP3(mW)}{(F-1)\cdot P_{DC}}) \tag{5.2}$$

5.3 Integrated Mixer and VCO Combo

5.3.1 Circuit Design

The mixer is driven by half of an emitter-degenerated quadrature oscillator, the core of which is shown in Figure 5.1. In this implementation of the LC oscillator the tank is provided by a parallel pair of on-chip transmission lines and MOS varactors. Grounded coplanar transmission lines are used as opposed to inductors because they achieve a higher Q within the frequency band of interest, provide local & low loss return paths, and enable more efficient floor planning to optimize for area. A benefit of this flexibility is the ability to accurately place the common bias node of the two tanks (VDD), so as to eliminate potential sources of parasitic deviations from the expected oscillation frequency. Other benefits of using transmission line based tanks is a reduction in coupling due to the signal shielding, and a greater ability to tune the

oscillation frequency of the oscillator by varying the transmission line length (no variations to the oscillator core required, unlike when using spiral inductors). The Oscillator core uses an AC cross-coupled emitter degenerated pair with an applied tail current to provide negative resistance. A pair of base connected heterojunction bipolar transistors (HBT's) are employed to provide the coupled output signals to drive the secondary oscillator (this device area was minimized to prevent significant parasitic loading of the oscillator nodes).

The mixer LO input ports are matched to 50 Ω and the output buffer of the VCO is also matched to 50 Ω. Even though it might be more advantageous to have a match of a higher impedance between the two components, it is convenient to use the existing breakout designs and simply connect them together, because the test environment requires 50 Ω interface for the breakouts. Since the LO port requires a large signal to sufficiently suppress switching noise and enhance conversion gain, the output buffer of the VCO cannot be eliminated due to its function as an isolation block to the VCO core and its ability to match to a low impedance load. To preserve symmetry, the quadrature output port is terminated by a 50 Ω load. The layout of the integrated mixer and VCO is greatly simplified due to its differential design. Careful layout is carried out to preserve symmetry whenever possible for the mixer and VCO. To simulate the whole design, traditional simulation methods for the mixer such as harmonic balance in ADS or PSS/PAC in Cadence do not work with the VCO, because those simulation methods require a known frequency in order to calculate the gain, noise figure, and linearity. Since a great deal of work has be done to characterize the mixer and the VCO separately, it is safe to assume that the performance of the combined design depends mostly on the matching of the LO port of the mixer and the layout impact on the interconnect between the mixer and the VCO. If the LO port matches to the VCO output port and layout parastics are kept at minimum, the

simulation results from each component can be used to predict the integrated performance. Only transient simulation is used to show the conversion gain. Noise and linearity analysis were not done due to aforementioned limitations. The IF output is far away from the pads, which is shown on Fig. 7. Long transmission lines are used to bring the signals to the pads. Since the down-converted signals are no more than 100 MHz, the loss in these transmissions lines is negligible.

The transient simulation result is shown below in Fig. 6 for an RF signal of 17.1 GHz and LO signal of 17 GHz. The mixer has a broadband response and 17.1 GHz is well within its covered bandwidth. The simulated LO signal is 17 GHz, which is different from measured 18 GHz. However, this discrepancy is acceptable because as long as the LO signal is large and the phase noise is small, the contribution to noise figure and the conversion of the overall circuit is small. From the plot the conversion gain is 12.6 dB.

5.3.2 Experimental Results

The integrated mixer and VCO is designed and simulated using Cadence Spectre and Agilent ADS. The chip is fabricated a production SiGe 47 GHz f_t process.

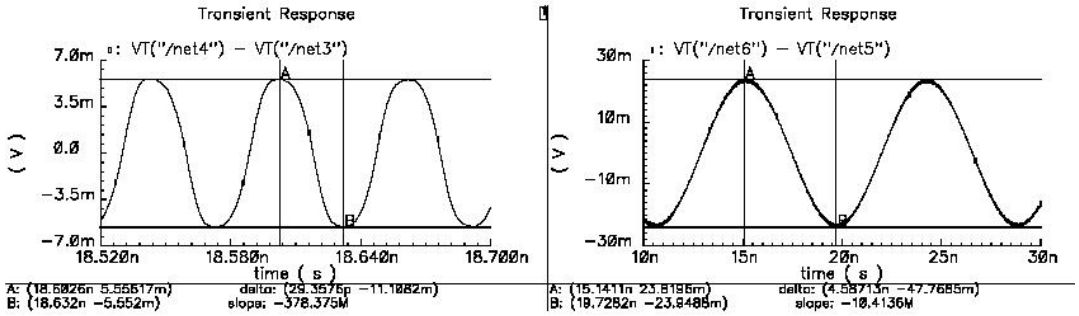

Figure 5.8: **Transient simulation plot for input and output magnitude and period of the integrated mixer and VCO.**

All passive components are implemented on-chip. A die photo of the chip, which has an area of 2.1mm x 1.08mm, is shown in Fig. 7 including pads for input, output, supply pin and ground. To wafer probe the chip, two GSGSG probes are used to provide input RF signal and output IF signal. Another pair of GSGSG probes is used to provide bias and supply voltage to the VCO. In order to show the feasibility of the design, only the in-phase output of the VCO is fed to the mixer. Since the VCO is fabricated separately, the quadrature performance can be verified independently, eliminating the need to connect both in-phase and quadrature signals to the mixers, as the layout symmetry would be well preserved very easily. In the following sections, measurement results for the mixer and VCO breakouts are presented separately followed by the integrated chip performance at the end.

The integrated mixer and VCO is measured using the probe set-up shown in Figure 5.9. The circuit simulation is performed around 17 GHz as shown in Figure 5.8. However, the VCO breakout measurement indicates an oscillation frequency of

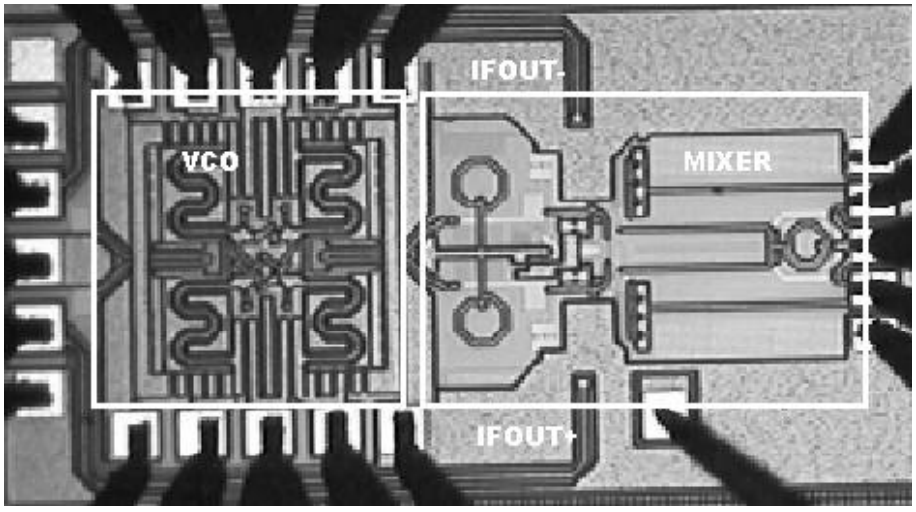

Figure 5.9: **Integrated mixer and VCO die photo**

18.4 GHz and higher. This is mainly due the small variations in transmission line length in the oscillator tank that are not accounted for in schematic simulation. As a result, the RF input signal needs to be close to the oscillation frequency as the output buffer of the mixer has a low pass filter at the load with its corner frequency at 400 MHz. The mixer input exhibits a broadband matching tendency that extends beyond 18 GHz; therefore by adjusting the input frequency to 18.3 GHz, there is minimum impact on the mixer performance. Due to the lack of feedback control loop to stabilize the LO frequency, it is not possible to evaluate the noise performance of the design, since the output IF frequency hops within a specific range, despite the effort to stabilize the LO frequency by using a battery as a control voltage source. The probe, cable, and connector loss also must be accounted for, and this information can be obtained from the mixer measurement set-up.

The final conversion gain of the mixer and VCO combo is determined to be –16 dB, which is less than the expected value of 13 dB from simulation. What cause the gain discrepancy are the lower gain of the mixer and the lower-than-expected output power of the VCO. The simulated conversion gain of the mixer is 12 dB, but the measurement only shows 4.5 dB. This discrepancy is mainly due to the tank layout that changes the tank resonate frequency from its simulated value, therefore lowering common-mode impedance. As for the VCO, the measured output power of the VCO breakout is –12 dBm, less than the simulated 0 dBm value. As mentioned earlier, the mixer conversion gain and noise figure are closely dependent on LO signal amplitude, since it determines how perfect the mixer switch is and how much noise is fed into the output, so a weaker gain is to be expected.

Even though the integrated mixer and VCO displays less gain than expected, the breakout components have performance specs that exceed or are comparable to recently published results. The low conversion gain can also be enhanced by

increasing the gain of the output buffer and variable gain amplifiers at base band, which usually have a large gain and can easily offset the loss in the mixing stage.

5.4 Conclusion

A K-band mixer and mixer-VCO combo design in SiGe technology are presented in this chapter. Optimization on noise and linearity is achieved by analyzing the inherent circuit topology qualitatively and subsequent simulation results confirm the qualitative analysis. Passive elements in the mixer topology are less critical since models provided by the foundry are sufficient to for K-band frequency. Testing equipment has a frequency range that stops at 18 GHz. Therefore measurement results are not possible beyond that frequency. However, with the obtained measurement results, a broadband response could be predicted for frequencies beyond 18 GHz. The mixer VCO combo has a less than ideal result for conversion gain. The output frequency of the VCO is not phase-locked and the lower than expected VCO output power contributes to some deviation from simulation. The K-band circuits discussed in this chapter clearly demonstrates the advantage of commercially available low cost SiGe process in implementing microwave circuits for wireless communication applications.

Chapter 6: 40 GHz Low Noise Amplifier in SiGe

6.1 Overview

Before the advent of 200 GHz f_t SiGe BiCMOS process, one of the BiCMOS processes that have an f_t more than 100 GHz is from IBM [44]. This process is capable of 120 GHz f_t and 100 GHz f_{max}. It features 0.11 μm L_{eff} CMOS and 0.2 μm emitter length SiGe devices. For Q band (36 GHz – 46 GHz) applications, this process provides a cost effective way of implementing a wireless transceiver system. In addition, FCC proposed to have several bands in the 40 GHz range for future wireless service, which brings real life benefit into research activities for circuits operating around this frequency.

This chapter presents an LNA designed in this 120 GHz f_t technology. Circuit design, simulation as well as measurement results are discussed. The previously mentioned parasitic-aware circuit design methodology is used to maximize circuit performance and minimize impact of unwanted parasitics. This design demonstrates the validity of the proposed design methodology and its flexibility in designing circuits at different frequencies, which usually presents different challenges as many characteristics of both active and passive devices are strongly dependent of frequency.

6.2 LNA Circuit Design

The goal for designing an LNA is to have a high gain, high linearity, and low noise figure with reasonable power consumption. As discussed in chapter 3, its circuit topology is chosen based on circuit performance requirement as well as operating

frequency. Compared to the 94 GHz LNA discussed in chapter 4, the quarter wavelength on a transmission line in silicon at 40 GHz is 1 mm, which is prohibitively expensive to implement. Therefore the configuration used in chapter 4 cannot be implemented for 40 GHz amplifier without incurring long meandering transmission lines that waste valuable silicon space. Therefore the other configuration discussed in chapter 3, which is common emitter with cascode configuration, is adopted to efficiently utilize space and provide reasonable performance.

In order to have adequate gain, the circuit is designed to have two cascode stages. Compared to the first stage, the second stage does not have emitter degeneration inductance for simultaneous power and noise match. Instead, the second stage is optimized for maximum gain. The degeneration transmission line T_1 is 100

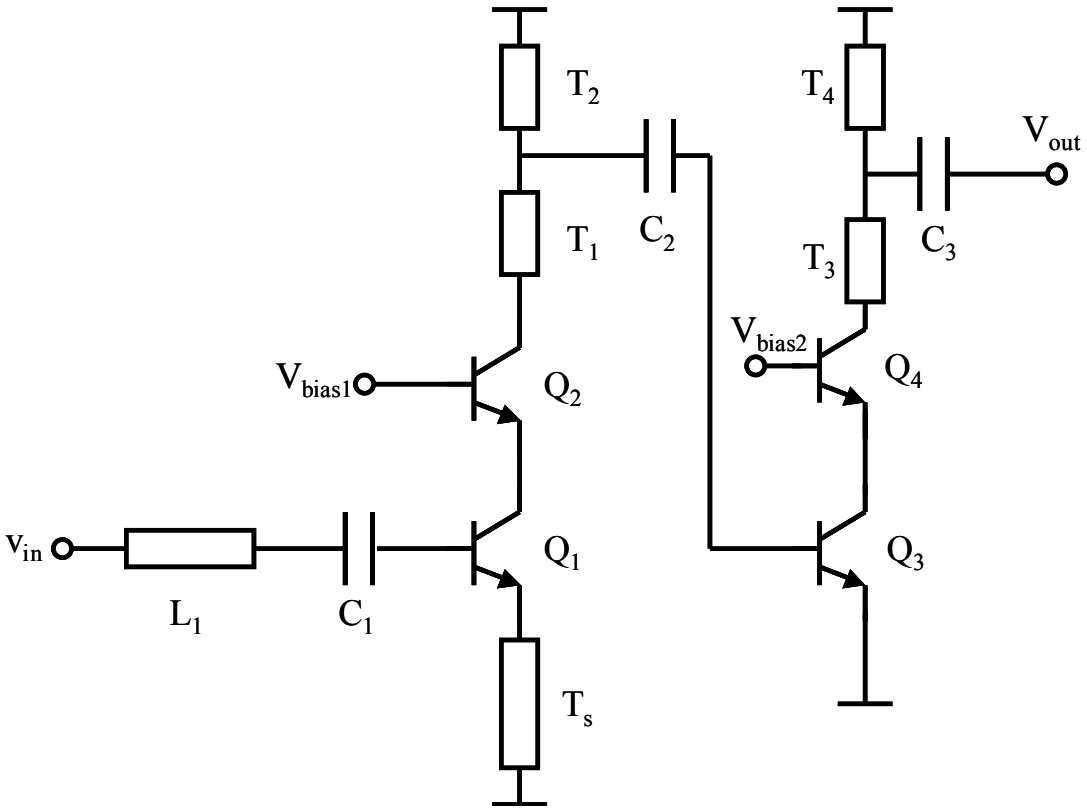

Figure 6.1: **40 GHz LNA Schematic**

μm long and connects to the ground at the same time. The matching network is composed of C_1 and L_1. C_1 is a 765 fF MIM capacitor that couples input RF signal and isolates the DC signal from the pad. L_1 is a 4 μm x 120 μm line inductor. For spiral inductors the inductance drops according to the following formula [45]

$$L_{eff} = L_s - M_{ind,sub} \tag{6.1}$$

where L_{eff} is the effective inductance of a spiral inductor, L_s is the low frequency inductance of the spiral and $M_{ind,sub}$ is the mutual inductance between the spiral and the substrate. The frequency dependency characteristic comes from the mutual inductance that increases with frequency. For a single turn spiral inductor, the effective inductance is also a function of the substrate doping [46]. Therefore for a lossy substrate, the effective inductance quickly drops to a low level compared to its DC value. For a line inductor, the advantage over a spiral inductor is less dependent on proximity effect. Spiral inductors suffer from conductors that are close by at the turns, whereas a line inductor does not have the same problem. In terms of inductor modeling, line inductors are much more accurately modeled.

$Q_{1,2,3,4}$ all have an emitter width of 6.4 μm. The size is chosen for optimal noise and power matching as well as linearity. The dimensions of the rest of the passive elements are listed below. All the transmission lines have a width of 4 μm. The lengths are 478 μm, 240 μm, 450 μm, and 205 μm for $T_{1,2,3,4}$ respectively. C_2 and C_3 are 458 fF and 921 fF respectively. They decouple DC levels from one stage to the next and provide power match for the connecting stages.

The circuit also achieves low power dissipation. The power supply is designed at 1.8 V and provides a total of 8 mA of current to both stages, which gives the circuit a competitive advantage in terms of future integration with CMOS blocks.

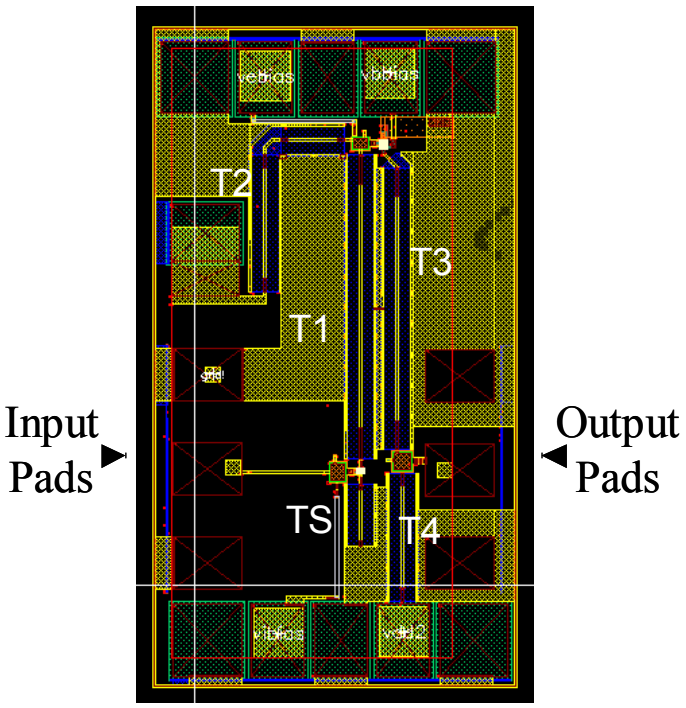

Figure 6.2: 40 GHz LNA Layout

6.3 40 GHz LNA Layout

The LNA uses efficient layout arrangement to reduce the layout area. Figure 6.2 is an image of the layout file for the LNA. The bottom and top pads are for power supply and ground. Input and output pads are place at the sides of the chip. The matching network for both stages are placed in a way such that the second stage starts at the junction between T_1 and T_2. The output matching network brings back the signal to the right side of the chip. Since the matching networks have similar dimensions, the two gain stages can be placed far away from each other, thus reducing cross-talk. This layout also facilitates routing power and bias signals to each transistor. For a typical on-wafer probe testing setup, probes are usually placed at each side of the chip, and this layout minimizes the delivery distance for all the DC pins.

6.4 Simulation and Measurement Results

Figure 6.3 shows the die photo of the LNA. The chip takes up an area of 1.05 mm by 0.57 mm, which is relatively small for circuits operating at 40 GHz with on-chip matching elements. The top and bottom are for DC bias probes and power supply. Extensive ground plane can be found that connects all the ground pads. Under the large ground plane, a large number of decoupling capacitors can be found. They eliminate any possibility of low frequency oscillation due to ground plane inductance and rejects high frequency spectrum content that may be present in DC power supply.

Due to equipment limitations, only S-parameter measurement is carried out for the LNA. Figure 6.4 and 6.5 shows the measured results for the LNA. The LNA has

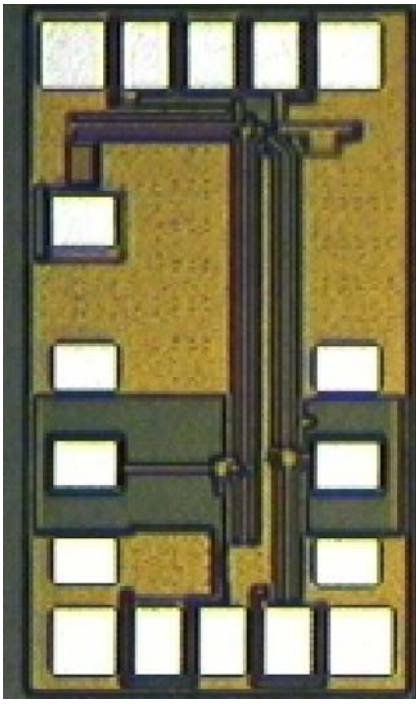

Figure 6.3: 40 GHz LNA die photo

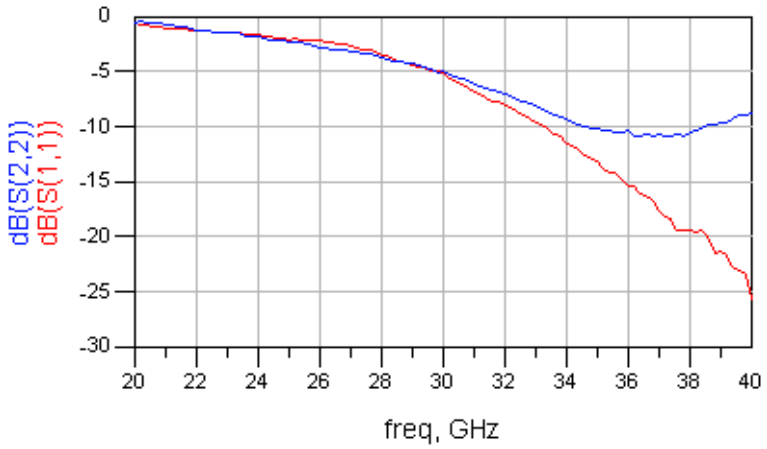

Figure 6.4: S_{11} and S_{22} response

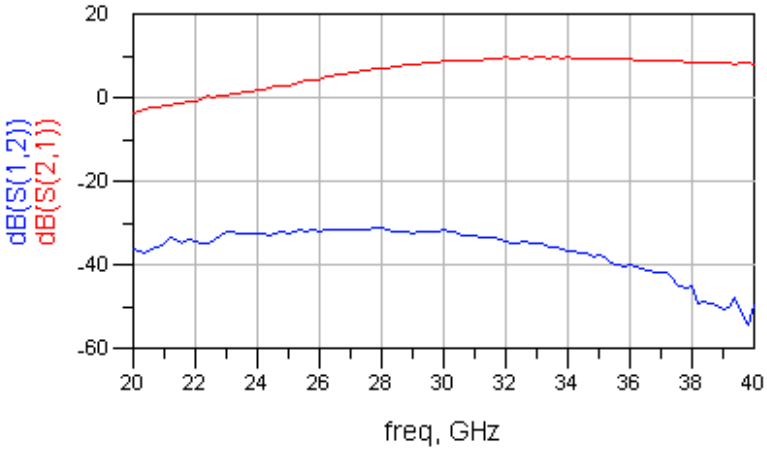

Figure 6.5: S_{21} Response

an excellent input and output power matching. It also achieves a broadband gain between 30 GHz and 40 GHz. Reverse isolation is better than –30 GHz. The measurement results are obtained after full de-embed procedure on a structure that has the same pad size on silicon.

Noise figure and linearity is simulated with full parasitic extraction. Figure 6.6 and 6.7 shows each simulation result. It achieves 5.2 dB of noise figure and a –3.3

dBm input IIP3. Even though only simulation results are shown for NF and IIP_3, given the good matching and high gain measurement, it can be predicted that the measurement data should be close to simulation.

The 40 GHz LNA designed in 120 GHz f_t SiGe technology is an ideal

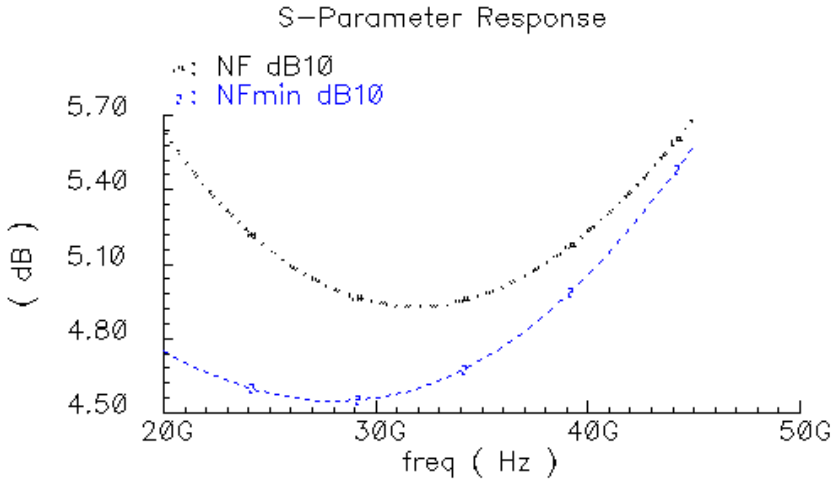

Figure 6.6: LNA simulated NF and NF_{min}

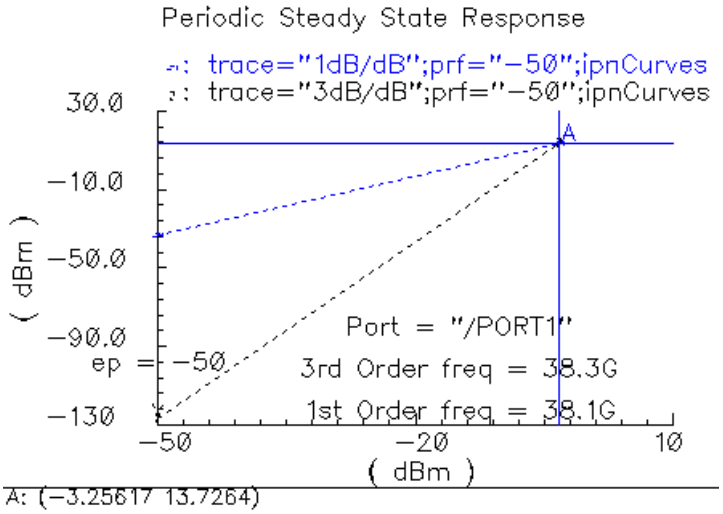

Figure 6.7: LNA simulated IIP_3

replacement for traditional III-V device based design. Its performance specs compete well against other published research. Table 6.1 lists several designs in similar frequency range and it can be shown that this design achieves similar specs with a inferior technology.

Table 6-1 Other published LNA specs comparison sheet

Ref	RF Freq. (GHz)	Process	Gain (dB)	NF(dB)	IIP3 (dB)	V_{DC} (V)	I_{DC} (mA)
My work	40	120 GHz f_t SiGe	8.5	5.2	-3.2	1.8	17
[47]	160	500 GHz f_t SiGe	9	6	N/A	1.4	33
[48]	26.5	150nm InP PHEMT	14.5	1.7	N/A	N/A	N/A
[49]	19	155 GHz f_t SiGe	26	2.2	NA	3	8.7
[50]	24	80 GHz f_t SiGe	10	9	N/A	3.6	46
[51]	49	205 GHz f_t SiGe	14	5.2	-11	1.8	2
[52]	40	SOI/149 GHz	9.5	4	N/A	2.4	17

6.5 Conclusion

A 40 GHz LNA is presented in this chapter. The design uses the methodology described in chapter 3 to achieve a performance similar to other published results with less advanced technology. Also layout issues are discussed since they are pertinent to this particular frequency range.

Chapter 7: Conclusion

7.1 Summary of this Work

A novel design approach for implementing millimeter wave wireless transceiver front-end circuits was proposed. It encompasses a wide range of issues related to active and passive elements in a circuit. All design aspects including modeling and simulation are considered for maximum accuracy and reliability. The new design approach simplifies circuit optimization and results in faster and more robust designs on silicon for millimeter wave range applications.

The constraints of millimeter wave front-end integrated circuit design were discussed. Limitations from SiGe device modeling and lossy substrate, passive element modeling, and parasitic element extraction make designs in the millimeter wave range much less reliable than designs in the lower frequency range. Those limitations force a simplification effort on the analysis and design aspects. Two critical components of a wireless transceiver – low noise amplifier and mixer, are chosen to demonstrate the new design methodology. Solutions are proposed for each circuit block for maximum design efficiency. To further validate those design principles, a 94 GHz LNA/Balun and mixer, a 40 GHz LNA, and an 18 GHz mixer and VCO combo are designed and the detailed design analysis are given. Though some circuit parameters cannot be extracted from measurement at current time, those that are available from measurement confirm the efficiency and validity of the

proposed design approach. Some circuit performance specs compare well against the published research done in comparable technology.

7.2 Technology Issues

The proposed design approach depends heavily on SiGe BiCMOS technology. Many design issues are specific to bipolar circuits and are not applicable to CMOS counter parts. In recent years, high speed CMOS technology has become a potential competitor for current SiGe BiCMOS technology [53]. It offers an even higher level of integration with digital blocks and lower cost. Another suitable technology for millimeter wave applications is SOI CMOS, which combines the advantage of easy system integration and high performance and avoids many problems associated with lossy substrate.

7.3 Future Work

The main purpose of this work was to demonstrate an integrated approach to designing millimeter wave range transceiver front-end circuits in SiGe BiCMOS technology. Currently only LNA and mixer blocks are discussed. In a wireless system, there are other components that are also critical to the system performance, namely frequency synthesizer and power amplifier. Future effort should be devoted to those blocks by applying similar design approach. A complete transceiver system designed under the same philosophy that interfaces with digital blocks on or off-chip and transmits and receives information would be the ultimate goal of this research and will undoubtedly demonstrate the validity of the novel design approach described in this dissertation.

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