THREE-DIMENSIONAL INTEGRATION FOR FLASH MEMORY CELL

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Scaling of flash memory cell structures for large-capacity nonvolatile storage will encounter serious technical challenges in lithography, disturbance and gate stack designs. An alternative way to increase the number of bits per unit chip area can be achieved by 3-D stacking of thin-film memory layers. 3-D stacking has caused different technology issues that must be overcome before it can be competitive. Due to the lack of a repeatable and affordable epitaxial growth method, the polycrystalline or amorphous thin films must be deposited with small thermal budget, good transistor quality and minimal parametric variation. The thin-film device geometry must allow reasonable scaling down to 20nm gate pitch. The electrical operation will need to minimize the power consumption and program/erase voltage to avoid reliability problems from temperature and migration due to heat dissipation and defect density concerns in 3-D integration.

In this dissertation, we propose new device solutions to support the 3-D stacking memory IC technology. We will first presents the fabrication process, material and electrical characteristics of ultra thin body (UTB) thin-film transistor (TFT) metal nanocrystal memories by using *in-situ* doped polysilicon chemical vapor deposition (CVD) followed by the chemical mechanical polishing (CMP) process, where surface roughness below 1nm is achieved. The resulting film is about 13nm thick with 10^{19} cm^{-3} body doping. SEM and STEM observation demonstrated that size, distribution, and density of nanocrystals could be controlled for electronic device purposes. CBED, 3D tomographic image and EELS analyses also confirmed the physical stability of the

nanocrystals. We are able to achieve memory windows of about 1.6V and 2.3V by ±6V program/erase (P/E) voltages in single and double layer NCs. From these results, it is confirmed that double layer nanocrystal memories demonstrate retention and charge density improvement over single-layer metal nanocrystals due to the increased number density of nanocrystals.

To obtain low contact resistance in the source and drain region, we then demonstrate the self-aligned silicidation (SAS) process. The device split without SAS is also shown where the source/drain resistance improvement by SAS can be clearly observed. Retention time characteristics were monitored in the Al_2O_3/Au/$(Ti,Dy)_xO_y$ devices with Ni SAS , and were extracted to be well beyond 10 years.

Vertical integration of Ge TFT devices is another promising method to achieve 3D integration from the low processing temperature and smaller bandgap. We have obtained a memory window of about 1.8V by ±5V P/E voltages for UTB Ge TFT with the gate stack of Al_2O_3/Au/$(Ti,Dy)_xO_y$ and single layer NCs. Retention characteristics were also satisfactory.

From these results, the ultra-thin planar polysilicon or Ge layer, SAS process and the gate stack design contribute to the long retention time and large memory window. Therefore, the demonstrated processes are expected to be applicable for 3D integration to meet high-density flash memory requirements.

BIOGRAPHICAL SKETCH

Jaegoo Lee was born in Jeonju, Jeonbuk province, South Korea on August 29, 1968 to parents Jonggeon Lee and Boksoon Baik. When he was 11 years old, his family moved to Seoul, the capital city of South Korea, where he received all his education from middle school to graduate school. In 1989, he entered Kwangwoon University in Seoul, and majored in Electronic Materials Engineering, where he developed a solid foundation in engineering and science, graduating with a B.S. degree in Feb. 1995 and a M.S. degree in Feb. 1997. His research at Kwangwoon University focused on the material growth and device fabrication of $Al_xGa_{1-x}Sb$ under the guidance of Professor Dong Chan Moon.

Upon completion of his M.S. program, he joined Samsung Electronics Company in Yongin, Korea and worked as a researcher with the Advanced Technology Team at the Semiconductor Research and Development Center until August 2004. His research projects at Samsung were 140nm and 90nm 1Gb (Giga bit) DRAM (Dynamic Random Access Memory).

To expand his expertise in electrical engineering, he joined the Ph.D. program at the School of Electrical and Computer Engineering at Cornell University in Ithaca, New York, U.S.A. from September 2004 to July 2009, during which time he was awarded the Samsung Fellowship for Ph.D. study from Samsung Electronics Company. At Cornell he worked with his advisor, Professor Edwin C. Kan, on three-dimensional integration flash memory with metal nanocrystals and high-k dielectric on polysilicon and Ge TFT. He has authored 29 publications and holds 13 U. S. patents in his research area.

To my mother, Boksoon Baik, wife, Jungeun Kong, sons, Donghoon and Jaehoon

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TABLE OF CONTENTS

Biographical Sketch ……...iii

Dedication ……..iv

Acknowledgments ……v

List of Figures ……...xi

List of Tables ……xvi

List of Abbreviations ……...……xvii

List of Symbols ……..……xix

CHAPTER 1: Introduction ……1

1.1 Review of Memory Technology 1

1.2 Flash Memory Trend 3

1.3 High-k Dielectric 6

1.4 Stackable Flash Memory Cell for 3-D Integration 9

1.5 Overview of Dissertation 12

REFERENCES 14

CHAPTER 2: 3-D INTEGRATION FLASH MEMORY CELL……20

2.1 Planar Polysilicon UTB TFT Cell 20

2.1.1 Motivation 20

2.1.2 The Concept of Ultra-Thin Body TFT 21

2.1.3 CMP Process 24

2.2 Ni Silicidation 30

2.2.1 Motivation 30

2.2.2 Nickel Silicide (NiSi) Formation 31

2.3 Ge Thin Film Transistor (TFT) 34

2.3.1 Ge Oxide Treatment 34

2.3.2 High-k/Ge Gate Stack 37

2.4 Nanocrystal Floating-Gate Memory with High-k Tunneling Barrier 42

REFERENCES 44

CHAPTER 3: PLANAR POLYSILICON TFT WITH Au NC AND HIGH-K DIELECTRICS ……50

3.1 Motivation 50

3.2 Polysilicon TFT with Single Au NC and $(Ti,Dy)_xO_y$ High-k Dielectric 51

3.2.1 Device Fabrication and Material Characterization 51

3.2.2 Electrical Characterization 57

3.3 Polysilicon TFT with Single Au NC and Al_2O_3 High-k Dielectric 59

3.3.1 Device Fabrication and Material Characterization 59

3.3.2 Electrical Characterization 63

3.4 Polysilicon TFT using Double Au NC and Al_2O_3 High-k Dielectric 65

3.4.1 Device Fabrication and Material Characterization 65

3.4.2 Electrical Characterization 68

REFERENCES 72

CHAPTER 4: FULL SILICIDATION PROCESS ……..……76

4.1 Motivation 76

4.2 Device Fabrication and Material Characterization 76

4.3 Electrical Characterization 78

REFERENCES 83

CHAPTER 5: PLANAR Ge TFT FLASH MEMORY CELL ……..……86

5.1 Motivation 86

5.2 Device Fabrication and Material Characterization 87

5.3 Electrical Characterization 90

REFERENCES 95

CHAPTER 6: CONCLUSIONS AND FUTURE WORK…….....98

6.1 Conclusions 98

6.2 Future work 99

REFERENCES 101

APPENDIX 1 .....…...……...……...…….....103

APPENDIX 2 .....…...……...……...…….....109

APPENDIX 3 .....…...……...……...…….....115

LIST OF FIGURES

Figure 1.1 ITRS roadmap for NAND flash transistor ……1

Figure 1.2 Schematic cross section of a floating-gate memory device ……3

Figure 1.3 Energy band diagram of floating gate memory cell at (a) equilibrium, enlarged conduction band edge of floating gate/tunneling barrier/ substrate at (b) programming and (c) erase states ……4

Figure 2.1 Vertical structures (schematics of (a) Samsung and (b) Toshiba) of promising candidates for 3-dimensional (3-D) integration of flash memory cells ……22

Figure 2.2 Schematics and channel potentials of (a) conventional TFT without CMP and (b) the proposed CMP processes ……23

Figure 2.3 (a) Schematic of chemical mechanical (CMP) process and (b) experimental apparatus of CMP process ……26

Figure 2.4 AFM results according to CMP factors ……28

Figure 2.5 The schematic of CMP process and statistical distribution of thickness. (a) After polsilicon deposition, (b) without the HF dip process, (c) with the HF dip process and (d) after polysilicon CMP processOxide electric field at the SiO_2/Si interface and tunneling current density into NCs as a function of the NC spacing ……29

Figure 2.6 Schematic diagrams for nickel silicide formation between in Ni and polysilicon ……33

Figure 2.7 Schematic on the effect of annealing on ZrO_2/Ge gate stack (a, b) and Al_2O_3/Ge gate stack (c, d) ……39

Figure 2.8 (a) BF-STEM image of a single NC layer embedded in the Ge gate stack, (b) CBED pattern of Al_2O_3 layer at Al_2O_3/Ge gate

stack ……40

Figure 2.9 (a) DF-STEM image of a single layer Au NCs Ge TFT gate stack, (b) Al EELS edge (taken from line A), (c) O EELS edge (taken from line A), (d) Cr EELS edge (taken from line A), and (d) Ge EELS edge (taken from line B) ……41

Figure 3.1 (a) Vertical device schematics of a UTB TFT memory with metal NC charge storage and $(Ti,Dy)_xO_y$ tunneling barriers and (b) the main process sequence ……52

Figure 3.2 The polysilicon removal rate and standard deviation of the film thickness under different CMP conditions ……53

Figure 3.3 3 μm × 3 μm AFM images of polysilicon thin film: (a) before CMP and (b) after CMP ……54

Figure 3.4 (a) BF-STEM image of a single NC layer embedded in the $(Ti,Dy)_xO_y$ gate stack, CBED patterns of (b) $(Ti,Dy)_xO_y$ layer, and (c) polysilicon layer ……56

Figure 3.5 (a) DF-STEM image of a Au NC TFT gate stack with a (Ti,Dy)O layer, (b) Si and Dy EELS edge, (c) Ti EELS edge, and (d) O EELS edge ……56

Figure 3.6 Lack of memory window in control polysilicon TFT without Au NC. W/L = 50 μm /45 μm ……57

Figure 3.7 Output characteristics of the $(Ti,Dy)_xO_y$/Au/$(Ti,Dy)_xO_y$ TFT device……58

Figure 3.8 Transfer characteristics with gate voltage sweeps for $(Ti,Dy)_xO_y$/ Au/$(Ti,Dy)_xO_y$ TFT flash memory cells ……58

Figure 3.9 (a) Vertical device schematics of a UTB TFT memory with metal NC charge storage and Al_2O_3 tunneling barriers and (b) the main process

sequence 59
Figure 3.10 BF-STEM image of single Au NCs TFT gate stack embedded in $Al_2O_3/(Ti,Dy)_xO_y$ layers 60
Figure 3.11 (a) DF-STEM image of single Au NCs TFT gate stack embedded in $Al_2O_3/(Ti,Dy)_xO_y$ layers, (b) Dy EELS edge, (c) Ti EELS edge and (d) O EELS edge (taken from line A) 61
Figure 3.12 (a) Size distribution of Au NCs deposited by e-beam evaporator on ALD Al_2O_3 and (b) an SEM image 62
Figure 3.13 Lack of memory window in control polysilicon TFT without Au NC (*W/L* = 50 μm/45 μm) 63
Figure 3.14 Output characteristics of $Al_2O_3/Au/(Ti,Dy)_xO_y$ TFT device 64
Figure 3.15 Transfer characteristics with gate voltage sweeps for $Al_2O_3/Au/(Ti,Dy)_xO_y$ TFT flash memory cells 65
Figure 3.16 (a) Structure and (b) process sequence of a double-layer nanocrystal TFT memory 66
Figure 3.17 (a) STEM image of the double-layer Au NCs TFT gate stack. (b) Ti EELS edge appears at 455 eV while O edge appears at ~525 eV. Si edge was also observed, but not shown here 67
Figure 3.18 (a) Transfer and conductance characteristic of polysilicon TFT, (b) transfer characteristics of lack of memory window in control TFT without Au NC. (*W/L* = 50μm/45μm) 69
Figure 3.19 Output characteristics of polysilicon TFT with double layer NCs ...70
Figure 3.20 Transfer characteristics with gate voltage sweeps for Au double NCs layer TFT flash memory cells 70
Figure 3.21 Retention time for TFT flash memory cells with single- and double-NCs gate stack 71

Figure 4.1 (a)Vertical structure of Au NCs embedded in Al_2O_3/(Ti,Dy)O gate stacks on SAS polysilicon TFT and (b) process sequences using SAS process ……77

Figure 4.2 3-D tomographic image of self-assembled Au NCs ……78

Figure 4.3 (a) Test pattern for sheet resistance measurement of NiSi film after annealing, (b) the cross section of the test structure and (c) sheet resistance of the NiSi film of 13 nm thickness after various annealing temperatures ……79

Figure 4.4 Lack of memory window in control FUSI polysilicon TFT without Au NC. *W/L*=50μm /45μm using SAS process ……80

Figure 4.5 Output characteristics of polysilicon TFT with and without SAS process ……81

Figure 4.6 Transfer characteristics with gate voltage sweeps for Au NCs TFT flash memory cells using SAS process with various voltage sweep ranges ……81

Figure 4.7 Retention time for Au NCs TFT flash memory cells using SAS process under 5V writing and -5V erasing conditions ……82

Figure 5.1 (a)Vertical structure of Au NCs embedded in Al_2O_3/(Ti,Dy)O gate stacks on Ge TFT and (b) process sequences Ge TFT process ……88

Figure 5.2 3 μm × 3 μm AFM images of Ge thin film: (a) as-deposited without CMP, (b) with CMP, 4psi-15RPM-15RPM (back pressure-table rotation speed-chuck rotation speed), (c) 4psi-25RPM-15RPM, (d) 4psi-15RPM-25RPM and (e) 4psi-25RPM-25RPM ……..89

Figure 5.3 Lack of memory window in control Ge TFT without Au NC (*W/L*=50 μm /45 μm) ……91

Figure 5.4 Output characteristics of the planar Ge TFT ……91

Figure 5.5 Transfer characteristics with gate voltage sweeps for Ge TFT flash memory cells with Au NCs ……..92

Figure 5.6 Retention time for Ge TFT flash memory cells with Al_2O_3/Au/ $(Ti,Dy)_xO_y$ gate stack ……93

Figure 5.7 Write/erase time test of Au nanocrystal Ge TFT at ±5V ……93

Figure 5.8 Cycle endurance characteristics of Au nanocrystal Ge TFT at ±5V ……94

LIST OF TABLES

Table 1.1 Material characteristics of high-k dielectric …… 7

Table 2.1 Chemical mechanical polishing condition …… 27

Table 2.2 The material characteristics of promising channel materials Chemical mechanical polishing condition …… 35

Table 2.3 Material characteristics of Ge oxides and Si dioxide …… 36

Table 3.1 The CMP process chosen in this study for the UTB TFT …… 53

Table 3.2 The statistical parameters of Au NCs …… 54

LIST OF ABBREVIATIONS

3-D	Three-Dimensional
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BF-STEM	Bright-Field Scanning Transmission Electron Microscopy
BiCS	Bit-Cost Scalable
BJT	Bipolar Junction Transistor
CBED	Convergent Beam Electron Diffraction
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
CNF	Cornell Nanoscale science and technology Facility
CNS	Center for Nanoscale Systems
CVD	Chemical Vapor Deposition
DIBL	Drain Induced Barrier Lowing
DRAM	Dynamic Random Access Memory
DF-STEM	Dark-Field Scanning Transmission Electron Microscopy
EELS	Electron Energy Loss Spectra
EOT	Equivalent Oxide Thickness
EUV	Extreme Ultra-Violet
FET	Field Effect Transistor
FN	Fowler-Nordheim
FRAM	Ferroelectric Random Access Memory
GOI	Ge-On-Insulator
ITRS	International Technology Roadmap for Semiconductor

LOR	Lift-Off Resist
MRAM	Magnetoresistive Random Access Memory
MOS	Metal-Oxide-Semiconductor
NCs	Nanocrystals
P/E	Program/Erase
PECVD	Plasma Enhanced Chemical Vapor Deposition
RF	Radio Frequency
RMS	Root Mean Square
RPM	Rotation Per Minute
S^3	Single-crystal Si layer Stacking
SAS	Self-Aligned Silicidation
SEC	Samsung Electronics Company
SEM	Scanning Electron Microscopy
STEM	Scanning Transmission Electron Microscopy
SOI	Silicon-On-Insulator
SONOS	Silicon-Oxide-Nitride-Oxide-Silicon
TEC	Toshiba Electronics Company
TFT	Thin-Film Transistor
ULSI	Ultra Large Scale Integration
UTB	Ultra-Thin Body

LIST OF SYMBOLS

a	Lattice constant
$dlog\ (I_d)$	Differential log drain current
dV_g	Differential gate voltage
E_{C_FG}	Floating gate conduction band energy level
E_{C_sub}	Substrate conduction band energy level
E_g	Energy bandgap
FG	Floating gate
I_{dsat}	Maximum drive current
I_{off}	Off state drain current
I_{ON}	Drive current
J_g	Gate leakage current density
k	Dielectric constant
N_C	Effective density of states in conduction band,
N_V	Effective density of states in valence band,
S	Sub-threshold slopes
T_m	Melting point
V_{CG}	*Control gate volatge*
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
V_T	Threshold voltage
e^-	Electron
χ	Electron affinity
$\mu_{e/}\mu_h$	Electron mobility/ Hole mobility

CHAPTER 1

INTRODUCTION

1.1 Review of Memory Technology

The semiconductor industry has been steadily growing since the development of the first integrated circuits. Metal-oxide-semiconductor (MOS) devices continue to be scaled to achieve the basic goals of VLSI semiconductor manufacturers. As a result, the number of transistors on a chip has doubled every two years and it is predicted that this trend will continue until 2018 [1]. According to the International Technology Roadmap for Semiconductor (ITRS), it is anticipated that gate length will be scaled down to 32 nm by the year 2011 as shown in Figure 1.1 [2].

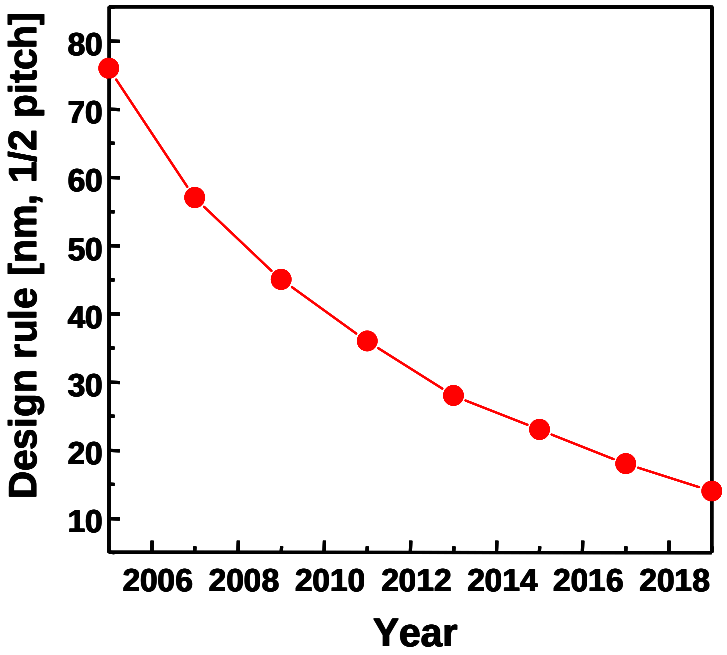

Figure 1.1 ITRS roadmap for NAND flash transistors.

During the next decade, device scaling challenges are expected to proliferate. The most severe problems include lithography, process integration and control, gate oxide thickness scalability, increased parasitic capacitance and resistance, novel material integration, and escalating development cost and time. Ever-increasing scaling demands and decreasing operational voltage also make it difficult to develop high-performance memory devices with faster read/write, longer retention, higher endurance, lower voltage/power operation, and higher density [3].

The solid-state memories can be categorized as volatile and nonvolatile memories according to their data retention capabilities. A typical volatile memory, dynamic random access memory (DRAM), which consists of one transistor and one capacitor, offers very high density and low cost per bit, but requires periodic refreshing or rewriting due to short retention time [4].

In contrast to the volatile high-speed memory of DRAM, flash memory can retain its data for at least 10 years without a power supply. However, its slow write/erase operations, limited endurance, and poor scaling require further improvement and new technologies [5-7].

Ferroelectric random access memory (FRAM) has been introduced as a potential replacement for the flash memory [8-12]. However, problems such as poor reliability due to fatigue [13] and imprint [14] of PZT, as well as poor scaling and high fabrication costs, need to be resolved before FRAM can be a viable alternative in the memory market. Another candidate is the magnetic random access memory (MRAM) [15-20]. Here, fabrication issues such as CMOS compatibility of magnetic materials and tight thickness control of the tunnel junction insulator are the main challenges [21]. Phase-change random access memory (PRAM) is another resistance-change-based memory similar to MRAM [22-26]. As the scaling proceeds, potential concerns

regarding thermal disturbance to adjacent bits must be addressed. [27]. In summary, even though new technologies are emerging, thus far none has proved to be the competitive substitute for conventional flash memories.

Despite enormous challenges facing the development of memory devices, the continuous improvement of flash memory in terms of fabrication, structural design, and operational schemes has strengthened their competitiveness in the market. However, reliability concerns accompanied by the aggressive scaling-down of the device geometries in order to achieve high density remain the primary obstacles for the future of the charge-storage-based approach.

1.2 Flash Memory Trend

The floating gate structure has been most popularly used for the nonvolatile memory application, as first proposed by S. M. Sze of the Bell Labs [28]. The schematic cross section of a floating-gate memory device is shown in Figure 1.2.

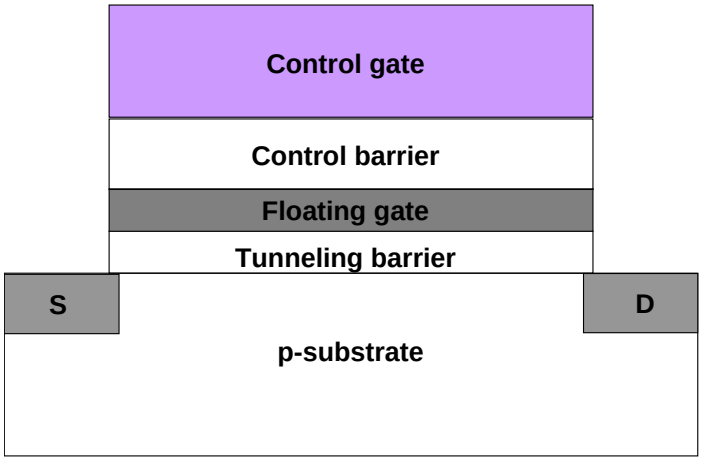

Figure 1.2 Schematic cross section of a floating-gate memory device

The upper gate in Figure 1.2 is the control gate, and the lower gate, which is completely isolated by dielectrics, is the floating gate. This floating gate acts as a potential well. Once the charges are injected into the potential well, they can hardly escape without an external electric field. In this device structure, the programming and erasing of the memory cell are implemented by applying a positive and negative electric field to the control gate, respectively, as shown in the band diagram in Figure 1.3.

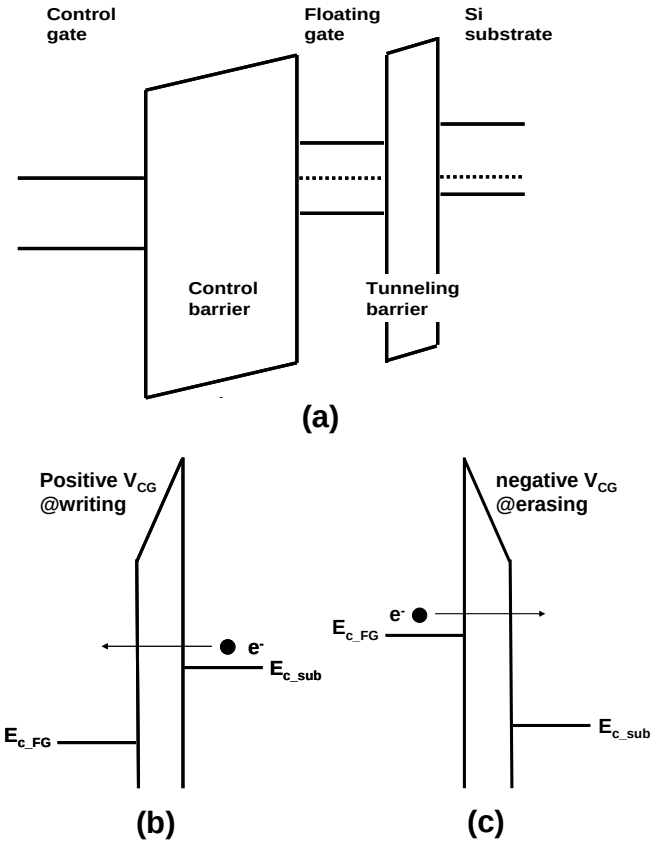

Figure 1.3 Energy band diagram of floating gate memory cell at (a) equilibrium, enlarged conduction band edge of floating gate/tunneling barrier/substrate at (b) programming and (c) erase states.

Therefore, programming and erasing operations depend not only on the applied electric field, but also on the tunneling current through the dielectric between the floating gate and the substrate, namely the tunneling barrier. For this reason, it is very important to scale down the tunneling barrier both for the low voltage and high speed operation of the memory cell by providing enough tunneling current [29]. However, the scaling down of the tunneling barrier is severely limited. For instance, the data retention characteristics which are also determined by the tunneling current (leakage current in this case) with zero gate bias must be considered in order for the memory cell to provide sufficient nonvolatility.

In conventional floating gate structure, percolation defects in the tunneling barrier will result in the whole charge loss. Similarly, charge losses along the lateral path to the source and drain can be a serious problem [30]. Moreover, the electrostatic potential is very high in the floating gate structure when the memory cell is programmed, resulting in high leakage current through the tunneling dielectric. These various leakage sources induce significant charge losses in the memory cell, resulting in the degradation of data retention. This trade-off between programming efficiency and data retention has been a fundamental limitation in scaling down the tunneling barrier. For that reason, nanocrystal floating-gate structure was introduced to overcome scaling limitation [31].

Because the nanocrystal floating gate structure has every nanocrystal electrically and physically separated in the cell, the local defects in the tunneling dielectric and/or the leakage current through the lateral path to the source and drain may cause the charge loss of only one or a few nanocrystals, maintaining the stored charges in the rest [32].

1.3 High-k Dielectric

There are two basic types of device scaling strategies in MOSFET logic technology: constant field scaling and constant voltage scaling, although in practice they are often used in a mixed manner to give the best overall performance and compatibility. In order to understand the device scaling factor on critical device operations, we will need to establish a minimalistic set of design parameters. When a MOSFET is turned on, the key electrical parameters are I_{dsat} (maximum drive current) , V_T (threshold voltage), and the DIBL (Drain Induced Barrier Lowing) effect that changes the threshold voltage and self gain. When turned off, the parameters are I_{off} (off state drain current) and the sub-threshold swing ($dV_g/d\log(I_d)$), which is also affected by DIBL.

These on/off characteristics should be closely monitored when the MOSFET device is scaled down. In order to achieve the required turn-off characteristics, the gate oxide thickness, source drain junction depth, and operating voltage must be decreased. In the 2007 ITRS road map [2], the required gate oxide thickness for 32 nm transistor is 0.5 - 1.0 nm. But in this thickness range, direct tunneling is dominant for SiO_2, which means that silicon oxide leakage can be greater than 10 A/cm^2. This is not an acceptable level for standby power consumption. Furthermore, the absolute scaling limit of pure silicon dioxide is believed to be 7 Å, since the wave length penetration effect is 3.5 Å for each surface of silicon dioxide [28]. Therefore, SiO_2 films less than 7 Å will hardly function as an insulator. SiO_2 has been used in the MOSFET process for more than 30 years due to its superior chemical stability, outstanding thermal stability, excellent dielectric performance, low interface state densities, diffusion barrier properties, low leakage current and good reliability performance. When we consider the selection of an alternative gate dielectric for a sub-30 nm MOSFET

process, characteristics such as high thermodynamic stability, low impurity diffusion coefficient, high interfacial layer quality, and large barrier height (>1 eV) for electrons and holes [33-35] should be considered. A wide range of high-k dielectric in Table 1.1 has been studied [36, 37].

Table 1.1 Material characteristics of high-k dielectric.

Material	Method	ε_r	E_{br} (MV/cm)	Stored energy density $\varepsilon E_{br}^2/2$ (J/cm^3)	Stored charge Q_{max} (μC/cm^2)
Al_2O_3	wet anodized	6	8	17	4.3
	reactive sputter	8	6	13	4.3
Ta_2O_5	wet anodized	25	6	40	13.3
	reactive sputter	23	4	16	8.2
ZrO_2	wet anodized	21	4	15	7.4
	reactive sputter	24	4	17	8.5
SiO_2	thermal oxidation (MOS gate oxide)	3.9	18	57	6.2
	reactive sputter	3.9	10	17	3.5
$(Ba,Sr)TiO_3$	CVD	400	0.1	0.2	3.5
$Ti_{0.8}Dy_{0.2}O_x$	reactive sputter	47	2.5	13	10.4
$Zr_{.25}Sn_{.42}Ti_{.33}O_2$	reactive sputter	27	7.6	70	18.2

Here, band alignment becomes critical [38]. For example, Ta_2O_5 (tantalum has a much lower gap for electrons than SiO_2, which results in high leakage problems due to Schottky emission of carriers into the band states. Ta_2O_5 has been studied extensively for capacitor application, having a reasonably large band gap of 4.4 eV.

However, as its electron barrier height with silicon is only 0.36 eV, high leakage current at high operation temperature is inevitable. On the other hand, $(Ti,Dy)_xO_y$ and Al_2O_3 have acceptable barrier heights for both electrons and holes, minimizing Schottky emission and making these compounds attractive candidates for gate dielectric application. Consequentlyafter 2005, microprocessor manufacturers have begun integrating high-k dielectrics and metal gates into mainstream silicon integrated circuits [39].

Fundamentally, high-k dielectrics are electrical insulators with significant polarizability in an electric field. This high polarization enables a high charge buildup on the oxide's electrodes when minimal voltage is applied, thus minimizing the power necessary to switch a transistor. The energy $(\varepsilon_r\varepsilon_0 E_{br}^2)$ and charge $(\varepsilon_r E_{br})$ storage capacities are listed in Table 1.1 as well.

Sputtering deposition and atomic layer deposition (ALD) are common tools in researching dielectric oxides [40]. In the conventional manufacturing, another deposition technique, chemical vapor deposition (CVD), is more common for depositing the dielectric material in high performance transistors in consideration of the low global defect density [41]. Chemical vapor deposition, along with its many derivatives, is a versatile deposition technique for oxides, nitrides, carbides, and metals [42]. The desired film components are introduced into the reaction chamber as volatile compounds which react in the gas or on the substrate [43].

ALD is a related technique, which relies on sequential introduction of each precursor compound into the chamber, separated by vacuum pump-out or purging cycles of argon [43]. Precursors are chosen which do not self-react, and because each precursor is introduced individually, at most a monolayer of material can be deposited with each cycle, controlled by surface adsorption. For oxide deposition, a volatile

compound of the metal ($AlCl_3$, $Al(CH_3)_3$, or $TiCl_4$, or $HfCl_4$) is sequentially introduced with water vapor [44]. The technique affords strong control of the oxide thickness and conformity to step edges, highly desirable for the convoluted structures of non-planar transistor geometries.

Some high-k dielectric materials, including Ta_2O_5 [45] and TiO_2 [30], have been found to be thermally unstable in direct contact with polysilicon substrate. The use of thermo-dynamically stable high-k dielectric in direct contact with polysilicon is needed to integrate simple gate structure. ALD Al_2O_3 and $(Ti,Dy)_xO_y$ are two of the most promising high-k materials in this regard. Replacement gate technology was used in order to avoid the exposure of metal to high-temperature source drain activation annealing.

1.4 Stackable Flash Memory Cell for 3-D Integration

Three-dimensional (3-D) integration is an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies and functional components together [46, 47]. The potential benefits of 3-D integration can vary depending on approach. They include multi-functionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration and reduced overall costs. The industry paradigm will shift to a new industry-fusing technology era that will offer tremendous global opportunities for expanded use of 3-D silicon-based technologies in highly integrated systems.

Recently, the great demand for higher density and lower bit cost in NAND flash memories is growing because these devices are keys for mass data storage applications in various portable electronic products, such as portable audio and video

players, cellular phones, USB memories and newly introduced solid state disks for mobile PCs.

In order to continue reducing the bit cost and increasing the bit density, the linear shrink of the patterns has been aggressively pursued by developing MLC (multi level cell) technology and early adoption of advanced lithographic tools [1]. However, the linear scaling down of the NAND flash memories is approaching the physical, electrical and reliability limitations, especially as the dimension of the technology node is below 30 nm.

First, EUV (extreme ultra-violet) lithography must be used for the patterning, since other nano-scale lithography based on scanning such as E-beam and nanoimprint still involves too much cost per chip due to the low throughput. The EUV technology, combined with immersion, is expected to be available after the year 2009, according to the ITRS roadmap [2]. Even when the tool is prepared, its cost will be quite high and its throughput will not be comparable to that of the conventional ArF lithography. In terms of the bit cost, even if the dimensions are shrunk and the density is increased, the bit cost may not continue its historical downward trend. Therefore, the economic need for increasingly small devices with higher density will diminish and the bit growth rate in the data storage applications will likely slow down if only a single layer of active memory is implemented in the chip area.

Secondly, from the electrical and reliability perspectives, shrinking the dimensions of the device to smaller than 30 nm will cause serious problems such as electrical isolation between the word-lines and the cell nodes, short channel effect, cell current reduction and tolerable charge losses of the stored charges for data retention even in newly developed SONOS (Silicon-Oxide-Nitride-Oxide-Silicon)-like structures.

Furthermore, these problems result from fundamental physical limits, which are difficult to overcome by the conventional modifications used in past nodes. Therefore, one of the best ways to circumvent these barriers caused by simple conventional linear shrinking technology is to stack the cell arrays in a 3-D manner while minimizing the additional stacking processes. An easy solution to increase density has been to stack chips or packages using bonding or packing technology. However, this stacking process does not reduce the bit cost nor the fabrication costs because they stack chips which have already been completely integrated.

Heat dissipation is a major concern in 3-D integration whether in the chip or packaging level. This will pose a performance improvement limit for most logic circuits. The 3-D integration technology for better control of heat dissipation is out of scope of this thesis. Fortunately, for 3-D integration of memory arrays, heat is much less a problem due to the very low percentage of device activation.

Recently, Bit-Cost Scalable (BiCS) flash technology has been introduced as a promising candidate [45]. With BiCS, an entire stack of electrode plates is punched through and plugged with poly-silicon all at once, forming a series of vertical FETs which act as a NAND string of SONOS-type memories. The memory FETs work in depletion-mode with the body polysilicon being undoped or lightly n-doped uniformly, which avoids the process complexity of forming p-n junctions within the plug. Each plate acts as a control gate with the exception of the lowest plate which functions as the lower select gate. However, certain fabrication issues, such as polysilicon surface roughness and non-uniformity of tunnel dielectric material due to step coverage need to be resolved before BiCS can become a viable and attractive alternative in the flash technology market. Another candidate is single-crystal Si layer stacking (S^3) technology [46]. In S^3 technology, the Si active layers are stacked with minimum

processes and are interconnected simultaneously with the bottom cell arrays and the peripheral circuits. Also, its electrical characteristics have been improved by reducing the capacitive and resistive loading without reducing the cell current. Its high-cost process and low-throughput due to adapting the epitaxial-layer growth are the main challenges facing this technology.

In this thesis effort, we propose novel planar UTB TFT based on deposited polycrystalline silicon or germanium as the technology capable of overcoming all aforementioned problems with its better process compatibility and cost-effectiveness for 3-D integration of flash memory cells.

1.5 Overview of Dissertation

From the fabrication process point of view, the memory device for 3-D integration must meet three major requirements. The first is compatibility with conventional process for cost-effective mass production. The second requirement is the floating-gate itself for reliable data retention and data endurance. The third is the dielectric integrity for control and tunneling barriers. This dissertation focuses mainly on what effects these three parts of the memory structure have on the electrical characteristics. The dissertation is organized as follows.

Chapter 1 introduces the background for this research and provides a basic description of the floating-gate memory device. Our motives for focusing on the metal nanocrystal floating gate are also discussed. The role of the tunneling barrier on the floating-gate nonvolatile memory structure is presented along with the importance of using high-k dielectric as a replacement of the conventional SiO_2 for the control and tunneling barriers. Also, an outline is provided in order to introduce the overall ideas of the dissertation.

Chapter 2 investigates the process characteristics of direct-deposit self-assembly metal nanocrystal formation and the physical characterization of high-k dielectric, self-aligned silicidation (SAS) and the Ge channel material. The chemical mechanical polishing for obtaining a uniform ultra-thin-body film is also studied for 3-D integration flash memory cell.

In Chapter 3, the tunneling barriers in a nanocrystal memory device are studied. The effects of the various tunneling barriers on the data retention and memory window are investigated with the experimental results. $(Ti,Dy)_xO_y$ and Al_2O_3 high-k dielectrics are proposed for the tunneling barrier as a means to prolong the data retention and enhance the memory window simultaneously. Chapter 3 also describes double layer metal nanocrystal floating gate memories as a means to further improve retention time and charge storage capacity.

Chapter 4 presents the fabrication of self-aligned silicidation (SAS) for the reduction of contact resistance near source and drain regions for UTB TFT. Both structural analysis and electrical characterization are performed.

The Ge TFT process is proposed in Chapter 5, as a replacement for the conventional polysilicon process for the 3-D integration nonvolatile memory device. Structural analysis and electrical characterization are presented.

Finally, chapter 6 concludes the dissertation with a summary and suggestions for future research.

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CHAPTER 2

3-D INTEGRATION FLASH MEMORY CELL

2.1 Planar Polysilicon UTB TFT Cell

2.1.1 Motivation

The continuous scaling of MOSFET technology into the deep sub-micron regime poses considerable challenge to the conventional MOSFET structure. To suppress short-channel effects such as drain induced barrier lowering (DIBL) and V_T roll-off, extremely high levels of channel doping are required, but these result in increased leakage by band-to-band tunneling and degraded mobility.

To overcome the one-layer fabrication limit for conventional bulk MOSFET structure, polysilicon TFT has been widely studied. However, due to the formation of the grain boundaries along the polysilicon channel, the characteristics of the polysilicon TFTs show much smaller transconductance and larger threshold voltage than those of bulk devices. Specifically, polysilicon TFTs show more complex electrical characteristics than single crystal devices, such as the *kink effect*, a large increase of output conductance in the saturation region due to body charge or self heating. There have been some attempts to overcome these problems [1-4].

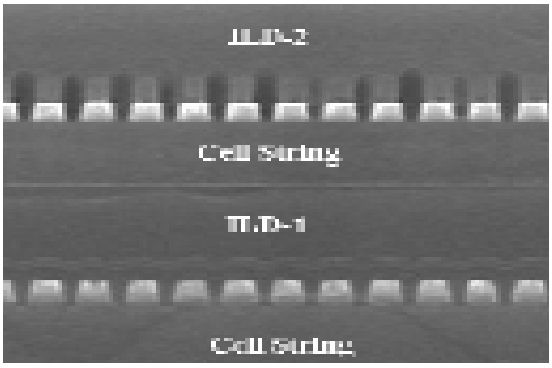
In this context, the ultra-thin body (UTB) MOSFET is one of the most promising alternative structures that effectively suppress DIBL and other short channel effects. The channel film thickness required is typically less than 30% of the gate length. The most difficult step for the fabrication of the ultra-thin body FET is the formation of a uniform, thin channel film with efficient source/drain contacts. Oxidation and etch back have been proposed [5], but are limited by the thickness uniformity of the starting SOI (silicon on insulator) wafers and by the process-induced

variation. On the other hand, deposited films can be well-controlled and have good uniformity. Therefore, establishing processes to form highly uniform ultra-thin channel material using chemical mechanical polishing (CMP) process step can be a competitive approach.

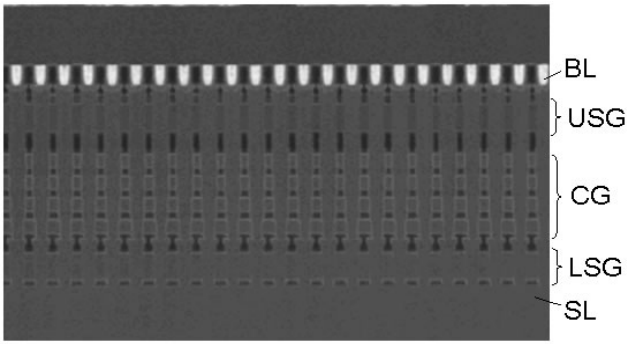
2.1.2. The Concept of Ultra-Thin Body TFT

Figure 2.1 shows two promising candidates for the 3-dimensional (3-D) integration of flash memory cells. The planar 3-D stacked NAND flash scheme by Samsung electronics company (SEC) as shown in Figure 2.1(a) has the advantage of being easily adapted to current technology [6]. One drawback is that it requires an additional lithography process for layer added. Alternately, in the Toshiba electronics company (TEC) scheme, the additional lithography step is not needed even though several layers are added onto the built-in structure as shown in Figure 2.1 (b) [7]. However, TEC technology has several problems such as scaling limitation of the contact opening diameter and surface roughness in the channel. To overcome these problems and easily adapt the technology for mass production, we need a new design for 3-D integration of flash memory cells. If the thickness of polysilicon is reduced, the total number of trap states and grain boundaries can be reduced as shown in Figure 2.2. This also makes the threshold voltage less sensitive to trap-density fluctuation when the flash memory cells operate. However, the TEC scheme ignores the surface roughness of the polysilicon channel in the step to adopt the vertical transistor in their flash memory cell, which made it impossible to get good surface roughness in the polysilicon channel because the CMP process cannot be adapted in the vertical structure. When the channel thickness is 100-200 nm, a few nanometers surface roughness is not critical. However, as the polysilicon channel thickness shrinks to the

proximity of tens of nanometers or even below ten nanometers, the issue of surface roughness will emerge due to surface scattering and a non-uniform electric field as shown in Figure 2.2 (a). To solve this problem, we introduce the CMP process to achieve the higher thickness and surface uniformity of polysilicon channel as shown in Figure 2.2 (b). The concept behind the UTB TFT is to reduce surface roughness and charge trap density which results in less threshold voltage fluctuation and a more uniform electric field at the interface between the tunnel barrier and the channel.



(a)



(b)

Figure 2.1 Vertical structures (schematics of (a) Samsung and (b) Toshiba) of promising candidates for 3-D integration of flash memory cells.

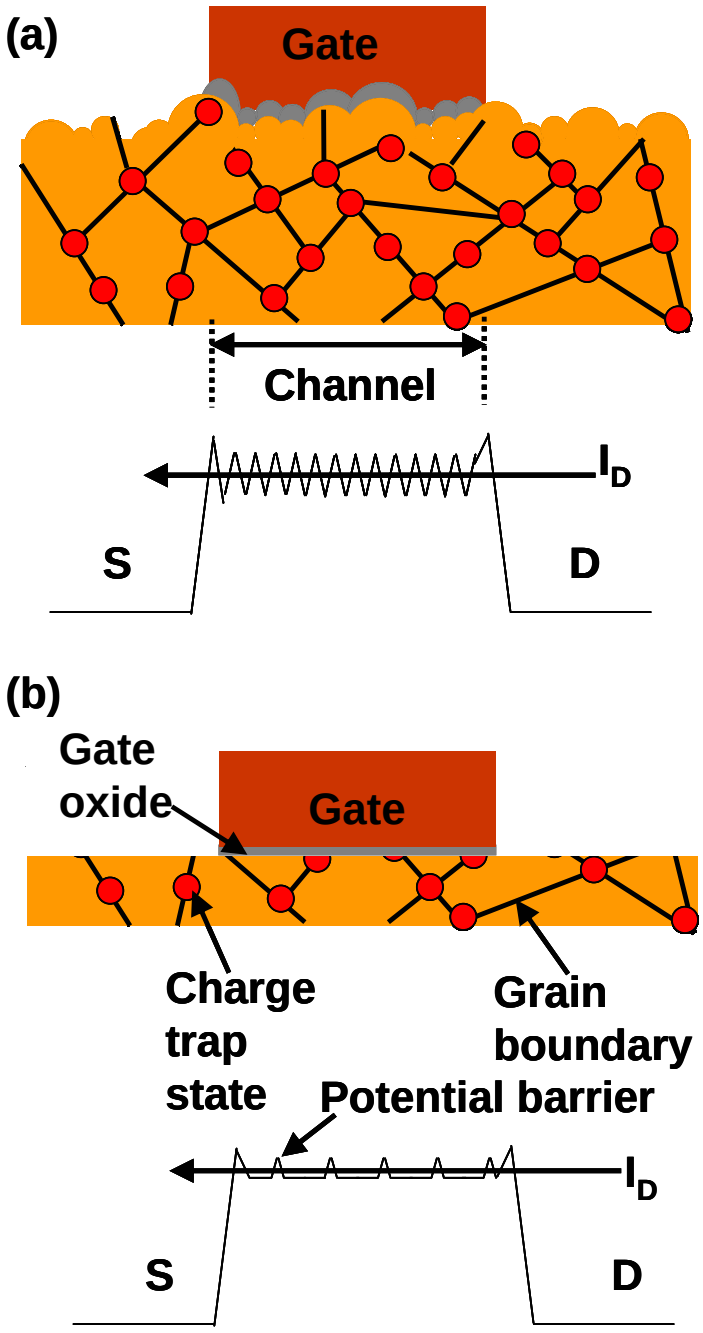


Figure 2.2 Schematics and channel potentials of (a) conventional TFT without CMP and (b) the proposed CMP processes.

2.1.3 CMP Process

Chemical mechanical polishing (CMP) is a useful tool for wafer-scale surface planarization in the semiconductor industry [8, 9]. The CMP process is essential to form the planarization of the interlayer dielectric, interconnection metal layers and polysilicon ultra-thin body TFT in multi-level technology.

The basic concept of the CMP process is that the wafer is held on a rotating carrier (holder) while the face being polished is pressed against a polishing pad attached to a polishing platen disk. For oxide, silicon and polysilicon polishing, alkaline slurry of colloidal silica (a suspension of SiO_2 particles), is used as the chemical abrasive. The size of the particles varies in the literature between 0.01 μm and 3 μm. The slurry is carried to the wafer by the porosity of the polishing pad. This slurry chemically attacks the wafer surface, converting the silicon to a hydroxilated form (with the OH^- radical), which is more easily removed by the mechanical abrasive.

Gross mechanical damage of the surface is prevented by the fact that the colloidal silica particles in the slurry are not harder than the oxide or silicon to be removed. Otherwise, the quality of the surface planarity would be limited by the diameter of the silica particles. CMP needs fewer steps compared to deposition/etch-back process and uses nontoxic substances. Furthermore, it has good removal selectivity and good controllability of rate. Another advantage of CMP lies in the global planarization. Since the size of the flat area on a chip becomes smaller, the quality of local planarization becomes worse. CMP process is essential in overcoming this problem in multi-stacking technology. Additional difficulties may arise for the filling of small holes in ULSI (ultra large scale integration) technology. CMP reduces the density of defects such as shorts and stringer due to residual metal [10]. Figure 2.3 shows the mechanism diagram and experimental apparatus of the CMP process.

During the ionization step, hydroxyl and aminium ions are formed. The hydroxyl ions in water then oxidize the surface of the polysilicon to form hydrous silica with the evolution of hydrogen [11].

Furthermore, there are several factors that have effects on the CMP process. Generally, the main factors are down pressure, table speed, chuck speed and slurry. To get high uniformity including local and global planarization in the wafer, one should carefully consider these factors. To control the subtle nature of the process, the removal rate of polysilicon should be less than 50 nm/minute. Polysilicon thickness variation in the wafer should also be below 10 nm. Table 2.1 shows the split conditions of the main factors. Figure 2.4 shows the AFM results according to the CMP factors.

The parameters in the experiment which were considered are slurry, down pressure, chuck speed and table speed. From these results, as shown in Table 2.1, poly slurry is superior to oxide slurry and sample #3 is the best CMP condition in terms of the root mean square (RMS) value. The results of surface roughness are in agreement with the removal rate and the standard deviation.

Figure 2.5 shows the schematic of the CMP process and the statistical distribution of thickness. After polysilicon deposition on the SiO_2, the thickness and the standard deviation of polysilicon are 100.9 nm and 2.5 nm, respectively, as shown in Figure 2.5(a). Before the CMP process, we need to carry out a diluted HF dip process to remove the native oxide. If this HF dip process step is skipped, the removal rate is drastically decreased due to the native oxide on the surface of polysilicon. This is because the removal selectivity of oxide and polysilicon is 1 to 300 during the specific CMP process as shown in Figure 2.5(b). After the HF dip, we can obtain a stable CMP process. The removal rate was 70 nm through 90 nm for 45 sec as shown

in Figure 2.5 (c). The thickness distribution in the 4-inch full wafer shows the desired Gaussian distribution as shown in Figure 2.5 (d). After completing the polysilicon CMP under optimal conditions, the average thickness and standard deviation of polysilicon are 19.1 nm and 6.4 nm, respectively.

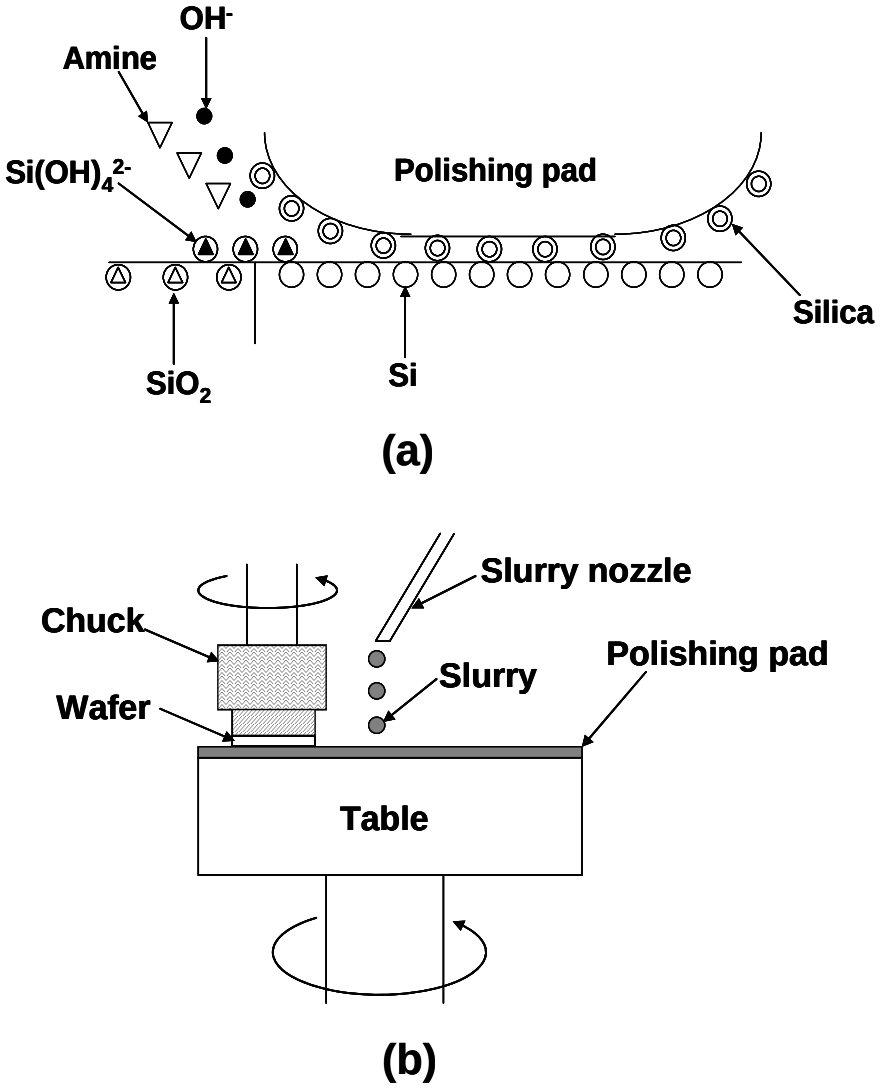


Figure 2.3 (a) Schematic of chemical mechanical (CMP) process and (b) experimental apparatus of CMP process

Table 2.1 Chemical mechanical polishing condition.

Factors / Sample #	Slurry	Down pressure [psi]	Chuck rotation speed [rpm]	Table rotation speed [rpm]	Root mean square [nm]
1	Poly	6	25	15	0.95
2	Poly	4	25	25	0.89
3	Poly	4	15	15	0.82
4	Poly	6	15	25	0.93
5	Oxide	4	25	15	1.65
6	Oxide	6	15	15	1.11
7	Oxide	4	15	25	2.28
8	Oxide	6	25	25	1.13

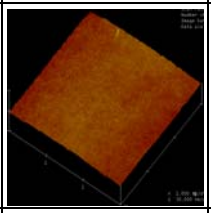
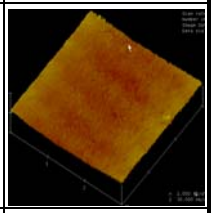
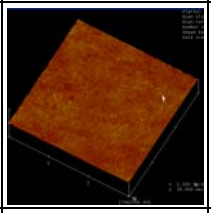
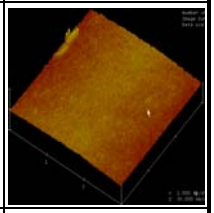
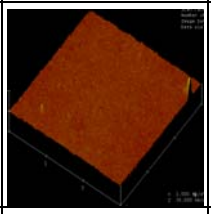
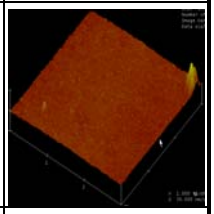
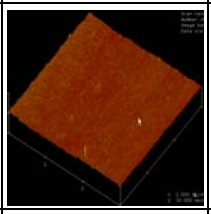
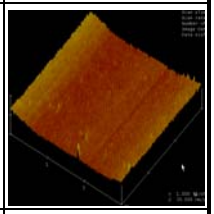
		6psi/25/15	4psi/25/25
Poly slurry	3D image		
	Roughness	0.954nm	0.892nm
		4psi/15/15	6psi/15/25
	3D image		
	Roughness	0.820nm	0.929nm
		4psi/25/15	6psi/15/15
Oxide slurry	3D image		
	Roughness	1.652nm	1.112nm
		4psi/15/25	6psi/25/25
	3D image		
	Roughness	2.275nm	1.127nm

Figure 2.4 AFM results according to CMP factors.

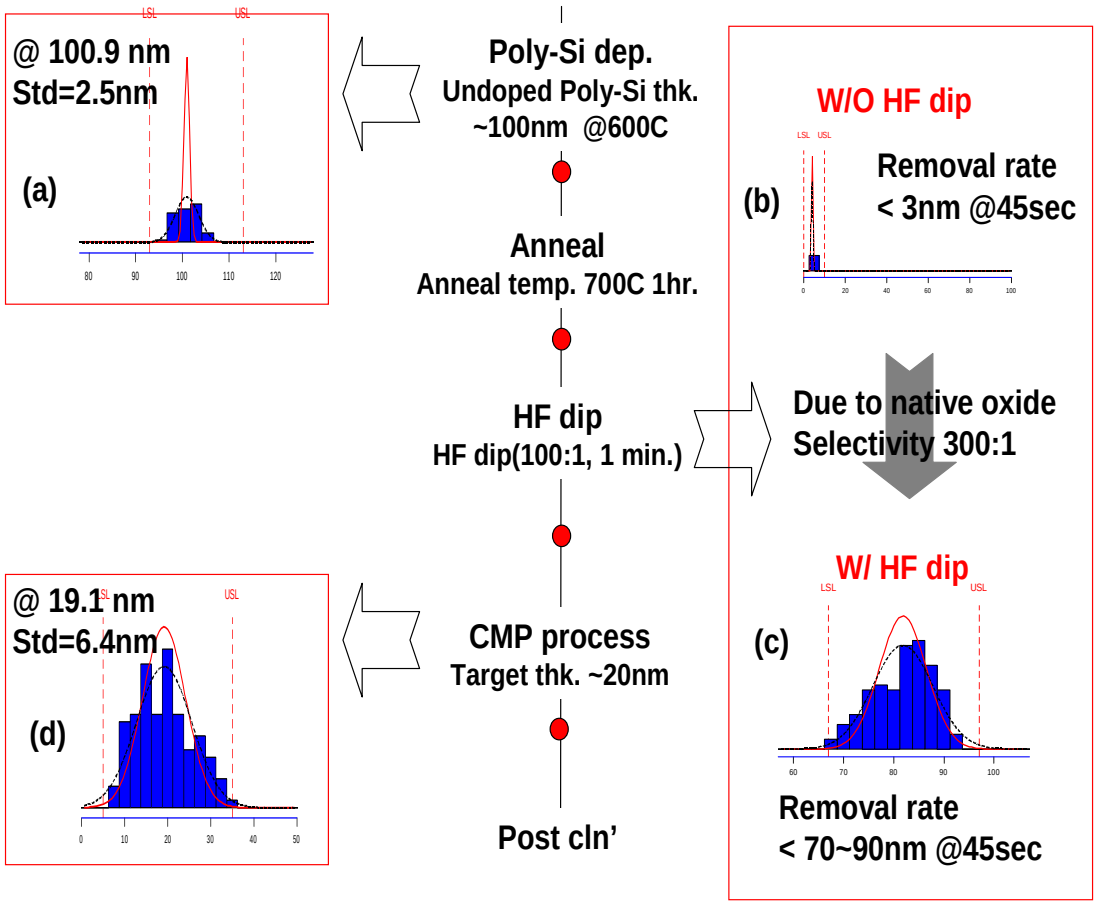


Figure 2.5 The schematic of CMP process and statistical distribution of thickness. (a) After polysilicon deposition, (b) without the HF dip process, (c) with the HF dip process and (d) after polysilicon CMP process.

2.2 Ni Silicidation

2.2.1 Motivation

Self-aligned silicidation (SAS) technology is widely used in submicron complementary metal-oxide–semiconductor (CMOS) manufacturing to reduce sheet and contact resistance of the gate, source and drain areas [12-16]. The silicide process is essential in UTB devices with several tens of nanometer thickness where contact resistance limits their performance. Silicides can be formed in two ways. The first is via a polycide process in which metal (Ti, Co or Ni) is deposited on polysilicon and both are then patterned. Alternately, in the SAS process, the polysilicon is deposited and patterned first, and then the metal is deposited. The unreacted metal is then removed by a selective wet etch. In both case, the silicide layer is formed by thermal reaction.

There are several metals such as Ti, Co, and Ni that can be used for SAS applications. It is very important to study various properties associated with these materials, *e.g.* process temperatures, time, resistivity, etchants, etch conditions and when the unreacted metal is removed. Some of the popular metal species that have been used for silicide processes include titanium di-silicide ($TiSi_2$), cobalt di-silicide ($CoSi_2$), and nickel silicide (NiSi).

Titanium silicide ($TiSi_2$) has long been used in silicide technology, but begins to show limitations in technology node of around 250 nm. It has difficulties in the formation of the low-resistivity layer on narrow polysilicon lines, and shows unwanted occurrences of polysilicon diffusion-dominated formation of silicides due to bridging issues [17, 18]

Cobalt silicide ($CoSi_2$) has replaced $TiSi_2$ in applications below the 250 nm technology node due to the line-width problems associated with $TiSi_2$ discussed above.

The $CoSi_2$ process has achieved somewhat better scalability for sub-250 nm nodes. However, $CoSi_2$ also exhibits limitations as the device dimensions are scaled down further. These problems include the difficulty associated in forming the low-resistivity $CoSi_2$ on line-widths less than sub-100 nm. $CoSi_2$ also suffers from high sensitivity to ambient contamination as well as high consumption rate of silicon and polysilicon.

Nickel silicide has emerged as one of the most promising candidates for silicide applications on sub-100 nm advanced technology devices. NiSi has many advantages over both titanium and cobalt di-silicides because of its low consumption rate of silicon and polysilicon, low-resistivity and the absence of narrow-line effects. The NiSi formation process can be accomplished by single-step annealing to form a low-resistivity NiSi layer followed by a high-selectivity etch process of the unreacted nickel. This study will investigate the properties and formation of NiSi on doped-polysilicon at the source and drain regions using the self-aligned silicidation (SAS) process.

2.2.2 Nickel Silicide (NiSi) Formation

The nickel silicide process is usually performed by depositing nickel on polysilicon followed by a thermal reaction treatment creating a metal-semiconductor compound that has different properties depending on the processing conditions. These conditions include the temperature at which the silicidation step is conducted, surface and ambient contamination, and self-aligned silicidation. For silicide formation on polysilicon, the thermodynamic driving force should be very similar to that shown on the crystalline Si. Although the polysilicon is at a higher energy state than single crystalline Si, the difference of energy state in Si is small compared with that polysilicon used in the silicides formation.

The process for full silicidation at the source and drain using self-aligned silicidation (SAS) is as follows: Ni films are deposited on doped-polysilicon wafers using e-beam evaporation. The polysilicon samples are cleaned with dilute buffered HF solution (30:1) to remove the native oxide on the surface before loading them into the evaporation chamber. The base pressure of the chamber is 1×10^{-7} Torr, and the evaporation rate is about 1 Å/s in a vacuum of better than 2×10^{-6} Torr. After the metal deposition, the NiSi is formed by thermal annealing at 600 ^{o}C in nitrogen ambient. The unreacted Ni on the wafer is removed by a selective etching solution (H_2SO_4:H_2O_2=4:1) at 60 °C for 10 minutes, without consuming the nickel silicide, oxide and polysilicon. The deposited Ni film thickness is measured by a crystal thickness monitor in the evaporation chamber.

Figure 2.2.1 shows the schematic diagram for nickel silicide formation by Ni and polysilicon. After depositing Ni on polysilicon substrate [see Figure 2.6 (a)], the formation of an intermixed amorphous Ni-Si layer at the interface occurs during the initial state of thermal annealing [see Figure 2.6 (b)]. The nickel silicide in the amorphous nickel silicide is then diffused [see Figure 2.6 (c)] and grown in the interfacial region of Ni and polysilicon [see Figure 2.6 (d)]. The desired phase of nickel silicide for this experiment was the nickel mono silicde (NiSi) which has been reported to form at temperatures around 450 °C to 700 °C allowing for a lower thermal budget [19-21]. At temperatures above 750 °C, the state of nickel silicide (NiSi) changes into nickel disilicide ($NiSi_2$), which has a higher-resistivity than the NiSi caused by polysilicon agglomeration in the NiSi film. This takes place at higher temperatures (>750 °C) causing a serious degradation in the performance of the devices. Therefore, when considering the silicide process conditions, it is important to understand the characteristics of the formed nickel silicide state depending on

temperature.

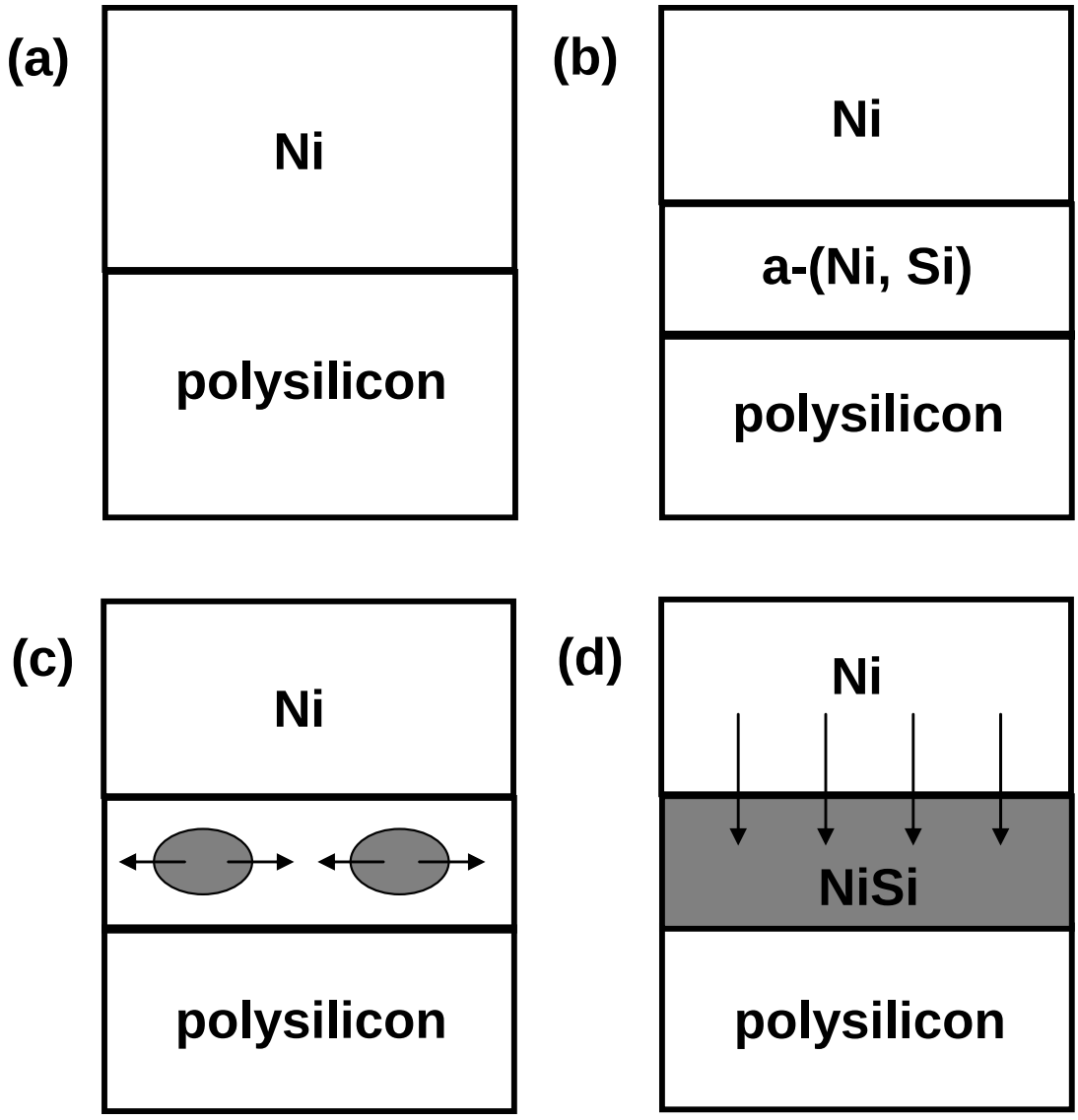


Figure 2.6 Schematic diagrams for nickel silicide formation between in Ni and polysilicon.

As for the SAS in the nickel silicidation process, the nickel will only react with polysilicon when nickel and polysilicon are in close contact in the source and drain regions. In Chapter 4, further details will be given on the fabrication of self-aligned silicidation (SAS) for the reduction of contact resistance near the source and drain regions. Both material and electrical characterizations are also performed.

2.3 Ge Thin Film Transistor (TFT)

2.3.1 Ge Oxide Treatment

The continuous achievement of high device performance is essential for the success of the semiconductor industry. This has been accomplished by simply scaling the feature size of transistors. However, the end of transistor scaling is forthcoming as the dimensions of transistors approach several tens of nanometers. The gate leakage current density (J_g) becomes unacceptably high when the physical thickness of SiO_2 has become less than 1.6 nm. Consequently, the conventional gate insulator (SiO_2) must be replaced by a high-k material for low power consumption.

Another technological requirement is speeding the low processing temperature and low contact resistance. The improvement of device performance such as high-speed device operation due to higher carrier mobility in the channel has been widely reported [22]. Table 2.2 shows the material characteristics of promising channel materials at the room temperature [23, 24].

In terms of high performance, Ge is one of the most promising materials due to several of its attractive material and electrical properties including higher carrier mobility [25] for larger drive current and smaller band-gap for supply voltage scaling and formation of low contact resistance. Since mass production of bulk Ge wafers is not yet cost-effective, Ge transistors will be fabricated on Si substrate as an UTB layer

such as Ge-on-insulator (GOI) [26-28].

We should carefully consider the material properties of Ge oxide layer, which are quite different from those of Si oxide even though Ge has advantages in terms of device performance. The Ge oxide layer should be removed from the UTB Ge surface because of its poor electrical characteristics as an insulator. Therefore, it is very important to understand and utilize the nature of Ge oxide. Table 2.3 summarizes the material characteristics of the Ge oxides [29–31]. It should be noted that solid-phase Ge monoxide, GeO (s), can exist at the process temperature for fabricating Ge MOSFETs. The material characteristics listed in Table 2.3 obviously depend on the oxidation condition and crystallinity.

Table 2.2 The material characteristics of promising channel materials.

	Si	Ge	GaAs
Bandgap, E_g [eV]	1.12	0.66	1.42
Electron affinity, χ [eV]	4.0	4.05	4.07
Hole mobility, μ_h [$cm^2V^{-1}s^{-1}$]	450	1900	400
Electron mobility, μ_e [$cm^2V^{-1}s^{-1}$]	1500	3900	8500
Effective density of states in valence band, N_V [cm^{-3}]	1.04×10^{19}	6.0×10^{18}	7.0×10^{18}
Effective density of states in conduction band, N_C [cm^{-3}]	2.08×10^{19}	1.04×10^{19}	4.7×10^{17}
Lattice constant, a [nm]	0.543	0.565	0.565
Dielectric constant, k	11.9	16.0	13.1
Melting point, T_m [°C]	1412	937	1240

GeO_2 is transformed from the hexagonal phase to tetragonal phase at 1033 °C by annealing because hexagonal or amorphous GeO_2 is a major phase at room temperature. However, GeO_2 is soluble in water. In contrast, GeO(s) is insoluble. The most important reaction to be considered is as follows:

$$GeO_2 + Ge \rightarrow 2GeO\ (s) \text{ or } 2GeO\ (g) \text{ at } 400\ °C \quad \text{(Eq. 2-1)}$$

Table 2.3 Material characteristics of Ge oxides and Si dioxide.

	GeO	GeO_2			SiO_2
Crystallinity	Amorphous	Hexagonal	Tetragonal	Amorphous	Amorphous
Dielectric constant	-	7	12	-	3.9
Solubility [g/100g, H_2O]	Insoluble	0.453 @25°C	0.00023 @25°C	0.5184 @30°C	Insoluble
Density [g/cm^3]	-	4.228	6.239	3.637	2.2
Transition temperature [°C]	-	1033			867
Melting point [°C]	710	1116	1086	-	~1600

The reaction on the left-hand side of Eq. (2-1) means that GeO_2 consumes Ge

at the interface. Meanwhile, the reaction on the right-hand side shows that GeO_2 on Ge not only changes into GeO (s) [32, 33] but also desorbs as gas-phase GeO (g) at 400°C [34, 35]. Since the dielectric constant of Ge oxide is as low as 7, complete removal of Ge oxide at the high-k/Ge interface is essential to achieve a thin equivalent oxide thickness (EOT) below 2.5 nm.

We have explored the efficacy of several methods which result in complete absence of Ge oxide at high-k dielectric and Ge interface. One of the most effective methods to remove the amount of Ge oxide prior to high-k film deposition on the Ge substrate is HF pre-treatment at high concentration (20%) [35]. Although HF is the only solution for removing SiO_2, all halogen acid group such as HF, HCl, HBr and HI can remove Ge oxide [31]. Another removal method is to use the sacrificial Si_3N_4 as a blocking layer when an oxygen source is provided from a surrounding environment such as the reaction gas in the furnace or the oxygen gas in the air.

2.3.2 High-k Dielectric in Ge Gate Stack

Various deposition methods and material characteristics of high-k dielectrics have been widely studied on Si and polysilicon channels. The major deposition methods for high-k dielectrics are atomic layer deposition (ALD) [36], chemical vapor deposition (CVD) [37-39], and sputter deposition [37]. There are two main reasons for using high-k materials on Ge or Si. High-k dielectrics have characteristics which allow us to obtain a thin equivalent oxide thickness (EOT) and provide a thermally stable insulation layer instead of Ge oxide on the Ge channel, which gives good electrical properties including high mobility due to a high quality interface of high-k/Ge gate stack. It also has implication for the electrostatic field distribution when the tunnel and control dielectrics have different permittivity.

Since the material characteristics of the high-k/Ge interface depend on the type of high-k materials, selection of gate dielectric is the key issue for higher performance. Therefore, effective processing to improve the high-k/Ge interface properties will also be required in the high-k/Ge process. The Ge diffusion phenomenon also depends on the crystallinity of the high-k material. Typical binary high-k material, such as ZrO_2, is crystallized at the dopant activation temperature in Ge at 400 °C to 500 °C. ZrO_2 cannot then act as a barrier against Ge diffusion into high-k films due to the occurrence of the fast diffusion of atoms at the grain boundaries of crystalline films as shown in Figure 2.7.

On the other hand, Al_2O_3 amorphous high-k films can suppress diffusion of atoms into the high-k film and may show minimal intermixing with Ge oxide to stabilize the interface [40]. From the convergent beam electron diffraction (CBED) pattern result in Figure 2.8, an amorphous Al_2O_3 layer can be clearly observed in the high-k/Ge gate stack. From scanning transmission electron microscopy (STEM) and electron energy loss spectra (EELS) results, we also find that Ge oxide at the high-k dielectric and Ge interface was completely removed after HF pre-treatment as shown in Figure 2.9. Figure 2.9 (a) shows a DF-STEM image of a single layer Au NCs Ge TFT gate stack. The Au NCs are located at the middle of the image and are brightest. Two lines of vertically aligned dots, denoted as lines A and B in Figure 2.9 (a), indicate sub-nanometer-sized focused electron beam spots from which electron energy loss spectra (EELS) were taken. Line A was used to acquire the Al, O, and Cr EELS edge while line B was used to acquire the Ge EELS edge. We used a separate line scan for Ge EELS edge because the energy dispersion for Ge was set at 0.7 eV per channel while for the other edges the energy dispersion was set at 0.3 eV per channel. From the EELS edges of Al, O, Cr, and Ge, which are shown in Figure 2.9 (b-e),

different layers of the gate stack can be clearly identified. These results indicate that ALD Al_2O_3 is one of the most promising high-k dielectrics for Ge TFT.

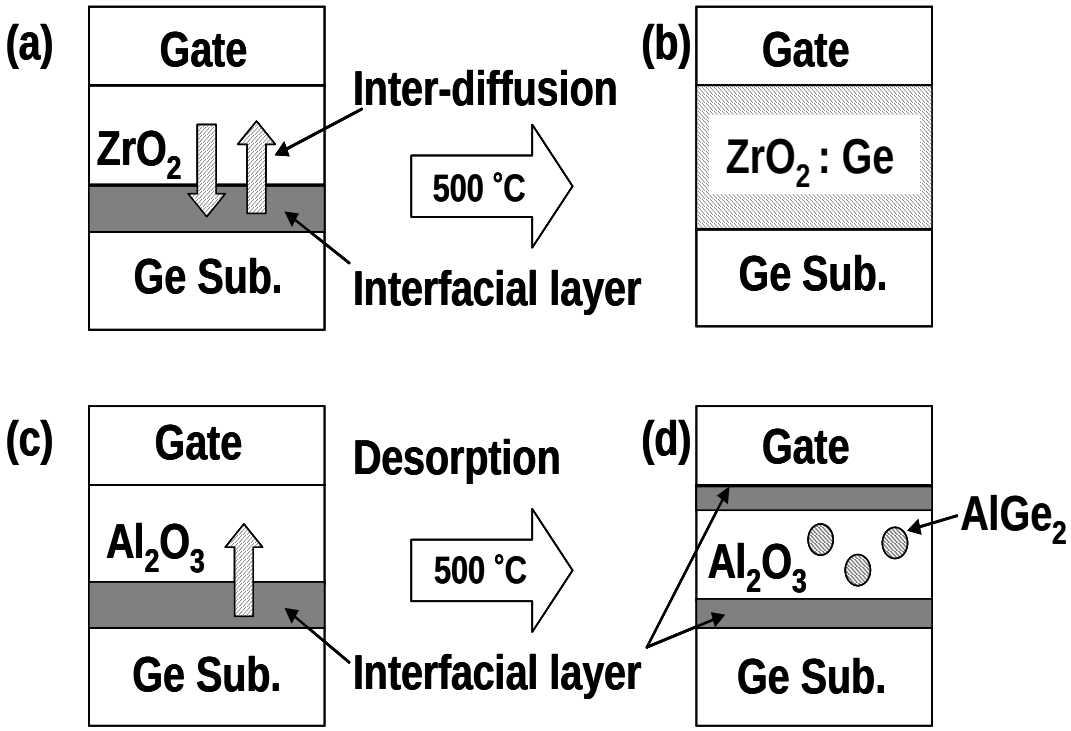


Figure 2.7 Schematic on the effect of annealing on ZrO_2/Ge gate stack (a, b) and Al_2O_3/Ge gate stack (c, d).

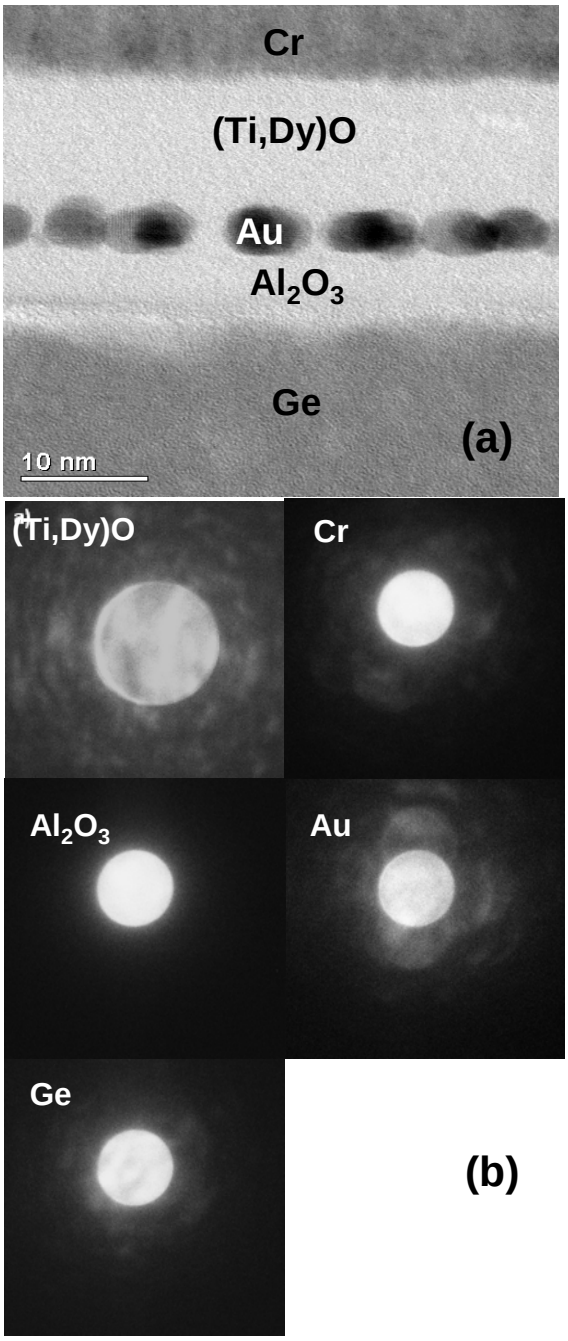


Figure 2.8 (a) BF-STEM image of a single NC layer embedded in the Ge gate stack, (b) CBED pattern of Al_2O_3 layer at Al_2O_3/Ge gate stack.

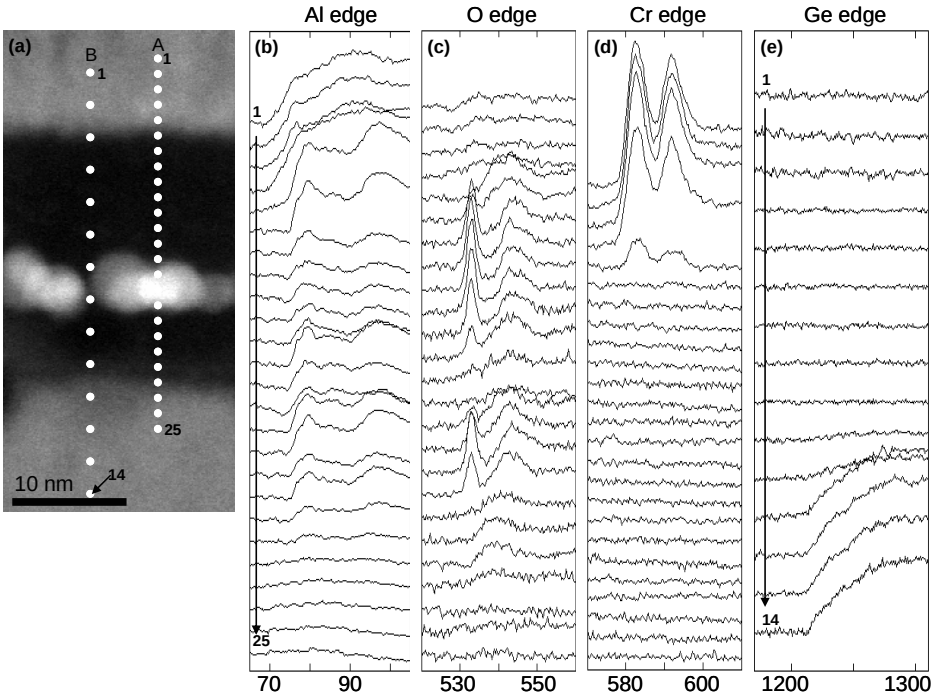


Figure 2.9 (a) DF-STEM image of a single layer Au NCs Ge TFT gate stack, (b) Al EELS edge (taken from line A), (c) O EELS edge (taken from line A), (d) Cr EELS edge (taken from line A), and (d) Ge EELS edge (taken from line B).

2.4 Nanocrystal Floating-Gate Memory with High-k Tunneling Barrier

The nanocrystal-based nonvolatile memory device has received considerable attention due to its faster programming capability, lower power consumption, superior endurance and higher density integration, which mainly results from its scaled down tunneling dielectric thickness [41, 42]. The goal of this device is to achieve a programming speed comparable to DRAM and data retention capability comparable to flash memory for possible replacement of these other devices in the future [42].

It has thus far proven difficult to improve the programming speed (voltage and/or time) and data retention simultaneously because they both rely on the tunneling current (J_g) between nanocrystals and substrate through a very thin tunneling dielectric layer. Efforts have been made with the traditional SiO_2 tunneling oxide [43, 44], but results have suffered from a continued trade-off between programming speed and data retention. It is for this reason that the high-k tunneling dielectric structure has been proposed [45] in order to achieve the enhanced tunneling current during programming without reducing tunneling dielectric thickness to avoid any sacrifice of data retention.

Several efforts have been made to improve the device performance of nanocrystal memory by replacing the traditional SiO_2 with various dielectrics such as oxynitride [46] and amorphous carbon on SiO_2 [47]. Being physically much thicker than SiO_2, the leakage currents of high-k dielectric are several orders of magnitude smaller than that of SiO_2 for the same electrical oxide thickness (EOT) [48], resulting in superior data retention behavior.

On the other hand, high-k dielectric may provide larger tunneling current than SiO_2 when the device operates in the programming regime of the Forler-Nordheim (FN) tunneling due to its lower electron barrier height. These characteristics result in a much higher programming-to-retention current ratio than is obtained with SiO_2, and so

contributes to longer retention. The use of thermo-dynamically stable high-k dielectric as a tunnel dielectric barrier in direct contact with polysilicon or Ge channel is also necessary to integrate simple gate structure. ALD Al_2O_3 and sputtering $(Ti,Dy)_xO_y$ are two of the most promising high-k materials in this regard because they do not need the additional heat process such as high temperature source drain activation annealing. Therefore, these methods are suitable for 3-D integration of flash memory cells. The Au nanocrystal formation process is also more stable than other processes such as Pt, Ag and Si because it shows the good uniformity of nanocrystal size without the additional heat budget. Based on these results, Au nanocrystal floating-gate memory with high-k tunneling and control barriers is one of the most promising candidates for 3-D integration flash memory cells. Chapters 3, 4 and 5 show the experimental results using these methods.

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CHAPTER 3

PLANAR POLYSILICON TFT WITH Au NC AND HIGH-K DIELECTRICS

3.1 Motivation

Driven by increasing demand for higher-density and lower-cost portable data storage, three-dimensional (3-D) integration for nonvolatile memory applications has been under active research [1-6]. The ultra-thin body (UTB) thin film transistor (TFT) with metal nanocrystals (NCs) and high-k gate dielectrics is one of the promising solutions [7-11]. Metal NCs embedded in high-k dielectrics are desirable for low program/erase (P/E) voltage due to smaller Coulomb energy and inherent field enhancement [9, 12]. Moreover, *in-situ* doped polysilicon by chemical vapor deposition (CVD), atomic layer deposition (ALD) Al_2O_3 and high-quality sputtered $(Ti,Dy)_xO_y$ films can satisfy the thermal budget of 3-D integration in a cost-effective manner, because the highest temperature does not exceed 600 ^oC [13]. However, sub-threshold characteristics of the conventional polysilicon TFT heavily depend on the trap density at grain boundaries, which cannot be well-controlled in most cases. Our approach is to make the polysilicon film much thinner than the depletion width [7, 8] so that the reduced total number of traps makes the device characteristics less sensitive to the trap density fluctuation [2]. Additionally, the polysilicon channel mobility should not be severely degraded by the traps or surface roughness. Therefore, a uniform ultra-thin polysilicon body (<20 nm) is preferred. Here, we present the material and electrical characterization of the low-temperature UTB-TFTs integrated with metal NCs and high-k dielectrics. If the control dielectric has a higher k than the tunnel dielectric, better 3-D electrostatics lead to a larger design space in program/erase (P/E) operations and better control of short-channel effects [9]. In this

chapter, we also present fabrication and characterization of a double-layer metal NC memory, which can further improve the performance in terms of storage capacity, volume charge density and retention time [14].

3.2. Polysilicon TFT with Single Au NC and $(Ti,Dy)_xO_y$ High-k Dielectric

3.2.1 Device Fabrication and Material Characterization

The device structure and process sequence are shown in Figure 3.1. A thick 100 nm CVD polysilicon film with 10^{19} cm^{-3} *in situ* phosphorous doping was deposited on 200 nm plasma enhanced CVD (PECVD) oxide, which emulates a stackable process. For better process control and uniform film thickness, different CMP process split setups such as backside pressure, table speed, chuck speed and slurry composition were examined in Figure 3.2. The final process conditions are summarized in Table 3.1.

Surface morphology of the deposited polysilicon film by atomic force microscopy (AFM) is shown in Figure 3.3(a) with RMS roughness of about 3.5 nm. CMP was then applied to achieve the desired film thickness of 13 nm with RMS roughness below 1 nm as shown in Figure 3.3(b). This is an important step since rough surface affects P/E consistency by non-uniform vertical fields [15], increases the interface states that degrade the cycle endurance, and reduces the transconductance due to the additional surface scattering.

After the CMP process, a $(Ti,Dy)_xO_y$ film as a tunnel dielectric of 2.6 nm effective oxide thickness (EOT) and 23 nm physical thickness was deposited by RF reactive sputtering from a metallic 2-inch target of the composition $Ti_{0.8}Dy_{0.2}$. The density of radio frequency power was 4.94 W/cm^2 when the deposition was done.

The sputtering ambient gas composed of 4:1 Ar and O_2, and the total pressure in the chamber by throttling the valve to the turbo-molecular pump was 30 mTorr. Under these conditions, the deposition rate was 10.2 nm/min [16]. The base pressure in the chamber prior to deposition was 2×10^{-6} torr.

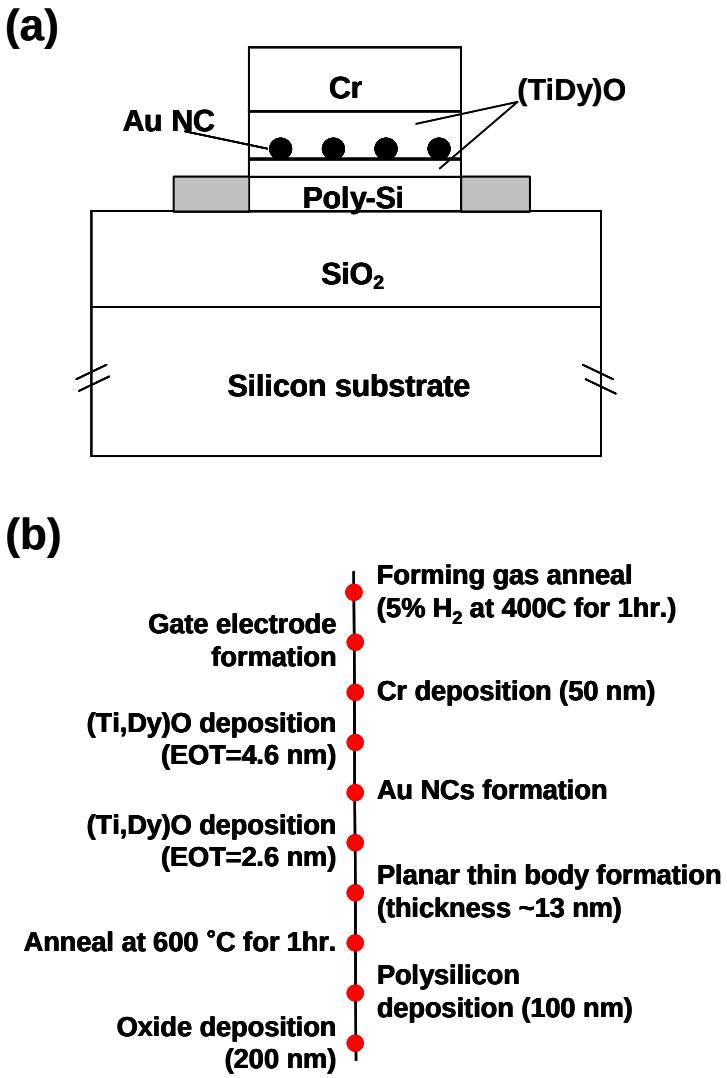

Figure 3.1 (a) Vertical device schematics of a UTB TFT memory with metal NC charge storage and $(Ti,Dy)_xO_y$ tunneling barriers and (b) the main process sequence.

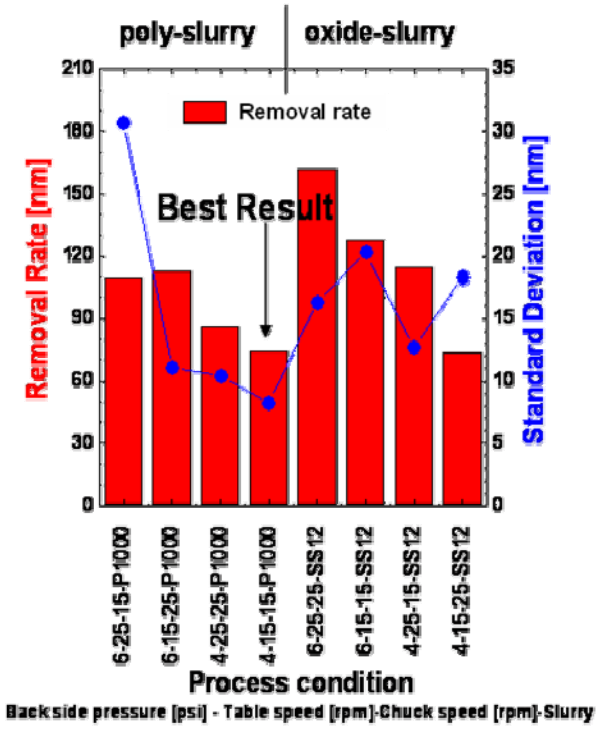

Figure 3.2 The polysilicon removal rate and standard deviation of the film thickness under different CMP conditions.

Table 3.1. The CMP process chosen in this study for the UTB TFT.

Factor	Value
Back side pressure [psi]	4
Table speed [rpm]	15
Chuck speed [rpm]	15
Slurry	Poly slurry (P-1000)

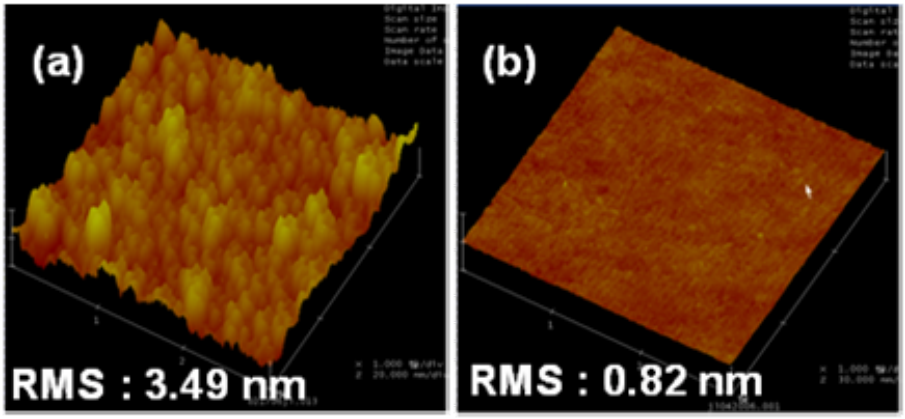

Figure 3.3 3 μm × 3 μm AFM images of polysilicon thin film: (a) before CMP and (b) after CMP.

Au NCs were self-assembled on the tunnel dielectric by e-beam evaporation [17]. The statistical parameters of Au NCs extracted from the top-view scanning electron microscope (SEM) are summarized in Table 3.2. Another $(Ti,Dy)_xO_y$ film with EOT of 4.5 nm and physical thickness of 40 nm was deposited as a control dielectric using the same recipe.

Table 3.2 The statistical parameters of Au NCs.

Item	Value
Diameter	5.8 nm
Standard deviation of diameter	1.2 nm
Surface fill percentage	22.19 %
Number density	7.5×10^{11} cm^{-2}

Finally, a 50 nm Cr film as the gate electrode was deposited by e-beam evaporation. After gate patterning, the device was annealed in the forming gas of (H_2: 5%) at 400 °C for one hour.

A bright field (BF) scanning transmission electron microscopy (STEM) image and convergent beam electron diffraction (CBED) patterns in Figure 3.4 show the discrete nearly-spherical Au NCs embedded in the $(Ti,Dy)_xO_y$ gate stack. Polysilicon grains can be clearly observed.

Bright spots between the Au NCs indicate the top $(Ti,Dy)_xO_y$ layer does not fill the spaces between the Au NCs. From the CBED patterns in Figures 3.4(b) and (c), the $(Ti,Dy)_xO_y$ layer looks amorphous while the distinct disks in the diffraction pattern of the polysilicon layer indicate that crystal grains exist. A dark field (DF)-STEM image and electron energy loss spectroscopy (EELS) data in Figure 3.5 show the compositional information of materials in the $(Ti,Dy)_xO_y$ gate stack.

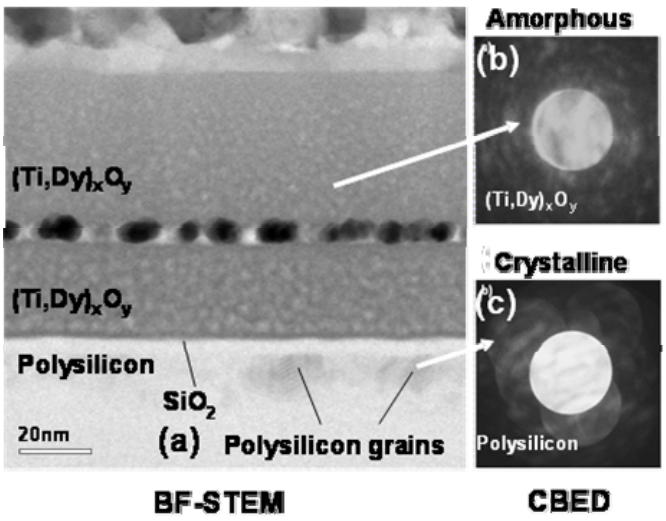

Figure 3.4 (a) BF-STEM image of a single NC layer embedded in the $(Ti,Dy)_xO_y$ gate stack, CBED patterns of (b) $(Ti,Dy)_xO_y$ layer, and (c) polysilicon layer.

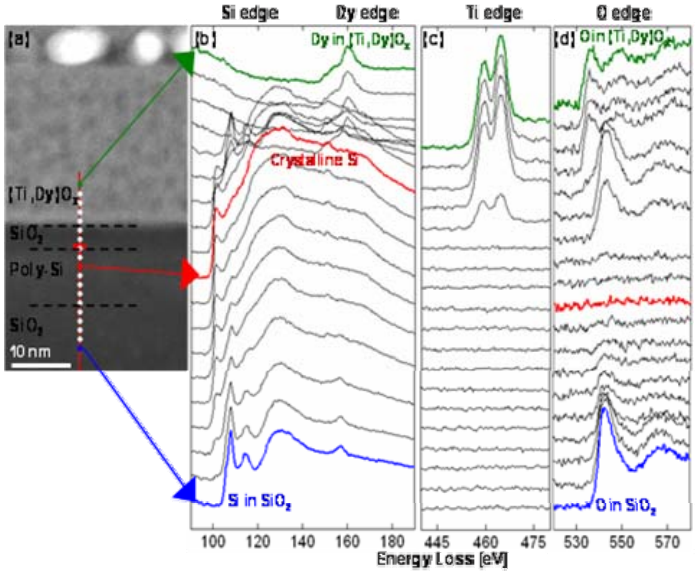

Figure 3.5 (a) DF-STEM image of a Au NC TFT gate stack with a (Ti,Dy)O layer, (b) Si and Dy EELS edge, (c) Ti EELS edge, and (d) O EELS edge.

3.2.2 Electrical Characterization

Figure 3.6 shows the negligible memory windows in the control devices with the same gate stack, but without the Au NCs. The dielectric constant of the $(Ti, Dy)_xO_y$ film is 35, and the off-state leakage current at −1 V bias and 2.8 nm equivalent oxide thickness is 5×10^{-7} A/μm^2.

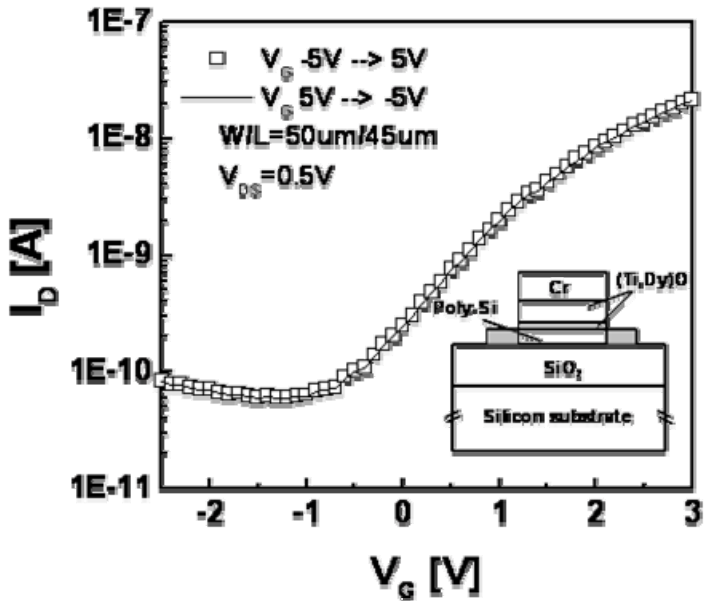

Figure 3.6 Lack of memory window in control polysilicon TFT without Au NC. *W/L* = 50 μm /45 μm.

The kink effect in the output characteristics is not observed in the CMP UTB film as is with the conventional TFT in Figure 3.7 because the thin body electrostatics suppresses the potential pocket for body charge accumulation and parasitic BJT (bipolar junction transistor) [18, 19]. The injection from impact ionization at high

V_{DS} (drain-source voltage) is probably as strong, but the holes will leak out through the source instead of accumulating at the buried oxide interface.

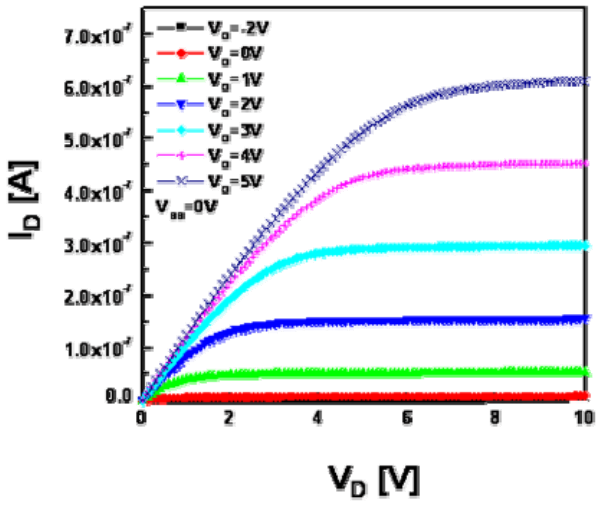

Figure 3.7 Output characteristics of the $(Ti,Dy)_xO_y$/Au/$(Ti,Dy)_xO_y$ TFT device.

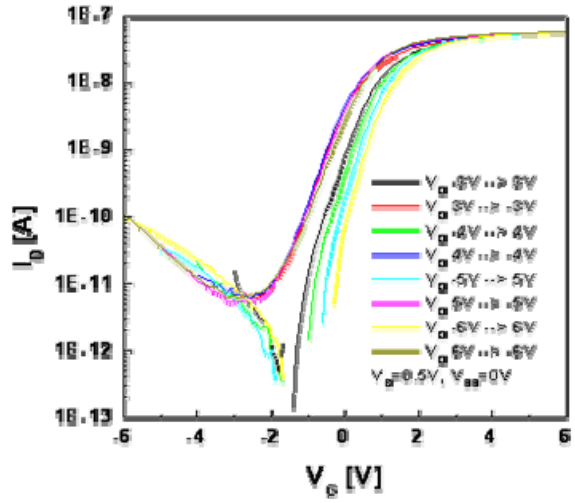

Figure 3.8 Transfer characteristics with gate voltage sweeps for $(Ti,Dy)_xO_y$/Au/$(Ti,Dy)_xO_y$ TFT flash memory cells.

The threshold voltage shift in the embedded-NC device in Figure 3.8 was measured after writing by ±3 V to ±6 V direct pulses of one second duration. Figure 3.8 shows reasonable sub-threshold slopes (*S*) and memory windows for the $(Ti,Dy)_xO_y/Au/(Ti,Dy)_xO_y$ device for various gate voltage sweeps. We have obtained a memory window of about 0.95 V by ±6 V P/E voltages.

3.3 Polysilicon TFT with Single Au NC and Al_2O_3 High-k Dielectric

3.3.1 Device Fabrication and Material Characterization

The process sequences and structure of the single NC UTB TFT memory structure are shown in Figure 3.9.

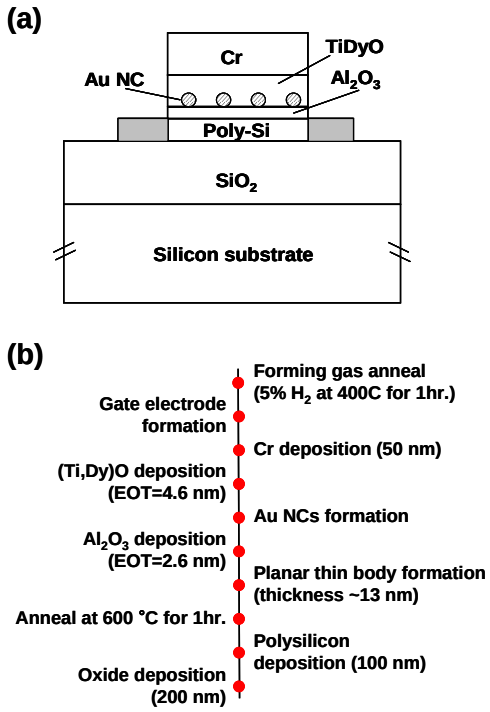

Figure 3.9 (a) Vertical device schematics of a UTB TFT memory with metal NC charge storage and Al_2O_3 tunneling barriers and (b) the main process sequence.

The thickness of the high-k dielectrics are expressed in terms of physical thickness in Figure 3.9. In Figure 3.10, bright-field scanning transmission electron microscope (BF-STEM) cross-sectional images show discrete spherical Au NCs embedded in the single NC gate stack.

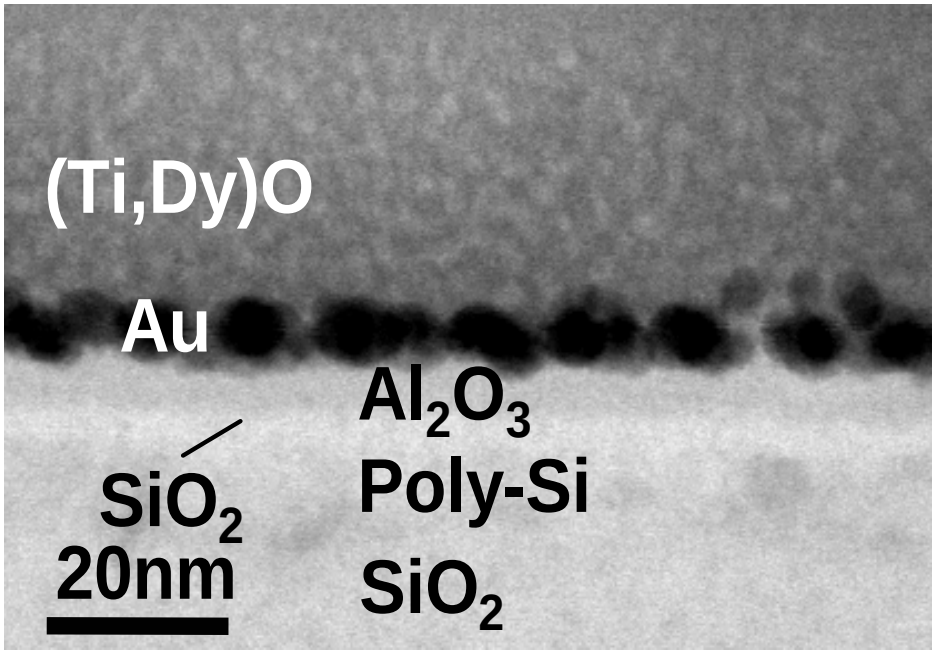

Figure 3.10 BF-STEM image of single Au NCs TFT gate stack embedded in $Al_2O_3/(Ti,Dy)_xO_y$ layers.

Figure 3.11(a) shows a dark-field scanning transmission (DF-STEM) image of a single layer Au NCs polysilicon TFT gate stack. The Au NCs are located at the middle of the image and are brightest. From the EELS edges of Dy, Ti, and O, which are shown in Figure 3.11(b-d), different layers of the gate stack can be clearly identified.

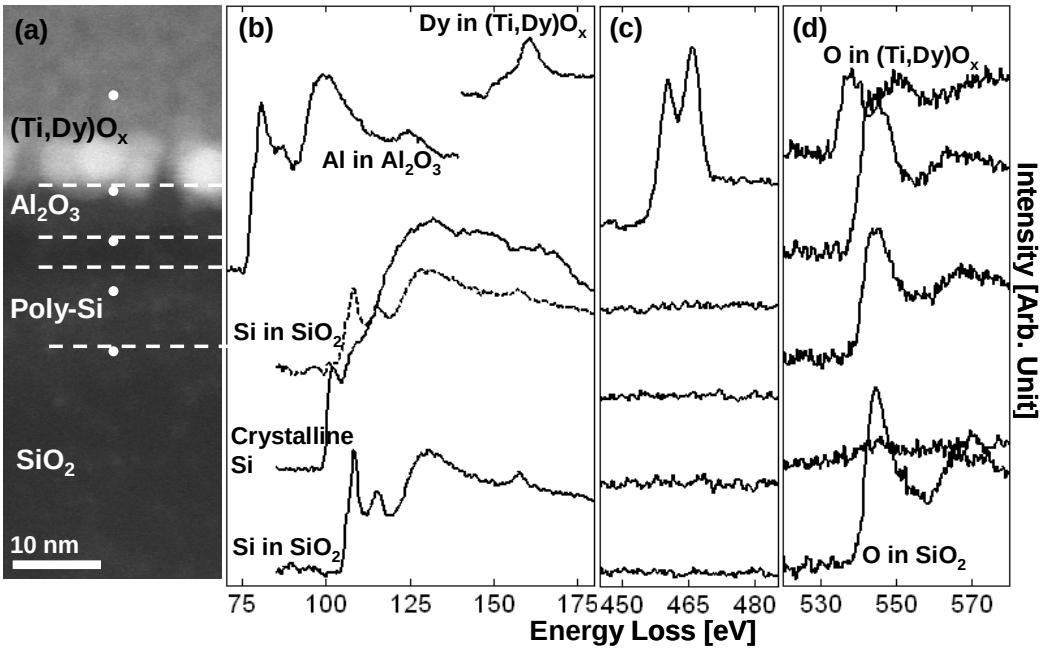

Figure 3.11 (a) DF-STEM image of single Au NCs TFT gate stack embedded in $Al_2O_3/(Ti,Dy)_xO_y$ layers, (b) Dy EELS edge, (c) Ti EELS edge and (d) O EELS edge (taken from line A).

A thick 100 nm polysilicon film with 10^{19} cm^{-3} *in-situ* phosphorous doping was deposited on 200 nm plasma-enhanced chemical vapor deposition (PECVD) oxide. The *in-situ* doping eliminates the need for high-temperature dopant activation and further reduces the potential barrier height in the channel. The phosphorous dopant redistribution and loss by diffusion and segregation is negligible in the process of repeated memory layers. Surface morphology of the deposited film with one-hour 600 °C annealing gives a root mean square (RMS) roughness of about 3.5 nm. CMP was then applied to achieve the desired film thickness of about 13 nm with RMS roughness of around 0.8 nm. The CMP thinning is an important step because the rough surface affects P/E consistency by non-uniform vertical fields [20], and increases the interface

states, which degrade the cycle endurance. The UTB film reduces the total number of traps in the depletion region and the threshold voltage.

After CMP, Al_2O_3 with an equivalent oxide thickness (EOT) of 2.6 nm and physical thickness of 6 nm was grown as a tunneling dielectric by atomic layer deposition (ALD). Au NCs were self-assembled on Al_2O_3 by e-beam evaporation. The wetting-layer thickness and pressure of the self-assembled process are 1.2 nm and below 2×10^{-6} torr, respectively. The SEM image of Au NCs is shown in Figure 3.12 (a). The density, average diameter and standard deviation of Au NCs are about 7.5×10^{11} cm^{-2}, 6.1 nm and 1.2 nm, respectively, as shown in Figure 3.12 (b).

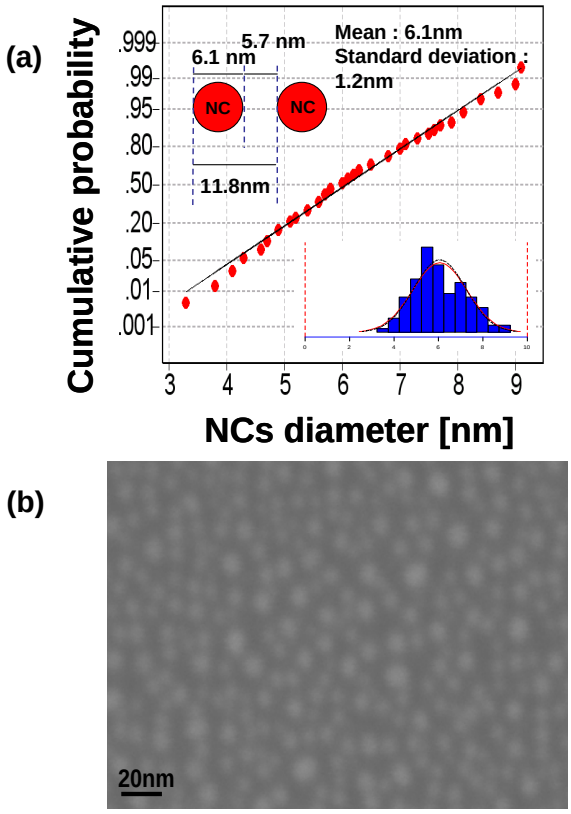

Figure 3.12 (a) Size distribution of Au NCs deposited by e-beam evaporator on ALD Al_2O_3 and (b) an SEM image.

The statistical parameters are extracted by cumulative probability. The $(Ti,Dy)_xO_y$ film as a control dielectric was deposited by sputtering with an EOT of 4.5 nm and physical thickness of 40 nm on the single-layer metal NCs. Finally, a 50 nm Cr gate electrode was deposited by e-beam evaporation. After gate patterning, the device was annealed in the forming gas (H_2: 5%) at 400 °C for one hour.

3.3.2 Electrical Characterization

Figure 3.13 shows the absence of memory windows in the control devices with the same gate stack, but without Au NCs. The off-state leakage currents of UTB TFT are at 2.7×10^{-14} A/μm^2 for V_{DS}=0.5 V and V_{GS}=1 V. The off-state leakage of Al_2O_3 as the tunnel dielectric is better than that of $(Ti,Dy)_xO_y$ due to the higher quality of the high-k dielectric.

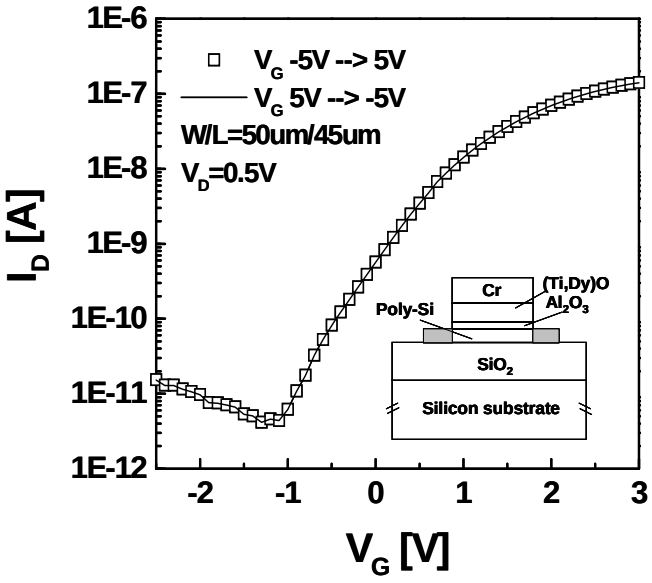

Figure 3.13 Lack of memory window in control polysilicon TFT without Au NC (*W/L* = 50 μm/45 μm).

The output characteristics of the Al_2O_3/Au/$(Ti,Dy)_xO_y$ TFT devices are shown in Figure 3.14. The kink effect in the output characteristics is not observed in the CMP UTB film as is with the conventional TFT in Figure 3.14 because kink effect was eliminated due to extremely flat ultra-thin film in comparison with the conventional TFT and the thin body electrostatics suppresses the potential pocket for body charge accumulation and parasitic bipolar junction transistor (BJT) [21].

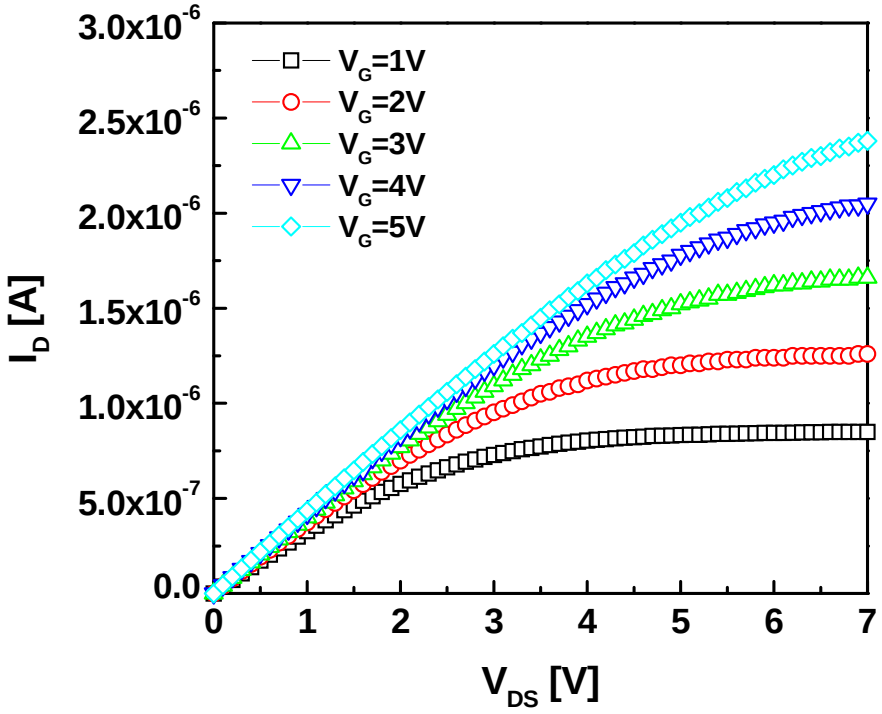

Figure 3.14 Output characteristics of Al_2O_3/ Au/$(Ti,Dy)_xO_y$ TFT device.

Figure 3.15 shows reasonable subthreshold slopes (*S*) and memory windows for the single NC devices for various gate voltage sweeps. We have obtained a memory window of about 0.95 V by ±6 V P/E voltages for UTB TFT with the gate stack of $(Ti,Dy)_xO_y$/Au/$(Ti,Dy)_xO_y$ and single layer NC.

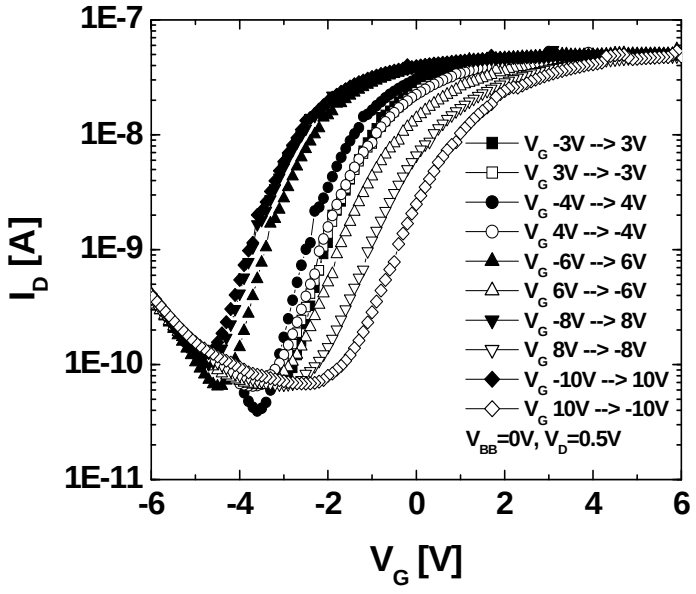

Figure 3.15 Transfer characteristics with gate voltage sweeps for Al_2O_3/Au/$(Ti,Dy)_xO_y$ TFT flash memory cells.

The memory windows in the devices with the gate stacks of Al_2O_3/Au/$(Ti,Dy)_xO_y$ and single-layer NCs are 2.3 V. The difference in dielectric constants in the control and control dielectrics also enables more efficient program/erase operations because the electric field and the percentage of voltage drop are larger in the Al_2O_3 tunneling oxide.

3.4 Polysilicon TFT using Double Au NC and Al_2O_3 High-k Dielectric

3.4.1 Device Fabrication and Material Characterization

For process integration, *in-situ* doped UTB polysilicon by chemical vapor deposition (CVD), Al_2O_3 by high quality atomic layer deposition (ALD) and radio

frequency (RF) sputtered $(Ti,Dy)_xO_y$ films can fulfill the requirements of 3-D integration in a cost-effective manner, since no high temperature steps are required. For a nonvolatile memory, the parametric yield of threshold voltage separation between two memory states is the most important factor among other parameters such as contact resistance and current drive. Therefore, the TFT is an appropriate platform. Furthermore, the polysilicon channel conductance should not be dominated by traps in the grain boundaries so that the charge storage in the metal NCs can effectively modulate the threshold voltage. A uniform UTB polysilicon layer (< 20 nm) is therefore desirable. Reduced surface roughness by full-wafer chemical mechanical polishing (CMP) also leads to improved device characteristics and reliably stackable process integration. The device structure and process sequence are shown in Figure 3.16.

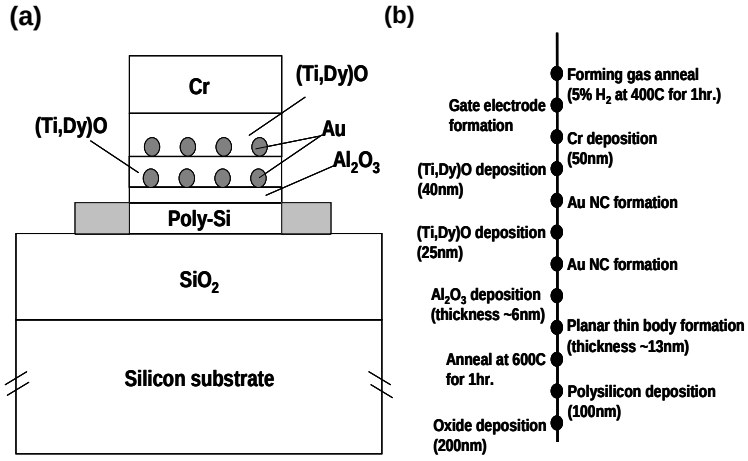

Figure 3.16 (a) Structure and (b) process sequence of a double-layer nanocrystal TFT memory.

In Figure 3.17(a), a bright-field scanning transmission electron microscope (BF-STEM) cross-sectional image shows discrete spherical Au NCs embedded in the

$Al_2O_3/(Ti,Dy)_xO_y$ gate stack. The $(Ti,Dy)_xO_y$, Al_2O_3, polysilicon, and the SiO_2 layers are distinguished by electron energy loss spectroscopy (EELS), which provides elemental identification at sub-nm resolution [see Figure 3.17(b)].

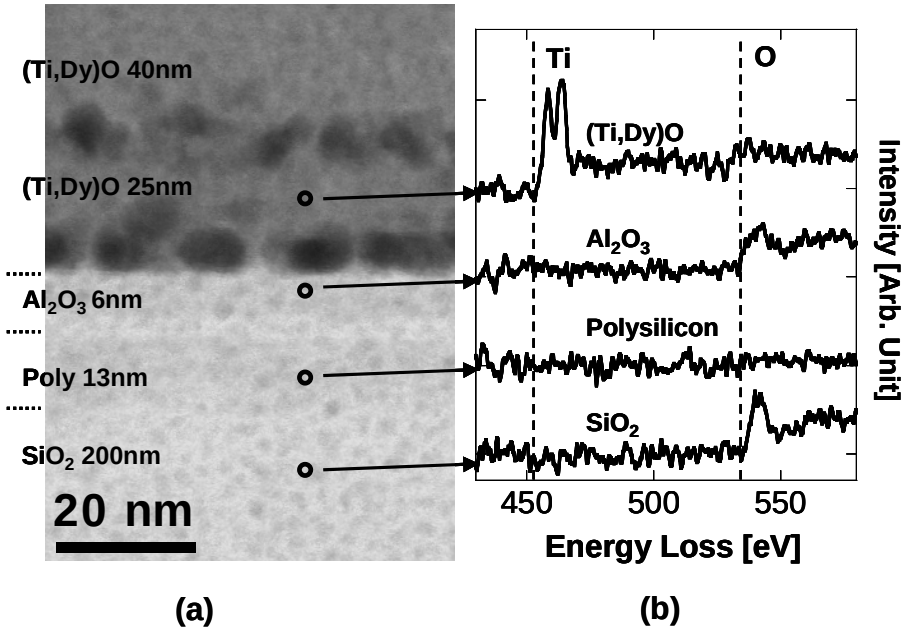

Figure 3.17 (a) STEM image of the double-layer Au NCs TFT gate stack. (b) Ti EELS edge appears at 455 eV while O edge appears at ~525 eV. Si edge was also observed, but not shown here.

A thick 100 nm polysilicon film with 10^{19} cm^{-3} *in-situ* p-type doping was deposited on 200 nm PECVD oxide. Surface morphology of the deposited film with one-hour 600 °C annealing gives a root mean square (RMS) roughness of about 4.1 nm. CMP was then applied to achieve the desired film thickness of about 13 nm with around 0.8 nm RMS roughness. After CMP, Al_2O_3 with an equivalent oxide thickness (EOT) of 2.6 nm and physical thickness of 6 nm was grown as a tunnel dielectric by

ALD. Au NCs were self-assembled on Al_2O_3 by e-beam evaporation.

The (Ti,Dy)O film as an interlayer dielectric was deposited by RF (radio frequency) sputtering with an EOT of 2.8 nm and physical thickness of 25 nm. Then, the same Au NCs formation recipe was adapted for the second NCs layer. The $(Ti,Dy)_xO_y$ film as a control dielectric was deposited with an EOT of 4.5 nm and physical thickness of 40 nm. Finally, a 50 nm Cr gate electrode was deposited by e-beam evaporation. After gate patterning, the device was annealed in the forming gas (H_2: 5%) at 400 °C for one hour.

3.4.2 Electrical characterization

Transfer and transconductance curves of the flash memory cell before NC charging are shown in Figure 3.18(a). The effective mobility is extracted as 45 cm^2/V-s. Figure 3.18(b) shows the lack of memory windows in the control device with the same gate stack, but without Au NCs. The output characteristics of the Al_2O_3/Au/(Ti,Dy)O/Au/(Ti,Dy)O device are shown in Figure 3.19. Kink effects were not observed in the CMP UTB film in comparison with the conventional TFT. A possible reason of the kink effect is a bipolar effect similar to that in floating-body crystalline SOI MOSFET's. When the hole trapping rates are low enough, the holes generated by impact ionization, reach the source contact and reduce the potential barrier between source and body. This decreases the threshold voltage and increases the channel current. Because the source-body junction becomes forward-biased, additional electrons are injected from the source to the body. If the channel is short enough, a significant fraction of these electrons do not recombine with the holes in the channel and are collected by the drain. This effect can be represented by a parasitic npn bipolar transistor in parallel with the FET transistor [22]. Figure 3.20 shows reasonable sub-

threshold slopes (*S*) and memory windows in this device for various gate voltage sweeps. We have obtained a memory window of about 3.5 V by ±10 V P/E voltages.

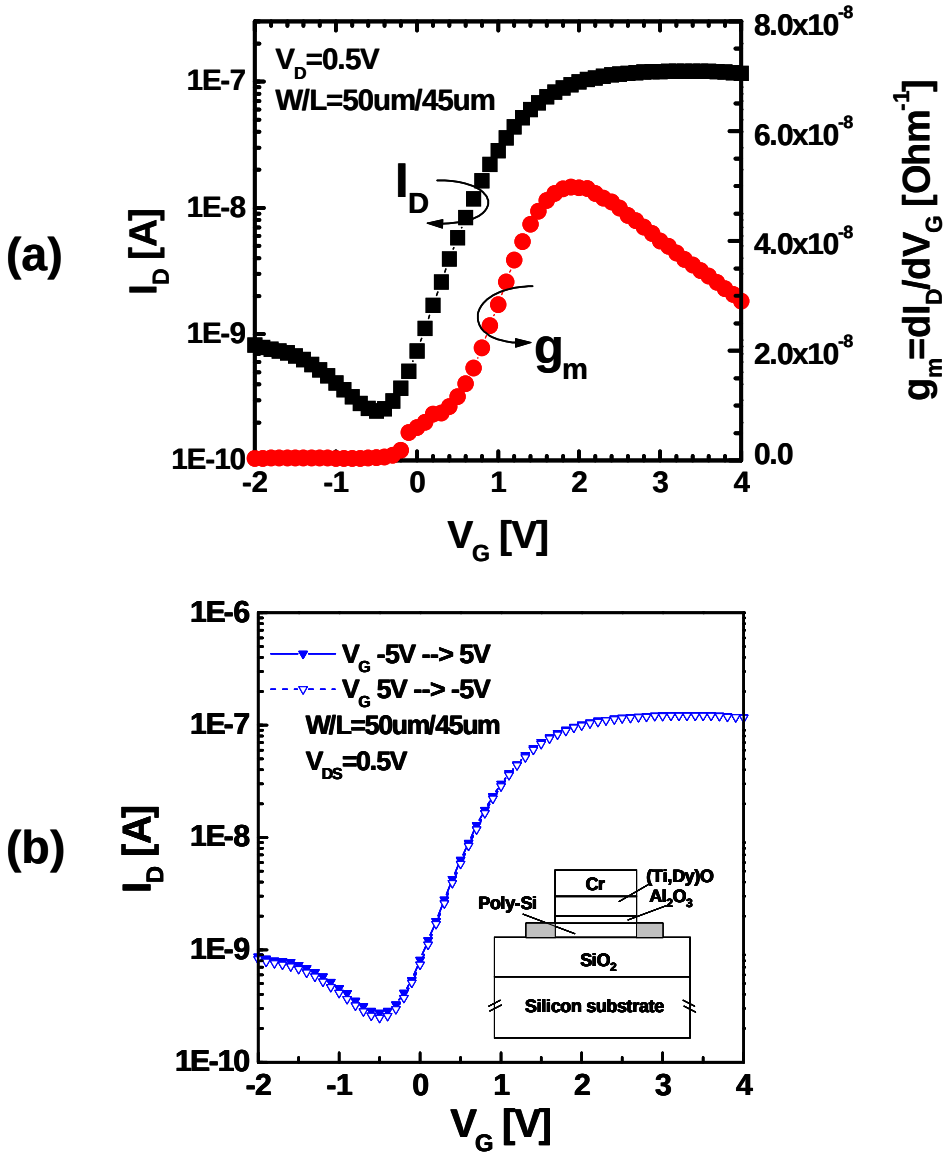

Figure 3.18 (a) Transfer and conductance characteristic of polysilicon TFT, (b) transfer characteristics of lack of memory window in control TFT without Au NC. (*W/L* = 50μm/45μm).

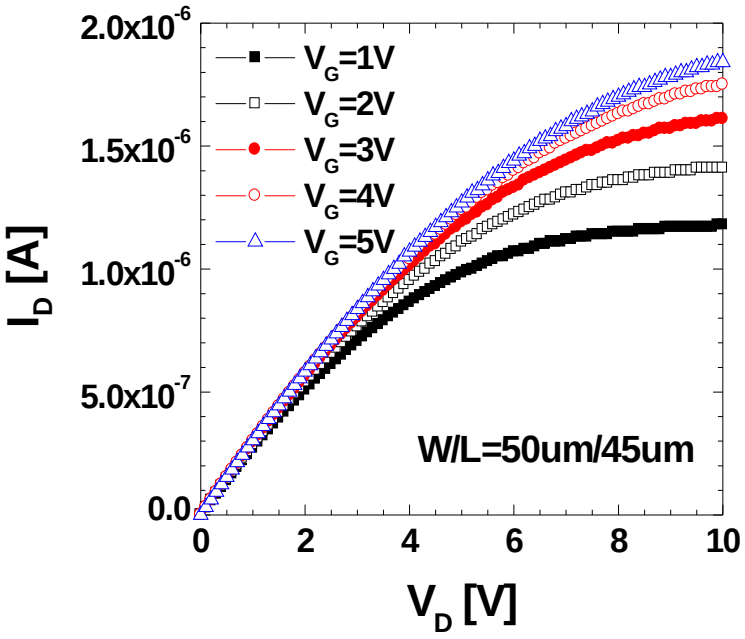

Figure 3.19 Output characteristics of polysilicon TFT with double layer NCs.

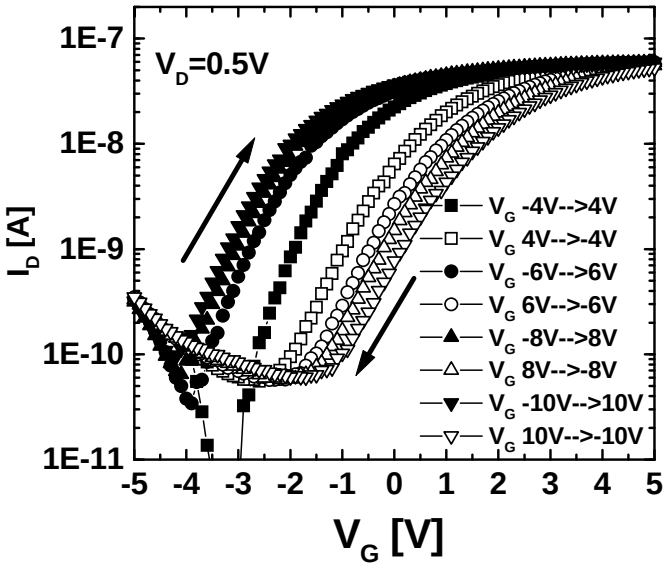

Figure 3.20 Transfer characteristics with gate voltage sweeps for Au double NCs layer TFT flash memory cells.

Retention characteristics were monitored in the single- and double-NC devices after writing by ±6 V direct pulses of 1 sec duration in Figure 3.21. The retention time of double-NC memory by ±6 V P/E is extracted to be well beyond 10 years.

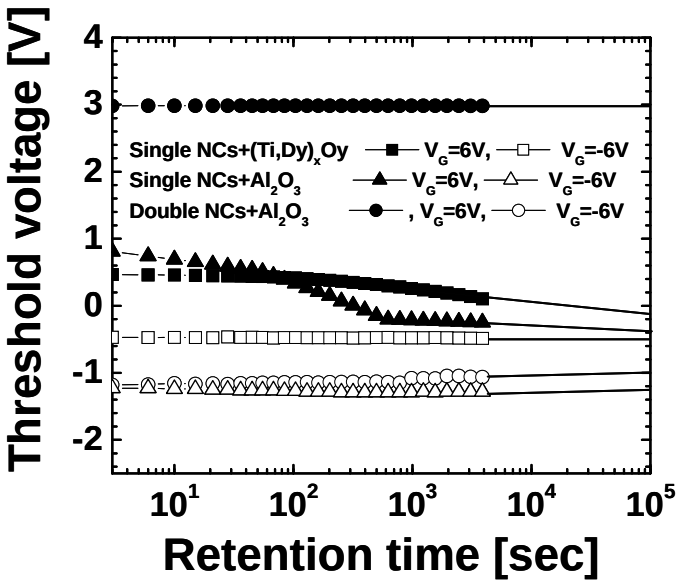

Figure 3.21 Retention time for TFT flash memory cells with single- and double-NCs gate stack.

The retention time and memory window in the single and double metal NCs memory cell with the CMP UTB film and the Au NCs are much larger than other published results [23-26], which is attributed to the enhanced 3-D electrostatics in the high-k/metal-NC gate stack [27] and the UTB TFT.

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CHAPTER 4

FULL SILICIDATION PROCESS

4.1 Motivation

High-density nonvolatile memory applications can benefit tremendously from three-dimensional (3-D) integration with low power consumption [1-4]. Among several proposals [5-10], the silicided source and drain planar polysilicon thin-film transistor (TFT) with metal nanocrystals (NCs) and high-k gate-stack is one of the promising candidates. From the results in Chap. 3, one of the device parameters to be improved is the source resistance, which is limited by the sheet resistance of the ultra-thin polysilicon film. The self-aligned silicidation (SAS) process is often used to reduce the source, drain and gate resistances of submicron logic MOSFET [5, 11]. Especially, NiSi has been proposed as a suitable silicide for SAS process due to its low resistivity, low formation temperature [12-14], and extended thermal stability range [5], as discussed in Chap. 2. Furthermore, since Ni consumes the least amount of polysilicon to form a given thickness of silicide (NiSi), it has the good compatibility with the ultra-thin polysilicon layers on the insulator substrates. Metal NCs are also introduced to allow a thin tunnel dielectric, lower the program/erase (P/E) voltage and enhance the cycle endurance [15]. Moreover, reduced contact and sheet resistance by Ni-based SAS process leads to improved device characteristics and reliable process integration.

4.2 Device Fabrication and Material Characterization

The device structure and the process sequence of Ni-based SAS polysilicon

TFT under study are shown in Figure 4.1 (a) and (b), respectively.

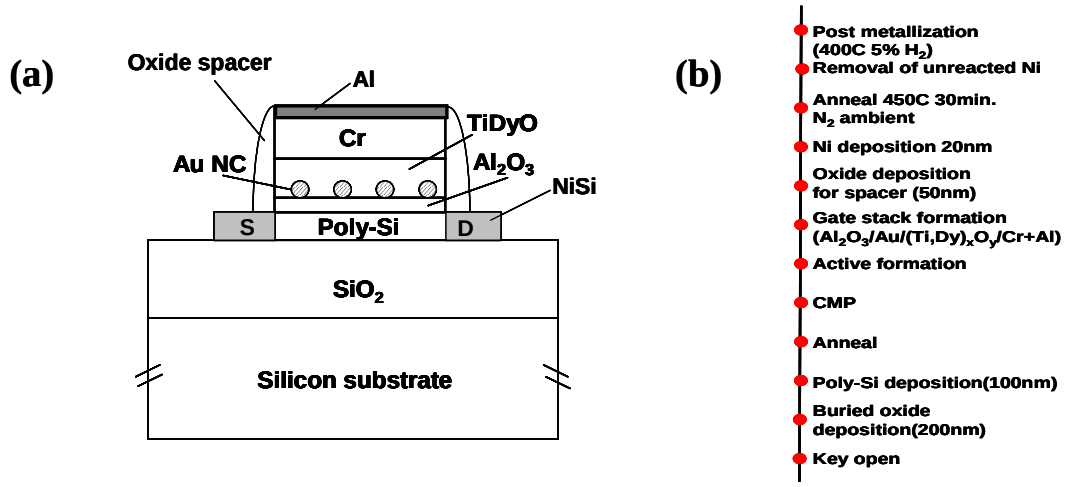

Figure 4.1 (a)Vertical structure of Au NCs embedded in Al_2O_3/(Ti,Dy)O gate stacks on SAS polysilicon TFT and (b) process sequences using SAS process.

A 100 nm thick polysilicon film with 10^{19} cm^{-3} *in situ* phosphorous doping was deposited on 200 nm PECVD oxide. Chemical mechanical polishing (CMP) was then performed to achieve the desired film thickness of about 13 nm with root mean square roughness below 1 nm [15]. This is an important step because rough surface affects the P/E consistency due to nonuniform vertical fields [16-18] and increases the interface states that degrade the cycle endurance, and also reduces the transconductance. After CMP, an Al_2O_3 film with equivalent oxide thickness (EOT) of 2.6 nm and physical thickness of 6 nm was grown as a tunnel dielectric by atomic layer deposition (ALD). Au NCs are self-assembled on the tunnel dielectric by e-beam evaporation [19]. The STEM tomographic image of Au NCs is shown in Figure 4.2. The $(Ti,Dy)_xO_y$ film as a control dielectric was deposited by sputtering with an EOT of 4.5 nm and physical

thickness of 40 nm.

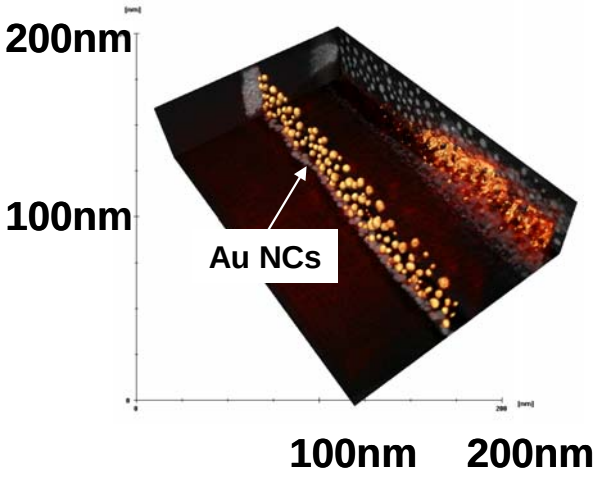

Figure 4.2 3-D tomographic image of self-assembled Au NCs.

The 50 nm Cr and 20 nm Al gate electrode was deposited by e-beam evaporation. After oxide spacer formation and Ni deposition, NiSi was formed by thermal annealing at 450 °C for 30 mins in nitrogen ambient. The unreacted Ni on the oxide was removed by a selective etching solution (H_2SO_4:H_2O_2 =4:1) at 60 °C for 10 minutes, without damaging the NiSi or oxide. Finally, forming gas anneal was carried out at 400 °C for one hour.

4.3 Electrical Characterization

The test pattern and the cross section of the device structure for the sheet resistance measurements are shown in Figures 4.3(a) and (b). Figure 4.3 (c) shows the sheet resistance of a NiSi film after 30 mins annealing in nitrogen ambient at temperatures ranging from 400 °C to 800 °C. The NiSi has a stable low resistance

when the annealing temperature is lower than 700 ^{o}C.

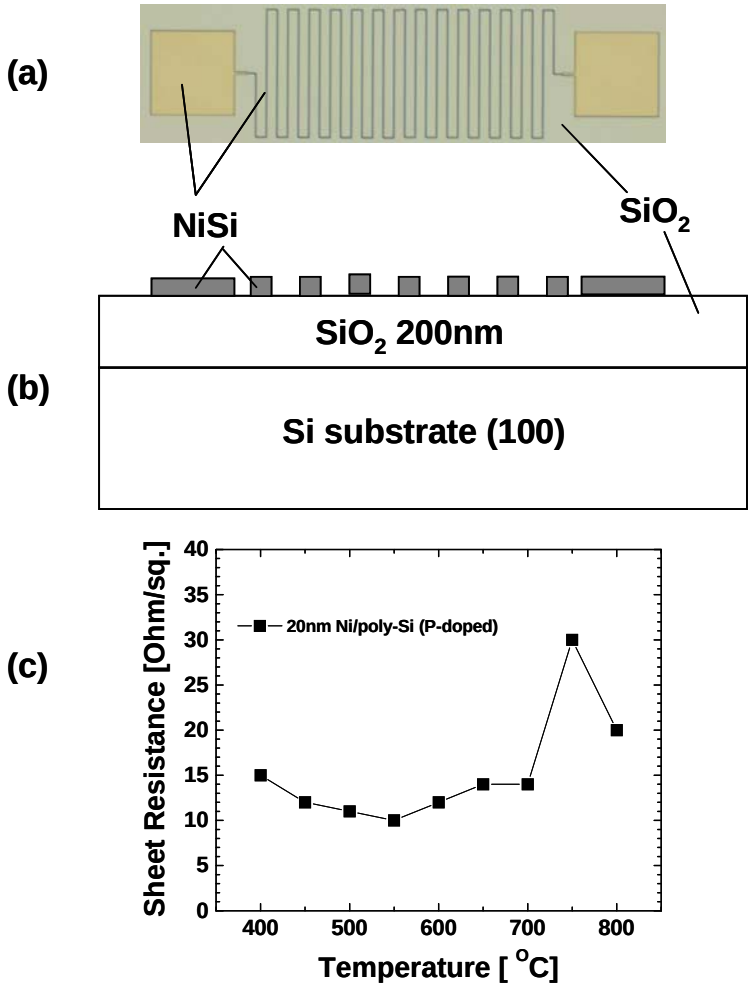

Figure 4.3 (a) Test pattern for sheet resistance measurement of NiSi film after annealing, (b) the cross section of the test structure and (c) sheet resistance of the NiSi film of 13 nm thickness after various annealing temperatures.

Figure 4 shows the lack of memory windows in the control devices with the identical gate stack but without the Au NCs. This validates that the injected charge is stored in nanocrystals instead of dielectric traps. The device split without SAS is also

shown where the source/drain resistance improvement by SAS can be clearly observed.

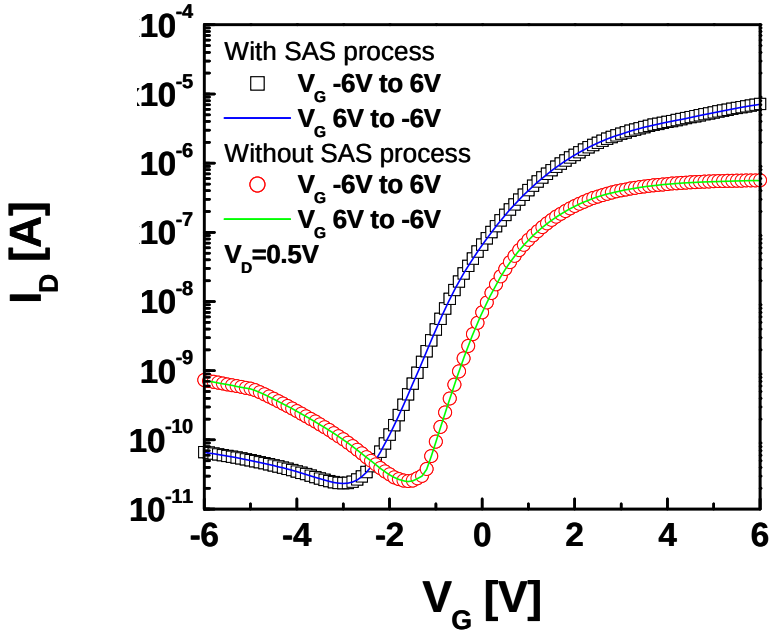

Figure 4.4 Lack of memory window in control FUSI polysilicon TFT without Au NC. *W/L*=50μm /45μm using SAS process.

The output characteristics of the Al_2O_3/Au/(Ti,Dy)O devices are shown in Figure 4.5, with and without the SAS process. The SAS device operated normally with reasonably low source/drain resistance. In addition, the kink effect was eliminated due to the fact the UTB film is extremely flat and ultra-thin in comparison with the conventional TFT film. Figure 4.6 shows reasonable subthreshold slopes (*S*) and memory windows for various gate voltage sweeps. We have obtained a memory window of about 3.1 V by ±5 V P/E voltages. Retention characteristics were monitored in the Al_2O_3/Au/$(Ti,Dy)_xO_y$ devices after writing by ±5 V direct pulse of 1 sec duration in Figure 4.7.

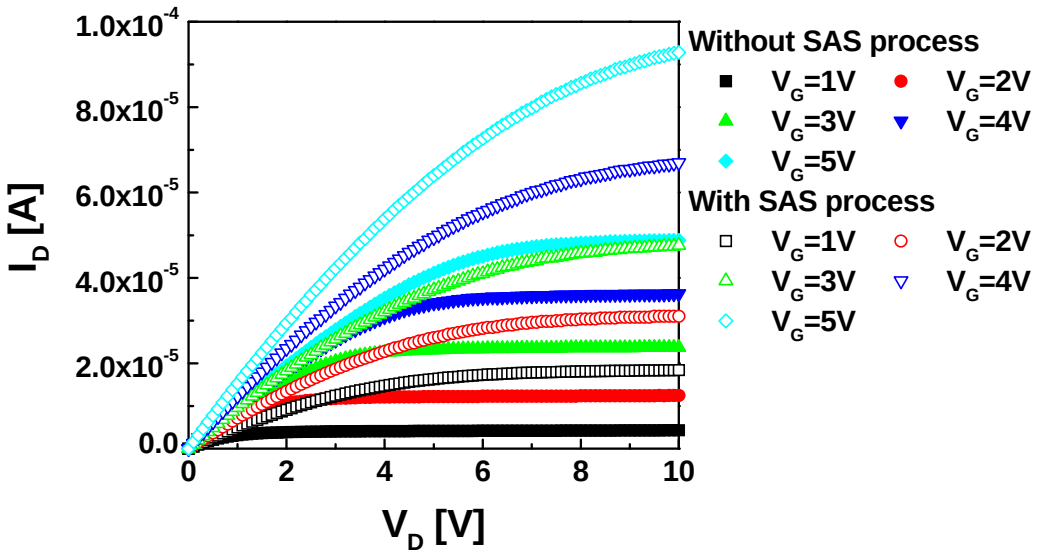

Figure 4.5 Output characteristics of polysilicon TFT with and without SAS process.

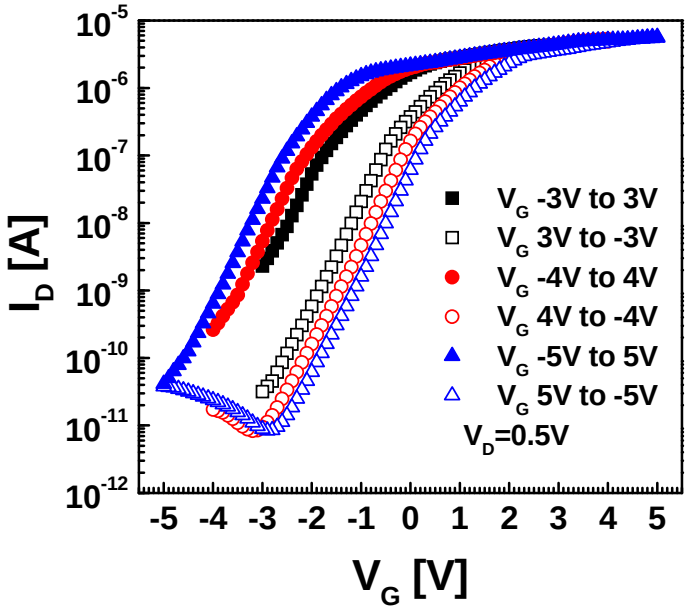

Figure 4.6 Transfer characteristics with gate voltage sweeps for Au NCs TFT flash memory cells using SAS process with various voltage sweep ranges.

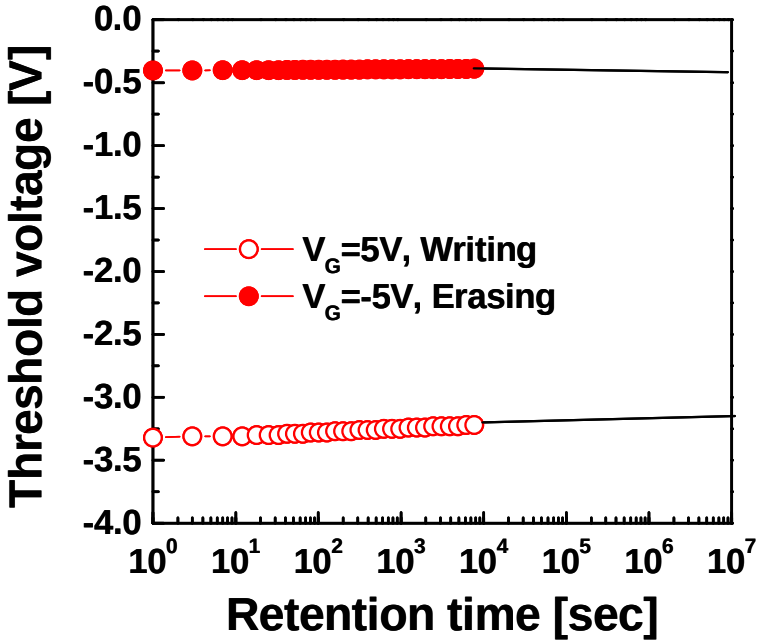

Figure 4.7 Retention time for Au NCs TFT flash memory cells using SAS process under 5V writing and -5V erasing conditions.

The retention time of Ni silicided NC memory by ±5 V P/E is extracted to be well beyond 10 years. In conclusion, we have demonstrated a low-temperature Ni-based SAS process on stackable polysilicon TFT devices for 3-D nonvolatile memory integration.

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CHAPTER 5

PLANAR Ge TFT FLASH MEMORY CELL

5.1 Motivation

As the scaling of classical bulk Si CMOS transistors approaches its fundamental limits, innovative device structures and new materials [1] should be considered. Ge is one of promising candidates for future advanced MOSFET devices due to several of its attractive properties including higher carrier mobility [2-5] for larger drive current, smaller band-gap for supply voltage scaling, and smaller optical band-gap to broaden the absorption wavelength spectrum. Its low processing temperature also makes it compatible with the advanced high-k dielectric [6-8] and metal gates stack technology, as discussed in Chap. 2. These attributes propel recent research efforts into Ge MOSFETs, in particular for Ge-on-insulator (GOI). Hence, following our previous TFT designs in Chaps. 3 and 4, a study of Ge devices for future highly scaled advanced 3-D memory stack with UTB structure is pertinent for understanding its prospect as a viable long-term solution [9-11]. In comparison with Si, Ge has smaller carrier transport mass and gap energy, giving rise to higher drive current (I_{ON}) but also higher tunneling leakage (I_{OFF}). Unlike silicon, however, the lack of a sufficiently stable native oxide hinders the passivation of Ge surfaces. The native germanium oxide is hygroscopic and water-soluble which hinders processing and application of Ge CMOS devices. Several gate dielectric materials with thick EOT on Ge have been reported [12, 13] to overcome this. Al_2O_3 has emerged as one of the most promising high-k gate dielectrics for Si MOSFET and polysilicon TFT [14] to cope with the issue of the native Ge oxide[15, 16]. In this chapter, we demonstrate the

material and electrical characteristics of Ge TFT flash memory cell with Al_2O_3 high-k dielectric and metal NCs.

Vertical integration of devices using Ge thin film transistors (TFT's) is also a promising method to achieve 3-D integration and increase the device density. Various simple vertically integrated cells have been demonstrated on vertically integrated flash memory cells [17-20]. The technique can be applied to aggressively scaled devices, making it very promising for next generation VLSI applications. The actual process is a remarkably simple batch process, and can therefore be used with relatively little cost increase. In chapter 5, we also describe the fabrication process and device performance to achieve vertical integration of Ge devices for the next generation of flash memory cell applications.

5.2 Device Fabrication and Material Characterization

The schematic and process flow of planar Ge TFT flash memory cell structure with Au nanocrystal floating gate is shown in Figure 5.1. A thick 100 nm undoped Ge film using e-beam evaporator is deposited on 200 nm plasma-enhanced chemical vapor deposition (PECVD) oxide. Surface morphology of deposited Ge film by AFM is shown in Figure 5.2(e), which gives a root mean square (RMS) roughness of about 0.224 nm. We then used CMP to achieve the desired film thickness of 30 nm with RMS roughness 0.122 nm as shown in Figure 5.2(b). This is an important step because the rough surface gives a non-uniform electric field that affects P/E consistency, increases the interface states and the surface scattering that affects the cycle endurance, and degrades the transconductance. For better process control and uniform film thickness, different CMP process splits such as backside pressure, table speed and chuck speed were examined.

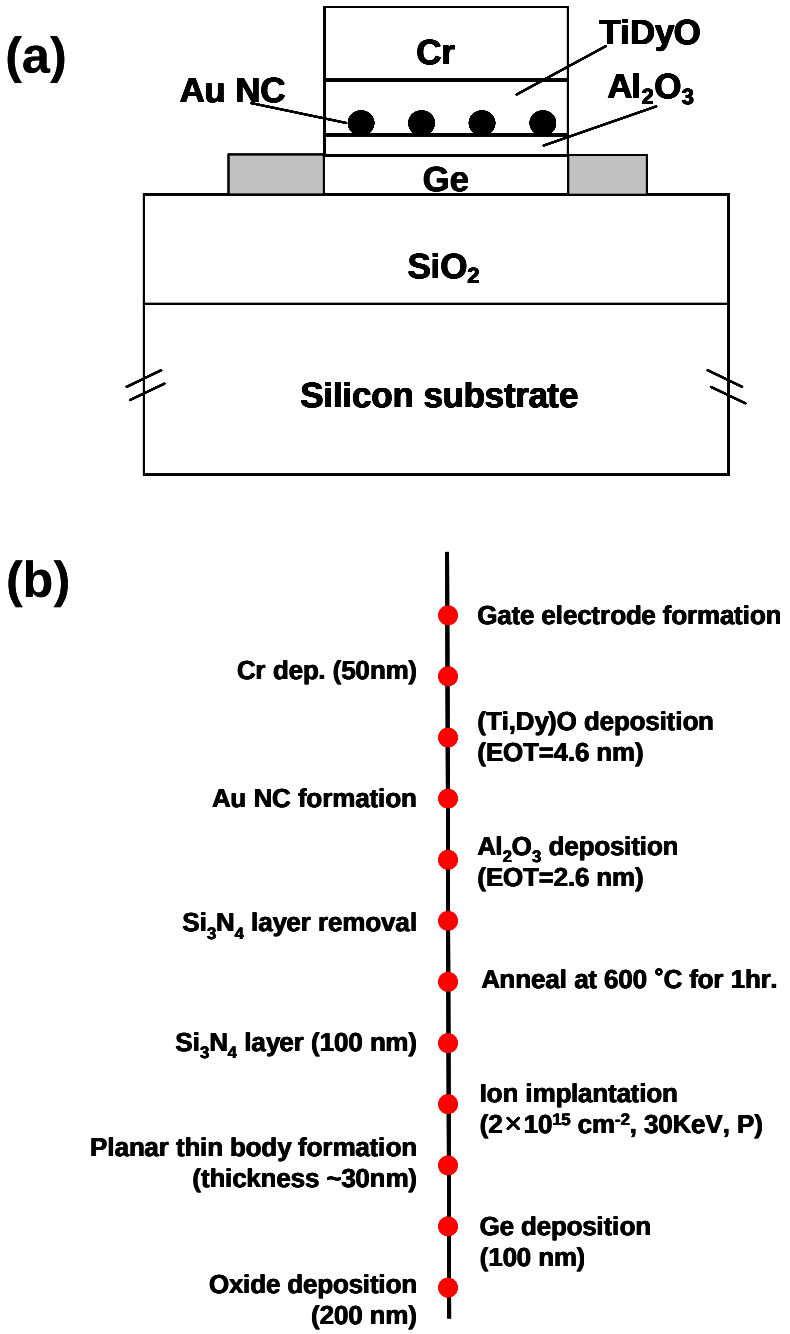

Figure 5.1 (a)Vertical structure of Au NCs embedded in Al_2O_3/(Ti,Dy)O gate stacks on Ge TFT and (b) process sequences Ge TFT process.

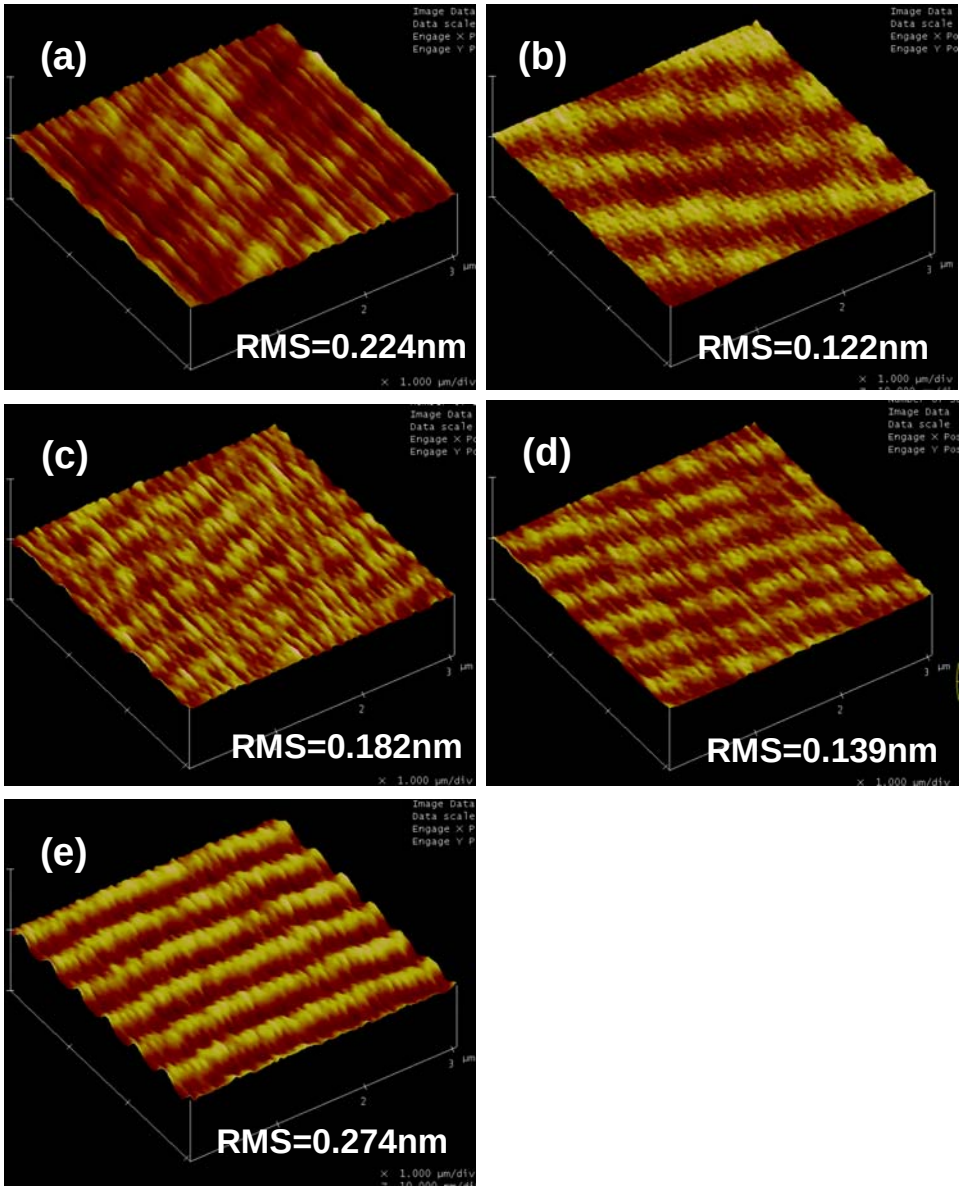

Figure 5.2 3 μm × 3 μm AFM images of Ge thin film: (a) as-deposited without CMP, (b) with CMP, 4psi-15RPM-15RPM (back pressure-table rotation speed-chuck rotation speed), (c) 4psi-25RPM-15RPM, (d) 4psi-15RPM-25RPM and (e) 4psi-25RPM-25RPM.

After the CMP process, phosphorous implantation is performed on planar undoped UTB Ge film with an initial doping concentration of $2\times10^{15}cm^{-2}$. 100 nm sacrificial Si_3N_4 is then deposited by PECVD to avoid the formation of a GeO_2 layer in the thin Ge film surface. The annealing process is accomplished in N_2 ambient at 600 °C for 60 minutes. This activates the implanted phosphorous dose and crystallizes the Ge film. After removing the sacrificial Si_3N_4 layer, Al_2O_3 film with equivalent oxide thickness (EOT) of 2.6 nm and physical thickness of 6 nm was grown as a tunnel dielectric by atomic layer deposition (ALD). Au NCs was self-assembled on Al_2O_3 by e-beam evaporation [21]. The $(Ti,Dy)_xO_y$ film as control dielectric was deposited by sputtering with EOT of 6.2 nm and physical thickness of 40 nm. Lastly, the 50 nm Cr gate electrode was deposited by e-beam evaporation. The gate is then patterned by a photo-lithographical step and lift-off resist (LOR) process.

5.3 Electrical Characterization

Figure 5.3 shows the absence of memory windows in the control devices with the Ge TFT gate stack, but without Au NCs. From the nearly ideal transfer characteristics measurement results of non-hysteresis behavior, the quality concern of the gate oxide of Al_2O_3 tunneling and $(Ti,Dy)_xO_y$ control dielectrics can be relieved. In addition, it can be proved that the memory operation of the NCs memories comes purely from the charge storage in the nanocrystals. The output characteristics of the Al_2O_3/Au/$(Ti,Dy)_xO_y$ Ge TFT device are shown in Figure 5.4. The kink effect [22] is not observed in the planar Ge UTB film similar to the planar polysilicon TFT because the thin body suppresses the body charge accumulation and parasitic bipolar junction transistor (BJT). Slightly poor current drivability was observed due to the polycystalline Ge TFT channel.

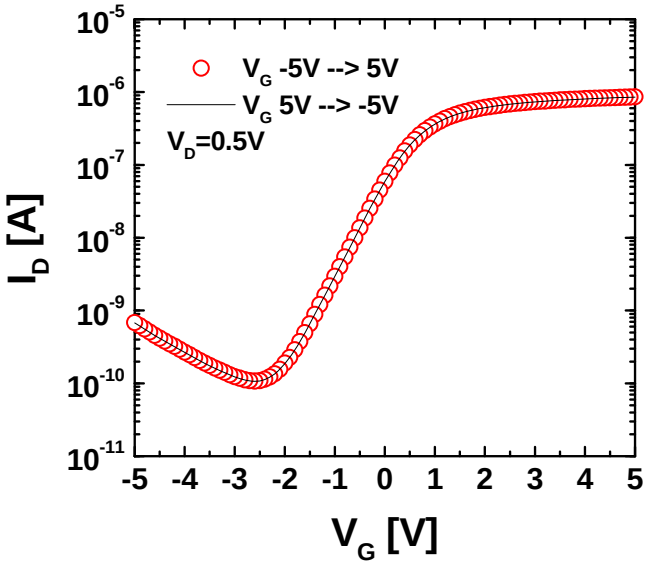

Figure 5.3 Lack of memory window in control Ge TFT without Au NC (*W/L*=50 µm /45 µm).

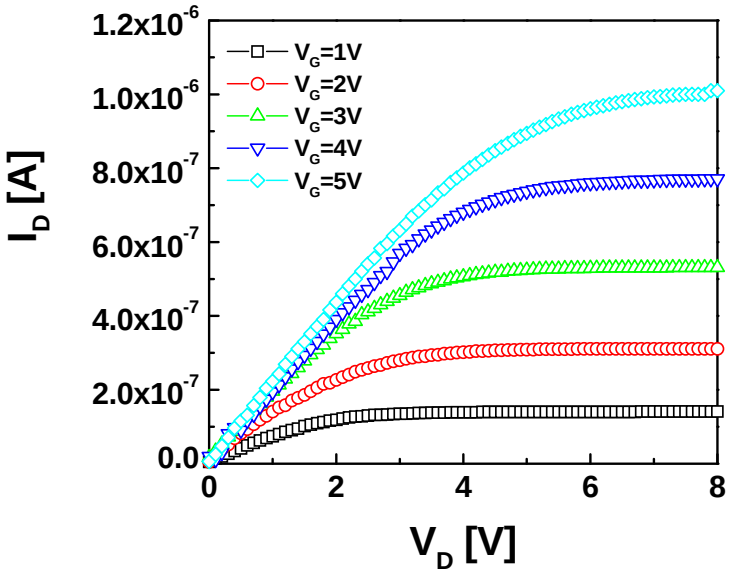

Figure 5.4 Output characteristics of the planar Ge TFT.

Figure 5.5 shows reasonable subthreshold slopes (*S*) and memory windows for the single NCs Ge TFT device for various gate voltage sweeps. We have obtained a

memory window of about 1.8 V by ±5 V P/E voltages for UTB Ge TFT with the gate stack of Al_2O_3/Au/$(Ti,Dy)_xO_y$ and single layer NCs.

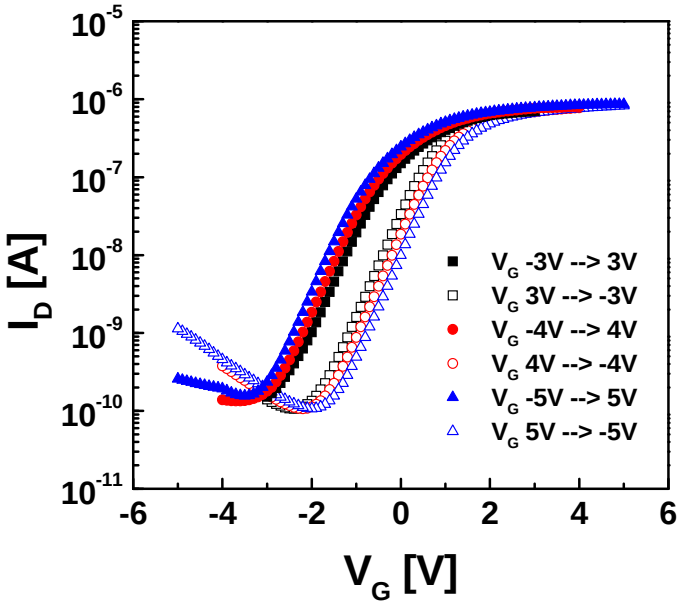

Figure 5.5 Transfer characteristics with gate voltage sweeps for Ge TFT flash memory cells with Au NCs.

Retention characteristics were monitored in the single-NCs Ge TFT device after writing by ±5 V direct pulses of 1 sec duration in Figure 5.6. From the results of Figures 5.5 and 5.6, the retention time and memory window in the single NCs memory cell with the planar Ge UTB film is adaptable for 3-D flash memory to increase the density of transistors. The write/erase time of Au nanocrystal Ge TFT is shown in Figure 5.7. In Figure 5.8, the extracted flat band voltage according to write/erase cycles does not show any memory window degradation, likely due to the low-voltage operations.

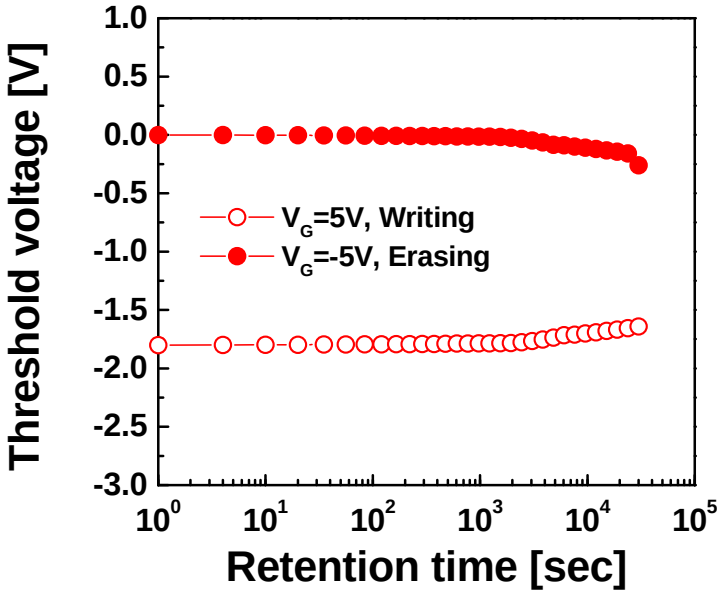

Figure 5.6 Retention time for Ge TFT flash memory cells with Al_2O_3/Au/$(Ti,Dy)_xO_y$ gate stack.

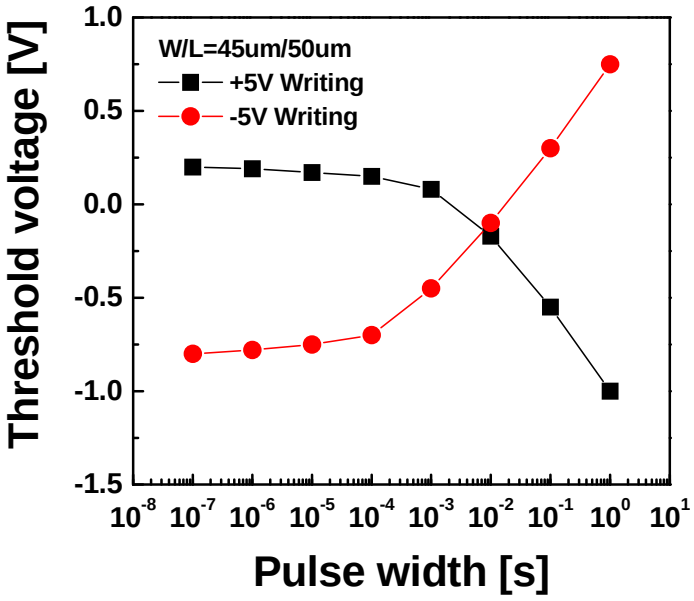

Figure 5.7 Write/erase time test of Au nanocrystal Ge TFT at ±5V.

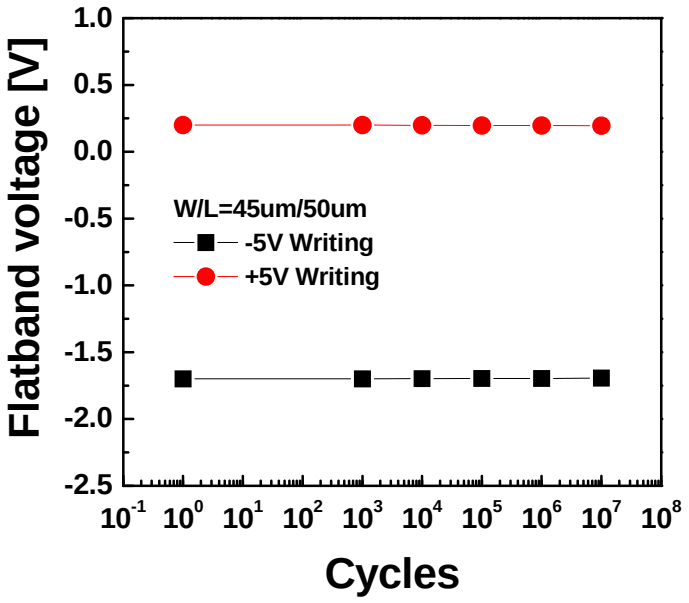

Figure 5.8 Cycle endurance characteristics of Au nanocrystal Ge TFT at ±5V.

From the electrical results, the reliability and performance with the planar Ge UTB TFT using Au NC and high-k dielectrics are adaptable for 3D flash memory integration to increase the bit density per unit area.

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CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

Planar UTB TFT for 3-D integration of flash memory cells has been investigated in this dissertation [1-8]. The scaling limitations of the flash memory cell caused by difficulties with lithography, gate oxide thickness scalability and new material requirements have been discussed. The electrical and physical characteristics using planar UTB and high-k dielectric demonstrate more stability and scaling capability than those of the conventional TFT flash memory cell structure, resulting in prolonged data retention and device reliability.

From the initial discussion of planar polysilicon UTB TFT to the final exploration of electrical and material characteristics of Ge UTB TFT, we have shown that both meet the high-density flash memory requirements and are applicable for 3-D integration.

In Chapter 2, various measurement tools were used to analyze the effectiveness of the planar UTB TFT to alleviate scaling limitations. SEM, STEM, AFM, CBED and EELS analyses confirmed the material characteristics of planar UTB structure with metal nanocrystals. A self-aligned silicidation process to reduce contact resistance was also investigated [5-7].

In Chapter 3, the tunneling barriers in a nanocrystal memory device on planar polysilicon UTB TFT was studied. The effects of the different deposited tunneling barriers, $(Ti,Dy)_xO_y$ and Al_2O_3, on the data retention and memory window were investigated with experimental results. Double layer metal nanocrystal floating gate memories which further improved retention time and enlarged charge storage capacity

was also described in Chapter 3. We have obtained memory windows of $(Ti,Dy)_xO_y$, Al_2O_3 and double layer about 0.95 V, 2.3 V and 3.0 by ±6 V P/E voltages, respectively [2, 3, 5-8].

In Chapter 4, the fabrication procedure, self-aligned silicidation (SAS) to reduce the contact and sheet resistance in the source and drain regions, was presented. Based on the electrical results of chapter 4, the SAS process proved more than adequate in achieving process stability and improvement of source resistance. We have obtained a memory window of about 3.1 V by ±5 V P/E voltages. The retention time of Ni silicided NC memory by ±5 V P/E is extracted to be well beyond 10 years [4].

The planar Ge UTB TFT process for 3-D integration was investigated in Chapter 5. An analysis of the material and electrical characteristics of Ge UTB TFT using high-k dielectric was performed. This analysis planar Ge UTB TFT using proper high-k dielectric shows its high adaptability for high-density flash memory cells. We have obtained a memory window of about 1.8 V by ±5 V P/E voltages for UTB Ge TFT with the gate stack of Al_2O_3/Au/$(Ti,Dy)_xO_y$ and single layer NCs [1].

6.2 Future Work

To achieve the stable process and high performance device for 3-D integration of planar UTB flash cells, further investigations are suggested in the following aspects:

For the planar polysilicon UTB TFT,

1. Optimization of coupling ratio (tunneling oxide/control oxide ratio) to increase the electric field on the tunneling oxide during program/erase while maintaining the retention specification.

2. Further improve the metal induced process to crystallize polysilicon channel for

increasing channel current.

3. The quantitative study on reliability of UTB TFT with metal nanocrystals and high-k dielectric to improve the effect of interface traps on memory performance further, including charge pumping and temperature instability.

4. Formation of higher number density of metal nanocrystals to increase the threshold voltage shift.

5. Fabrication of multiple-layer nanocrystals to increase the charge storage capacity.

6. Demonstration of the minimal parameter sheet in bottom layer UTB TFT flash memory cells buried under at least three repetitive TFT processes.

For the planar Ge UTB TFT,

1. Low-temperature overall process (< 450 °C) to be applicable to the back-end process.

2. Metal induced process to crystallize Ge channel for increasing channel current.

3. Optimization of high-k dielectric process to stabilize the device performance.

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APPENDIX 1

Process Sequence of Polysilicon TFT for Flash Memory Cell

Process number	Process description	Process parameter	Notes	Equipment
Define Key open pattern: Mask 0: Key open				
1	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
2	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
3	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
4	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
5	Inspection	Inspect key area		Scope
6	Post bake.	Follow resist data sheet.	115 °C, 90 sec	Hotplate
7	Silicon Substrate etch	Si etch rate =1μm/min. Etching gas : SF_6/O_2 Time= 1 min. 30sec.	Target depth =1.5μm (1.5min.)	Oxford 80-1
8	Ashing	Recipe #5	RF time =60 sec Removal rate	Aura 1000

			=2.9 μm	
9	Inspection	Measure key area depth	Depth = 1.5μm	P-10
MOS clean				*MOS hood*
10	Base bath.	10 min.		
	DI rinse.	Resistivity > 16		
	Acid rinse.	10 minutes		
	DI rinse.	Resistivity > 16		
11	Buried oxide	Temp. = 400 °C, Time = 1 min. Deposition rate = 230 nm/min.	target thickness ~230nm	GSI PECVD
12	Inspection		target thickness ~230nm	Filmetrix
MOS clean				*MOS hood*
13	Base bath.	10 min.		
	DI rinse.	Resistivity > 16		
	Acid rinse.	10 minutes		
	DI rinse.	Resistivity > 16		
14	Polysilicon deposition	Doped (Phosphorous, 10^{19} cm^{-3}) poly deposition	Time=22 min. Deposition rate = 4.6 nm/min.	Poly (LPCVD)
15	Inspection	Filmmetrix	target thickness =100 nm	Filmmetrix
16	Annealing	700C 1hr.	N2 ambient	Anneal 4
Sample CMP				
17	HF dip.	100:1 1min.		Wet bath
18	CMP process	Chuck and table speed=15 rpm Down force =4	Target thickness = 20 nm	Strasbaugh 6EC

		psi		
19	HF dip.	100:1 1min.		Wet bath
20	Cleaning after CMP Process	in-situ process		Hamatech post CMP brushcleaner
21	Inspection	Measured point = 30 point	Target thickness = 20 nm	Filmetrix
Main CMP				
22	HF dip.	100:1 1min.		Wet bath
23	CMP process	Chuck and table speed=15 rpm Down force =4 psi	Target thickness = 20 nm	Strasbaugh 6EC
24	HF dip.	100:1 1min.		Wet bath
25	Cleaning after CMP Process	in-situ process		Hamatech post CMP brushcleaner
26	Inspection	Measured point = 30 point	Target thickness = 20 nm	Filmetrix
27	Back side poly etching	Si etch rate =1 μm/min. Etching gas : SF_6/O_2 Time= 1 min. 30sec.	Target depth =1.5μm (1.5min.)	Oxford 80-1
Define active pattern : Mask 1: Active mask.				
28	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30	Wash wafer with Acetone and IPA on spinner, then apply P20 and	Spinner

		sec.	S1813.	
29	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
30	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
31	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
32	Inspection	Inspect key area		Scope
33	Post bake.	Follow resist data sheet.	115 °C, 90 sec	Hotplate
34	Poly etch	Polysilicon etch rate =150 nm/min. Etching gas : SF_6/O_2 Time= 1 min.	Etch target = 150 nm	Oxford 80-1
35	Ashing	Recipe #5	RF time=60 sec Removal rate =2.9 μm	Aura 1000
36	Inspection	Filmetrix	Target thickness = 0 nm	Filmetrix
Define Self-aligned Gate Stack : Mask 2: LOR mask				
37	LOR spinning.	Spin condition 3000 RPM, 45sec LOR 5A		Spinner
38	LOR prebake.	180C, 5min		Hotplate
39	Resist spinning.	Photo resist : S1813 for 5x stepper.	Wash wafer with Acetone and IPA on	Spinner

		Spin condition: 4000 rpm, 30 sec.	spinner, then apply P20 and S1813.	
40	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
41	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
42	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
43	Resist post-bake.	Follow resist data sheet.	115 °C, 1 min 30 sec	Hotplate
44	Tunnel oxide growth.	(Ti,Dy)O	Physical thickness = 31 nm EOT = 3 nm	Sputter
45	Inspection		Target thickness = 31 nm	Filmmetrix
46	Au nano crystal formation	Evaporation of Au	Thickness = 1.2 nm	CVC SC4500
47	Control oxide	(Ti,Dy)O	Physical thickness = 60 nm EOT = 6.7 nm	Sputter
48	Inspection		target thickness = 60 nm	Filmmetrix
49	Gate deposition.	Evaporation of Cr	200 nm	CVC SC4500
50	Lift-off resist	Ashing solution : 1165	Dip the wafer for 1 day	
51	Inspection	Pattern		Scope

		(Transistor area) inspection		
52	Passivation	5% H_2/N_2	400 °C 30 min.	Anneal 3,4

APPENDIX 2

Process Sequence of SAS for flash memory cell with polysilicon TFT

Process number	Process description	Process parameter	Notes	Equipment
Define Key open pattern: Mask 0: Key open				
1	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
2	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
3	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
4	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
5	Inspection	Inspect key area		Scope
6	Post bake.	Follow resist data sheet.	115 °C, 90 sec	Hotplate
7	Silicon Substrate etch	Si etch rate =1μm/min. Etching gas : SF_6/O_2 Time= 1 min. 30sec.	Target depth =1.5μm (1.5min.)	Oxford 80-1
8	Ashing	Recipe #5	RF time=60 sec Removal rate =2.9 μm	Aura 1000
9	Inspection	Measure key	Depth = 1.5μm	P-10

		area depth		
10	Buried oxide	Temp. = 400 °C, Time = 1 min. Deposition rate = 230 nm/min.	target thickness ~230nm	GSI PECVD
11	Inspection		target thickness ~230nm	Filmetrix
MOS clean				
12	Base bath.	10 minutes		MOS hood
	DI rinse.	Resistivity > 16		
	Acid rinse.	10 minutes		
	DI rinse.	Resistivity > 16		
13	Polysilicon deposition	Doped (Phosphorous, 10^{19} cm^{-3}) poly deposition	Time=22 min. Deposition rate = 4.6 nm/min.	Poly (LPCVD)
14	Inspection	Filmmetrix	target thickness =100 nm	Filmmetrix
15	Annealing	700C 1hr.	N2 ambient	Anneal 4
CMP				
16	HF dip.	100:1 1min.		Wet bath
17	CMP process	Chuck and table speed=15 rpm Down force =4 psi	Target thickness = 20 nm	Strasbaugh 6EC
18	HF dip.	100:1 1min.		Wet bath
19	Cleaning after CMP Process	in-situ process		Hamatech post CMP brushcleaner
20	Inspection	Measured point = 30 point	Target thickness = 20 nm	Filmetrix
21	Back side poly	Si etch rate	Target depth	Oxford 80-1

	etching	=1 μm/min. Etching gas : SF_6/O_2 Time= 1 min. 30sec.	=1.5 μm (1.5 min.)	
Define active pattern : Mask 1: Active mask.				
22	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
23	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
24	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
25	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
26	Inspection	Inspect active area		Scope
27	Post bake.	Follow resist data sheet.	115 °C, 90 sec	Hotplate
28	Poly etch	Polysilicon etch rate =150 nm/min. Etching gas : SF_6/O_2 Time= 1 min.	Etch target = 150 nm	Oxford 80-1
29	Ashing	Recipe #5	RF time=60 sec Removal rate =2.9 μm	Aura 1000
30	Inspection	Filmetrix	Target thickness	Filmetrix

			= 0 nm	
Define Self-aligned Gate Stack : Mask 2: LOR mask				
31	LOR spinning.	Spin condition 3000 RPM, 45sec LOR 5A		Spinner
32	LOR prebake.	180C, 5min		Hotplate
33	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
34	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
35	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
36	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
37	Resist post-bake.	Follow resist data sheet.	115 °C, 1 min 30 sec	Hotplate
38	Tunnel oxide growth.	ALD Al_2O_3	Physical Thickness6.4nm EOT : 2.5nm	ALD
39	Au nano crystal formation	Evaporation of Au	Thickness = 1.2 nm	CVC SC4500
40	Control oxide	(Ti,Dy)O	Physical thickness = 60 nm EOT = 6.7 nm	Sputter
41	Inspection		target thickness = 60 nm	Filmmetrix

42	Gate deposition.	Evaporation of Cr	200 nm	CVC SC4500
43	Lift-off resist	Ashing solution : 1165	Dip the wafer for 1 day	
44	Inspection	Pattern (Transistor area) inspection		Scope
Define spacer for silicidation. : Mask 3: spacer mask				
45	LOR spinning.	Spin condition 3000 RPM, 45sec LOR 5A		Spinner
46	LOR prebake.	180C, 5min		Hotplate
47	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
48	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
49	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
50	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
51	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
52	SiO_2 deposition	SiO_2 50nm		CVC SC4500

53	Lift-off resist	Ashing solution : 1165	Dip the wafer for 1 day	
54	Inspection	Pattern (Transistor area) inspection		Scope
55	Ni deposition	Ni 2 nm		CVC SC4500
56	Annealing	450 ºC 30 min. N_2 ambient		Anneal 3, 4
57	Unreacted Ni removal	H2SO4:H2O2 (1:4) 60°C 5 min.		Wet batch
58	Passivation	5% H_2/N_2	400 °C 30 min.	Anneal 3,4

APPENDIX 3

Process Sequence of Ge TFT for Flash Memory Cell

Process number	Process description	Process parameter	Notes	Equipment
Define Key open pattern. : Mask 0: Key open.				
1	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
2	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
3	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
4	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
5	Inspection	Inspect key area		Scope
6	Post bake.	Follow resist data sheet.	115 °C, 90 sec	Hotplate
7	Silicon Substrate etch	Si etch rate =1μm/min. Etching gas : SF_6/O_2 Time= 1 min. 30sec.	Target depth =1.5um (1.5min.)	Oxford 80-1
8	Ashing	Recipe #5	RF time=60 sec	Aura 1000

			Removal rate =2.9 µm	
9	Inspection	Measure key area depth	Depth = 1.5 µm	P-10
10	Buried oxide	Temp. = 400 °C, Time = 1 min. Deposition rate = 230 nm/min.	Target thickness = 230nm	GSI PECVD
11	Nitride deposition	Temp. = 400 °C, Time = 1 min. Deposition rate = 115 nm/min.	Target thickness = 115 nm	GSI PECVD
12	Ge deposition	Evaporation of Ge	Thickness = 100 nm	CVC SC4500
13	Ion implantation	Phosphorous 10^{19} cm^{-3} Energy : 30KeV, tilt : 7º		Eaton implater
14	Nitride deposition	Temp. = 400 °C, Time = 1 min. Deposition rate = 115 nm/min.	Target thickness = 115 nm	GSI PECVD
15	Annealing	600 ºC 30 min. N_2 ambient		Anneal 3, 4
16	nitride etch	Nitride etch rate =27 nm/min. Gas CHF_3/O_2 Time= 4 min	Etch target = 115 nm	Oxford 80-1

		20sec.		
17	D.I water cleaning	spin dryer		Wet bath
18	CMP process	Chuck and table speed=15 rpm Down force =4 psi	Target thickness = 20 nm	Strasbaugh 6EC
19	Cleaning after CMP Process	in-situ process		Hamatech post CMP brushcleaner
Define active pattern. Mask 1: Active mask.				
20	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
21	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
22	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
23	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
24	Inspection	Inspect key area		Scope
25	Post bake.	Follow resist data sheet.	115 °C, 90 sec	Hotplate
26	Ge etch	Ge etch rate =120 nm/min. Gas CF_4 Time= 30sec.	Etch target = 30 sec	Oxford 80-1
27	Ashing	Recipe #5	RF time=60 sec	Aura 1000

			Removal rate =2.9 μm	
Define Self-aligned Gate Stack. : Mask 2: LOR mask				
28	LOR spinning.	Spin condition 3000 RPM, 45sec LOR 5A		Spinner
29	LOR prebake.	180C, 5min		Hotplate
30	Resist spinning.	Photo resist : S1813 for 5x stepper. Spin condition: 4000 rpm, 30 sec.	Wash wafer with Acetone and IPA on spinner, then apply P20 and S1813.	Spinner
31	Resist prebake.	Follow resist data sheet.	90 °C, 1 min	Hotplate
32	Align and expose wafers.	Exposure time : 0.8sec		5X Stepper
33	Resist development.	Use auto developer MIF300 90 sec.	Recipe : #6	Hamatech-Steag wafer processors
34	Resist post-bake.	Follow resist data sheet.	115 °C, 1 min 30 sec	Hotplate
35	Tunnel oxide growth.	ALD Al_2O_3	Physical Thickness6.4nm EOT : 2.5nm	ALD
36	Inspection	Filmetrix (monitoring wafer)	target thickness ~ 6.4nm (physical thickness)	Filmetrix
37	Au nano crystal formation	Evaporation of Au	Thickness = 1.2 nm	CVC SC4500
38	Control oxide	(Ti,Dy)O	Physical thickness	Sputter

			= 60 nm EOT = 6.7 nm	
39	Inspection		target thickness = 60 nm	Filmmetrix
40	Gate deposition.	Evaporation of Cr	200 nm	CVC SC4500
41	Lift-off resist	Ashing solution : 1165	Dip the wafer for 1 day	Wet bath
42	Inspection	Scope	Pattern(Transistor area) inspection	