# ULTRA NARROW SILICON FETS INTEGRATED WITH MICROFLUIDIC SYSTEM FOR SERIAL SEQUENCING OF BIOMOLECULES BASED ON LOCAL CHARGE SENSING

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Ultra-narrow channel silicon field effect transistors (FET) with suspended gates, integrated with on-chip micro-fluidic delivery system are demonstrated. These devices are designed to be used for serial sequencing of DNA, RNA and proteins, by detecting the local charge variations along these molecules as they are passed between the gate and the channel of the FETs in an aqueous solution.

Devices are fabricated with down to 5 nm high tunnels passing between the gate and the channel of the FETs, integrated with larger scale micro-fluidic delivery system. The smallest fabricated active area width is less than 10 nm. A silicon nitride based shallow trench isolation (STI) scheme is developed in order to accommodate fabrication of the tunnels going through the FET, through removal of sacrificial silicon dioxide in HF.

A device architecture with an independently controlled side-gate, surrounding the active area, is developed to suppress the edge related leakage currents and allow further scaling of the device width while achieving high sensitivity. The side-gated devices are fabricated as nFET prototypes using thermally grown silicon dioxide gate insulator and silicon nitride STI. The leakage currents are suppressed below 50 fA down to 70 nm gate length with the application of a negative side-gate bias.

Side-gated sub-10 nm wide devices exhibit threshold voltage tunability in a range exceeding 2.5 V and with a maximum sensitivity of $\delta V_t/\delta V_{side} > 2$ V/V. Wider channel devices with gate lengths less than 70 nm retain $I_{on}/I_{off}$ ratios exceeding $10^9$

and achieve drive currents exceeding 1.5 mA/μm. Narrow channel devices with 150 nm gate length show less than 5 mV/V drain induced barrier lowering. With these performance parameters, side-gated device geometry is a promising candidate for future generation low-power, and higher performance circuits. The possibility of using this device geometry as a side-trapping FLASH memory structure is also demonstrated.

A capacitance measurement technique is developed to achieve aF resolution using an instrument with 0.1 fF resolution at 1 MHz utilizing the random fluctuations. These capacitance measurements, performed on the small scale devices, are used to extract effective device dimensions, carrier density and effective carrier mobilities.

BIOGRAPHICAL SKETCH

Ali Gokirmak was born in Van, Turkey. He has completed his early education in Istanbul, Turkey. After finishing his high school education at Kadikoy Anadolu Lisesi in 1994, he started his undergraduate education at University of Maryland at College Park. He received his Bachelor of Science degrees in electrical engineering and physics from University of Maryland at College Park in 1998. He joined the M.S./ Ph.D. program in Department of Electrical and Computer Engineering at Cornell University in 1998. His research interests include applications of nanostructures, nanofabrication technology, small-scale MOSFETs for sensors, logic and non-volatile memories, quantum confinement effects in restricted geometries in MOSFETs, integration of electronics with MEMS/NEMS structures for RF and non-volatile memory applications and electrical measurement techniques.

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To my parents, Nevin and Hikmet Gokirmak

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# 1 Introduction

The objective of this thesis has been the development of an ultra-narrow width silicon field effect transistor (FET) with a suspended gate, integrated with on-chip microfluidic delivery system. The device is designed to be used as an FET based sensor for sequencing of DNA, RNA and proteins, by detecting the local charge variations along the chains of these molecules as the samples are passed between the gate and the channel of the FET (Figure 1.1).

The sequence information of these molecules are important for recognition of living organisms for identification of diseases for medical purposes, biochemical and pharmaceutical research, as well as human identification for judicial cases. Existing methods of bio-molecule sequencing require large-scale laboratories and trained technical staff and rely on statistical analysis. There is a growing demand for small-scale, high-speed bio-molecule sequencing techniques [1][2].

The main device-related challenges for charge based biomolecule sequencing

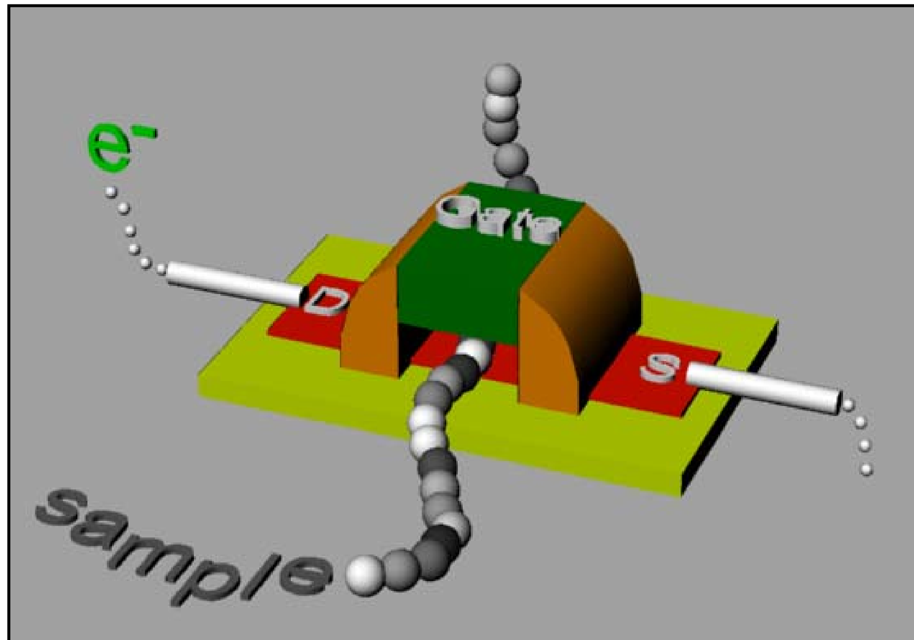


**Figure 1.1** 3D schematics of the device structure. The source-drain current is monitored as the sample is passed perpendicular to the channel of the transistor.

scheme are:

- Fabrication of small scale transistor structures with sub 10 nm channel width and suspended gates in which the sample can be flown between the channel and the gate of the transistor.
- Integration of suspended gate transistors with on-chip microfluidic delivery systems.
- Design of an FET structure which is compatible with these processes and achieve high gain, which will result in a high level of sensitivity.

Using standard CMOS compatible processes allow high sensitivity low noise circuitry to be integrated in close proximity to sensor devices on the same chip. Fabrication techniques using optical lithography, in addition to a CMOS compatible process flow, allow easy transition from prototype to large-scale manufacturing at low-cost in commercial fabrication facilities in the future.

In this thesis two process flows developed to integrate microfludic tunnels with narrow channel silicon air-gap FETs are presented. Hydrofluoric acid (HF) is used to remove sacrificial silicon dioxide in order to fabricate the nano/micro-fluidic tunnels [3][4]. Silicon nitride based shallow trench isolation (STI) schemes are developed so that HF release process can be integrated with the fabrication of narrow channel transistors [5].

The two schemes developed to integrate microfluidic tunnels with the FETs are: monolithic integration, which is described along with the device fabrication in chapter 2 [6], and back-end-of-line integration of microfluidic tunnels, described in chapter 3 [7]. The processes developed for these integration schemes can be used for a number of different applications requiring microfluidic structures.

In addition to a planar Si FET geometry using silicon nitride STI as described in chapter 2, a side-gated device is developed, allowing further scaling of the width of

the transistor. Side-gated devices exhibit excellent transistor characteristics, suitable for sensor applications. The side-gated device structure, with its slight variations, was observed to be a good candidate for future generation high-performance, low-power, low-noise logic and analog devices as demonstrated in chapter 4. The possibility of using this device geometry for trap-based FLASH [8][9] memory structures as a possible alternative for further scaling of FLASH memories is also demonstrated. Side-gated device geometry in combination with HF resistant STI scheme, is very suitable for a number of different applications which include fabrication of tunable resonant-gate structures for high frequency band-pass filter applications [10]-[14] and alternative memory structures (section 4.11) as well as monolithic integration of on-chip resonant electro-mechanical devices with CMOS circuitry.

## 1.1 Background on bio-molecules

Life functions in living organisms are carried out by large organic molecules. DNA is the main information template in every living organism. Cells can replicate copies of the DNA template, and generate RNA templates that are in turn used to generate the proteins needed by the cell [16][17].

DNA and RNA molecules are chains composed of sub-units which are called nucleotides. There are four different kinds of these sub-units forming two complementary pairs, which can selectively bind to one-another (Figure 1.2) [17]. The diameter of double helix DNA structure is approximately 2 nm (Figure 1.3) [15]. The nucleotide spacing in a DNA molecule is 0.34 nm and the sugar-phosphate backbone of the DNA molecule carries a net negative charge in salt solution. Due to this net charge on its backbone, DNA molecules tend to stay unbundled in low concentration salt solutions. The charge distribution over the DNA molecule varies by a very small amount from one nucleotide to another. Although the charge variation along a single-

strand DNA molecule is very small, it is possible to increase the charge contrast significantly by selectively attaching one kind of nucleotide in the matching locations of a single-strand DNA. This can be achieved by immersing a single-strand DNA in a solution which contains only one of the four possible nucleotides.

Proteins, the molecular machinery in living cells, are long chains of amino acids. Amino acids can have different charge levels at different pH values, depending on their side-chains. There are twenty different, naturally occurring amino acids. Proteins are formed by the carboxylic acid site of one aminoacid binding to the amino site of another (Figure 1.4) [18].

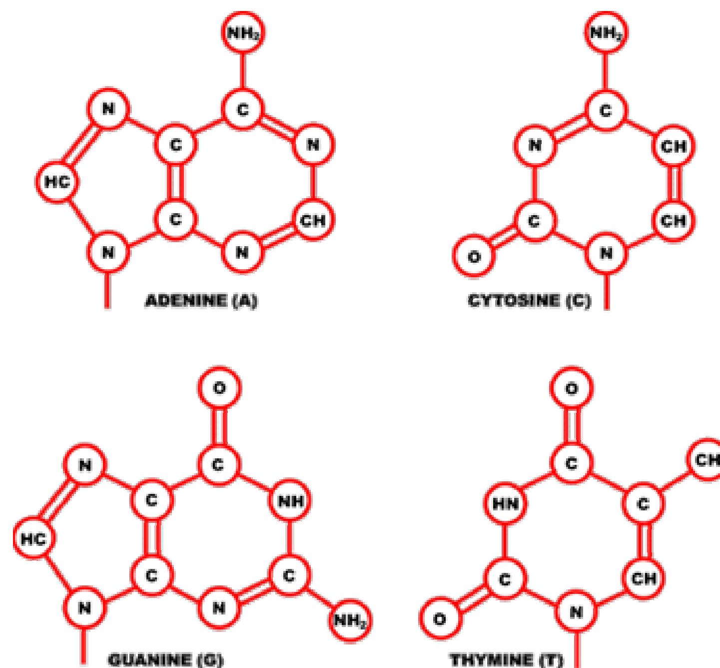


**Figure 1.2** Molecular structure of the four nucleotides found in DNA molecules. The unsatisfied bon on N binds to the sugar-phosphate backbone to form a strand.

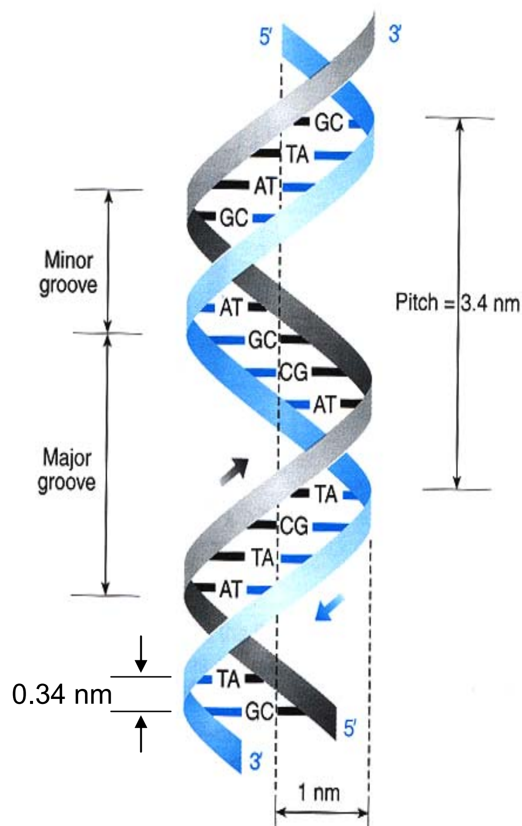


**Figure 1.3** Schematics of double stranded DNA structure. The DNA strands are bonded together through hydrogen bonds between the complimentary pairs [15].

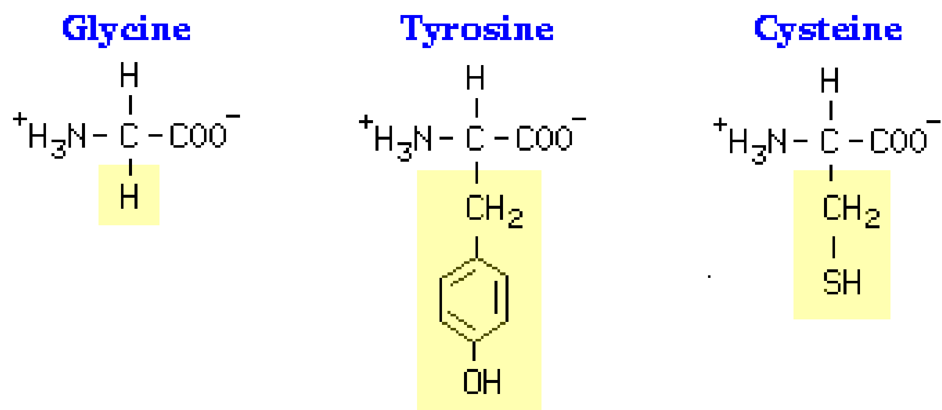


**Figure 1.4** Three examples of naturally occurring amino acids. Amino or the acid group can get activated at certain pH values [18].

## 1.2 Method of detection

A small variation in the electric potential of the channel of a small FET results in a significant change in the drain to source current level. This property makes a narrow channel FET structure a very sensitive sensor for small charges in close proximity [19][20]. The biggest advantage of using an FET is the front-end, intrinsic and high-gain amplification that is achieved when the device is operated in the subthreshold regime [21]. Since the charge detection is performed with a high gain device, the signal to noise ratio is improved over detectors which rely on higher gain amplification in the electronic circuitry used to sense the signal.

In an FET structure, local charges between the channel and the gate of a transistor perturb the channel potential. This potential perturbation is manifested as a change in source-drain current ($I_{ds}$) of a transistor. The magnitude of the perturbation

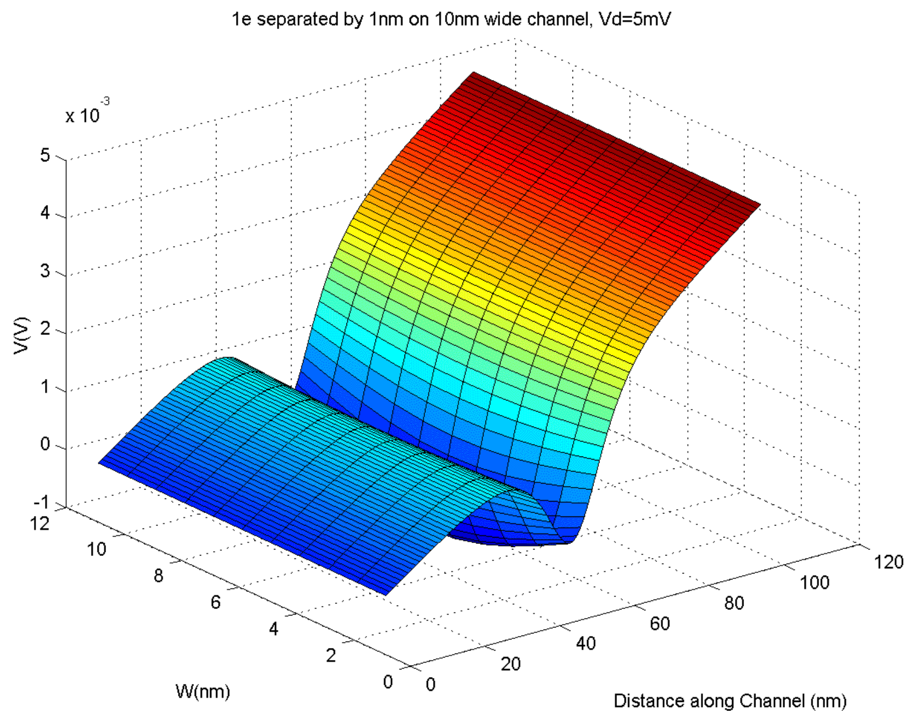


**Figure 1.5** Potential perturbation caused by a dipole over the channel of a 10 nm wide FET in the subthreshold regime.

increases as the distance from the perturbing charge to the channel is reduced. The perturbation is expected to result in a larger change in the current level for narrower channel FETs. However, in the sub-10 nm regime the transistor sensitivity also depends on the channel width due to significant effect of the interface related leakage currents and strong capacitive coupling of the channel to the surrounding. As the dielectric constant of the media is increased, the dipole shielding of the charge increases and reduces the perturbation on the channel potential. This makes it harder to detect charges surrounded by high-permittivity materials, like water.

For a charge dipole of 1 $e^-$ x 1 nm, 10 nm away from the channel surface, within a layer of $SiO_2$, the maximum perturbation on the channel is expected to be in the order of 3 mV if the FET is biased in the subthreshold regime of operation (Figure 1.5). However, it is possible to fabricate the tunnels to be in the order of 6 nm in height and with approximately 2 nm oxide thickness on the active area surface as described in chapter 2. In such a configuration, the DNA molecules can be placed as

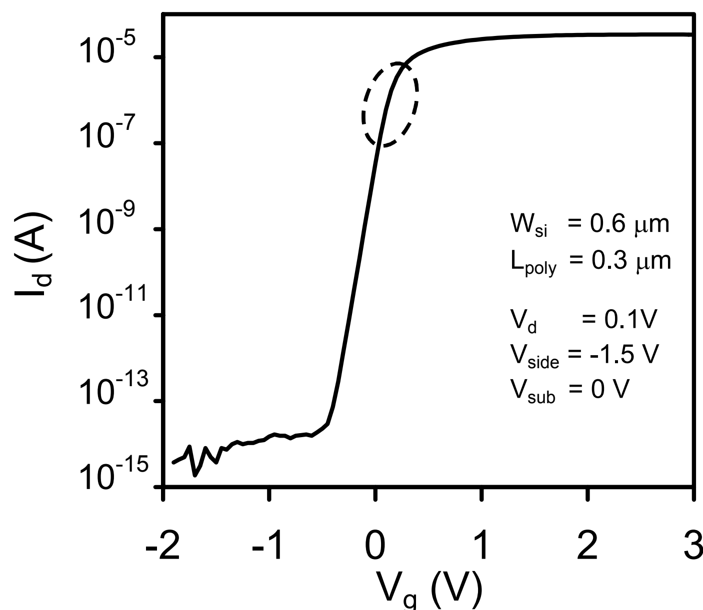


**Figure 1.6** Typical drain current versus gate voltage characteristics of a field effect transistor. The optimum sensitivity is expected to be achieved slightly below onset of inversion (circled regime).

close as 2 nm to the channel surface.

In order to use this technique, the sample has to be passed between the gate and the channel of a narrow channel FET, delivered through micro/nano-fluidic tunnels. Although it is possible to build structures and flow the sample over the channel without a gate electrode, having a gate electrode gives the flexibility of adjusting the bias condition for maximum sensitivity as well as testing the transistor response prior to attempting to sense charges. Figure 1.6 shows a typical $I_{ds}$ - gate voltage ($V_g$) (transfer) characteristics of an FET structure fabricated with 4 nm gate oxide with a subthreshold slope better than 70 mV/dec at room temperature.

The Subthreshold regime of an FET has the highest % gain, $\delta I_{ds} / I_{ds}.\delta V_g$, resulting in the highest sensitivity. The speed and the signal to noise ratio of a transient measurement improve by the amount of current being sensed. The optimum operation regime for sensing is therefore expected to be the higher end of subthreshold regime, slightly below onset of weak inversion, as illustrated in Figure 1.6. A subthreshold slope of 70 mV/dec corresponds to approximately 3% change in $I_{ds}$ for 1 mV change in $V_g$ in the subthreshold regime, which is a measurable change (Figure 1.7). The potential perturbations due to the charges or dipoles over the channel surface result in a local potential change in the channel rather than an increase in the whole channel potential. If the effect of the point charges are approximated as uniform distributions for very small scale devices, the effect of the charges between the gate and the channel can be calculated in terms of amount gate bias required to counter the effect of the charges as discussed in chapter 2. More detailed calculations are needed to understand the effect of the local potential perturbations in narrow channel devices. Similar circumstances with carbon-nanotube devices are analyzed by Guo et. al. [22].

The bias conditions for the transistor are needed to be optimized in order to achieve the maximum sensitivity and signal to noise ratio. However, the electrical potentials on the gate, source, drain and the substrate, also have an effect on the distribution of the ions in the solution, as well as the orientation of the DNA molecule going through the sensor. For low threshold voltage ($V_t$) devices, the gate is needed to be biased negatively in order to achieve the highest FET sensitivity. This repels the negatively charged DNA molecule from the gate surface pushing it towards the electron channel and result in reduced shielding due to the positive ions in the solution (Figure 1.8). For high $V_t$ devices positive gate bias would be required to achieve the highest FET sensitivity. In this case the DNA molecule would be pulled away from the electron channel, being attracted to the gate surface, and the positive ions in the solution would be attracted to the channel surface (Figure 1.9). This configuration of the molecule reduces the perturbation done on the channel potential and it is more pronounced if the tunnel height is much larger than the double strand DNA diameter

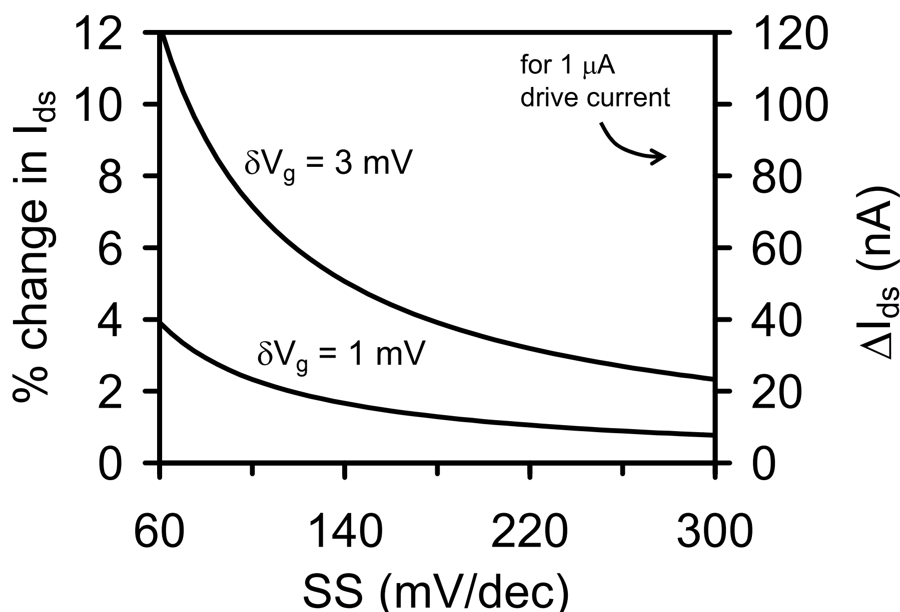


**Figure 1.7** Sensitivity of the FET as a function of the subthreshold slope. Left axis shows the percentage change in drain to source current and right axis is showing the magnitude of the change for bias condition resulting in 1 μA of drive current.

of 2 nm. If the channel height is small, slightly larger than 2 nm, the perturbation from the DNA molecule is expected to be increased when the DNA molecule is attracted to the gate surface since the charge tags attached to the single strand DNA would be facing the channel surface.

In the case of an FET structure with physical channel width of 10 nm, there will be approximately 30 nucleotides over the electron channel at one time if the DNA molecule is oriented orthogonal to the electron channel direction, aligned with the tunnel direction. The special resolution and the sensitivity of the sensor will be limited by the number of nucleotides over the channel at one time. However, if the signal to noise ratio of the device is good enough, it is possible to detect the tagged nucleotides entering the sensing area by taking a derivative of the time-domain signal.

The spatial resolution of the sensor can be increased further, down to approximately 2 nm, by electrostatically confining the electrons by either to the central part of the channel or to the two corners. Confinement of the channel to the central part of the channel can be achieved by forming a parabolic potential profile along the width of the electron channel (Figure 1.10) through employment of additional gates on the two sides of the channel (Figure 1.11). It is possible to achieve this confinement with positive or negative top-gate bias. The width of the electron confinement increases with the electron density due the electrostatic contribution of the electron charge to the potential profile.

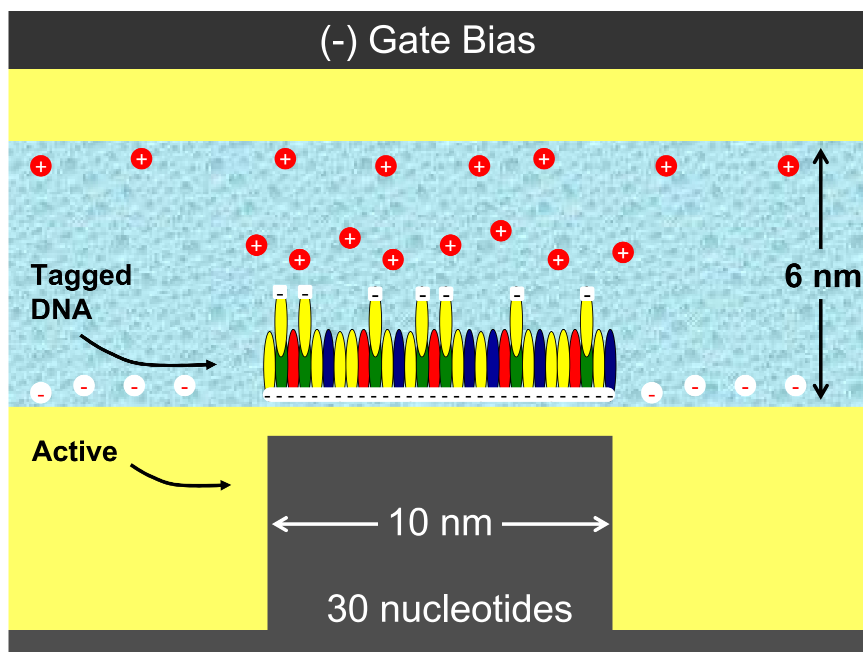


**Figure 1.8** Cross-section schematics of an FET sensor with 10 nm wide electrical channel and 6 nm high nanofluidic tunnel passing under the gate. Orientation of DNA molecule and ion distribution is shown for the case of a negative gate potential.

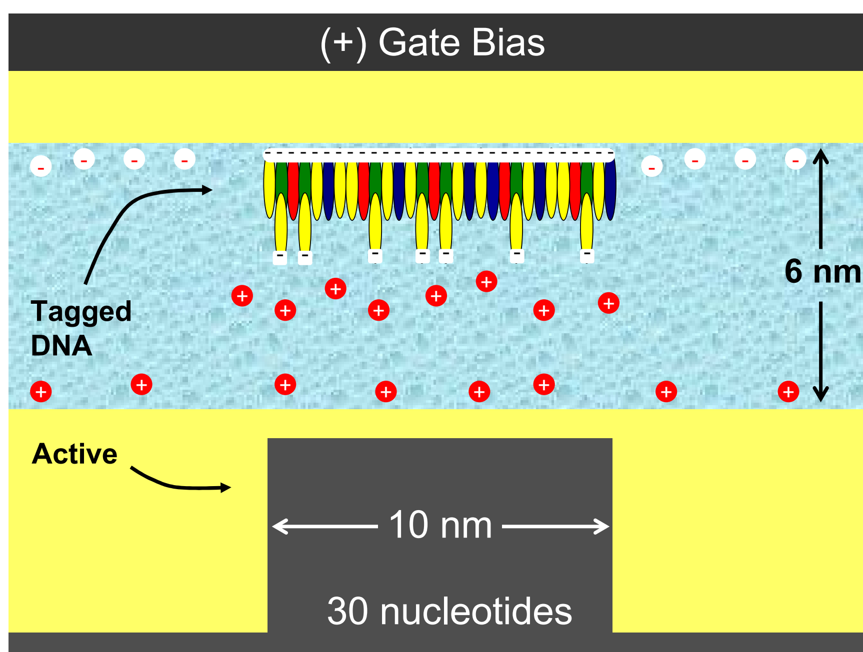


**Figure 1.9** Cross-section schematics of an FET sensor with 10 nm wide electrical channel and 6 nm high nanofluidic tunnel passing under the gate. Orientation of DNA molecule and ion distribution is shown for the case of a positive gate potential.

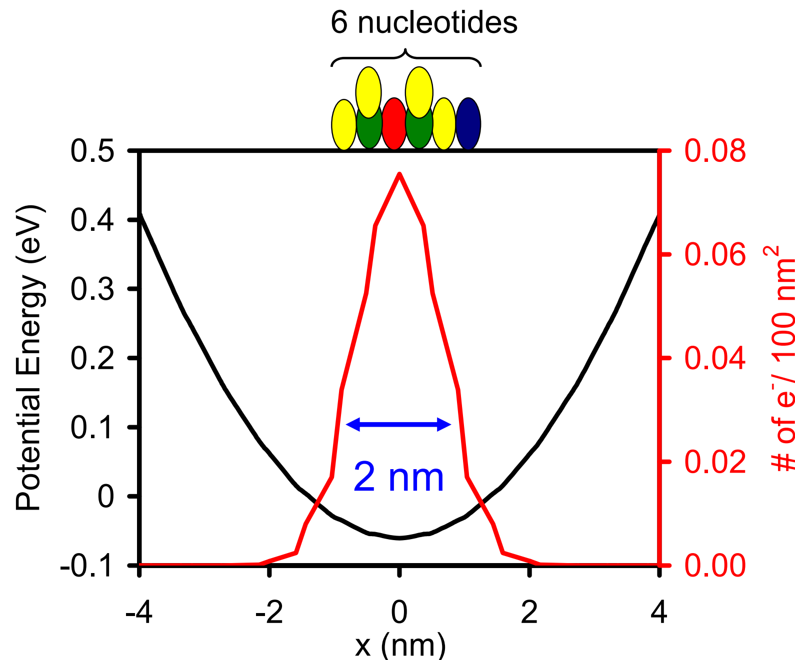


**Figure 1.10** Electron confinement to the central region in a 8 nm wide channel with a parabolic potential profile simulated by using classical electrostatics. It is possible to confine electrons into a 2 nm wide nanowire for low electron concentrations.

Confinement of the electrons to the two edges of the device can be achieved by making use of the fixed charges on the active-isolation interface at the edges (Figure 1.12). In this case, one of the two channels forming on the edges can be eliminated by changing the dopant density on one of the edges through angled implantation, hence changing the threshold voltage of one of the edges with respect to the other. However, in this case, the device has to be operated with a positive top-gate bias and the body doping level should be adjusted appropriately so that the electrical current is confined only the top corners of the silicon active area, without resulting in leakage currents along the side-walls of the silicon active area.

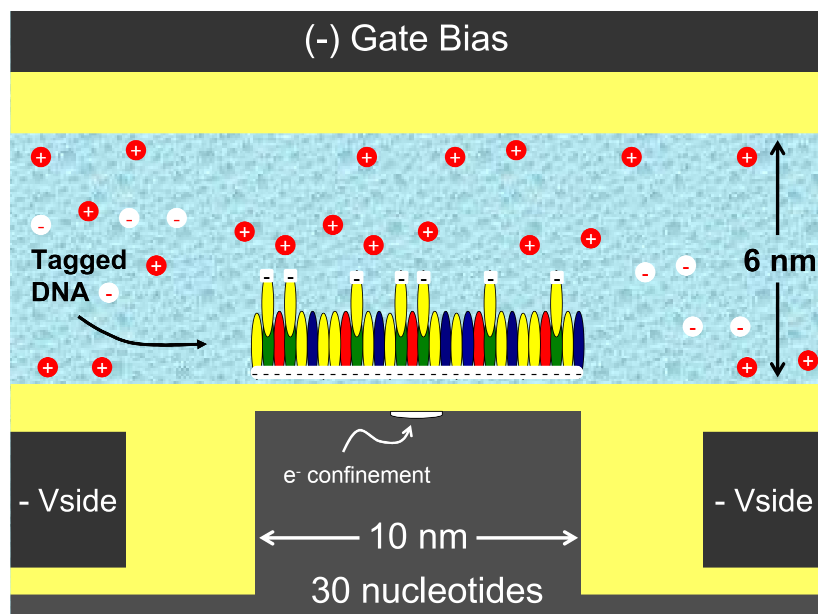


**Figure 1.11** Cross-section schematics of the sensor structure with electrons confined to the central portion of the channel with the aid of additional side-gates. The confinement can be achieved by either applying a negative or positive bias on the top-gate depending on the side-gate bias conditions and the body doping level.

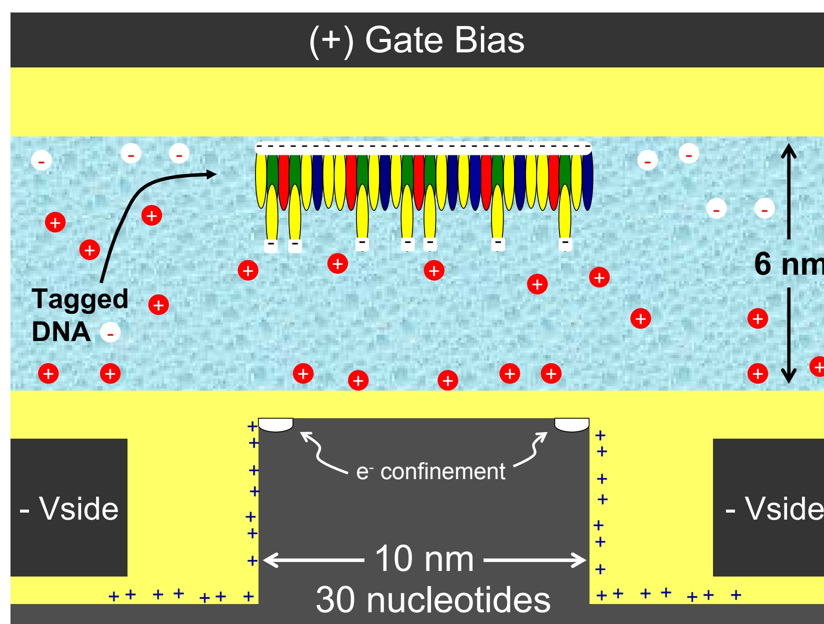


**Figure 1.12** Cross-section schematics of the sensor structure with electrons confined to the two edges of the active area with the aid of interface fixed charges and additional side-gates. Current confinement to the top surface at the edges can only be achieved by application of positive top-gate bias.

Although it is possible to get better channel confinement on the two edges, this case is more prone to current fluctuations due to trapping and de-trapping events taking place in the traps at the active-isolation interface [23]. These trapping and de-trapping events will result in sudden and significant changes in the threshold voltage of the nano-wire formed between the source and the drain. This would result in stepwise changes in the current level similar to the expected current changes due to the potential perturbations caused by the DNA molecules passing over the channel.

The transportation of DNA molecules in nano-fluidic tunnels are usually achieved by application of a DC bias to the solution [24][25]. The electrostatic force applied on the negatively charged DNA molecule results in the motion where the viscosity of the fluid is so significant that no flow is expected to be achieved through a pressure gradient.

## 1.3 Integration of micro/nano-fluidic structures with an air-gap FET

An air-gap transistor can be formed by selectively removing the material deposited as gate insulator (Chapter 2). If this can be achieved, micro/nano-fluidic tunnels can be attached to the system for on-chip sample delivery. Our first approach was to use $Si_3N_4$ as sacrificial gate insulator and a polysilicon gate and remove $Si_3N_4$ using hot phosphoric acid. This process required back-end of the line integration of fluidic sample delivery system. We have successfully developed a process flow for low temperature back end of the line integration of micro-fluidic tunnels which are electrically isolated from the FET structure (Chapter 3). However, removal of ~10 nm thick sacrificial $Si_3N_4$ underneath the gate over a lateral extension of 3-4 μm proved to be unsuitable due to low etch rate, unreliability of the wet etch process and incompatibility with doped polysilicon gate structures. On the other hand, $SiO_2$ can be chemically etched in HF solution very reliably, with an etch rate higher than 1μm/min

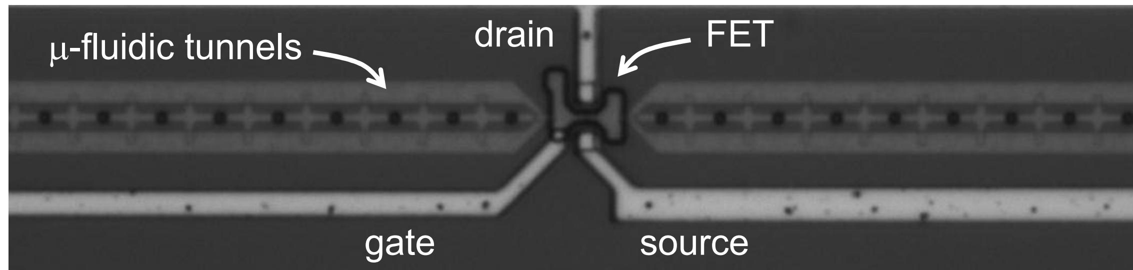


**Figure 1.13** Air-gap FET monolithically integrated with microfluidic sample delivery tunnels using silicon nitride isolation process.

even in very constricted areas [3]. This wet etch process has very good selectivity to both Si and $Si_3N_4$. Integration of an extended wet etch step in HF solution into the process flow entails usage of an alternative dielectric material to $SiO_2$ for device isolation. $Si_3N_4$ is a CMOS compatible isolation material compatible with HF wet etch process which can be taken up to higher temperatures required by the consecutive process steps. I have chosen $Si_3N_4$ as shallow trench isolation (STI) material and succeeded in fabricating ultra-narrow width FETs with polysilicon gates suspended 10 nm above the transistor channel, integrated with microfluidic delivery system (Chapter 2) [5][6].

## 1.4 MOSFET prototypes using silicon nitride STI process

The success of standard Si CMOS is partly due to the low fixed charge density and mechanical properties of Si-$SiO_2$ system. Switching to another dielectric material for device isolation introduces additional mechanical and electrical problems that need to be addressed. Mechanical stress, electrical leakage, high interface defect density at Si-$Si_3N_4$ interface and high concentration of fixed charges in as-deposited $Si_3N_4$ films are the challenges to be addressed in order to use a $Si_3N_4$ based STI process for fabrication of Si FETs.

### 1.4.1 Structural problems

The thermal expansion coefficient of $Si_3N_4$ is significantly higher than that of Si. Since the deposition is performed at around 800 C, $Si_3N_4$ cannot be deposited thicker than approximately 200 nm due to high level of stress that forms as the substrates are cooled down to room temperature. However, thicker films of low stress (silicon rich) silicon nitride can be deposited on Si with an acceptable level of stress. In order to fabricate the FETs, after the definition and etch of the active areas, low stress silicon nitride films are deposited as STI material up to 1.2 μm thick and the wafers are planarized using chemical mechanical polishing (CMP).

### 1.4.2 Electrical problems

Initial FET prototypes using low stress silicon nitride as STI material and LPCVD deposited gate oxide showed significant level of source-to-drain and drain-to-substrate leakage (Figure 1.14). Two of the main problems leading to the leakage currents were identified as the high concentration of defects and fixed charge density

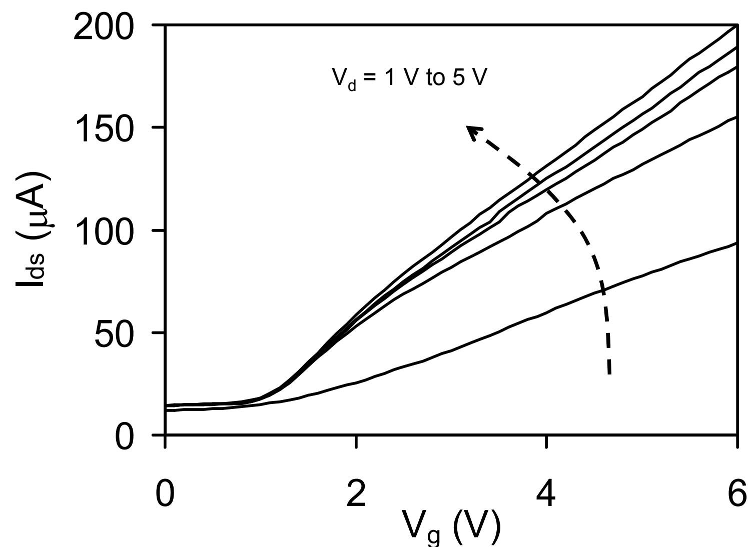


**Figure 1.14** Drain current versus gate voltage characteristics of a field effect transistor build using low stress silicon nitride as STI material, with 10 nm deposited oxide.

in the Si-STI interface and electrical leakage in low stress silicon nitride (Figure 1.15). The relative contribution of these leakage currents on the periphery of the device significantly increase for ultra narrow channel devices. This results in significant degradation of the sensitivity of the FET to any potential changes.

Electrical leakage through low stress nitride can be suppressed by using a thin buffer layer of stochiometric $Si_3N_4$ at the Si-STI interface, capped with a thicker layer of low stress nitride.

Electrical leakage from the reverse biased drain to substrate diode is due to high level of defect assisted recombination current at the Si-$Si_3N_4$ interface [26][27]. The defect assisted recombination process, is most efficient when the Si-$Si_3N_4$ interfaces are depleted. The leakage is significantly suppressed if the Si-$Si_3N_4$ interface is in accumulation or inversion [26][27]. Since inverting the Si-$Si_3N_4$ interface would result in formation of a conduction path between the source and drain of the FET, the drain to substrate leakage can only be suppressed by putting the interfaces into accumulation.

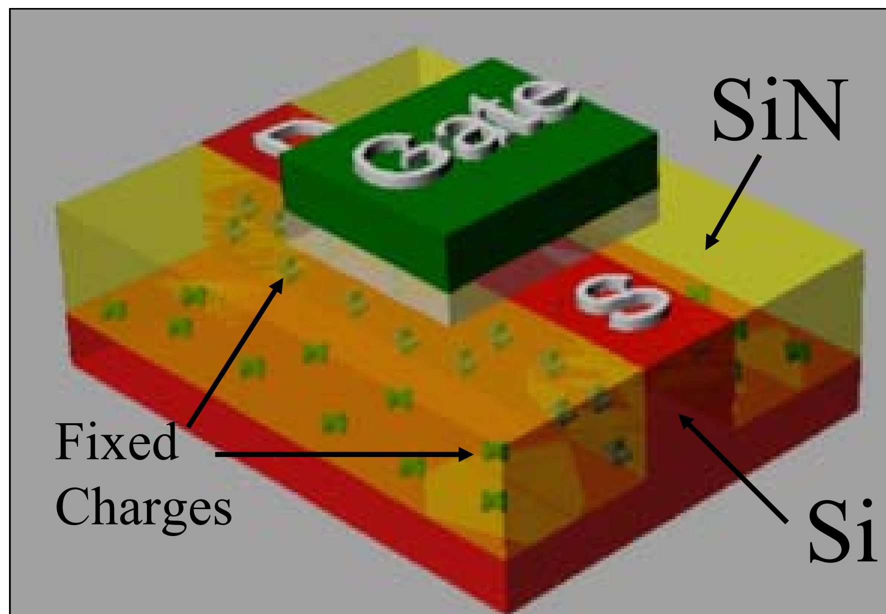


**Figure 1.15** 3D schematics of an FET using silicon nitride as field isolation. There is a high density of fixed charges and defects at the interfaces.

High level of drain to source leakage (off currents) at the Si-STI interfaces of nFETs result from lowered threshold voltage at the interfaces due to positive fixed charges at the interfaces (Figure 1.15). This is a concern even for devices built using $SiO_2$ as isolation material, impeding the device performance [28], though to a lesser extent compared to the $Si_3N_4$ case. Increase of the body potential restores the potential barrier between the source and drain at the interfaces, increasing the threshold voltage and suppressing the drain to source leakage. This increase in the bulk potential, compared to source potential, can be achieved by either increasing the dopant concentration at the Si-STI interface or by employing additional gates surrounding the active area of the devices, supplied with a negative bias [29]. Both of these approaches would result in suppression of the drain to substrate leakage currents due to the reduction in the depletion depth of the junctions. In the case of a negatively biased additional gate surrounding the active area, accumulation of the interfaces can be achieved easily by tuning the side-gate bias, resulting in even lower level of leakage currents [26][27].

The process flow for increasing the body dopant concentration at the interfaces is discussed in chapter 2, resulting in suppression of leakage currents below $10^{-10}$ A in a narrow channel device with 1 μm gate length.

## 1.5 Side-gated FET

The approach of integration of additional gates in order to suppress the leakage currents resulted in the device design discussed in chapter 4. In this device design, an independently controlled polysilicon side-gate surrounds the active area. Side-gated devices with thermally grown top-gate oxide are fabricated as prototype FETs in order to understand the device behavior before integration with micro/nanofluidics. The processing of the side-gated devices is compatible with the processes developed for

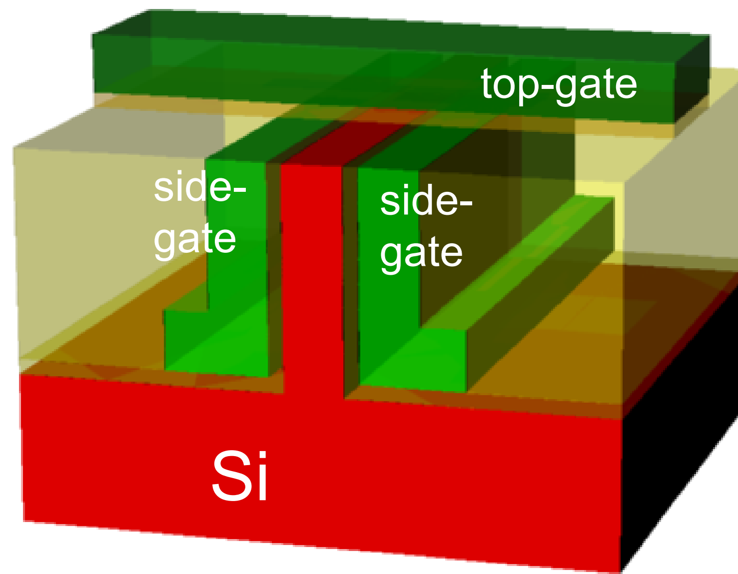


**Figure 1.16** 3D schematics of side-gated FET utilizing silicon nitride field isolation. The two side-gates are connected together and the top gate is operated independently.

forming a nano-fluidic tunnel under the gate and integration of micro-fluidic delivery system.

Using this approach, the leakage currents were suppressed below $10^{-14}$ A and remarkable device characteristics were observed. Two different device structures were obtained by slightly varying the process steps.

### 1.5.1 High performance FETs

Side-gated devices have distinctly different characteristics depending on the channel width and if the side-gates are recessed compared to the active area as opposed to being at the same level (Figure 1.17). The recessed side-gate devices' threshold voltage does not depend on the side-gate bias. The electrical device characteristics of recessed side-gate devices and planar devices were both observed to be comparable or superior to those of modern high performance CMOS devices. Measured device characteristics are remarkable down to sub-70 nm in gate length and sub-100 nm in channel width, retaining $I_{on}/I_{off}$ ratios exceeding $10^9$, subthreshold

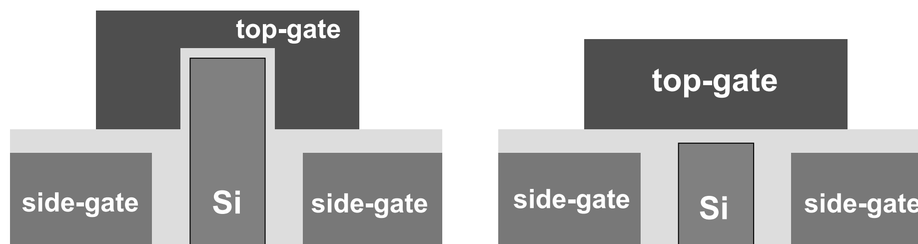


**Figure 1.17** Cross section schematics of devices with recessed side-gates (left) and planar top-gate geometry.

slopes better than 80 mV/dec, and drive currents up to 1.5 mA/µm (section 4.4.6). Devices with 0.3 µm gate length show subthreshold slopes down to 65 mV/dec. and $I_{on}/I_{off}$ ratios exceeding $5x10^{10}$ (section 4.4.4). Devices with effective width in the order of 40 nm exhibit drain induced barrier lowering (DIBL) as low as 2 mV/V with 150 nm gate length (section 4.4.5). These device characteristics, described in detail in chapter 4, make this device architecture suitable for high performance, low-power logic, analog circuit and memory applications.

### 1.5.2 Ultra-narrow width planar FETs

Side-gated devices with planar top surface geometry show significant threshold voltage response to the side-gate potentials. The threshold voltage response increases as the width of the transistor is scaled down. For sub-10 nm channel width, threshold voltage is tunable in a range exceeding 2.5 V with an average sensitivity of 1.55 V/V to the side-gate bias (section 4.4.7). This level of threshold voltage tunability is significantly higher than the values reported for threshold voltage tunable devices in the literature so far [30]-[33].

## 1.6 aF resolution C-V characterization of nanoscale FETs

A high resolution C-V characterization technique was needed in order to understand the behavior of very small-scale devices and to extract important device parameters such as inversion layer charge density, effective device dimensions and

carrier mobility. After evaluation of possible approaches reported in the literature on fF resolution C-V measurement techniques and experiments conducted in the lab, I have developed a technique to measure inversion layer capacitances of these small scale devices with aF resolution, utilizing the ambient noise [34], using a commercial HP 4275A RLC meter (Chapter 5). This technique of utilizing ambient noise is also demonstrated to be useful for measuring current levels below 10 fA using a HP 4145B parameter analyzer with 50 fA current resolution (section 5.4).

# 2 Monolithic Integration of Micro/nano-fluidic tunnels with FET based chemical sensors.

## 2.1 Introduction

Main challenges in the fabrication of the ultra narrow-width FET based chemical sensors are in implementing a process flow to fabricate FET structures with tunnels passing between the gates and the channels of the transistors, integrating these transistors with on-chip microfluidic delivery systems, and developing the FET design to achieve high sensitivity, compatible with the process flow.

Fabrication processes for on-chip micro-electromechanical structures have been developed extensively in the past decades. Similarly many of the issues in fabricating very small scale FETs have been addressed by the semiconductor industry which also resulted in a large number of tools and significant expertise in building silicon based semiconductor devices. However, integration of microfluidics with electronics has a number of process integration challenges.

On-chip micro fluidic systems and suspended structures are usually built by depositing a sacrificial layer which is capped with another layer. HF removal of sacrificial $SiO_2$ in order to release polysilicon or silicon nitride structures is a reliable CMOS compatible process [3][4]. However, the requirement of HF release process makes it very hard to integrate these MEMS elements with electronics and CMOS circuitry utilizing $SiO_2$ electrical isolation in close proximity. One possible approach to overcome this problem is to use HF resistant isolation material for shallow trench isolation of the electronic devices.

In this chapter, a process flow for making narrow channel Si FET structures using silicon nitride STI with the option of monolithically integrated micro-fluidic

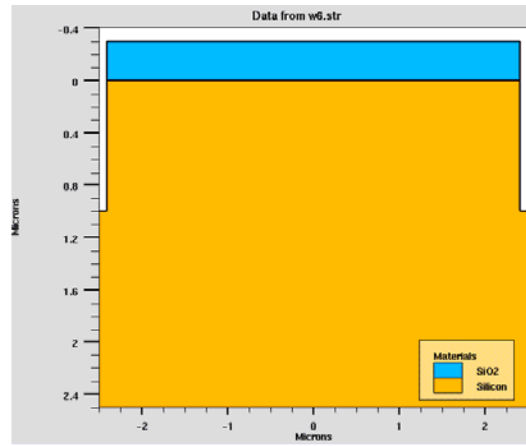


**Figure 2.1** Cross section view after the alignment mark RIE.

delivery system is described. An alternative scheme for integration of micro-fluidic tunnels after the fabrication of the FET structures is discussed in the following chapter.

## 2.2 Fabrication process

The fabrication processes used to build these structures utilize standard CMOS processes and i-line optical stepper. The details of the process flow are described below, and the process parameters for each step are presented in the appendix (section 7.1).

### 2.2.1 Alignment marks

The first lithography step is making the alignment marks and the device labels. In order to etch down the alignment marks and the active area patterns in the following step, 300 nm of thermal oxide is grown in $H_20$ / $N_2$ ambient at atmospheric pressure. After vapor priming of the surface in HMDS oven, 0.6 μm of SPR 620-7i is spun on the wafers, and baked at 90 C for 75 seconds on a hot plate. Wafers are exposed with GCA AS200 Autostep i-line stepper with an exposure time of 0.36 sec. Wafers are baked at 115 C for 90 seconds on a hot plate and chemically developed in AZ 300 MIF for 90 seconds. After a 15 s oxygen plasma descum, the alignment mark patterns are etched into the oxide layer using $CHF_3/O_2$ reactive ion etch (RIE). After removing

the photoresist using $O_2$ RIE, a 30 - 45 s of $CHF_3/O_2$ RIE is performed to clear the thin oxide film formed on the surface during the $O_2$ RIE step. Immediately after this step, the alignment marks are etched down approximately 1 μm into silicon using $Cl_2/BCl_3$ RIE (Figure 2.1).

### 2.2.2 Active area definition

The active areas of the devices are defined by etching into the Si substrates. Shallow trench isolation (STI) is used as the isolation scheme for the devices. The patterning of the oxide hard mask and etching of the Si substrate are identical to the patterning of the alignment mark level, this time using the 'active layer' mask for photolithography. The mask oxide remaining on the wafer from the previous step is used as hard mask to etch Si.

The active layer is aligned to the alignment mark layer using global alignment by finding the marks under the microscope and using local alignment for which the stepper locates the local alignment marks through an automated scheme using interferometric means. Local alignment achieves better than 100 nm alignment between the two layers.

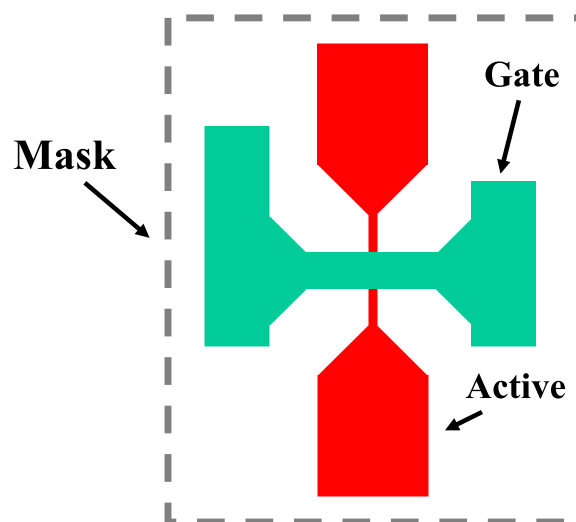


**Figure 2.2** Schematics of mask layout showing the active, gate and mask layers.

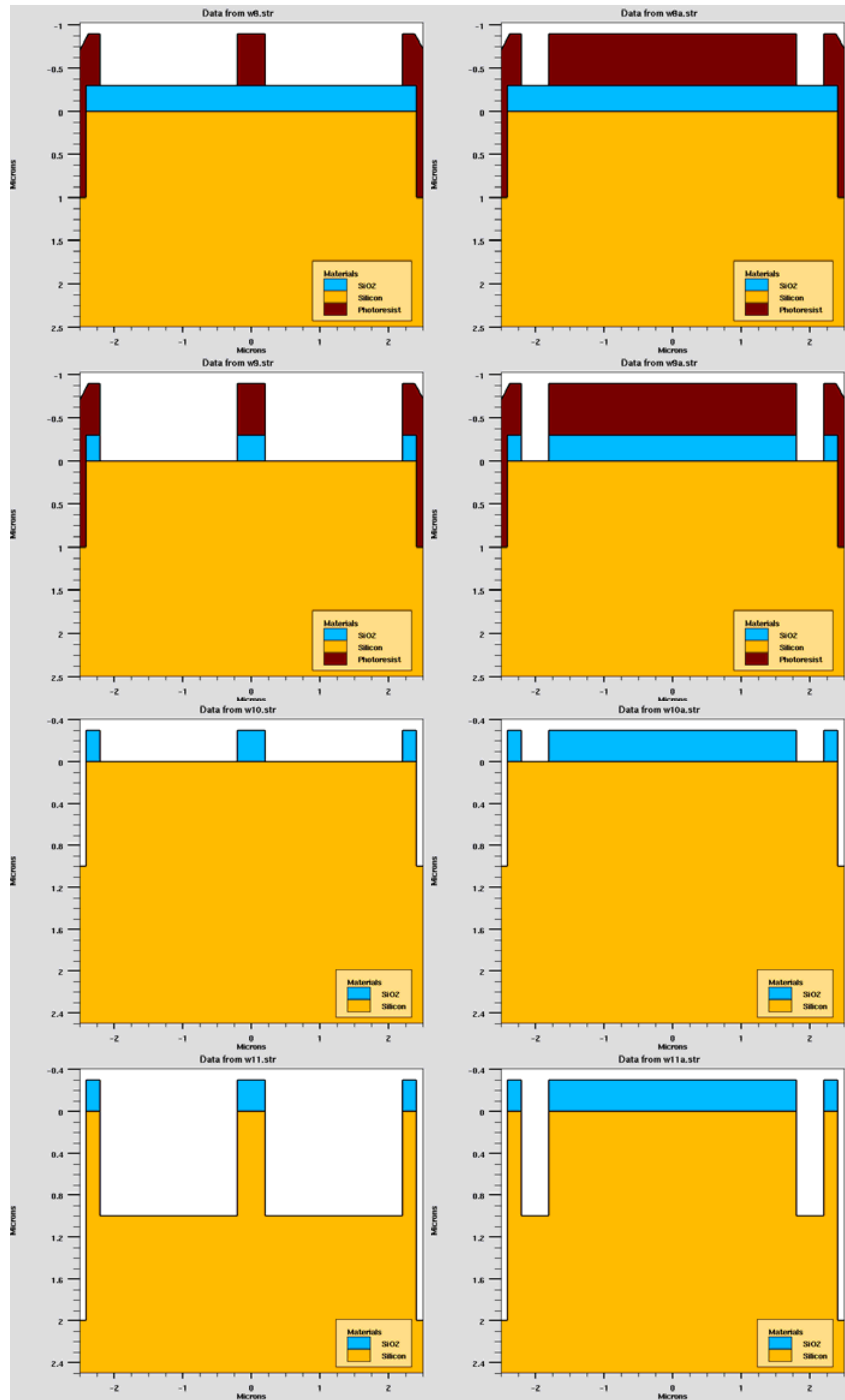


**Figure 2.3** Cross section view along the width (left) and length of the device (right) after resist spin, lithography, mask oxide etch in RIE and active area RIE.

The exposure step is repeated with a higher dose using an additional mask called 'mask layer' which has rectangular areas covering the active areas of the devices (Figure 2.2). This results in over exposure of the areas away from the devices ensuring a clean surface left behind between the devices.

The alignment marks are protected in the 'active' and 'mask' level masks. This leaves the oxide around the alignment marks intact during the oxide etch step as illustrated in Figure 2.3. After the removal of the photoresist layer the alignment marks are again uncovered and they are etched down further, during the active area Si etch. The trenches are etched down 1 μm, leaving the alignment marks approximately 2 μm deep. Repeated trials showed that there is not any noticeable advantage in the alignment process if the alignment marks are deeper than 1.4 μm. The depth of the alignment marks will be reduced by approximately 0.3 μm after the chemical mechanical polishing (CMP) step performed in a later step, leaving the alignment marks approximately 1.7 μm deep.

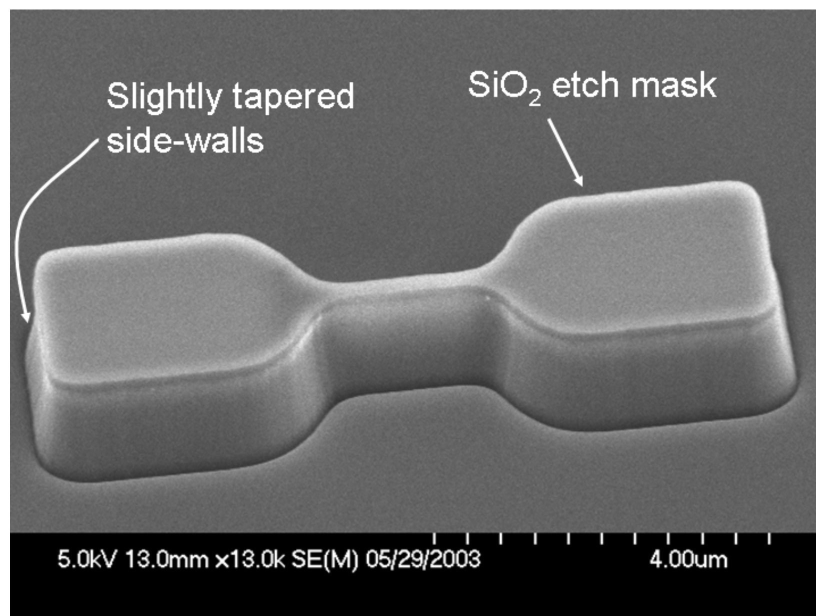


**Figure 2.4** SEM micrograph of the active area, imaged at 45° tilt. The ripple visible on the sidewalls are significantly reduced as the device is sized down through oxidation during the process sequence for dopant enhancement and width sizing.

The RIE process using oxide etch mask and $Cl_2/BCl_3$ chemistry results in fairly vertical sidewalls with some tapering at the bottom part of the device (Figure 2.4). This tapering helps the structural integrity of the active areas during the subsequent oxidation and wet etch processes to make the ultra-narrow channel devices but results in increased device width if the wafers are over-polished in the subsequent CMP step.

### 2.2.3 Substrate dopant enhancement

After the active area definition the wafers are oxidized in $H_2O$ / $N_2$ ambient at 800 C and oxide is removed in diluted HF solution in order to clean the sidewalls of the etched structures. A thin oxide is then grown on the surface and the wafers are implanted with boron at 100 keV with 5 x $10^{13}$ $cm^{-2}$ dose, expected to result in a peak concentration of $3x10^{17}$ $cm^{-3}$ at 0.5 μm below the surface. A 350 nm layer of $p^+$ doped polysilicon is deposited on the wafers at 600 C (Figure 2.5). Wafers are then oxidized,

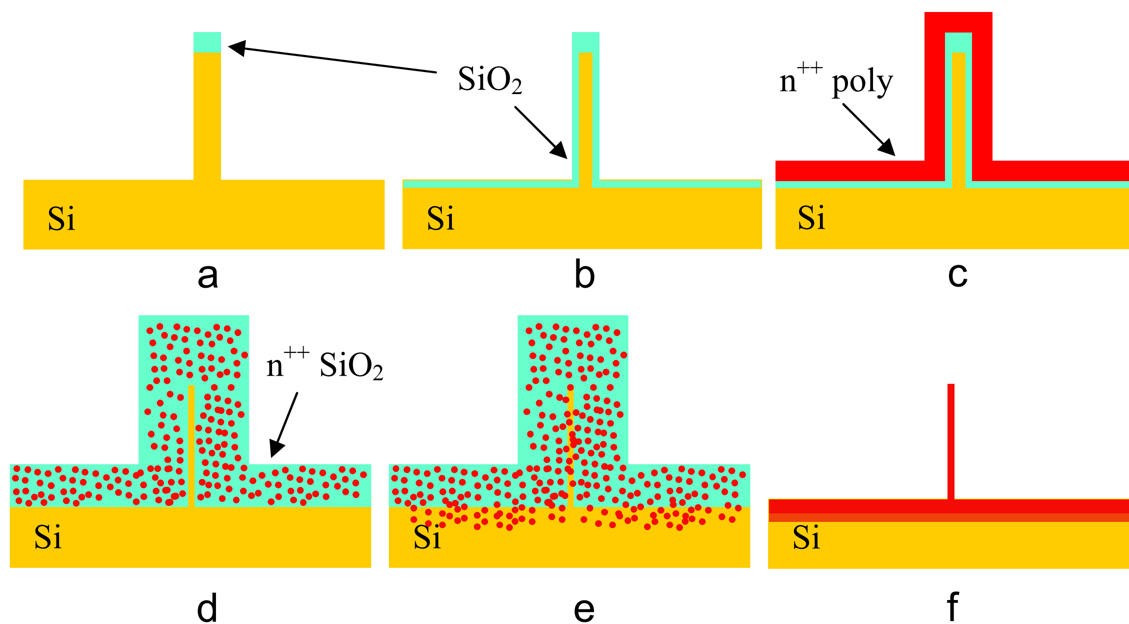


**Figure 2.5** Cross sectional schematics showing the processes to enhance the body doping and sizing down the device width. Active area RIE (a), thermal oxide growth (b), doped polysilicon deposition (c), oxidation of doped polysilicon and active Si (d), dopant diffusion (e) and removal of oxide resulting in doped interfaces with reduced channel width (f).

depleting the deposited polysilicon and consuming approximately 0.1 µm of the single crystal Si. This oxidation process results in a highly boron doped oxide layer conformally covering the Si active structures, which are now approximately 0.2 µm narrower. The dopants are driven into the Si surface by annealing at 900 C. The oxide film is then removed in diluted HF.

### 2.2.4 Shallow trench isolation

Silicon nitride is used as dielectric material for device isolation. Low pressure chemical vapor deposited (LPCVD) stochiometric silicon nitride films, deposited at 850 C are measured to be good electrical insulators. However, it is not possible to deposit stochiometric $Si_3N_4$ thicker than approximately 200 nm due to thermal expansion coefficient mismatch with Si. Si-rich SiN can be deposited up to more than 1 µm in thickness, without serious stress problems. Si-rich SiN, however, is not a very

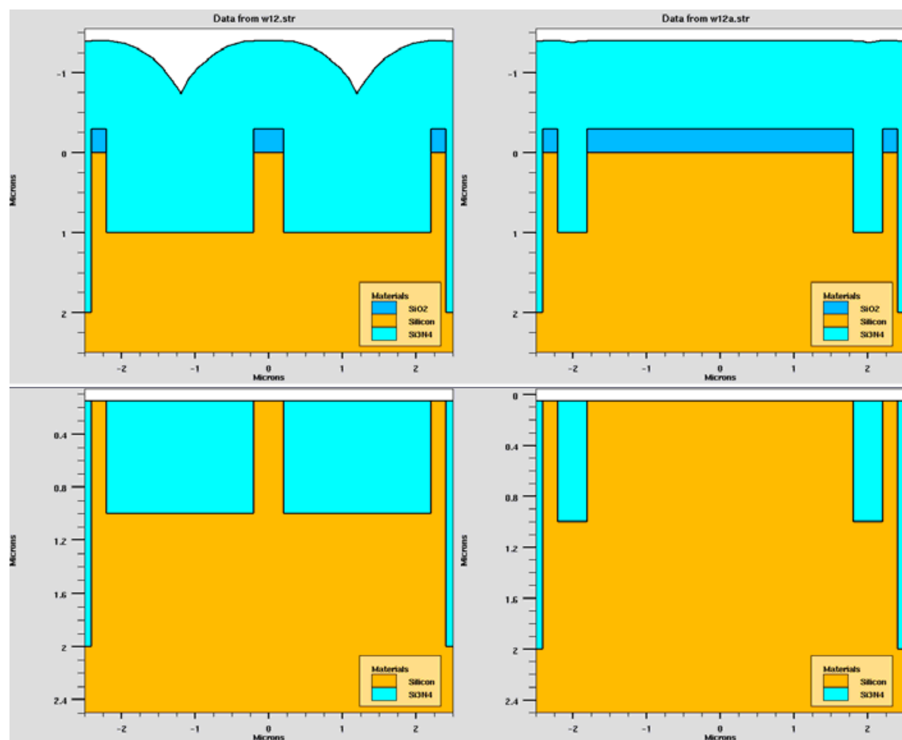


**Figure 2.6** Cross sectional schematics after silicon nitride deposition (top) and planarization (bottom)

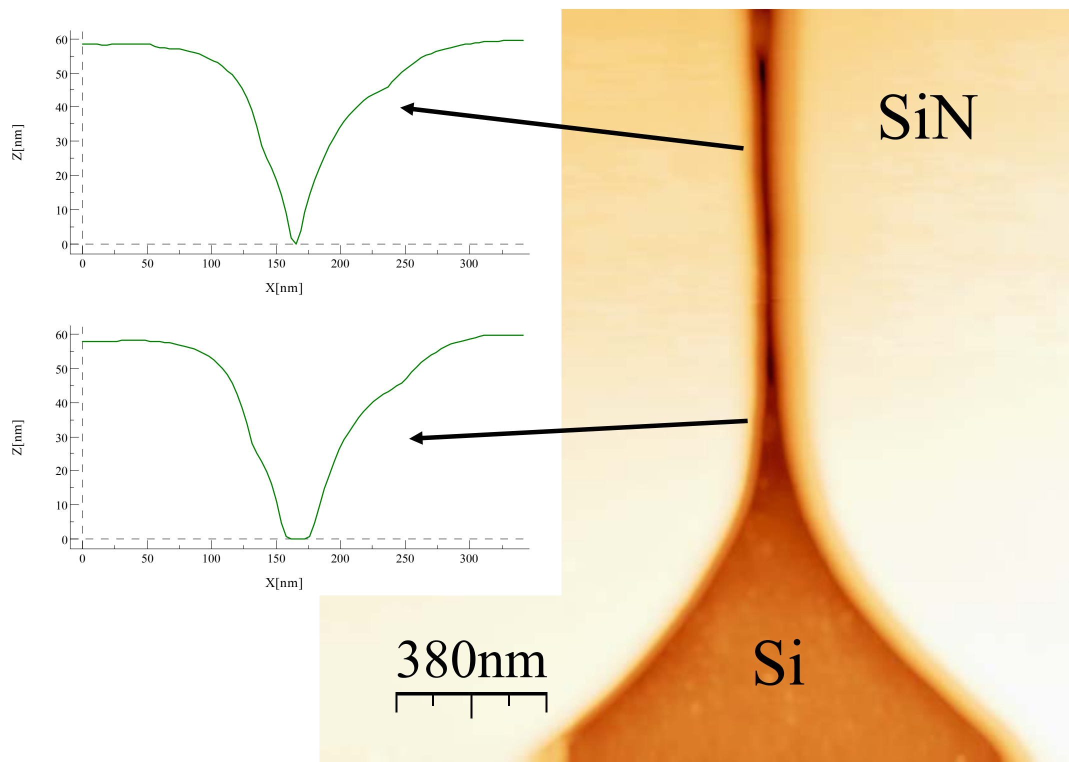


**Figure 2.7** AFM image of an ultra-narrow channel transistor (right) and two cross sections (left). The silicon surfaces are recessed below the nitride field by approximately 60 nm. The measurable width in the narrow region is limited by the AFM tip (~10 nm) [35].

good electrical insulator, resulting in significant leakage currents. In order to overcome the mechanical stress and electrical leakage problems, a 20 nm layer of stochiometric nitride is deposited for electrical isolation and a 1 μm layer of low stress nitride is deposited as the filling material (Figure 2.6). The deposited films are annealed at 1000 C.

One level of photolithography, using a contact aligner, is performed to expose the areas between the dies. A contact mask covering the die areas is used for this step. Silicon nitride between the dies is etched stopping on the Si surface, using $CHF_3/O_2$ RIE. This step, isolating the nitride in the die areas, removes the continuous lines of thrust formed by large area film on the front surface of the wafer between the dies. If the nitride film between the dies is not removed from the front surface of the wafer,

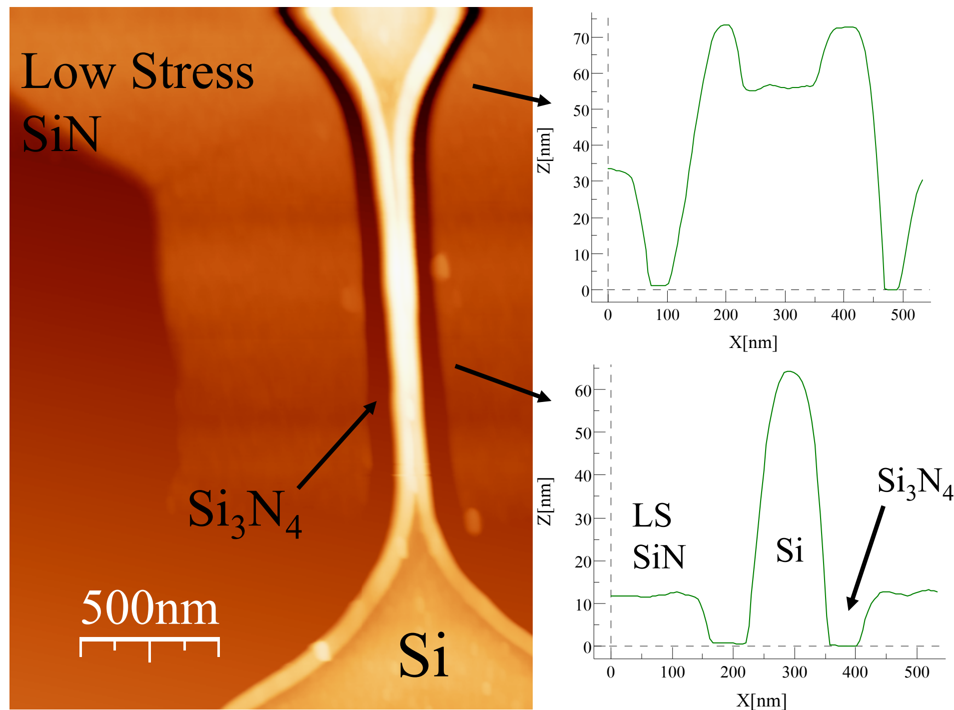


**Figure 2.8** AFM image of an over-polished active area. The edges of the Si active form rims around the recessed planar areas. The surface is imaged after recessing the field nitride through 21 min. of HF etch. $Si_3N_4$ areas are recessed more than the silicon rich silicon nitride field [35].

wafers have significant bow towards the front surface after the removal of the nitride film from the back-side of the wafers. Removal of films from the back-side is necessary to make electrical contact to the substrate. High levels of wafer bow would result in difficulties in the remaining processing steps.

After the RIE step, wafers are planarized using CMP, with a hard pad and oxide slurry (Figure 2.6). The etch rate of SiN is slower compared to that of both $SiO_2$ and Si. The CMP process is stopped as the Si surfaces of the active areas are exposed (Figure 2.7). Over-polishing results in increased device width due to tapering. It also results in a topographical change over the surface where large openings of Si surfaces continue to etch down but the Si areas close to the edges remain at a higher level (Figure 2.8).

After the CMP process the wafer surfaces are cleaned using either a sponge with IPA and DI water or using the automated Hamatech wafer cleaning tool. Wafers then go through an RCA clean with short diluted HF dip and a thin cleaning oxide is grown on the surfaces. The thin cleaning oxide is then removed from the surfaces after the RCA clean preceding the gate stack deposition.

### 2.2.5 Gate stack deposition and definition

$SiO_2$ is used as sacrificial material to form the tunnels passing under the gate of the transistor. I have realized that if the sacrificial $SiO_2$ is prematurely removed from underneath the gates on the edges in the consecutive steps, there is electrical leakage from the gates of the structures to the active areas. In order to prevent this and increase the process reliability a 10-20 nm layer of LPCVD $Si_3N_4$ is deposited over the

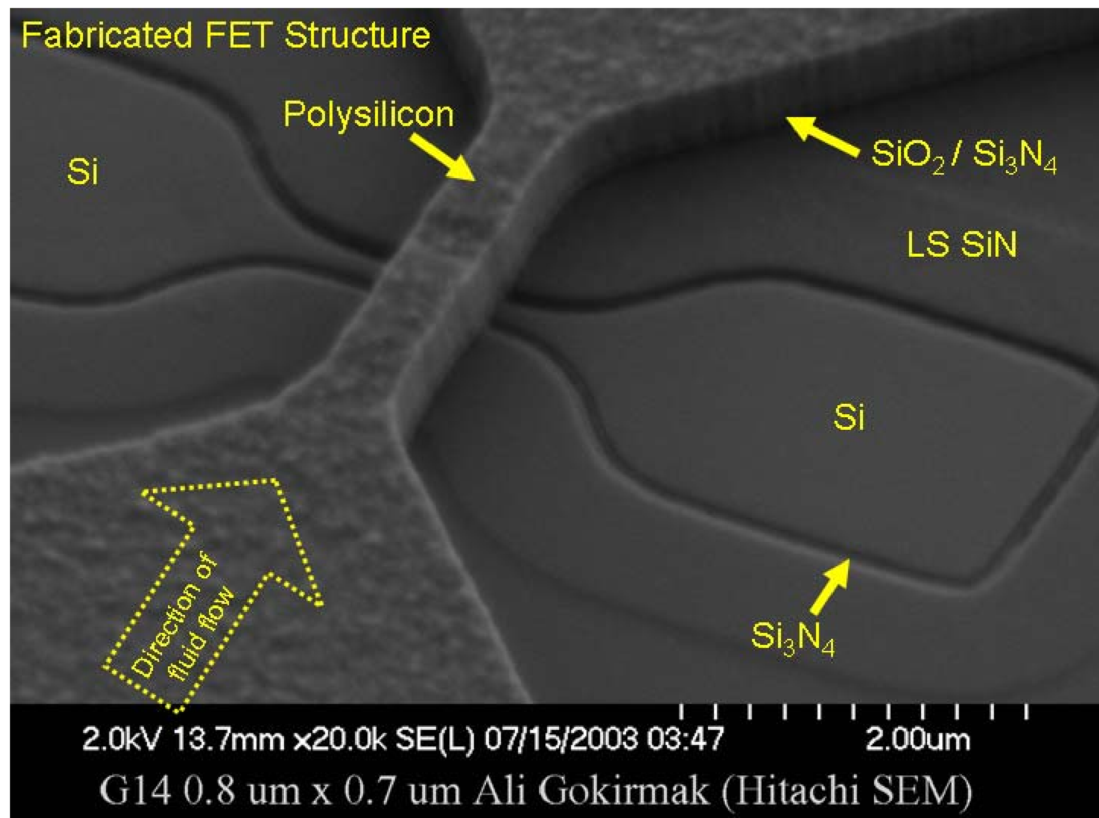


**Figure 2.9** SEM image of the FET structure after gate stack definition and etch

sacrificial $SiO_2$ in the gate stack. During the sacrificial oxide removal some of the $Si_3N_4$ is also removed. The remaining $Si_3N_4$ serves as an electrical insulation layer underneath the gate of the transistor cutting down the electrical leakage and electrolysis of the water during the sensor operation. A 350 nm thick $n^+$ doped polysilicon is deposited at 600 C as the gate material and a 150 nm PECVD oxide layer is deposited over the gate stack to be used as hard mask for the gate etch.

Photolithography is carried out as described for the active layer, this time using the 'gate' and 'mask' level masks. The areas between the dies are exposed using contact lithography using the same contact mask as described earlier. Wafers are chemically developed. The $SiO_2$ etch and Si etch processes are carried out as described in section 2.2.1.

The rows of dies are separated by 3 mm wide empty strips. These plain areas are wide enough for interferometric and ellipsometric measurements of film thicknesses at different locations on the wafer. Interferometric and ellipsometric measurements on these locations are performed for etch and deposition thickness monitoring.

The mask oxide layer and the polysilicon layer are etched using RIE as described in section 2.2.1. The etch time in $Cl_2/BCl_3$ RIE system for polysilicon etch is kept long enough to etch down the underlying nitride layer and stopping on the oxide film.

### 2.2.6 Self-aligned source/drain implantation

A thin layer of oxide is grown on the sidewalls of the defined gate structure consuming the etch damaged areas on the edges and forming a thin spacer for self-aligned implantation. The oxidation time and temperature is set for 7-8 nm oxidation

of 100 plane of single crystal silicon. The oxide forming on the sidewalls of the highly doped poly silicon gate structure is expected to be 3-4 nm thicker.

Wafers are implanted with arsenic at 1 to 5 $x10^{14}$ $cm^{-2}$ at 20 keV with 90° rotation and 8° tilt. This is the only source/drain implantation used in the fabrication process in order to minimize the process complexity. Activation of the dopants is achieved through annealing during the subsequent nitride deposition steps.

### 2.2.7 Silicon nitride sidewall deposition

Silicon nitride sidewalls are used to seal the sides of the tunnels which will be formed under the gates of the structures, and hold up the ceiling of the tunnels formed by the polysilicon gate structure.

The oxide on the exposed surfaces is removed in diluted HF. The wafers are kept in HF solution slightly longer in order to etch approximately 20 nm more to ensure that there is no oxide left on the surfaces and to slightly undercut the gate-stack on the edges. LPCVD $Si_3N_4$ and Si rich SiN films are deposited over the structure at 800 – 850 C.

### 2.2.8 Removal of sacrificial oxide

In the case of back-end-integration of tunnels for sample delivery into the FETs, trenches are etched down from the two ends of the gate structure using $CHF_3/O_2$ RIE in order to bring the sample in and take it out. As these trenches are etched into the substrate, overlapping with the two ends of the gate structure, the SiN sidewalls are also etched away, exposing the sacrificial oxide in the gate stack (Figure 3.3).

The wafers are kept in 49% HF solution for 7 minutes in order to remove the sacrificial oxide. This process is initially tested using a thicker layer of sacrificial oxide and gate structures made of SiN. In this case, since the gap between the gate and

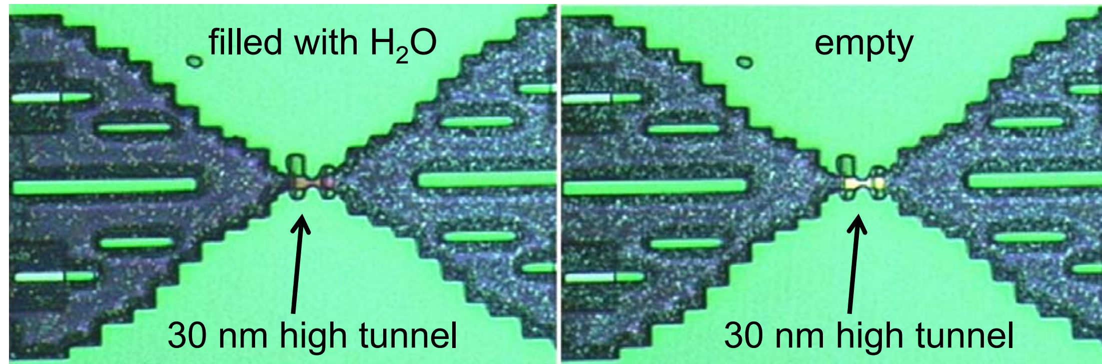


**Figure 2.10** Optical microscope images of shallow test tunnels made out of silicon nitride with (left) and without (right) water. Shallow tunnel height is approximately 30 nm and are attached to larger delivery tunnels.

the wafer surface is thicker and $Si_3N_4$ is transparent, it is possible to see the color change as water penetrates underneath the gate (Figure 2.10).

### 2.2.9 Monolithic integration of the delivery tunnels

It is possible to integrate the sample delivery tunnels using monolithic integration or back-end-of-line integration techniques. The back-end-of-line integration of the tunnels is explained in chapter 3. Monolithic integration of the tunnels, which is explained in this section, was found to be a more reliable process.

Monolithic integration of the tunnels is carried out by depositing sacrificial oxide and patterning tunnel structures prior to nitride side-wall deposition, explained in section 2.2.7.

#### 2.2.9.1 Sacrificial oxide definition

Two different tunnel structures are defined: one for fluid delivery which is 3 μm wide and a second tunnel structure for irrigation purposes which is < 1 μm wide. The final fluid delivery tunnel height is approximately 0.5 μm and the final height of the irrigation tunnels is approximately 0.3 μm (Figure 2.11).

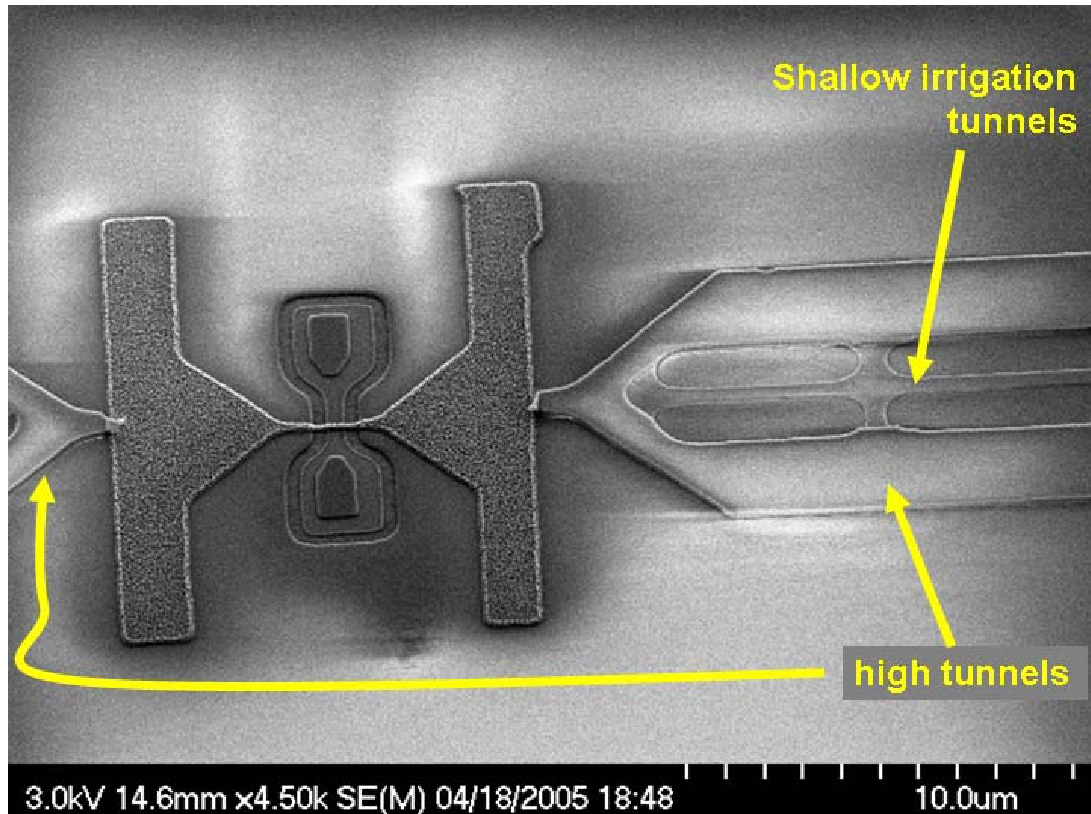


**Figure 2.11** SEM image of a patterned sacrificial oxide leading to an FET structure. The oxide layer for delivery tunnels is higher than the shallow tunnels which will be used for irrigation.

A 300 nm thick $SiO_2$ film is deposited at 400 C in a PECVD system to be used as the sacrificial material for the tunnel structures. Photolithography is carried out as described in section 2.2.1 using a mask layer which defines the wider fluid delivery tunnels. This time, the wafers are exposed to $NH_3$ ambient after the exposure for image reversal. $NH_3$ diffuses into the photoresist neutralizing the acid produced in the photoresist by the UV exposure, making those areas insoluble during chemical development. After $NH_3$ image reversal, wafers are flood exposed and developed leaving resist on the areas which were exposed initially. At the end of this sequence there is no resist left between the dies and the oxide etch can be monitored through interferometric measurements.

After chemically developing the resist and oxygen plasma descum, oxide is etched in 6:1 buffered oxide etch (BOE). The etch is monitored by interferometric measurements after short-time etches. The etch process is timed to leave 50 nm of the oxide on the wafers. The resist is removed using acetone and IPA and the surfaces are re-primed using vapor phase HMDS.

Photolithography for the second layer of tunnels is carried out in the same manner as for the first tunnels. The oxide structures are again etched in 6:1 BOE, this time slightly over etching to make sure that there is no oxide left on the sidewalls of the gate structures (Figure 2.11). After this step, silicon nitride films are deposited as described in section 2.2.7.

#### 2.2.9.2 Irrigation holes and vias for metal contacts

A photolithography step is carried out using a mask made for irrigation holes. These irrigation holes, 1 μm x 1 μm in size, are opened on the irrigation tunnels using $CHF_3/O_2$ RIE process.

After the removal of photoresist in $O_2$ plasma, photolithography and etch steps are repeated for the 'via' level in order to open the contact areas of the source/drain and the gate of the FET. The etching of the vias is stopped when the SiN film is thinned down to 20-50 nm. The remaining nitride will be removed in 49% HF solution during the sacrificial oxide removal step, ensuring a proper etch stop on the Si surface.

Stopping RIE process before reaching the Si surface prevents the etching of the silicon surface which would lead to etching through the shallow source/drain diodes formed on bulk silicon. The RIE process should be stopped at a point ensuring that none of the devices on the whole of the wafer will be over etched, despite the center to edge variations in the deposition and RIE processes. The nitride thicknesses at different spots on the wafer should be measured by interrupting the RIE process in

order to accurately determine when to finish the RIE process. Etch times should be adjusted so that minimum etch time is at least 45 s – 1 min. in order to minimize the errors due to changes in the etch rates in the chamber during the first several seconds of the RIE process.

#### 2.2.9.3 Removal of sacrificial oxide

The sacrificial oxide is removed from the tunnels and underneath the gate structure using 49% HF solution in approximately 7-10 minutes (Figure 2.12). The sacrificial oxide underneath the gate of the FET and the tunnels form a continuum,

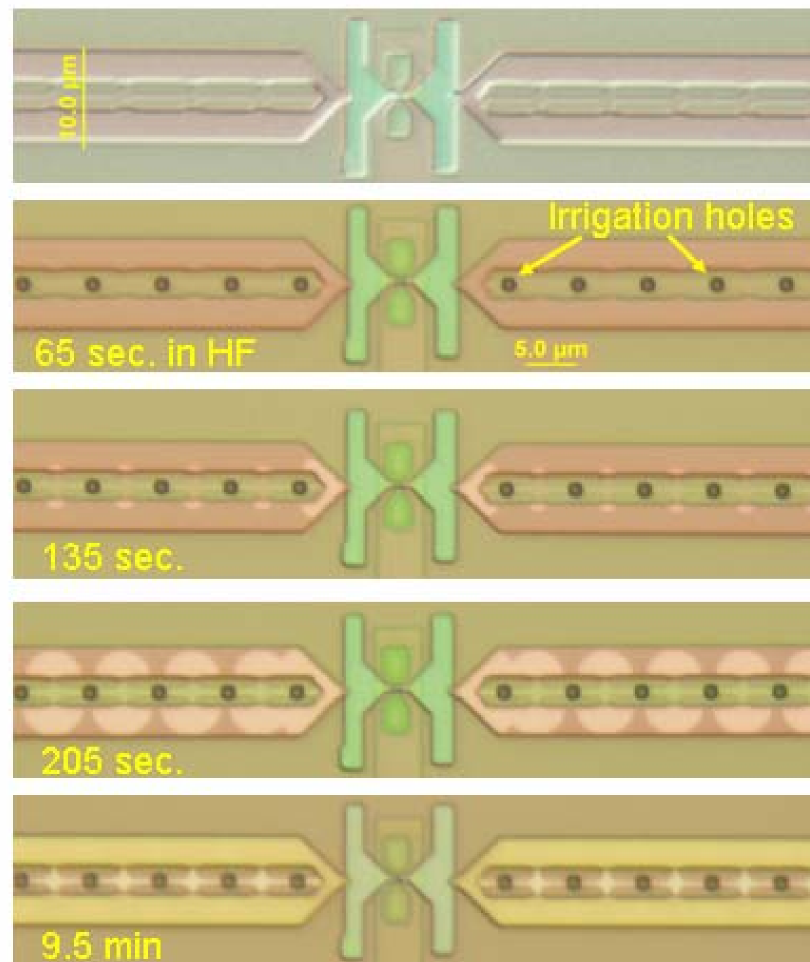


**Figure 2.12** Optical images depicting the sequence of sacrificial oxide removal from the sample delivery tunnels

assuring the continuity of the tunnels after the etch process. The thin nitride layer left over the vias is also removed by HF in the mean time, exposing the silicon surfaces of the source/drain and the gate contact areas. This wet etch process rounds the corners of the vias which helps ensure the continuity of the metal lines deposited using metal evaporation and lift-off process.

### 2.2.10 Gate oxide regrowth

After the removal of the sacrificial oxide, a 2 - 4 nm layer of oxide is thermally grown in $O_2/N_2$ ambience. This oxide layer is intended to be a low defect density oxide covering the active areas of the device in order to improve the device performance, and reduce the current leakage into the liquid sample and avoid possible problems which might be caused by electrolysis of water inside the devices.

### 2.2.11 Metallization

The metal contacts to the FETs are defined by using a bi-layer resist lift-off process. A 1 µm thick light-insensitive resist layer is spun on the wafers and baked at 160 C. A second layer of photoresist is spun to be 1.2 µm in thickness. Photolithography steps are repeated as in the previous steps. This time, the wafers are developed for an additional 30 s to remove the underlying light-insensitive resist layer (Figure 2.13). This process results in resist overhang all around the structures, ensuring successful lift-off of metals evaporated as thick as 0.8 µm.

Wafers are descumed in oxygen plasma and the oxide that forms on the contact

**Figure 2.13** Schematics of metal lift-off process using a bi-layer resist process

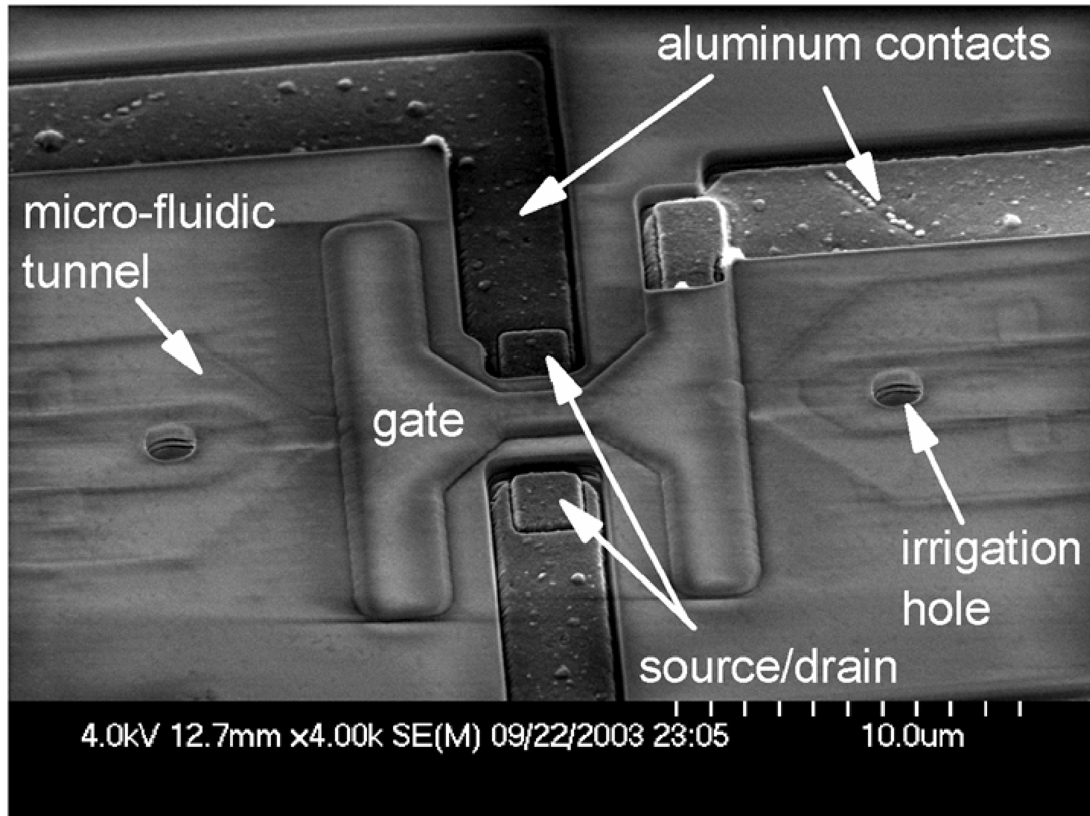


**Figure 2.14** SEM image of the FET structure integrated with micro-fluidic delivery tunnels after metallization.

areas is removed in 30:1 BOE, immediately before loading into the evaporation chamber. A 250 nm layer of Ti and 600 nm of Al is evaporated. Metal lift-off is performed in resist removing solvent over several hours (Figure 2.14).

The Ti layer deposited underneath the Al metal acts as a diffusion barrier, preventing pure Al alloying with Si during the subsequent anneal steps and spiking into the Si surface. With the use of Ti layer, it is possible to anneal the samples in forming gas at temperatures above 400 C without any problems due to Al spiking.

Al spiking can be observed up to 2 μm into silicon surface if pure Al is used to contact the Si surface. This problem can also be solved by using 2% Si mixed into Al which can be deposited in a sputtering system. This process adds significant amount of complexity to the process flow and may require integration of electrostatic discharge

(ESD) structures into the design in order to prevent shorting of the devices due to charge build up during the metal deposition and etch steps. Due to these problems, this alternative process is avoided.

### 2.2.12 Substrate contact

After the completion of the processing of the structures, the films on the back side of the wafer are removed using RIE while the front surface is protected by photoresist. The back side of the wafer is then polished using CMP. A polished surface on the back side of the wafer allows interferometric measurements on the back surface in order to ensure that there are no films left on the back side prior to back-side metallization. The polishing step can be performed earlier in the process, in which case, the deposited films have to be removed before the backside metallization step.

After the films on the back-side of the wafers are removed, a stack of Ti & Al metal films are evaporated on the back surface.

As a final step the wafers are annealed at 400 C in 5% $H_2$ in Ar for 15 min. in order to reduce the contact resistance and minimize the contribution of interface defects in device performance.

## 2.3 Testing

### 2.3.1 Structural testing

The structure is tested by placing a droplet of DI water on the irrigation system which is driven into the tunnels by capillary forces. The parts of the larger tunnels filled with water have a different color compared to the empty sections (Figure 2.15).

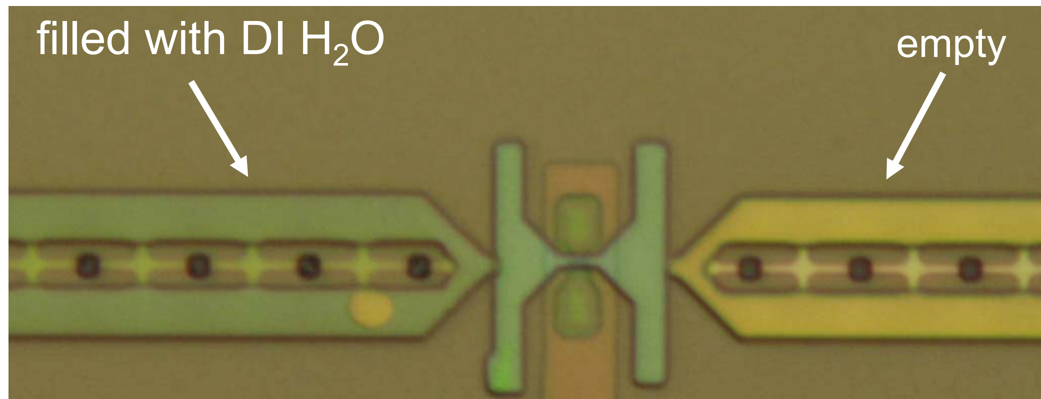


**Figure 2.15** Optical image of a device structure with microfluidic delivery system. The DI water is applied onto the tunnels a few mm left of the device.

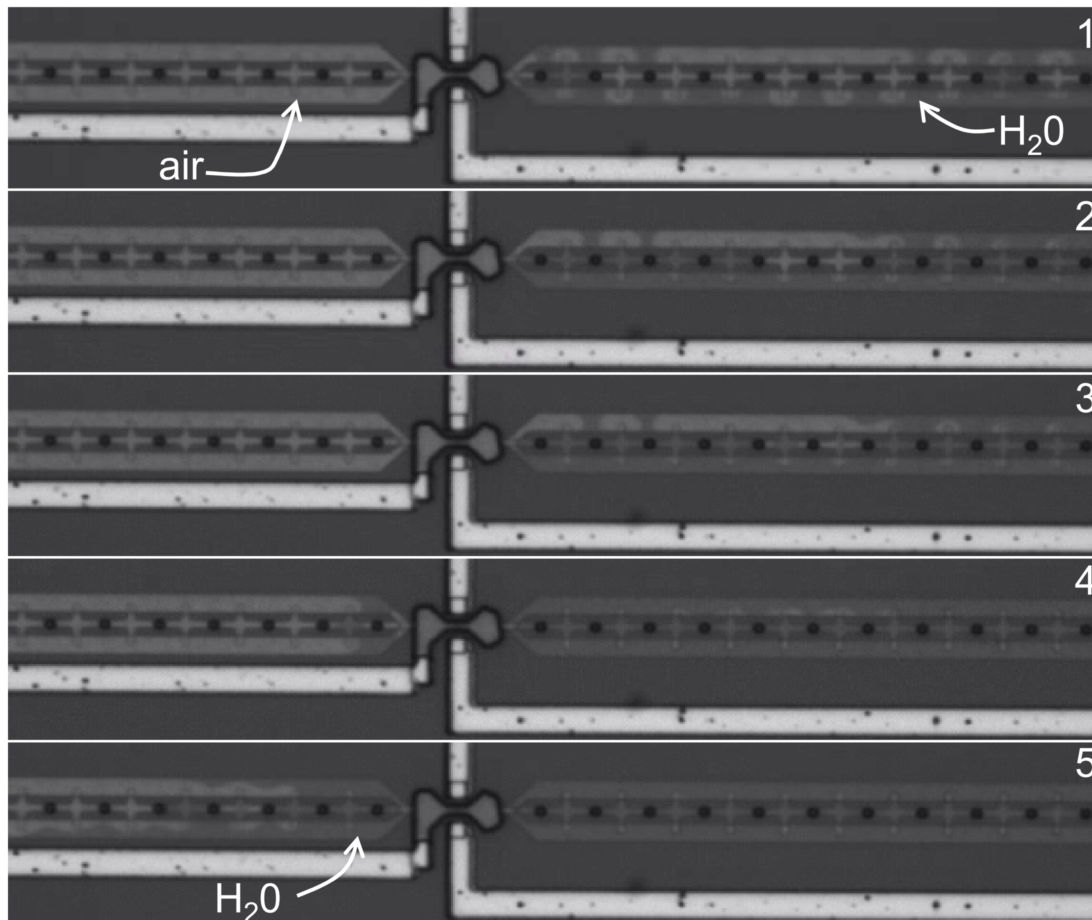


**Figure 2.16** Optical snap-shots of a device structure with microfluidic delivery system after application of a droplet of DI water on the tunnel system a few mm away from the device on the right side.

Although it is not possible to see any color change in the shallow tunnels due to the penetration of water, the continuity of the tunnels is confirmed by observing the water going into the device and come out from the other side (Figure 2.16). The opening under the gate of the transistor is approximately 6 nm high. Figure 2.16 is constructed by extracting frames of a movie recorded as a drop of DI water is applied to the tunnel system from the right side of the device. The parts of the tunnels filled with water look darker than the empty sections.

### 2.3.2 Electrical testing

The I-V characteristics of the narrow channel devices are tested using an HP 4145B parameter analyzer. The transistors' transfer characteristics change as a drop of water is supplied to the irrigation system and the water enters between the channel and the gate of the transistor (Figure 2.17). The changes are expected to be due to the

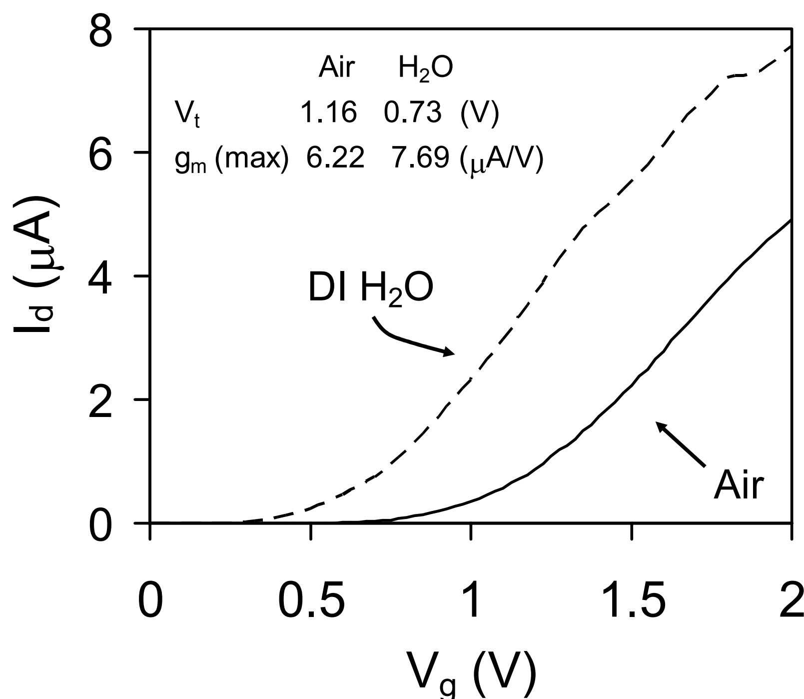


**Figure 2.17** Transfer characteristics with Air and DI water in linear scale.

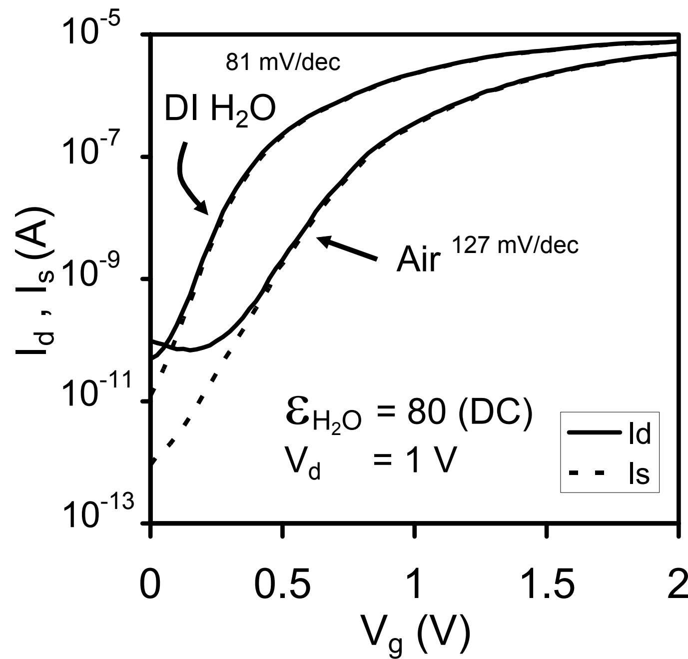


**Figure 2.18** Transfer characteristics of a narrow channel FET with air gap and with DI water filled into the tunnel between the gate and the channel. DI water is applied on the delivery tunnel system and the capillary forces drive DI water into the FET resulting in significant change in the device characteristics.

changes in the capacitance of the gate dielectric and the changes in the interface charge density. The dielectric constant of water is 80 at small DC field.

As the water enters the tunnels, the threshold voltage reduces by 0.46 V (from 1.19 V to 0.73 V) and transconductance improves by approximately 20 %, from 6.45 μA/V to 7.69 μA/V (Figure 2.17). The subthreshold slope improves from approximately 127 mV/dec. to 81 mV/dec (Figure 2.18).

If the transistor is assumed to be behaving as a wide and long channel device, it is possible to estimate the oxide thickness grown on the bottom surface of the doped polysilicon gate and the single crystal silicon channel surface using subthreshold slope for the two different cases. The oxidation rate of the doped polysilicon is expected to be approximately twice the single crystal silicon.

The subthreshold slope for a long channel FET is approximately given by [21]:

$$SS = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}(1+\frac{C_{dm}}{C_{ox}})$$

At room temperature kT/q = 26 mV, hence the constant term is approximately 60 mV/dec. $C_{dm}$ is the depletion layer capacitance and $C_{ox}$ is the capacitance of the gate dielectric [21]. The expressions for the two cases then become:

$$SS_{H_2O} = 60mV/dec(1+\frac{C_{dm}}{C_{H_2O}})$$

$$SS_{air} = 60mV/dec(1+\frac{C_{dm}}{C_{air}})$$

The oxidation process is expected to consume silicon by approximately 40% of the oxide thickness resulting in a thickness reduction in the air-gap by 60 % of the total grown oxide. The air-gap thickness is expected to be 11 nm prior to oxidation process, hence: 0.6 $t_{ox}$ + $t_{air}$ = 11 nm. By taking the ratio of the subthreshold slope expressions and plugging into the thickness relation, the air-gap height and the total oxide thicknesses are calculated to be; $t_{air}$ = 5.4 nm and $t_{ox}$ = 9.3 nm. The oxide is expected to be grown approximately 3.1 nm on the channel surface and 6.2 nm on the bottom surface of the polysilicon gate [36]. This is within the thin oxide thickness range expected from the oxide growth process.

The depletion depth in the channel region is calculated to be 82 nm using these values, which corresponds to a channel doping density of 1.65 x $10^{17}$ $cm^{-3}$. However the threshold voltage shift is expected to be approximately 1.3 V for this substrate dopant density, from the theoretical calculation, while the experimental value is approximately 0.4 V. The change in the transconductance is 23.6 %. This change is expected to be by a factor of 3, assuming that the carrier mobilities do not degrade for the case with water.

Some of this discrepancy may be attributed to the large contact resistances of the device. Large source and drain contact resistances result in a drop in actual $V_{ds}$ across the intrinsic device and large source resistance results in negative feedback, degrading the observed transconductance. The contact resistances of this ultra-narrow channel device may be larger than 50 kΩ. A second possible reason may be permittivity of water in a tunnel of 5 nm in height being different than that of bulk case. This may be possible due to water dipole – $SiO_2$ surface interactions in this length scale. This interaction may be restricting the response of the water molecules to electric field resulting in an effectively lower permittivity. Another possible reason is the dielectric constant in the tunnels being higher than air due to possible moisture build up on the surfaces prior to the application of DI water into the tunnels.

## 2.4 Sensitivity

The expected sensitivity for the tested transistor structure can be estimated using the extracted device parameters. In this particular case the highest FET sensitivity can be achieved for approximately $V_g$ = 0.25 V, corresponding to 81mV/dec. For this bias condition, if a DNA sample were to be applied to the system, the molecule would be attracted to the gate surface due to the net negative charge on the backbone of the single strand DNA molecule. The tags attached to the single strand DNA would be facing the channel surface, hence the fixed negative charges on the tag nucleotides would be approximately 2 nm offset from the ceiling of the tunnel (Figure 2.19)

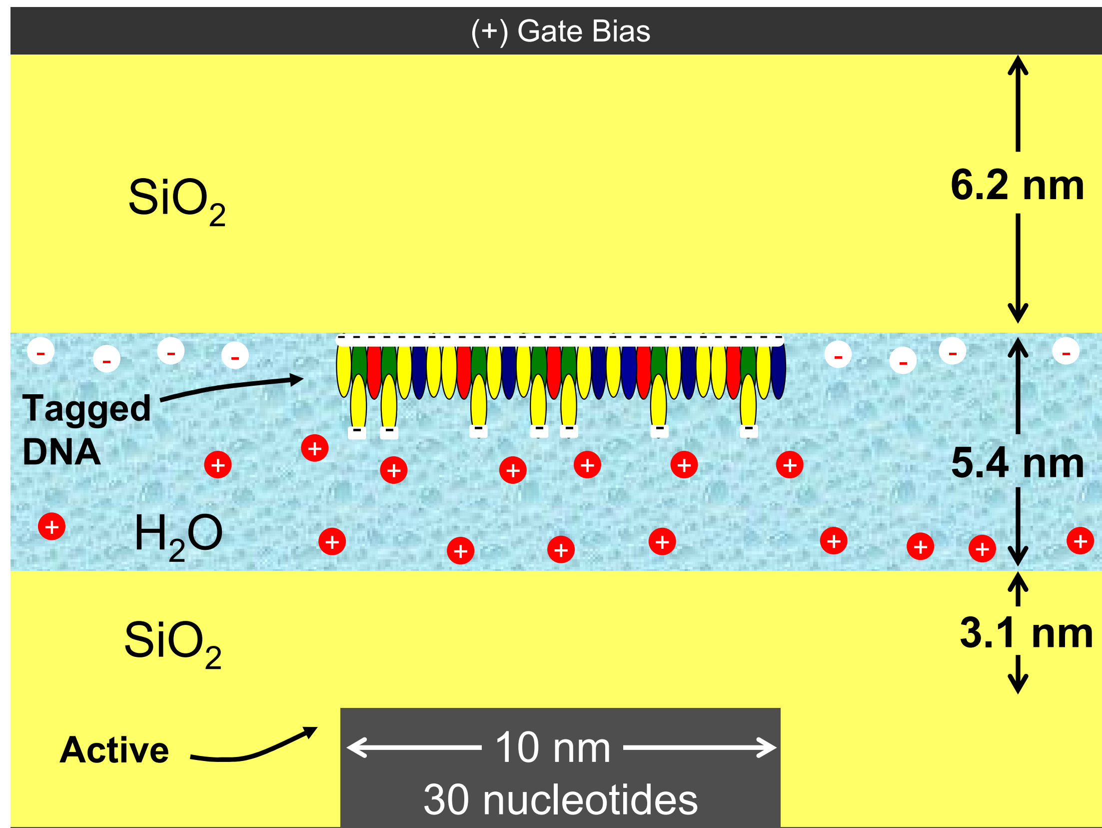


**Figure 2.19** Schematics of the device structure and DNA molecule drawn to scale for the estimated device dimensions.

If the current limiting section of the transistor is assumed to be 10 nm long, and the perturbation from a single charge is assumed to be a uniform charge distribution over 10 nm x 10 nm area, the problem can be simplified to 1D in order to calculate the range of expected sensitivity. By making this assumption, the effect of the fixed charge can be calculated from the Gauss's Law as the electric potential needed to counter the affect of the charge [21] (Figure 2.20):

$$\delta V_g = -\frac{xQ}{\varepsilon_{ox}}$$

Using this relation, it is possible to calculate the threshold voltage change due to dipoles passing between the gate and the channel where $Q = 1e^{-}/\ 100\ nm^2$ for each

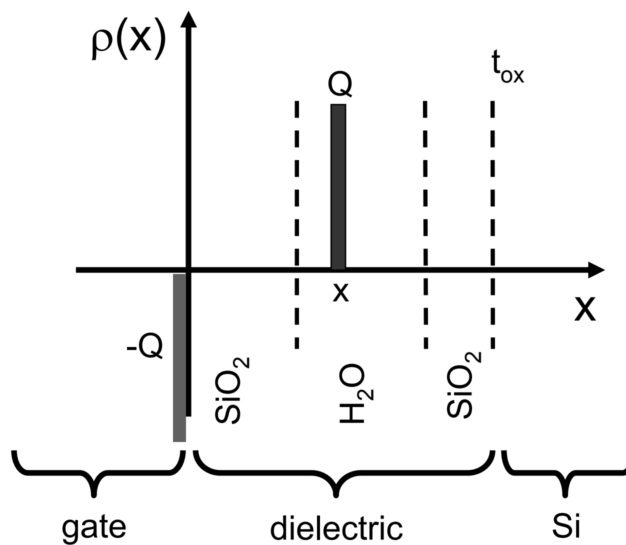


**Figure 2.20** Schematics of charge distribution in an FET gate stack. Q is the additional fixed charge density due to the molecules in the solution.

charge. If the perturbation due to a single nucleotide is a dipole of $1e^-$ charge attached to the DNA molecule and a single + ionic charge shielding the nucleotide, the threshold voltage shift will be the sum of the contributions due the two charges forming the dipole. The dielectric between the gate and the dipole consists of approximately 2 nm of $H_2O$ with $\varepsilon_{H20} = 80$ and 6.2 nm of $SiO_2$ with $\varepsilon_{SiO2} = 3.9$ for the negative charge on the tag. The perturbation for the negative charge on the tag is $\delta V_{g1} = 0.29$ V, and the perturbation due to the positive charge forming the dipole in the solution is plotted as a function of the location of the single positive ionic charge in the vicinity of the nucleotide within the tunnel (Figure 2.21). If the shielding ionic charge is 0.5 nm away from the negative charge the net change in the threshold voltage is approximately 1.3 mV. The current level in the higher end of the subthreshold regime is approximately 100 nA as seen in Figure 2.18.

The expected percentage change in the current level for 100 nA drive current can be estimated from Figure 1.7. The expected change in the current level is in the order of 5 nA if the positive ion is 0.5 nm away from the ceiling of the tunnel and the

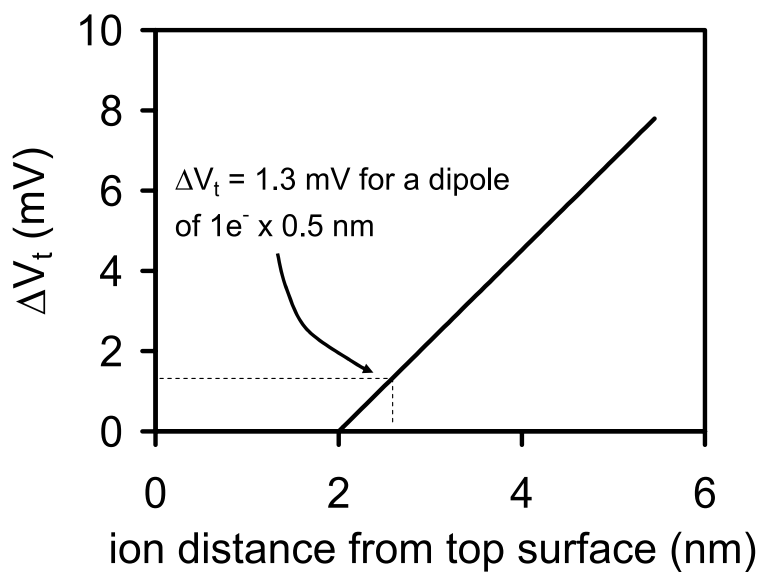


**Figure 2.21** Expected change in the threshold voltage as a function of distance of the shielding ionic charge in the solution.-1e$^-$ ionic charge is taken to be screening +1e$^-$ charge on the tag.

DNA molecule is at the ceiling as illustrated in Figure 2.19. Due to the high dielectric constant of water, the electrical sensitivity of the device to the DNA molecule would not be noticeably different if the device was operated with a negative gate bias and the DNA molecule is pushed against the electron channel for the given device dimensions, keeping the assumption of uniform charge distribution over 10 nm x 10 nm area in mind. This configuration, however, would improve the spatial resolution of the sensor.

## 2.5 Conclusion

Fabrication processes for sub-10 nm width air-gap field effect transistors monolithically integrated with microfluidic delivery system are developed. The devices show good transistor characteristics with and without application of DI water into the system.

The channel width can be fabricated to be less than 10 nm by sizing down the Si channel through oxidation. The effective channel width can be further reduced

using side-gates to achieve electron confinement down to less than 5 nm. The tunnel passing between the gate and the channel of the transistor can be reliably fabricated down to 5 nm and smaller in height. The electrical biases applied to the transistor terminals will determine the orientation of the DNA molecule and ionic charges as well as the operation regime and the sensitivity of the transistor.

Interface related leakage currents significantly affect the sensitivity of ultra-narrow channel FETs, and are expected to contribute to the noise in the system due to trapping and de-trapping events at the interfaces. Therefore, electrical isolation of the FET structure is a key component in achieving high sensitivity nanowire sensors. Side-gated device architecture effectively reduces the interface related leakage currents, increasing the device sensitivity. However, the ultra-narrow channel devices, less than 10 nm in width, are still prone to significant current fluctuations due to extreme sensitivity to single electron events in the surrounding of the device.

It is possible to achieve channel confinement down to 2 nm using a side-gate device architecture with good electrical characteristics as discussed in chapter 4. In this case, there can be 6 nucleotides over the electron channel at a given time. This approach of fabricating single charge sensor for DNA sequencing can achieve single nucleotide resolution if signal processing techniques are utilized to deconvolute the time-domain signal obtained from the sensor.

Another possible alternative is implementing the device geometry described in this chapter using a pFET device. In the case of a pFET device, the positive fixed charges at the Si-$Si_3N_4$ interfaces would rather enhance the device performance. The drain to substrate leakage currents are expected to be very low, since the low-doped body of the n-type body would be in accumulation of electrons [26][27]. Drain to source peripheral leakage currents are expected to be very low since the interfaces would have increased threshold voltage [28]. The effective device width would be

significantly smaller than the physical dimension for sub-10 nm channel width due to increased potential height for holes on the two edges of the channel due to high density of positive fixed charges.

# 3 Back-end-of-line Integration of Micrometer Scale Silicon Dioxide Tunnels for On-chip Fluidic Sample Delivery to Nanometer-scale Chemical Sensors

## 3.1 Overview

Use of these very small scale sensors, as described in chapter 2, requires a system to deliver the sample from an outside source into the sensor on a chip. In order to interface an external pluming system with the on-chip sensors, on-chip microfluidic tunnels are needed to bring the sample from one end of the chip into the nano-fluidic sensors and to take the sample out (Figure 3.1). For FET based sensors the delivery tunnels have to be electrically isolated from the devices. The microfluidic tunnels must be large enough to allow the necessary throughput. These tunnels can either be monolithically integrated with the sensor, where the sensors and the tunnels are fabricated together as described in chapter 2, or the tunnels can be fabricated after the fabrication process of the sensors in a back-end-of-the-line-integration fashion. In both approaches there are specific materials, process and temperature constraints for successful integration of the microfluidic tunnels with the sensors.

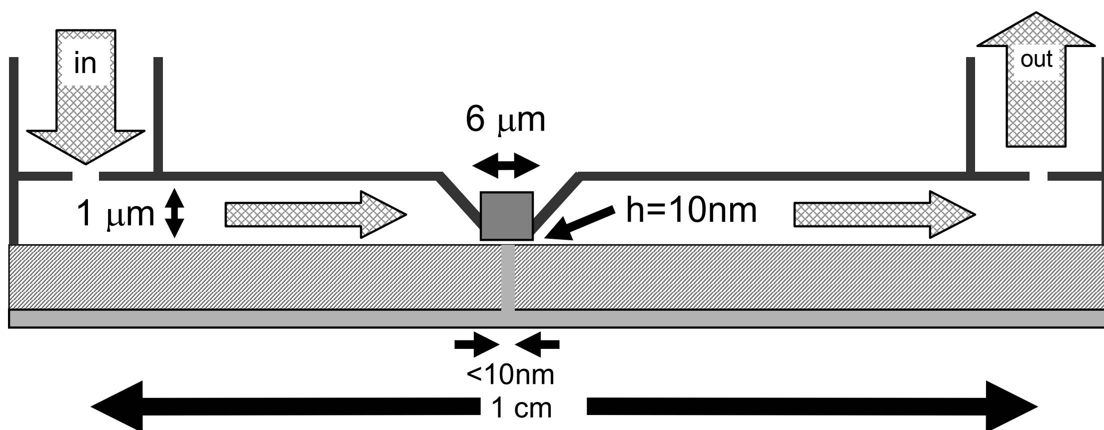


**Figure 3.1.** Fluid delivery into nano-fluidic chemical sensors from off chip reservoir. Sensors < 10 nm in width can be fabricated with a suspended gate.

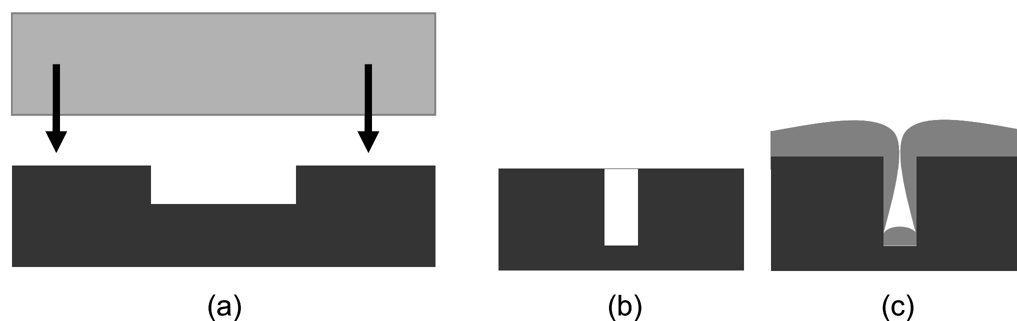


**Figure 3.2.** **(a)** Wafer bonding and **(b-c)** deposition over trenches.

Back-end-of-line integration of microfluidic tunnels gives more flexibility in the size of the tunnels and simplifies the processing of the sensors. There are a few different possible approaches for integrating microfluidic tunnels after the formation of the sensors [36].

One of the most common approaches is to use wafer bonding (Figure 3.2 a). In this approach, a planar wafer is bonded on top of the patterned surface after the formation of micrometer size trenches by RIE, sealing the top surface and forming the microfluidic tunnels. This method is very useful if optical detection schemes are used for sensing. However, it is not practical if electrical sensing schemes are used, due to the necessity of making electrical contact to the sensor electrodes and difficulty in etching through the bonded top wafer.

Another alternative for forming microfluidic tunnels is by deposition of a thin film over the wafer after the formation of trenches (Figure 3.2 b-c). During the deposition process, the active areas of the FET structures and the two ends of the tunnels leading into the sensing area are exposed to the ambient gases and a film of deposited material will form in these areas. Although this method allows easy access to the contact areas of the electrodes, the deposition of the thin film over the active area of the transistor would significantly degrade the sensing capabilities and the films deposited at the ends of the nanometer-scale tunnels can seal off the sensors.

Deposition of a blanket layer over patterned sacrificial structures is yet another alternative approach for making the tunnels. In this process the sacrificial layer can be etched from small holes opened on the top surface of the tunnels. The deposition and etch processes used for the fabrication of the tunnels should leave the existing structures intact. This requires careful selection of the sacrificial material, capping material and wet chemistry. The deposition temperature of the sacrificial and the capping layers need to be low enough to minimize dopant diffusion and in some cases allowing the metal structures' survival during the process. The capping layer needs to be a good insulator in order to prevent any electrical leakage and it is desired to be strong enough to withstand subsequent cleaning and annealing steps.

In this chapter a low temperature method for back-end-of-line integration of microfluidic tunnels with nanometer-scale FET based chemical sensors is described. Photoresist is used as sacrificial material and $SiO_2$ is used as capping material.

## 3.2 Fabrication process

FET based chemical sensor structures are fabricated with polysilicon gates suspended approximately 10 nm over the active area as described in chapter 2 (Figure 3.3). The gate structure forms the ceiling of a shallow tunnel passing through the device where the two sides of the tunnels are covered with deposited $Si_3N_4$. The sample is delivered from an off chip source to the sensors through ports attached to the chip and on-chip delivery tunnels. The sample delivery ports are attached to the chip at approximately 1 cm separation.

This process allows fabrication of 1.3 μm high and 40 - 100 μm wide delivery tunnels. In this design support pillars are used at every 10 μm. Tunnel ceilings are designed to have arch-shaped geometry in order to achieve good mechanical strength and less viscous drag.

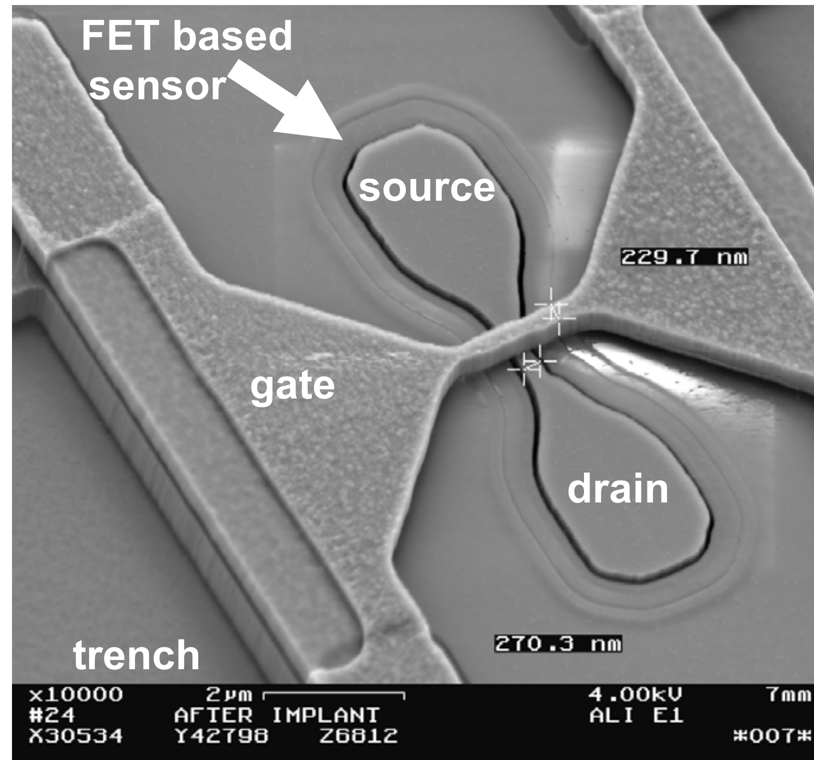


**Figure 3.3.** Scanning electron micrograph (SEM) of a FET based chemical sensor after trench formation

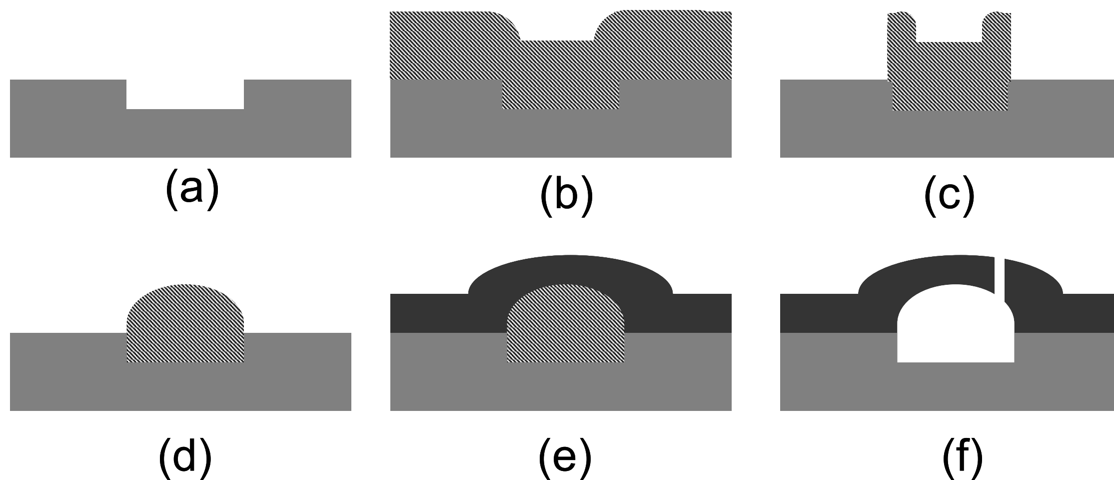


**Figure 3.4.** Tunnel fabrication process using sacrificial resist: (a) Etch trenches using RIE, (b) spin resist, (c) pattern resist, (d) smooth resist profile, (e) deposit cap oxide, (f) open irrigation holes & dissolve resist.

In order to fabricate these tunnels, trenches of approximately 0.3 μm are etched into the substrate overlapping with the two ends of the sensor devices (Figure 3.4a). This step also opens the ends of the shallow tunnels for the removal of sacrificial material underneath the gate of the FET structure (Figure 3.3). After the removal of the sacrificial material underneath the gate of the FET, a 1.2 μm resist layer is spun on the wafer. The wafers are exposed with UV light through the same mask as used to define the trenches with a higher dose in order to form wider resist patterns than the existing trenches to accommodate slight misalignment between the layers (Figure 3.4 b). An $NH_3$ image reversal process is performed. The wafer is then flood exposed to UV light and developed, resulting in photoresist filling inside the trenches. The resist filling slightly extends out of the trenches on the sides and forms abrupt edges (Figure 3.4 c). The resist fill is then smoothed by heated oxygen plasma and baking in a convection oven at 135 C for 1 hour (Figure 3.4 d) resulting in a resist profile forming a smooth arc on the top surface (Figure 3.5). The structures are then capped with $SiO_2$ and the sacrificial resist is dissolved from irrigation holes etched down from the top surface. The $SiO_2$ deposition temperature has to be kept below the baking temperature of the resist in order to avoid out-gassing of the resist during deposition. The maximum process temperature must be kept under 140 C for easy removal of the sacrificial resist using acetone.

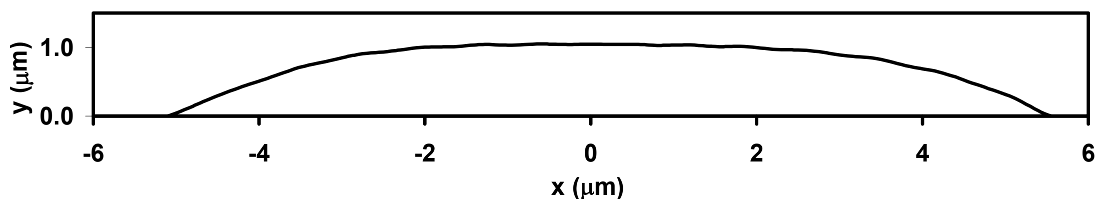


**Figure 3.5**. Sacrificial resist profile after heated oxygen plasma treatment and oven

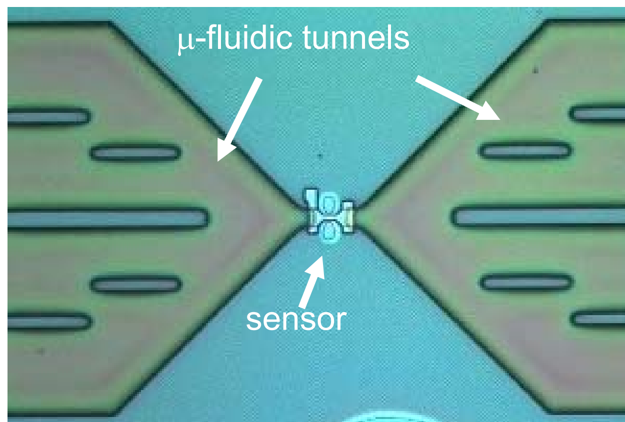


**Figure 3.6.** Optical image of the sensor and the microfluidic tunnels for sample delivery after oxide sputter deposition.

Silicon dioxide cap layer can be deposited over the structures using e-gun evaporation, RF sputtering or plasma enhanced chemical vapor deposition (PECVD) at temperatures under 140 C (Figure 3.6). E-gun evaporation is a room temperature process, however, it is a line of sight deposition and small steps with steep slope result in cracks in the deposited films. Furthermore, the deposited films are not robust enough to survive subsequent processing steps.

PECVD $SiO_2$ films deposited at 110 C are mechanically robust and conformal. However the intersection of the delivery tunnels with the shallow tunnels of the sensors get clogged if PECVD $SiO_2$ is directly deposited onto the resist structures. This may be due to conformation change in the resist-filling and/or gases leaking into the openings between the resist fill and the shallow tunnels at the intersection during deposition. Since the shallow tunnel heights are in the order of 10 nm, a small amount of material deposition at the intersection is enough to clog the system.

RF sputtering of $SiO_2$ is also a very low temperature process (< 100 C). The sputter deposited films are more conformal than evaporated films, and do not clog the system unlike the PECVD $SiO_2$ films. However the lower parts of the sputtered $SiO_2$ structures tend to be very weak if the top surfaces have relatively steep angles as seen

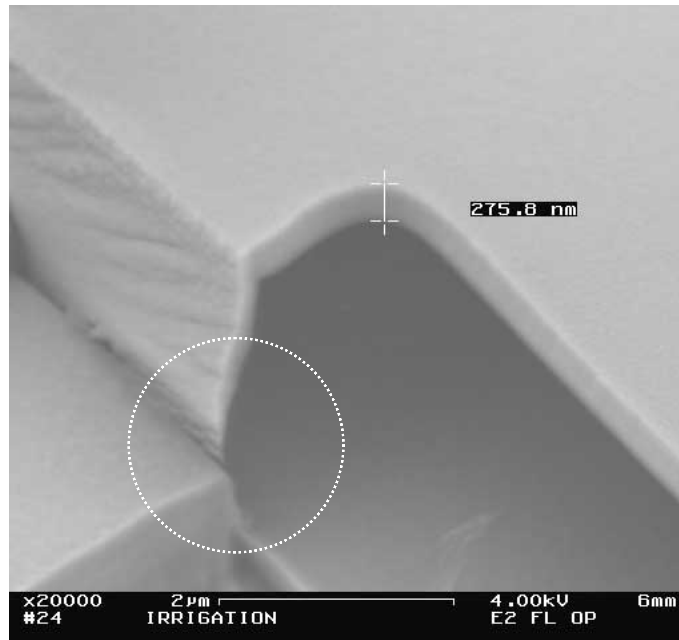


**Figure 3.7** RF sputter deposited oxide tunnel structures. The sputtered oxide is significantly thinner at the bottom portion of the side-walls.

in Figure 3.7. These films are not robust enough to survive the resist removal process and tend to break at the weak points as highlighted in the figure.

A combination of an initial RF sputter deposition followed by PECVD process proved to be a viable approach (Figure 3.8). An initial RF sputter deposited 0.25 μm $SiO_2$ shell minimizes the movement of the resist-fill and prevents the clogging of the tunnel junctions during the PECVD deposition of an additional 1 μm $SiO_2$ layer at 110 C. The deposited PECVD oxide forms a robust film covering the top of the microfluidic tunnels. The sacrificial resist is dissolved with acetone through the irrigation holes opened on the top surface of the tunnels. The tunnels are then washed with isopropanol (IPA) and deionized water. At this stage preliminary tests using deionized water can be performed. For a fully functional system the irrigation holes need to be sealed. This can be carried out by deposition of $SiO_2$ or spinning of polyimide on the wafer. The size of the irrigation holes and the tunnel height at the locations of the holes should be minimized to reduce the deposition of the final

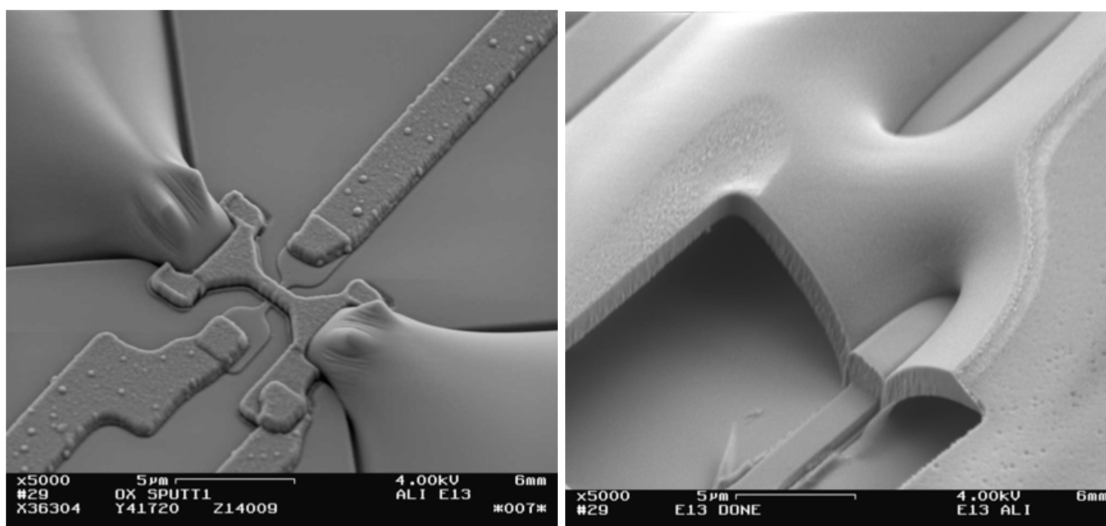


**Figure 3.8.** SEM image of resist filled tunnels after oxide RF sputter deposition (left) and sidewalls of the oxide structure after PECVD oxide deposition and resist removal (right).

capping material into the inner walls of the tunnels. This can be achieved by opening the irrigation holes on the edges of the tunnels where the tunnel height is significantly smaller. If polyimide is going to be used for sealing of the irrigation holes, the input and output areas on the tunnel system should be opened prior to curing of polyimide. The solvents trapped in the tunnels can dissolve the polyimide film and polyimide can fill into the tunnels if the input and output areas are not opened. Using a vacuum oven would be useful, ensuring process reliability, for the curing process.

## 3.3 Conclusion

A low temperature (< 135 C), CMOS compatible back-end-of-the-line process of making micrometer scale silicon dioxide tunnels for fluidic sample delivery to CMOS based chemical sensors is developed. A combination of RF sputtered $SiO_2$ and PECVD $SiO_2$ films are used to reliably cap the sacrificial photoresist patterns ensuring the continuity of the tunnels into the sensors. It is possible to fabricate multiple levels of microfluidic networks with tunnels crossing one over another by repeating the

process steps. This process requires a good temperature control to ensure that the samples are not heated over 140 C in order to allow the removal of sacrificial photoresist. Due to temperature control problems experienced in the PECVD system used for the process, a monolithic integration scheme of the tunnels with the sensors was found to be more suitable. Monolithic integration scheme, described in the previous chapter, does not allow as much flexibility in making the delivery tunnels as large as back-end-of-line integrated tunnels as described in this chapter; however monolithic integration reduces the process complexity and improves the process reliability as it was described earlier.

# 4 Side-gated MOSFET

Side-gated device structure was developed in order to suppress the interface related leakage currents for the devices fabricated using silicon nitride as HF resistant CMOS compatible isolation material. In addition to suppression of peripheral leakage currents, short channel effects can be significantly suppressed for sub-70 nm gate length and threshold voltage tuning can be achieved for narrow channel devices using this approach, in a bulk CMOS geometry [5][29][41][36]. The fabrication process, using bulk planar silicon processing, is significantly simpler compared to other double-gate structures developed for high performance VLSI circuits and adaptive threshold voltage control [30]-[33], [42]-[49]. This geometry also allows increased process flexibility for integration of high-K and low-K insulating materials and HF-released active and passive mechanical structures [3][4], [10]-[14].

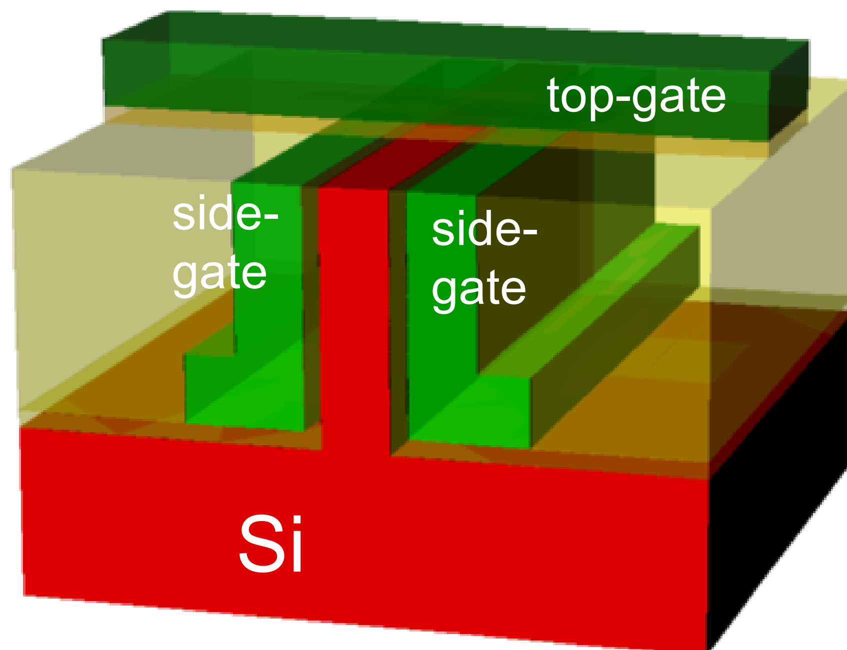


**Figure 4.1** 3D schematics of side-gated FET utilizing silicon nitride field isolation. The two side-gates are connected together and the top gate is operated independently.

Side-gated device architecture, effectively reducing leakage currents, is well suited for VLSI circuits where power dissipation is a key concern [38][39][40], especially for ultra-low power circuits in many mobile applications that do not demand the highest speeds.

## 4.1 Power concerns in VLSI devices

Static power dissipation, arising from gate leakage ($I_g$), drain-to-substrate leakage ($I_{d\text{-}sub}$) and drain-to-source ($I_{ds}$) off-current, are major contributors to total power dissipation in bulk Si devices [39]. Controlling power dissipation, while achieving required speed performance, is critical for transistors at the sub-50 nm length scale. Elimination of peripheral leakage mechanisms, suppression of short channel effects and ability to electrostatically tune the threshold voltage ($V_t$) [30][31] allow increased scaling and control of power dissipation.

Gate leakage ($I_g$) is proportional to the gate area (W x L) of the device. $I_g$ can therefore be reduced if the gate area can be scaled down while achieving the desired performance. $I_{d\text{-}sub}$ and $I_{ds}$ leakage currents in a MOSFET constitute of bulk and peripheral components. The bulk component of $I_{d\text{-}sub}$ and $I_{ds}$ leakage, and $I_g$ are directly proportional to the channel width (W). These leakage components can be reduced by scaling the width of the devices. The peripheral components of $I_{d\text{-}sub}$ and $I_{ds}$ leakage, mainly due to defects and fixed charges on the active-STI interface, do not scale with W and become increasingly important as the device widths are scaled down. The active-STI interface defects lead to reduced $V_t$ on the edges [28], giving rise to increased $I_{ds}$ off-currents, and enhances $I_{d\text{-}sub}$ leakage currents through defect assisted recombination mechanism in the depletion region of the reverse biased drain junction [27]. Decreasing ability to modify the threshold voltage on the periphery of narrow channel devices to suppress these leakage currents through implantation necessitates

alternative approaches. Ultra-thin body SOI and double-gated structures [42] reduce the total area of the periphery, thus reducing the associated leakage, but at a cost of increased source/drain resistance. Fully depleted SOI approaches totally eliminate $I_{d\text{-}sub}$ leakage, but suffer floating body effects and an additional silicon–insulator interface with fixed charges at the bottom of the device.

Suppression of short channel effects allows continuation of conventional gate length scaling. Dynamic $V_t$ control allows optimization of power consumption commensurate with speed requirements. This can be achieved by changing the body potential by either directly biasing the body via body contact or capacitively controlling the body potential using a double-gate approach. Most of the reported double-gate structures have a back-gate placed on the opposite side of the main gate allowing device width to be an independent variable and utilizes significantly complicated processing techniques. As the device dimensions shrink, gate length and width of devices approach the depletion depth (in bulk) or the body thickness (in fully-depleted SOI), side-gated device approach, another independently controlled multi-gate structure, becomes viable where the gates controlling the threshold of the device are on the two sides of the active area.

## 4.2 Device design

In order to control all the Si-STI interfaces relevant to the devices, the side-gate structure is designed to surround the active areas of the devices and lead to a contact area running inside the STI structure. The side-gate of the structure is designed to be composed of highly doped polysilicon, conformally deposited in an LPCVD system. The contact area for the side-gate is designed to be away from the device, in order not to interfere with the source, drain and gate contacts. An additional via is needed to make electrical contact with the side-gate electrode. The side-gates of the

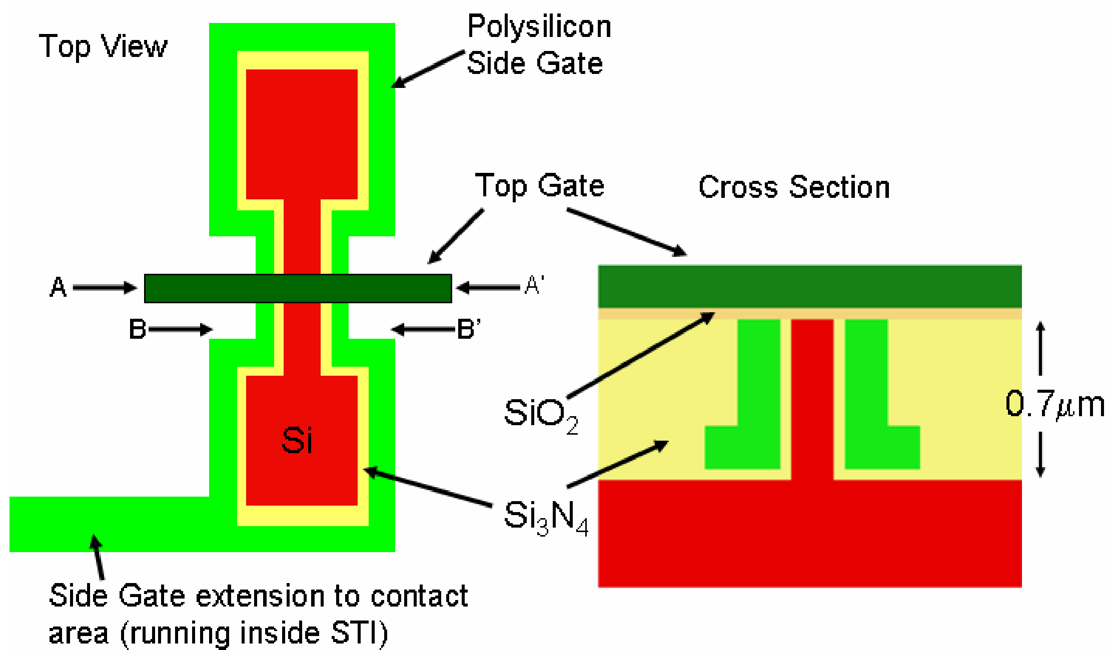


**Figure 4.2** Top (left) and cross sectional schematics of the side-gated FET.

devices extend from the top surface to the bottom silicon surface and are part of the STI structure. Polysilicon side-gate can be routed from one device to another inside the STI, as side-gate local interconnects, leading to very minimal area penalty in high density circuits.

The side-gated device structure resembles a finFET transistor [45][46] with the exception of an independently controlled top gate (Figure 4.2).

While the employment of side-gates significantly suppresses the leakage currents in wide devices, the potential applied on the side-gate has more significant effect on the narrow channel devices. In the case of narrow channel devices, electrical

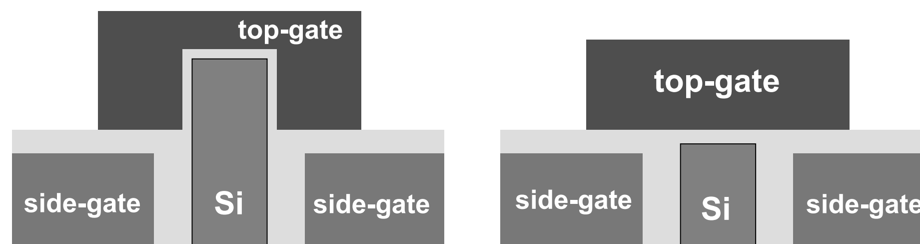


**Figure 4.3** Cross section schematics of devices with recessed side-gates (left) and planar top-gate geometry.

characteristics of the devices significantly depend on the device dimensions and the topography of the channel (Figure 4.3).

The active areas of the devices can be made to be slightly higher than the surrounding structure, which leads to a device structure where the top part of the active area is wrapped over by the top gate. In this device structure, resembling a tri-gate FET [50], the top-gate of the device has very good control over the channel potential.

### 4.2.1 Side-gate control over body potential in planar geometry

In the case of a device structure where the channel of the device is at the same level as the surrounding side-gate, the potential in the channel is significantly affected by the side-gate bias, especially for ultra-narrow devices. Application of a negative potential from the two sides of the channel in a narrow-channel nMOSFET restores the source to drain potential barrier and leads to enhanced current confinement to the top silicon-oxide interface. The top-gate potential achieves a stronger control over $I_{ds}$,

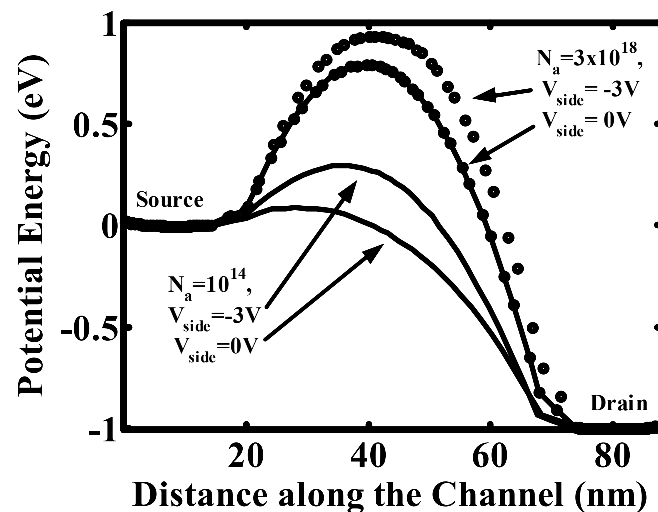


**Figure 4.4** Simulated potential barrier for a W x L = 50 nm x 40 nm device with side-gate for intrinsic channel and $N_{sub}$ = 3x10$^{18}$ cm$^{-3}$ at the device center. $t_{side}$ = 15 nm ($Si_3N_4$), $Q_{interface}$ = 3x10$^{10}$cm$^{-2}$.

leading to significant improvements in $I_{on}/I_{off}$ in small-scale devices. 2D simulated potential profiles [51] for a W x L = 50 nm x 40 nm device show approximately 0.2 eV recovery in potential barrier with the application of -3 V at the side gate for an intrinsic channel device. Similar improvement is observed in the highly doped drain case (Figure 4.4).

In the case of a 30 nm x 30 nm device, where the short channel effects and the edge related leakage currents become more important, the improvement in the height of the potential barrier exceeds 0.5 eV with the application of -3 V at the side-gates for a highly doped body. The case for a low positive interface charge density, with $Q_{int}$ = $3x10^{10}$ $cm^{-2}$ is shown in Figure 4.5. The potential at the device edges is recovered and increased over the barrier height in the center of the device. The sag in the center potential, seen in the potential cross section along the width of the device, is due to the drain potential (Figure 4.6). The effect of the body and the top gate potentials are not

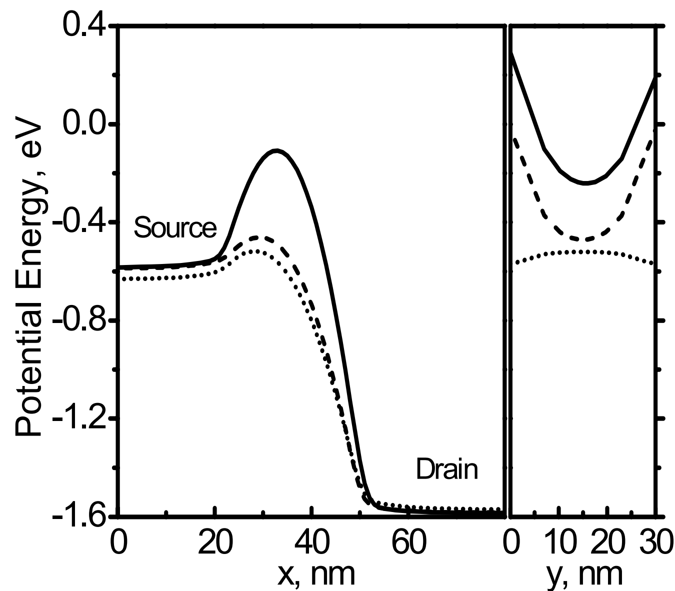


**Figure 4.5** Simulated potential profiles for a 30 nm x 30 nm side-gated device, $t_{side}$ = 19 nm ($Si_3N_4$) along the channel (left) and across the channel (right) for $N_{sub} = 3x10^{18}$ $cm^{-3}$ (solid), $N_{sub} = 1x10^{14}$ $cm^{-3}$ (dashes) and a conventional bulk device with $N_{sub}$ = $3x10^{18}$ $cm^{-3}$ (dots). Interface charge density $Q_{int} = 3x10^{10}$ $cm^{-2}$.

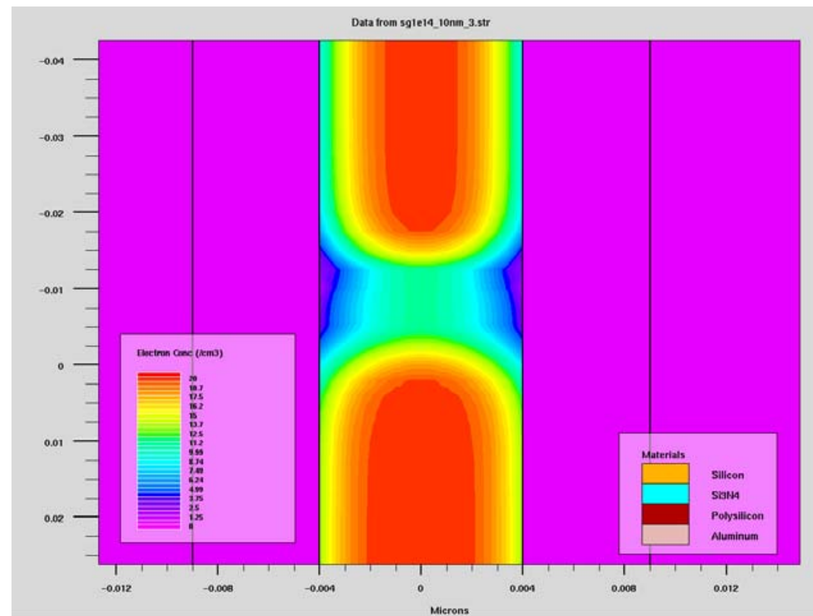


**Figure 4.6** 2D simulated electron concentration profile of a W x L = 8 nm x 10 nm, $t_{side}$ = 5nm ($Si_3N_4$), intrinsic channel device. The electrons are confined to approximately 5 nm in the central section of the channel.

reflected in the 2D simulations. The potential profile across the width of the device is expected to be more uniform for a higher positive interface charge density since the potential barrier is significantly lowered at the edges due to the positive fixed charges at the interfaces.

In the case of an extremely short and narrow device structure with 10 nm x 10 nm device dimensions, it is not possible to form a potential barrier between the source and the drain through increased concentration of body doping . However, 2D simulation results show that a 8 nm x 10 nm intrinsic channel device with 5 nm $Si_3N_4$ side-gate isolation can have a potential barrier exceeding 0.5 eV through application of –3 V on the side-gates (Figure 4.7). It is seen that strong coupling by the two side-gates straddling the active area have significant control over the body potential and only very small amount of drain induced barrier lowering (DIBL) is observed.

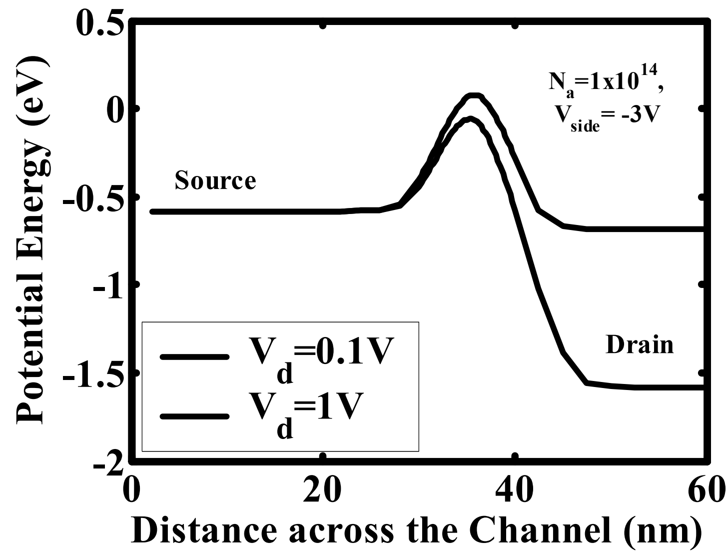


**Figure 4.7** Simulated potential barrier for a W x L= 8 nm x 10 nm, $t_{side}$ =5 nm ($Si_3N_4$), intrinsic channel device with side-gate for two drain biases, $V_{side}$ = -3 V. A potential barrier higher than 0.5 eV is observed.

In standard short-channel planar devices, the gate control the on the body potential is significantly reduced as a function of the distance from the channel. The potential of the bottom part of the Si body is significantly controlled by the source and drain potentials down to the level of the source/drain junctions which necessitates introduction of halo implants to suppress the short channel effects. In the case of the side-gated approach, the potential barrier seen in Figure 4.7 exists in the same way independent of the distance from top interface. The volume underneath the top-gate can be put into accumulation and hence, significantly reduce the depletion depths of the source-drain junctions. This, in a way, is equivalent to employment of halo implants in order to reduce the junction depletion depths to facilitate suppression of the short channel effects. This results in extreme confinement of the current to the very top Si-$SiO_2$ interface, controlled by the top-gate.

Simulation results show that control of the channel potential with an independently controlled side-gate makes it possible to use intrinsic channels for very

small-scale bulk Si MOSFETs, and reduces or eliminates the need for halo (pocket) implants, which is practically impossible to achieve at 10 nm device scale. It may be possible to achieve the electrostatic construction of the potential barrier through fixed charges on the two sides of the channel or using highly polarized material in contact with the silicon surface on the two edges. It is also possible to inject charges into a thin polysilicon layer, acting as a floating gate, surrounding the active area through a tunneling process. This approach can lead to a similar potential barrier, avoiding the penalty of the additional parasitic capacitance.

Lower doping levels in the channel result in higher low-field carrier mobility and the use of undoped channels eliminates the threshold voltage variation due to random dopant effects which is becoming one of the limiting factors in high performance VLSI devices. Reduction or elimination of pocket implants leads to reduced band-to-band tunneling in the drain junctions of bulk and partially depleted SOI devices, thus reducing the bulk component of the $I_{d\text{-}sub}$ leakage. The improvement in the $I_{d\text{-}sub}$ leakage with the application of a negative side-gate bias is, however, limited by the onset of the gate induced drain leakage (GIDL) [52]. GIDL is more severe for abrupt junctions of highly doped drains. The side-gate structure surrounding the active area of the devices form ground planes with a DC bias. This is similar to guard rings and deep trenches employed in mixed signal technology in order to suppress the synchronous substrate noise [53]. If the side-gates are biased through a low resistance path, the devices can be effectively isolated from the noise generated by the neighboring devices.

### 4.2.2 Side-gate control over body potential in tri-gate geometry

While the potential profiles look the same at the bottom portion of the Si fin shaped active area in planar and tri-gate geometries, the potential profile on the top

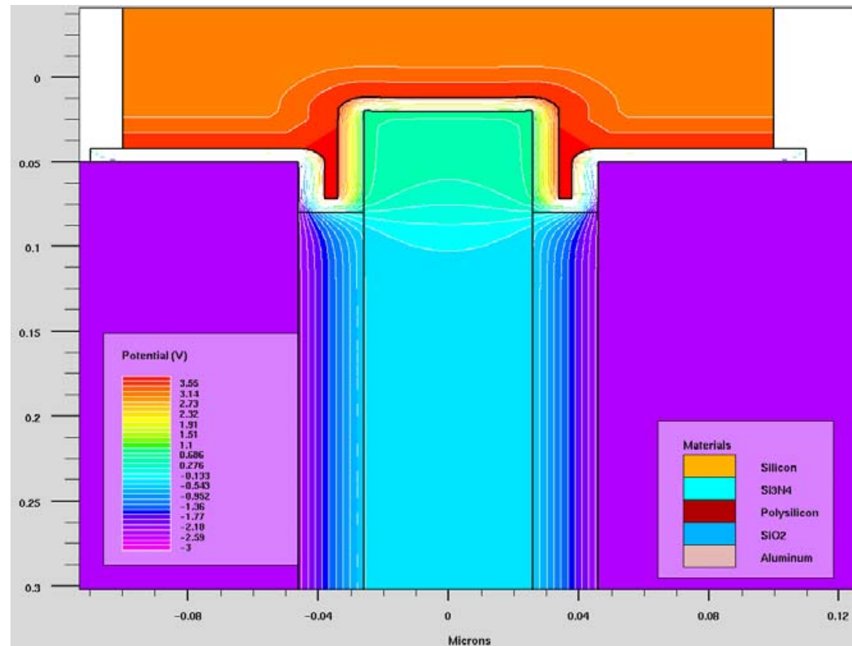


**Figure 4.8** Simulated potential profile of a 50 nm wide tri-gate structure with 50 nm side recess. $V_{side}$ = -3 V, $V_g$ = 3.5 V

portion of the fin is predominantly controlled by the top-gate in the tri-gate geometry. The tri-gate structure benefits from the significant reduction in the peripheral leakage mechanisms at the bottom portion of the device in the side-gated geometry but the channel potential is almost totally independent of the side-gate potential.

Compared to the standard tri-gate and finFET structures built on SOI substrates, bulk tri-gate geometry with the side-gate passivation of leakage currents does not have any interfaces which is not electrostatically controlled by a gate. Standard tri-gate and finFET devices built on SOI substrates achieve control over the 3 of the 4 interfaces between the source and the drain but does not have any strong electrostatic control over the bottom active (Si)-oxide interface and suffer from floating body effects. Elimination of the bottom silicon-oxide interface results in elimination of fixed charge related problems at the bottom of the device, floating body effects and problems in heat dissipation due to thermal insulation provided by the oxide layer. Another

advantage of this bulk tri-gate architecture is reduction of the source-drain resistance experienced in ultra-thin body SOI structures.

Figure 4.8 shows simulated 2D potential cross-section of a side gated tri-gate structure for $V_g$ = 3.5 V and $V_{side}$ = -3 V. The bottom part of the fin is kept at a higher potential while the top-part is turned on. Figure 4.9 shows the electron distribution for the same case. Bottom part of the fin is in accumulation of holes.

Additional advantages of the tri-gate geometries are increased carrier density and reduced polysilicon gate depletion effects due to larger flux of field lines being terminated on the channel surface. The electric field in the tri-gate area is also smaller compared to planar devices. This is expected to reduce mobility degradation due to high field effects. Increased carrier concentration for the same surface area is expected to result in increased drive current for a given amount of gate leakage.

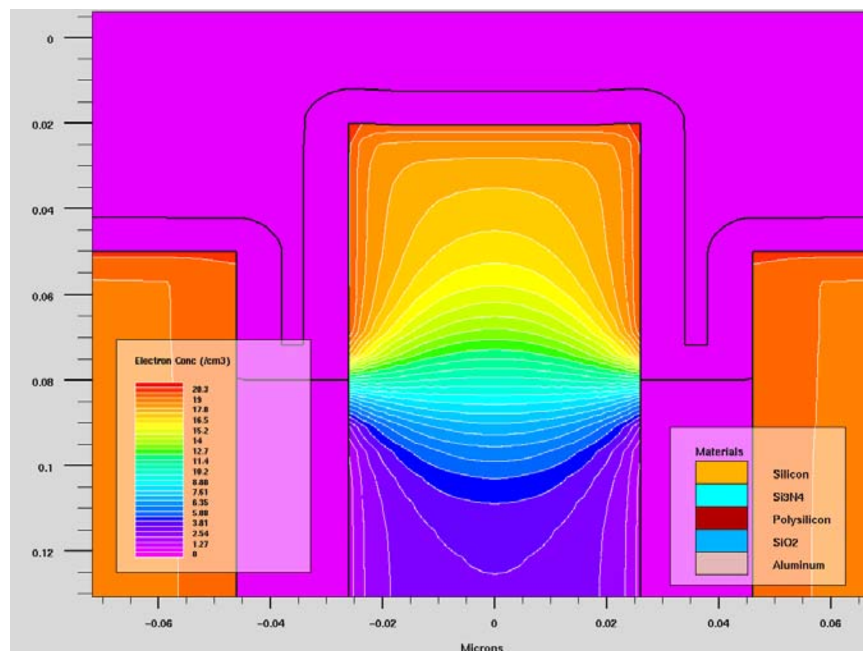


**Figure 4.9** Simulated electron concentration profile of a 50 nm wide tri-gate structure with 50 nm side recess. $V_{side}$ = -3 V, $V_g$ = 3.5 V

## 4.3 Fabrication

The side-gated devices are fabricated by slight alterations done to the fabrication process described in chapter 2. The tools and the steps used for photolithography are the same. The nMOSFETs reported in this chapter are fabricated without using any halo implants or silicidation process, similar to the devices described in chapter 2.

### 4.3.1 Side-gate deposition and patterning

Active area definition, etch, dopant enhancement and device width reduction through oxidation are performed, as explained in chapter 2. The diffusion time for dopant enhancement is kept shorter in this case. After these steps a 19 nm conformal layer of LPCVD $Si_3N_4$ is deposited. Nitride deposition is immediately followed by LPCVD deposition of 350 nm $n^+$ in-situ doped polysilicon layer at 600 C. This film

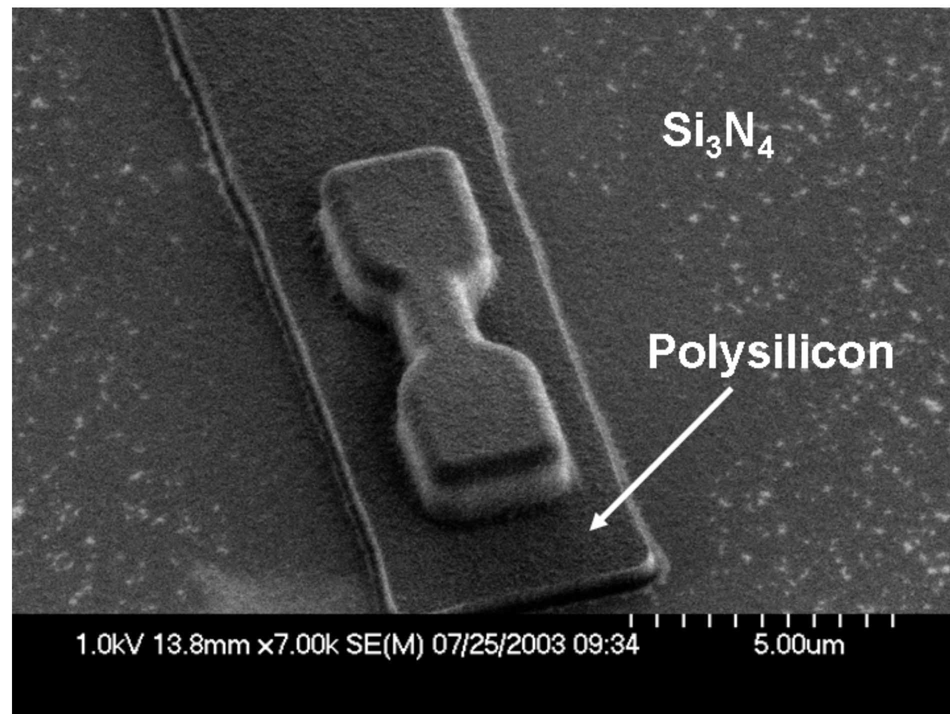


**Figure 4.10** SEM micrograph of the active area after side-gate patterning prior to STI nitride deposition. The polysilicon film extends away from the device to a contact area

conformally covers all the surfaces just like the underlying $Si_3N_4$ layer. A 150 nm oxide layer is deposited using a PECVD system at 400 C to be used as etch mask. Side-gate areas are patterned using a mask for side-gate layer following the same steps described in section 2.2.1. Mask oxide and polysilicon are etched using RIE following the same procedure described in section 2.2.5 for gate poly definition. The remaining mask oxide at the end of the RIE process is removed in 6:1 BOE (Figure 4.10).

### 4.3.2 Shallow Trench Isolation

After side-gate definition, a thin layer of stochiometric nitride and a thicker layer of low stress nitride are deposited and the wafers are planarized using CMP in the same way as described in section 2.2.4.

In order to achieve the tri-gate structure, wafers are oxidized in $O_2/N_2$ ambient and oxide is removed in diluted HF after the planarization step. This process results in slight increase in the recess of the side-gate structure compared to the silicon active area due to the difference in oxidation rate, resulting in the tri-gate device structure (Figure 4.3). Tri-gate device structure can also be achieved by keeping the wafers in HF solution for an extended period of time, removing some of the nitride on the sides between the active areas and the side-gates (Figure 4.11).

Oxidation of the Si surface is omitted and the exposure of the wafers to HF is minimized in order to build the devices with planar top-gate geometry. An alternative approach of depositing a thin layer of $Si_3N_4$ and a short CMP, after slight recess of the side-gates can be used to ensure a planar top-gate geometry.

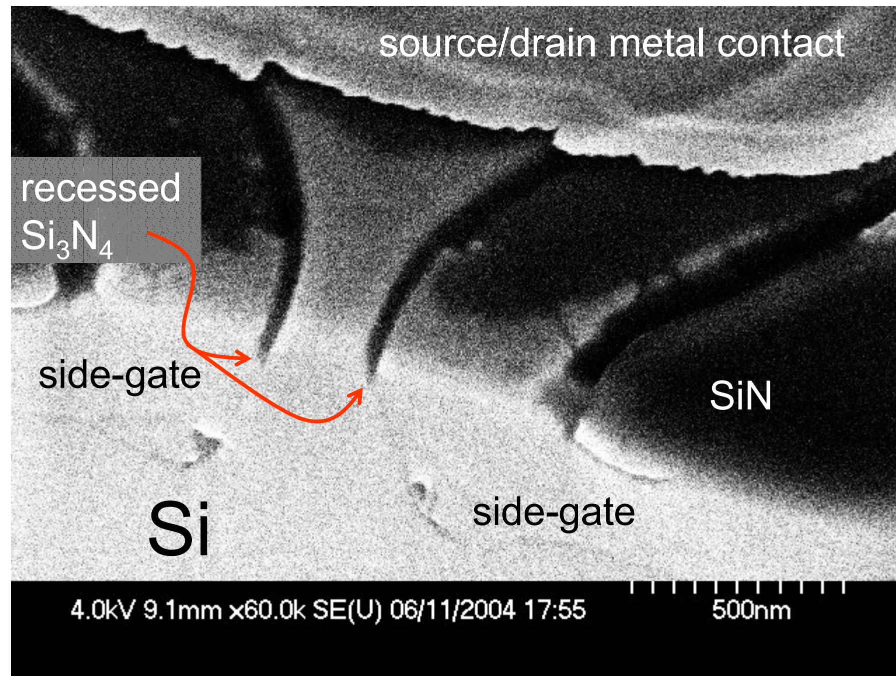


**Figure 4.11** Cross sectional micrograph of a side-gated FET gone through side-gate $Si_3N_4$ recession in HF. Device is cut through the active region using a focused ion beam (FIB) system.

### 4.3.3 Gate stack

A 4 nm oxide layer is grown in $O_2/N_2$ ambient at 725 C to serve as gate dielectric. In this step, an oxide layer is also grown over the side-gates of the structure which will be serving as the side-gate to top-gate isolation. The oxidation rate of doped polysilicon is higher, hence leading to a thicker oxide over the side-gates, which is desirable for reduced parasitic coupling and increased oxide reliability. The oxide grown on the polysilicon is expected to have a lower breakdown field compared to oxide grown over single crystal silicon.

A 100 nm polysilicon layer is deposited using an LPCVD system at 600 C to be defined as the top-gate of the structure. The top-gate of the structure is defined and etched with RIE in the same manner as described in section 2.2.5 with RIE process terminated at the $SiO_2$ surface (Figure 4.37).

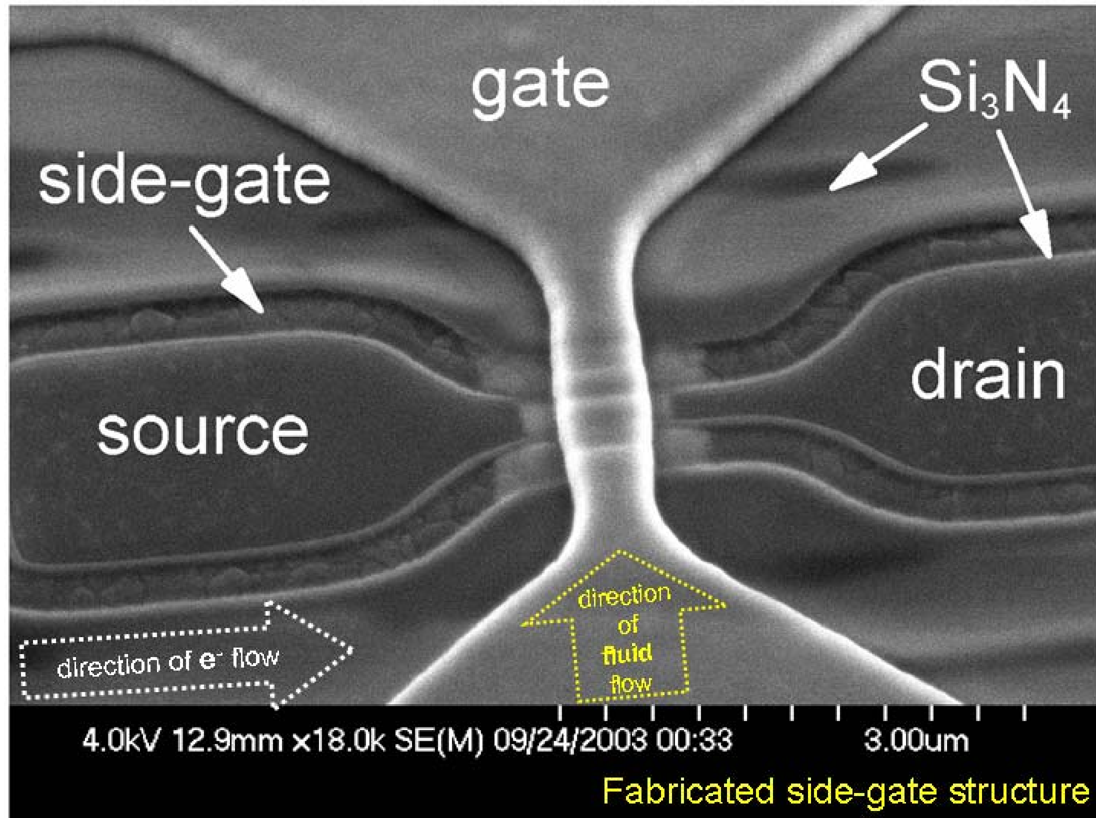


**Figure 4.12** SEM image of a side-gate FET before passivation. The direction of the fluid flow in the case of sensor application is indicated, though this particular device is not fabricated as a sensor.

### 4.3.4 Self-aligned source/drain formation

A thin layer of oxide is grown on the sidewalls of the polysilicon gate as described in section 2.2.6. Wafers are then implanted with arsenic with $5x10^{14}$ $cm^{-2}$ at 20 keV with 90° rotation and 8° tilt.

After the implantation, the films on the back-side of the wafer are removed and the back side of the wafer is polished using CMP in the same manner as described in section 2.2.12

### 4.3.5 Passivation & vias

A 90 nm layer of $SiO_2$ is deposited at 400 C using a PECVD system as a passivation layer. A photolithography step is carried out to define the vias. After oxygen plasma descum, the vias are opened using wet chemistry in 6:1 BOE. This process ensures the termination of the etch process on the silicon surface and results in a curved profile going down from the passivation surface to the Si contact areas, desired for metal contacts which will be deposited through evaporation of a metal stack.

An additional via is needed to be opened in order to access the side-gate contact area. This is carried out by performing an additional photolithography step using a mask to open large vias into the side-gate contact areas. The oxide and the nitride films at the side-gate contact via areas are etched using RIE with $CHF_3/O_2$ chemistry.

### 4.3.6 Metallization & anneal

Metallization using Ti/Al lift-off process is carried out in the same manner as described in section 2.2.11. The Ti/Al stack is evaporated on the back-side of the wafer immediately after the metal evaporation onto the front-side, prior to lift-off. The wafers are annealed in $H_2$/Ar at 400 – 450 C for 15 min. in order to improve the contact resistance and reduce the contribution of the interface states.

## 4.4 Electrical Characteristics

In this section electrical results are categorized as peripheral leakage characteristics common to all devices and device characteristics for five different cases as tri-gate, long & wide channel, narrow channel, short channel and ultra-narrow channel side-gated devices.

The peripheral leakage characteristics do not change as a function of the device size or topography of the active area, and depend on the doping densities and concentration of fixed charges and defects common to all devices. Tri-gate structure is presented to show the distinct characteristic of threshold voltage immunity to the side-gate bias of the tri-gate topography. The long (0.3 μm) & wide (0.6 μm) channel device characteristics are demonstrated for comparison with standard nMOS transistor characteristics, showing the device performance parameters in the long channel case. Narrow channel (W < 100 nm) and short channel (L < 70 nm) tri-gate transistor characteristics show potential improvement over standard high performance CMOS devices, with extremely low peripheral currents and suppression of short channel effects. Ultra narrow-channel (< 10 nm) planar device characteristics show significant threshold voltage response to side-gate bias. Drain to substrate leakage and drain to source peripheral leakage characteristics are very similar for all cases. Other device characteristics such as subthreshold slope (SS), drain induced barrier lowering (DIBL), on current ($I_{on}$), transconductance ($g_m$) and response of the threshold voltage ($V_t$) to $V_{side}$ vary significantly depending on the device width and topography of the channel surface.

### 4.4.1 Drain-to substrate diode

DC current-voltage characteristics of abrupt $n^+$- p junctions formed at the source/drain & substrate interfaces are measured as a function of side-gate bias ($V_{side}$) (Figure 4.13). Drain to substrate reverse-bias leakage current decreases as a function of $V_{side}$ down to approximately $V_{side}$ = -1.5 V as the interface is accumulated with holes [27]. After this point the leakage current starts to increase again which can be explained by increased band to band tunneling known as gate induced drain leakage (GIDL) [52]. The $I_d$-$V_d$ characteristics of the side-gated drain to substrate diodes for

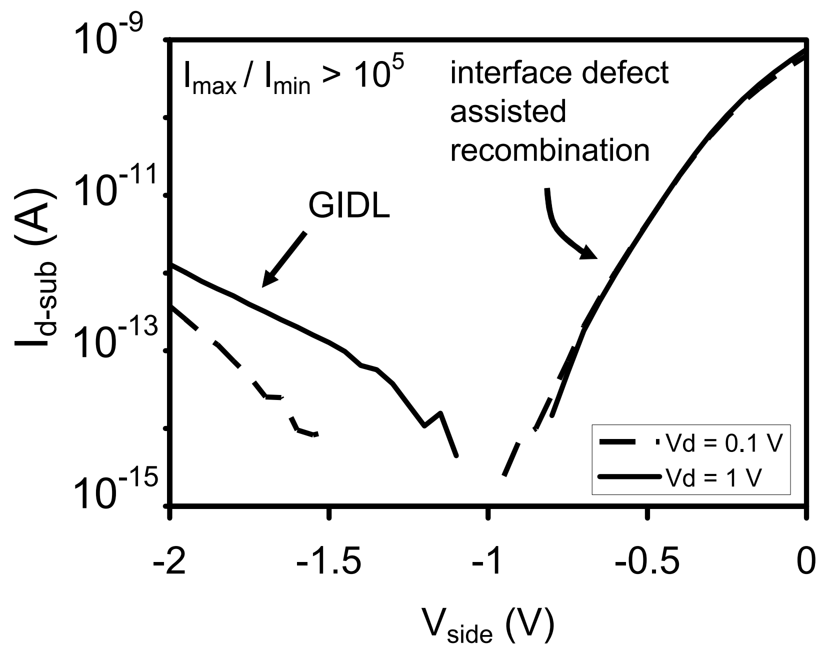


**Figure 4.13** Reverse-bias leakage current of a drain to substrate diode as a function of $V_{side}$. Area ~ 5 μm$^2$, perimeter ~ 18 μm.

different $V_{side}$ show that there is no change in the on currents for different $V_{side}$ (Figure 4.14).

The effect of GIDL is not observable for low doped drain (LDD) devices (Figure 4.15). In the LDD case, the junctions are graded and a larger negative bias on the side-gate is required to increase the band-to-band tunneling process to an observable level in the current measurements.

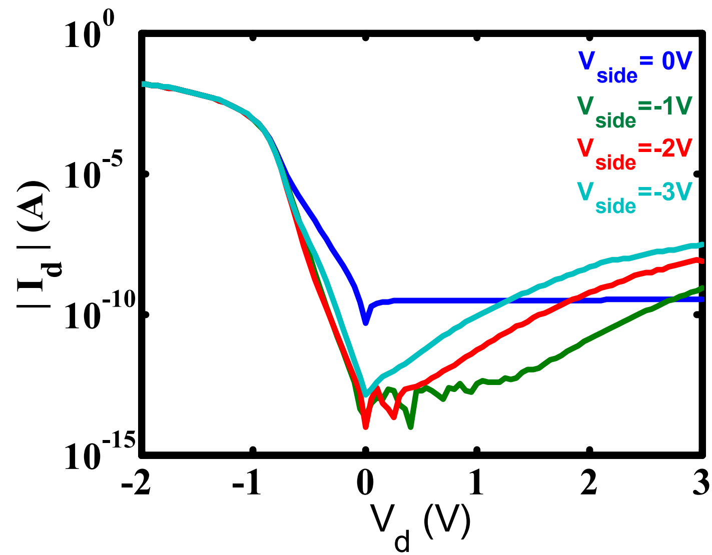


**Figure 4.14** Current versus voltage characteristics of a drain to substrate for different side-gate potentials . Area ~ 6 μm$^2$, perimeter ~ 18 μm.

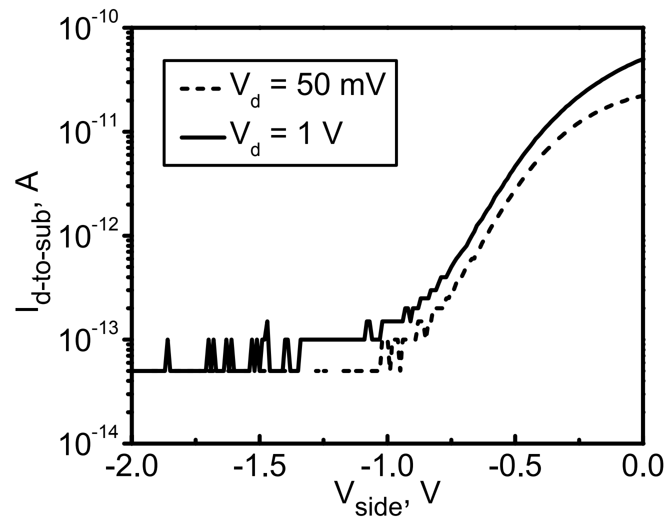


**Figure 4.15** Drain to substrate leakage for a low doped drain as a function of $V_{side}$. Area ~ 6 μm$^2$, perimeter ~ 18 μm. Leakage due to GIDL is not observed due to graded junctions

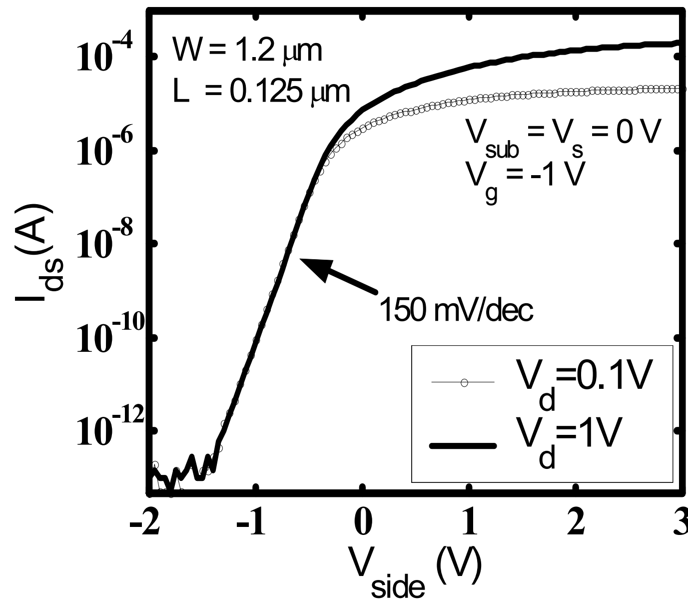


**Figure 4.16** Drain to source off current of a side-gated FET as a function of $V_{side}$. $W_{eff}$ = 1.2 μm, $L_{eff}$ = 0.125 μm.

### 4.4.2 Drain to source leakage

The sidewalls of the Si active area form transistors between the source and the drain. The current level along these sidewalls depends on the $V_t$ at the interfaces, which is a strong function of fixed charge density. In the side-gated geometry, the side-wall transistor behavior can be observed clearly by varying the side-gate potential and monitoring the source-drain current (Figure 4.16). The case without side-gates, as described in chapter 2, is equivalent to $V_{side}$ = 0 V case, which corresponds to inversion of the side-wall surfaces for the measured device in Figure 4.16. This negative threshold voltage due to interface fixed charges explains the high level of source-drain leakage observed in the preliminary devices (Figure 1.14). Drain to source leakage currents are significantly suppressed by applying a negative $V_{side}$ as the Si-STI interfaces are turned off.

### 4.4.3 Side-gated tri-gate MOSFET

The channel potential in tri-gate geometry is predominantly controlled by the top-gate as illustrated in section 4.2.2. In these structures, side-gates can be used to suppress the leakage currents. The side-gate potential does not have a significant effect on other device characteristics. Subthreshold slope of the long channel tri-gate FETs are slightly worse than comparable gate length wide planar devices, possibly due to corner effects. However, they retain a subthreshold slope of approximately 80 mV/dec. even at shorter gate lengths.

Device response gradually changes depending on the amount of side-gate recess and top-gate wrap over the active area. In extreme cases, where the side-gates are significantly recessed, $V_{side}$ only effects the leakage currents and has very small impact on $V_t$, $g_m$, DIBL or subthreshold slope (Figure 4.17). Devices presented in the following sections are expected to have very small amount of side-gate recess, if at all.

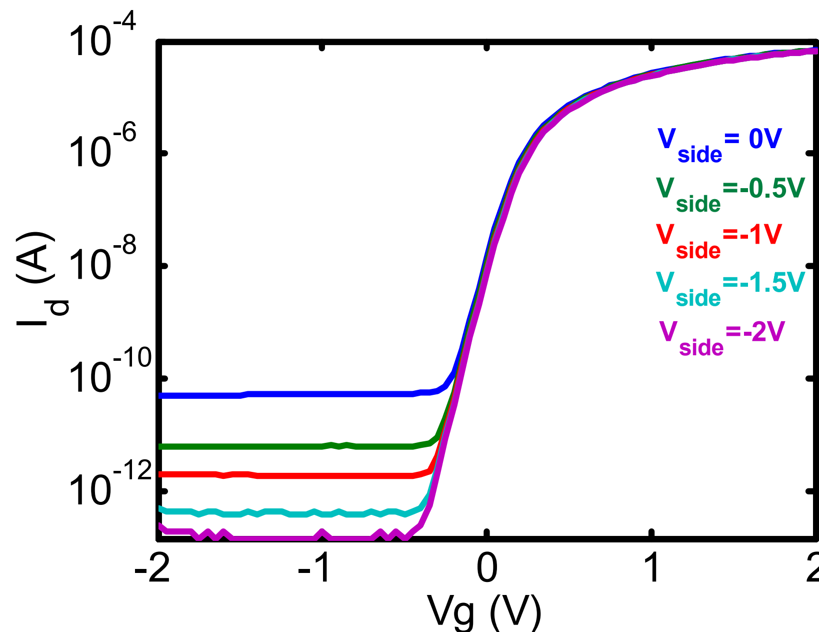


**Figure 4.17** Transfer characteristics of a side-gated tri-gate FET. W x L ~ 0.2 μm x 0.3 μm, $t_{ox}$ =7 nm. $V_{side}$ effectively lowers drain-to-substrate leakage but does not have a visible effect on $V_t$.

### 4.4.4 Side-gated wide MOSFET

In the case of wide devices, where the device width is larger than 200 nm, the top topography at the device edges has a small contribution. Wide planar devices behave similar to tri-gate structures with minimal threshold voltage response to the side-gate bias. These devices respond to the substrate bias as standard planar bulk transistors.

In this section, detailed analysis of experimental current-voltage characteristics of a W x L = 0.6 μm x 0.3 μm device with $t_{ox}$ = 4.0 nm is presented. Transfer characteristics, achieved by averaging 10 traces, show a subthreshold slope (SS) of 68 mV/dec. and DIBL of 3 mV/V, suggesting that the device is behaving as a long-channel device for $V_{sub}$ = 0 V and $V_{side}$ = -1.5 V (Figure 4.18). The measured off-current of the device is suppressed down to approximately 5 fA, which is limited by

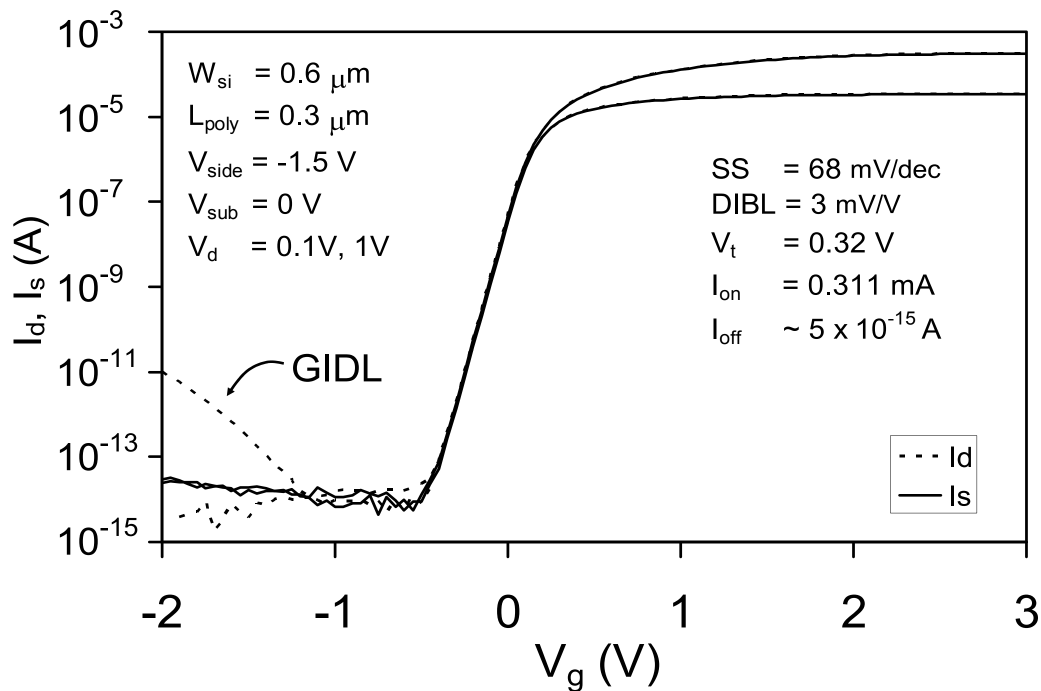


**Figure 4.18** Transfer characteristics of a W x L = 0.6 μm x 0.3 μm device. Sub-10 fA current resolution is achieved through repeated measurements. $I_{on}/I_{off} > 6 \times 10^{10}$

cable leakage in the measurement setup. The measurement of off-current at this level is made possible by the ambient noise being higher than the equipment resolution of 50 fA (see chapter 5 for the details of the measurement technique). Increase in the drain to substrate GIDL is visible for $V_g < -1.1$ V. The drive current of the transistor is 0.311 mA at $V_d = 1$ V, corresponding to approximately 0.5 mA/µm. The drive current increases to a saturation value of 0.525 mA for $V_g = 3$ V, corresponding to 0.875 mA/µm (Figure 4.19).

The output characteristics of the device are shown as a function of the applied drain bias and as a function of the actual potential drop across the intrinsic device by accounting for the resistive drop across the contact resistances.

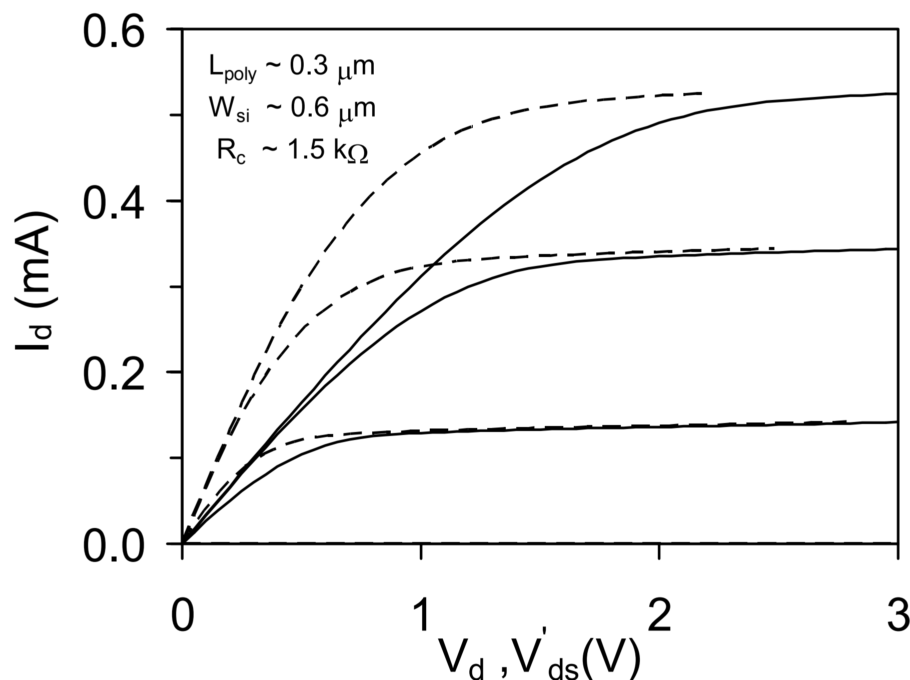


**Figure 4.19** $I_d$ as a function of applied drain bias ($V_d$) (solid), and potential drop across the source and drain ($V'_{ds}$) accounting for contact resistance ($R_c$) (dashed). W x L = 0.6 µm x 0.3 µm .

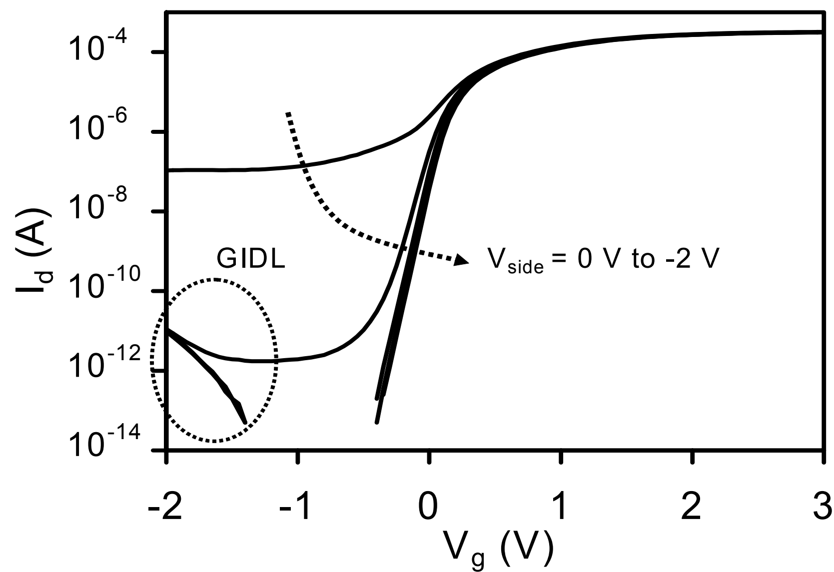


**Figure 4.20** Transfer characteristics of wide & long device for different $V_{side}$ . W x L = 0.6 μm x 0.3 μm.

As the side-gate potential is varied, the transfer characteristics change significantly in the $V_{side}$ = 0 to -1 V range (Figure 4.20). The changes in the subthreshold transfer characteristics saturate as the side-channels at the Si-STI interfaces are turned off. The saturation in the SS and the DIBL are clearly observed as these values are plotted as a function of $V_{side}$ (Figure 4.22). The saturation value for subthreshold slope is 67.7 mV/dec.

The values for DIBL plotted in Figure 4.22 are higher than what is seen in Figure 4.18. Data in Figure 4.18 was obtained from later repeated measurements performed on the same device. Slight changes in the device characteristics are observed after the devices are stressed during long measurements. In this case, the DIBL seems to be slightly improved after stressing.

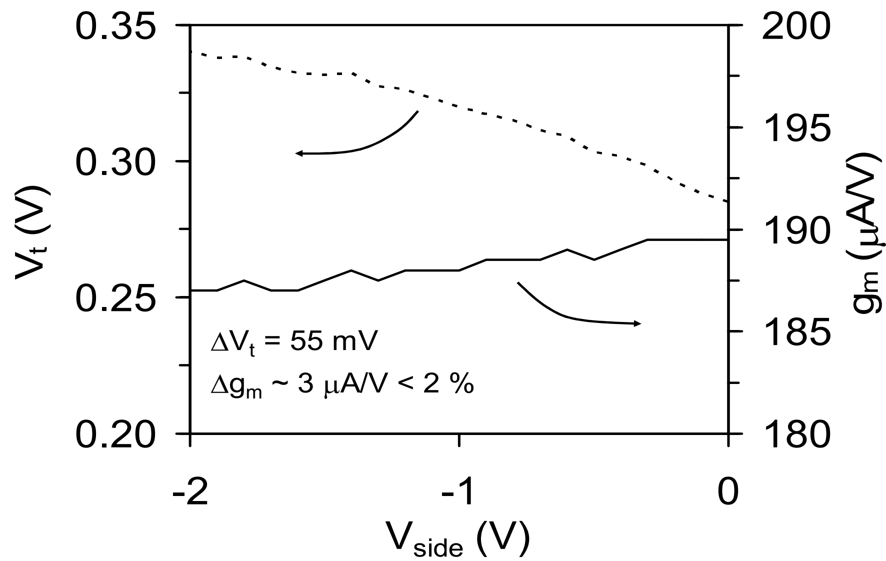


**Figure 4.21** Threshold voltage and maximum transconductance response to $V_{side}$ for $V_{sub}$ = 0 V. W x L = 0.6 μm x 0.3 μm.

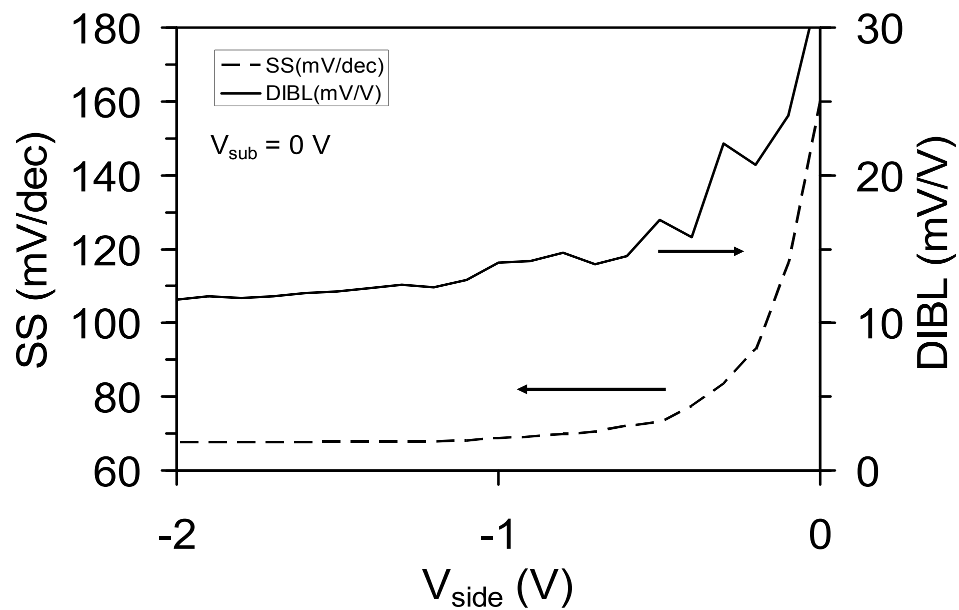


**Figure 4.22** Subthreshold slope and DIBL as a function of $V_{side}$ for $V_{sub}$ = 0 V. W x L = 0.6 μm x 0.3 μm.

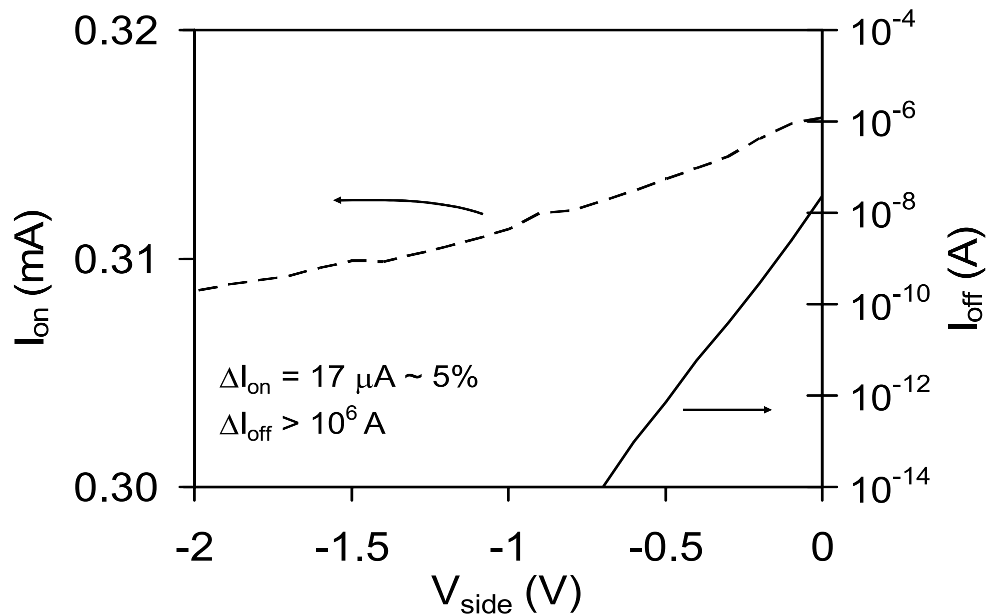


**Figure 4.23** Variation in $I_{on}$ and $I_{off}$ as a function of $V_{side}$ for $V_{sub}$ = 0 V. W x L = 0.6 μm x 0.3 μm.

The variation in the threshold voltage is 55 mV for $V_{side}$ = 0 V to -2 V range. Change in the maximum transconductance is less than 2 % within the same range (Figure 4.21). The off currents are suppressed by a factor larger than $10^6$ while the degradation in the on current is approximately 5 % (Figure 4.23).

Reduction in the substrate bias widens the depletion depth which results in improved subthreshold slope [21]. A negative substrate bias applied to this device is observed to improve the subthreshold slope down to 65 mV/dec (Figure 4.24). As the substrate bias is lowered below -1.4 V, band-to-band tunneling in source-to-substrate and drain-to-substrate diodes become observable in the I-V characteristics.

Drain induced barrier lowering is observed to degrade slightly as the negative substrate bias is increased (Figure 4.24). This is due to the widened drain depletion, increasing the relative contribution of the drain potential on the channel potential aggravating the short channel effects [21]. In the wide channel case, this brings up a compromise between the increased short channel effects and improved subthreshold

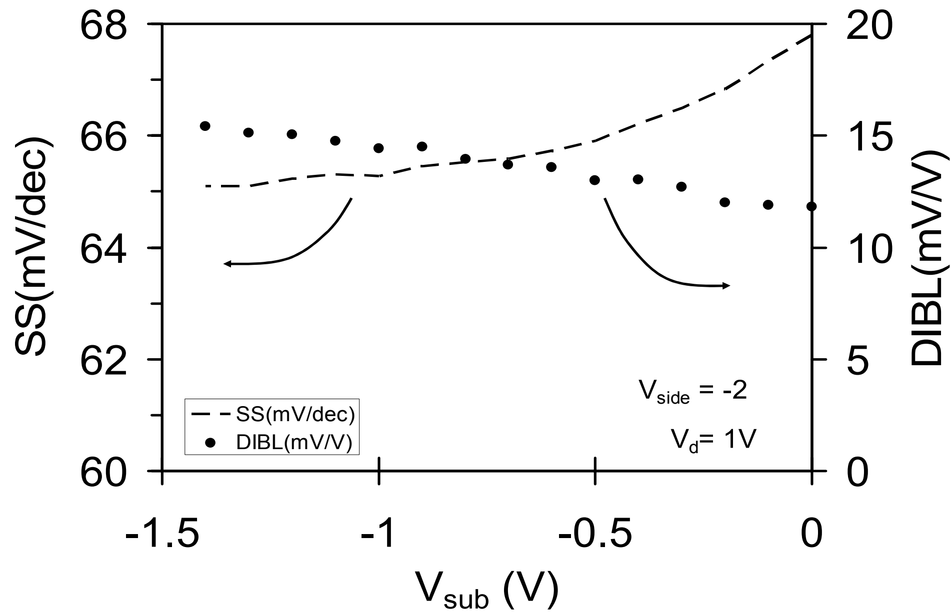


**Figure 4.24** Subthreshold slope and DIBL as a function of substrate bias for $V_{side}$ = -1.5 V W x L = 0.6 μm x 0.3 μm.

slope. An advantage of the increased depletion depth is the reduction in the junction capacitances. In the case of the narrow channel devices, which will be discussed in the following sections, a negative substrate bias can be used to reduce junction capacitances in the large contact areas of the device without any increase in the short channel effects due to the extreme control of the side-gates on the narrow body of the device.

The threshold voltage of the device is observed to change by 82 mV in the $V_{sub}$ = 0 to -1.5 V range. The maximum transconductance shows almost no response to the substrate bias (Figure 4.25).

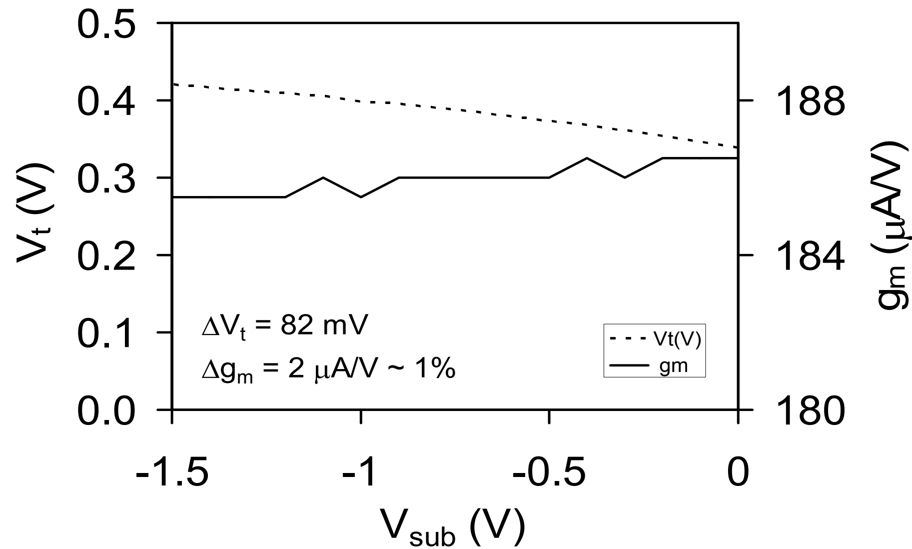


**Figure 4.25** Threshold voltage and maximum transconductance response to the substrate bias for $V_{side}$ = -1.5 V. W x L = 0.6 μm x 0.3 μm.

### 4.4.5 Side-gated narrow channel MOSFET

The fin width of narrow channel MOSFET structures are comparable to the finFET and tri-gate structures in the literature [45][50]. The active area width, in the order of 20 nm, is very sensitive to process variations. In order to properly characterize these devices a capacitance measurement technique is developed to measure the inversion layer capacitances down to sub 0.1 fF range (chapter 5).

In this section the characteristics of a device with approximately 150 nm gate length is demonstrated. The device gate length is estimated from SEM micrographs of a twin device in a different die, 2 cm away on the same wafer (Figure 4.26). The active area of the structure analyzed with SEM did not complete the process as intended. Existence of side-gate polysilicon structures suggest that the active area exists slightly below the surface, but parts of it were broken on the very tip, prior to side-gate polysilicon deposition. The active area could be exposed as a continuous surface if the CMP process was slightly extended. The twin structure analyzed in this section has survived the process as it is observed from the electrical characteristics.

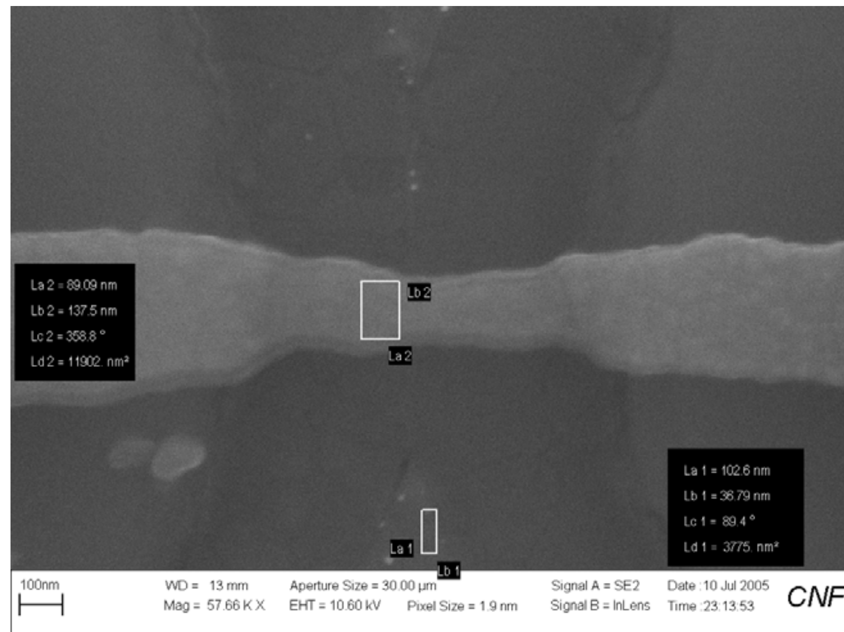


**Figure 4.26** SEM micrograph of a twin device of the one analyzed in this section. In this device, the active area, expected to be ~ 10 nm wide, is not continuous. Gate length is approximately 150 nm.

The effective device width of the electrically characterized device is estimated to be around 40 nm from the inversion layer capacitance measurements amounting to approximately 50 aF (Figure 4.27 inset).

In this device, with $L_{poly}$ ~ 150 nm, subthreshold slope is observed to be 83 mV/dec. and DIBL is approximately 2 mV/V for $V_{side}$ = -1.5 V, $V_{sub}$ = 0 V (Figure 4.27). The extreme low value of the DIBL suggests that the source-drain potential barrier is practically immune to the changes in the drain bias. The subthreshold slope, 83 mV/dec, is slightly worse than 68 mV/dec measured in the wide device with $V_{sub}$ = 0 V. This is possibly due to reduced depletion depth due to the negative side-gate potential, larger channel to side-gate capacitance and to the threshold voltage variation along the width of the device due to corner effects. This threshold voltage variation is due to termination of a larger flux of electric field at the corners resulting in inversion of the corners earlier than the planar sections.

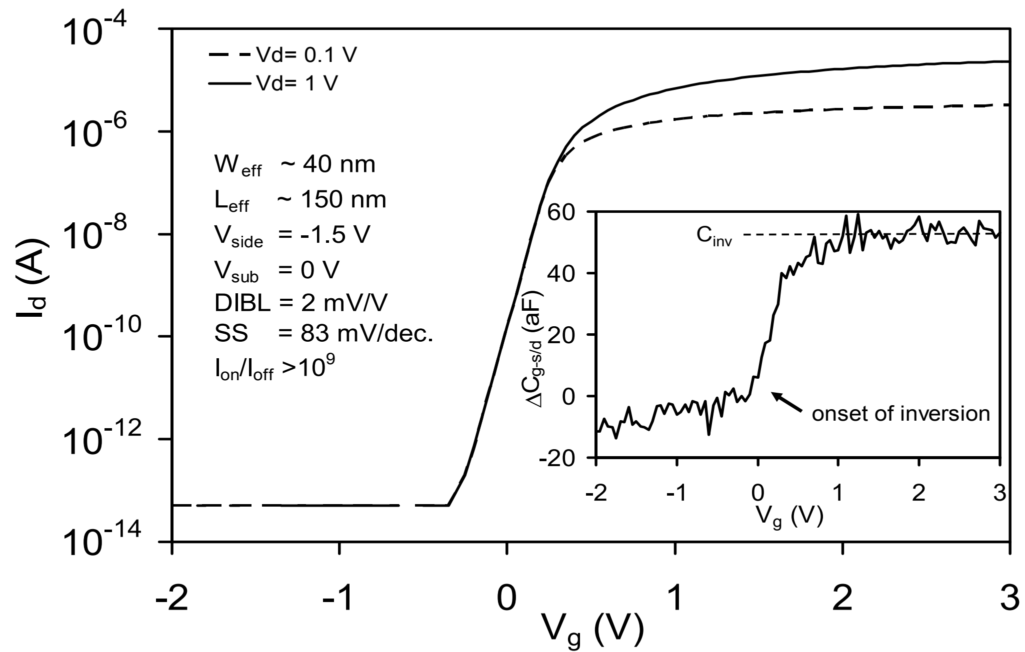


**Figure 4.27** Transfer and C-V (inset) characteristics of a narrow channel d channel device. Effective device width is estimated from the C-V characteristics.

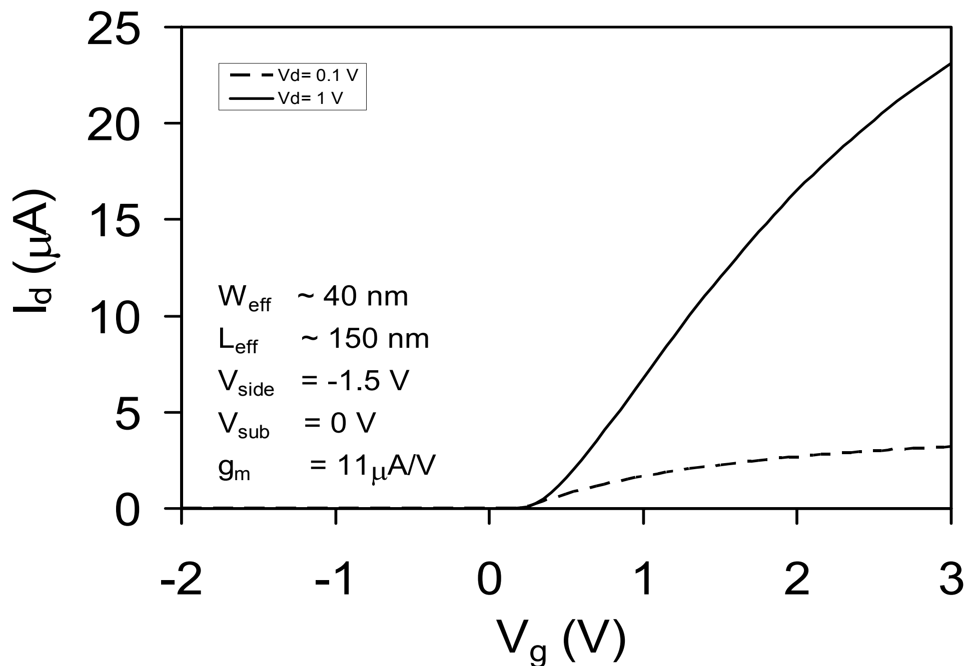


**Figure 4.28** Transfer characteristics in linear scale for $V_d$ = 0.1 V and 1 V.

The DIBL observed in the narrower and shorter channel device is smaller than of the wider and longer channel device. This shows that the effect of the negatively biased side-gates is very pronounced when the effective device width is in the order of 40 nm. The accumulation of the interfaces with holes effectively isolates the source and drain depletion regions at this device width. Current conduction is significantly confined to the top interface, DIBL and punch through is prevented.

Since this device geometry does not display any sign of short channel effect even at 150 nm gate length, it is possible to further scale the gate length of narrow channel side-gated FETs compared to wide devices, before running into limitations due to short channel effects.

The transfer characteristics show that this device is fully turning off, with $I_{off}$ < 50 fA (HP 4145B current resolution) and turning on with 23 μA, leading to an $I_{on}/I_{off}$ ratio of $10^9$ or better (Figure 4.28) for $V_d$ = 1 V. Transfer characteristics for different

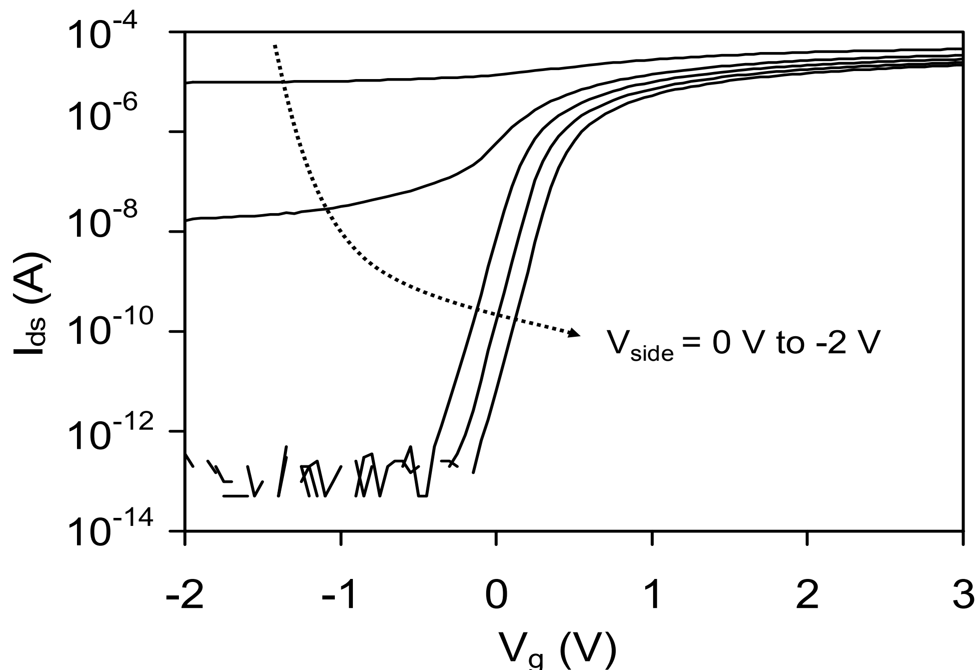


**Figure 4.29** Transfer characteristics of a narrow device for different $V_{side}$ . W x L ~ 40 nm x 150 nm.

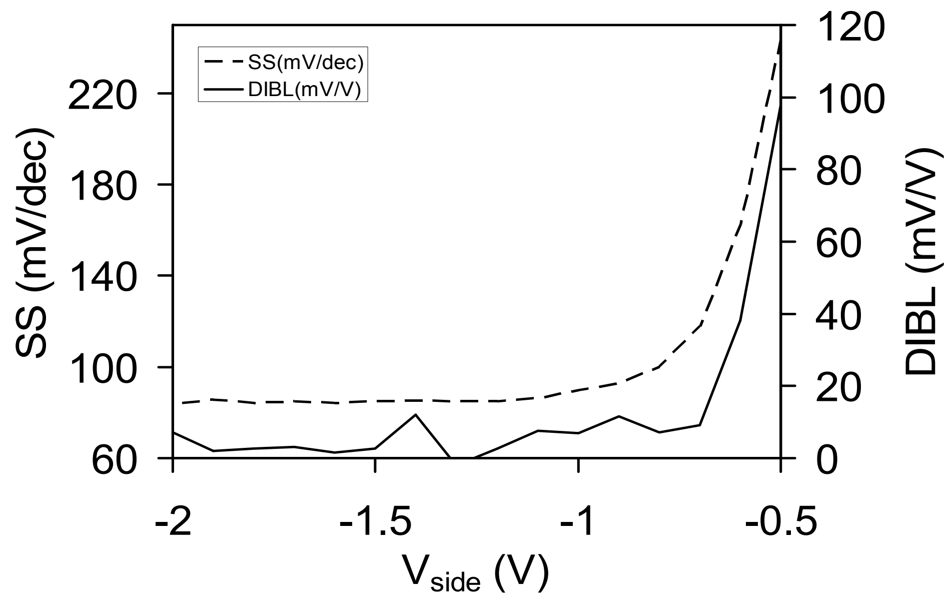


**Figure 4.30** Subthreshold slope and DIBL as a function of $V_{side}$ for $V_{sub}$ = 0 V. W x L ~ 40 nm x 150 nm.

side-gate biases show that the interface related leakage is turned off within the $V_{side}$ = 0 to -1 V range and threshold voltage continues to shift as the negative side-gate bias is increased (Figure 4.29). Similarly subthreshold slope and DIBL improves significantly as negative $V_{side}$ is increased. Subthreshold slope saturates around 80 mV/dec and DIBL saturates around 2 mV/V (Figure 4.30).

Output characteristics show that the drive current starts saturating around 33 μA for $V_g$ = 3 V, 75 % of gate oxide breakdown field and $V_{side}$ = -1.5 V, and around 43 μA for $V_g$ = 3 V and $V_{side}$ = 0.5 V (Figure 4.31). These drive currents correspond to approximately 1 mA/μm for $V_{side}$ = -0.5 V and 0.83 mA/μm for $V_{side}$ = -1.5 V.

Output conductance values calculated for 3 different side-gate biases do not show any distinctive response to side-gate bias (Figure 4.32).

With the application of a negative side-gate bias, $I_{off}$ is improved by $10^6$ and the $I_{on}$ is degraded by 30 % (Figure 4.33).

While the subthreshold slope and DIBL saturate for $V_{side} < -1.2$ V (Figure 4.30), the threshold voltage of the device changes by 0.39 V in the range of $V_{side}$ = -0.5 to -2 V (Figure 4.34). Maximum transconductance is degraded by 30 % in the same range. The degradation in the transconductance is partially due to degradation in the carrier mobility due to high field effects and partially due to the reduction in the carrier concentration at the fringes of the inversion layer.

$V_t$, $g_m$ and subthreshold slope does not show noticeable response to the substrate bias, slight degradation in DIBL is observed (Figure 4.35, Figure 4.36). The potential in the channel is predominantly controlled by the side-gates and the top-gate. Device characteristics are fairly immune to the changes in the body potential, suggesting that the device is suitable for mixed signal applications where the substrate coupling noise is a significant concern [53].

These narrow channel device characteristics clearly show that the device length can be significantly scaled down if the channel width is kept small. This advantage makes the narrow channel side-gated device very attractive for high density low-power applications. The increase in the device capacitance due to the additional side-gate capacitance maybe compensated by this performance increase in short channel devices for very low level of off currents and DIBL. A short channel device is discussed in the next section. The performance characteristics of this short channel device are very significant. However, the width of the short channel device in the next section is larger than 50 nm, which is not fully utilizing the effect of the side-gates for the suppression of short channel effects.

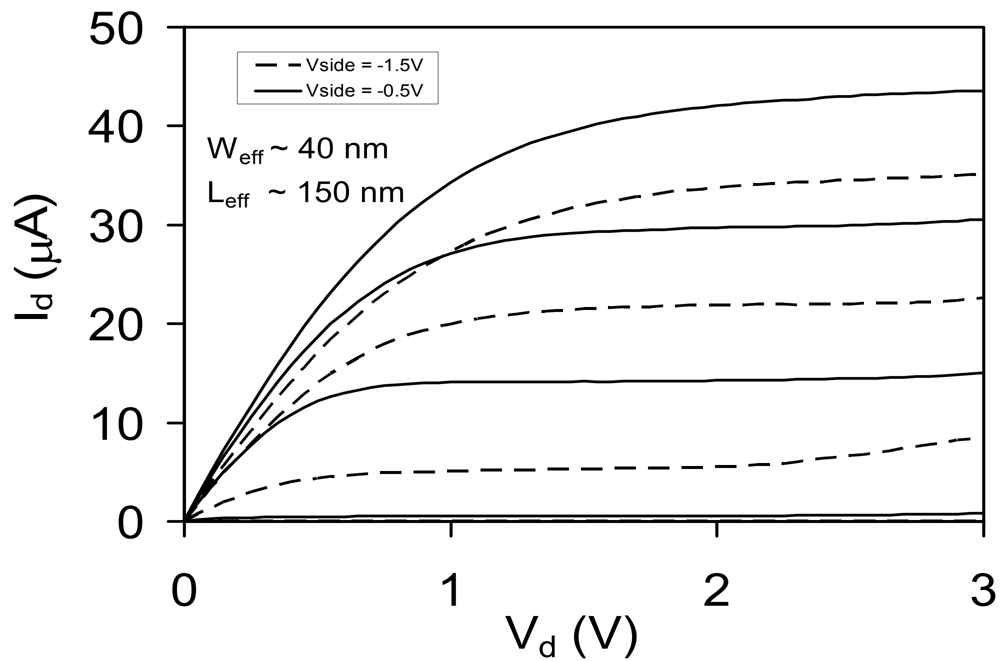


**Figure 4.31** Transfer characteristics of narrow channel side-gated FET.

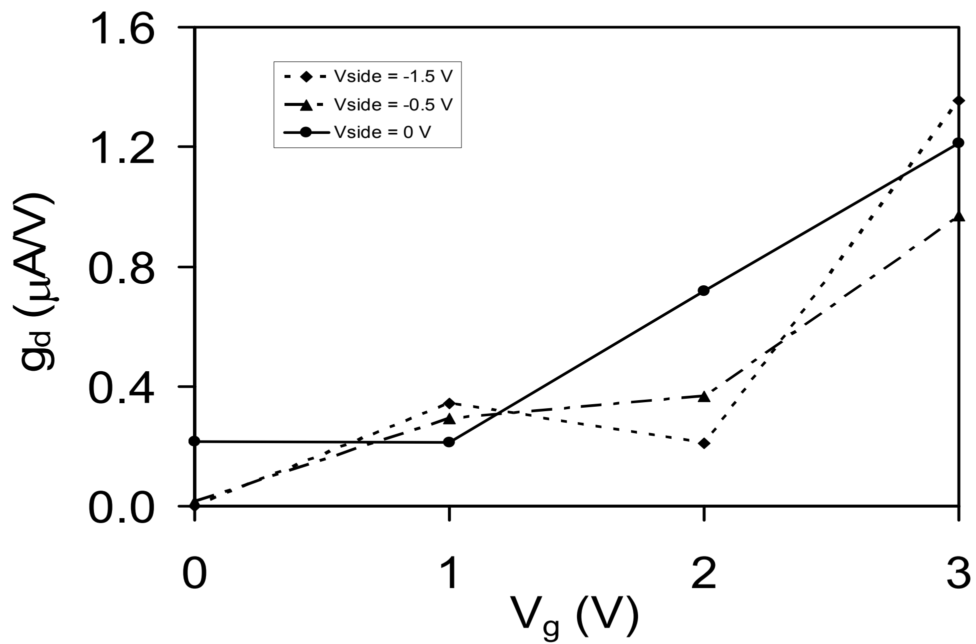


**Figure 4.32** Output conductance of narrow channel side-gated FET for different side-gate biases (W x L ~ 40 nm x 150 nm).

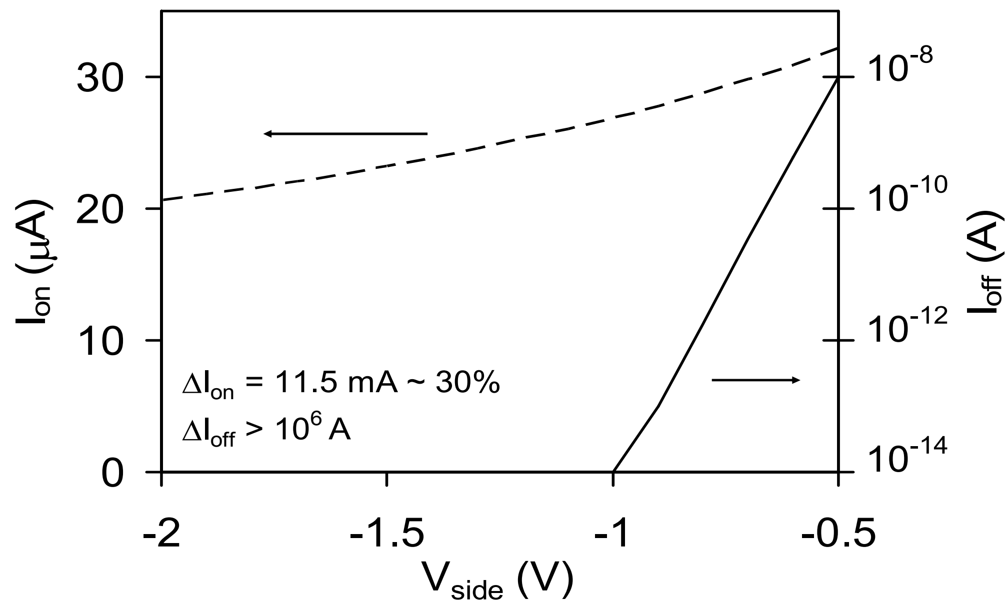


**Figure 4.33** Variation in $I_{on}$ and $I_{off}$ as a function of $V_{side}$ for $V_{sub}$ = 0 V. W x L ~ 40 nm x 150 nm.

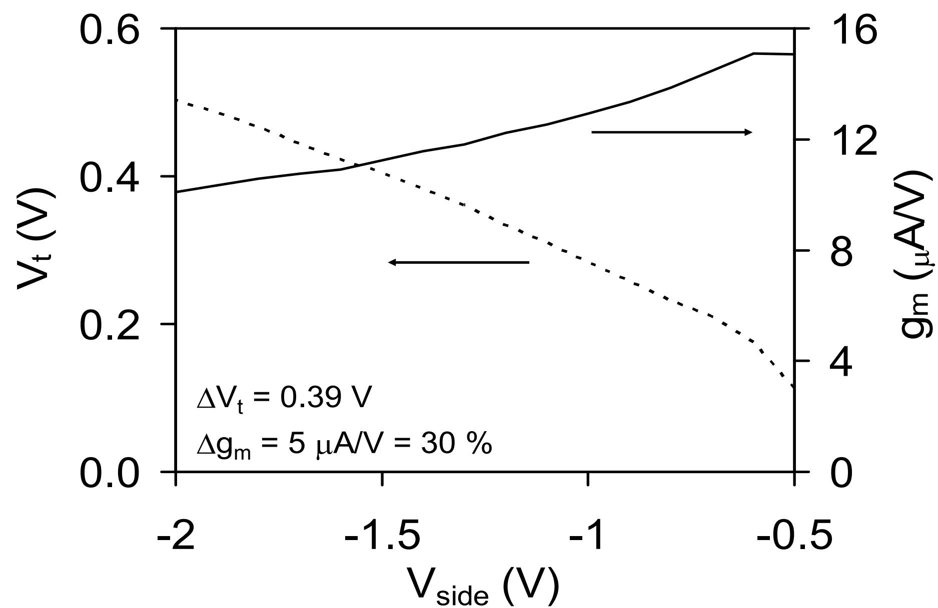


**Figure 4.34** Threshold voltage and maximum transconductance response to $V_{side}$ for $V_{sub}$ = 0 V. W x L ~ 40 nm x 150 nm.

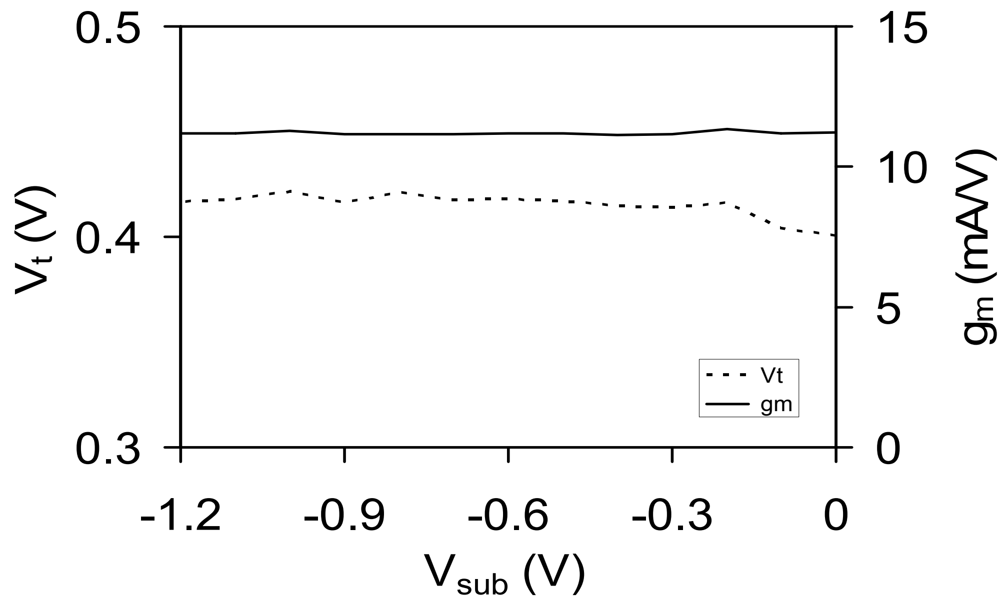


**Figure 4.35** Threshold voltage and maximum transconductance response to $V_{sub}$ for $V_{side}$ = -1.5 V. W x L ~ 40 nm x 150 nm.

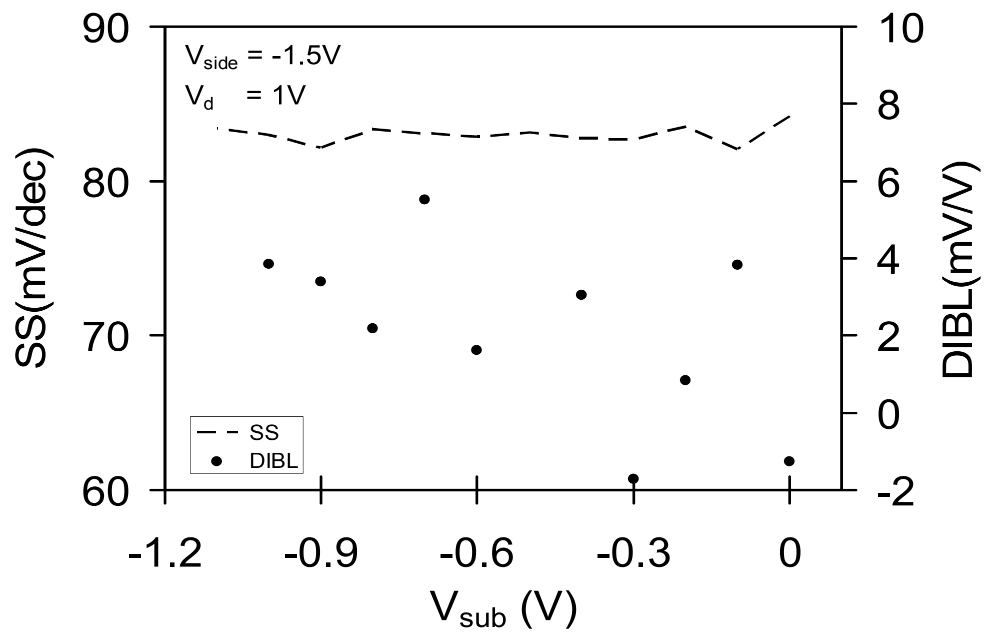


**Figure 4.36** Subthreshold slope and DIBL as a function of $V_{sub}$ for $V_{side}$ = -1.5 V. W x L ~ 40 nm x 150 nm.

### 4.4.6 Side-gated short-channel MOSFET

Preliminary measurements on the short channel device seen in Figure 4.37 have been performed prior to removing the passivation oxide and the metal in order to image the device with SEM. The device seen in the SEM image was not annealed after metal deposition step, hence its performance is expected to be worse than the twin device extensively analyzed in this section. The physical device dimensions were measured to be W x L = 78 nm x 68 nm as viewed from the top.

This short channel device (seen in the SEM) shows the best subthreshold slope and DIBL for $V_{side}$ = -3 V and $V_{sub}$ = -1.2 V as SS = 104 mV/dec and DIBL = 165 mV/V (Figure 4.38). The device characteristics significantly improve as a function of

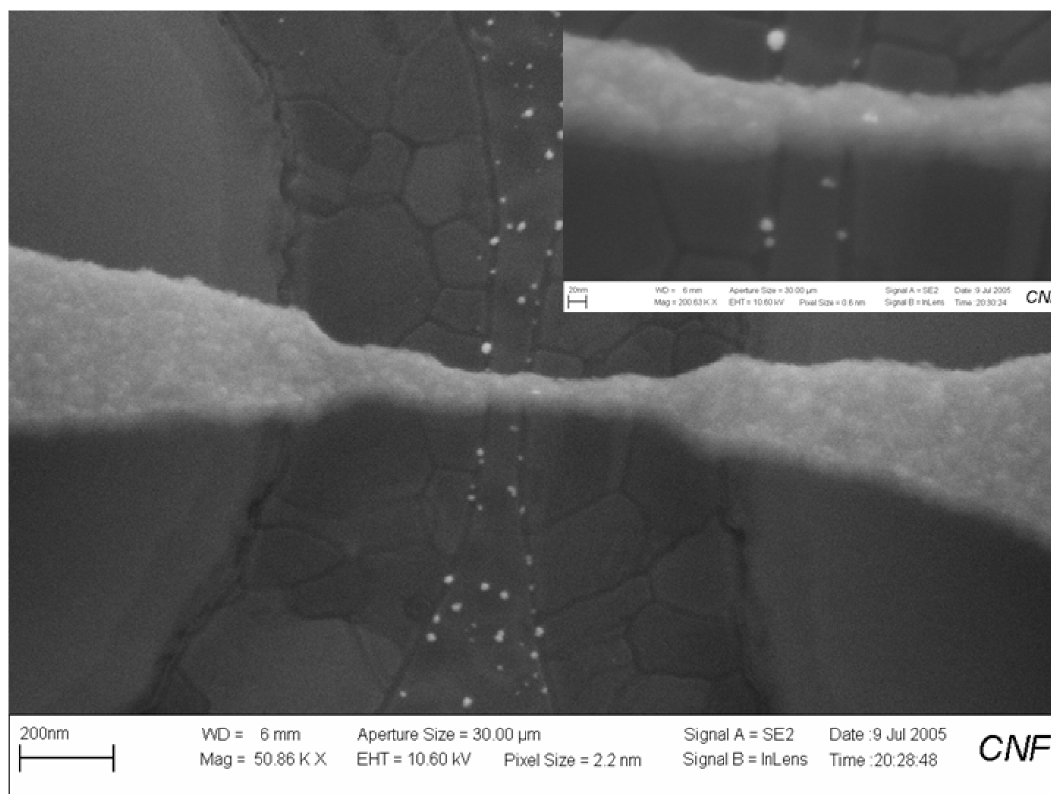


**Figure 4.37** SEM micrograph of a narrow and short channel side-gated FET (35° tilt). Image is taken after removing the passivation layer and metal after preliminary electrical testing. The single crystal silicon channel is straddled with polysilicon side-gates. Gate length is measured to be 68 nm (when imaged at 0° tilt).

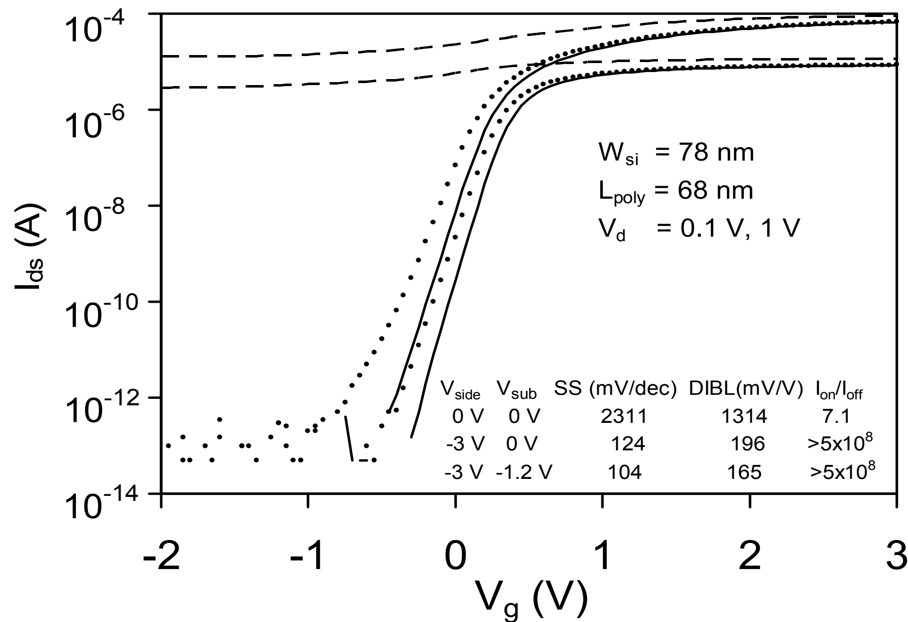


**Figure 4.38** Transfer characteristics of W x L = 78 nm x 68 nm device seen in Figure 4.37 for $V_{side} = V_{sub} = 0$ V (dashed), $V_{side} = -3$ V, $V_{sub} = 0$ V (dot), $V_{side} = -3$ V, $V_{sub} = -1.2$ V (solid).

the increased negative side-gate bias. This device also responds to the substrate bias, indicating that the channel potential for this device is partially controlled by the substrate. The $I_{on}$ for $V_d = 1$ V, $V_g = 3$ V is 66.6 μA, corresponding to 0.85 mA/μm.

The rest of the measurement results presented in this section are performed on a twin device on a different die 2 cm away which contains all the measured FETs mentioned in section 4.4 . This die is annealed in forming gas as described in the section on fabrication process.

The capacitance measurements performed on this twin device suggest that the effective width is approximately 150 nm (Figure 4.39 inset). The difference between the estimated effective width and the width measured using SEM can be partially accounted for the physical size difference between the two devices due to process variations. This variation is not expected to account for more than 20 nm of variation. The second factor is the difference in the recess of the side-gates, which can be up to

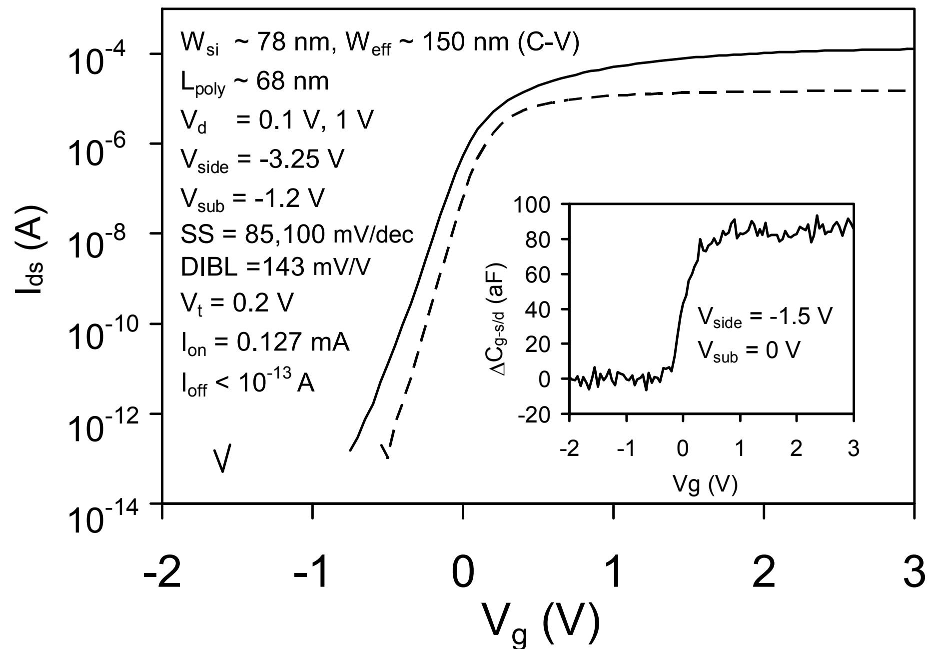


**Figure 4.39** Transfer and C-V (inset) characteristics of a short channel side-gated FET.

30 nm resulting in an effective surface width change of approximately 60 nm. The third factor for the increase in the capacitance is expected to be the geometrical factor due to the corners of the structure and the top-gate wrapping over the body.

The current drive of the device corresponds to 0.85 mA/μm, for effective width extracted from C-V characteristics, at $V_d$ =1 V, $V_{side}$ = -3.25 V (Figure 4.39, Figure 4.40). Output characteristics show that the saturation current density for $V_g$ = 3 V and $V'_{ds}$ = 1.7 V corresponds to approximately 1.5 mA/μm of $W_{eff}$, which is a substantial amount of current in the industrial standards for silicon MOSFETs. Due to approximately 5.4 kΩ source/drain contact resistance, a source-to-drain potential, $V'_{ds}$ = 1.7 V is achieved if the terminals are supplied with $V_{ds}$ = 3 V. The drain current as a function of applied source drain bias (solid lines) and as a function of actual source-to-drain potential drop is shown in Figure 4.41. Avalanche breakdown of the device is observable for $V'_{ds}$ > 1.9 V.

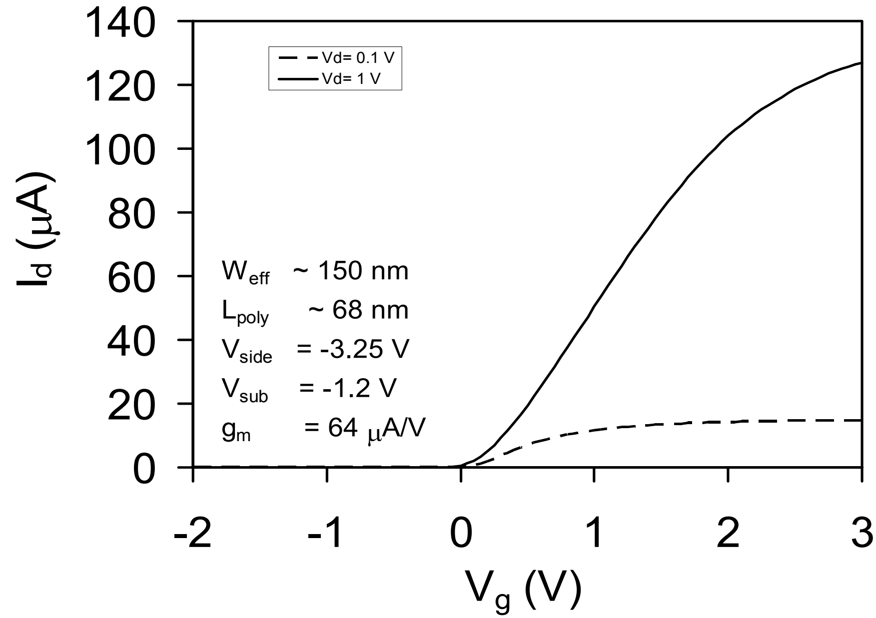


**Figure 4.40** Transfer characteristics of a short channel side-gated FET.

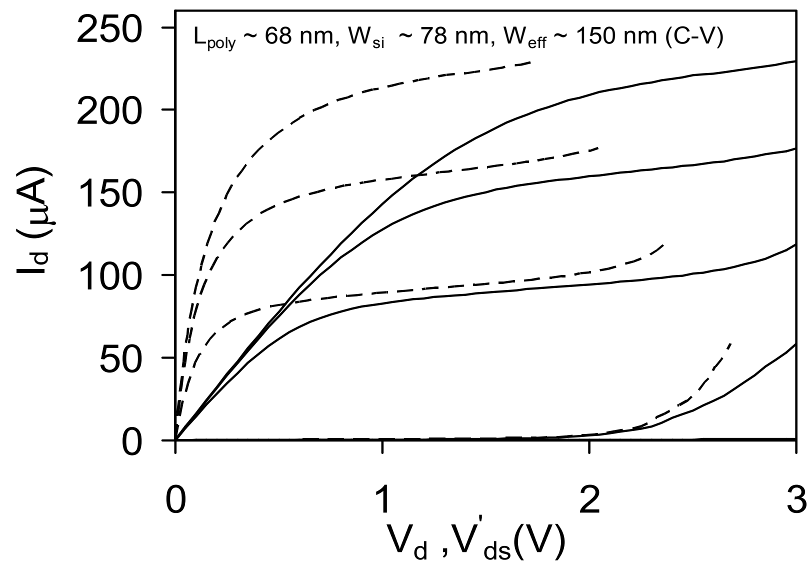


**Figure 4.41** Drain current of short channel side-gated FET as a function of applied drain bias ($V_d$) (solid) & actual source-drain potential ($V'_{ds}$) (dashed), $V_{side}$ = -3.25 V.

The best subthreshold slope for this device is measured to be 100 mV/dec and best DIBL = 143 mV/V with $V_{side}$ = -3.25 V, $V_{sub}$ = -1.2 V.

The peak value for transconductance of the device is not affected by the substrate bias and the threshold voltage changes by only 26 mV in the range of $V_{sub}$ = 0 to -1.5 V for $V_{side}$ = -2 V (Figure 4.42).

Subthreshold slope goes down to slightly below 180 mV/dec from 250 mV/dec as a negative substrate bias is applied with $V_{side}$ = -2 V. No change in SS observed in the case of $V_{side}$ = -3 V beyond $V_{sub}$ = -0.2 V (Figure 4.43). Similarly, DIBL is not sensitive to substrate bias in the same range for $V_{side}$ = -3 V. This shows that substrate bias does not have an appreciable effect on the channel potential in the case of large negative side-gate biases.

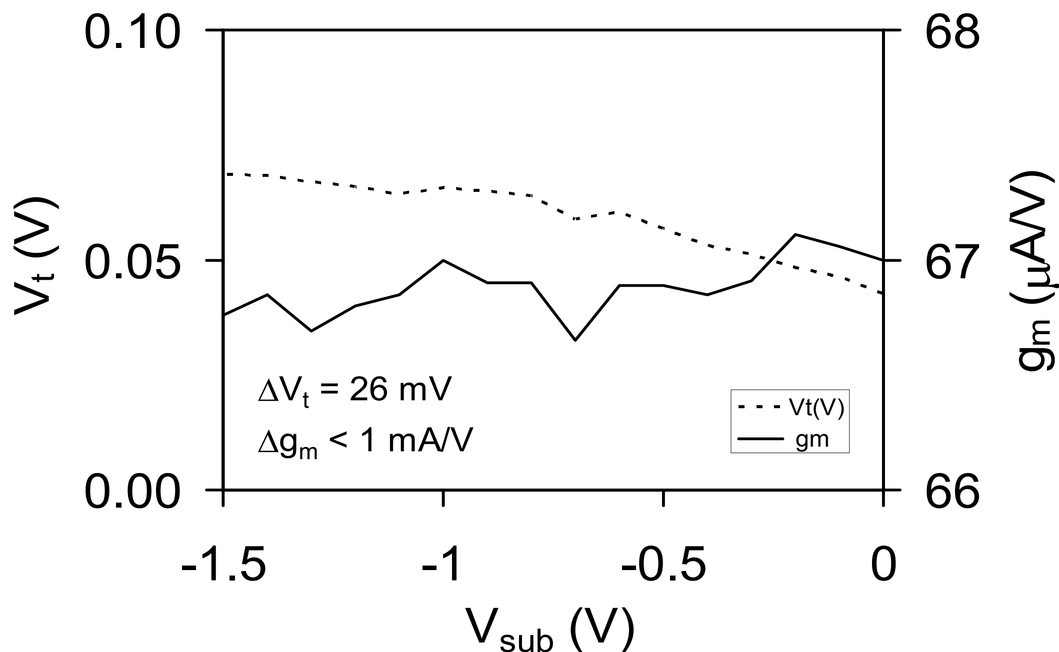


**Figure 4.42** Threshold voltage and maximum transconductance response to $V_{sub}$, $V_{side}$ = -2 V of short channel side-gated FET.

The change in the threshold voltage changes slope around $V_{side} = V_{sub}$ and maximum transconductance peaks around the same point (Figure 4.44).

Subthreshold slope and DIBL improve for larger side-gate biases, saturating at approximately SS = 100 mV/dec, and DIBL = 150 - 200 mV/V for $V_{sub}$ = -1.2 V (Figure 4.45). For the same side-gate bias range with $V_{sub}$ = -1.2 V, $V_d$ = 1 V, $I_{on}$ degrades by 20 % while the suppression in the $I_{off}$ is in the order of $10^9$ with the increased negative side-gate bias (Figure 4.46).

Significantly high current drive of the device for its physical size is mainly due to the carrier density in the channel as extracted from the gate to source/drain C-V measurements performed on the device Effective electron mobility ($\mu_{eff}$), extracted from the I-V and C-V measurements performed on this device, is calculated to be 208 $cm^2$/V.s in the high field regime for approximately 7.5 MV/cm across the gate oxide (Figure 4.47). This value is comparable to high-field effective electron mobility in standard silicon MOSFETs. The calculated mobility value is very sensitive to the errors in gate length estimation at this device scale. An error of 10 nm in the effective device length estimation results in approximately 14 % error in the calculated value for $\mu_{eff}$.

The drive current of the transistor, approximately 1.5 mA/μm, is calculated using the effective device width extracted from the C-V characteristics. With this drive capability and very low off currents indicate that the short channel effects can be significantly suppressed for a sub 70 nm gate length device using a side-gated approach. The short channel effects, mainly DIBL is expected to be even more suppressed for devices with sub-50 nm width.

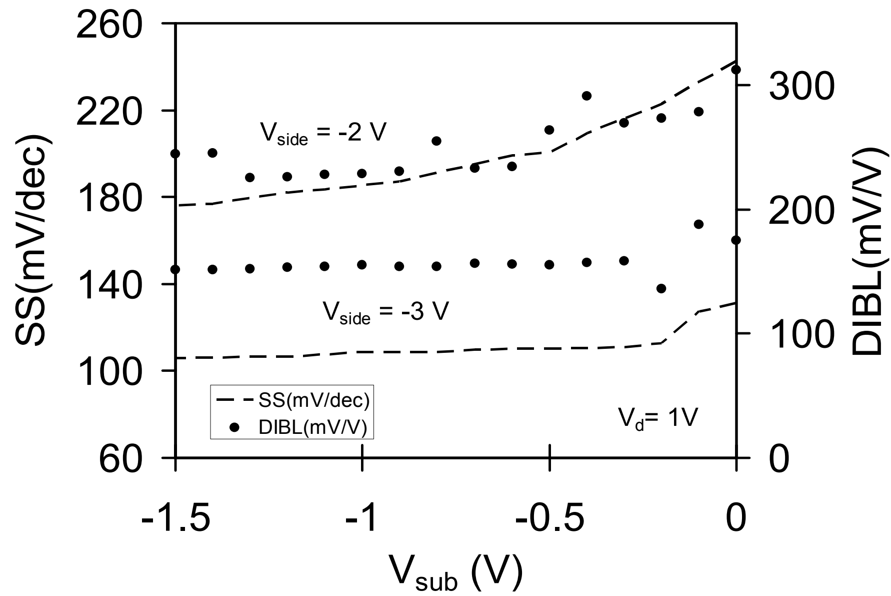


**Figure 4.43** Subthreshold slope and DIBL response to $V_{sub}$ of short channel side-gated FET for two different $V_{side}$.

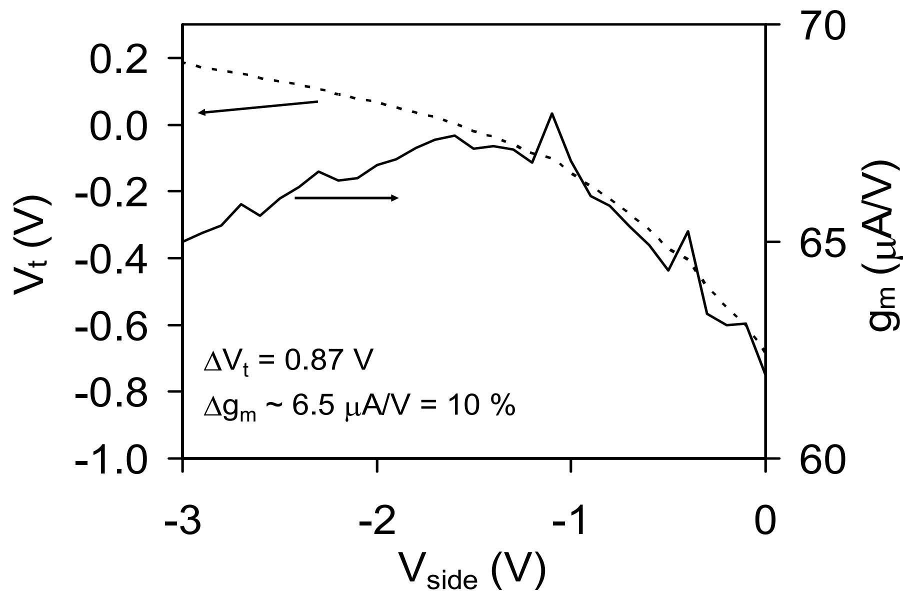


**Figure 4.44** Threshold voltage and maximum transconductance response to $V_{side}$ of short channel side-gated FET, $V_{sub}$ = -1.2 V.

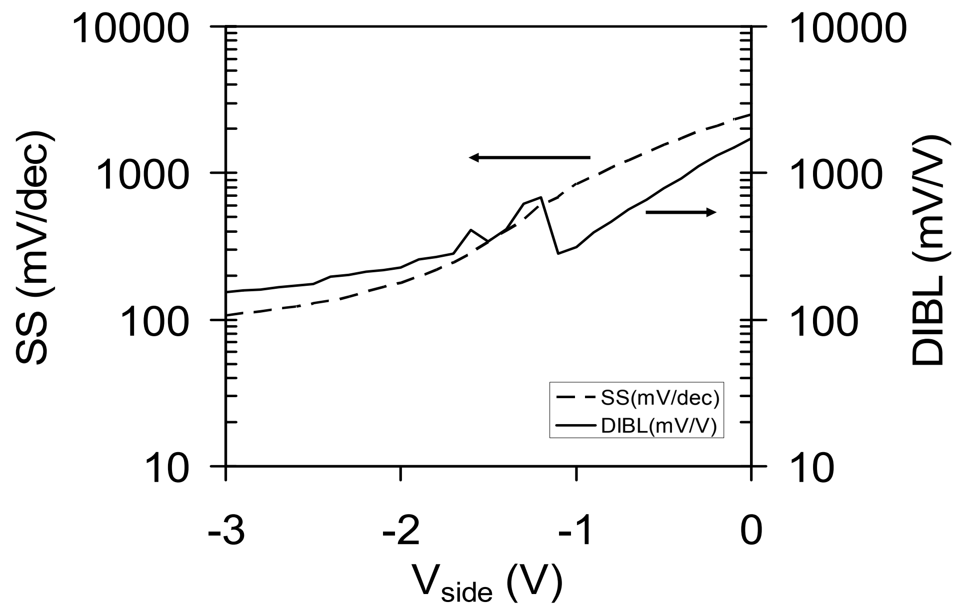


**Figure 4.45** Subthreshold slope and DIBL response to $V_{side}$ of short channel side-gated FET, $V_{sub}$ = -1.2 V.

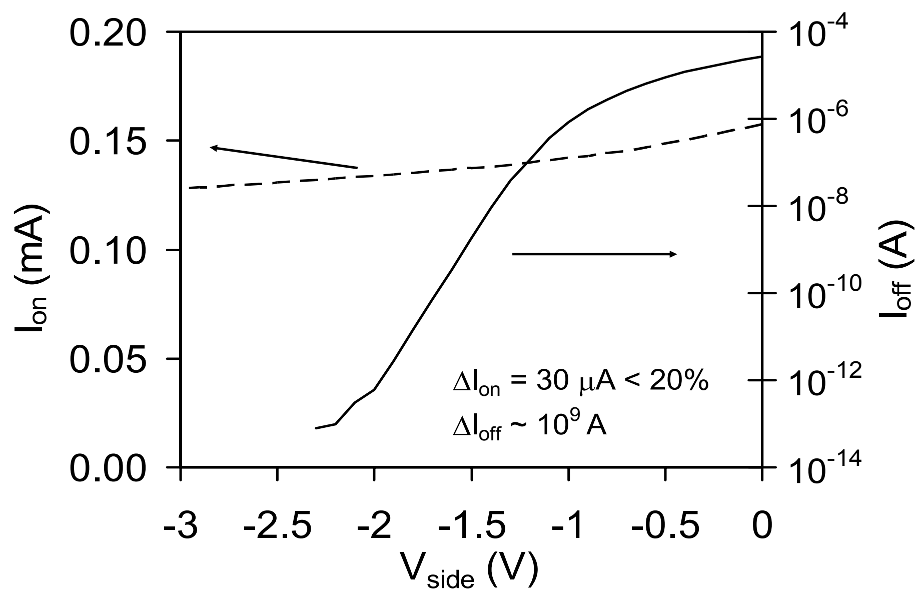


**Figure 4.46** Variation in on current and off current as a function of $V_{side}$ for short channel side-gated FET. $I_{on}$ and $I_{off}$ are maximum and minimum current levels in $V_g$ = -2 V to 3 V range for $V_d$ = 1 V.

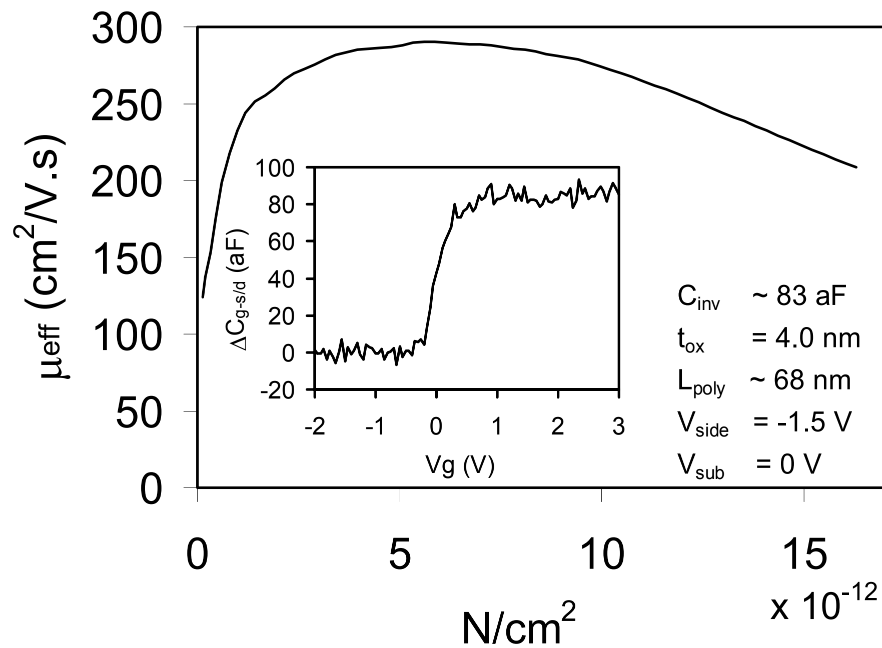


**Figure 4.47** Effective electron mobility versus carrier density for short channel side-gated FET. Inset show gate to source/drain capacitance characteristics used for mobility extraction.

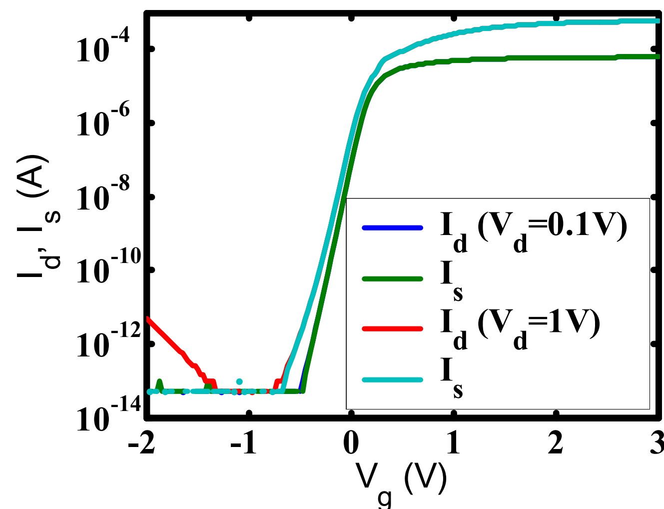


**Figure 4.48** Transfer characteristics of a $W_{eff}$ x $L_{eff}$ = 1.2 μm x 125 nm side-gated FET with $t_{ox}$ = 4.3 nm, $V_{side}$ = - 1.5 V. $V_t$ = 0.3 V, DIBL = 70 mV/V, SS = 81 mV/dec, $I_{on}$ = 0.588 mA, $I_{on}/I_{off} > 1.1 \times 10^{10}$

The improvement in the off currents, subthreshold slope and DIBL for narrow and short channel devices is not purely due to suppression of the leakage currents at the interfaces. A wide device structure with $L_{eff} \sim 125$ nm, comparable to the gate length of the device presented in section 4.4.5, exhibits more dominant short channel effects (Figure 4.48). The side-gate biases reconstruct the potential barrier between the source and the drain as discussed in section 4.2.1. However, the effect of the side-gates in narrow channel devices build on bulk substrate is expected to be more significant than what is seen in the 2D simulation results in section 4.2.1.

In a bulk FET, the gate electrode controls the electrical potential of the volume ($d_G$) below the interface between the source and drain regions (Figure 4.49). The depletion regions of source ($d_S$) and drain ($d_D$) junctions start merging and the volume controlled by the gate of the transistor ($d_G$) gets smaller as the gate length of the

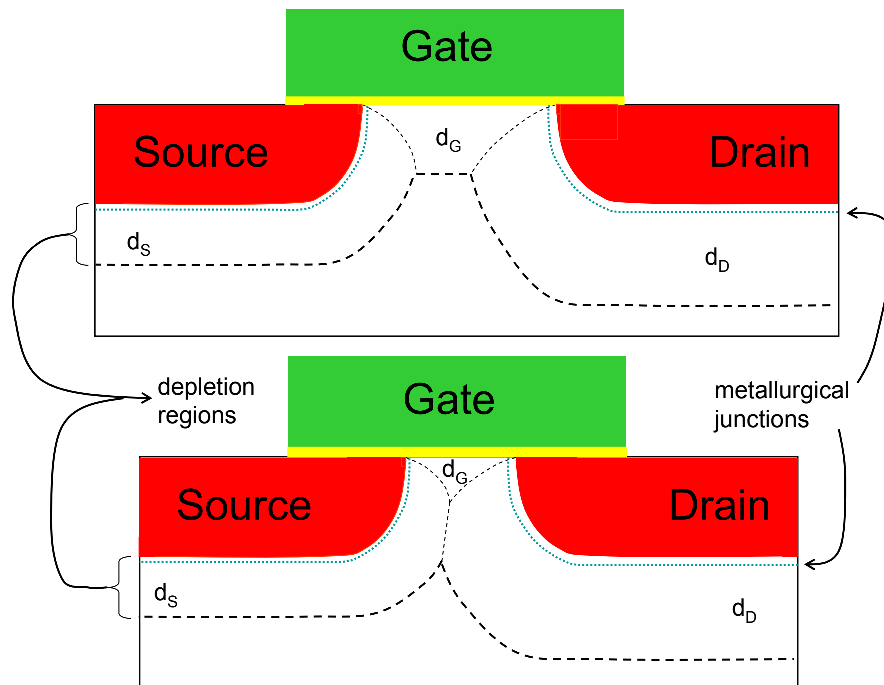


**Figure 4.49** Cross sectional schematics of a short channel bulk FET (top) and a shorter channel bulk FET (bottom). Dashed lines indicate the boundaries of depletion regions controlled by source, drain and the gate. Dotted lines indicate the metallurgical junctions.

device is scaled down, assuming that the source/drain junction depths are kept constant (Figure 4.49 bottom). The electrical potential of the depletion regions around the source and drain junctions are strongly coupled to the source/drain potentials; hence the depleted volume slightly below the gate oxide interface is no longer controlled by the gate potential. This results in short channel effects and punch through, observed as increased off currents, degraded subthreshold slope and increased DIBL.

If a negative gate bias is applied for an nFET, the area under the gate is accumulated with holes. For larger negative gate biases, the holes are brought into the n+ source/drain regions at the interface and these volumes are inverted (Figure 4.50 top). This results in increased gate length at the top interface and increased band-to-band tunneling known as GIDL for larger negative bias (Figure 4.18). The same dynamics take place if a large negative bias is applied to the side-gates of a side-gated

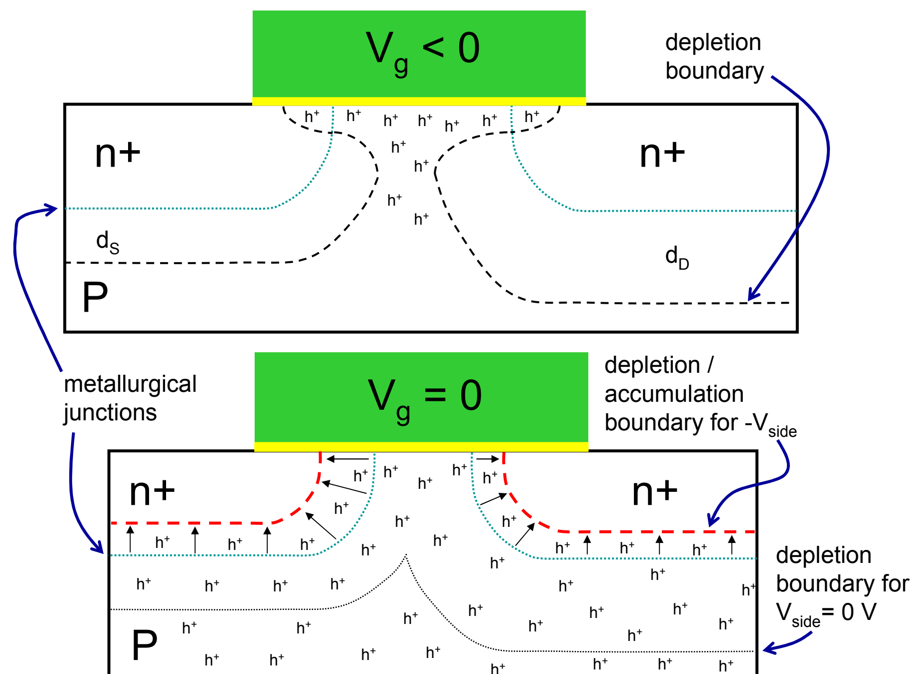


**Figure 4.50** Cross sectional schematics of a short channel bulk FET, top interface accumulated with holes (top). Cross sectional schematics of a narrow channel side-gated device where the body of the transistor is in accumulation (bottom).

device. As the channel width of a side-gated FET is reduced, the accumulated volumes at the two side interfaces merge, leading to accumulation of the whole body of the transistor with holes (Figure 4.50 bottom). Hence, junction depths are significant reduced. The boundaries between the hole accumulated volume and the depletion regions of the junctions move beyond the metallurgical junctions as $-V_{side}$ is increased, inverting the parts of source drain regions with lower doping level (Figure 4.50 bottom). This results in a significant increase of the distance between the source and drain junctions, effectively increasing the device channel length. Hence, narrow channel side-gated devices can achieve very low off currents even at very short gate lengths when the top-gate is set at a low potential. The side-gate bias is needed to be optimized to prevent increased substrate leakage due to GIDL.

The junction regions at the top-interface can be accumulated easily with electrons as a positive top-gate bias is applied, and the channel is inverted at larger positive top-gate biases (Figure 4.51). The volume slightly below the top interface remains in accumulation of holes due to strong coupling to the side-gates and the large negative side-gate bias. Source-drain current is confined to the top interface, resulting in large drive currents while achieving low off currents, reduced DIBL and good subthreshold slope as seen in sections 4.4.5 and 4.4.6.

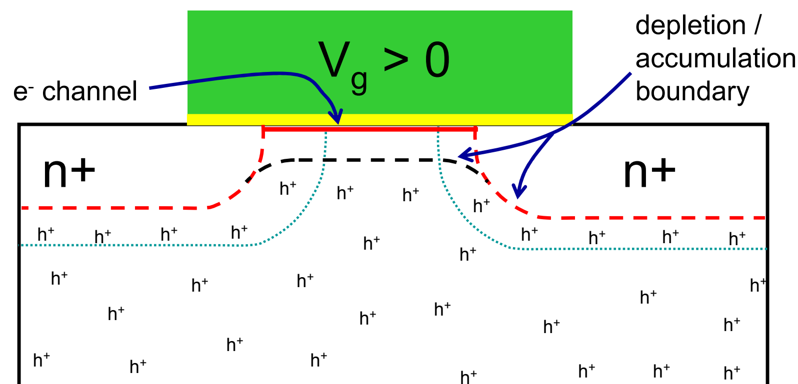


**Figure 4.51** Cross sectional schematics of a narrow channel side-gated device where the body of the transistor is in accumulation and the channel is in inversion.

### 4.4.7 Ultra-narrow width side-gated MOSFET

In the case of the narrow channel planar device geometry, the side-gates have strong control over the body potential as shown in the simulation results (Figure 4.4). In this section the data obtained from an ultra-narrow width device with a gate length within 0.2-0.3 μm range is presented. The device width is expected to be in the order of 10 nm, possibly narrower. A planar device structure with ultra-narrow width, as in this device, is the desired device geometry for the FET based charge sensor for the detection of the biomolecules.

This device shows significant threshold voltage response to side gate bias along with the suppression of the edge related leakage currents but the subthreshold slope is significantly worse compared to the wide-channel and tri-gate structures discussed in the previous sections (Figure 4.52 - Figure 4.54). This is possibly due to the strong control of the side-gates pinning the channel potential. The pinning of the channel potential is stronger on the two edges of the device, possibly resulting in a gradual channel formation starting from the center of the device to the edges.

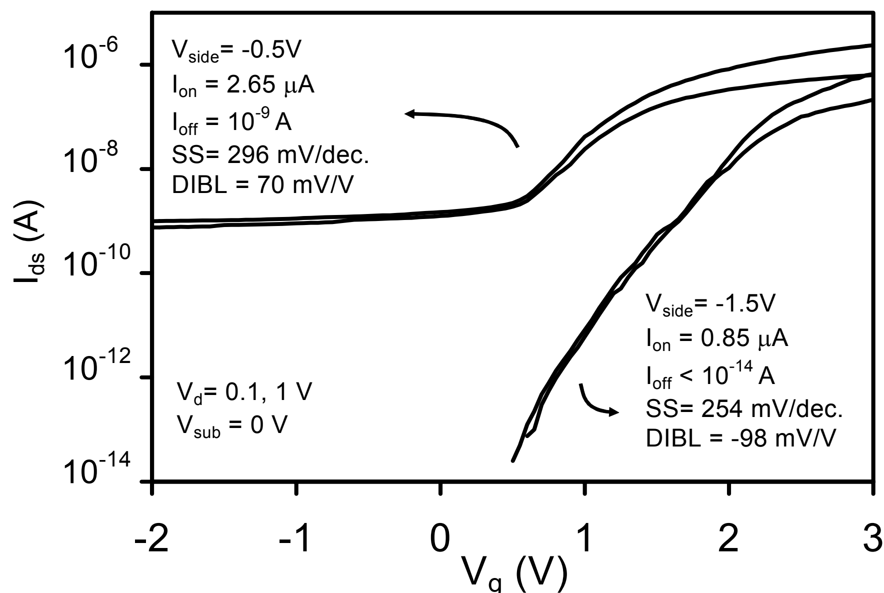


**Figure 4.52** Transfer characteristics of an ultra narrow width side-gated FET.

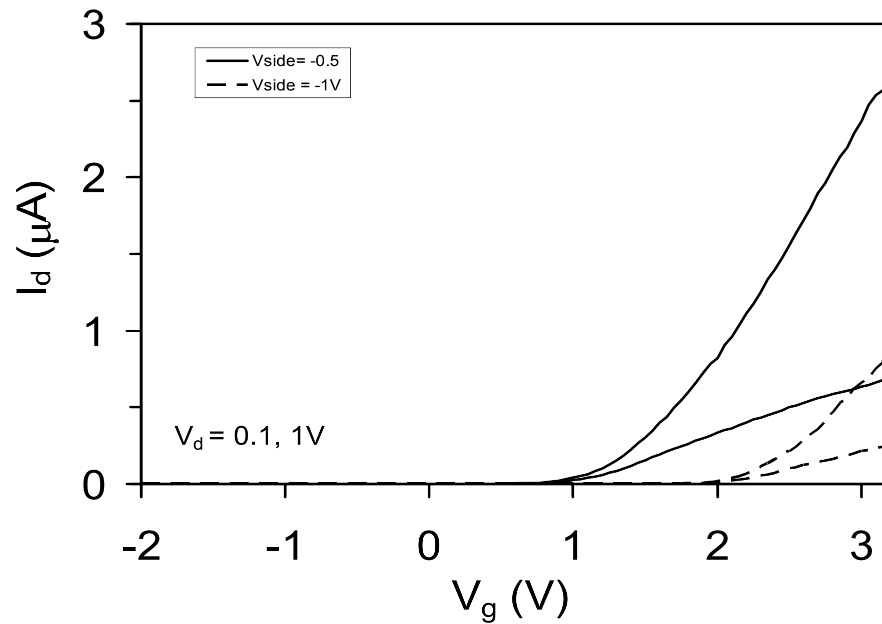


**Figure 4.53** Transfer characteristics of an ultra narrow device W < 10 nm, L ~ 0.2-0.3 μm.

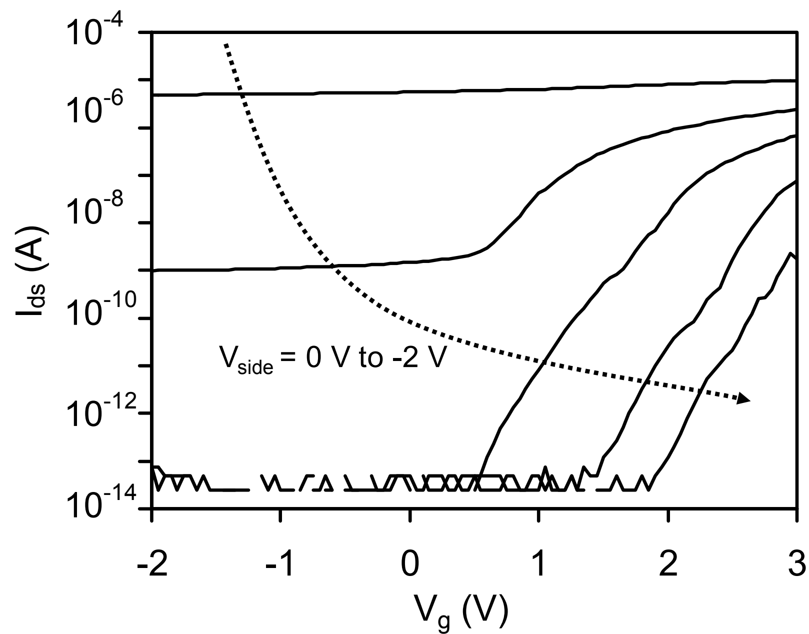


**Figure 4.54** Transfer characteristics for different side-gate biases of an ultra narrow side-gated FET.

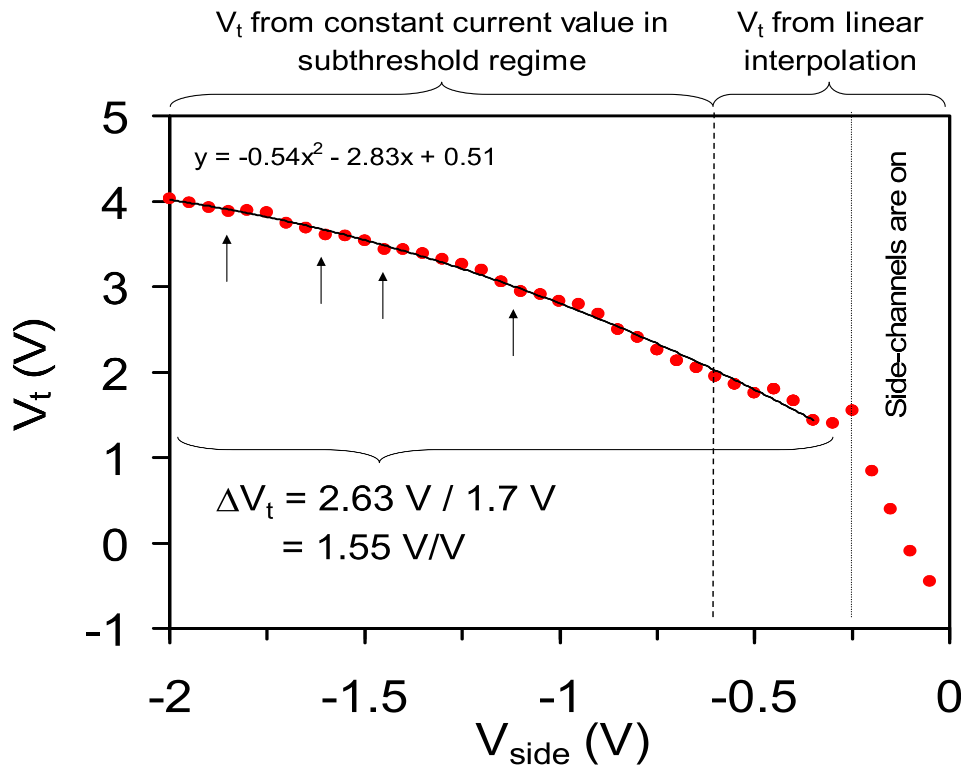


**Figure 4.55** Threshold voltage response to $V_{side}$ of an ultra narrow channel side-gated FET. The data in the $-2 < V_{side} < -0.3$ V range is fit by a quadratic function. The arrows highlight the locations where the $V_t$ change seems to have a stepwise increase.

The threshold voltage of the device changes by 2.63 V within the range of $V_{side}$ = -0.3 V to -2 V, with an average sensitivity of $\delta V_t / \delta V_{side}$ = 1.55 V/V (Figure 4.52-Figure 4.54). This level of sensitivity is significantly larger than in the wider channel devices illustrated in the earlier sections. The sensitivity of best performing threshold voltage tunable dual-gate structure reported in the literature so far is approximately $\delta V_t / \delta V_{side}$ = 0.79 V/V [30].

The threshold voltage of the device is calculated using linear interpolation of the current at the maximum transconductance condition for $V_d$ = 1 V within the $V_{side}$ = 0 to -0.6 V range (Figure 4.55). The threshold voltage shift of the device for large negative side-gate bias is calculated using a constant current method since the devices are not turning on within $-2 \text{ V} < V_g < -2$ V range for $V_{side} < -0.75$ V. The constant

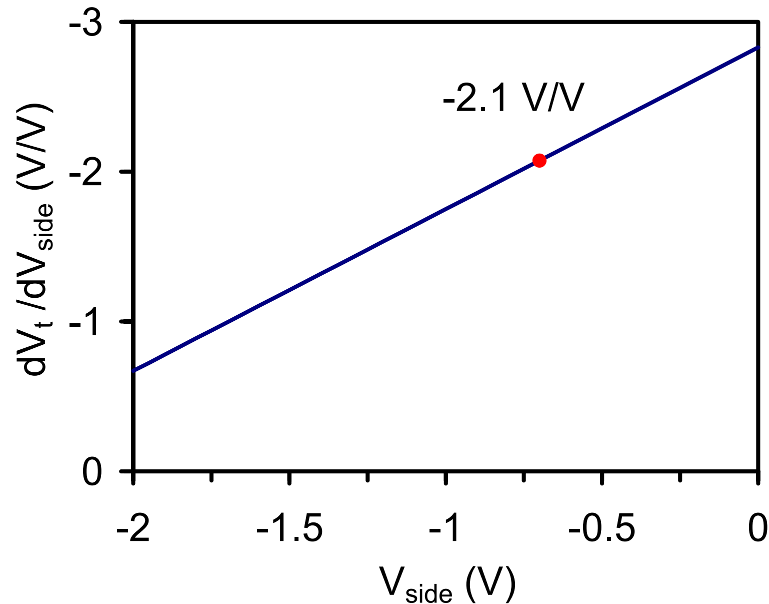


**Figure 4.56** Threshold voltage sensitivity as a function of side-gate bias for ultra narrow channel side-gated FET.

current method for the extraction of the threshold voltages could not be used for the low $V_{side}$ cases due to significant level of leakage currents. The change in the $V_t$ in the $V_{side}$ = -0.6 V to -2 V is added to the value of $V_t$ at $V_{side}$ = -0.6 V in order to obtain the values for $V_t$ in the $V_{side}$ = -0.6 to -2 V range.

The $V_t$ response to $V_{side}$ follows a parabolic trend, saturating at larger negative side-gate biases (Figure 4.55). The sensitivity, $\delta V_t / \delta V_{side} > -2$ V/V for low $V_{side}$ and goes down to 0.8 V/V for $V_{side}$ = - 2 V (Figure 4.56).

The $V_t$ of this device seems to be increasing in a stepwise fashion as indicated in Figure 4.55. This can either be due to quantum confinement effects or trapping of charges at the interfaces during measurements. Studies on similar structures using $SiO_2$ side-gate isolation are necessary to minimize the contribution of charge trapping at the interfaces.

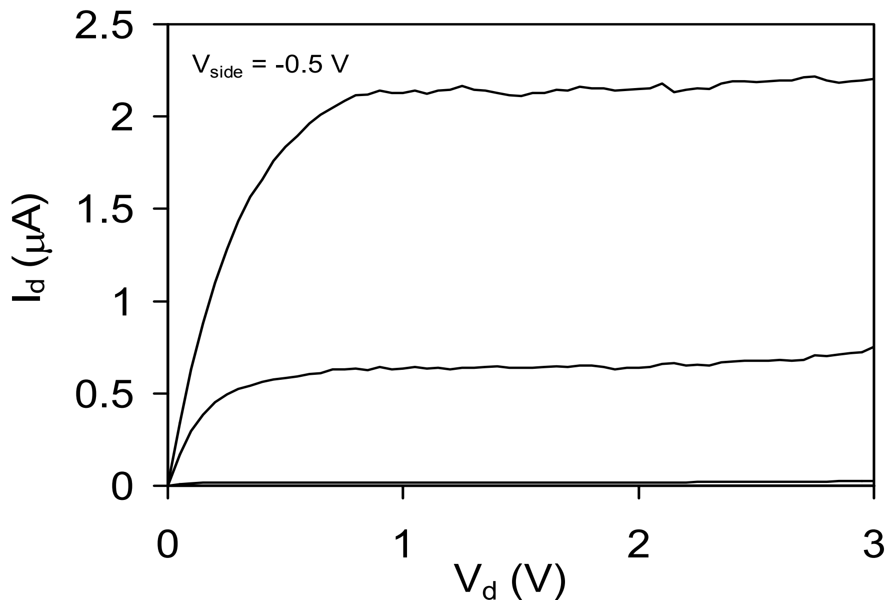


**Figure 4.57** Output characteristics of an ultra narrow device W < 10 nm, L ~ 0.2-0.3 μm.

The drive current of the transistor is approximately 2 μA for $V_{side}$ = - 0.5 V and $V_g$ = 3 V. The current is observed to saturate at around $V_d$ = 0.75 V (Figure 4.57). The saturation level of the drive current suggest that if the gate oxide thickness is around 4 nm , as in the case of surrounding devices, the current limiting area of the transistor is < 10 nm in width. For an estimated current level of 0.5 mA/μm calculated from other devices in the same sample, the current limiting section of the transistor is calculated to be approximately 5 nm in width. This is assuming that there is not an appreciable carrier mobility degradation in the device. It is possible that the width of the whole transistor is < 10 nm or there are narrower regions along the transistors length which are forming the bottle neck for the drive current. Avalanche breakdown of the device is visible for $V_d$ > 2.1 V for $V_g$ = 0 V.

The transistor is also operated in a double gate mode (Figure 4.58) where the side-gate biases are changed along with the top gate bias with a scaling factor and offset in order to accommodate the difference in the dielectric constants and

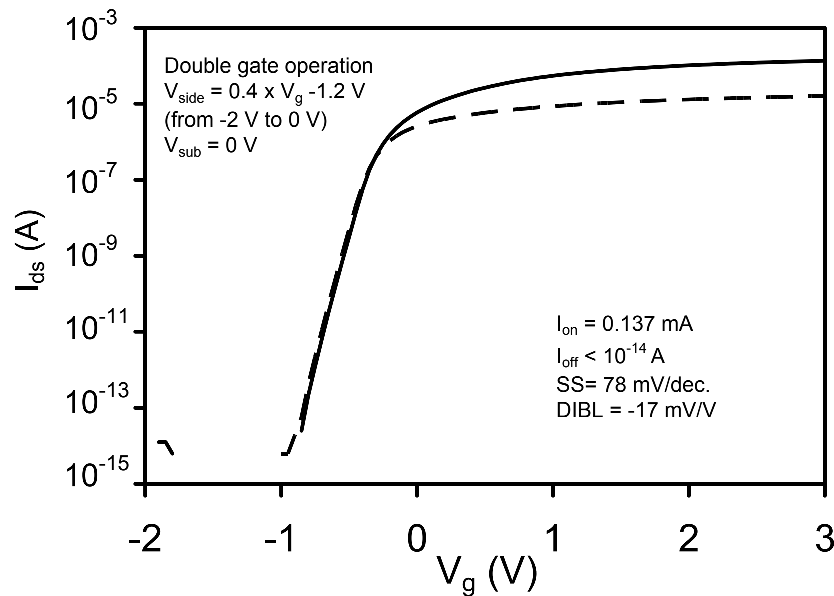


**Figure 4.58** Double gate operation of the ultra-narrow device where the side-gate potential is changed along with the top gate potential as indicated in the figure.

thicknesses, and the difference in $V_t$ due to different fixed charge density on the top and side-surfaces. In the double gate operation, the drive currents are as high as 0.137 mA and the subthreshold slope is 78 mV/dec. This suggests that there are no contact related problems limiting the current drive.

The maximum transconductance measured in the -2 V < $V_g$ < 3.2 V range significantly degrades for $V_{side}$ < -0.5 V (Figure 4.59). The turn-on behavior of these devices are rather gradual due to large source resistance, since the source potential changes depending on the amount of current passing through the device. This, combined with extremely high threshold voltages for $V_{side}$ < -0.5 V results in a significant degradation in the maximum transconductance observed in the device. The devices are no longer getting into strong inversion for $V_{side}$ < -1 V, as it can be seen in the transfer characteristics (Figure 4.54). The control of the side-gates on the top-channel potential is strong enough to turn the devices off even at for $V_g$ = 3.2 V (Figure 4.60). It is also seen that the $I_{off}$ of the device changes by a subthreshold slope

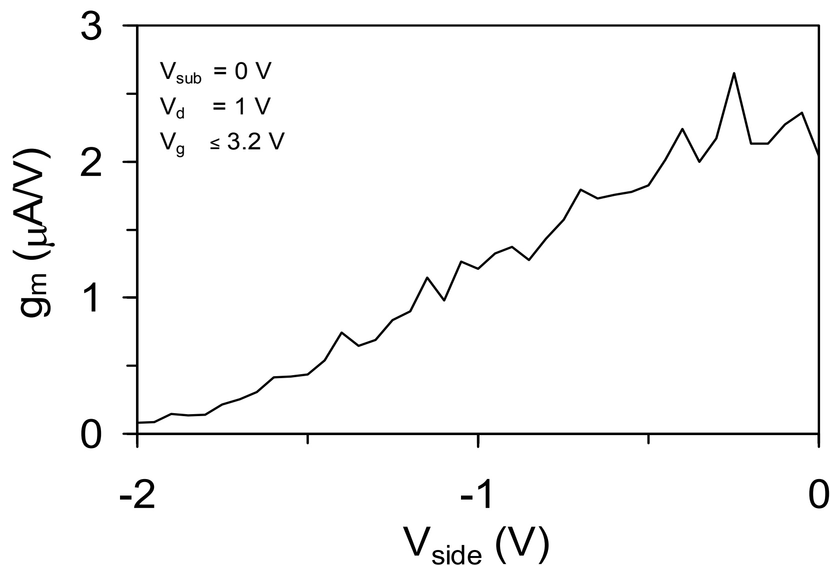


**Figure 4.59** Maximum transconductance as a function of $V_{side}$ of ultra narrow channel side-gated FET

of 75 mV/dec, indicating that the side-gates are forming a good double gate FET on the side-walls of the structure.

The subthreshold slope and the measured DIBL in the device significantly improves as the devices edges are turned off for $V_{side} < -0.5$ V. Part of the contribution for these improvements is the reduction in the leakage currents along the sidewalls. A big part of the improvement is expected to be due to accumulation of holes in the body of the device between the source and the drain, induced by the large negative side-gate biases reducing the source drain junction depths significantly suppressing short channel effects.

The subthreshold slope saturates around 200 mV/dec. (Figure 4.61). These subthreshold characteristics are significantly worse compared to the wider channel devices reported in the earlier sections. This value for the subthreshold slope suggests that the channel is coupled to the side-gates and the substrate twice as strongly as it is

coupled to the top-gate unless other ultra-narrow width effects are playing an important role.

DIBL measured on this device fluctuates around 0 mV/V for $V_{side}$ < -0.5 V. As it can be seen from Figure 4.52, the transfer curves for high $V_d$ and low $V_d$ cross over each other. This is partially due to trapping and untrapping of electrons at the interfaces. Quantum confinement effects may also have a role in this behavior.

Subthreshold slope and DIBL is observed to have a degrading trend as the substrate bias is reduced for a given $V_{side}$ (Figure 4.62). The threshold voltage and maximum transconductance of the device is observed to be independent of the substrate bias (Figure 4.63). As $V_{sub}$ approaches $V_{side}$ the side interfaces of the device move from accumulation to depletion and into weak inversion. The degradation in the subthreshold slope and the DIBL can be explained by reduced effect of the side-gate bias and aggravated short channel effects for low $V_{sub}$ values.

Due to the extremely narrow width of the device, the source-drain currents of these devices are very sensitive to any changes in the trapping-detrapping taking place in the dielectrics surrounding the active areas. This was observed in the repeated measurements performed on this device (Figure 4.64). The variation in the threshold voltage of the device is in the order of 0.1 V as extracted from the subthreshold electrical characteristics (Figure 4.65).

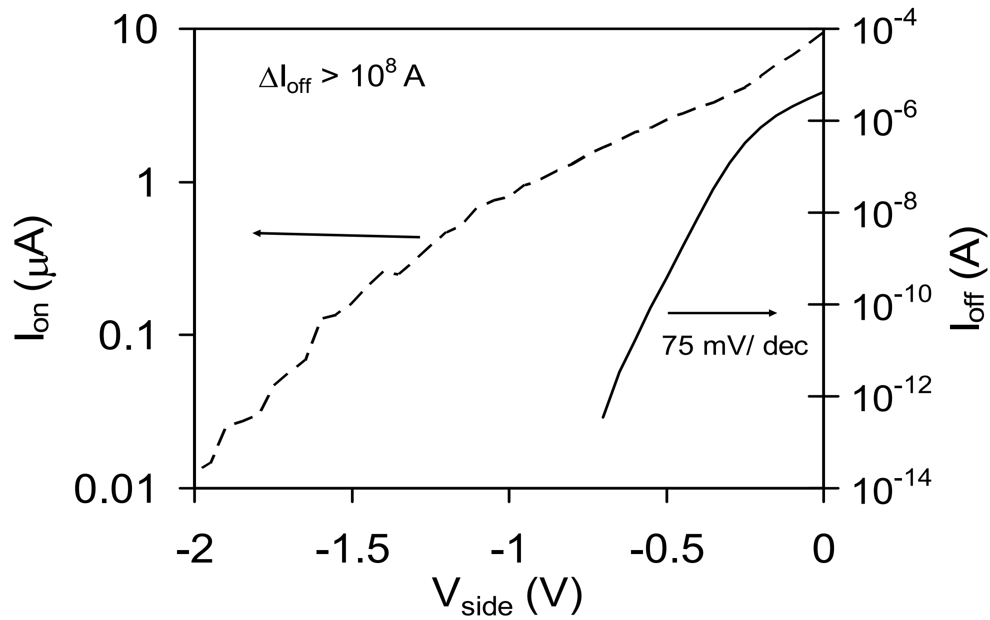


**Figure 4.60** On current and off current as a function of $V_{side}$ of ultra narrow channel side-gated FET.

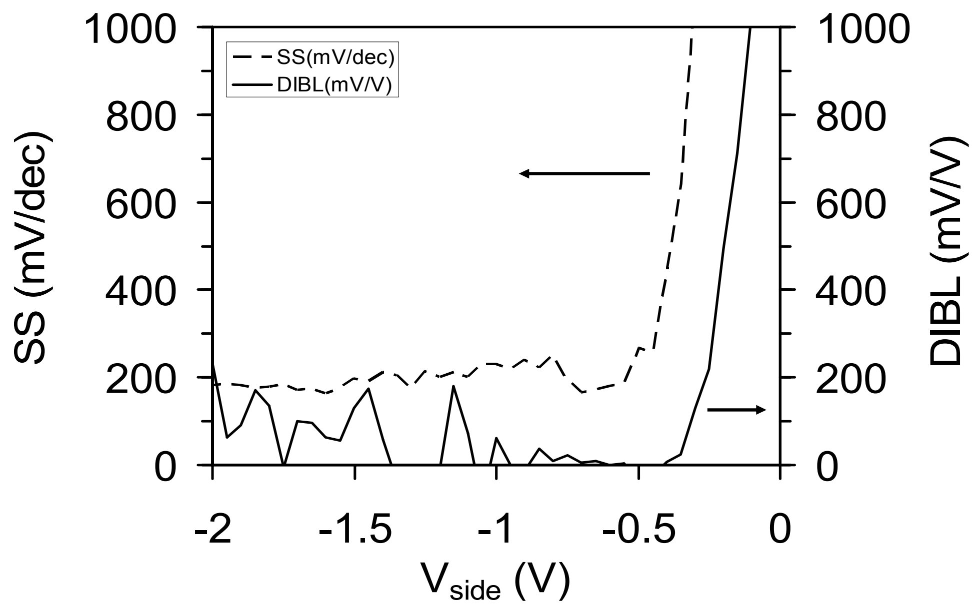


**Figure 4.61** Subthreshold slope and DIBL as a function of $V_{side}$ of ultra narrow channel side-gated FET.

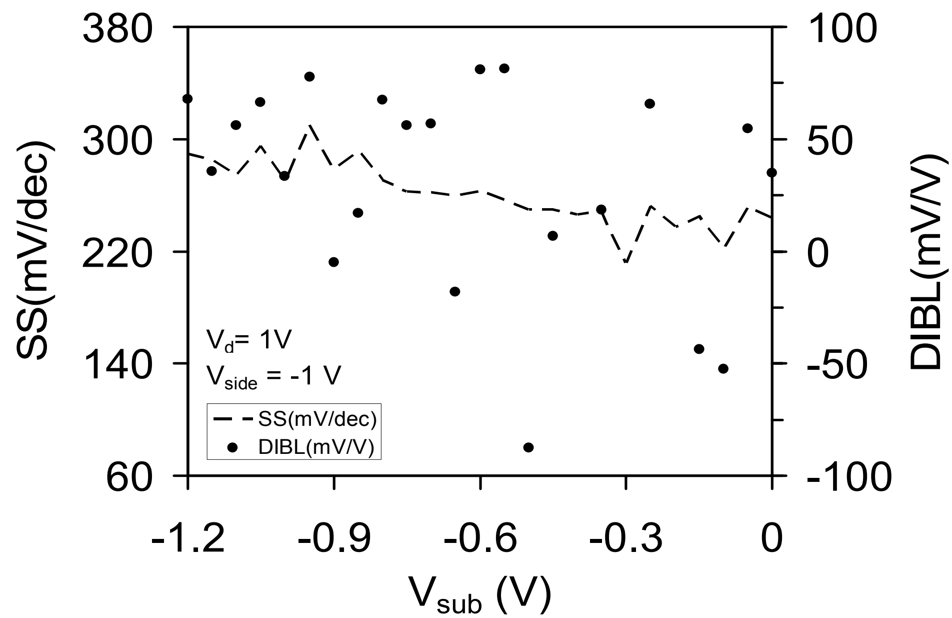


**Figure 4.62** Subthreshold slope and DIBL as a function of $V_{sub}$ of ultra narrow channel side-gated FET.

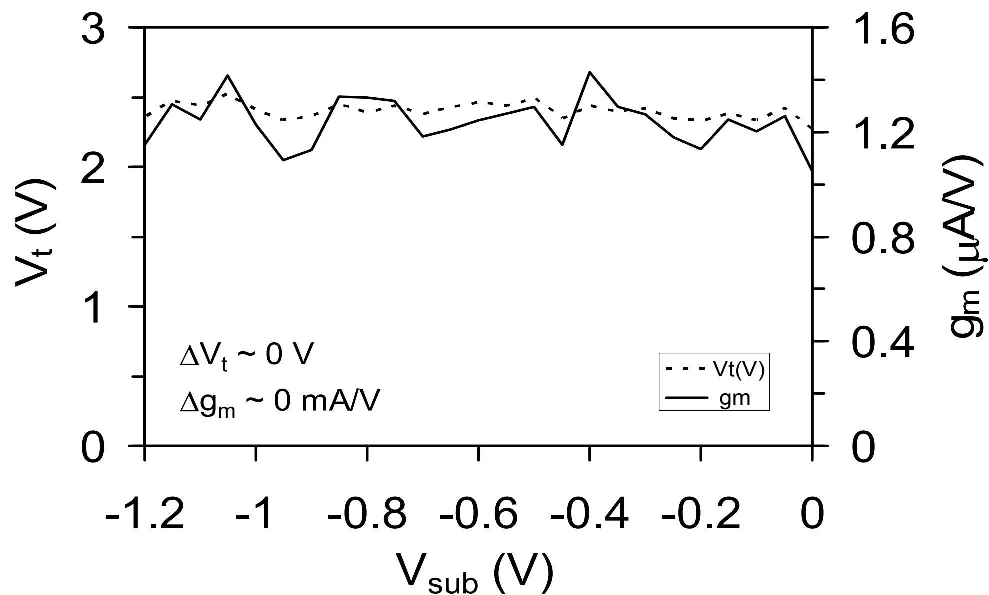


**Figure 4.63** Threshold voltage and maximum transconductance response to $V_{sub}$ of ultra narrow channel side-gated FET.

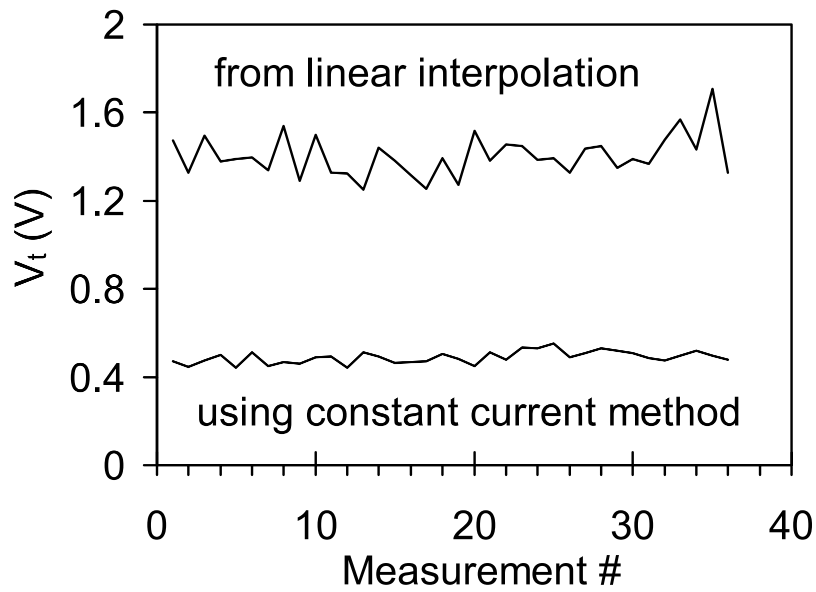


**Figure 4.64** Threshold voltage of ultra-narrow channel side-gated FET extracted from repeated measurements. $V_t$ is calculated linear interpolation and using a constant current method. $3x10^{-8}$ A is used as the threshold current level, $V_{side}$ = -0.5 V.

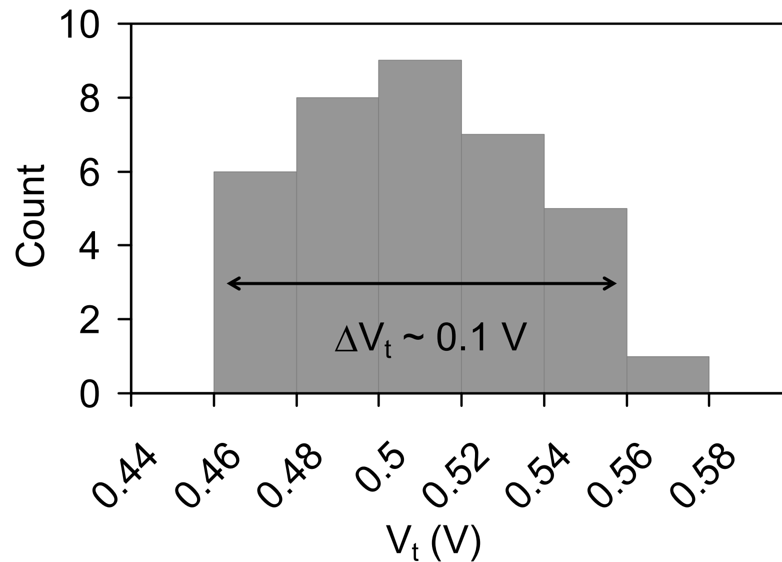


**Figure 4.65** Threshold voltage variation in ultra-narrow channel side-gated FET. $V_t$ is calculated using constant current method using $3x10^{-8}$ A as threshold level. $V_t$ variation in the repeated measurements is around 0.1 V.

## 4.5 Mobility

In order to calculate the effective carrier mobilities in these devices, effective device dimensions (section 7.4) and contact resistance values (section 7.5) should be known. Using these values, and inversion layer capacitance information and the transfer characteristics obtained from the devices at low $V_d$ bias, we can calculate the effective carrier mobility (section 7.6). Knowledge of inversion layer capacitance necessitates capacitance measurements to be performed on the actual devices due to the complicated 3D geometry, corner and edge effects (chapter 5).

A combination of the information obtained from the SEM micrographs and the measured inversion layer capacitance is used to extract the effective device dimensions. The total contact resistance ($R_C$) for each device is calculated from $W_{eff}$, $L_{eff}$ and resistivity data obtained from gate-less devices. The effective carrier mobility ($\mu_{eff}$) is then calculated using:

$$\mu_{eff}(V_g) = \frac{L_{eff}^{\ 2}}{\left(\frac{V_d}{I_d(V_g)} - R_c\right)\int C_{inv}(V_g)dV_g}$$

The electron mobility in the measured devices are in the order of 200 $cm^2/V.s$ for an applied gate field of 7.5 MV/cm (Figure 4.66). The calculated mobilities vary slightly from device to device. The variation is expected to be due to processing and variation in the stress levels. Large side-gate biases are observed to result in reduction in transconductance of the devices. Capacitance measurements performed on the devices suggest that there is not a significant reduction in the carrier density in the channel of the device (Figure 4.66 inset), hence the reduction in $g_m$ is due to degradation in electron mobility in the channel. The reduction in the effective electron mobility is in the order of 10 % for 1 V increase in negative side-gate bias. Due to the

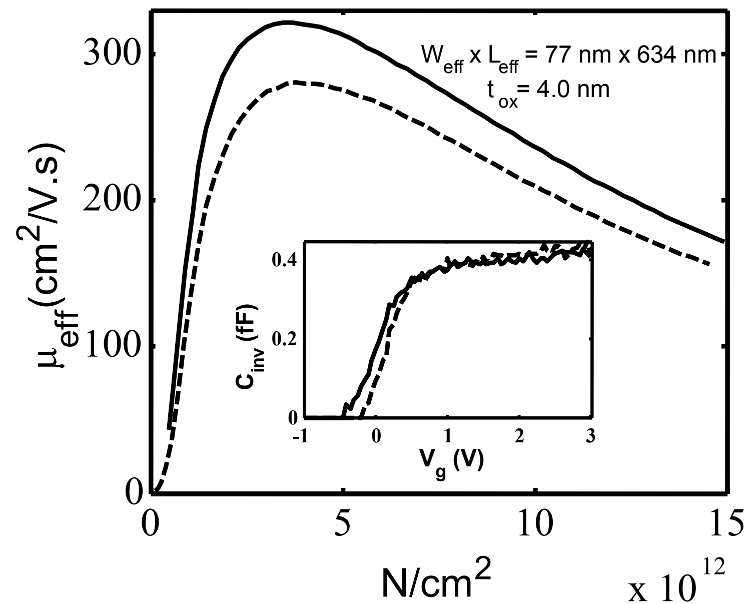


**Figure 4.66** Effective mobility versus electron concentration of a narrow channel side-gated nFET for $V_{side} = -0.5$ V (solid), -1.5 V (dashed) ($V_d = 20$ mV). Inset shows $C_{inv}$ as a function of $V_g$ for the two $V_{side}$.

increased field at the channel gate-insulator interface in order to achieve the same channel potential and carrier density, increased surface scattering, hence, carrier degradation is expected.

Using a side-gated approach, sub-70 nm gate length devices can be fabricated with 3 x $10^{17}$ $cm^{-3}$ doping density and the short channel effects can be significantly suppressed using a field applied from the side-gates. The doping density should be increased to $10^{18}$ $cm^{-3}$ range in order to achieve acceptable device performance using standard planar device geometry, which results in increased impurity scattering and increased field at the channel-gate insulator interface. Therefore, narrow channel side-gated FETs are expected to have comparable or better carrier mobilities, compared to standard planar devices fabricated using same process conditions and surface roughness.

Even though the mobility of these narrow channel devices are not higher than those of the standard planar devices, the current derives are significantly higher due to higher density of carriers inside the device for a given surface area, possibly due to corner effects (Figure 4.39).

## 4.6 Capacitance penalty

The significant reduction in the leakage currents and possibility of using smaller scale devices with overall smaller capacitances by employing the side-gate structure, comes at the cost of additional side-gate to top-gate ($C_{g\text{-}sg}$) overlap and drain-to-side-gate ($C_{d\text{-}sg}$) overlap capacitances (Figure 4.67). The relative ratio of $C_{g\text{-}sg}$ to gate capacitance ($C_g$) can be minimized by using a very thin polysilicon film for the side-gate. The $C_{d\text{-}sg}$ can be reduced significantly by recessing the $Si_3N_4$ between the source/drain and the side-gate down to the level of the drain-substrate metallurgical junction.

The concerns about overlap capacitances differ depending on the intended application. For sensor devices, where a small charge is trying to be sensed, side-gate

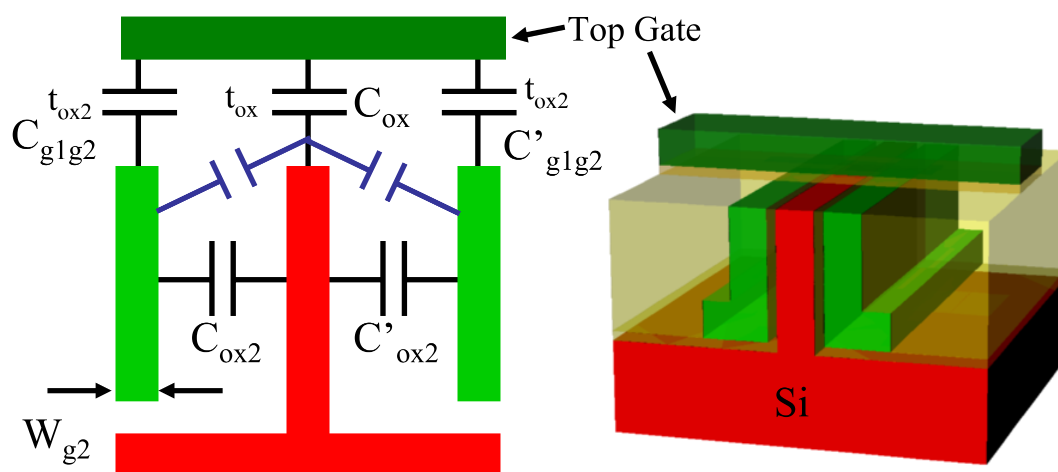


**Figure 4.67** Schematic view of the side-gated FET cross section taken through the channel area(left) and 3D illustration (right).

to top-gate overlap capacitance is not a concern since both of these gates are statically biased during the measurement. The top-gate to channel, side-gate to channel and side-gate to drain and source overlap capacitances are important. The side-gate to channel capacitance affects the subthreshold slope of the device, hence the current sensitivity to the charge perturbations coming from the sample. Side-gate to drain and source capacitances increase the RC time constant of the system, resulting in limitation on the current measurement speed.

The side-gate to top-gate overlap capacitance is extremely important for logic applications in addition to the side-gate to body and drain/source to side-gate overlap capacitances. The relative contribution of the overlap capacitance has to be evaluated as a function of the desired $I_{on}$ and $I_{off}$. Even though the relative contribution of the $C_{g1g2}$ (Figure 4.67) is more significant for narrow channel devices, since the short

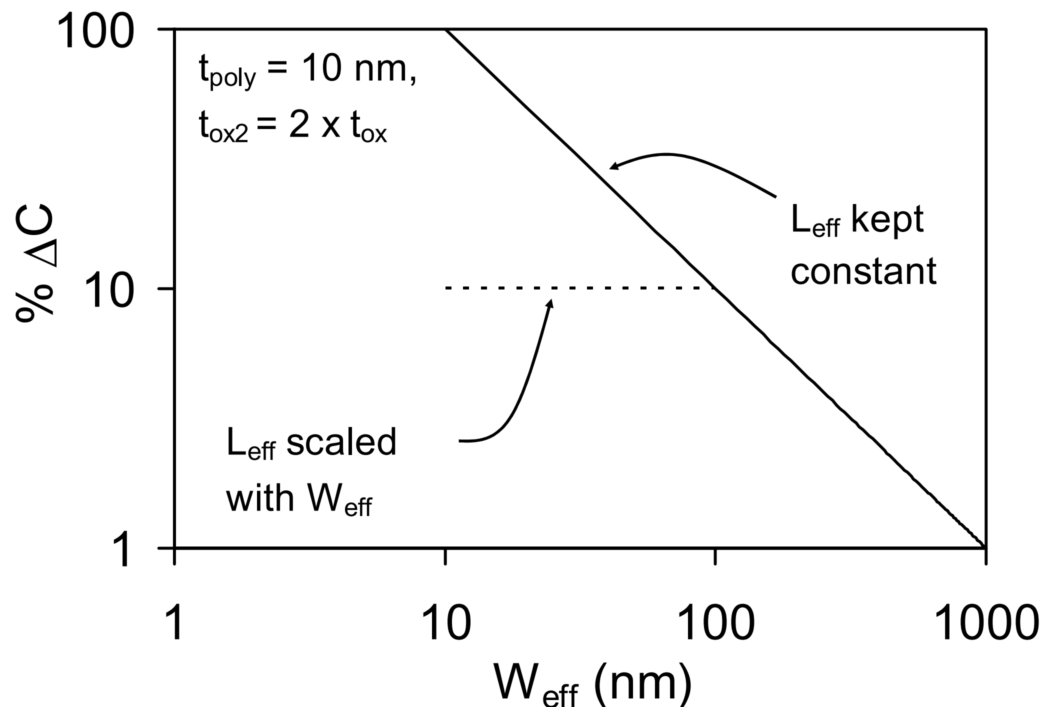


**Figure 4.68** Additional top-gate to side-gate capacitance as a percentage of inversion layer capacitance as a function of effective device width, if gate length is kept constant (solid) and if gate length is scaled along with width for $W_{eff} < 100$ nm (dashed).

channel effects are significantly reduced, the gate length of the device can be made significantly shorter, while still achieving the targeted $I_{off}$ values. Reduction in the gate-length results in a reduction in the scaling factor of the overlap capacitances and reduces the channel resistance, allowing larger current drive in a smaller width device (Figure 4.68).

For larger width devices, the affect of the side-gate on suppression of short channel effects weaken, but the relative contribution of the $C_{g1g2}$ also reduces.

All of the devices benefit from the reduction in the peripheral leakage currents. Narrow channel devices benefit more in suppression of short channel affects, wider devices do not experience significant increase in parasitic capacitances, hence the side-gated approach can be implemented in VLSI circuits successfully using the flexibility of employing devices with different channel width and gate length.

## 4.7 Channel optimization for sensor application

The device parameters are needed to be optimized for high sensitivity charge detection using these devices. The channel width of the FET is needed to be as small as possible for increased spatial resolution and for increased current response to the charge perturbations on the channel. The effect of a charge perturbation is larger if the capacitances coupling the channel to the surrounding electrodes are minimized. This can be achieved by employing thicker top-gate and side-gate dielectrics.

The current in ultra narrow channel devices are very sensitive to trapping and untrapping events take place at the device interfaces. The defect density is much larger at the Si-Si3N4 interfaces compared to Si-SiO2 interfaces. The $Si_3N_4$ layer on the edges of the channel can be recessed using HF after tunnel formation and a thin oxide can be formed on the device edges in order to minimize the noise contribution of the

defects at the interfaces. This will also allow increased confinement of the electrons to the central section of the device.

If the channels are intended to be formed on the two edges of the active area, making use of the positive fixed charges at the interfaces (Figure 4.69), the channel width should be chosen to be wider. However the width of the device should be chosen such that subthreshold leakage in the central part of the active area is much less than the current flowing in the inversion layers forming on the two edges of the active area. One of the two channels forming at the edges of the device can be kept off and the subthreshold leakage in the central portion of the device can be adjusted through angled implants. This approach is limited with the diffusion of the dopant atoms in the later high temperature steps.

The approach of confining the electrons to the edges of the device can increase

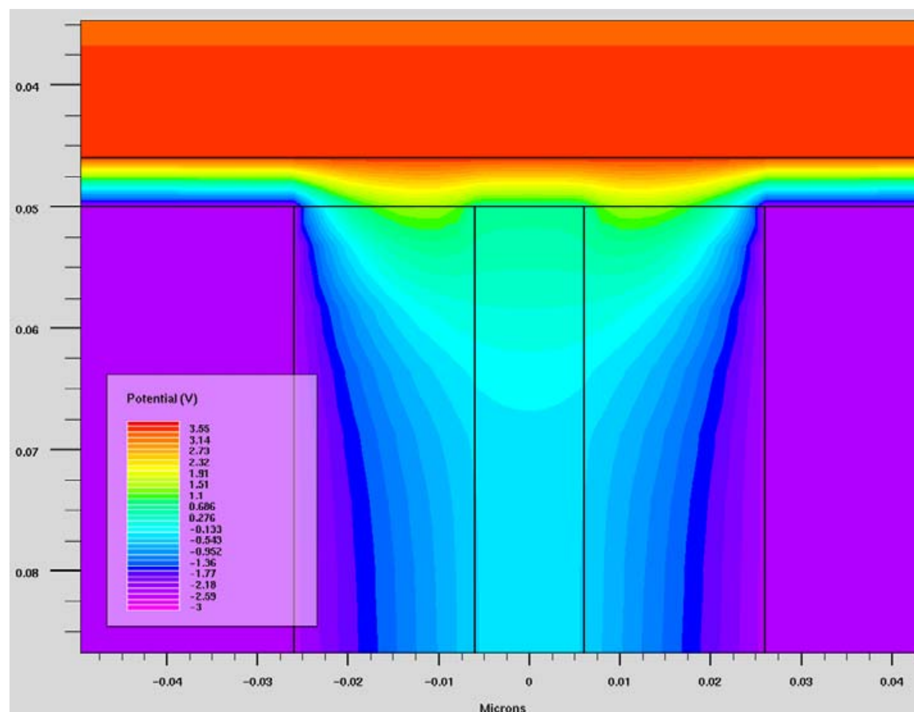


**Figure 4.69** Simulated potential profile of a 12 nm wide channel with side-gates. The side-gates are negatively biased, the top-gate is positively biased. $Q_{int} = 3 \times 10^{10}$ $cm^{-2}$ [51].

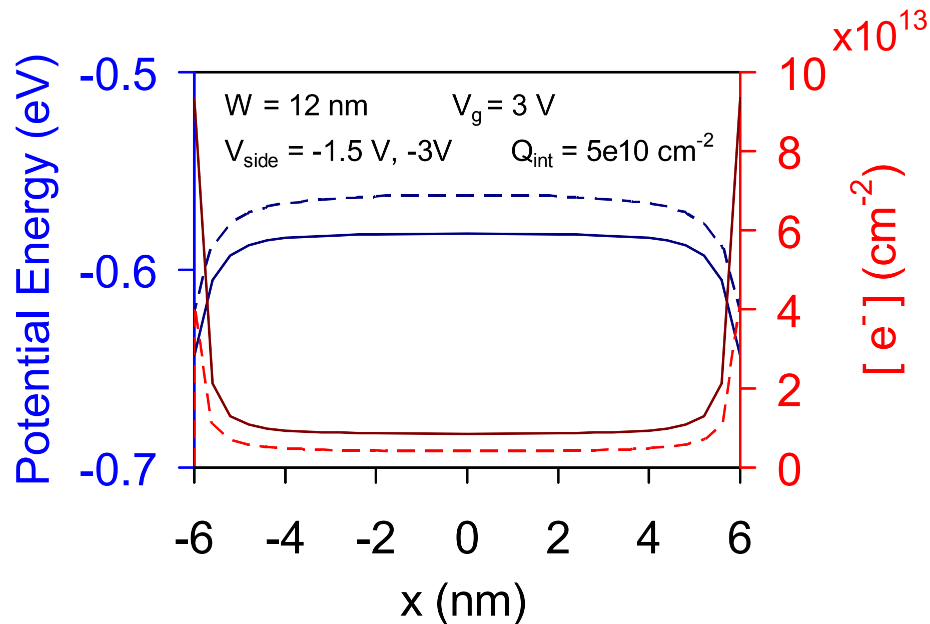


**Figure 4.70** Cross sections of simulated potential profile and electron density at the top interface for $V_{side}$ = -1.5 V (solid) and $V_{side}$ = -3 V (dashed) [51].

the current confinement down to 1 nm regime (Figure 4.70), however, it is more prone to current fluctuations due to trapping and untrapping events which take place at the interfaces.

## 4.8 Side-trapping non-volatile memory

As it is demonstrated in the section 4.4.7, is possible to change the threshold voltage of the planar narrow channel devices significantly by changing the side potentials of the side-gated FET. This suggests that it is also possible to trap charges on the two sides of the channel in order to change the threshold voltage of the device, hence operate as a non-volatile memory. The side dielectrics of the fabricated prototypes are silicon nitride, which has a large density of traps. It is possible to trap charges in the nitride between the side-gate and the channel in order to demonstrate this concept.

The transfer characteristics ($I_d$-$V_g$) of a side-gated FET with $t_{ox}$ = 7 nm is measured with $V_{side}$ = 0 V (right curve in Figure 4.71). The device is then biased with $V_{side}$ = +3 V for 30 seconds in order to inject charges into the nitride layer serving as side-dielectric. Next, $I_d$-$V_g$ characteristic is measured again with $V_{side}$ = 0 V as before (left curve in Figure 4.71). The transfer characteristics of the device before and after "write" operation show a $V_t$ shift of 1.3 V. This significant $V_t$ shift results in a maximum current level change by a factor of approximately $10^6$. This result suggests that side-trapping architecture is a viable approach to making non-volatile memory devices. If the side dielectrics are deposited as oxide/nitride/oxide stack or oxide with embedded Si nano-crystals instead of silicon nitride, the side gated device can be used as a side SONOS memory with side interface storage and high speed read from top transistor. This concept is similar to back gated SONOS memory demonstrated by H. Silva & S. Tiwari [66].

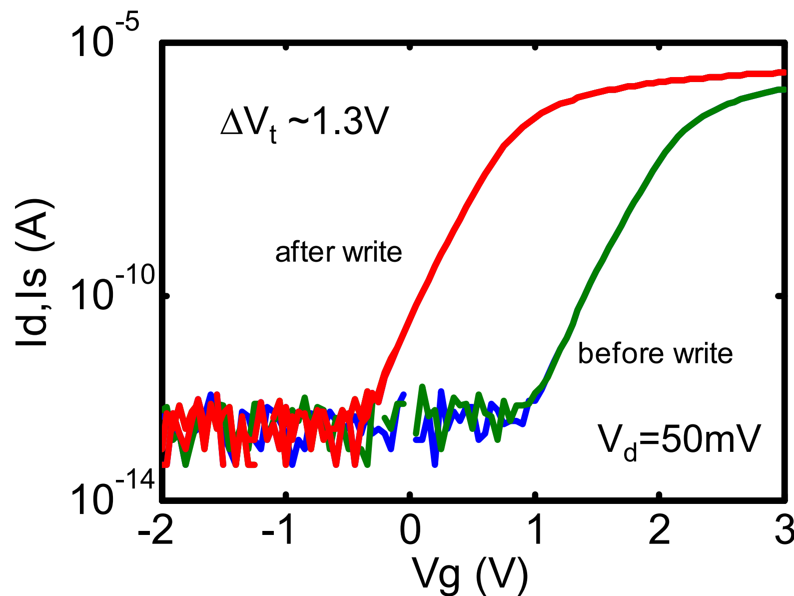


**Figure 4.71** $W_{eff}$ x $L_{eff}$ < 0.2 μm x 0.33 μm , $V_{side}$= 0 V for read, $V_{side}$= +3 V for 30 seconds for write. Effective device width is estimated from the design dimensions and a set of measurements performed on an array of devices with different dimensions. The actual device width may be smaller than 0.2 μm.

The possible advantage of this structure is utilizing combination of quantum confinement effects and electrostatics in ultra narrow channel structures to change the $V_t$, while the electrostatic effect of the charges are enhanced due to charges stored on both sides of the channel. This device structure can be scaled down smaller than the standard floating gate FLASH structures since the control oxide of the device can be made very thin, suppressing the short channel effects, as in the case of [66]. This structure also has isolated read operation, using the top gate which would not perturb the stored charges on the two sides of the channel.

## 4.9 An instrumentation anomaly

In the case of some of the narrow channel devices the transfer characteristics measured with HP 4145B parameter analyzers showed significant changes in the transfer characteristics depending on the applied side-gate bias. The transfer characteristics of a narrow channel side-gated device with 19 nm $Si_3N_4$ side-gate dielectric and top-gate dielectric of 7 nm $SiO_2$ is as seen in Figure 4.72 (left) for $V_{side}$ = -0.5 V. This device is not annealed in $H_2/N_2$ ambience, hence the defect density is expected to be higher than those devices reported in sections 4.4.4 - 4.4.7. As the $V_{side}$ varied from -0.8 V to -1.6 V subthreshold slope of the device seem to degrade significantly and the current level of the device start changing in a very non-linear fashion. The current seems to be settling at some certain current values for $V_{side}$ ~ -1 V and for higher negative side-gate biases sudden drops in the current level is observed. The periodicity of these drops and the amount of reduction in the current level change consistently as the negative side-gate bias is increased. In the case of -1.6 V $< V_{side} <$ -1.8 V this dependency on the side-gate bias is clearly observed (Figure 4.73). For $V_{side}$ = -1.8 V the current level drops down by a factor of 30 as the $I_{ds}$ reaches 1 nA. In all of the figures seen in this section $I_d$ and $I_s$ are plotted together. In some of the plots slight

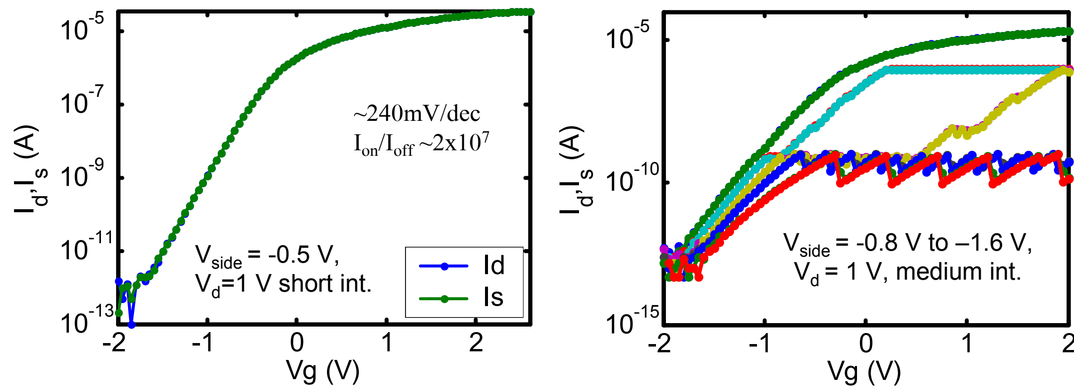


**Figure 4.72** Transfer characteristics obtained for small $V_{side}$ using short integration time (left) and for larger $V_{side}$ values using medium integration (right).

differences between $I_d$ and $I_s$ are visible for some $V_g$ values, however the difference in these current levels are extremely small. This suggests that the drops observed in $I_d$ are real and not due to leakage into other terminals.

Repeated measurements on the same device with the same bias condition have resulted in significantly repeatable results (Figure 4.74). The drop in the current level is consistently taking place around 1 nA. In most measurements, the current level drops down by approximately 30 times and in some cases it only drops down by a factor of 2. The measurements were repeated by using a different 4145B parameter analyzer and very similar results were obtained.

In order to understand the effect of charge trapping on the device behavior, hysteresis measurements are performed. After taking a forward sweep, going from $V_g$ = -2.5 V to 2.5 V, another sweep is started after a few seconds going from $V_g$ = 2.5 V to -2.5 V (Figure 4.75). This measurement showed that there is a very significant change in the current level at the start of the reverse sweep and the current level significantly drops down to below 50 fA for $V_g$ < 1.5 V.

The existence of significant hysteresis in the transfer characteristics suggest that there is a very significant influence of charge trapping in the device characteristics.

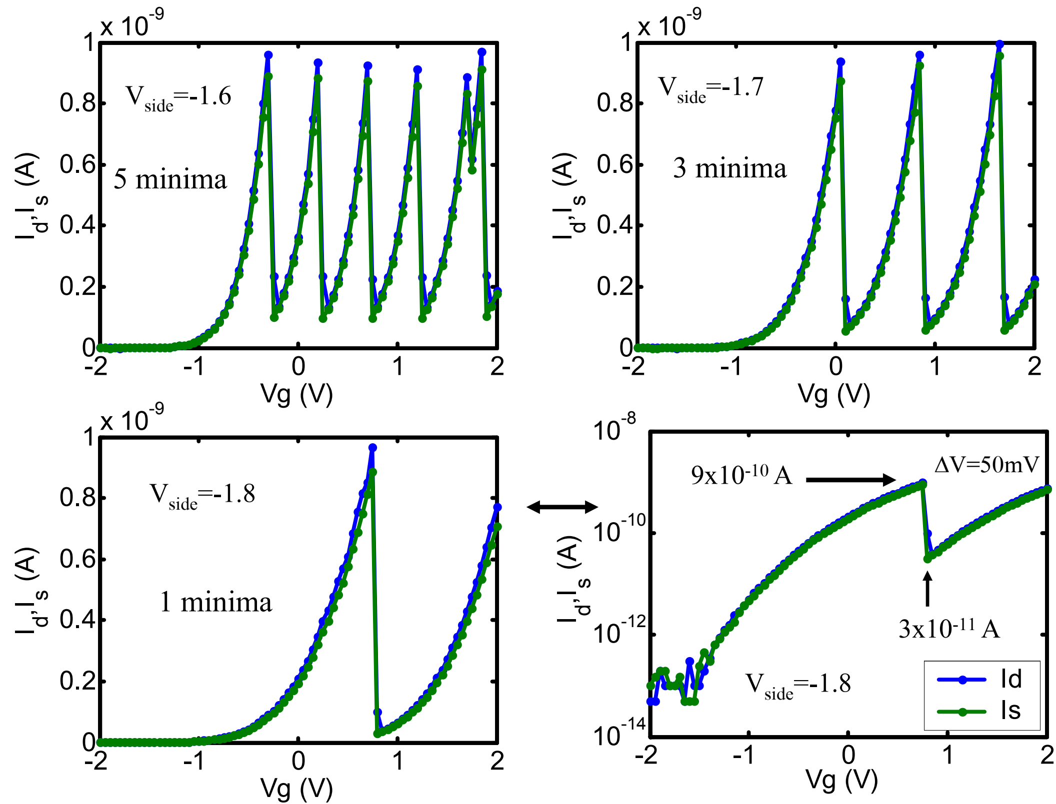


**Figure 4.73** Sudden drops in current is observed as the current value approaches 1 nA. The number of peaks observed in the measurement window consistently decrease as negative $V_{side}$ is increased.

However it was not very clear why we would be observing the zigzag behavior in the current level.

Electrical measurements conducted on nano-crystal memory structures [67] with H. Silva using an Agilent 4156C parameter analyzer has resulted in similar sudden drops in the current level and zigzag pattern for certain bias conditions. Monitoring the parameter analyzer while making the measurements, we have observed that the parameter analyzer spends more time at some bias conditions as the current level moves from one decade to the next. This significant change in the time scale of the measurement is not observed in standard logic FETs as such presented in sections 4.4.4 - 4.4.7. This is probably due to a combination of more than one phenomenon.

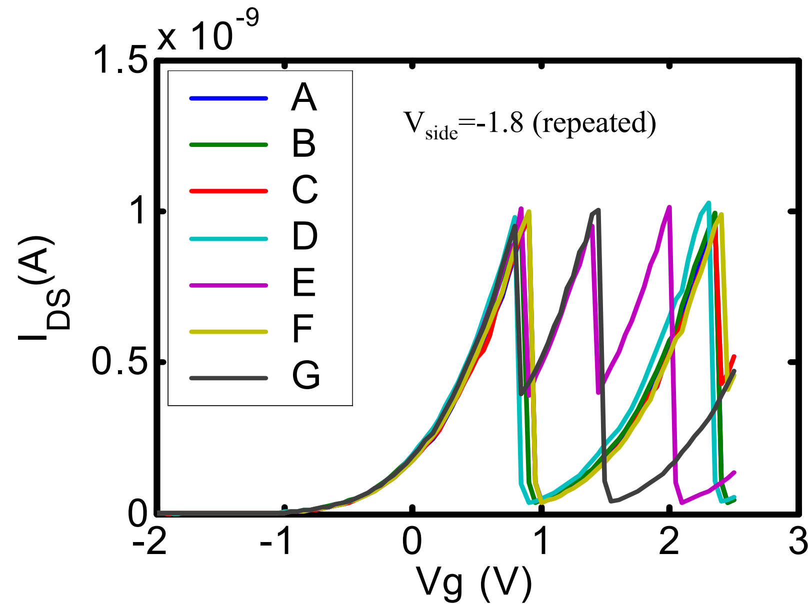


**Figure 4.74** Consistent current drops observed in repeated measurements.

As it is demonstrated in the previous section, it is possible to inject charges into the nitride on the two sides of the channel which results in significant change in the threshold voltage of the device. The amount of threshold voltage shift observed in the device depends on the amount of charges stored in the nitride, location of the charges and the width of the channel. The width of the channel can have slight variations due to processing. The defect locations in $Si_3N_4$ and Si-$Si_3N_4$ interface and the time required to trap and detrap charges from these defects have significant variations. Since there is no oxide barrier layers on either side of the nitride layer the traps in the Si-$Si_3N_4$ interface and inside $Si_3N_4$ film in close proximity to the interfaces can get filled and emptied rather easily. These traps can be filled or emptied during the time period of a voltage sweep performed to acquire the transfer characteristics of the device.

The traps filled with electrons increase the $V_t$ of the FET. Some of these traps are filled during the period of the gate voltage sweep, which result in a continuous change in the $V_t$ of the device during the measurement. At every decade HP 4145B

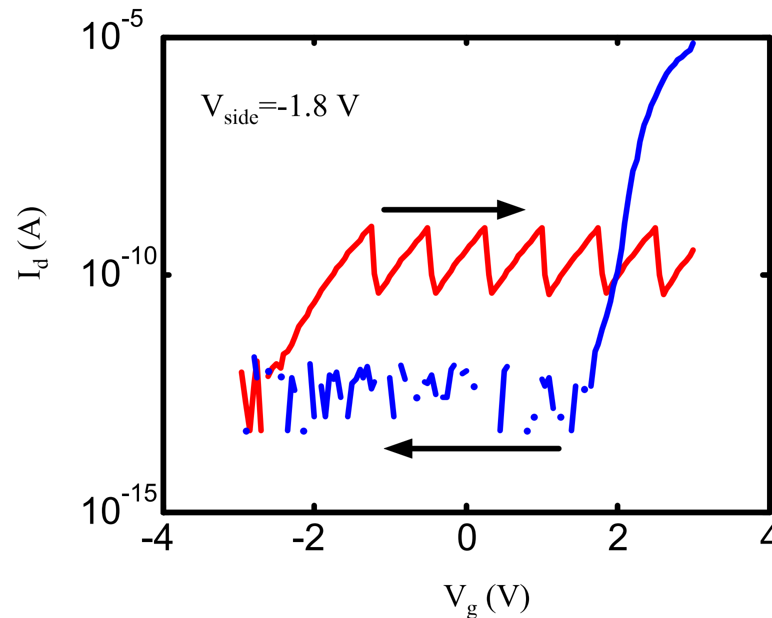


**Figure 4.75** Hysteresis measurement on the same structure.

spend slightly more time in acquiring data, this is probably due to amplifier switching in the parameter analyzer. During this switching period, the current level in the device continues to decrease due to continuous injection of changes, hence $V_t$ shifts. Since the current level is dropped below the threshold value of the current required to switch the amplifier for sensing a larger value of current, the parameter analyzer switches back to the earlier sensitivity level. During this time period, which can be as long as 1 sec, the current level drops down significantly. As $V_g$ is further increased, the current level is again increased to a threshold level, such as 1 nA. This results in the repletion of what has been taking place at this current level. This process, repeated for increased $V_g$ values, result in a zigzag pattern in the current level.

In the case of the reverse sweep, the current level for $V_g = 2.5$ V is significantly high, suggesting that the $V_t$ of the device is low, hence significant portion of the traps are empty. As the measurement started, the traps get filled as in the forward sweep. However, this time $V_g$ is continuously reduced and any extra time

spend in amplifier switching results in a drop in the current level, which is observed as improved subthreshold slope (Figure 4.75).

The particular device analyzed in this section exhibits a $V_t$ shift larger than 4 V during the measurement of transfer characteristics. This suggests that the current limiting section of the channel is rather small and the trap density on the two sides of the device are significantly high. Experimentalists working on charge trapping devices should be cautious about similar instrumentation anomaly.

## 4.10 Transconductance oscillations

It is possible to observe single electron effects in the ultra narrow channel devices. The single electron effects become more dominant as the device width is scaled down. It is possible to shrink the device width down by applying larger negative biases on the side-gates of a side-gated narrow channel transistor. The filled traps on the two sides of the channel also have a strong contribution on the channel potential, hence can lead to further reduction in the channel width. Due to non-uniform

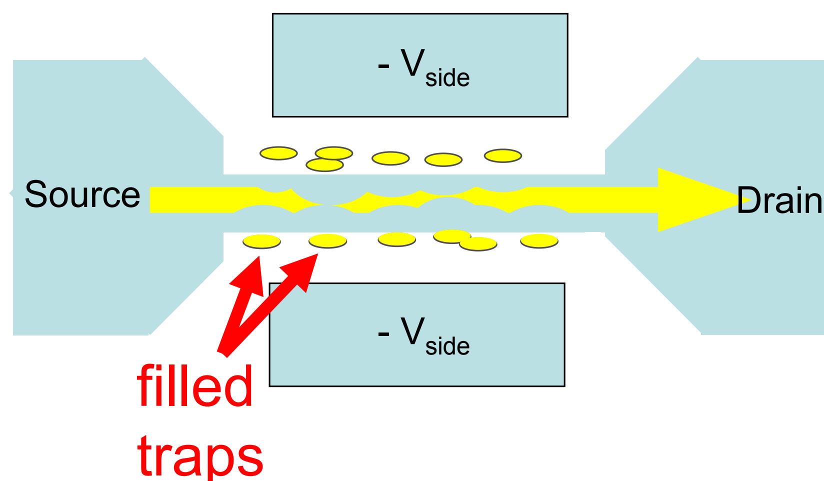


**Figure 4.76** Schematic view of effect of non-uniformly distributed filled traps on the two sides of a narrow channel side-gated FET with strong side-gate biases. The channel may be pinching off at various locations forming one or more quantum dots inside the channel.

distribution of these traps, it might be possible to achieve isolated potential wells along the channel of the device forming quantum dots (Figure 4.76). These 3D confined areas can lead to coulomb blockade oscillations. If the region of electron confinement is small, these oscillations may be observable at room temperature.

However, due to instrument related complications of charge trapping devices, observations of narrow channel device behavior should be done at a bias regime where it is known that there is not any contribution of the instrumentation in the measurements. In order to eliminate the problems described in the previous section, the devices are biased with a large $V_{side}$ value which keeps the current level below the 1 nA level where amplifier switching seems to be resulting in sudden current drops.

Experiments conducted on some of the devices showed that these are some non-linear changes in the current level during $I_d$-$V_g$ sweeps conducted at room temperature (Figure 4.77). Although the repeated measurements do not reveal the same exact transfer characteristics, all of the measurements showed these non-linear behavior in $I_{ds}$. The first derivative of the transfer characteristics show clear transconductance oscillations for two different side-gate bias conditions in Figure 4.78.

Figure 4.79 show the transfer characteristics for $V_{side}$ = -3 V for 3 V < $V_g$ < 4 V. The solid dots in the plot show the actual measurements of $I_d$ and $|I_s|$ and the solid lines are formed by using a moving average of the data. In this regime there are two clear plateaus in $I_d$ and $I_s$. Transconductance in the -2 V < $V_g$ < 4 V show clear oscillations corresponding to these plateaus and also some smaller oscillations (Figure 4.80). The oscillation amplitude is smaller for $V_{side}$ = -3.1 V case. For $V_{side}$ = -3.1 V the transconductance calculated from $I_d$ and $|I_s|$ slightly differ.

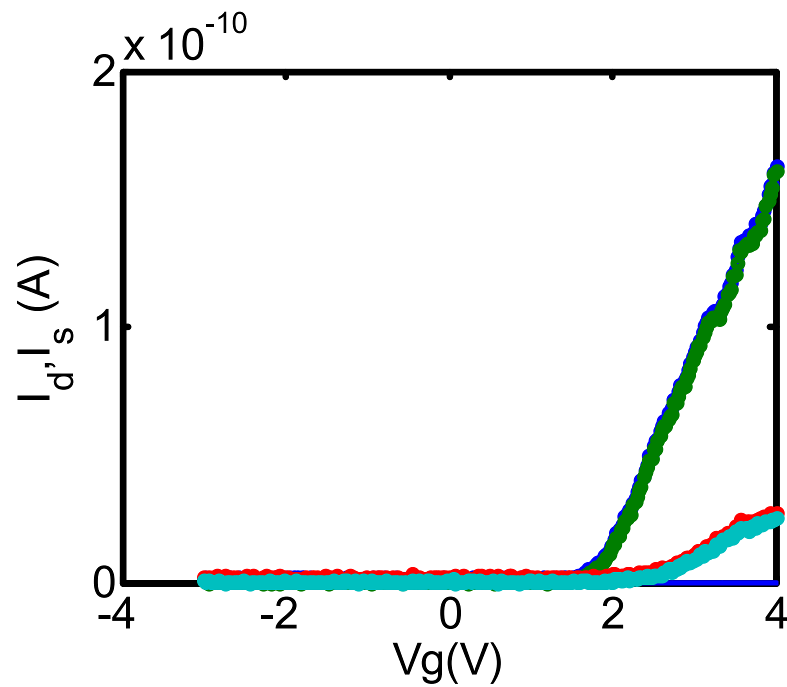


**Figure 4.77** Transfer characteristics of a side-gated FET after a write bias for $V_{side}$ = -3 V, -3.1 V. Data is taken with 25 mV steps in $V_g$.

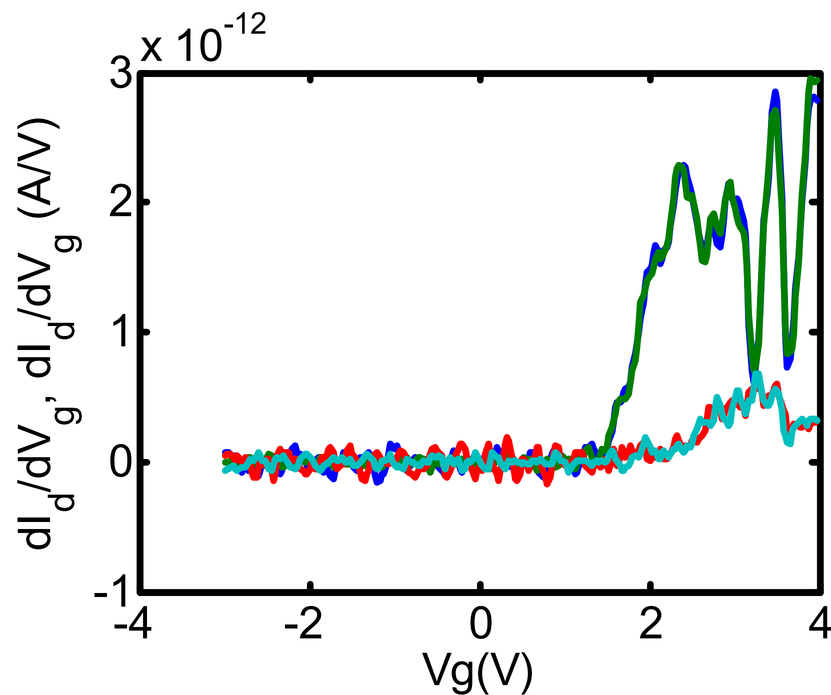


**Figure 4.78** Transconductance as a function of top gate bias for $V_{side}$ = -3 V, -3.1 V.

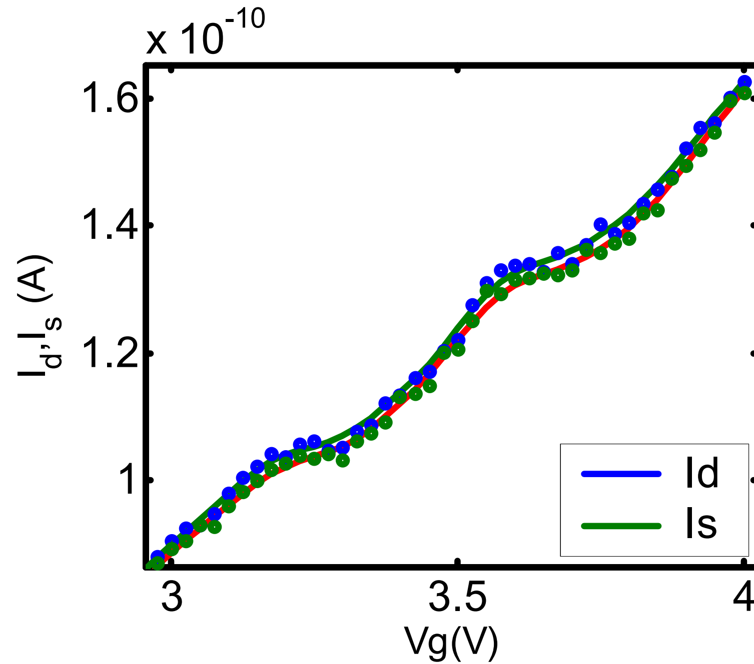


**Figure 4.79** Transfer characteristics of a side-gated FET for 3 V < $V_g$ < 4 V after a write bias for $V_{side}$ = -3 V. Zoomed in version of Figure 4.77. The points are actual measurements, the solid lines are constructed through a moving average.

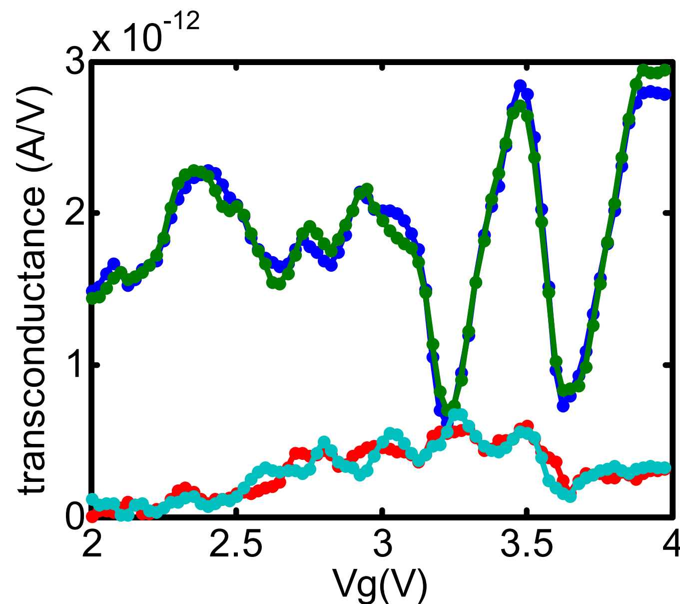


**Figure 4.80** Transconductance as a function of top gate bias for 3 V < $V_g$ < 4 V and $V_{side}$ = -3 V, -3.1 V. Zoomed in version of Figure 4.78. The points are the actual measurements, the solid lines are constructed through a moving average.

It is very hard to identify the reason for these transconductance oscillations. One dominant contributor is the charging of the traps. If the charging of the traps are resulting in formation of 3D confinement regions, these regions change over time and also as the $V_g$ is varied. Although there is not conclusive evidence, the oscillations are possibly due to the combined effect of both, charging during the measurement and formation of isolated quantum dots inside the channel region. Further studies should be conducted on a system where the nitride trapping layer is isolated from the channel, the side-gate and the top-gate with thin oxide layers. In this configuration the charges can be kept in the traps for a longer time and detailed transconductance measurements can be conducted.

## 4.11 Low-power resonant gate AC Write/Erase DC read non-volatile memory for RF-ID applications and RF imaging schemes

FETs which can be fabricated utilizing HF resistant STI structure, using silicon nitride as isolation material with excellent transistor characteristics, allow a number of other possible device architectures where a released polysilicon gate can be integrated with the FET structure. This possibility can be utilized by making use of high frequency mechanical resonant response of short polysilicon beams in very close proximity to the channel of the transistor [10]-[14].

### 4.11.1 Non-volatile memory

A very promising device architecture is a floating gate memory structure where the control gate of the transistor is suspended over the floating gate, where the only isolation material between the control gate is air (or vacuum)(Figure 4.81). With the application of a small AC signal corresponding to the resonant frequency of the polysilicon beam, forming the control gate, the control gate can be made to touch the top surface of the floating gate of the structure in each cycle. In this manner the

floating gate of the transistor can be brought to the electric potential of the control gate through the transfer of the charges. The floating gate can be charged to the desired level by application of a DC bias on the control gate. When the AC signal is removed, the control-gate stops its movement and the transistor can be operated with a DC bias. Depending on the charge level of the floating gate, the transistor can read a high current or a low current at the read bias just as in a standard floating-gate non-volatile memory.

The gap between the floating gate and the resonant control gate can be made to be smaller than 10 nm using the HF release process. The bottom dielectric, between the floating gate and the channel, can be made out of silicon nitride. The resonant response of the gate can be designed to be in the 1 GHz to 10 GHz range depending on the details of the structure.

The low power operation of this non-volatile memory structure makes this approach a very attractive solution for rewritable RF-ID tags where the power is

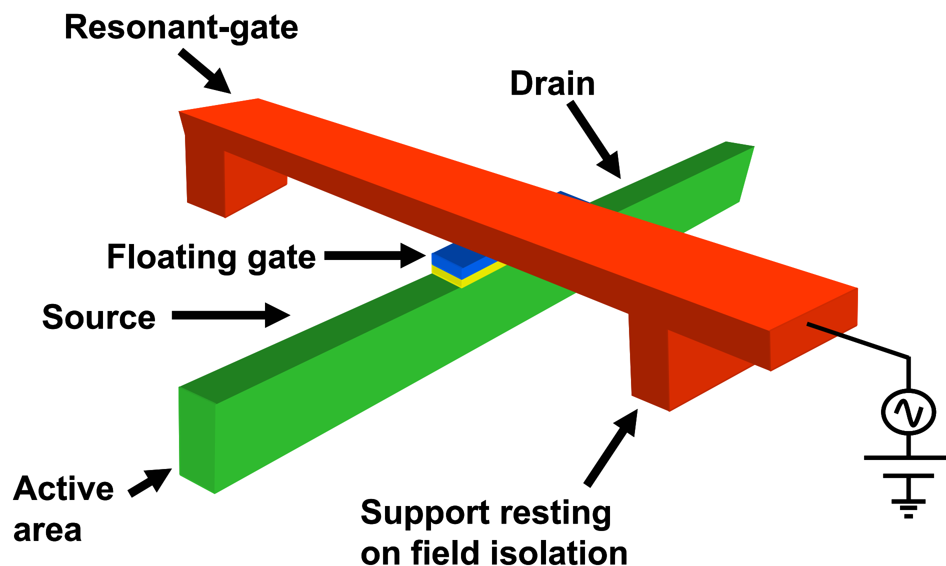


**Figure 4.81** Schematics illustration of the resonant gate non-volatile memory structure. The resonant-control-gate is suspended over the floating gate. Charge transfer is carried out by physically contacting the control-gate to the floating gate

delivered to the device through radiative coupling and it is difficult to achieve > 10 V of write-erase voltages required by standard floating-gate memory structures.

The resonant nature of the write-erase process makes it possible to implement some level of frequency domain addressing of the devices, where application of a signal with different frequency components can selectively write or erase devices. This allows connecting the gates of the devices with different resonant frequency together in a high density array. This scheme maybe particularly useful for write-erase processes for close proximity RF-ID devices where the memory elements can be written or erased all at once by direct radiative coupling of the signal onto the whole array.

The side-gated device architecture gives increased flexibility in this memory structure since the side-gate of the structure can be used as an additional electrode to tune the necessary electrostatic force required to get the anticipated mechanical response from the resonant gate.

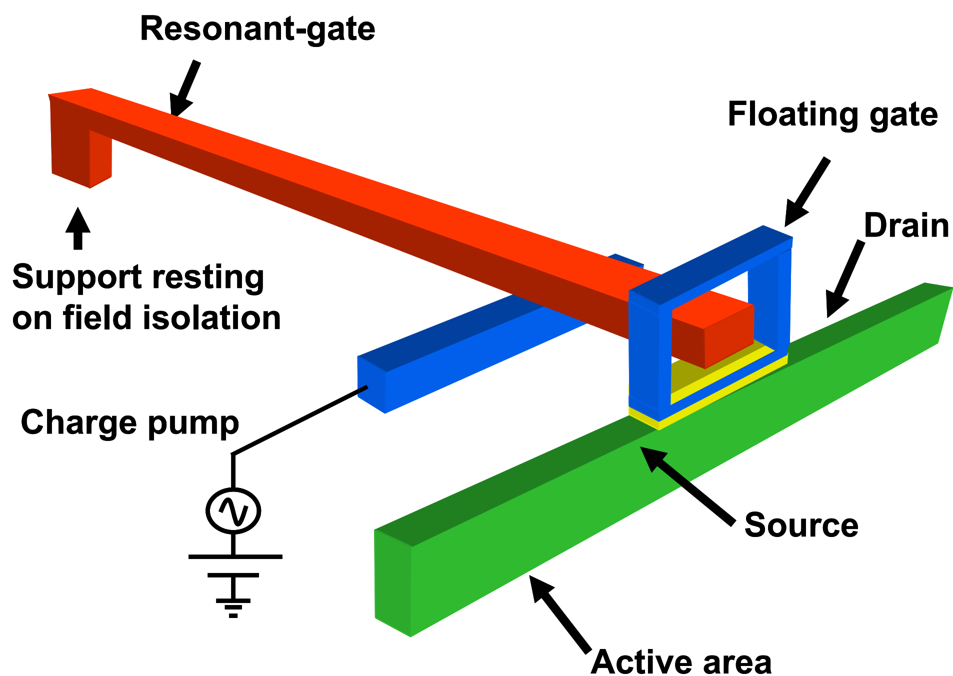


**Figure 4.82** Alternative resonant-gate non-volatile memory structure which can possibly achieve a higher level of charge density in the floating gate.

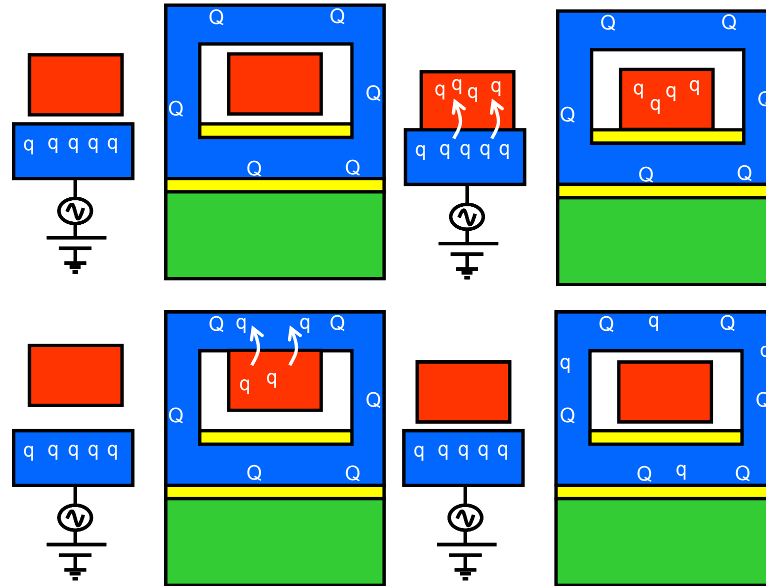

**Figure 4.83** Schematics showing the charge transfer process from the charge pump to the resonant gate (top) and from resonant gate to the floating gate (bottom)

It is also possible to achieve DC write & erase with application of larger biases between the control gate and channel / side-gate. This can possibly be used to achieve high speed 'block-erase' as well as for the applications where the write-erase voltages are not required to be extremely low.

A slightly different structure can be formed by modifying the floating gate to form a ring around the control gate in order to achieve high level of charge density with very small amount of power (Figure 4.82). In this case the charges deposited on the floating gate are expected to distribute themselves on the outer periphery of the structure allowing a higher level of saturation charge which can be achieved on the floating gate (Figure 4.83).

In this case, capacitive coupling to the sides and the top surface of the floating gate are needed to be adjusted properly in order to maximize the effect of the stored charges during read operation. If the capacitive coupling to the top portion of the ring forming the floating gate is stronger than the bottom part, the charges would move to the bottom part of the ring, between the gate and the channel of the device as a large

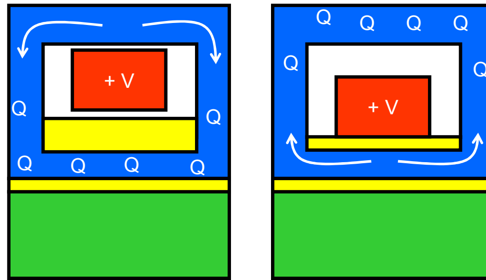


**Figure 4.84** Schematics illustration of movement of stored charges during read operation. Positive charges can move down (left) or up (right) depending on the capacitive coupling ratios to the bottom and top.

bias with the same sign of the stored charges is applied to the gate (Figure 4.84). If the capacitive coupling to the bottom portion is stronger, the stored charges would move to the top portion.

### 4.11.2 Microwave imaging

There is a demand for low cost, high frequency microwave imaging arrays for detection of metal objects for high speed, remote sensing for security purposes [67]. Resonant gate non-volatile memory architectures seen in Figure 4.81 - Figure 4.82 are viable low-cost approaches which can be implemented in these high frequency imaging arrays. The beam designs can be made to correspond the resonant response of the gate structure with the frequency of the RF signal used for imaging. Gates are needed to be either designed to serve as the miniature antennas, or they should be attached to miniature on chip antennas. After the image capture process, the data can be read from the devices at a much lower speed which can easily be handled by the Si circuitry.

# 5 aF Resolution Split C-V Characterization of Nanoscale FETs using Random Fluctuations

## 5.1 Introduction

Carrier mobility and effective device dimensions are important parameters in CMOS design [54]-[57]. Modern deep submicron FET structures exhibit significant edge and stress related effects [14], and non-uniform distribution of carriers due to complicated electric field pattern [41][50]. Due to these effects, which vary with device dimensions, parameters such as carrier distribution and mobilities, effective device width ($W_{eff}$) and length ($L_{eff}$) can only be extracted using C-V measurements performed on the specific small scale devices. Techniques for high resolution

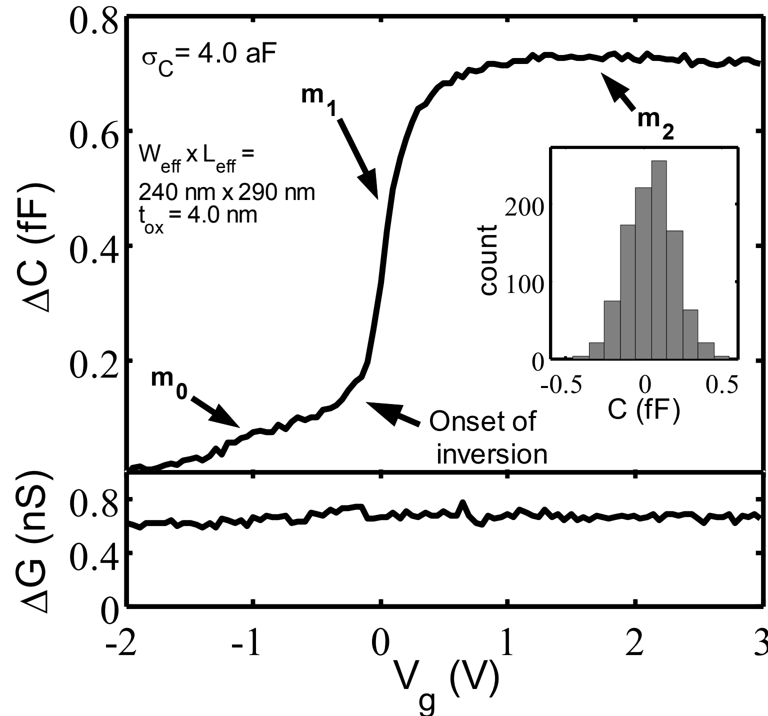


**Figure 5.1** $\Delta C_{g\text{-}s/d}$ and $\Delta G_{g\text{-}s/d}$ characteristics of a side-gated device. Average of 177 sweeps using 45 mV AC signal with 8 point average at each $V_g$ ($V_{side}$ = -1.5 V). Capacitance data has a resolution of 0.5 aF and $\sigma_C$ = 4.0 aF for 1.2 V < $V_g$ < 2.4 V. Inset shows the distribution in acquired C for a fixed bias condition.

capacitance measurements are also needed to quantify the high carrier mobilities ($\mu_{eff}$) reported for carbon-nanotubes [60] and mobilities reported for semiconducting nanowire transistors [61]. In order to avoid capacitance contribution from interface states, room temperature C-V measurements should be performed at a frequency higher than 200 kHz [58]. Capacitance extraction from frequency dependent RF measurements are reported down to a few fF resolution [62][63], Wafer level measurements with down to 0.1 fF resolution using an RLC meter have been reported in [64], however, source/drain dopant gradings are not accounted for, resulting in significant underestimation of hole mobility. In this chapter, reliable wafer level measurements of gate to channel capacitance on side-gated bulk Si nMOSFETs [5][41] are demonstrated down to 0.5 aF resolution and 4 aF standard deviation (Figure 5.1) using 45 mV, 1 MHz AC signal by taking advantage of random fluctuations [34]. Using this technique effective device dimensions and carrier mobilities of the side-gated devices are extracted. The resolution can be improved and the required time for the measurement can be reduced significantly if 100 mV AC signal is used (Figure 4.27 inset).

## 5.2 Experimental details

Wafer level C-V measurements are carried out by using a HP 4275A RLC meter operated at 1 MHz with 20-45 mV AC signal amplitude. The probe station is encapsulated in a shielding box, isolating the ambient electrical noise and reducing the mechanical perturbations on the probes caused by the ambient air currents. Signal output (low) is connected to source and drain, and signal (high) is connected to the gate through *16048A Test Leads* with 1 m coaxial cables, through contacts on the shielding box, short coaxial cables and low frequency probes (Figure 5.2). The bias voltage applied by HP 4275A RLC meter is measured by a multimeter. The RLC

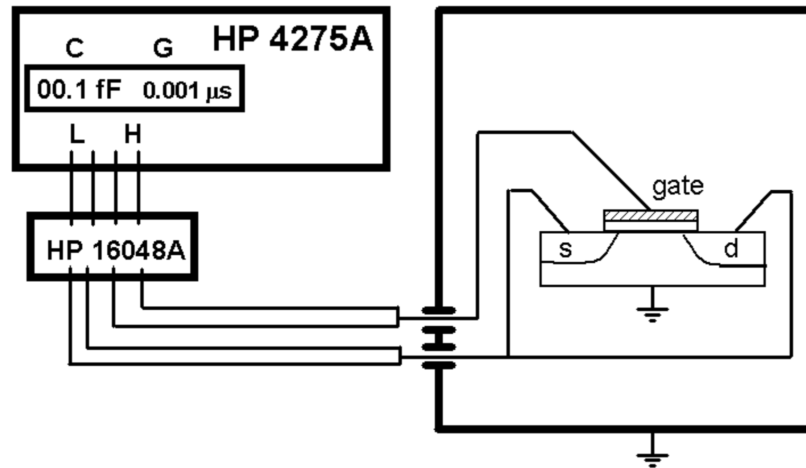


**Figure 5.2** Schematics of the electrical connections for the C-V measurements.

meter and the multimeter are software controlled by a PC through the GPIB network (Section 7.2.3).

Pad to substrate overlap capacitances are bias dependent for semiconducting substrates and are much larger than the inversion layer capacitance of small scale devices. Although this constitutes a significant problem in determining the gate-to-substrate capacitance ($C_{g\text{-}sub}$), it is possible to measure the changes in gate to source/drain capacitance ($C_{g\text{-}s/d}$) accurately when the system is calibrated. The variation in the source/drain to gate contact parasitic capacitance is in the order of 50 aF within the $-2$ V $< V_g <$ 3 V range for the measured devices. This change in the parasitic capacitance is non-linear, however, since it is in parallel with the change in $C_{g\text{-}s/d}$ it can be subtracted out. In order to subtract out this parasitic component, C-V measurements should be performed on devices without gates but with same pad and contact configuration. The details of this procedure are explained in section 7.2.5.3 (page 181).

The *short*-calibration of the system is carried out only once by disconnecting the coaxial cables off the gate and drain probes and connecting them together through

a transmission line approximately twice the length of one probe extension which connects the probe needle to the coaxial cable. The *open*-calibration is carried out at the beginning of each sweep with the probes contacted to the pads and $V_g = 0$ V in order to remove the parasitic contribution of the contact pads. The threshold voltages ($V_t$) of the measured FETs are around 0.3 V.

In a system where the fluctuation level exceeds the measuring instrument resolution, resolution is no longer limited by the resolution of the measuring instrument [65]. Hence, there is an optimum level of noise, in the order of the resolution limit of the instrument, known as stochastic resonance [34]. Increase of noise after this level degrades the signal to noise ratio, hence the standard deviation. As the signal + noise from repeated measurements are averaged, the capacitance value can be obtained with high precision. The standard deviation in the average decreases with the square root of the number of readings (N) and the precision increases linearly with N.

$$\lim_{N\to\infty}\frac{\sum_{i}^{N}C_i}{N}\to C_{true},\sigma_{AVG}=\frac{\sigma_i}{\sqrt{N}}$$

Small changes in the orientation and the placement of the probes lead to sudden jumps of 0.1 - 0.5 fF in capacitance and/or 1 - 5 nS in conductance (G) offset values. The angled probes used to make pressure contact to the pads, in wafer level testing, are prone to slight changes in the orientation and placement over time. Minimizing the time for completing full traces, reduces the probability of these changes during the sweeps. Even though, changes in the offset values during a sweep make the acquired data unusable, changes between two sweeps are undisruptive. Using an HP 4275A RLC meter, 0.1 fF resolution capacitance data can be acquired every 1 second with a fluctuation level of around 0.5 fF (Figure 5.1 inset). Averaging

6-10 readings at every bias point was found to be sufficient for easy detection of any sudden changes in offset values in our setup.

## 5.3 Analysis

C-V traces which do not exhibit sudden discontinuities in C-V or G-V data are selected and averaged (Figure 5.1, Section 7.2.5). The C-V and G-V data have arbitrary offset values depending on the *open*-calibration conditions. If the change in measured quantity is monotonous, such as the conductance value obtained in our measurements, absolute value of the measured quantity cannot be achieved. However, in an FET structure the $C_{g\text{-}s/d}$ -$V_g$ relationship has two characteristic slope changes; first at the onset of inversion ($m_0$ to $m_1$) and second as the device gets into strong inversion ($m_1$ to $m_2$) (Figure 5.1) [21]. Initial slope ($m_0$) in the C-V data is related to the changes in the g-s/d overlap capacitance due to accumulation of the holes in the gate oxide - silicon interface when the device is off [21]. $m_0$ is independent of $L_{eff}$ , scales linearly with $W_{eff}$ and it is more pronounced as the g-s/d overlap length scale becomes comparable to $L_{eff}$. Onset of inversion is calculated by fitting a line to the linear part of the C-V data below the $m_0$-to-$m_1$ kink and identifying the point where the data deviates by $3\sigma_{m0}$ from the fit, where $\sigma_{m0}$ is the standard deviation in the fit (Section 7.2.5.3).

It is possible to extract $W_{eff}$ of the fabricated devices by plotting $C_{inv}$ as a function of design width ($W_{mask}$) for a constant design gate length ($L_{mask}$) (Figure 5.3a). The intercept of the linear fit to the data ($\Delta W$) gives the difference between $W_{mask}$ and $W_{eff}$ [50]. The accuracy of extracted absolute $C_{inv}$ value is verified by plotting $C_{inv}$ as a function of maximum transconductance ($g_m$) data obtained from $I_d$-$V_g$ measurements performed on the same devices (Figure 5.3b). $C_{inv}$ is -12 aF ± 183 aF for $g_m$ = 0 mA/V as obtained from a linear fit, verifying that $C_{inv}$ is extracted accurately from the C-$V_g$.

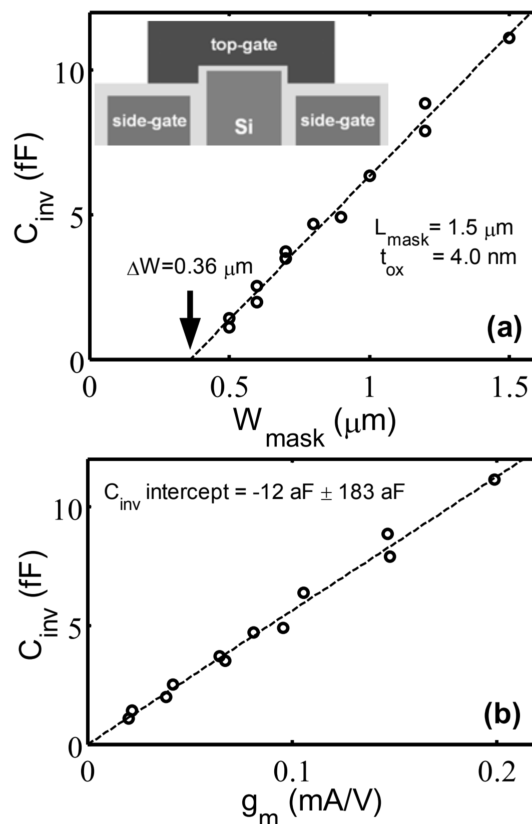


**Figure 5.3** (a) $C_{inv}$ versus $W_{mask}$ for $L_{mask}$ = 1.5 μm. Inset shows cross-section schematics of a side-gated FET. (b) $C_{inv}$ versus $g_m$ for the same devices. Dashed lines are linear fits to the data.

data. The error in the fit is dominated by errors on the active and gate level masks and process variations.

## 5.4 Application of this technique for fA resolution current measurements

The technique used for achieving aF resolution capacitance data can be applied to current measurements to achieve a resolution much better than the current measuring equipments resolution limit. The resolution limit of an HP 4145B parameter analyzer is 50 fA in the highest sensitivity range. The typical reading obtained from this parameter analyzer is as seen in Figure 5.4 when the probe is lifted slightly above the pads to disconnect the probe from the device. The ambient noise

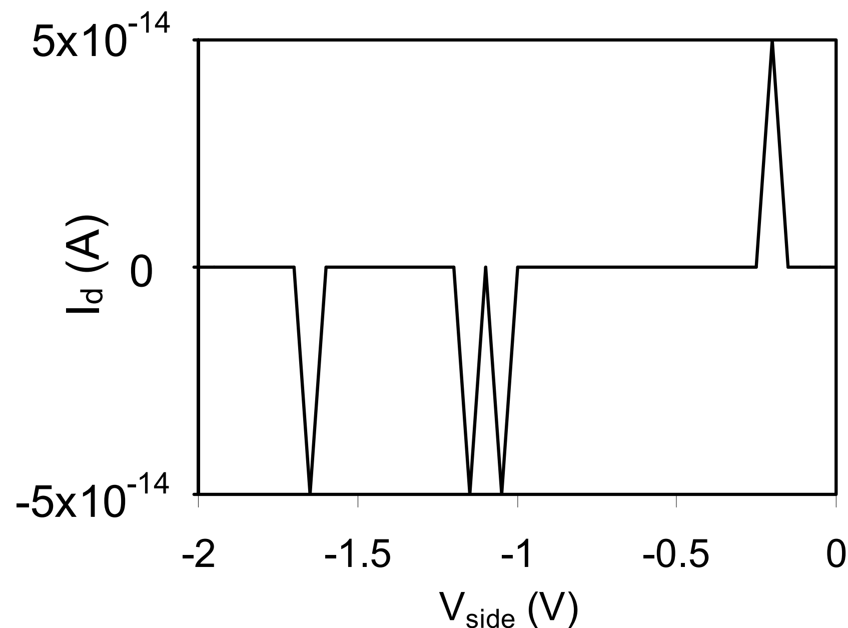


**Figure 5.4** A typical drain current reading when the drain probe is lifted. The reading is intended for estimation of leakage current in the probe and cable assembly. The resolution limit of the parameter analyzer is 50 fA.

results in slight deviations from zero in the measured current, while the grand majority of the data points are measured to be zero. By averaging a large number of traces as such, it is possible to get a good measure of the leakage currents in the probe and cable assembly which are less than 50 fA (Figure 5.5).

The drain to substrate current can be measured in the same manner after the probe is connected to the drain of a side-gated device and sweep the side-gate bias. Averaging a large number of traces shows that the minimum leakage current in a reverse biased drain to substrate diode is less than the leakage current in the probe and cable assembly used to carry out the measurement (Figure 5.5). The leakage currents in the setup are in the order of 10 fA, 5 times smaller than the resolution limit of the instrument. It is possible to obtain a measure for the lowest level of current leakage in the drain to substrate diode by subtracting the measured leakage currents in the setup from the values obtained from the current measurement performed on the drain to

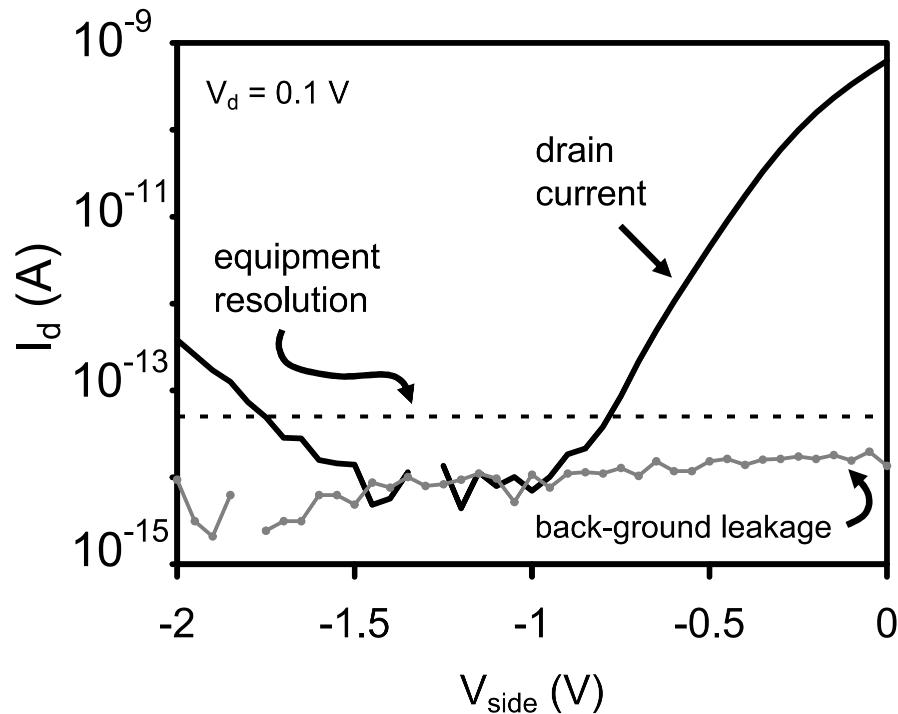


**Figure 5.5** Average of 114 I-V measurements of drain to substrate reverse biased diode (solid) and average of 143 I-V measurement of the drain leakage when the drain probe is not connected to the pad (gray dots). The dashed line shows the parameter analyzer's resolution limit of 50 fA. The leakage current measured for the diode is less than the current leakage in the probe and cable assembly.

substrate diode. It is possible to achieve a very reliable measure of the leakage currents, with better than 10 fA resolution if a larger number of measurements are performed.

## 5.5 Conclusion

In this chapter it is demonstrated that the absolute capacitance information of the inversion layer in nanoscale FETs can be extracted with sub-aF resolution using an instrument with 0.1 fF resolution in a split C-V setup by utilizing the random fluctuations in the system and non-linear response of gate to source/drain capacitance. The resolution of the measurement is only limited by the total acquisition time. Accuracy of calculated inversion layer capacitance depends on how well the onset of

inversion is extracted. Using the capacitance information, reliable effective carrier mobility and effective device dimensions of nanoscale FETs with complicated 3D geometries, nanowires, nanotubes, and device-dependent stress variations can be extracted. It is possible to achieve fA resolution current measurements using the same technique.

## 5.6 Acknowledgment

I would like to thank Arvind Kumar from IBM T.J. Watson Research Center for insightful discussion on capacitance measurements.

# 6 Conclusions

A nanometer scale air-gap FET structure integrated with on-chip microfluidic delivery system is successfully fabricated using silicon nitride based shallow trench isolation scheme. The processes developed for the fabrication of the transistor, using optical lithography, allow the scaling of the channel width of the transistors below 10 nm, and formation of tunnels with less than 10 nm in height, passing between the gate and the channel, by removal of sacrificial oxide. Achieving good electrical performance in the FET operation at narrow widths is critical for the desired high level of sensitivity. The relative contribution of peripheral electrical leakage at the active-isolation interfaces become increasingly important as the device width is scaled down. These leakage currents degrade the device sensitivity and result in increased noise.

The side-gated approach resulted in effective suppression of peripheral leakage currents. In addition, short channel effects are significantly suppressed in narrow channel devices, which in turn permit gate length scaling beyond the scaling limits of standard planar bulk MOSFETs. In the case of ultra narrow channel devices, significant threshold voltage tunability is achieved.

Suppression of peripheral leakage currents leads to close to ideal DC performance with less than 65 mV/dec subthreshold slope and $I_{on}/I_{off} > 6 \times 10^{10}$ in wide and long channel devices. In the case of narrow channel devices, negative bias on the side-gates accumulates holes in the volume between the source and the drain junctions, reducing the junction depletion depth, and raising the potential barrier between the source and drain. Hence, short channel effects are totally eliminated, as demonstrated for devices with 40 nm effective width, 150 nm physical gate length exhibiting DIBL = 2 mV/V. Drive currents exceeding 1.5 mA/μm and $I_{on}/I_{off} > 2 \times 10^9$ are achieved in sub-70 nm channel length devices.

In the ultra narrow channel side-gated devices, where the device width is reduced down to sub-10 nm, significant threshold voltage response to side-gate bias is observed. The electrostatic threshold voltage tunability range exceeds 2.5 V with an average sensitivity of $\delta V_t/\delta V_{side}$ = -1.55 V/V, higher than any of the threshold voltage tunable devices reported so far. The sensitivity exhibits a quadratic behavior with maximum $\delta V_t/\delta V_{side}$ = -2.5 V/V and minimum $\delta V_t/\delta V_{side}$ = -0.8 V/V for $-0.3\ V < V_{side} < -2\ V$ leading to a threshold voltage variation from 1.4 V to 4 V.

The performance parameters for side-gated devices are comparable or better than state-of-the-art silicon devices used for high-performance and low-power VLSI applications. Threshold voltage tunability achieved in narrow and ultra-narrow channel side-gated devices allows implementation of power adaptive circuits and the use of this structure as a multi-gate building block for analog circuit applications.

Planar side-gated ultra-narrow width device architecture can be used for detection of localized charges over long biomolecules. This device architecture allows electrostatic confinement of electrons to the central part of the silicon channel, which is expected to minimize the current fluctuations due to the interface traps on the two sides of the structure, while improving the spatial resolution of the sensor. The demonstrated results suggest that it is possible to achieve single nucleotide resolution using the side gated FET based sensor where the channel width can be electrostatically reduced down to 2 nm. In this case, the data acquired from the sensor would be a convolution of potential perturbations due to 6 nucleotide long molecule sections. A signal processing scheme is needed to extract the sequence information from the time-domain information obtained from the sensor.

Using the side-gated device architecture, it is possible to reduce the channel width down to slightly less than 2 nm by confining the channels to the two sides of the active area instead of the center, utilizing the contribution of the positive interface

fixed charges and tuning the side-gate biases. This approach can increase the spatial resolution; however, current fluctuations due to trapping events at the Si-SiN interface can deteriorate the device sensitivity.

The ultra-narrow channel device structure should be engineered to minimize the inversion layer width, channel capacitance, and the fluctuations in the current level due to traps in order to achieve the required sensitivity to the variations in local charges on the sample, which are separated by 0.34 nm in the case of DNA and RNA.

Side-gated device architecture has served as a very valuable diagnostic tool, allowing evaluation of the leakage currents, their causes and level of sensitivity which can be achieved from ultra narrow-channel devices. As a result of this diagnosis, an ultra-narrow channel pFET device utilizing silicon nitride STI and the processes described in this thesis came into sight as a possible alternative for achieving high sensitivity and spatial resolution. In the case of a pFET, the positive fixed charges at the Si-$Si_3N_4$ interfaces would rather enhance the device performance by reducing the leakage currents and increasing the channel confinement. These positive fixed charges would suppress the drain to source peripheral leakage currents. The drain to substrate leakage is also expected to be very low, due to accumulation of low-doped body-STI interface. Significant confinement of holes to the central part of the device would be achieved, resulting in effective device width much smaller than the physical dimension for sub-10 nm channel widths. This potential well for holes, formed in the central part of the channel, can be as effective as a potential well formed by side-gate biasing in an nFET, and it can further be enhanced with the employment of a positively biased side-gate structure in the pFET.

The ability of shifting the threshold voltage of the device by storing charges on the two sides of the narrow channel enables the side-gated device geometry to be used as a non-volatile memory structure. This approach utilizes the combined effect of

electrostatics and quantum confinement effects. The decoupled write/erase and read operations of this structure and the ability of changing the threshold voltage beyond 1.3 V make this structure a good candidate for extending the scalability of FET based non-volatile memories into sub-50 nm gate length range.

Compatibility with HF release processes, using silicon nitride device isolation, provides increased flexibility for integration of HF-released active and passive elements, such as resonant gate structures, with electronics for a variety of different applications including alternative non-volatile memories and sensors. The side-gated device architecture allows use of high-K and low-K isolation materials for a large number of applications and achieves very low levels of leakage currents. Side-gated devices with sub-10 nm channel width can be used to study quantum effects in extremely confined geometries. The use of optical lithography and CMOS compatible processes for building these structures makes it possible to build large number of devices in a cost efficient manner. This also allows building of very large scale integrated circuits with ultra narrow devices which exhibit non-classical behavior.

Mobility and carrier concentration of ultra-small devices, nanowires and nano-tubes can be studied through C-V measurements conducted on the actual small-scale devices using the described sub-aF resolution C-V measurement technique. This technique, utilizes ambient noise in order to achieve a resolution more than 100 times better than the resolution of the equipment used for the measurements. The accuracy of the technique relies on non-linear behavior of the measured C-V characteristics since the parasitic capacitances in the system are several orders of magnitude larger. Inversion layer capacitance in FET structures can be extracted with aF accuracy making use of the non-linearity in the source/drain to gate C-V characteristics. The ability to directly measure these small capacitances can lead to a better understanding of carrier transport in highly confined geometries.

# 7 Appendix

## 7.1 Details of fabrication process

The details of the side-gated device fabrication, monolithically integrated with microfluidic delivery system is given in a table format as below. The masks used for the process are named as 'ALI 0 ALIGN', 'ALI 1 STI', etc.

| | Task | Tool | Process | Par. 1 | Par. 2 | Par.3 | Rate |
|---|---|---|---|---|---|---|---|
| 1 | Alignment Marks | | RCA Clean | | | | |
| 2 | | MOS Oxide Furnace | Wet oxidation | 1000 C | 40 min | 300 nm | |
| 3 | | YES wafer priming oven | vapor prime HMDS | | 30 min | | |
| 4 | | | spin resist | 620-7i | 4000 RPM | 60 sec | |
| 5 | | Hot plate | Bake | | 90 C | 75 sec | |
| 6 | | AutoStep | ALI 0 ALIGN | 0.35 sec | F=0 | | |
| 7 | | Hot plate | Bake | | 115 C | 75 sec | |
| 8 | | | Develop | 300 MIF | 90 sec | | |
| 9 | Etch Si | Aura 1000 | Descum D | O2 | heated | 15 sec | |
| 10 | | Oxford 80 | etch oxide | CHF3 / O2 | 15 min | 300 nm | ~ 30 nm/min |
| 11 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100 nm/min |
| 12 | | Oxford 80 | etch oxide | CHF3 / O2 | 1 min | | ~ 30 nm/min |
| 13 | | PT 720 | etch Si | Cl2 & BCl3 | 10 min | 1 μm | ~ 100 nm/min |
| 14 | STI | YES wafer priming oven | vapor prime HMDS | | 30 min | | |
| 15 | | | spin resist | 620-7i | 4000 RPM | 60 sec | |
| 16 | | Hot plate | Bake | | 90 C | 75 sec | |
| 17 | | AutoStep | ALI 1 STI | | 0.35 sec | F=0 | |
| 18 | | AutoStep | ALI 11 MASK | | 0.5 sec | F=0 | |
| 19 | | HTG Contact Aligner | expose between dies | | 30 sec | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 20 | | Hot plate | Bake | | 115 C | 75 sec | |
| 21 | | | Develop | 300 MIF | 90 sec | | |
| 22 | | Aura 1000 | Descum D | O2 | heated | 15 sec | |
| 23 | Etch Si | Oxford 80 | etch oxide | CHF3 / O2 | 12 min | 300 nm | ~ 30 nm/min |
| 24 | | Oxford 80 | etch resist | O2 | 15 min | | ~ 100 nm/min |
| 25 | | Oxford 80 | etch oxide | CHF3 / O2 | 1 min | | ~ 30 nm/min |
| 26 | | PT 720 | etch Si | Cl2 & BCl3 | 10 min | 1 μm | ~ 100 nm/min |
| 27 | Clean Side-Wall | | RCA Clean | | | | |
| 28 | | MOS Oxide Furnace | Wet oxidation (no Anneal) | 850 C | 30 min | 40-50 nm | |
| 29 | | Diluted HF | Wet etch oxide | | remove all oxide | | |
| 30 | Body Doping | B implant | 3.5e17 /cm3 @ 0.5 μm (peak ) | 5e13 cm-2 100 KeV | | | |
| | | | RCA Clean | | | | |
| 31 | | MOS Oxide Furnace | Wet oxidation ( + Anneal) | 850 C | 30 min | 40-50 nm | |
| 32 | | LPCVD Polysilicon Furnace | P++ poly | 600 C | 30 min | 100 nm | double spaced |
| 33 | | MOS Oxide Furnace | Wet oxidation | ~ 350 nm oxide | 950 C | 60 min | |
| 34 | | | Anneal | 950 C | 30 min | | |
| 35 | | Diluted HF | Wet etch oxide | remove all oxide | | | |
| 36 | SiN STI with Side-gate | LPCVD Nitride Furnace | Stochiometric Nitride | 800 C | 6 min | ~ 20 nm | single spaced |
| 37 | Side-gate | LPCVD Polysilicon Furnace | n++ poly | 600 C, 300 mT | 200 min | 380 - 400 nm | |
| 38 | | GSI PECVD | low dep. Rate ox. | 400 C | 60 sec | ~ 130 nm | |
| 39 | photolith - Side-Gate | YES wafer priming oven | Vapor prime HMDS | | 30 min | | |
| 40 | | | spin resist | 897-12i | 4000 RPM | 60 sec | |
| 41 | | Hot plate | Bake | 90 C | 75 sec | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 42 | | AutoStep | ALI SG | | 0.35 sec | F=0 | |
| 43 | | HTG Contact Aligner | Between Dies | | 30 sec | | |
| 44 | | Bake | | 115 C | 75 sec | | |
| 45 | | Develop | 300 MIF | | 90 sec | | |
| 46 | Etch Side-Gate | Aura 1000 | Descum D | O2 | | 15 sec | |
| 47 | | Oxford 80 | etch oxide | CHF3 / O2 | 5 min | | ~ 32 nm/min |
| 48 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100 nm/min |
| 49 | | Oxford 80 | etch oxide | CHF3 / O2 | 1 min | | ~ 32 nm/min |
| 50 | | PT 720 | etch Si | Cl2 & BCl3 | 5 min | | ~ 100 nm/min |
| 51 | | wet etch oxide | | BOE (6:1) | remove all | | ~ 100 nm/min |
| 52 | | LPCVD Nitride Furnace | Stoic Nitride | 800 C | 25 min | ~ 150 nm | |
| 53 | | LPCVD Nitride Furnace | Low Stress Nitride | 850 C | 300 min | ~ 1100 nm | |
| 54 | Planar-ization | CMP | Chuck 25, Table 30 RPM | Slurry 150 ml/min | P=1psi, Down F=8psi | 7 min | ~800 nm left |
| 55 | Leveling | Wet etch Nitride | | 49 % HF | 1 min | | |
| 56 | Touch polish to get flat Si surface | CMP | Chuck 25, Table 30 RPM | Slurry 150ml/min | P=1psi, Down F=8psi | 20 s | |
| 58 | Gate Stack | LPCVD Nitride Furnace | High Temp Oxide Dep. | 850 C | 10 min | 10 nm | ~ 1 nm/min |
| 59 | | LPCVD Nitride Furnace | Stoic Nitride | 800 C | 10 min | 30 nm | |
| 60 | | LPCVD Polysilicon Furnace | n++ poly | 600 C, 300mTorr | 200 min | 400 nm | |
| 61 | Oxide Etch Mask Dep. | GSI PECVD | Low dep rate oxide | 400 C | 60 sec | ~ 130 nm | |
| 62 | photolith - Gate | | vapor prime HMDS | | 30 min | | |
| 63 | | | spin resist | 620-7i | 4000 RPM | 60 s | |

| 64 | | Hot plate | Bake | 90 C | 75 sec | | |
|---|---|---|---|---|---|---|---|
| 65 | | AutoStep | ALI 1 GATE | | 0.35 sec | F=0 | |
| 66 | | AutoStep | ALI 11 MASK | | 0.5 sec | F=0 | |
| 67 | | HTG Contact Aligner | Between Dies | | 30 sec | | |
| 68 | | Hot plate | Bake | 115 C | 75 sec | | |
| 69 | | Develop | 300 MIF | | 90 sec | | |
| 70 | Etch Gate Poly | Aura 1000 | Descum D | O2 | | 15 s | |
| 71 | | Oxford 80 | etch oxide | CHF3 / O2 | 5 min | slight over etch | ~ 32 nm/min |
| 72 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100 nm/min |
| 73 | | Oxford 80 | etch oxide | CHF3 / O2 | 1 min | | ~ 30 nm/min |
| 74 | | PT 720 | etch Si / SiN stop on SiO2 | Cl2 & BCl3 | 6 min | 400 nm / 30 nm | 100 / 20 nm/min |
| 75 | Self-aligned Source / Drain | | RCA Clean | | | | |
| 76 | Side-wall formation | MOS Oxide Furnace | dry oxidation | 800 C | 30 min | 7 nm | |
| 77 | | implant As | 7° Tilt, 90° Rot. | 5e14 cm-2 30 keV | | | |
| 78 | Remove Mask oxide | | BOE (30:1) | remove all | | | 30 nm/min |
| 79 | | MOS Clean | | | | | |
| 80 | Backside etch | Spin resist on front side | | 897-12i | 3000 RPM | | |
| 81 | | Oxford 80 | etch films on backside | CF4 | 60 min | | |
| 82 | Backside Polish | CMP | CMP backside | oxide Slurry | ~ 9 min | | |
| 83 | | Hamatech Clean | | | | | |
| 84 | | IPA & Acetone | Strip Resist | | | | |
| 85 | | MOS Clean | | | | | |
| | Tunnel Formation | | | | | | |
| 86 | Tunnel Sacrificial Ox. Dep. | GSI PECVD | low dep. Rate oxide | 400 C | 2 min | ~ 250 nm | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 87 | large tunnels | | vapor prime HMDS | | | | |
| 88 | | | spin resist | 897-12i | 4000 RPM | 60 sec | |
| 89 | | AutoStep | ALI FL2 | | 0.9 sec | F=0 | |
| 90 | | AutoStep | ALI 7 VIA | | 0.45 sec | F=0 | |
| 91 | | YES oven - Image Reverse | NH3 | | | | |
| 92 | | HTG Contact Aligner | Flood expose | | 30 sec | | |
| 93 | | Hot plate | Bake | 115 C | 3 min | | |
| 94 | | Develop | 300 MIF | | 90 sec | | |
| 95 | Tunnel Etch 1 | Thin down oxide to 20 nm | BOE (30:1) | 7 min | | | ~33 nm/min |
| 96 | | Inter. Thick. Measurement | shoot for ~ 20-25nm oxide | | | | |
| 97 | | Strip Resist | Spin Acetone & IPA | | | | |
| 98 | shallow tunnels | | vapor prime HMDS | | | | |
| 99 | | | spin resist | 897-12i | 4000 RPM | 60 sec | |
| 100 | | Hot plate | Bake | 90 C | 75 sec | | |
| 101 | | AutoStep | ALI FL1 | | 0.9 sec | F=0 | |
| 102 | | AutoStep (optional) | ALI FL2 | | 0.9 sec | F=0 | |
| 103 | | AutoStep (optional) | ALI 7 VIA | | 0.45 sec | F=0 | |
| 104 | | YES oven - Image Reverse | NH3 | | | | |
| 105 | | HTG Contact Aligner | Flood expose | | 30 sec | | |
| 106 | | Hot plate | Bake | 115 C | 3 min | | |
| 107 | | Develop | 300 MIF | | 90 sec | | |
| 108 | Tunnel Etch 2 | Remove all surface oxide | BOE (30:1) | | | 1.5 min | 33nm/ min |
| 109 | | Inter. Thick. Measurement | shooting for ~ 0 nm oxide | over etch to remove gate mask oxide | | | |
| 110 | | Strip Resist | Spin Acetone & IPA | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 111 | Tunnel Cap<br>Nitride Dep. | LPCVD<br>Nitride<br>Furnace | Stoic<br>Nitride | 800 C | | 33 min | |
| 112 | | | LS Nitride | 850 C | ~ 700<br>nm | 240<br>min | |
| 113 | Fluid Open | YES oven | vapor<br>prime<br>HMDS | | | | |
| 114 | | | spin resist | 897-12i | 4000<br>RPM | 60 sec | |
| 115 | | Hot plate | Bake | 90 C | 75 sec | | |
| 116 | | AutoStep | ALI  FLOP | | 0.9 sec | F=0 | |
| 117 | | HTG Contact<br>Aligner | Between<br>Dies | | 30 sec | | |
| 118 | | Develop | 300 MIF | | 90 sec | | |
| 119 | Etch Nitride<br>open | Aura 1000 | Descum D | 15 sec | | | |
| 120 | | Oxford 80 | CHF3 / O2 | 25 min + 1<br>min | | | |
| 121 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100<br>nm/min |
| 122 | Empty<br>Tunnels | wet etch<br>oxide | HF | 5-10 min | | | |
| 123 | Test<br>Tunnels | drop of DI<br>water | under μ-<br>scope | | | | |
| 124 | Recess<br>nitride for<br>metal | YES oven | vapor<br>prime<br>HMDS | | | | |
| 125 | | | spin resist | 897-12i | 3000<br>RPM | 60 sec | |
| 126 | | Bake | Hot plate | 90 C | 75 sec | | |
| 127 | | AutoStep | ALI 8<br>METAL | | 0.9 sec | F=0 | |
| 128 | | HTG Contact<br>Aligner | Between<br>Dies | | 30 sec | | |
| 129 | | Oxford 80 | CHF3 / O2 | leave<br>~150 nm | | | |
| 130 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100<br>nm/min |
| 131 | Via | YES oven | vapor<br>prime<br>HMDS | | | | |
| 132 | | | spin resist | 897-12i | 4000<br>RPM | 60 sec | |
| 133 | | Hot plate | Bake | 90 C | 75 sec | | |
| 134 | | AutoStep | ALI 7 VIA | | 0.9 sec | F=0 | |
| 135 | | HTG Contact<br>Aligner | Between<br>Dies | | 30 sec | | |
| 136 | | Hot plate | Bake | 115 C | 75 sec | | |
| 137 | | Develop | 300 MIF | | 90 sec | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 138 | Etch via | Aura 1000 | Descum D | 15 sec | | | |
| 139 | | Oxford 80 | CHF3 / O2 | leave ~ 20 nm | | | |
| 140 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100 nm/min |
| 141 | Open side-gate contact | YES oven | vapor prime HMDS | | | | |
| 142 | | | spin resist | 897-12i | 3000 RPM | 60 sec | |
| 143 | | Bake | Hot plate | 90 C | 75 sec | | |
| 144 | | AutoStep | ALI SG OP | | 0.9 sec | F=0 | |
| 145 | | Hot plate | Bake | 115 C | 75 sec | | |
| 146 | | Develop | 300 MIF | | 90 sec | | |
| 147 | | Oxford 80 | CHF3 / O2 | slight over-etch | | | |
| 148 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100 nm/min |
| 149 | | wet etch nitride | HF | down to Si in vias | | | |
| 150 | Channel oxide regrowth | Dry Oxidation Furnace | shoot for ~2-3nm oxide | 700 C | 20 min | | |
| 151 | Metal Contacts | YES oven | vapor prime HMDS | | | | |
| 152 | | | spin resist | LOR-10A | 3000 RPM | 60 sec | |
| 153 | | Hot plate | Bake | 160 C | 5 min | | |
| 154 | | | spin resist | 897-12i | 4000 RPM | 60 sec | |
| 155 | | Hot plate | Bake | 90 C | 75 sec | | |
| 156 | | AutoStep | ALI 8 METAL | | 0.9 sec | F=0 | |
| 157 | | Develop | 300 MIF | | 90 sec | | |
| 158 | | Aura 1000 | Descum D | 15 sec | | | |
| 159 | | wet etch oxide | BOE (30:1) | 30 sec | | | |
| 160 | Metal | Evaporate Ti | 200 nm | | | | |
| 161 | | Evaporate Al | 700 nm | | | | |
| 162 | | lift-off | 1165 res. Remover | | over-night | | |
| 163 | Metal Anneal | anneal | 350 C | 15 min | | | |
| 164 | Electrical Testing | | | | | | |
| 165 | | | | | | | |
| 166 | Seal Irrigation Holes | GSI PECVD | Oxide Dep. 2 to 3 Microns | 400 C | ~10-15 min | | |

| 167 | contact open, fluid I/O | YES oven | vapor prime HMDS | | | | |
|---|---|---|---|---|---|---|---|
| 168 | | | spin resist | 897-12i | 4000 RPM | 60 s | |
| 169 | | Hot plate | Bake | 90 C | 75 sec | | |
| 170 | | AutoStep | ALI CONTOP | | 0.9 sec | F=0 | |
| 171 | | AutoStep | ALI I/O | | | | |
| 172 | | HTG Contact Aligner | Between Dies | | 30 sec | | |
| 173 | | Hot plate | Bake | 115 C | 75 sec | | |
| 174 | | Develop | 300 MIF | | 90 sec | | |
| 175 | Etch | Aura 1000 | Descum D | 15 sec | | | |
| 176 | | Oxford 80 | CHF3 / O2 | down to Al | | | |
| 177 | | Oxford 80 | etch resist | O2 | 10 min | | ~ 100 nm/min |
| 178 | photolith fluid I/O | YES oven | vapor prime HMDS | | | | |
| 179 | | | spin resist | 897-12i | 4000 RPM | 60 s | |
| 180 | | Hot plate | Bake | 90 C | 75 sec | | |
| 181 | | AutoStep | ALI I/O | | 0.9 sec | F=0 | |
| 182 | | HTG Contact Aligner | Between Dies | | 30 sec | | |
| 183 | | Hot plate | Bake | 115 C | 75 sec | | |
| 184 | | Develop | 300 MIF | | 90 sec | | |
| 185 | Etch | Aura 1000 | Descum D | 15 sec | | | |
| 186 | Clear inner surfaces of the tunnels | Diluted HF (50:1) | | | | | |
| 187 | | Acetone & IPA | remove resist | | | | |

## 7.2 Software tools developed for instrument control for electrical characterization

### 7.2.1 Parameter Analyzer

The parameter analyzer controller program is developed for HP 4145B parameter analyzers using Labview$^{TM}$ 7.0 (Figure 7.1). This program can also be used for HP 4145A parameter analyzers by increasing the delays in the program.

The program has the indexing and the numbering functions which is identical in all of the measurement tools I have developed. The index file stores a significant portion of the information about the measurements including; the time and the data, file name, most of the measurement parameters, the user comments and wafer label entered in the windows at the bottom portion of the control panel. The index file path is displayed on the top portion of the control panel and it can be changed by the user. The 'file path' is the directory and file name prefix for the measurement. The data file name is composed by appending a file number and a suffix of '.data' to the prefix. The file number is kept in a file in the hard drive. The number is incremented for each measurement if the counter is turned on by pressing the 'count' button. The file number is not incremented if the counter is off. The file number can be reset to a desired number by pressing the 'reset' button and entering the 'offset' value. The data file name is constructed and displayed in the 'file name' field as the program is run.

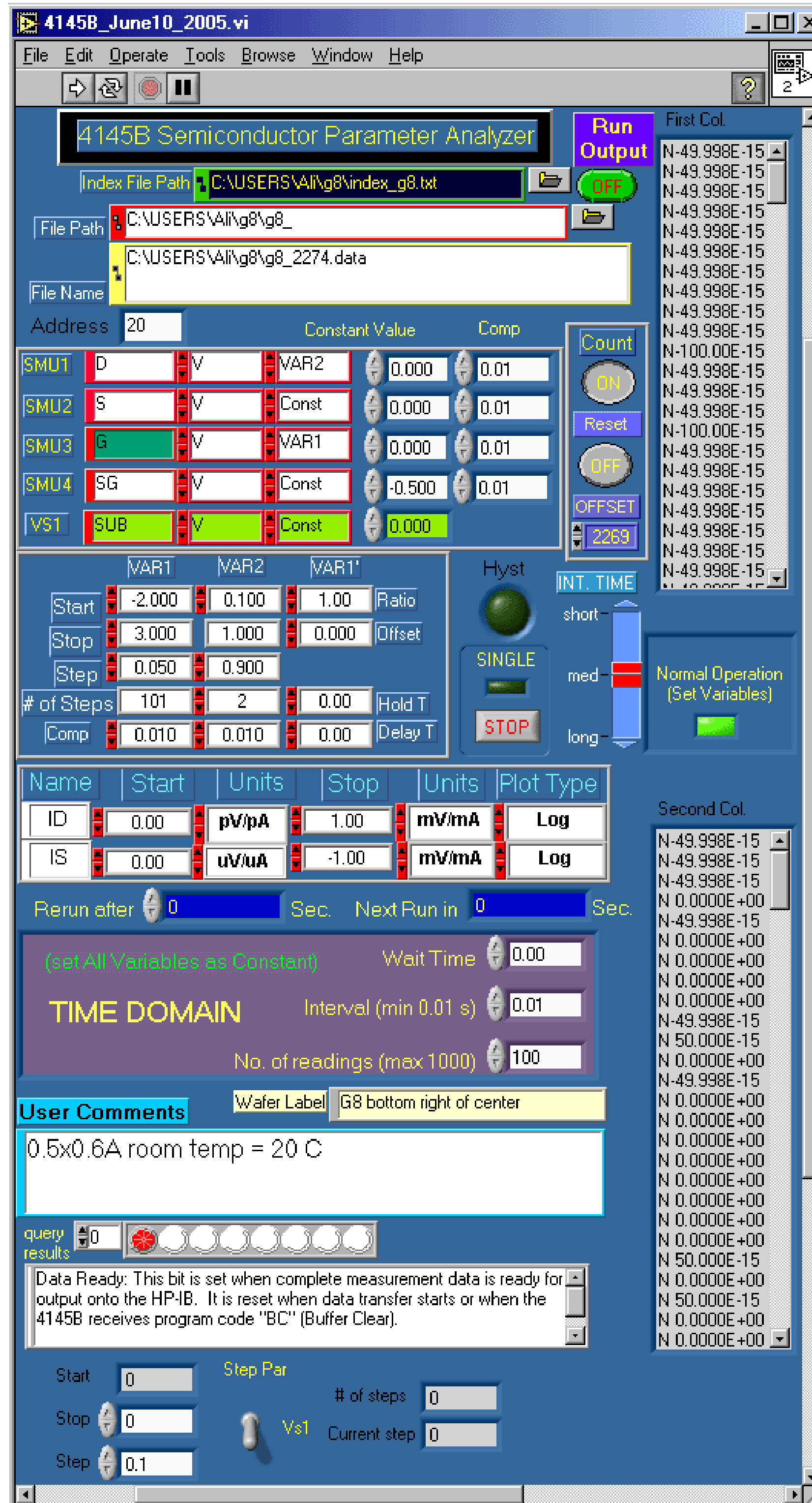


**Figure 7.1** Front panel of parameter analyzer HP 4145B controller developed using Labview™ 7.0.

The parameter analyzer GPIB address should be entered in the ‘address’ field. Parameter names, functions and compliances can be set for four SMUs and VS1 (one of the two sources in the HP 4145B without measurement capability).

The parameter values for variable 1, variable 2 and variable 1’, hold time and delay time can be entered from the front panel and these values are transmitted to the parameter analyzer and executed if the ‘Normal Operation (Set Variables)’ light is lit. The program acquires data without setting these variable values if this button is turned off, displaying ‘do not set variables’. The time for setting the parameter values is eliminated for repeating the same measurements if this button is turned off. The integration time is set by the slide rule on the right side.

Parameter analyzer can be set to run a single trace or can be put in the repeated mode by turning on the ‘repeat’ button, which otherwise is labeled as ‘single’. The repeated measurements can be stopped by clicking the stop button below this switch. In this case, the data from the last measurement is transferred to the computer. If undesired values are accidentally entered as the parameters for the measurement, the measurement can be stopped by clicking on the same stop button on the front panel of the program.

At the end of the run, the program changes the order of the values for variable 1 in order to do a reverse sweep if the ‘Hyst’ button is pressed. This option is useful for observation of charge trapping in the dielectrics surrounding the channel of the transistor.

The two parameters of interest can be displayed on the parameter analyzer screen and transferred over to the computer. The display setting for the parameter analyzer are controlled for each parameter next to the ‘name’ field which determines the parameter to be plotted. The second ‘name’ field can be left blank if only one parameter is going to be measured.

If the program is run indefinitely by using the automatic rerun option of Labview™, a delay time between the measurement can be set by changing the value set in the 'rerun after' field in seconds. This option can be useful for large number of measurements done on devices which change over time.

The parameter value for SMU4 or VS1 can be changed in a loop by setting the stop and the step values at the bottom portion of the control panel. Using this option a third parameter, other than variable 1 and 2, can be incremented. The switch is needed to be set to the parameter which is wanted to be looped. If the stop value of the parameter is the same as the start value, the program is executed only once. This feature is useful for gathering the parameters like DIBL, SS etc. for different substrate or side/back-gate biases. The plotting program has a feature of plotting sequential data files one after another automatically in order to allow easy viewing of large number of files generated using this additional loop. The plotting program also logs all the calculated parameters for the data files in a tab delimited text file for convenient plotting of the parameters.

The data acquired from the parameter analyzer is displayed separately for each measured quantity on the right side for debugging purposes. If no data is being received from the parameter analyzer, the problem is most likely to be caused by the GPIB network. This can be fixed by either restarting Labview™, restarting the computer or the parameter analyzer.

It is possible to automatically run another window of the same program, saved with a different file name, if the 'run output' button is pressed. In this case the parameters on the second window can be set for output characteristics if the main program is used for transfer characteristics, allowing efficient device characterization.

The time domain control section is set for time domain measurements. In order to run a time-domain measurement, all of the parameters should be set to be constant.

### 7.2.2 Software tool developed for analysis and algorithms used for MOSFET parameter extraction

The plotting program, ‘plot_all’ is developed using Labview™ 7.0. The program plots the data in the large window and calculates a large number of parameters which are mainly suited for transfer curves of an FET (Figure 7.2). Program is setup to plot the data by treating the first column as the x-axis data and the rest of the columns as y-axis data. The first line in the data file is expected to be the title row and it is displayed as “File Header”. Different data sets can be plotted together if the ‘clear graph’ button is not pressed. The last data replaces the previously plotted data if the ‘clear graph’ button is pressed. ‘clear graph’ button is alternated automatically every time the program is run if the ‘hyst’ button is pressed. This allows easy viewing of the measured hysteresis curves. The absolute value of the data can be plotted, while keeping the x-axis the same, by pressing the ‘ABS’ button. The number

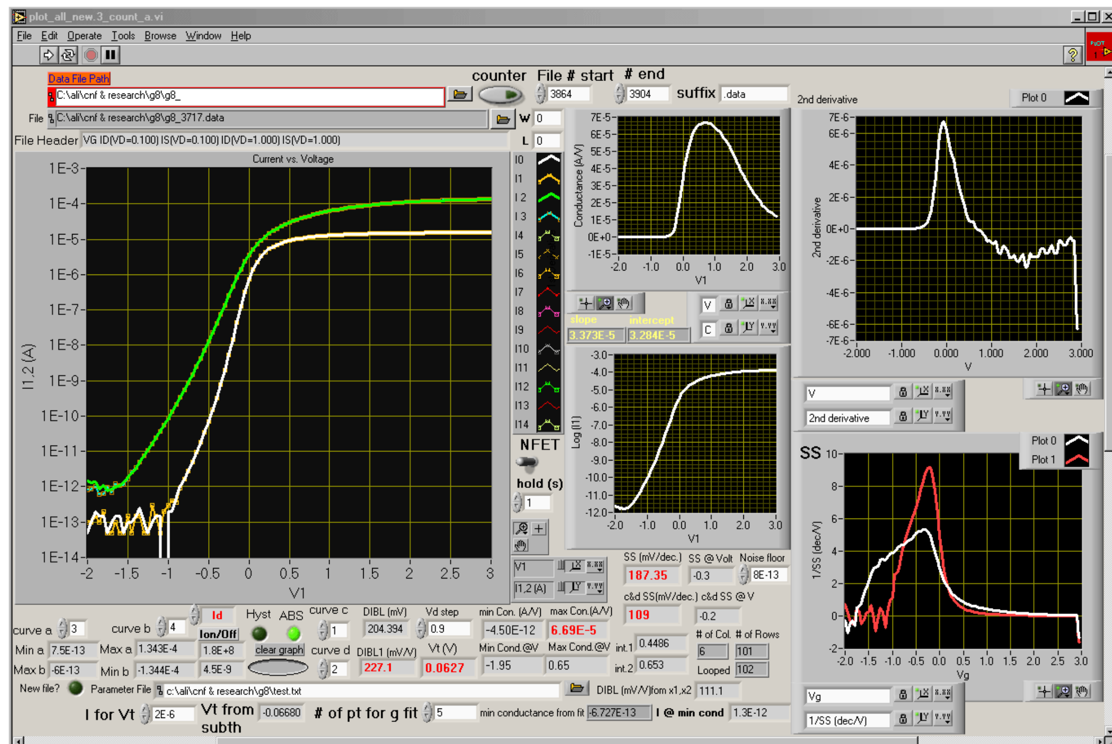


**Figure 7.2** Front panel of parameter analysis tool developed using Labview™ 7.0

of columns and the rows for data read from the file are displayed in the lower right corner.

#### 7.2.2.1 Data File Selection

The program can be either run independently or called from other programs, such as the program written to control the parameter analyzer. If the program is run independently the file name is needed be entered in the window labeled as ‘File’. Data file name is the only input parameter if the plotting program is called from another program. Multiple data files with consecutive file numbers can be plotted one after the other if the ‘counter’ is turned on. If the ‘counter’ is on, the program takes the file path entered in the ‘Data File Path’ field and appends a number, starting with the number indicated in ‘File # start’ window, and a suffix indicated in the ‘suffix’ window. The file number is incremented and the data is plotted until the data, with the file number as indicated in the ‘# end’ window. This file numbering scheme is compatible with all the controller programs I have developed. The consecutive data can be displayed one after another with a time delay. The time delay is set in seconds in the ‘hold (s)’ window. This aids the visualization of the evolution of the device characteristics if an additional parameter is varied, such as in the case of the transfer curves for two drain biases for different side-gate biases.

#### 7.2.2.2 Data Selection

Four curves can be selected for the calculation of the parameter extraction. These are labeled as ‘a & b’ and ‘c & d’. The program is setup assuming that the drain current and the source currents are measured for two different drain bias values. The small window under the large plot allows the choices of ‘Id’, ‘Is’ and ‘Id&Is’. If ‘Id’ is selected the parameters are calculated using the curves selected as ‘a’ & ‘c’, if ‘Is’ is selected the parameters are calculated using curves ‘b’ and ‘d’ and if ‘Id&Is’ is

selected, the parameters are calculated using the average of ‘a’ and ‘b’, and ‘c’ and ‘d’. Usually the first pair (a & b) is setup to be high $V_d$ (e.g. 1 V) and the second pair (c & d) is set up to be low $V_d$ (e.g. 0.1 V), and the curves will be referred to as such in the rest of the descriptions in order to avoid confusion.

#### 7.2.2.3 Calculated Parameters

A number of parameters relevant to FET characteristics are calculated, displayed and saved by the program. Device dimensions ‘W’ and ‘L’, ‘noise floor’, ‘Vd step’ and the curve selections ‘a,b,c,d’ are taken as input parameters. The device dimensions entered in the front panel are recorded in the parameter file but they are not used for calculation of any parameter.

#### 7.2.2.4 Extremum

Minimum and the maximum values and their ratios of the selected curves are displayed as ‘Min a’ and ‘Max a’ for high $V_d$ and as ‘Min b’ and Max b’ for low $V_d$. The ratio of the extrema in the current values are calculated and displayed as “Ion/Ioff”.

#### 7.2.2.5 Conductance

Minimum conductance and maximum conductance values (the first derivative of the plotted data) are calculated for high $V_d$ (a & b). The maximum conductance corresponds to maximum transconductance in the case of transfer characteristics and minimum conductance corresponds to output conductance in the case of output characteristics. The maximum and the minimum conductance values and the corresponding voltages are displayed in the front panel. These conductance values are calculated from the slope achieved from two consecutive data points.

In order to get an accurate value for the output conductance, in the case of output characteristics, a linear fit is used as a second method for calculating the minimum conductance. The points around the minimum conductance point as identified using the first method are fitted to a line. The number of points to be used for the linear fit is entered in '# of pt for g fit' window. The minimum conductance from the fit is displayed in the 'min conductance from fit' window. The corresponding current level is displayed in 'I @ min cond' window.

#### 7.2.2.6 Threshold Voltage

The threshold voltage is calculated using two different methods; one using a linear fit to the transfer characteristics in the on regime and the second using a constant current method in the subthreshold regime.

The first method for obtaining the threshold voltage ($V_t$) is carried out by

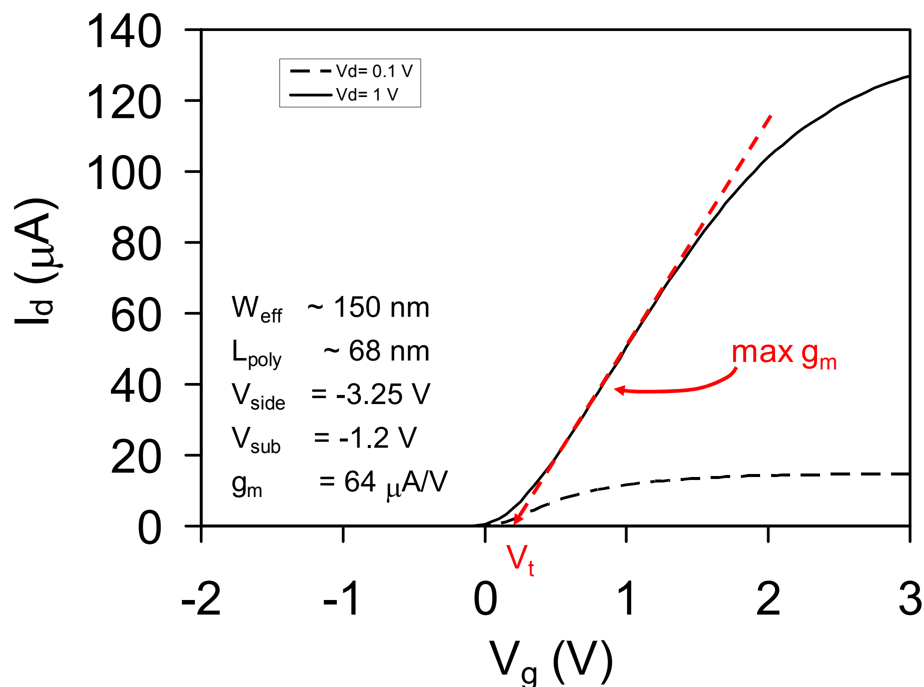


**Figure 7.3** The linear interpolation for the $V_t$ is taken from the maximum transconductance point and the $V_t$ is calculated as the x-axis intercept.

identifying the maximum transconductance bias condition and extrapolating a line from this point with the same slope as the maximum transconductance, intercepting the x-axis. The x-axis intercept is taken to be the threshold voltage (Figure 7.3).

The second method, constant current method, is carried out by identifying the gate voltage corresponding to a certain current level. This gate voltage is identified as threshold voltage and the desired current level is set in the small window at the bottom of the front panel labeled as ‘I for Vt’. The program finds the corresponding voltage value through linear interpolation of the $\log(I_{ds})$ between the two closest points to the specified current level and displays it in the window labeled as ‘Vt from subth’. This method is especially suitable for measuring the threshold voltage changes in a single device for different side-gate or back-gate values. The change in the threshold voltage value can be extracted even for the bias conditions where the device does not turn on. This method also avoids complications in the change in the extracted threshold voltage due to large contact resistances.

#### 7.2.2.7 Subthreshold Slope

Subthreshold slope (SS) is calculated from the a&b curves at the steepest location, using the slope calculated from two consecutive data points (Figure 7.4). SS for c&d is calculated and displayed separately. The noise in the measurement can result in significant fluctuations in the $10^{-13}$ A regime. When the slope of $\log(I_{ds})$ is calculated, the fluctuations in the measurement in the very low current levels can yield the maximum slope. In order to avoid this problem, a constant value can be added to the data. The added value is specified in the ‘noise floor’ window and should be adjusted depending on the noise level in the measurement. The log plot of the data with the added value for ‘noise floor’ is displayed in the bottom right plot. For most measurements it is sufficient to add $10^{-11}$ to $10^{-13}$ A to the measured data in order to

avoid this problem. This added value results in a slightly increased value of subthreshold slope measured in mV/dec. This increase is less than 1% if the added value is in the $10^{-11}$ A range for most measurements. The value for 'noise floor' should be set as low as possible to avoid miscalculation of the subthreshold slope. The calculated values for SS and the corresponding voltages are displayed. 1/SS for both curves is plotted in a window on the bottom right in units of decades per V.

#### 7.2.2.8 Drain Induced Barrier Lowering

Drain induced barrier lowering, DIBL, is defined as $\delta V_t/\delta V_d$ and it is extracted from the subthreshold characteristics in this program. DIBL is calculated from the bias condition corresponding to the minimum subthreshold slope, steepest point on the

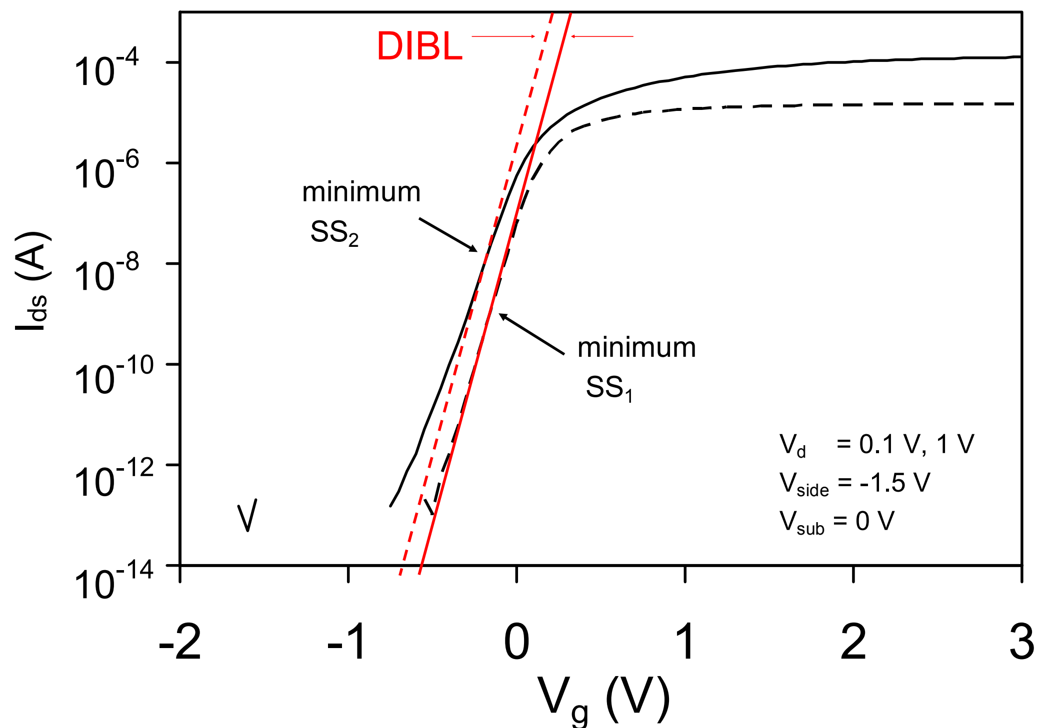


**Figure 7.4** DIBL is estimated from subthreshold characteristics of the $I_d$-$V_g$ curve. Minimum subthreshold slope is calculated for high $V_d$ and low $V_d$ cases. A line is passed at these points with the slope of the low $V_d$ case. The difference in the intercepts is taken to be the value for DIBL.

log($I_{ds}$) curves (Figure 7.4). The SS for high $V_d$ and low $V_d$ cases can differ significantly for small scale devices. Therefore, it is not possible to get an accurate value for DIBL by simply fitting lines to the curves at the minimum SS conditions and taking the difference of the intercepts. In order to avoid this problem the slope of the low $V_d$ curves are used for calculation of intercept for high $V_d$ curves as well. A line for high $V_d$ case is fitted by using the slope of the low $V_d$ curve and the point identified as the minimum SS point for the high $V_d$ case in order to calculate the intercept (Figure 7.4). The intercept for the low $V_d$ case is calculated by fitting a line to the curve at the minimum SS point and using the slope at that point. The difference between the two intercepts are calculated and displayed in mV in 'DIBL(mV)' window. DIBL as mV / V is calculated by diving this value by the difference in $V_d$ for the two curves, as entered in the '$V_d$ step' window.

#### 7.2.2.9 Parameter File

All of the calculated parameters and the input values are written into a tab delimited text file along with the data file name. The parameter file is chosen in the 'Parameter File' window at the bottom of the front panel. A header line would be inserted into the file if the 'New file ?' is turned on.

The header line for the recorded parameters is:

data file, W(um), L(um), min a, max a, max a/min a, min b, max b, max b/min b, Vt(V), SS(mV/dec), DIBL(mV/V), Max Cond (A/V), Min Cond(A/V), Max Cond@V, Min Cond@V, SS@ V, c&d SS(mV/dec.), c&d SS@V, DIBL(mV),Vd step, a, b, c, d, noise floor, slope, intercept, min. cond from fit, I@min cond, Vt (subth), I for Vt

#### 7.2.2.10 NFET / PFET Switch

This program is designed to extract the parameters for nFET devices. However, it is possible to extract the parameter for a pFET by switching the nFET/pFET switch to pFET. By doing so the parameters such as $V_t$, DIBL, SS are accurately calculated but the calculated voltages are negated. The user should be attentive to this difference for pFET characterization especially for the value for $V_t$.

#### 7.2.2.11 Slope & Intercept

The data for high $V_d$ is fitted to a line. The slope and the intercept of the fit is displayed under the conductance plot window. These values allow easy characterization of resistors, useful for contact resistance extraction. In the cases where the contacts are ohmic and there is no current saturation in the resistor, the current voltage characteristics are linear and pass through origin.

### 7.2.3 Software tool developed for C-V measurements through LCR meter

Majority of the capacitance measurements are done at 1 MHz for characterization of MOSFETs in this work. In order to make the capacitance measurements at this frequency range a HP 4275A LCR meter is used. The HP 4275A LCR meter has the capability of carrying out measurements at a number of frequencies between 10 kHz and 10 MHz and has an internal DC voltage source which can be used for bias sweep. The applied DC bias is monitored by a HP 3456A multimeter connected to the LCR meter from the back panel of the instrument and both of these instruments are controlled by a single program developed in Labview™ (Figure 7.5).

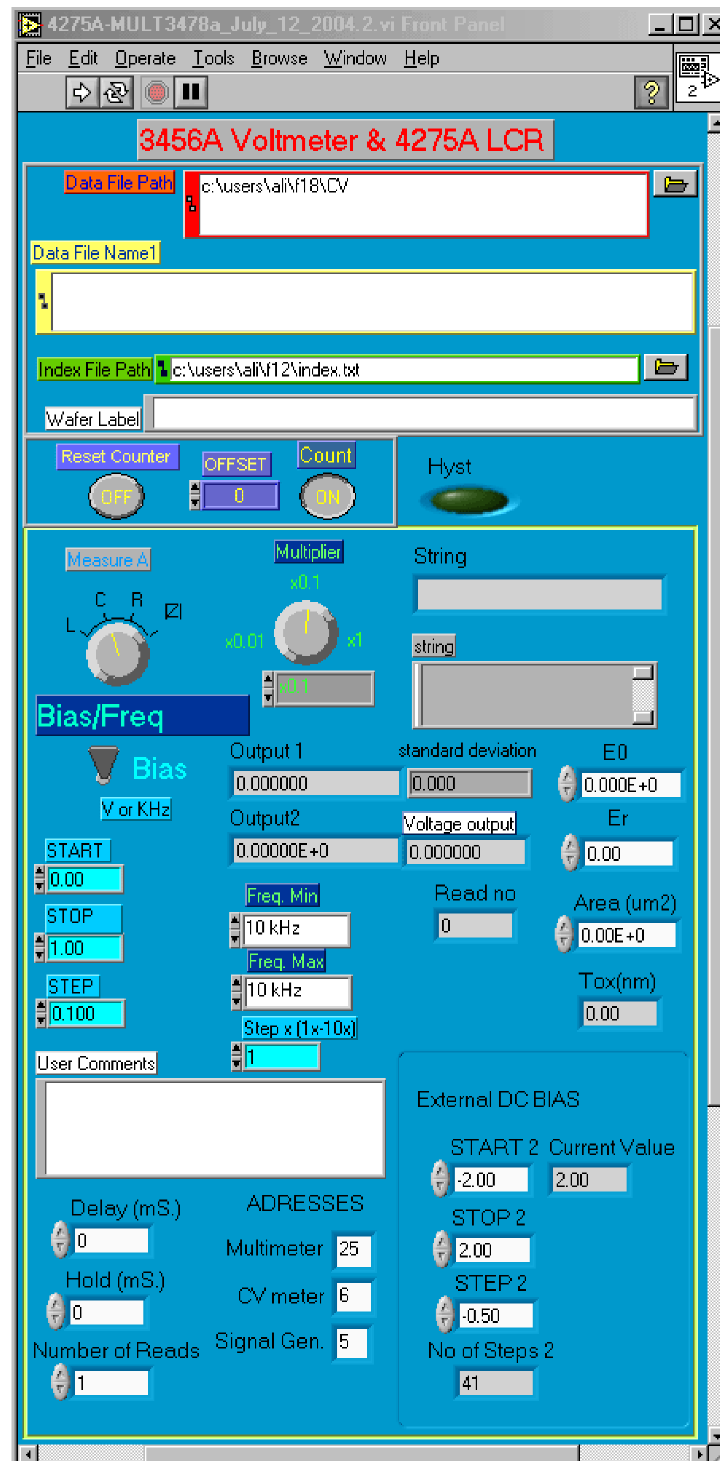


**Figure 7.5** Front panel of capacitance measurement program for HP 4275A LCR meter using a HP 3456A multimeter for external bias monitoring.

The interface for the data file name, numbering, user comments and wafer label are identical to the interface for the parameter analyzer HP 4145B control program (page 162). Similarly, this program also has the hysteresis option. After the completion of the first measurement a second measurement is started by swapping the start and stop values and negating the step value of the DC bias if the 'Hyst' button is turned on.

This program can perform a bias or frequency sweep, determined by the 'Bias/Freq' switch. However there are only a few discrete frequencies available. The program can step each available frequency or skip some determined by the 'step x' value.

If the sweep is set to be 'bias', the chosen frequencies are stepped. A 'delay time' and a 'hold time' can be set from the front panel in mS. The 'delay time' is the wait time after the first bias point is set until the first measurement is acquired. The 'hold time' is the wait time for the bias points after the first bias point between each bias change command and the first measurement acquired at that bias point. The program can acquire data multiple times at each bias point set by 'Number of Reads'. The average of the acquired data and the associated standard deviations are written into the data file, forming a six column data file. The name for this data file is constructed from the data file path, file number and a suffix which includes the frequency of the signal used for acquisition. All of the acquired (raw) data are recorded into an additional file with the same file name but with the file extension of 'data_detail'.

The amplitude of the AC signal can only be set from the front panel of the LCR meter. The multiplication factor is set from the front panel of the program (program resets the multiplication factor at the beginning of each run). Two quantities

can be measured simultaneously, first of which can be controlled from the program but the second quantity is needed to be set from the front panel of the instrument.

For C-V measurements, the first quantity is set as C (capacitance) and the second parameter as G (conductance) by default. HP 4275A is capable of reading 0.1 fF resolution data for C if the signal amplitude is less than 100 mV. It can read 10 aF resolution data for C if the signal amplitude is equal to or larger than 100 mV. The fluctuation level in the measured value decreases with the increased AC signal. The fluctuation level is in the order of 0.5 fF for 45 mV signal. Very high resolution C-V information can be achieved through averaging as described in chapter 5.

A gate dielectric thickness is calculated in real time if the permittivity of space, the dielectric constant and the area of a parallel plate capacitor is entered in the front panel. The dielectric thickness is displayed in the 'Tox(nm)' window in nm.

This program is also setup to use an HP Signal Generator as an additional external power supply. The start, stop and step values can be entered from the front panel. The program has an out-most loop setting up the signal generator bias before running the measurements. The hysteresis loop is within this loop.

The signal generator used for this purpose has an output resistance of 50 Ω. The user should be attentive to this while biasing the devices and consider proper termination of the signal generator output. If a gate is biased, where the input impedance to the device is very large, the applied bias to the gate will be as high as twice the desired value. An external multimeter can be used to monitor the actual bias applied by the signal generator.

The GPIB addresses of the Multimeter, LCR meter and the signal generator can be set from the front panel of the program. The program will still run if no signal generator is connected to the GPIB network or if wrong address is entered. This configuration is used to make a large number of repeated measurements without using

the signal generator as an external power supply. In this case the parameter analyzer, HP 4145B can be manually run in repeat mode in time-domain, in order to supply the desired additional external bias.

### 7.2.4 Plotting

The C-V data file generated by the data acquisition program contains six columns. The fist column through third column are the applied potential, measured capacitance and measured conductance. The errors associated with these measured quantities are recorded as columns four through six. The capacitance and conductance curves are plotted in two different programs, one using the second column and the other using the third column as vertical axis data. The plotting programs can be called from the C-V measurement or analysis program or operated independently. If the plotting program is operated independently, the file name is needed to be entered in the indicated field (Figure 7.6). The most recent data will be plotted on both the right

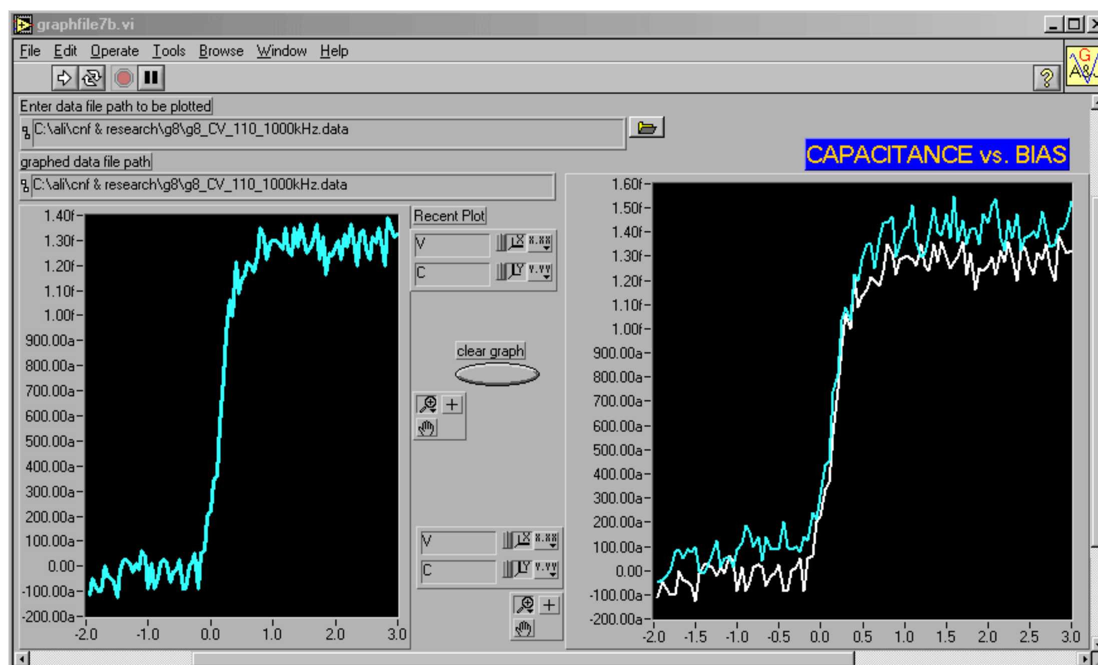


**Figure 7.6** Front panel of capacitance plotting program. The most recent plot is displayed on the left. The window on the right accumulates all the plotted data.

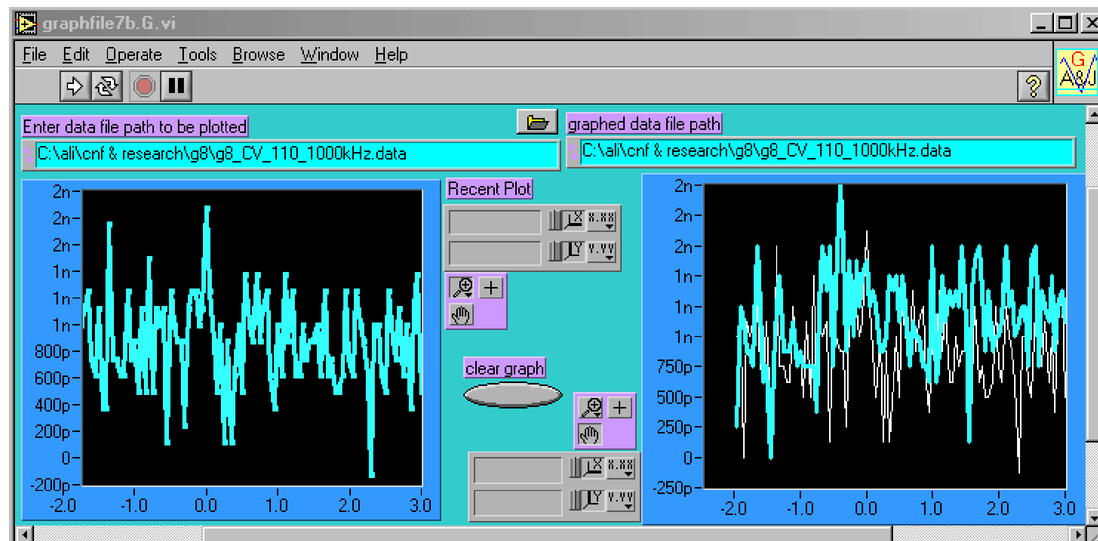


**Figure 7.7** Front panel of conductance plotting program. The most recent plot is displayed on the left. The window on the right accumulates all the plotted data.

and the left windows. The right window will accumulate all the plotted data unless 'clear graph' button is pressed. In this case the previous data will be deleted and only the most recent data will appear in both of the windows.

The conductance data is plotted in the exactly the same fashion as the capacitance data using a program identified as 'graphfile_G' (Figure 7.7).

### 7.2.5 C-V Analysis

aF resolution C-V information can be achieved through averaging a large number of repeated measurements (Chapter 5). In order to handle a large number of C-V data files two programs are developed for the data analysis. The first one, named as 'CV Review', is an averaging program allowing the user to plot a large number of data files numbered in a sequence, select the desired data files and average them. The second program "CV hyst average" allows the user to select the averaged C-V data for forward and reverse sweeps, average the two and extract a number of parameters, and generate data files where the offset capacitance is subtracted.

#### 7.2.5.1 CV Review

This program has the same data file name interface as the data acquisition programs (Figure 7.8). The file name is constructed from the data file path, file number and the suffix entered in the front panel. The data file number is set to start at the value entered in the 'File # start' field and is incremented by one, ending with the file number indicated in the '# end' field. If 'Plot all?' button is turned on, all the data files in the range are plotted one after the other. If the 'Review all' button is turned on, then a small window appears after plotting each data file asking the user if the last

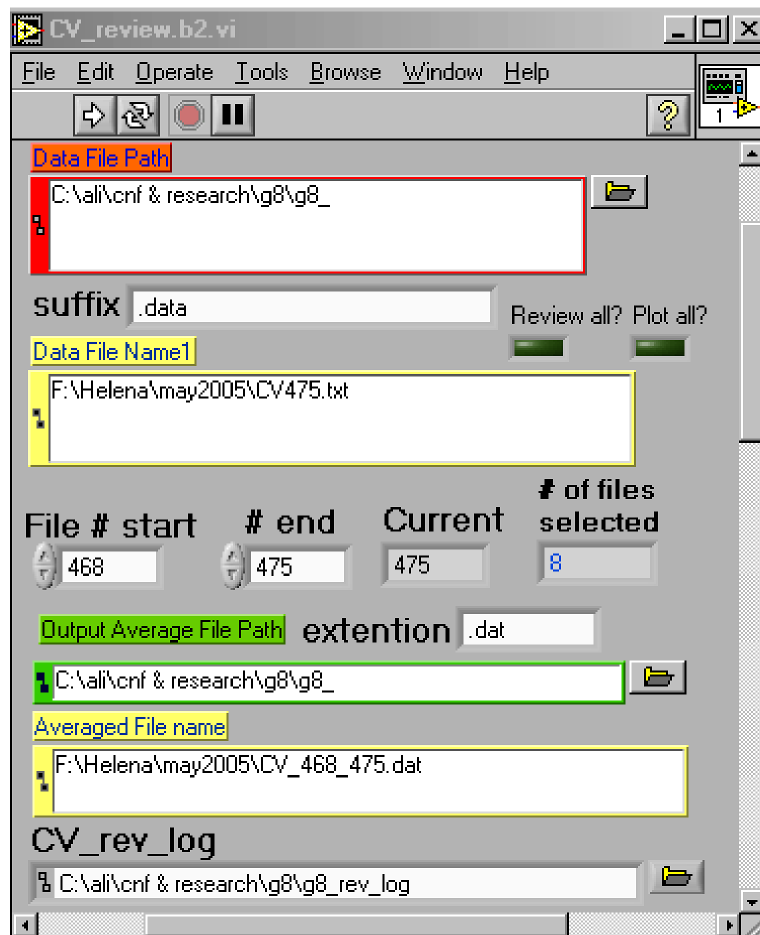


**Figure 7.8** Front panel of CV review program. Program allows plotting of individual data files for selection and averages the selected files with in a sequence.

plotted data should be included in the average or not (Figure 7.9). If the ‘Review all’ button is not turned on, all the data in the range are averaged.

The averaged data is saved into a data file where the data file name is constructed as ‘output average file path’ + ‘start#’ + ‘_’ + ‘end#’ + ‘extension’. The file names and the number of the files used for the averaging is recorded in a log file as indicated in the ‘CV_rev_log’ field.

### 7.2.5.2 Data file selection criteria

The reason for review of all the C-V data files is to identify the data sweeps

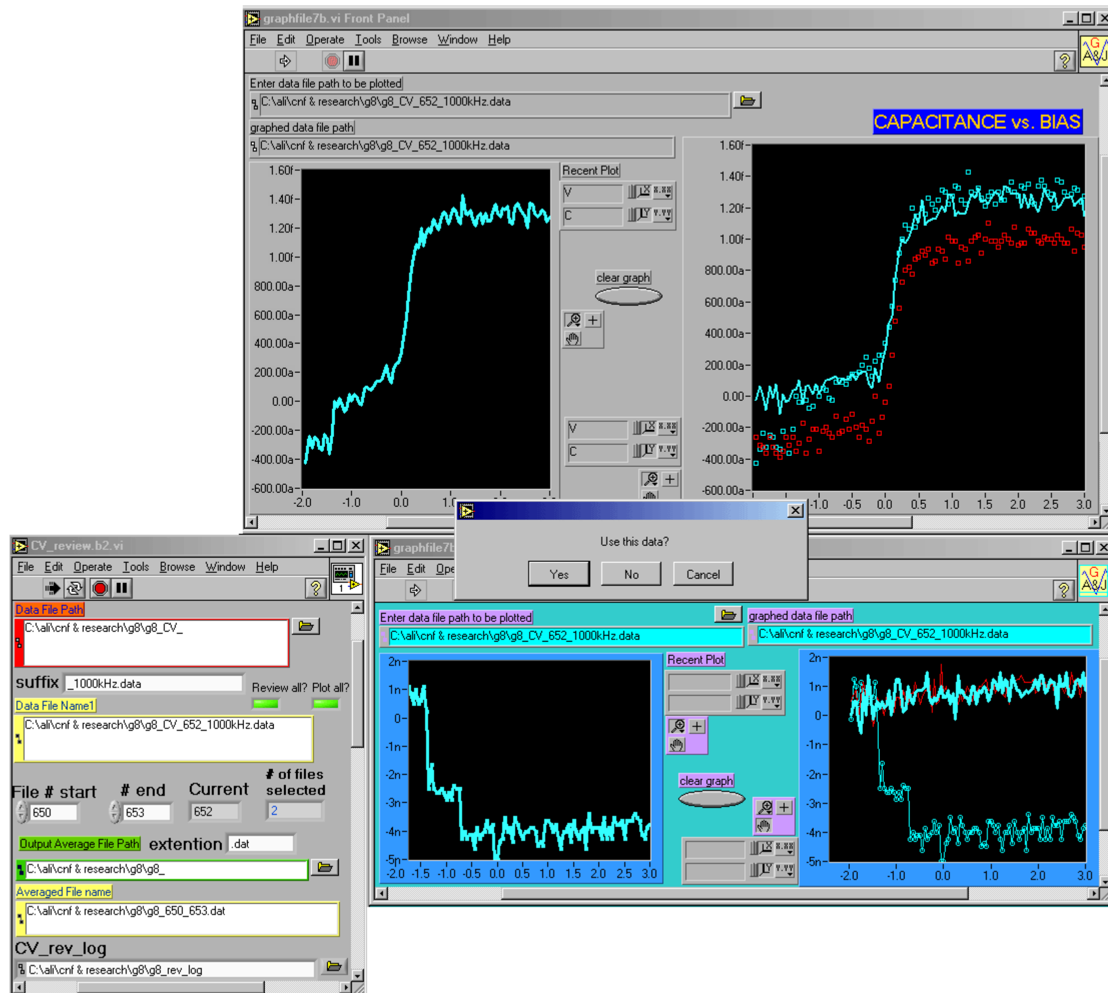


**Figure 7.9** Data file selection process. A small window appears after plotting the C-V and G-V data asking if the displayed data should be included in the averaged file.

during which the setup has undergone some sudden changes resulting in changes in the offset values. The acquired data has arbitrary offset value, since we can only measure the change in capacitance rather than absolute capacitance in this range. The changes in the offset values which occur between two runs are not disruptive since all the data in each sweep has the same constant offset values. However, changes in offset values during a sweep make the data from that particular sweep unusable. These sudden changes are likely to be due to slight changes in the probe locations or the cable orientations. If the cable connections are not changed for a long time, these changes are observed to be a lot less frequent than otherwise. The changes in the LRC meter resulting in changes in offset values due to internal and environmental factors are relatively slow and can only be isolated by averaging of large number of data sets.

The sudden changes in the setup show up as discontinuities in the conductance or capacitance data. These data files should be excluded from the average by clicking 'no' in the window which appears after the plotting of the data. If 'cancel' button is clicked, the program is stopped. The number of selected files is displayed in the front panel of the 'CV review' program.

#### 7.2.5.3 CV hysteresis average

This program is setup to take the averaged data files generated by the 'CV review' program as input, average the forward and the reverse sweeps together, and carry out an offset subtraction from the capacitance data (Figure 7.10). The data file name is constructed by appending the chosen file extension to the 'Averaged File name'. The program expects to have a reverse sweep data with the same file name but identified with an additional string before the file extension, 'h' by default, forming a name as 'Averaged File name' + 'hyst identifier' + 'extension'.

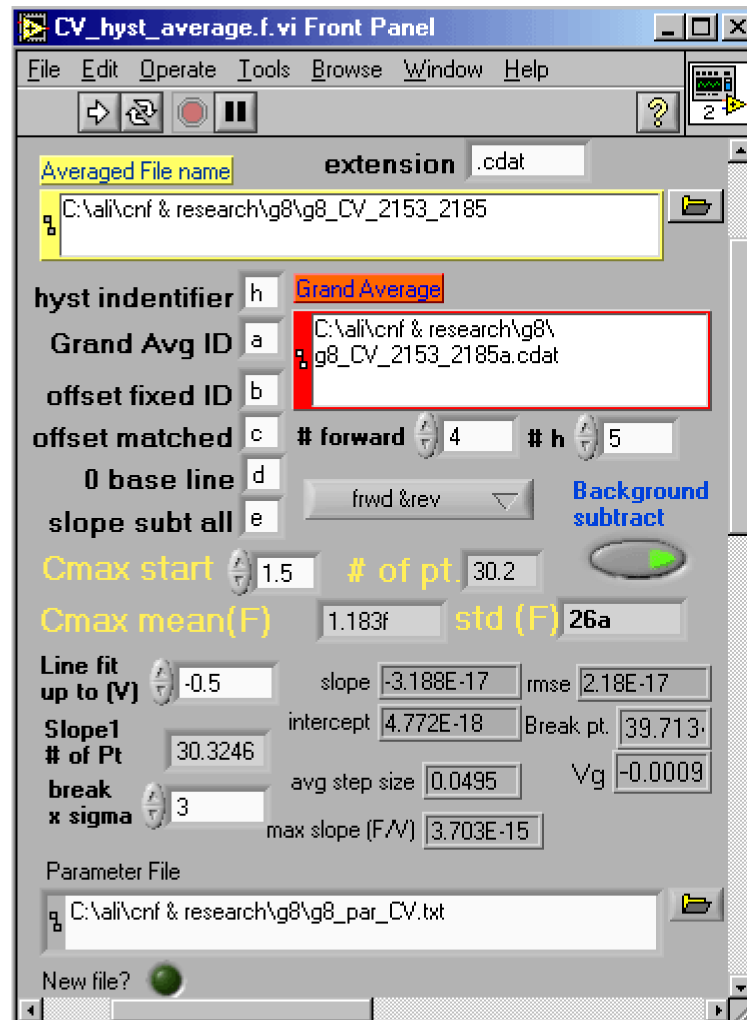


**Figure 7.10** Front panel of CV_hyst_average program. Program takes the averaged forward and reverse sweep data, calculate a number of parameters and generate off-set removed data files

The capacitance data from the measurement has an arbitrary offset value since it is not possible to calibrate the system in order to extract the actual capacitance of the transistor for very small scale devices, with less than 1 fF inversion layer capacitance. However, since the source/drain to gate capacitance of an FET structure is a nonlinear function of the gate bias, it is possible to calculate the absolute inversion layer capacitance with a good accuracy. This is through identification of onset of inversion from the data.

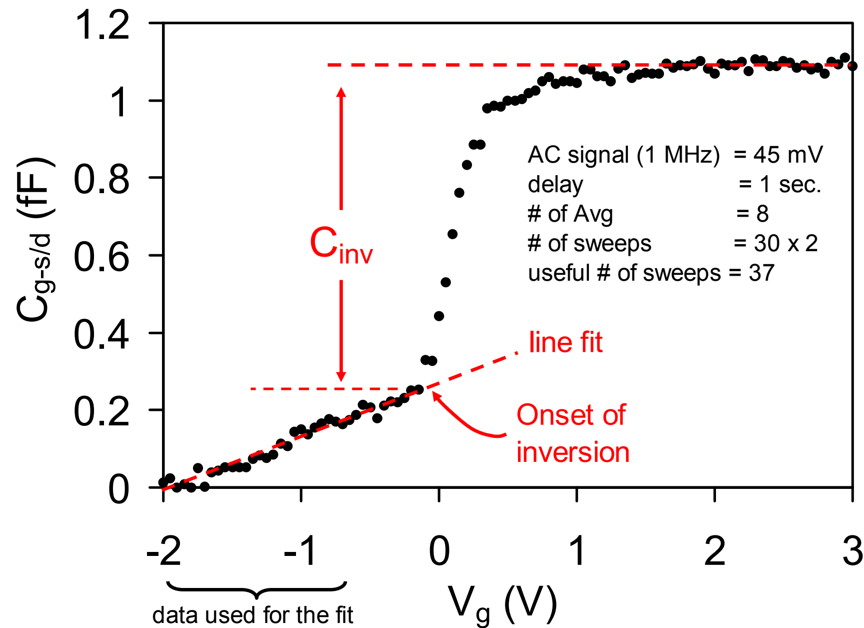


**Figure 7.11** A typical averaged C-V data for a device with $L_{eff} < 0.2$ µm. The onset of inversion is determined from the point where the data deviates 3 σ from the line fitted to data points for $V_g < -0.5$ V

This program is setup to identify the onset of inversion in the C-V data by fitting a line to the data in the bias regime where the channel is not inverted ($-2$ V $< V_g < -0.5$ V range in Figure 7.11). The change in the capacitance value in this regime is primarily due to source drain grading. As the inversion layer starts forming, the gate to source/drain capacitance starts increasing at a much higher rate compared to the capacitance change due to the source/drain dopant grading. This line is fit to the first data points in the data file, up to the bias point identified in the 'Line fit up to (V)' field. The fit parameters and the standard deviation, σ (sigma), in the fit are calculated and displayed in the front panel as 'slope', 'intercept', 'rmse' (root mean square error). The deviation from the fitted line is calculated for all the data. The break point, identified as the onset of inversion is set to be 3σ by default, and it can be changed as desired by the user by changing the number in the 'break x sigma' field. 3σ point was found to be sufficient to avoid any errors due to the noise in the measurement and

accurately identify the breakpoint in the C-V characteristics. The index of the break point and the corresponding gate bias are also displayed on the front panel.

The program calculates and displays the average step size in the gate bias increments and the maximum slope in the C-V data in F / V.

The inversion layer capacitance is calculated to be the difference between the identified breakpoint and the value for the saturation capacitance. The saturation capacitance is calculated to be the average of the values beyond a certain bias point set in the ‘Cmax start’ field. The average value is displayed as ‘Cmax mean(F)’ and the standard deviation in the average value is displayed in the ‘std (F)’ field. The user should be attentive to these values if there is a significant change in saturation capacitance due to gate depletion.

The program allows the user to enter the number of traces used to make the forward and the reverse averages and allows the user to choose to use forward, reverse or the average of the forward and reverse sweeps. The program generates five different data files with slight variations. These files are identified by a letter appended to the file name before the file name extension. The file identified as “Grand Avg”, ‘a’ by default, is the average of the forward and the reverse sweeps. The file identified as “offset fixed”, ‘b’ by default, has the slope prior to onset of inversion (break point) subtracted from the data, up to the onset of inversion and the constant value of the capacitance at the break point is subtracted from the rest of the data. “Offset matched”, ‘c’ by default, has the constant value of the capacitance at the break point subtracted from all the data, bringing the onset of inversion (breakpoint) to zero. “0 base line”, ‘d’ by default, has all the points prior to the break point set to zero and the value at the break point subtracted from all the data points. “slope subt all”, ‘e’ by default, has the initial slope subtracted from all of the data points. Among these data files, ‘b’ and ‘d’

reflects the inversion layer capacitance and they should be used for extraction of effective carrier mobilities.

The program also has the option of subtracting a background capacitance change from the data prior to calculating any of the parameters. If “subtract background” is turned on, the program subtracts a curve from the data, defined by a cubical function. This utility is useful for very small inversion layer capacitance values, in the order of 100 aF, or smaller, where the changes in the coupling capacitance between the contacts pads are comparable to the inversion layer capacitance. This variation in parasitic capacitance is in the order of 30-50 aF for most side-gated devices reported in this thesis. The function for the background capacitance can be obtained by fitting a cubical to the C-V characteristics measured on gateless devices, where the change in the capacitance are purely due to the parasitics, mainly the coupling capacitance between the contact pads through the field isolation and low doped semiconductor substrate. The users should be attentive to the device to device variations in the parasitic capacitances due to slight variations in leakage currents. These changes are in the order of 30 aF for the side-gated devices with large contact areas. The function for the background capacitance change can only be changed in the block diagram by changing the expression field.

## 7.3 C-V extraction through RF measurements

It is possible to extract capacitance of a device through transmission and reflection measurements performed on the device using a network analyzer. Using these parameters it is possible to calculate the impedance of the device as a function of frequency. Performing a linear fit to the data it is possible to extract the capacitance of the device. The details of this technique can be found in [62][63]. This technique is

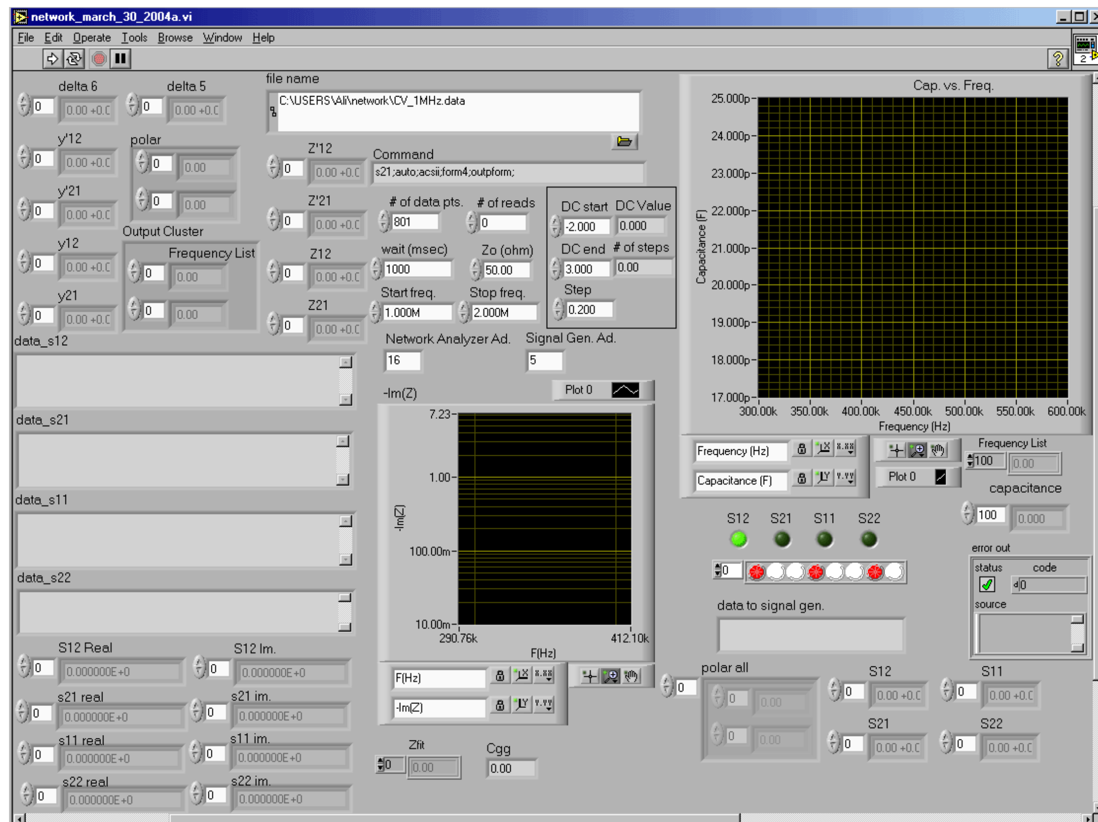


**Figure 7.12** Front panel of C-V extraction using S-parameters. The program uses a network analyzer and a DC power supply to calculate C from frequency response. The calculated C for different bias points are then plotted using a simple version of "plot_all" program

reported to be suitable for leaky dielectrics and can be used to extract the capacitance characteristics of the devices in GHz regime.

The C-V extraction algorithm form S-parameter measurements are implemented in a program named as "network_march_30_2004". This program calculates C for each bias point and records in a data file. The program calls "plot_all" in order to plot the generated C-V data file.

The data obtained using a low-frequency setup were as expected from large scale devices, where the capacitance values are in the order of pF. However, the signal to noise ratio in the setup was not good enough to achieve the desired aF resolution in the setup used for the measurements. This technique may also result in sub fF

resolution capacitance characterization if a high frequency setup is used or the devices are individually packaged for high frequency measurements [69].

## 7.4 Effective device dimension extraction from electrical measurements

Knowledge of effective device dimensions is important for understanding the performance parameters. Physical gate length and channel width can be measured using an SEM or AFM prior to deposition of passivation layer on the devices. The data obtained from SEM can give a good understanding of the physical gate length. However, it is difficult to estimate the effective device width for narrow channel devices with non-planar topography due to the corner effects.

The physical device dimensions cannot be measured using SEM or AFM once the device processing is completed in a nondestructive fashion. Hence it is important to be able to extract the effective device dimensions from electrical measurements

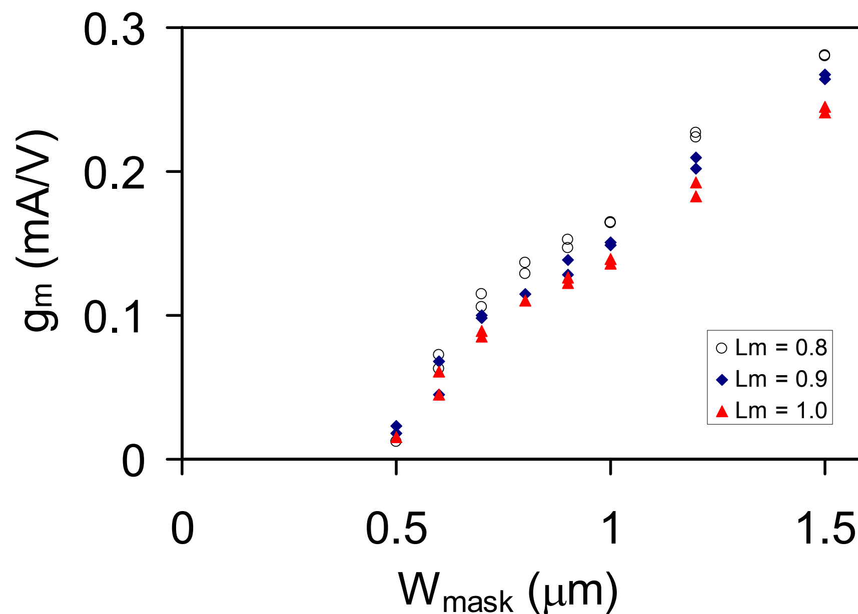


**Figure 7.13** Maximum transconductance as a function of designed device width for three different design gate lengths in μm.

which can be performed on the devices.

It is possible to extract the effective device dimensions from electrical measurements if there is an array of devices with different mask dimensions. However uncertainty in the mask dimensions and non-linear variation in printed dimension of small-scale devices, dimension dependent processing variations result in significant difficulties in device dimension extraction using linear fits (Figure 7.13).

If these dimension dependent process variations are small, the difference between the design and fabricated dimension of the devices are expected to be a constant amount for all devices due to constant amount of resist trimming and oxidation on all devices. The effective device width can be extracted from electrical measurements performed on devices with the same gate length and varying widths. Similarly, effective device length can be extracted from electrical measurements performed on devices with same width and varying gate length. Although it is possible to extract the effective width from both C-V and I-V measurements, gate length extraction in the very small scale devices can be done more accurately from C-V measurements. The inaccuracy for the device dimension extraction from I-V characteristics in the small scale devices arise from short channel effects, dimension dependent contact resistances and device to device contact resistance variations. The most accurate way of extracting the device dimensions from I-V characteristics is by plotting the maximum transconductance of the devices as a function of design dimension. The transconductance of the devices are less affected from the variations in the contact resistance and $V_t$ of the devices compared to the drive currents, especially for higher drain biases where the device is in saturation. In this case the x-axis intercept of a line fitted to the data would result in the offset value which indicates the difference between the design dimensions and the physical dimensions of the devices.

Both the measured conductance of the gateless devices and the transconductance of the fabricated FET structures (Figure 7.13) show a non-linear behavior as a function of design width. This variation can be due to process variations, mainly due to dishing in the CMP process.

Since the sidewalls of the active layer etched into silicon does not have perfectly vertical sidewalls. If the top surface is etched down slightly more, the effective device width increases. Although the variations and the reasons for the variations are hard to understand, we can try to go around the problem by using the capacitance measurements done on long channel devices ($L_{eff}$ ~1.2 μm).

Inversion layer capacitance data on the long devices show a similar non-linear behavior as a function of design width as the transconductance data on the measured FETs to some extend. However it is much easier to extract the effective width of devices from a $C_{inv}$ versus $W_{mask}$ data.

## 7.5 Contact resistance extraction from electrical measurements

Effective carrier mobility is an important parameter for small scale FETs and there is a growing interest in investigating carrier mobility in nano-structures. One of

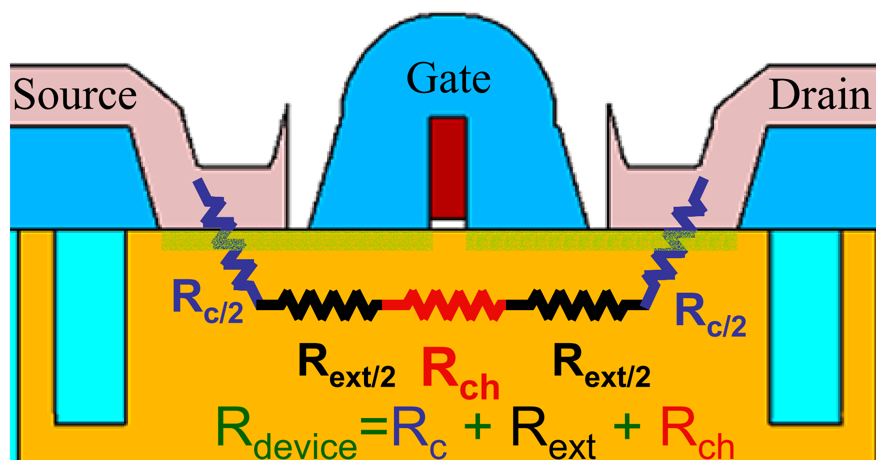


**Figure 7.14** Cross section schematics of an FET, indicating the resistances between the source and the drain contacts: metal-semiconductor contact resistance, extension resistance, and channel resistance for a given bias condition.

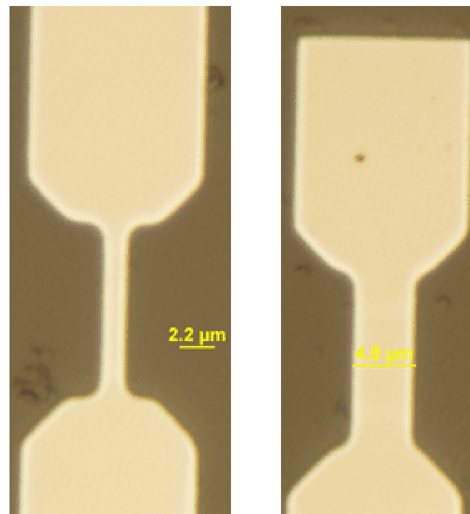


**Figure 7.15** Optical images of active area patterns on the mask for a narrow channel (left) and a wide channel (right) device. The narrow areas are the extension regions for short channel devices.

the important parameters necessary for effective carrier mobility extraction is the contact resistance of the devices. The total contact resistance from the metal contacts to the intrinsic FET consists of the resistance at the metal-semiconductor contacts and the leads extending to the devices (Figure 7.14 - Figure 7.16). If the variations in the device width due to processing are relatively small, it is possible to extract the contact resistance of the devices by plotting $1/W_{eff}$ as a function of the measured resistance of gateless devices. The gateless devices are fabricated in the same way as the regular FETs but since they do not have gates, all the active surfaces are implanted with As ions. The intercept of the $1/W_{eff}$ versus resistance plot gives the resistance value common to all of the devices (Figure 7.17). This resistance value is the sum of metal-semiconductor contact resistance and the resistance of the large source/drain connecting to the lead areas of the devices. The lead resistance varies as a function of $1/W_{eff}$ and the total resistive extend leading to the device, $L_{tot}$-$L_{eff}$.

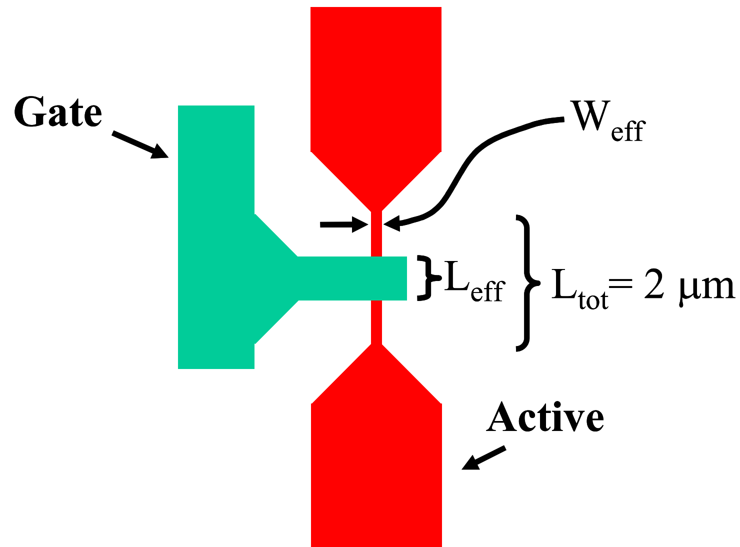


**Figure 7.16** Schematic view of the device layout. The only two varying parameters for different size devices are the effective gate length ($L_{eff}$) and effective channel width ($W_{eff}$).

The inversion capacitance for the MOSFETs are directly proportional to $W_{eff}$. The total resistance of the gateless devices, $R_{gateless}$, have $1/W_{eff}$ dependence. $R_{contact}$ value can be extracted from the intercept of $1/C_{inv}$ of $L_{eff}$ = 1.2 μm versus $R_{gateless}$ for

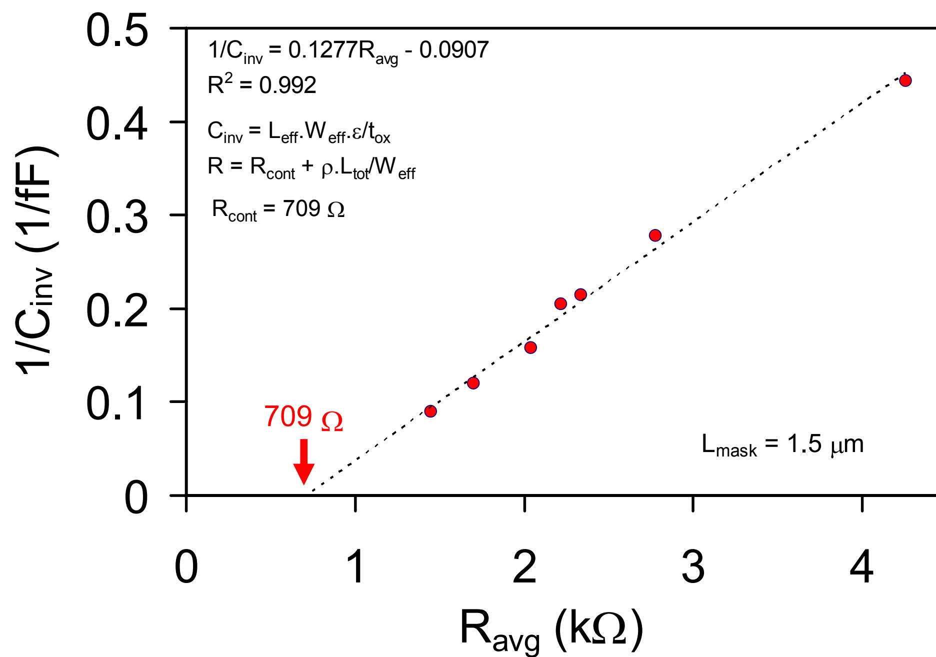


**Figure 7.17** Inverse of inversion layer capacitance for design gate length of 1.5 μm versus average resistance of the gateless devices for different design widths

the same design widths. Here $R_{contact}$ is the sum of the lead resistance common to all devices and metal-semiconductor contact resistances.

$$R_{gateless} = R_{contact} + \frac{\rho L_{tot}}{W_{eff}}$$

$$C_{inv} = \frac{L_{eff} W_{eff} \varepsilon}{t_{ox}}$$

The total contact resistance of all of the devices can be calculated using the $R_{contact}$ value and the resistivity of the source drain extensions, ρ, which can be extracted from the slope of the linear fit. The slope of the plot in Figure 7.17 is:

$$Slope = m_1 = \frac{t_{ox}}{\varepsilon_{SiO_2} L_{eff} \rho L_{tot}}$$

The effective oxide thickness can be extracted from C-V measurements performed on large, 100 μm x 100 μm devices. The oxide thickness, $t_{ox}$ = 4.0 nm for the devices reported in chapter 4. $L_{tot}$ = 2 μm by design, and effective gate length is estimated to be $L_{eff}$ = 1.167 μm for the devices used for capacitance information as extracted from the series of capacitance measurements. Using these known parameters and the slope from the fit, the resistivity, ρ of the source drain extension regions are calculated.

$$\rho = \frac{t_{ox}}{m_1 \varepsilon_{SiO_2} L_{eff} L_{tot}}$$

## 7.6 Carrier Mobility Extraction

In order to extract the carrier mobility in the channel of the transistor, the effective device dimensions, carrier concentration and the current drive and the actual potential drop across the device is needed.

The effective device dimensions can be estimated from SEM micrographs or the I-V and C-V measurements performed on the array of devices with varying

dimensions. The carrier concentration in the channel can be calculated from the inversion layer capacitance. The current level for a given bias condition is measured and the actual potential drop across the device can be calculated if the contact resistance values are known.

The channel resistance for a given device is:

$$R_{ch} = \rho \frac{L_{eff}}{W_{eff}} = \frac{1}{qn\mu_{eff}} \frac{L_{eff}}{W_{eff}}$$

$$qn = \frac{Q_{ch}}{L_{eff}W_{eff}} = \frac{\int C_{inv}(V_g)dV_g}{L_{eff}W_{eff}}$$

$$R_{ch} = \frac{L_{eff}W_{eff}}{\mu_{eff}\int C_{inv}(V_g)dV_g} \frac{L_{eff}}{W_{eff}}$$

If the capacitance measurements are performed on the same device, the $W_{eff}$ terms cancel out:

$$R_{ch} = \frac{L_{eff}^{\ 2}}{\mu_{eff}\int C_{inv}(V_g)dV_g}$$

$$R_{dev}(V_g) = \frac{V_d}{I_d(V_g)}$$

$$= R_{contact} + R_{ext} + R_{ch}$$

The effective carrier mobility can be extracted by plugging in the values for $R_{contact}$ and $R_{ext}$:

$$R_{ch} = \frac{V_d}{I_d(V_g)} - R_{contact} - R_{ext}$$

$$\mu_{eff} = \frac{L_{eff}^{\ 2}}{(\frac{V_d}{I_d(V_g)} - R_{contact} - R_{ext})\int C_{inv}(V_g)dV_g}$$

$$R_{ext} = WL_{ext}\rho_{ext}$$

$$L_{ext} = L_{tot} - L_{eff}$$

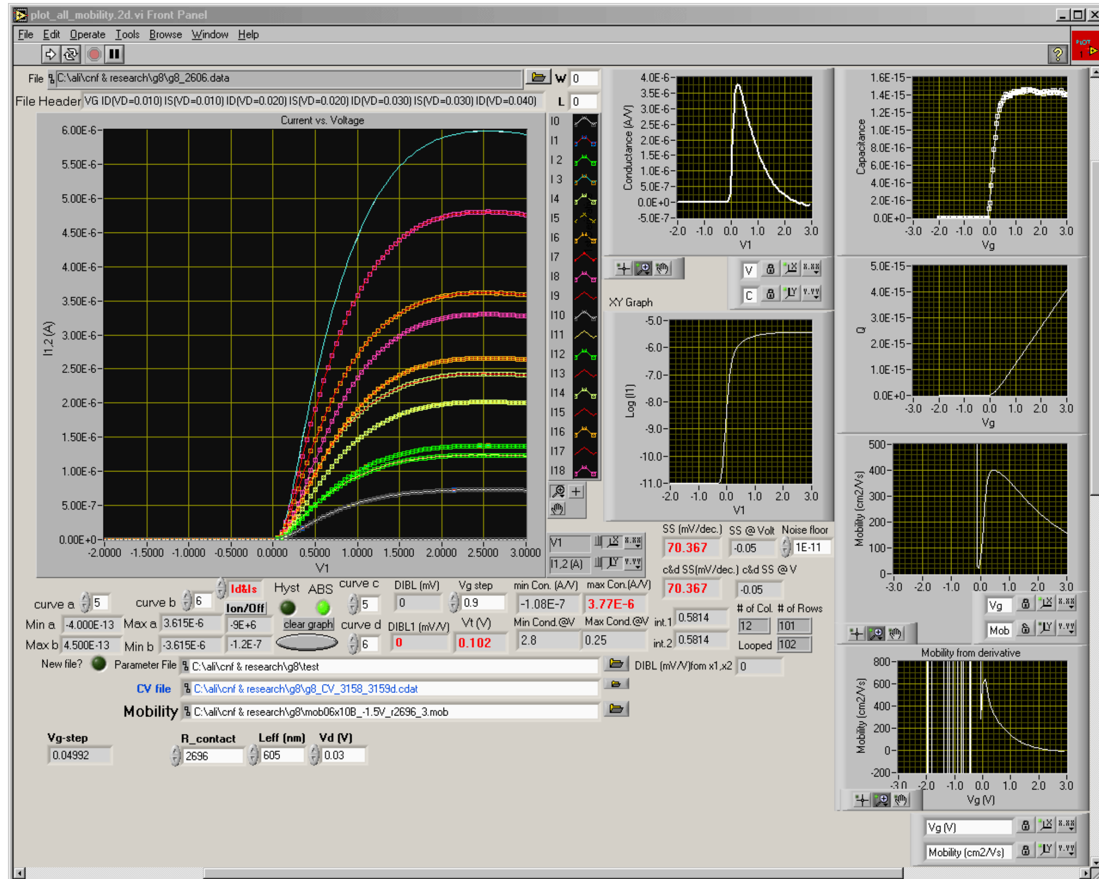


**Figure 7.18** Front panel of parameter analysis tool with mobility extraction, developed using Labview$^{TM}$ 7.0

### 7.6.1 Software Tool for Carrier Mobility Extraction

The parameter analysis tool "Plot_all" is modified to calculate carrier mobilities in nFETs. This version of the program takes additional inputs of C-V data file, contact resistance, gate length and drain bias values. For the selected curves. It calculates the mobility from the Ohm's law as derived in previous section and from the theoretical transconductance expression for long channel devices [61]:

$$\mu_{eff} = \frac{L_{eff}^{\;\;2}}{C_{inv} V_d} \frac{dI_d}{dV_g}$$

The values calculated using both methods are written to a file selected in the "Mobility" field. The mobility versus gate bias data for the two methods are plotted in separate windows on the lower right corner.

The capacitance file used for the measurement is required to have the offset value subtracted properly in order not to over estimate the number of carriers in the inversion layer. The C-V data and the total charge calculated by integrating the C-V data are plotted on the top right corner in separate windows.

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