ELECTRON TRANSPORT IN MOLECULAR TRANSISTORS

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ELECTRON TRANSPORT IN MOLECULAR TRANSISTORS

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In this thesis I will describe the conductance properties of certain organic molecules.

I will first show that two metal electrodes can be fabricated with a nm-scale gap between them by causing electomigration-induced failure in a nanoscale wire. These two electrodes are separated by a few nanometers from a metallic gate electrode. Organic molecules can be incorporated into the gap between the electrodes creating a transistor geometry.

Transport measurements on metal-organic complexes at low temperatures show Coulomb blockade and Kondo-assisted tunneling. Using the specially designed molecule C_{140}, I have studied the coupling between the vibrational modes of the molecule and electron flow through transistors made from it.

I have also been able to make magnetic electrodes to pass spin-polarized current through molecules. Using this, I have studied the coexistence of the Kondo effect and ferromagnetism in the electrodes.

I have also modified the technique to have a mechanically adjustable distance between the two electrodes, which is useful for studying the influence of the contact on the conductance of a device.

BIOGRAPHICAL SKETCH

Abhay Narayan Pasupathy was born in Bombay, India in 1976. In a couple of years, his parents moved to the (then) small city of Bangalore. Abhay attended the FAPS school down the road from his home for thirteen years, at the end of which he, his school, and the city had all grown to unexpected proportions. During his final school years, Abhay decided he wanted to study chemistry at college. Faced with the mysteries of organic chemistry however, he jumped ship and joined the physics program of the Indian Institute of Technology at Kanpur in 1993. After five years with the worst class attendance record in history, Abhay somehow graduated with a Masters degree and decided to do some damage to Dan Ralph's equipment at Cornell. Six more years down the line brings us to this thesis. Abhay now likes organic chemistry but still does not understand it.

To my parents,

my brother,

and my late *athai* Rathna.

ACKNOWLEDGEMENTS

Six years have slipped by since I came to Ithaca. Thanks to all the wonderful friends I have made here, my stay here has felt like a long holiday.

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Finally, thanks to my parents and Shankar for all they have done for me over the years.

TABLE OF CONTENTS

LIST OF FIGURES

Chapter 1

Introduction

1.1 Perspective

If you open up a product catalog of Alfa Aesar [1], a typical chemical company, you will notice that of the 22000 compounds sold by the company, 12000 are organic compounds. Carbon's chemical structure is of course responsible for the amazing variety of organic compounds that exist. Apart from being "organic", carbon compounds are used in every sphere of human activity.

Yet, a majority of electronics used today is based on silicon. Silicon possesses one great advantage over carbon - you can make large single crystals of semiconducting material from it (the "organic" analog, diamond, is an insulator). This is well suited to the methods of electronics manufacturing developed over the last few decades, where the game is to shape semiconducting material into useful electronic devices. These methods are not necessarily the best or only ones by which electronic devices can be made. For example, the human body is all-organic, but has several electronic components that work rather well. Silicon's dominance comes from our ability to understand its material properties and to work it into useful devices.

Advances in lithographic techniques and our understanding of solid-state systems have brought us to a point where we are interested in the electronic transport properties of organic molecules that are a few nanometers in size. One reason for this study is that simply the fact that such studies have not been performed before. Another reason is that we could conceivably make several socially useful organic electronic devices.

1.1.1 Understanding the nature of electron transport through molecules

A good reason to flow current through molecules is because we want to know what the basic physical mechanisms are that contribute to electron transport. Molecules have some attributes that make them interesting for such studies:

1. They are small (typically 0.5 - 10 nm in size). This means that very often, they behave like zero [2] or one [3] dimensional confining potentials for electrons flowing through them, a property they share with other mesoscopic systems such as metallic [4] and semiconducting quantum dots [5]. Electron flow through such small objects can also be ballistic, giving them very different conductance properties from bulk materials.
2. Unlike other mesoscopic systems, the addition of a single electron can significantly affect the molecule *physically*. Thus, significant charge reorganization can take place in a molecule (discussed in 6.4) upon addition or removal of a *single* electron causing new effects in conduction. For example, electron tunneling through the molecule can excite vibrational modes of the molecule [6, 7]. I will discuss these effects in chapters 4 and 6.
3. The environment of the molecule is very important to electron flow through

it. For example, we find that the presence of neighboring charges can significantly affect the conductance of a molecule (discussed in sections 4.8 and 6.3). Identical molecules that are contacted in different ways to an electron reservoir can have widely differing conductances [8].

4. The electronic structure of molecules can affect electron flow. Small molecules have discrete electronic levels that may or may not be available for electrons to flow through. Thus, a variety of behaviors such as tunneling [9] and single-electron charging [10] are seen in different molecules.

5. Electron flow through molecules can also be phase coherent, resulting in effects such as Kondo-assisted tunneling [11] (discussed in chapters 5 and 7).

1.1.2 Device reasons

Studies of solid-state systems sometimes lead to the invention of socially useful devices, the famous example being the transistor. One reason to study molecule conduction is the attempt to make "molecular electronics" - devices that use organic or metallorganic molecules as an integral part of their device structure. There are several reasons why "molecular electronics" would be desirable:

1. Molecules are small. If one, or a few molecules could be used to make a transistor or a sensor, it would be possible to miniaturize electronic components to a few nanometers.

2. Molecules are cheap. Current (2004) cost estimates for a 300 mm wafer production factory are upwards of a billion dollars [12]. A lot of this cost

stems from the fact that the machines and technology required to create billions of functional devices from silicon that are small (≈ 100 nm at present) are expensive. Molecules, on the other hand, are always perfect. If they can be integrated in a useful way into electronic components, presumably the cost of manufacturing them will decrease.

3. Molecules can be found that have special functional properties. Examples of this kind are the materials that go into organic light-emitting diodes [13], liquid-crystal displays [14] and solar cells [15].

In this thesis, I will mostly talk about the transport properties of devices made from *single* molecules. The reader will find a few interesting facts about electron transport through molecules, but nothing that will be useful in the manufacture of socially useful electronic devices.

1.2 Previous work

Studying conduction through a *single* molecule is still a daunting technological task. The reason is simple - to study molecules that are typically about a nanometer big, you need to have electrical contacts which are defined to this accuracy. Such technology does not exist today. Thus, almost all studies of single molecule conduction involve new experimental techniques. Some of the molecules and techniques used previously are:

1.2.1 Directly contacted molecules, polymers and thin films

The simplest method to make contact to molecules is using conventional lithography. Such direct contact methods are currently limited to thin films of molecules and polymers. Devices made from thin films of molecules have proved to be commercially useful in a variety of applications such as organic light-emitting diodes [16]. Experiments on such systems typically involve two lithographically patterned electrodes between which a film of molecules is present. A few such geometries are illustrated in 1.1. We will discuss one such experiment in 9.1.

Perhaps the only *single* molecule that can be contacted by (current) standard lithographic techniques is the carbon nanotube [17]. Nanotubes are relatively easy to study since they have one long dimension, to which it is easy to make electrical contact (as illustrated in fig. 1.2(a)). These molecules are currently the best candidate for making commercially useful molecular transistors, and electronic devices made from these molecules have properties that easily rival conventional silicon transistors [18]. However, unlike short molecules, they cannot currently be synthesized reproducibly.

1.2.2 Molecules in tunnel junctions

Many of the previous studies of molecular conduction involve the incorporation of several molecules into a tunnel junction between two electrodes. Some of these experiments are illustrated in Fig. 1.3. These experiments all measure electron transport through several molecules in parallel. The assumption made is there is no interaction between the molecules, so that the transport characteristics obtained

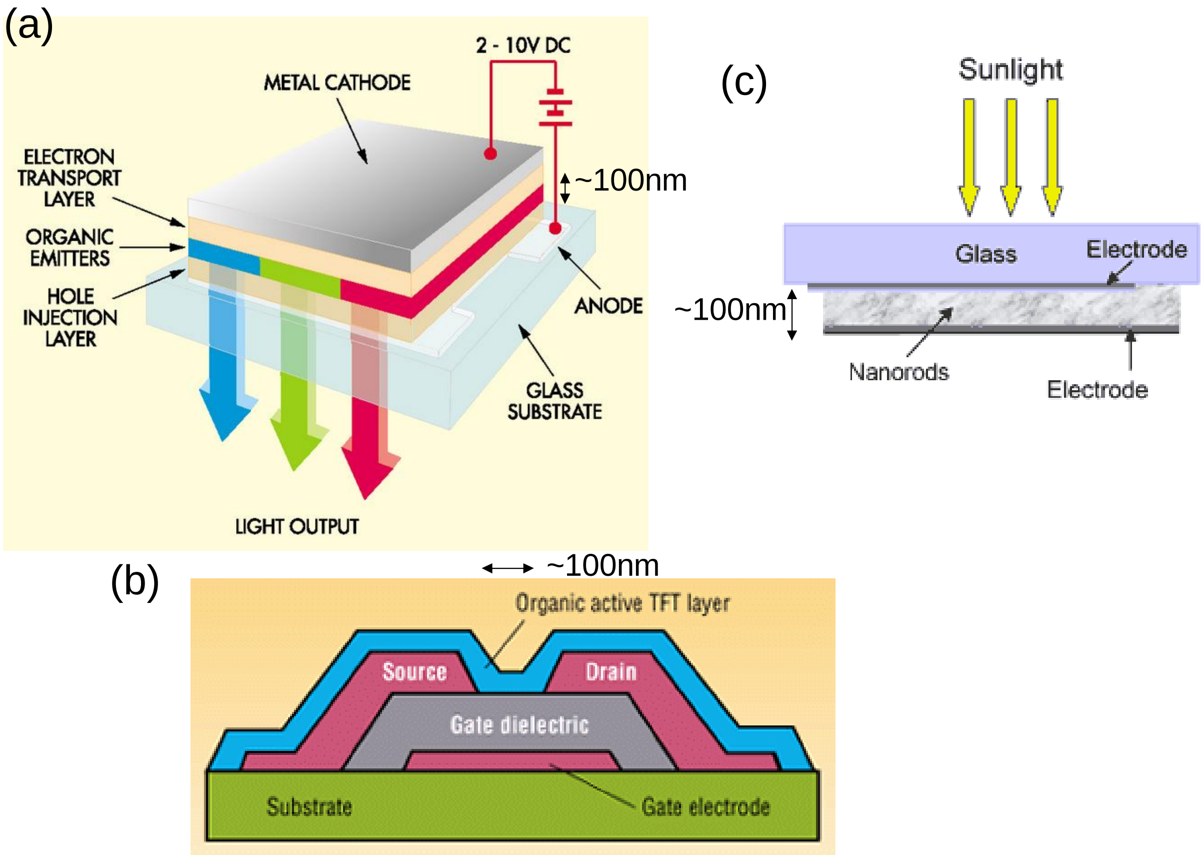

Figure 1.1: Schematic (a) - organic light emitting diode (b) - organic thin film transistor (c) - organic solar cell. These devices can be made by conventional lithographic techniques

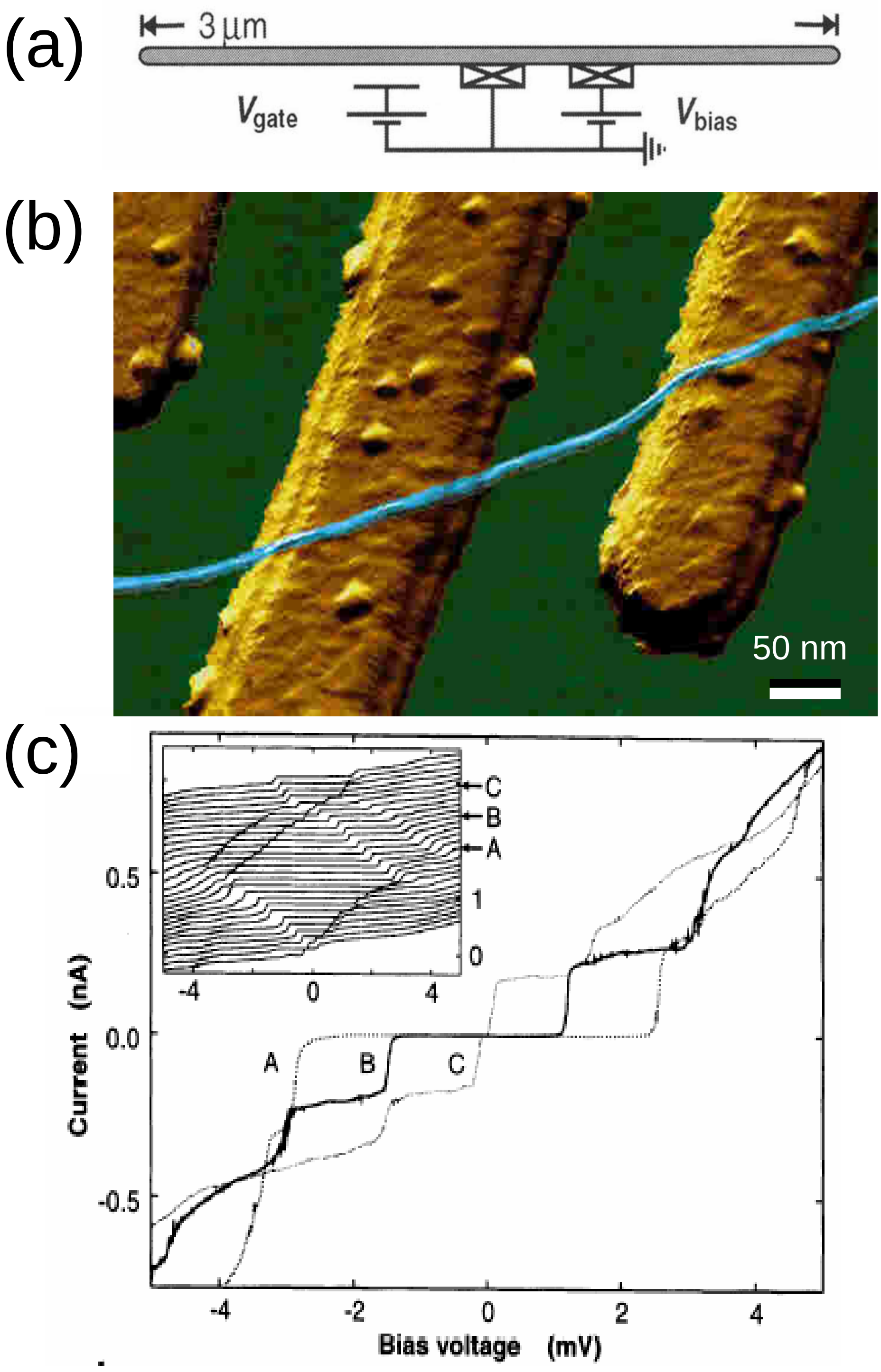

Figure 1.2: Transport through a carbon nanotube, from [10]. (a) Schematic of the device. (b) AFM image of the device. (c) I-V curves at low temperature showing Coulomb blockade.

in the experiment are representative of the transport characteristics of a single molecule. Some of the behavior seen in this experiment is simple tunneling (fig. 1.3(b)) and vibration-assisted tunneling (fig. 1.3(c)).

While these techniques are not difficult to implement, the geometry inherently has two drawbacks. The first is that the active layer is buried in the device and thus cannot be imaged non-destructively. This is a problem since the conduction properties of single molecules are heavily influenced by the atomic-scale contact between the molecule and the electrode. Secondly, there is no possibility of incorporating a gate electrode into the setup. A gate electrode allows for control of the electrostatic potential of the molecule, thus changing its conductance. It is an important tool in understanding the details of electron transport in the device.

1.2.3 Molecules contacted to scanning probes

Another method for making contact to molecules is via scanned probes such as the Scanning Tunneling Microscope (STM) [22] or the Atomic Force Microscope (AFM) [23] (illustrated in Fig. 1.4). In these technique, a layer of molecules is deposited on a conducting substrate. A conducting electrode with a sharp tip scans across and finds one of these molecules. After finding a molecule, the scanning is stopped and the transport measurements are performed. These measurements have the great advantage that they are able to visualize the molecule that is being studied and thus the exact geometry of the device is much better characterized. They suffer from a lack of a gate electrode, as well as the necessity of having a complicated measurement instrument. Behaviors such as Kondo-assisted tunneling

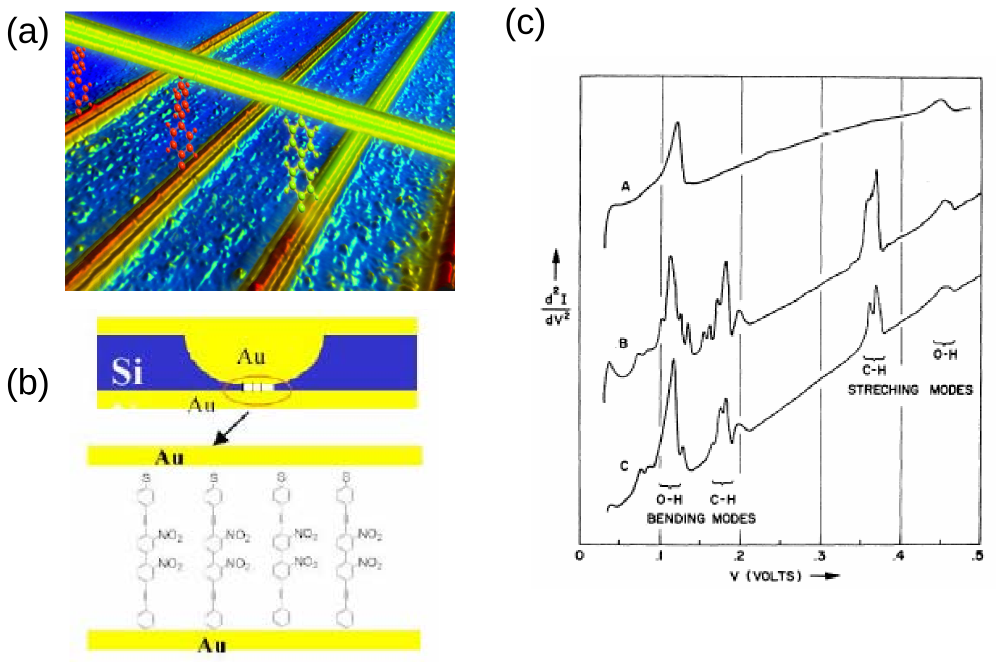

Figure 1.3: Molecules in tunnel junctions. (a) Schematic illustration of crossed-wire experiments [19]. (b) Schematic illustration of the nanopore technique [20, 21]. (c) Data from [6] showing the influence of molecular vibrational modes on electron transport.

[24] (discussed in chapter 5) have been seen in these experiments.

In some beautiful recent experiments [25], a solution is used as a gate electrode in an STM or AFM setup (illustrated in fig. 1.4(c). Conductance histograms of repeatedly-formed junctions created by pressing the tip into the substrate give information about the conductance of individual molecules (fig. 1.4(d)). By applying a potential to the solution, the conductance of the molecule can be changed (fig. 1.4(e)). This technique, while usable only at room temperature, promises to be a useful tool in studying molecule conduction.

1.2.4 Break junctions

A variant on the scanned probe experiments is the mechanical break junction. In this technique, two sharp tips are created by pulling apart a thin wire that is mounted on a flexible substrate. By flexing the substrate the gap between the tips can be repeatedly closed and opened. Occasionally, a molecule can be trapped between the tips [7]. The experimental apparatus required for these experiments is less complicated than conventional scanned-probe techniques. We will describe the manufacture of such devices in detail in chapter 8. A gate electrode can also be incorporated into the setup as described in 8.4. However, these advantages over conventional scanned probes come at the expense of the ability to move the tip in all three dimensions.

Another variant is the technique used in most of this thesis, the electrical break junction. In this technique, a narrow wire is broken by passing high current through it [27] in such a way that a nanometer-sized gap is formed in the wire.

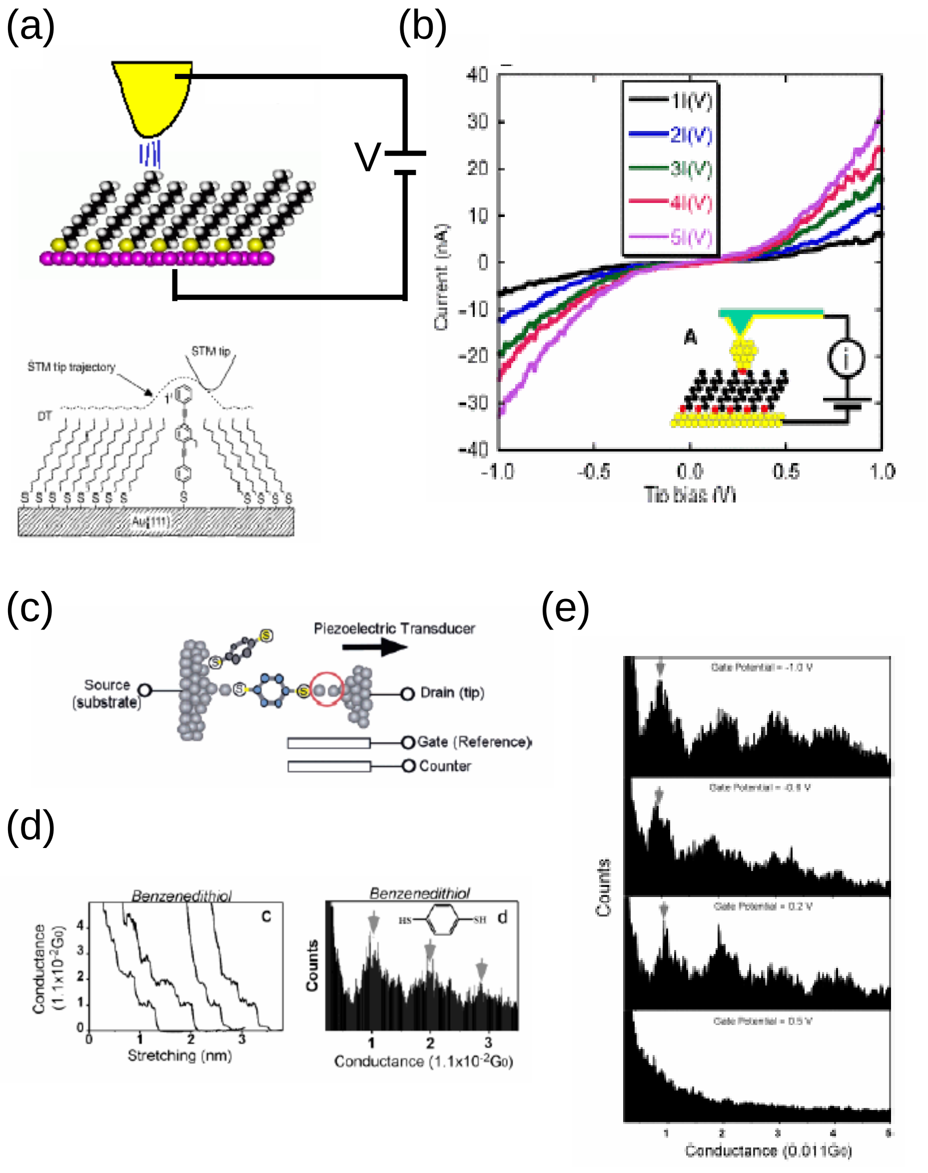

Figure 1.4: Scanned probe techniques for molecule transport measurements. (a) Scanning tunneling microscopy (from [26]) and (b) Atomic force microscopy (from [23]): a tunnel tip is positioned over a molecule. (c) Using an electrolyte to gate the molecule (from [25]). (d) and (e) conductance histograms showing the conductance (d) and its gate voltage dependence (e) of a benzenedithiol molecule.

Molecules can then be incorporated in the gap. We will describe the manufacture of such devices in detail in chapters 2 and 3. We will describe devices made using this technique in chapters 4, 5, 6 and 7.

1.3 Generic features of single-molecule conduction

What has been seen before in experiments where electrons pass through single molecules?

1.3.1 Tunneling

Perhaps the simplest behavior that molecules can exhibit is to act as a simple barrier for electron flow. When two electron reservoirs are separated by a thin insulator, electrons can quantum-mechanically tunnel from one to the other. The WKB approximation for the tunnel current across a rectangular barrier of height ϕ when a voltage $V < \phi$ is applied between the reservoirs is (at zero temperature) [28]

$$I_S(V) = \frac{eA}{4\pi^2\hbar d^2}\left((\phi - eV/2)e^{-\frac{2d}{\hbar}(2m(\phi-eV/2))^{\frac{1}{2}}} - (\phi + eV/2)e^{-\frac{2d}{\hbar}(2m(\phi+eV/2))^{\frac{1}{2}}}\right). \tag{1.1}$$

Here d is the thickness of the barrier and A is the area over which current flows. It is in general not simple to estimate ϕ. One estimate for ϕ is the difference in workfunction between the metal and the ionization potential of the molecule as illustrated in fig. 1.5(a). The situation when you have tunneling between metals with different workfunctions, or if there is charge redistribution at the interface can be considerably more complicated [29]. However, as long as $\phi >> eV$ (as is usually the case in our experiments) eqn. 1.1 can be used effectively to extract barrier heights from I-V curves. A plot of the current from eqn. 1.1 for some typical parameters is shown in fig. 1.5(b)

Such behavior is shown by a number of simple molecules, notably alkane-based molecules [9]. Eqn. 1.1 can be used to make estimates of the barrier height of the molecule. While tunneling by itself is rather unremarkable, useful devices might be made from magnetic tunnel junctions [31].

At voltages low compared to the barrier height ϕ, eqn. 1.1 can be linearized to

$$I_T(V) = \frac{V}{R_T}, \tag{1.2}$$

with the tunnel resistance R_T given by

$$R_T = \frac{4\pi^2\hbar d^2}{e^2 A} e^{\frac{2d}{\hbar}(2m\phi)^{\frac{1}{2}}}. \tag{1.3}$$

1.3.2 Vibration-assisted tunneling

It has previously been observed that molecules incorporated into a tunnel barrier can enhance the tunnel current across the barrier [6, 7]. This enhancement usually leads to a peak in $\frac{d^2I}{dV^2}$, which can be understood from the form of the tunnel current (eqn. 1.1). If we assume that the probability for exciting a given vibrational mode i with energy ω_i is P_i, then the total current flowing across the barrier is

$$I_V(V) = I_S(V) + \sum_{i, V>\omega_i} P_i I_S(V - \omega_i). \tag{1.4}$$

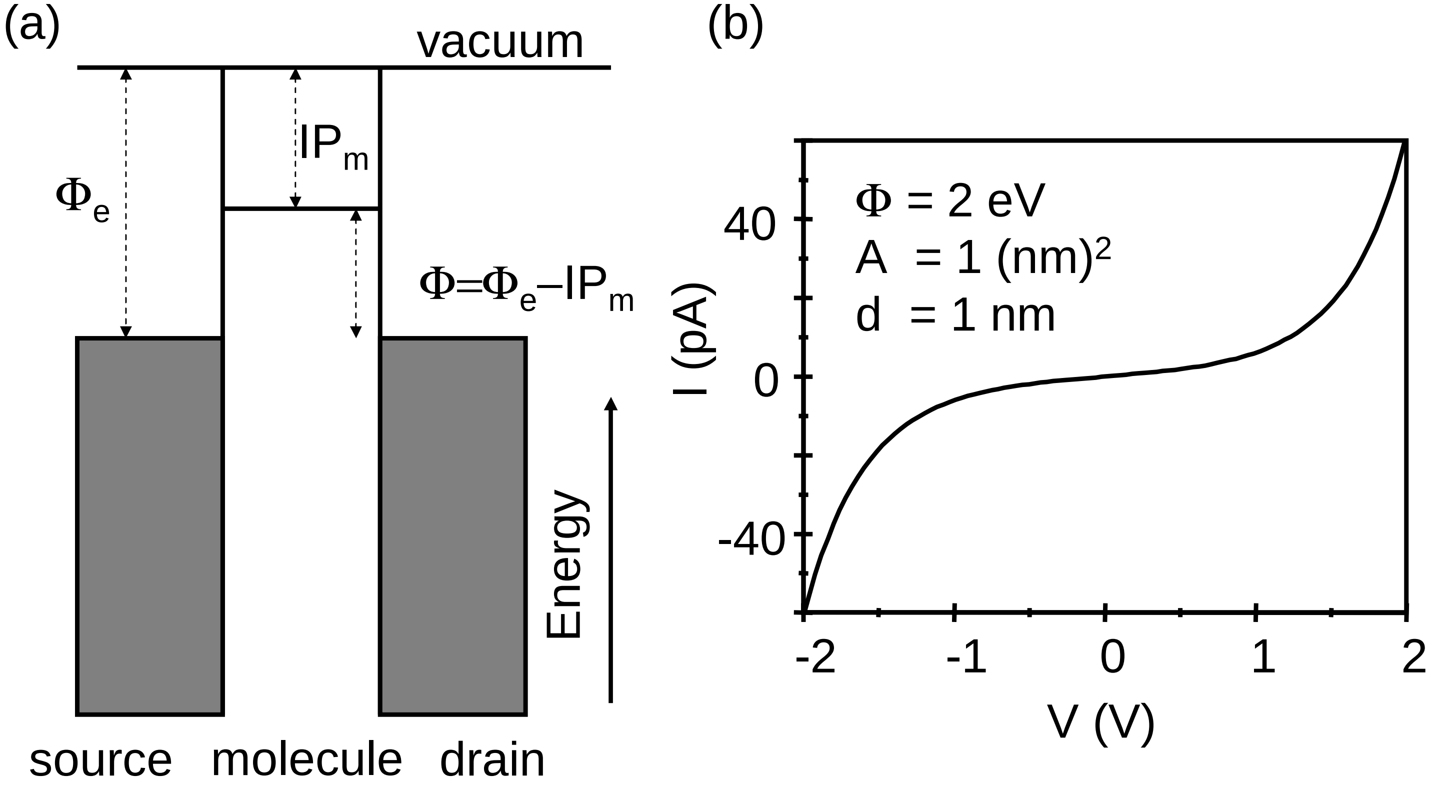

Figure 1.5: (a) Simple model for a tunnel junction. See [30] or chapter 4 for an explanation of the energy diagram. (b) I-V from the Simmons formula eqn. 1.1 for the parameters displayed on the plot.

Here $I_S(V)$ is the current from eqn. 1.1. This equation implies that parallel conduction paths open up at each vibrational frequency with a resistance

$$R_{T,i} = R_T P_i, \tag{1.5}$$

where R_T is the tunnel resistance from eqn. 1.3. These steps in the resistance (and conductance) show up better as peaks in $\frac{d^2I}{dV^2}$ as plotted in fig. 1.3(c)

1.3.3 Coulomb blockade

In certain cases, electrons can tunnel onto and off from resonant energy levels on the molecule. This is very common for example in the case of carbon nanotubes [32]. When a mesoscopic object is capacitively coupled to several electrodes (that are grounded to infinite electron reservoirs) as shown in fig. 1.6 (a), it costs an energy

$$E_c = \frac{Q^2}{2\sum_{i=1}^{N} C_i} \tag{1.6}$$

to add a charge Q to the object. The capacitance entering eqn. 1.6 is at least as large as the self capacitance of the object. For a metal sphere of radius r, the self capacitance is

$$C_\infty = 4\pi\epsilon_0 r, \tag{1.7}$$

with $\epsilon_0 = 8.85 * 10^{-12}\text{F m}^{-1}$ being the permittivity of free space.

This energy cost shows up prominently in current-voltage (I-V) curves, as illustrated in Fig. 1.6. The current is blocked (Coulomb blockade) till the voltage applied is sufficient for electrons to charge the molecule. Once the Coulomb blockade is overcome, the I-V curve depends on the density of states available

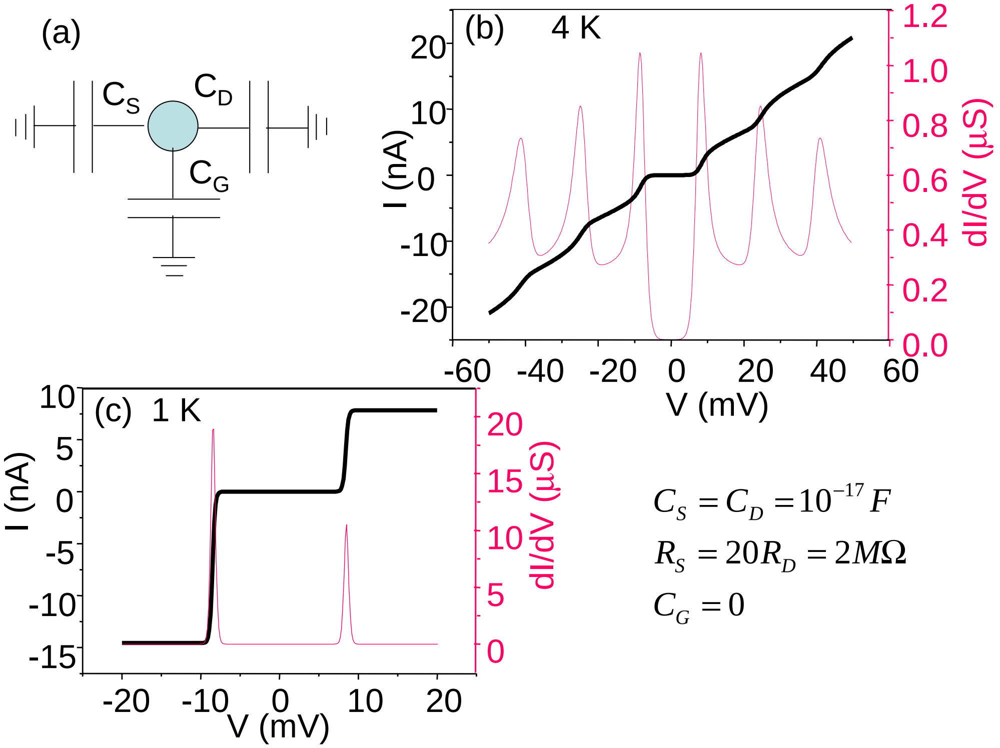

Figure 1.6: (a) It costs an energy $e^2/(C_S + C + D + C_G)$ to add an electron to the dot. (b) Theoretical I-V and dI/dV for a "classical" dot (continuous DOS) - the current continuously increases. (c) Theoretical I-V and dI/dV for a "quantum" dot with a single, spin-degenerate level through which transport occurs. The current saturates beyond the blockade threshold.

for transport on the molecule. If the density of states is continuous (or the level spacing smaller than the temperature), the current increases continuously beyond the blockade region (fig. 1.6 (b)). This is "classical" Coulomb blockade, as against "quantum" Coulomb blockade, where the density of states is discrete, and the current increases in steps beyond the blockade region (fig. 1.6 (c)).

In the case where the density of states is discrete, the energies of the states contributing to electron transport can be deduced from the I-V curve [33]. We will discuss the details of this in chapter 4.

1.3.4 Coherent tunneling

Sequential tunneling of the sort discussed in the previous subsection is an incoherent process. Electrons can also be involved in coherent processes where they temporarily populate resonant states on the molecule (such as the one illustrated in fig. 1.7(a)). Such effects become prominent when there is good contact between the molecule and the electrode (a contact resistance comparable to the resistance quantum $h/2e^2 = 12.9$ kΩ, which can be achieved fairly easily in the case of carbon nanotubes). The Kondo effect is one such coherent many body effect where a spin-degenerate quantum dot that is deep within the Coulomb blockade region can conduct current via all higher-order processes such as the one shown in fig. 1.7(a) [34].

Kondo-assisted tunneling shows up in I-V curves as a peak in dI/dV at $V = 0$ [36], and as a lifting of the "Coulomb blockade" [35]. This has been observed in carbon nanotubes - see fig. 1.7(b). This topic is discussed in detail in chapter 5.

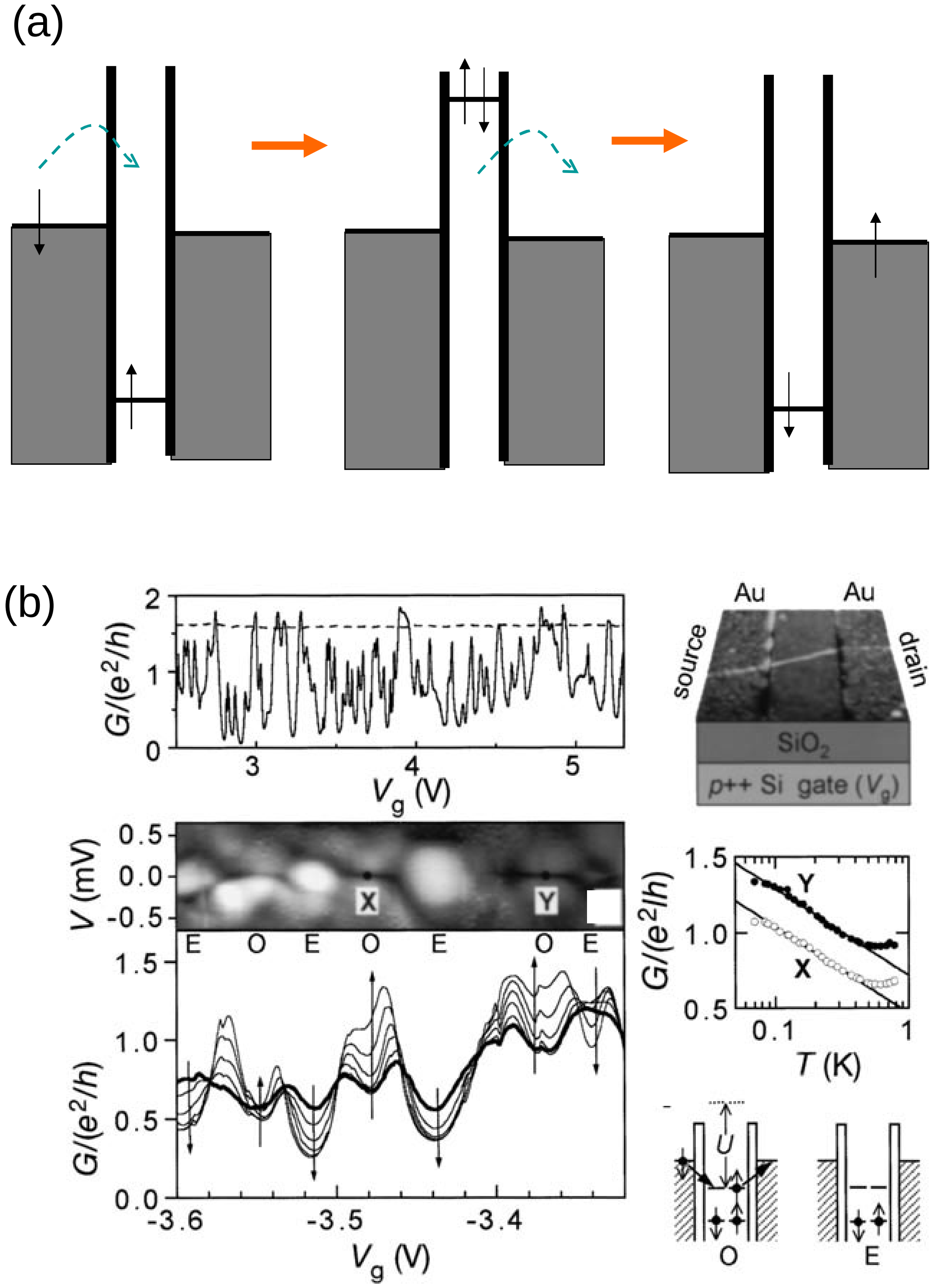

Figure 1.7: (a) Coherent two-step tunneling process that contributes to the Kondo effect. (b) Kondo effect in a carbon nanotube from [35].

1.4 Organization of this thesis

I have discussed briefly the reasons for studying the transport properties of small molecules, and some experiments done previously on this topic. The rest of this thesis is organized as follows.

1. Chapter 2 describes the nanofabrication of electromigration-based break junctions.
2. Chapter 3 describes the electromigration procedure and techniques to perform measurements on samples.
3. Chapter 4 describes the transport properties of $Co-(tpy-(CH_2)_5-SH)_2$ molecules using the techniques described in chapters 2 and 3. A discussion of the generic features of single-electron transistors is included.
4. Chapter 5 describes the transport properties of $Co-(tpy-SH)_2$ molecules. I will briefly describe the Kondo effect in a single-electron transistor.
5. Chapter 6 describes the transport properties of C_{140} molecules. I will describe the effect of vibrational modes of the molecule on electron transport.
6. Chapter 7 describes the transport properties of C_{60} molecules contacted to ferromagnetic electrodes. The emphasis will be on studying the Kondo effect in the presence of itinerant-electron ferromagnetism in the contacts.
7. Chapter 8 describes the fabrication and measurement of mechanical break-junctions. Some preliminary results of the technique will be presented.

8. Chapter 9 briefly describes other experiments performed using the electromigration break-junctions in which I participated, and suggestions are made for future experiments.

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Chapter 2

Sample Nanofabrication - electromigration junctions

In this chapter, I will describe the nanofabrication techniques developed in order to make electrodes suitable for the electromigration procedure described in chapter 3. The aim of the nanofabrication is to make wires of metal that are about 50 - 100 nm wide, attached to macroscopic (several hundred μm) contacts. These wires are separated by a few nm of gate insulator from a gate electrode. Several such wires are made on a chip (fig. 2.1). Several chips are made on a single 4-inch silicon wafer (fig. 2.2). The original geometry was developed by Paul McEuen's group at Berkeley [1]. I have made some changes to the photolithography procedures in order to do the fabrication at Cornell. The electron-beam lithography steps have been developed on the Leica VB6. All the fabrication was done in the old CNF facility in Knight lab, and the procedures described below are specific to the CNF equipment that existed there. With the facility moving to Duffield hall, the procedures should likely be modified to take advantage of the new machines available. The techniques used are part of standard lithographic processing, and can be easily modified to work on specific tools.

There are three basic types of samples we fabricate, which are distinguished by the kind of gate electrode present:

1. No gate electrode present.

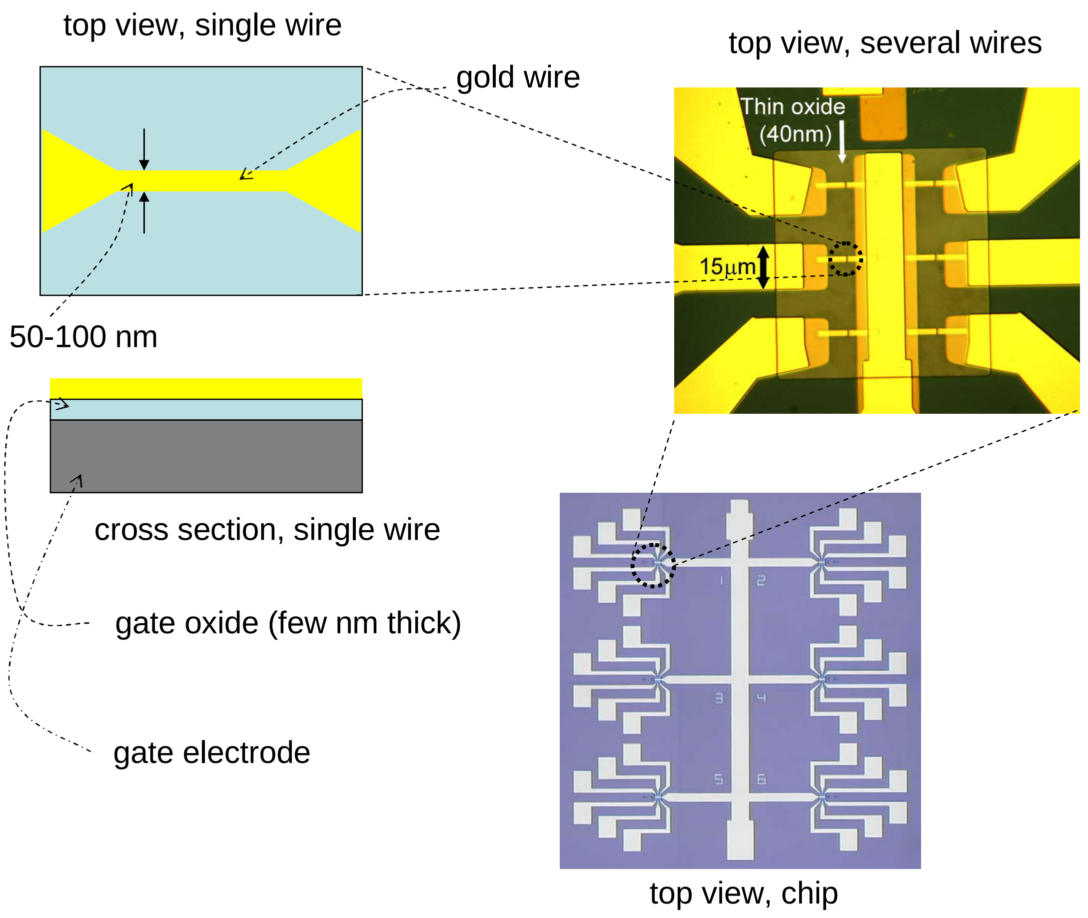

Figure 2.1: The aim of the fabrication process is to create several metal wires on a single 6 mm × 6 mm chip.

2. Silicon back-gate electrode.
3. Aluminum gate electrode.

The end result of the fabrication process is a four-inch wafer as shown in fig. 2.2(a).

I will now describe each of these fabrication procedures in turn.

2.1 Non-gated samples

These samples have no gate electrode present, and are therefore easiest to fabricate. These samples are used for cases where the gate electrode is not needed (some Kondo samples, as discussed in 5) or where a solution-based gate is used (polyaniline transistors described in 9.1). The process flow diagram is shown in fig. 2.3. I will now describe in detail each of the steps of the procedure.

2.1.1 Field oxide

We start with a 4-inch diameter silicon wafer that is polished on one side. Our first job is to grow a thick layer of oxide on the wafer so that it is an insulating substrate for the remaining steps.

I have experimented with buying wafers that have already been oxidized by the manufacturer. I have had a couple of very bad experiences. In one particularly bad case, the oxide looked fine to the naked eye, but turned out to be very porous. On

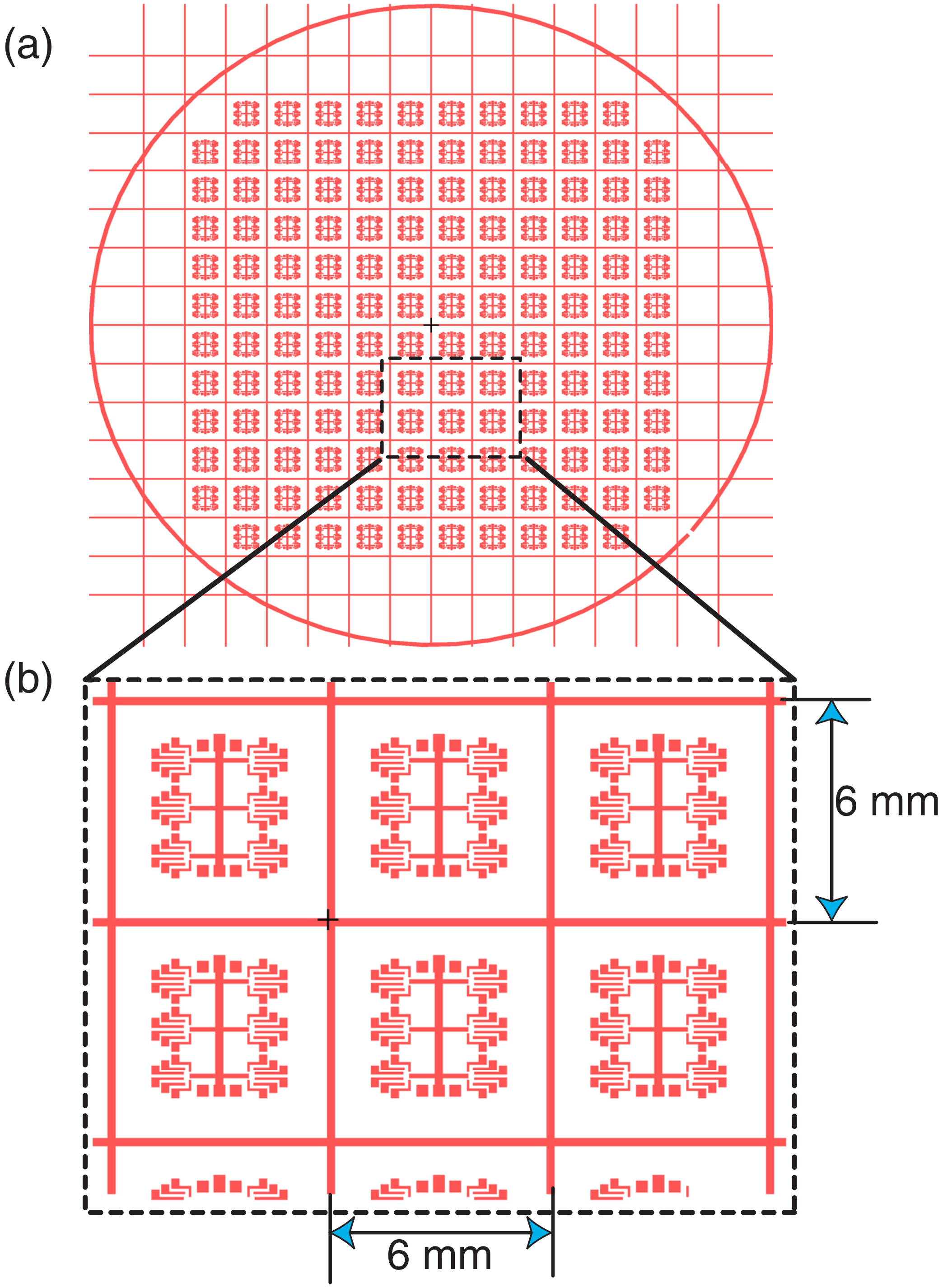

Figure 2.2: (a) View of the wafer after completion of the front-end processing steps (b) Magnified view showing the dicing streets.

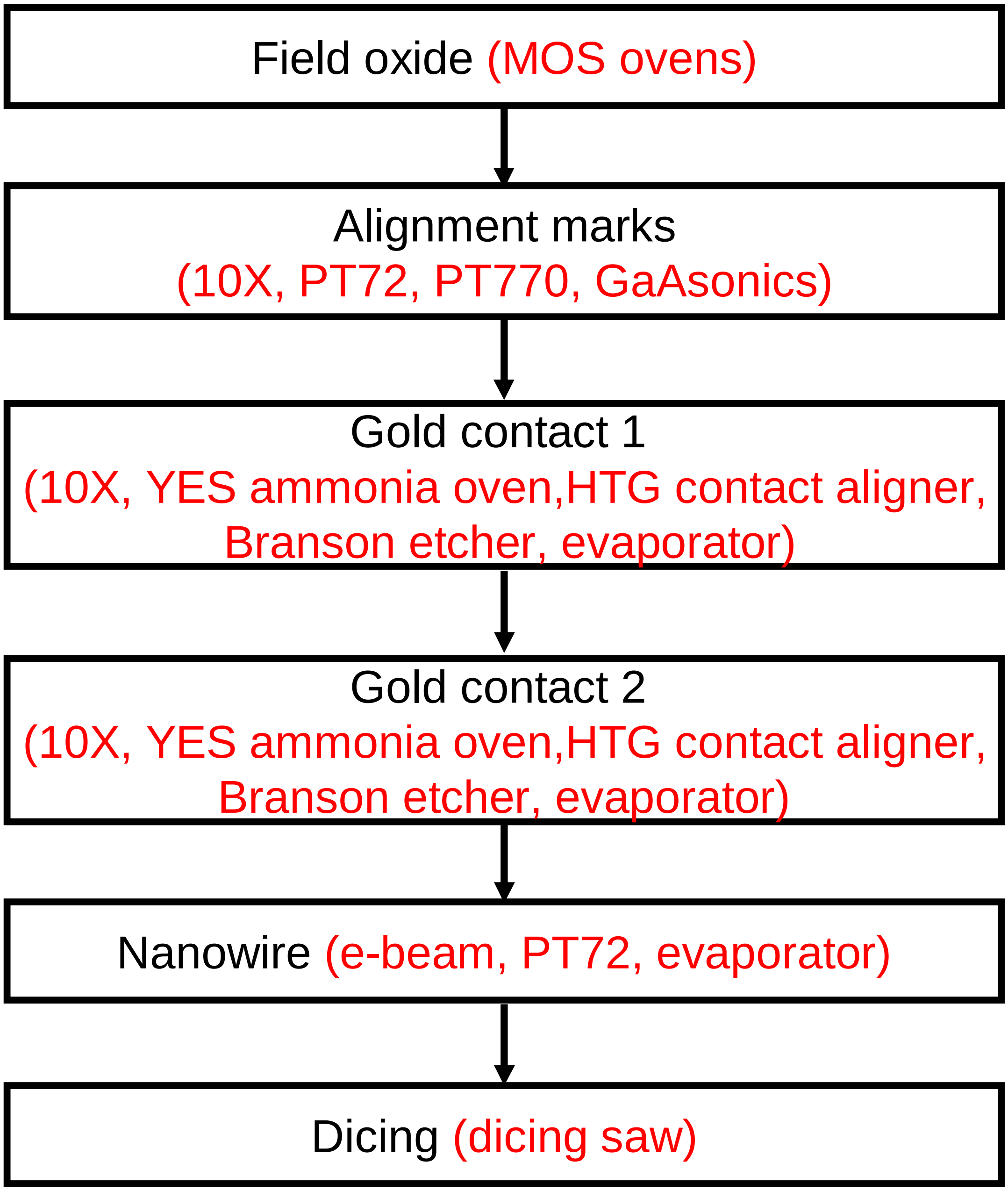

Figure 2.3: Process flow for the fabrication of non-gated samples. In red are given the names of the various machines that are used in the corresponding step of the fabrication process

exposing any resist spun on this surface to ultraviolet light, minute defects would appear on the wafer, presumably from explosions of trapped gas. In another case I received electrically leaky oxide. For these reasons, I strongly recommend growing the oxide at Cornell. It is better to spend a day growing good oxide than a week understanding what is going wrong with your wafers.

The oxide is grown by the TCA wet oxidation process in the MOS ovens. Anything thicker than 200 nm works well as an insulator. Oxides thinner than about 100 nm are sometimes damaged by the wirebonder. If the oxide grown is too thick ($>$ 500 nm), you will spend forever dry-etching it. It took about a half-hour to grow this oxide in the furnaces in Knight lab.

2.1.2 Alignment marks

The next step is to make alignment marks in the wafer to align the different photolithography layers. I usually do this step on several wafers at one time. The process is:

1. Prime the wafer for resist. If I am doing a large batch of wafers (almost always the case), I use the vapor prime process in the YES oven. If you do not want to spend the 20 minutes required to do this, spin on P-20 at 4000 rpm for 30 seconds.

2. Spin coat S1813 resist at 3000 rpm for 50 seconds. This gives a thickness after baking of 1.1 μm.

3. Bake on the hot plate at 115 °C for 1 minute.

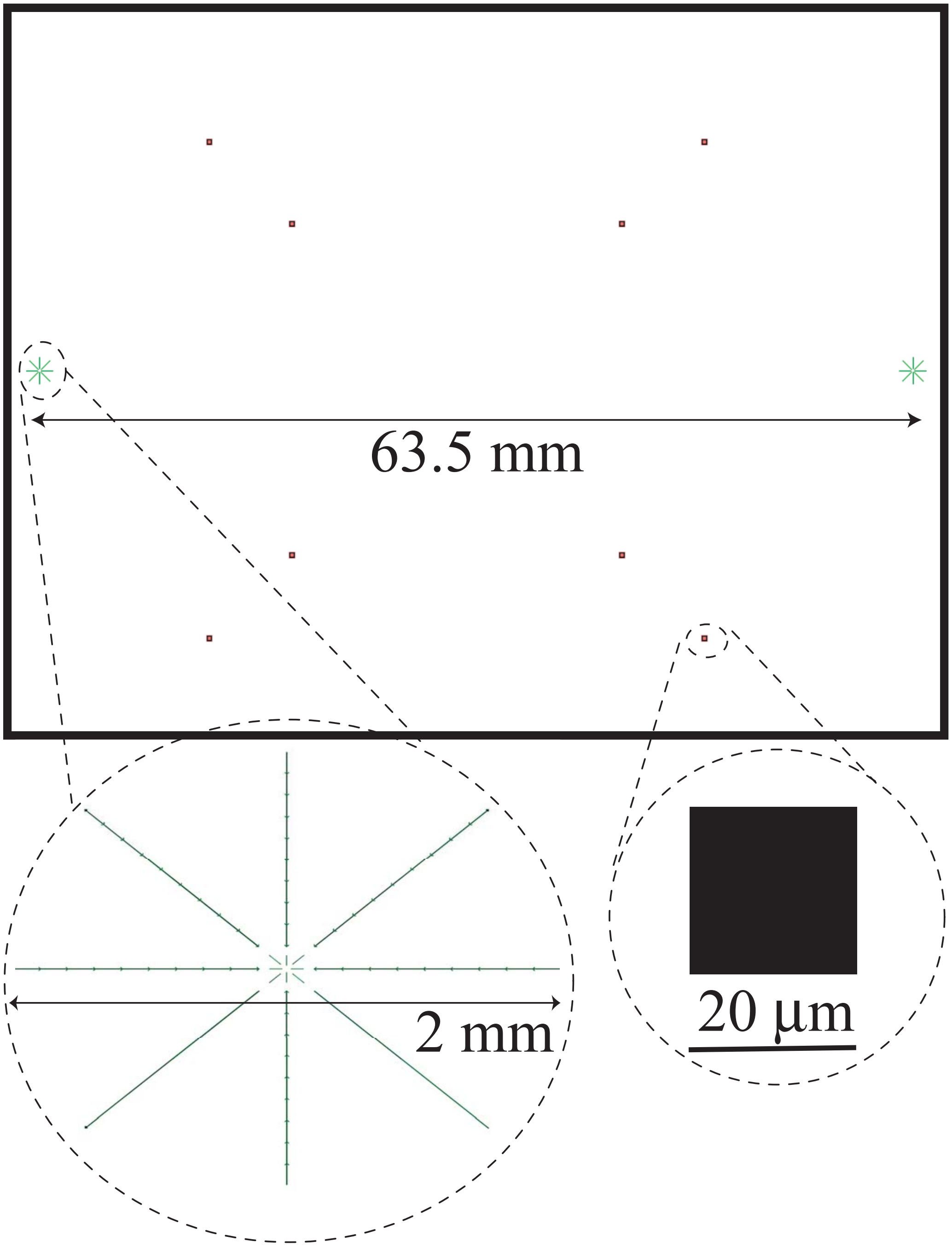

Figure 2.4: Alignment mark mask. The stepper marks are GCA_ KEYs.

4. Expose on the HTG contact aligner for 6 seconds. The mask I use is shown in fig. 2.4. It has the 10X stepper alignment marks (GCA_KEY) spaced the usual 63.5 mm apart. It also has some 20 μm squares that can be used for alignment on the e-beam, although I usually do not use them.

5. Develop in MIF-300 for 1-2 minutes.

6. Etch through the oxide. I try to do this in parallel on two etchers (Applied Materials RIE and PT72). Three wafers go into the PT72 and two into the App. Mat. at one time. Start with a 30 second descum using an oxygen plasma. This is recipe 1 on the PT72. The settings on the App. Mat. are a power of 90 watts, an oxygen flow of 30 sccm and a chamber pressure of 30 mtorr. Then etch through the oxide. I use the 30 sccm CHF_3/ 1 sccm O_2 recipe on both machines. The nominal etch rate is 30 nm/min. I etch for twice as long as this rate suggests.

7. Etch into the silicon. This helps you see the marks well on the 10X's ancient monitor and is essential if you want to do e-beam alignment with this level. I use the PT770 and Unaxis770 in parallel if possible. Two minutes of the standard trench etch etches about 4 μm into the silicon, which is plenty.

8. Get rid of the resist. The easiest way to do this is on the GaAsonics asher. I use the recipe with the highest power and time settings.

2.1.3 Thin gold layer

The purpose of this layer of metal is to make electrical contact with the nanowire. I usually do this step on a batch of four wafers, since the metal deposition can be done on all four at one time (with the help of Ferdinand's German technology - the evaporator stage that can be used to perform evaporations on four 4-inch wafers in a single pumpdown). The process is:

1. Prime the wafer, coat and bake S1813 resist as described in 2.1.2.
2. Expose the wafer on the 10X stepper using the mask shown in fig. 2.5. I do a 12×12 array of these patterns spaced 6 mm apart (the corner dies do not fit on the wafer and have to be dropped). If you use standard keys on the job, the key offset is X=-1.25 mm, Y=-9 mm. I use a 2 second exposure.
3. Bake the wafer in the YES ammonia oven for the usual 78 minutes.
4. Flood expose the wafer on the HTG contact aligner for 60 seconds.
5. Develop the wafer in MF-321 for 90 seconds.
6. Descum the wafer for one minute on the Branson barrel etcher using the standard descum recipe.
7. Evaporate 2 nm of titanium or chrome + 15 nm of gold on the wafer.
8. Liftoff in acetone for 2-3 hours.

The ammonia bake procedure creates an undercut profile. This is shown in fig. 2.6. Here, a sample pattern was created using the image-reversal procedure, and aluminum was evaporated over the wafer. The false-color SEM image in the figure shows a typical undercut of about 0.3 μm. The resist shadows the evaporated metal. Since the angle with which the evaporated metal hits the wafer is different at different points across the wafer, the patterns on the wafer will have some

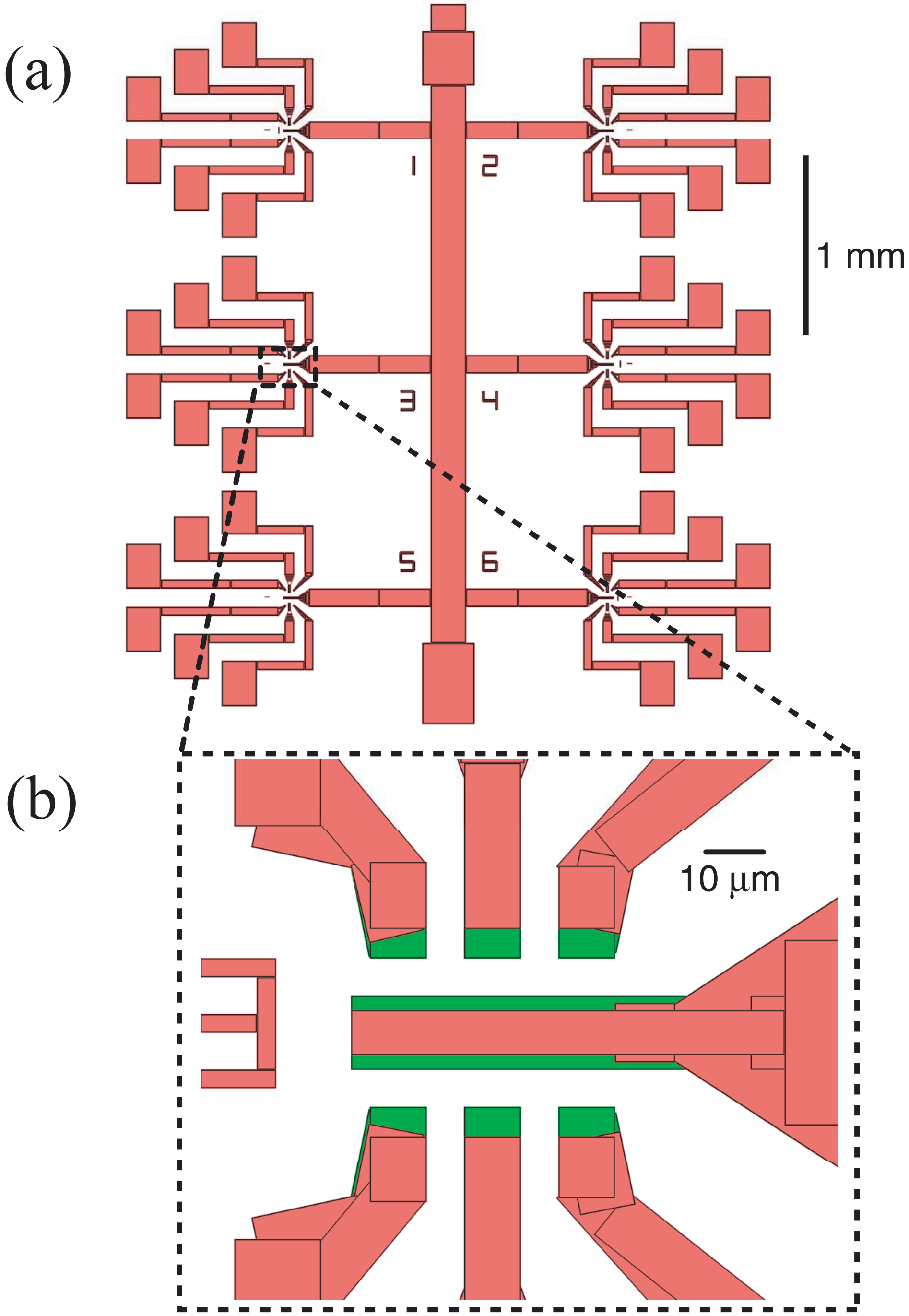

Figure 2.5: (a) Mask for the thin and thick gold layers. (b) Magnified view showing the difference between the thin (green) gold layer and thick (red) gold layer.

spread in position across the wafer. This is evident on the SEM image. For a four-inch wafer in the Sharon evaporator, the spread in the position of the pattern is about 200 nm across the wafer. While the image-reversal process takes longer to complete, it works more reliably than the two other processes I have used to create undercut (chlorobenzene [2] and toluene [3] soak).

2.1.4 Thick gold layer

The purpose of this layer is to have thick metal to which you can make wirebonds. I use about 150 nm of gold for this purpose. The fabrication process for this layer is identical to the previous layer. The mask used is very similar to the one used for the thin gold layer. It is also shown in fig. 2.5.

Both the mask used in this layer as well as the thin gold layer are image-reversed masks. It is possible to make the 6×6 mm dicing grid shown in fig. 2.2 with these masks. Simply make the image-reversal bounding box a little smaller than 6 mm (say 5.99 mm). This will automatically create nice 20 μm-wide dicing streets on the wafer.

2.1.5 Electron-beam lithography

The all-important nanowire itself is created by electron-beam lithography on the Leica VB6. Any dedicated e-beam writer with sub-100 nm resolution should work fine. This process goes as follows:

1. Pre-clean the wafer by running an oxygen plasma on the Branson barrel

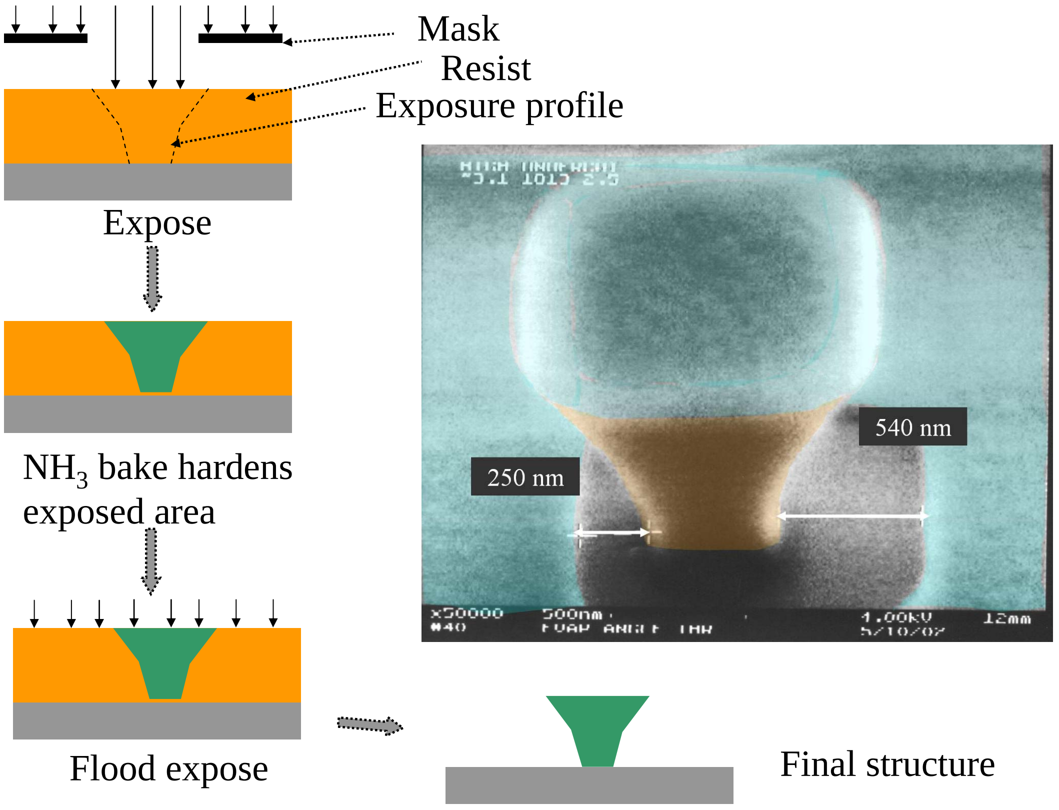

Figure 2.6: The image-reversal process. The false-color SEM image is taken after evaporation of 100 nm of aluminum (blue) on the wafer (grey) after the image reversal process. The resist is colored brown.

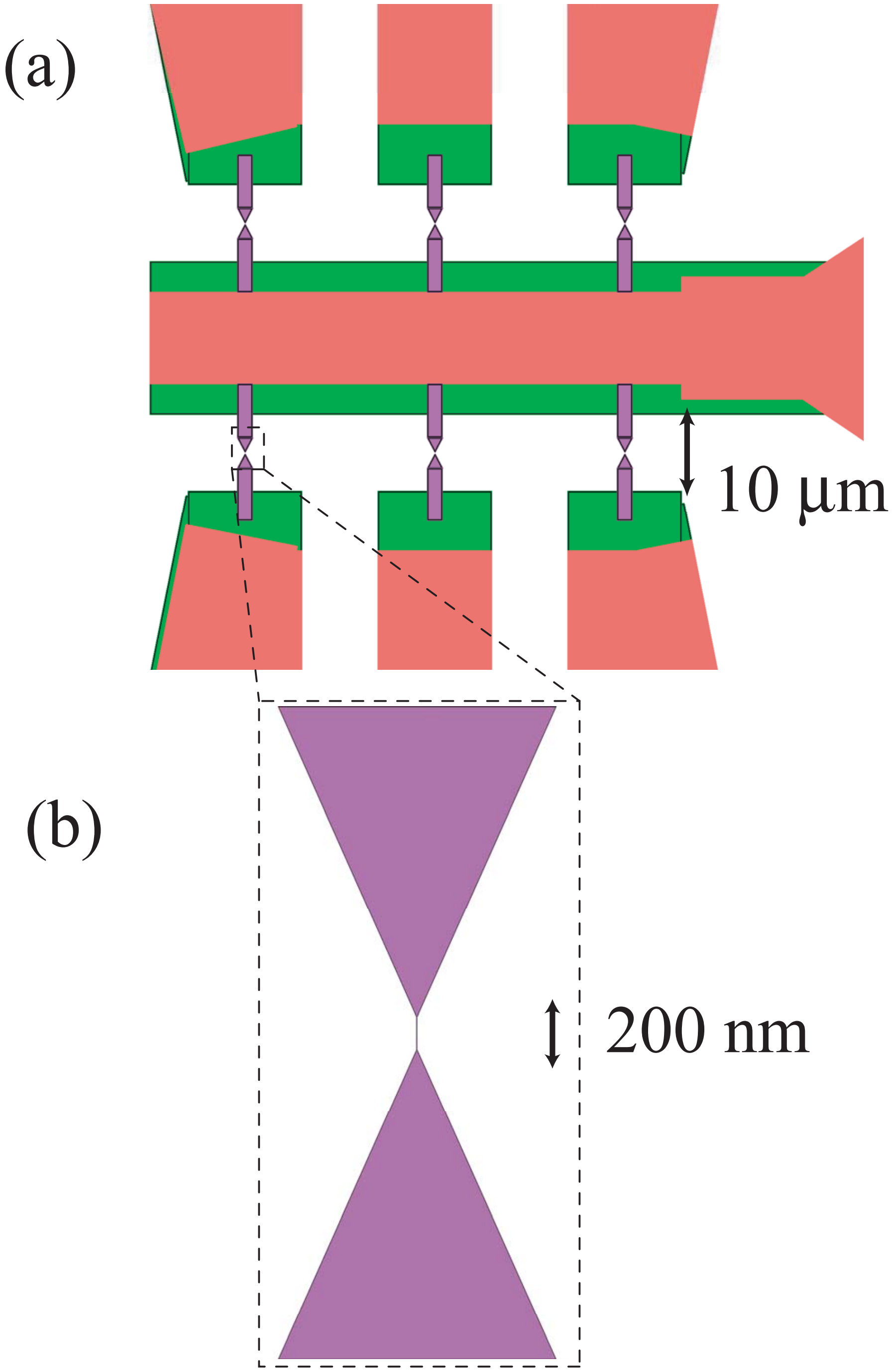

Figure 2.7: (a) Typical e-beam pattern used (purple area)(b) Magnified view. The narrowest feature is a single-pass (5 nm) line.

etcher for 1 minute.

2. Spin on resist. I have used various different resist recipes. The one I use the most is:

    (a) Spin on PMMA/MAA copolymer (3:1 or 1:1 in Ethyl lactate) to a thickness of 200-250 nm.

    (b) Bake on the hot plate at 170 °C for 15 minutes.

    (c) Spin on 4 % 496 K PMMA to give a final thickness of 130 nm.

    (d) Bake on the hot plate at 170 °C for 15 minutes.

    Other bilayer recipes (such as 496 K PMMA / 950 K PMMA) can be used, which produce slightly narrower lines. The copolymer recipe described above gives >100 nm undercut, which makes liftoff work well. However, the minimum linewidths obtained on a regular basis with this resist is limited by the thickness of the resist to about 60 nm.

3. Get your pattern ready for the VB6. This involves creating a GDS file from L-Edit, converting to CFLT format using CATS and then using WRITEFILE to convert it to FRE, which is what the VB6 accepts. Pay attention to the centering of the pattern. The program JEBCAD is useful for checking this. In general, if you are doing this for the first time, ask somebody about this procedure, or it will most likely not work. A typical pattern used is shown in fig. 2.7.

4. Expose the wafer on the VB6. I have been using three (automatically located) global alignment marks (in particular, the number “1” on the thick gold layer) to do the alignment of the ebeam pattern to the photolith patterns.

This gives me <0.5 μm placement accuracy across the wafer. Much better accuracy can be achieved by doing a die-by-die alignment, at the cost of additional time lost in finding these marks.

The dose depends on your pattern. Typical area doses I use (relevant to fig. 2.7) are:

   (a) Areas larger than 10 μm × 10 μm : 800 μC/cm^2.
   (b) Between 1 and 10 μm a side : 1000 μC/cm^2.
   (c) Between 100 nm and 1 μm a side : 1500 μC/cm^2.
   (d) Single-pass lines : 6000 μC/cm^2.

5. Develop the wafer. I develop in 1:3 MIBK:IPA for 65-70 seconds, transfer to methanol for 15-20 seconds and rinse in IPA. The methanol etches the bottom layer of resist.

6. Descum the wafer. Before the descum, clean the PT72 for at least 30 minutes. I clean it for 20 minutes using the high-power oxygen plasma recipe #6, followed by 10 minutes using process #1. After this, descum your wafer for 6-8 seconds (not longer, or all your PMMA will disappear) using the low-power recipe #1.

7. Evaporate 20 nm of gold or whatever else catches your fancy.

8. Liftoff the resist for 6-8 hours. Agitate every half-hour or so. Use sonication or swabs if necessary, although you run the risk of lifting off your metal as well.

2.1.6 Dicing

At the end of the previous step, you will have a four-inch wafer with a pattern as shown in fig. 2.2. The final step is to dice your wafer into chips. The streets along which the dicing has to be done (a 6×6 mm grid as shown in fig. 2.2(b)) have already been defined by the masks for the thin and thick gold layer. The process for dicing is:

1. Prime the wafer as described in 2.1.2.
2. Spin on S1827 resist at 3000 rpm for 50 seconds. This gives a thickness of $\approx$ 3 μm after baking.
3. Bake on the hotplate for 2-3 minutes at 90 °C.
4. Dice it into 6×6 mm chips on the Cornell dicing saw or (more reliable, since the Cornell saw has been known to kill wafers) send it out to a dicing company to get it diced [4].

2.2 Silicon back-gated wafers

These samples use the wafer itself as a gate electrode. For the wafer to be conducting at low temperature, it has to be heavily doped. Wafer retailers specify the resistivity of the wafer at room temperature. A resistivity of 0.001-0.005 $\mu\Omega$cm works well. The process flowchart for making samples is shown in fig. 2.8.

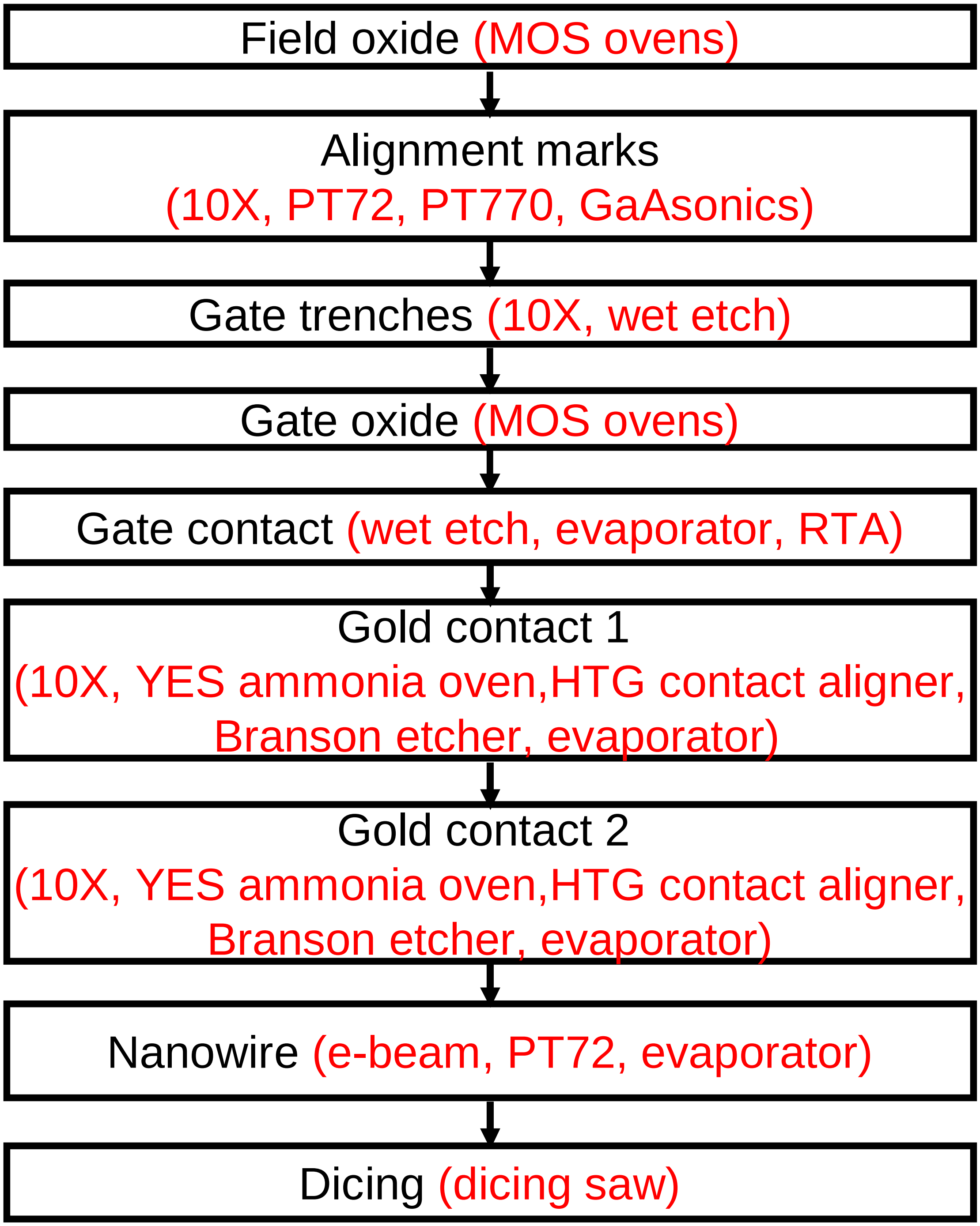

Figure 2.8: Process flow for the fabrication of silicon back-gated samples. In red are given the names of the various machines that are used in the corresponding step of the fabrication process

2.2.1 Field oxide

This works exactly the same way as for the non-gated samples (2.1.1). You should grow a slightly thicker oxide (about 50 nm thicker) to account for the etching that will happen in 2.2.4.

2.2.2 Alignment marks

This step is also done the same way as for non-gated samples (2.1.2).

2.2.3 Gate trenches

The next step of the fabrication process is to make trenches that reach down to the silicon substrate. I usually perform this step on 25 wafers at one time. The process works as follows:

1. Prime, spin coat and bake the wafers as in 2.1.2.
2. Expose the wafer on the 10X stepper using the mask shown in fig. 2.9, and the same alignment procedure as 2.1.3.
3. Develop the wafer in MIF300 for 90 seconds. Rinse in water.
4. Descum the wafer for 30 seconds on the applied materials RIE or the PT72 RIE using an O_2 plasma. It is good to do this (rather long) descum rather than risk micromasking by scum.

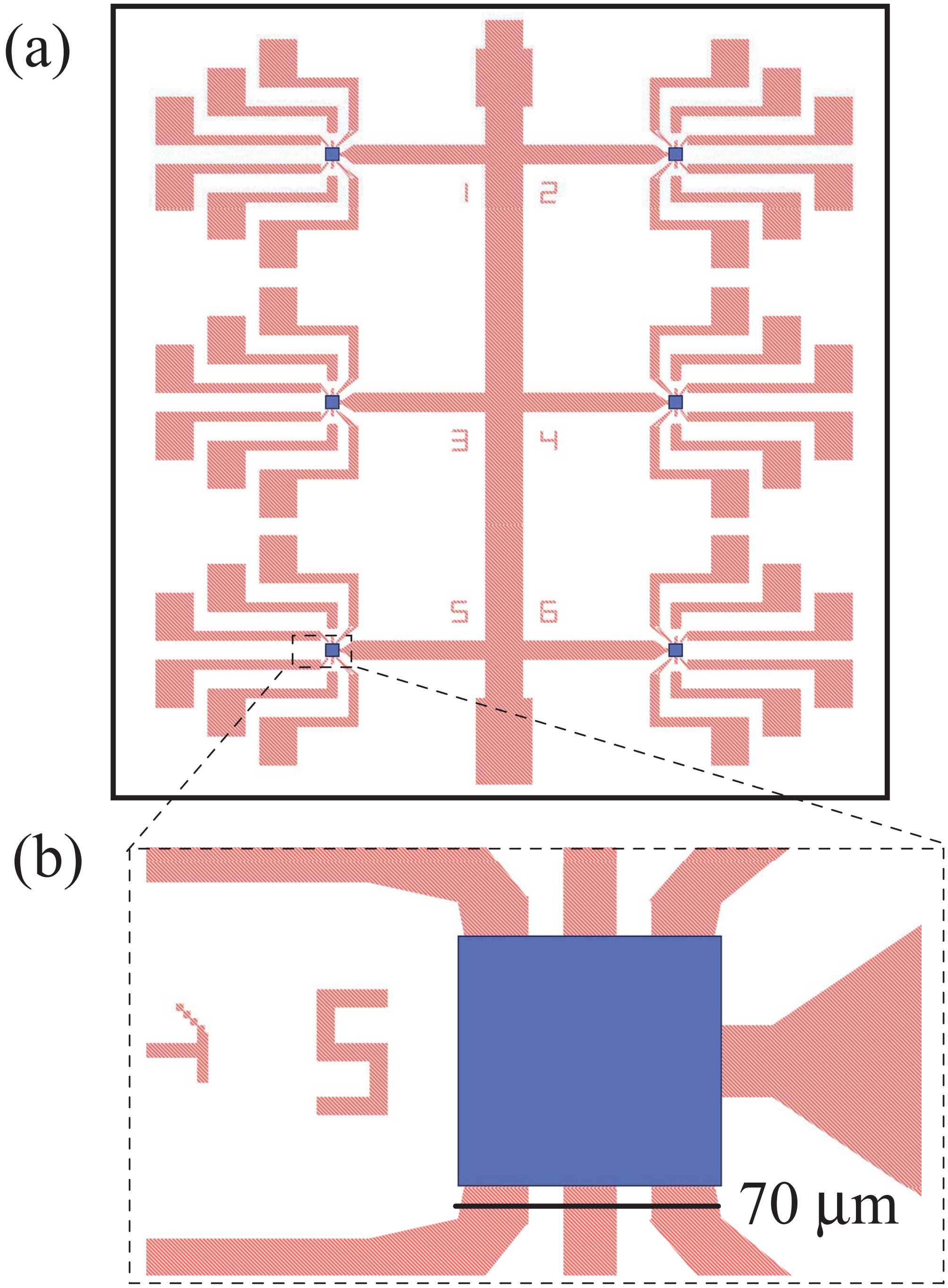

Figure 2.9: (a) Mask for making gate trenches. The squares shown in blue are part of the mask. The red area shows the alignment with the metal layers (b) Magnified view

5. Etch the oxide in buffered HF (1:6 in NH_4F). The nominal etch rate is about 30 nm/minute. Etch for about twice as long as this rate suggests. Rinse in water.
6. Remove the resist with the GaAsonics asher as in 2.1.2.

2.2.4 Gate oxide

The next job is to grow the oxide that will insulate the gate electrode from the source and drain electrodes. I usually do 6-12 wafers at one time. The process is:

1. Do the MOS RCA clean on the wafers.
2. Grow the oxide using the dry oxide process. I have found that a thickness of about 30 nm upwards is reasonably defect-free (breakdown fields ≈ 1 V/nm). I once grew 10 nm of oxide and about half the gates leaked badly. This might have changed with the new ovens. There are two reasons to have thin gate oxide:
    (a) Although the breakdown field is roughly independent of the gate oxide thickness, having a gate closer to the sample by a factor of two does increase the capacitive coupling of the gate to the molecule by more than a factor of two.
    (b) You have to apply smaller gate voltages. The voltage sources I have used (HP3325A, Yokagawa 3651) produce noise proportional to the signal amplitude. Thus, having smaller signal amplitudes reduces capacitive noise pickup on the source and drain lines going down the cryostat.

At the end of the growth process, take one wafer out of the MOS area and measure its thickness using the interferometer. You can then adjust the oxide growth time in the next growth process.

3. Etch the oxide using the diluted HF kept in the MOS clean wet bench. I usually overetch by a factor of 1.5.
4. Repeat the growth of the oxide using the dry oxide process. The reason the first growth and etch of the oxide is done is to increase the smoothness of the surface of the oxide. Whether this really is necessary or even true has not been tested by me, but it seems to be popular among the MOSFET makers at Cornell.

2.2.5 Gate contact

The next step in the process is to make contact to the gate electrode. The process is:

1. Protect the front surface of the wafer with resist. S1827 with a thickness of 3 μm works quite well for this purpose. Use the same recipe as sec. 2.1.6.
2. Use a cotton swab dipped in acetone/IPA to make sure that there is no resist residue on the back surface of the wafer. Take care to make sure the acetone does not ruin the front surface resist coat.
3. Wet etch the oxide from the back surface using buffered HF (same recipe as sec. 2.2.3

4. Evaporate metal to make contact to the back surface. I usually try to do the evaporation right after the etch. Good metals to make contact to the wafer are those that react with silicon to form silicides. The best choice is platinum. Platinum is quite difficult to evaporate on the Sharon evaporator since it requires a high e-gun current to get it to evaporate. Consequently, the substrate gets hot during the evaporation and the resist can melt. While doing platinum, I water-cool the stage and evaporate about 50 Å at one time, with a 5 minute cool between successive evaporations. To avoid waiting forever, my favorite recipe for the gate contact is 200 Å of platinum followed by 1000 Å of titanium, finally capped by 200 Å of platinum.
5. Remove the resist from the front surface by soaking in acetone, followed by a 5-minute oxygen plasma on the Branson barrel etcher. Do not use the GaAsonics asher once there is metal on the wafer - the metal is quite likely to disappear if you do this.
6. Anneal the wafer to make good electrical contact. This is done on the RTA Heatpulse, at 400 - 500 °C with a 1 minute warmup.

If you have any gold on the wafer while doing the anneal, it will flow all over your wafer and make a mess. This is why the gate contact has to be done before the other metal steps. I tried skipping the anneal step twice. I got good ohmic contact on one wafer but did not on the other.

2.2.6 Thin gold layer

This step is performed the same way as in sec. 2.1.3.

2.2.7 Thick gold layer

This step is performed the same way as in sec. 2.1.4. Here, the gold serves the additional purpose of making electrical contact between the top and bottom of the gate trench created in sec. 2.2.3. The fact that the gate trench was created by wet etching helps, since the sidewall profile will be rounded by the wet etchant. However, it is still essential to have a gold layer that is at least one-half the height of the gate trench in order to make reliable electrical contact.

2.2.8 Electron-beam lithography

This step is performed the same way as in sec. 2.1.5.

2.2.9 Dicing

This step is performed the same way as in sec. 2.1.6.

2.3 Aluminum-gated wafers

Since 2003, we have been using aluminum as the gate electrode. Our fabrication process follows that used by Persson [5] and developed by Liang [6]. The process flowchart is shown in fig. 2.10. The steps are explained below.

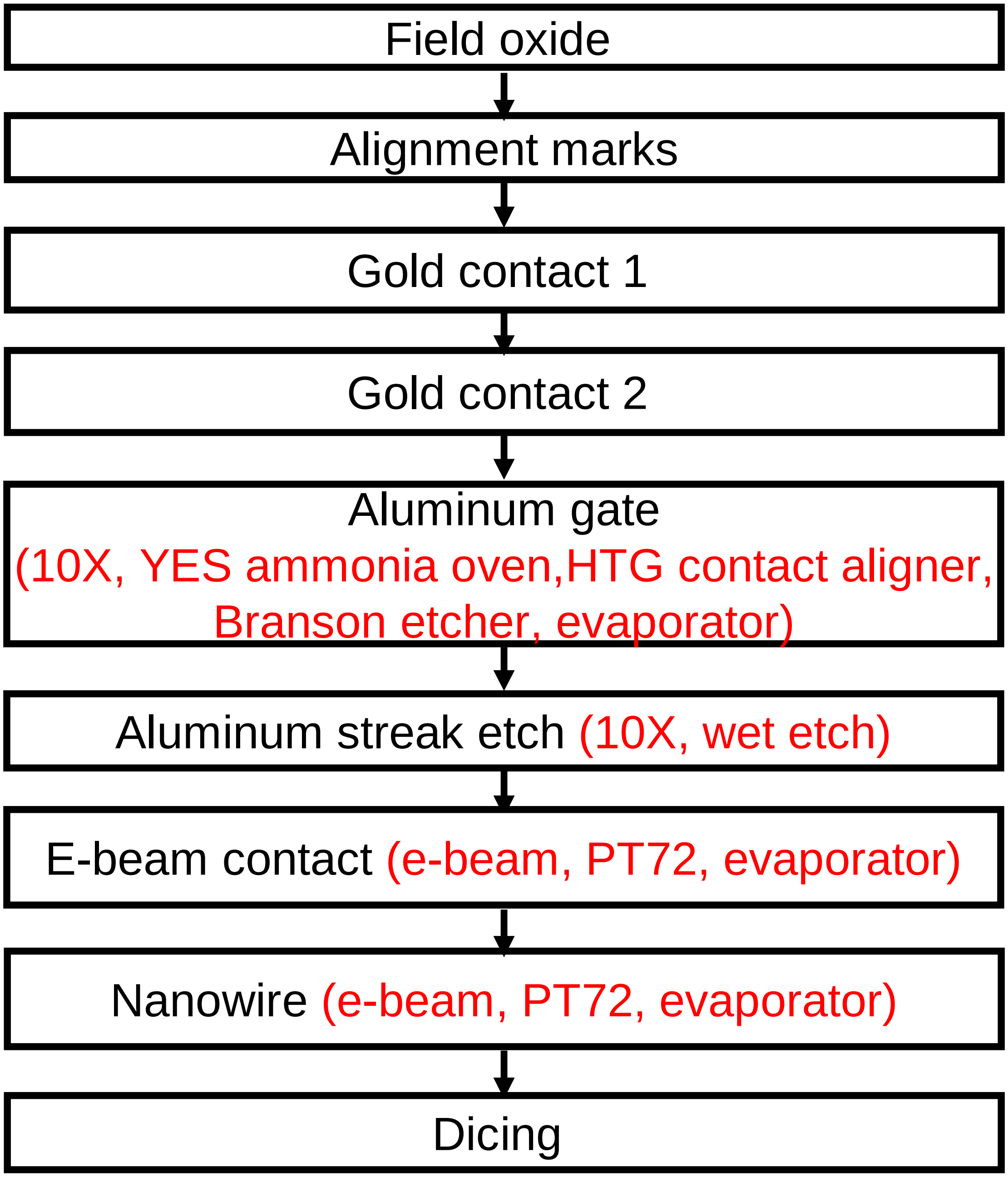

Figure 2.10: Process flow for the fabrication of aluminum-gated samples. In red are given the names of the various machines that are used in the corresponding step of the fabrication process (for steps common to sec. 2.2, please refer to fig. 2.8.

2.3.1 Field oxide

The first step of the fabrication procedure, is to grow the insulating field oxide as in sec. 2.1.1. The substrate need not be conductive at low temperature.

2.3.2 Alignment marks

This step is performed as in sec. 2.1.2.

2.3.3 Thin gold layer

This step is performed as in sec. 2.1.3.

2.3.4 Thick gold layer

This step is performed as in sec. 2.1.4.

2.3.5 Aluminum gate electrode

The next step of the fabrication is to lay down the gate electrode, which is a strip of aluminum as illustrated in fig. 2.11(b). The photolithography is done the same way as sec. 2.1.3 using the mask shown in fig. 2.11(a). I take a little more care while developing the resist in this step than in the other steps, since the feature size is smaller. I first develop the wafer for 60 seconds and inspect it under the optical

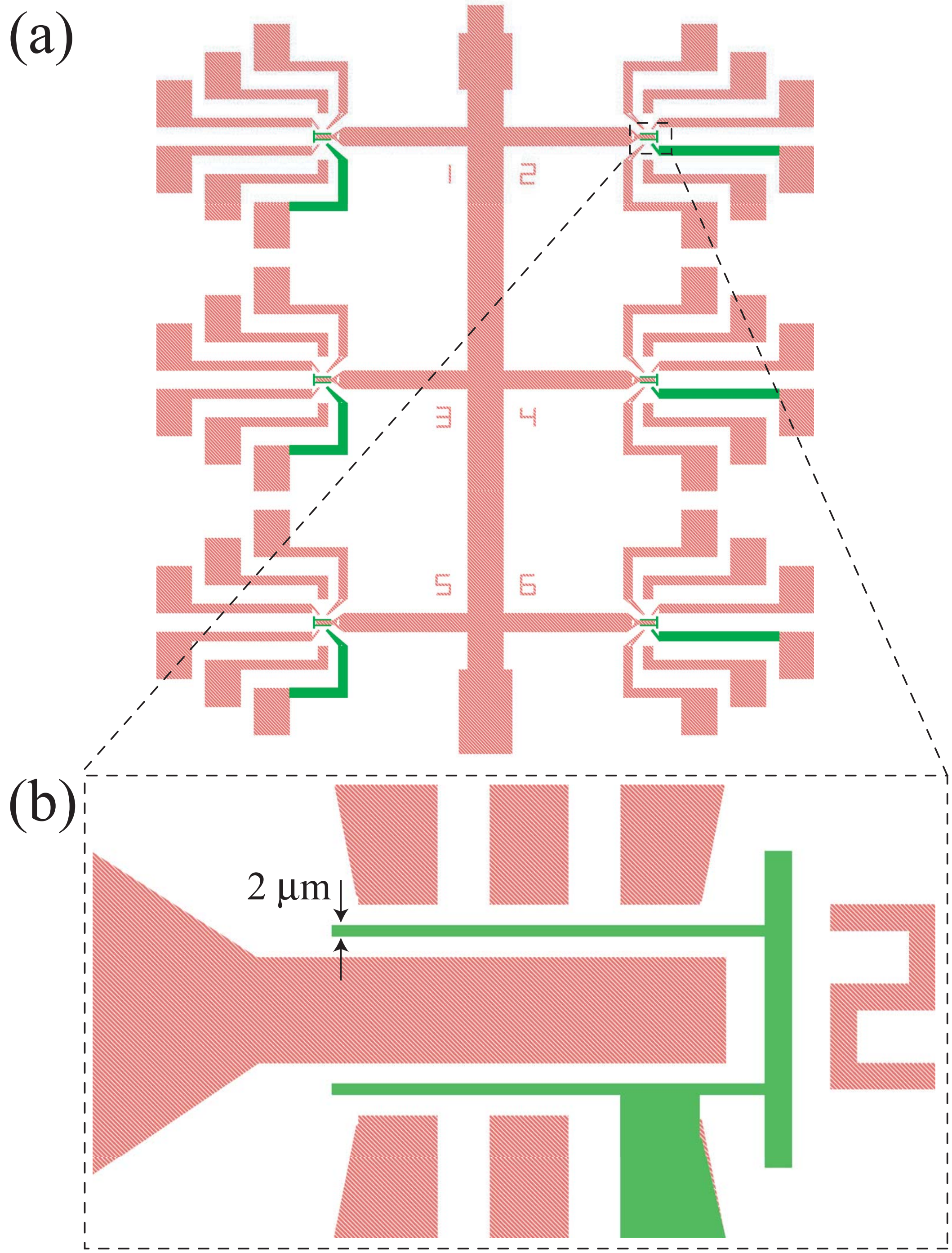

Figure 2.11: (a) View of the aluminum gate mask. The gates are shown in green and the overlay with the gold contact layers (not on the mask) is shown in red (b) Magnified view

microscope. I then develop in additional steps of 15 seconds each till development is completed. After completing the photolithography, the evaporation process is:

1. Clamp the wafer down well onto the 4-inch evaporator stage with the pot. Use 6-8 screws for good contact.
2. After pumping out the chamber and degassing the sources, cool the pot with liquid nitrogen. It takes about 20 minutes to cool it down below 85 K.
3. Evaporate 160 Å of aluminum. A 20 Å sticking layer of titanium is optional. If you do use the titanium, use the e-gun for both sources so the shadows overlap on the wafer.
4. Warm up the stage to room temperature using compressed air. It takes about one hour to warm up.

The gate insulator for the aluminum oxide gates is the film of native oxide that forms on the surface when the aluminum gate is exposed to air. It may be possible to form a thicker or better oxide by using a stream of pure oxygen, or using plasma oxidation. I have not experimented with this.

Evaporating the aluminum at low temperature produces smoother films. The gates were not good (leaked heavily) the one time we tried it without the cooling. However, further studies need to be done before deciding that the process will not work at room temperature.

After evaporation, liftoff the resist in acetone. In most cases, the resist would have cracked at low temperature, leading to a pattern of streaks of aluminum on the wafer. The streaks usually cause severe gate leakage. In order to check this, probe the leakage current between the common electrode and several gate electrodes. If I find that <10% of the gates are leaking, I skip the next step.

2.3.6 Aluminum streak etch

If after the deposition of the aluminum electrode I find that over 10% of the gates leak to the common electrode, I remove the streaks causing this leakage. The process is:

1. Prime, spin coat and bake the wafer as in sec. 2.1.2.
2. Expose the wafer on the 10X stepper using the mask shown in fig. 2.11.
3. Develop the wafer in MIF300 for 60-90 seconds. Rinse in water.
4. Aluminum is etched fairly quickly by the developer (MIF300). In case the streaks are not gone after developing the wafer, you can use Aluminum etchant (type A, which does not attack silicon oxide) to remove the remaining streaks.
5. If you used titanium as a sticking layer for the gate electrode, streaks of titanium will still remain on the wafer. If this is causing electrical shorts, you will want to get rid of it. Unfortunately, all the conventional titanium etchants (such as HF) also etch silicon oxide. Radek found that hydrochloric acid etches titanium slowly but does not attack silicon oxide.
6. Remove the resist with S1165 remover, followed by acetone and IPA.

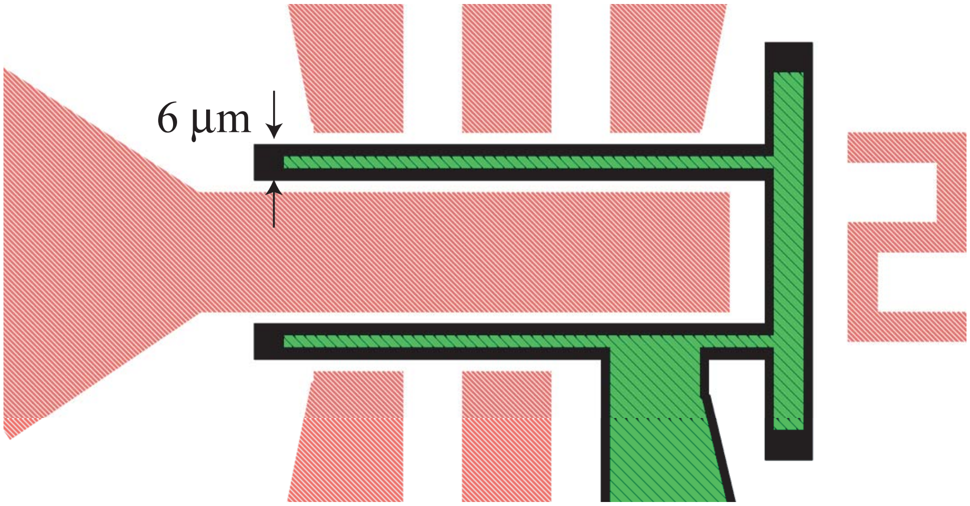

Figure 2.12: View of a part of the aluminum streak etch mask. The mask area (black) covers the gate (green) with a 2 *mu*m margin on either side. The gold contacts are shown in red. A full view of the mask looks like fig. 2.11(a).

2.3.7 E-beam nanowire

We now need to lay our nanowire across the aluminum gate in order to complete the fabrication process. However, since the nanowire is typically about the same thickness as the aluminum gate electrode, getting good metal coverage across the step caused by the gate electrode can be a problem. In order to avoid this problem, the nanowire is created in two steps. The first of these steps uses a pattern as shown in fig. 2.13. It is created by electron-beam lithography as in sec. 2.1.5.

2.3.8 E-beam contacts

The next step is to make contact to the nanowires created in sec. 2.3.7. This is also done using electron-beam lithography as in sec. 2.1.5. A typical pattern is shown in fig. 2.13. I use 20 Å of titanium followed by 300 Å of gold to make good electrical contact.

2.3.9 Dicing

This is performed as in sec. 2.1.6.

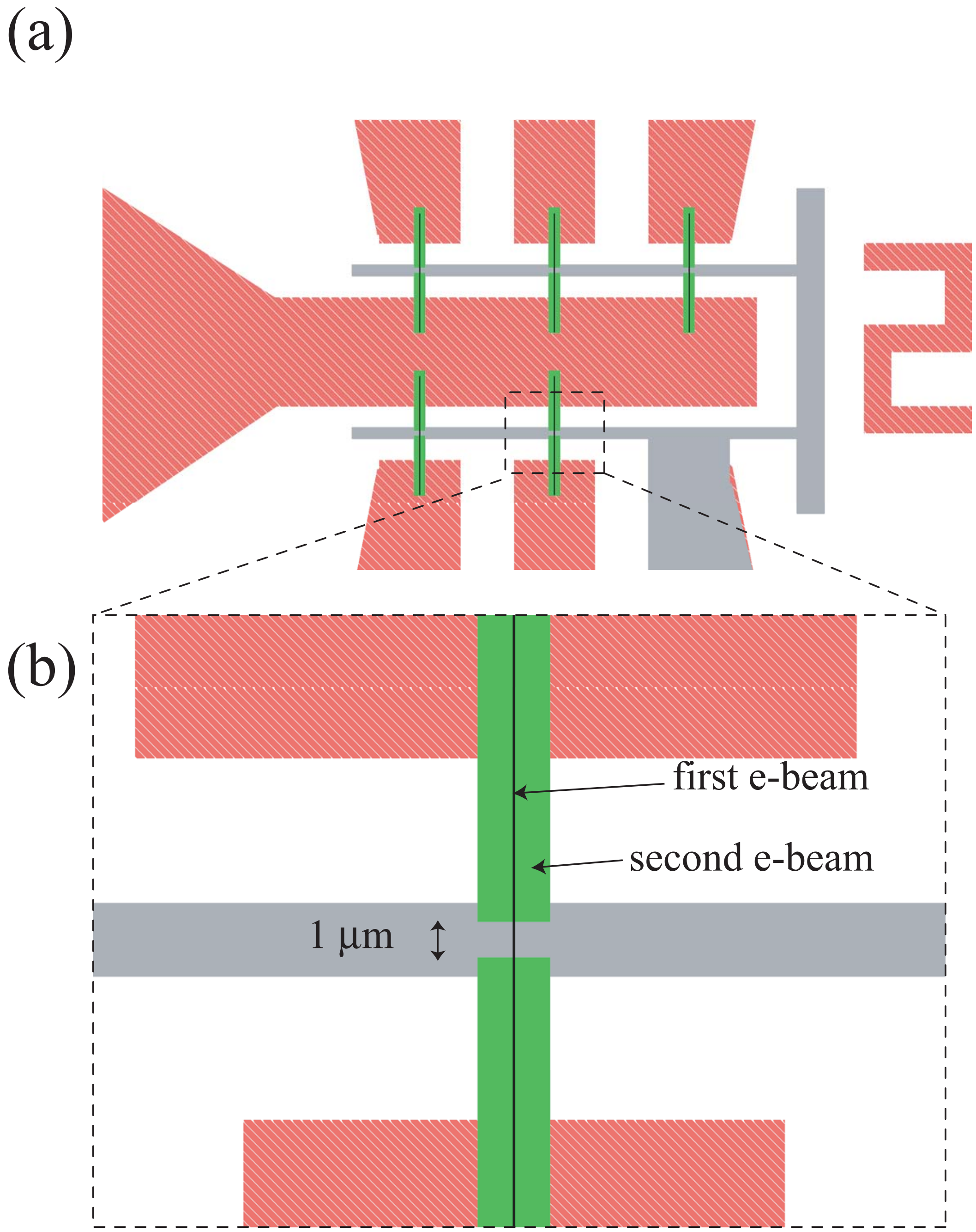

Figure 2.13: Two-step e-beam lithography pattern. (a) Die view. The first e-beam layer is shown in black (a single pass line) and the second layer is shown in green. (b) Magnified view.

Bibliography

[1] Jiwoong Park showed me how the silicon-gated sample fabrication was done at Berkeley. I have used the same design.

[2] In this process, the wafer is soaked in chlorobenzene for 10 minutes before or after exposure. No image reversal is done.

[3] In this process, the wafer is soaked in toluene for 1-2 minutes after exposure and then baked at 90 °C for 1 minute. No image reversal is done.

[4] I send my wafers to Larry Stogner of Micro Precision equipment, Inc. (Greenville TX). See www.micrope.com.

[5] S. H. M. Persson, L. Olofsson, and L. Gunnarsson, Appl. Phys. Lett. **74**, 2546 (1999).

[6] W. Liang et al., Nature **417**, 725 (2002).

Chapter 3

Electromigration: making good samples

In the previous chapter, I described how we fabricate nanowires at the CNF. In this chapter, I will describe how we go from these nanowires to a "good" sample - the kind that is described in chapters 4 - 7. I will start by discussing how we mount and cool down our nanowires in a cryostat (section 3.1). I will then describe the electromigration procedure we use to create two-closely spaced electrodes (section 3.2). It is important to identify artifacts in the measurements (and there are plenty of them). I will describe control experiments that we can use to distinguish between "good" and "bad" data in section 3.3. Finally, in the (unlikely) event that we actually have a good sample, it is important to do the measurement correctly in order to collect good data. I will describe the measurement techniques that we use in section 3.4.

3.1 Cooling down samples

Most of the measurements done by me have been performed at low temperatures (below 77 K). The cryostats we use all have sample holders that accept 28-pin chip carriers [1]. All the cryostats have 24 of these 28 pins wired up to a switchbox with BNC connectors, although the wiring for each cryostat is unique (this gives you a good opportunity to curse the person who did the wiring). The first job is to get a chip mounted and electrically connected to the chip carrier. The trick to doing this successfully (without killing all your samples) is leaving your favorite fleece jacket at home.

Start by probing the nanowires and discard the ones already broken. Check the leakage current on the gates. A good aluminum gate will have <10 pA leakage up to 2 V. The 30 nm SiO_2 gate oxide should be good to about 20 V. Once you have decided on which gates and wires to use, attach the chip to the chip carrier. If you use a silicon-gated chip, you have to be able to make electrical contact to the back surface of the wafer. This is easily done with silver paint. Place a drop of silver paste on a glass slide and stir till it is sufficiently gooey. Using a sharpened Q-tip, put a drop on the chip socket. Place the chip on the paste, press and heat at 50 °C for 5 minutes. Remember to push the chip to one side of the carrier so you can wirebond to the bottom of the carrier.

If you are using an aluminum-gated chip, you can use superglue instead of silver paste to stick the chip to the carrier. Superglue is easier to dispense (no stirring) and makes stronger bonds.

Once the chip is ready, mount it into the wirebond holder, and ground yourself to the holder. If you are paranoid (I am) either wear no gloves or wear conducting gloves. After wirebonding, you can either pull the chip out of the wirebond holder and place it in a gel-pak, or take the wirebond holder to the cryostat. I prefer the latter, but both methods seem to work. After grounding everything in sight, place the chip carrier into the sample holder on the cryostat. Everybody has their own theory for how to do this correctly, so I will not bother you with mine.

Once your sample is in the cryostat's holder, it is time to cool it down. I have used several different cryostats to cool samples down:

1. Dipstick in a helium dewar: Just toss it in LN_2 and then into the dewar. You cannot go wrong.
2. The Desert Cryogenics "dipstick": Alex Champagne should be consulted about this.
3. Oxford Variable Temperature Insert ("VTI"): Since it takes $\approx$ 1.5 hours to warm the insert up from base temperature, it is useful to check and see that your samples are good at room temperature before cooling them down. This is easily done by applying a 5 mV bias to your sample and measuring the current. Samples do not usually die while cooling down.
4. Oxford ^{3}He one-shot fridge: this cryostat was resurrected by Jacob, Radek and I but it is best not to use it unless one is forced to. Consult Jacob about this.
5. Oxford Top-loading 200 μW dilution fridge: it takes about three hours to cool down a sample and an hour to warm it up. Like the VTI, you must check your samples at room temperature or you might curse needlessly.

I have not described the operation or maintenance of the cryostats used. These are best learned by experience.

3.2 Electromigration procedure

Once your nanowires are cold, the next job is to blow them up so you can create pairs of closely-spaced electrodes. The overall procedure is described well by

Hongkun Park *et. al.* [2]. I will briefly describe the procedure and a few tips for doing it right.

The electromigration procedure is summarized in fig. 3.1. The voltage across the ends of the nanowire is ramped up slowly in time (typical rates are 10-30 mV/s). The current initially increases linearly with voltage. Beyond point A in fig. 3.1 the resistance increases with voltage. Since this resistance increase is reversible, it probably comes from additional scattering mechanisms that can be accessed at higher energies (phonons, defects, etc). Beyond point B the resistance once again decreases. This change is irreversible and is likely due to melting of parts of the wire. Finally, at point C, the resistance of the wire increases rapidly due to electromigration. One amusing fact confirms that electromigration is really responsible for the failure of the wire rather than just melting. When a wire is imaged after it is broken (fig. 3.2(b)), the break is seen to happen always closer to the side connected to the lower potential of the voltage source [3]. Many times, a chunk of gold that has been deposited by the electron "wind" can be seen on the side connected to the positive terminal.

What is the end result after electromigration? It would be extremely informative to have atomic scale imaging of the electrodes after the electromigration procedure is carried out. The only technique that currently has the resolution required to give us this kind of information is transmission electron microscopy (TEM). To be able to perform TEM, the wire has to be on a substrate that is transparent to electrons. We have fabricated nanowires on a transparent silicon nitride membrane in order to do imaging with the TEM. Unfortunately, we found that the nanowires do not electromigrate the same way on a thin silicon nitride

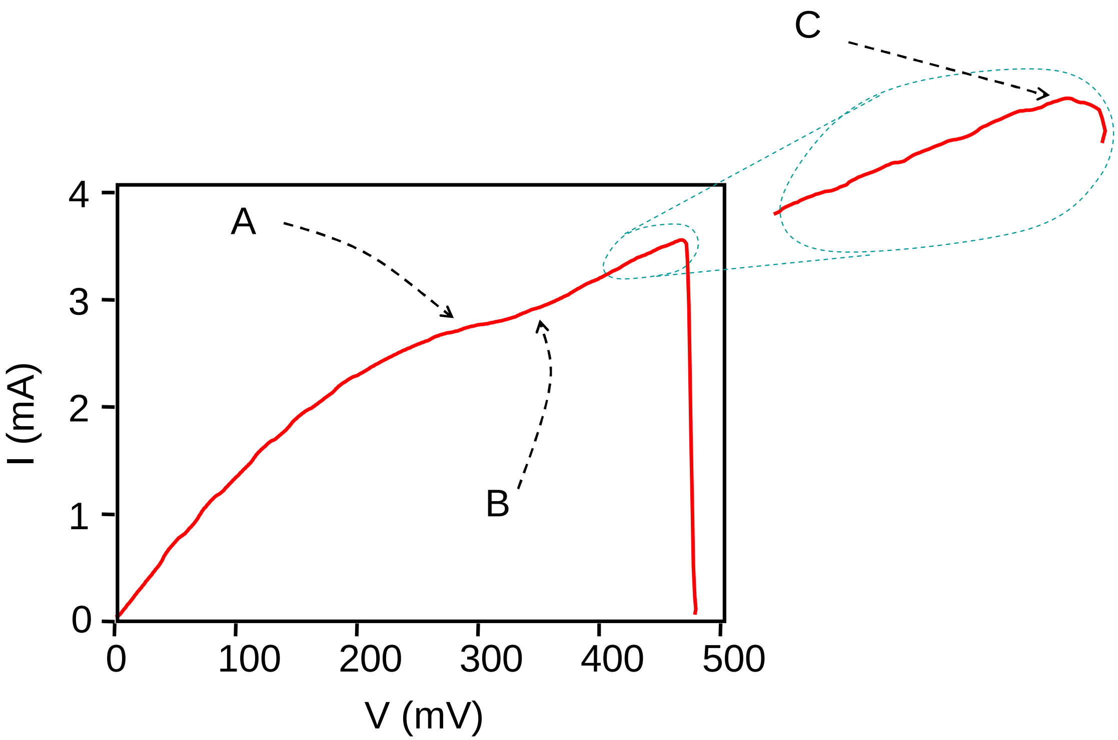

Figure 3.1: I vs. V for a nanowire during the electromigration procedure.

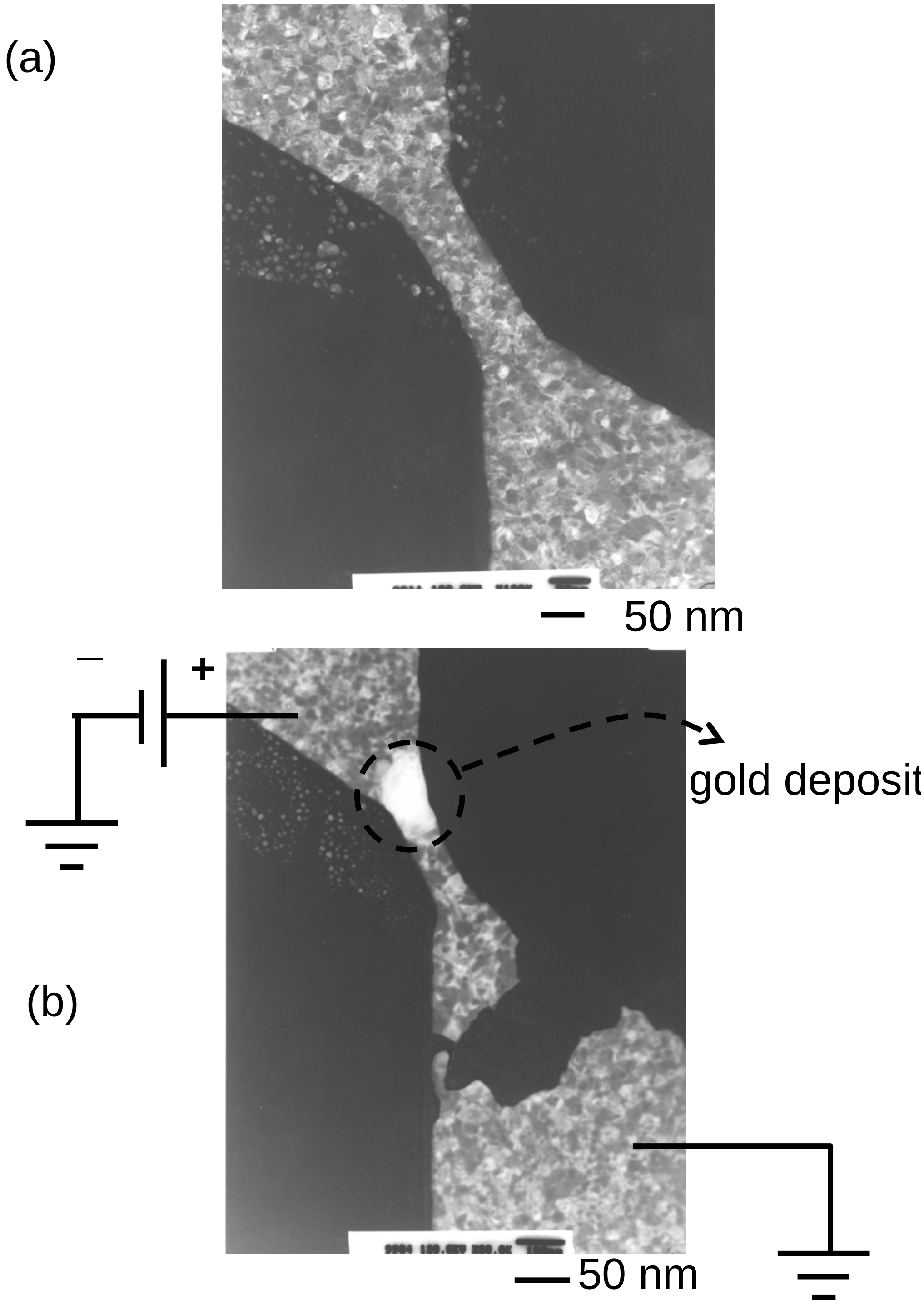

Figure 3.2: TEM pictures of nanowires. (a) unbroken nanowire. (b) broken nanowire, showing that the breaking point occurs closer to the cathode.

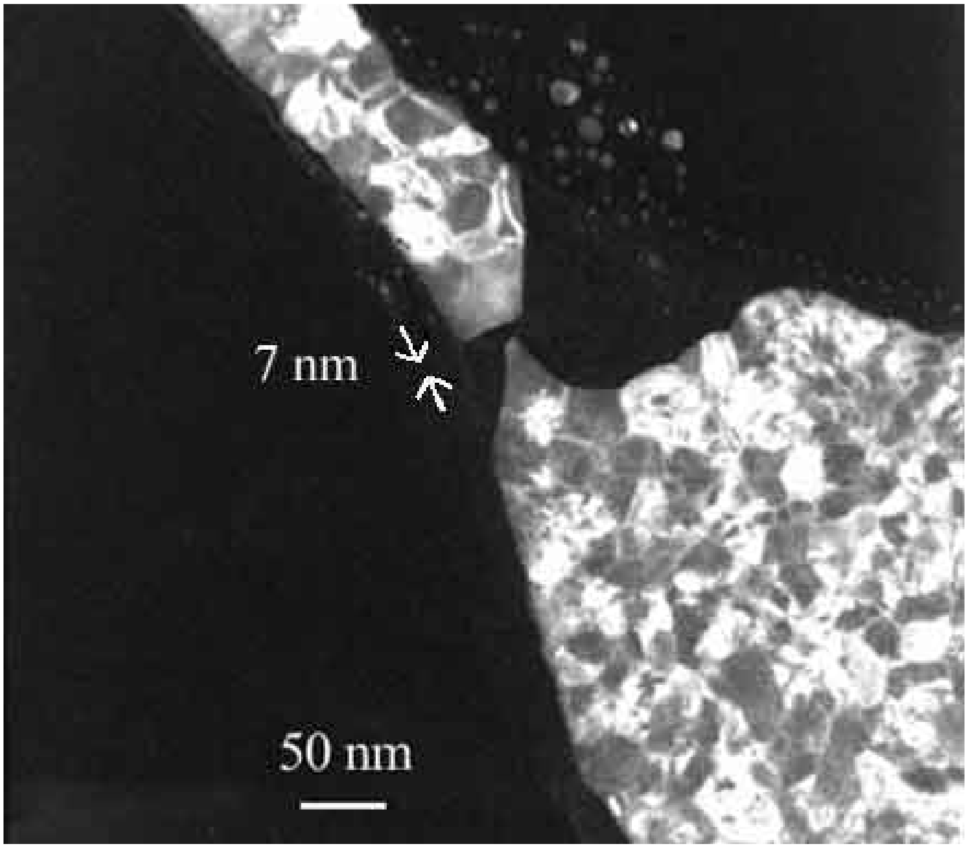

Figure 3.3: TEM picture of a nanowire that has undergone the electromigration procedure on a thin silicon nitride substrate.

substrate as they do on the thick substrates we normally use. In particular, the wires broke when much higher voltages (1-1.5 V) were applied across them and the resulting gaps between the electrodes were much larger. Shown in fig. 3.3 is a broken wire on a silicon nitride membrane that has been imaged by TEM. The gap is about 7 nm. While this gap is too large for the molecules we study, such junctions might be useful for the nanoparticle experiments that Kirill and Ferdinand are doing currently. Another difference is that these junctions were created at room temperature. Repeating the experiment at low temperature might produce different results.

Given the lack of imaging information on our wires, our best characterization tool is the resistance of the wires after the electromigration procedure. Shown in fig. 3.4 (taken from [2]) are the resistances of 400 wires measured after the electromigration process. If we assume that the structure of the electrodes is a simple tunnel junction, we can convert the resistances to an estimate for the distance using the tunneling formula in eqn. 1.3. This formula states that the resistance increases by about an order of magnitude per angstrom increase in separation between the electrodes. The unknown in this formula is the area over which the tunneling occurs. If we assume that contacts having a resistance equal to the resistance quantum (13 kΩ) correspond to a single-atom gold contact, we get typical gap sizes of 0.5 - 1 nm from the resistance values. These values are however highly dependent on several parameters like the nature of the metal deposited and the rate at which the voltage is ramped. While no thorough studies have been performed by me relating gap sizes to these various parameters, the following tips might be useful while performing the electromigration procedure.

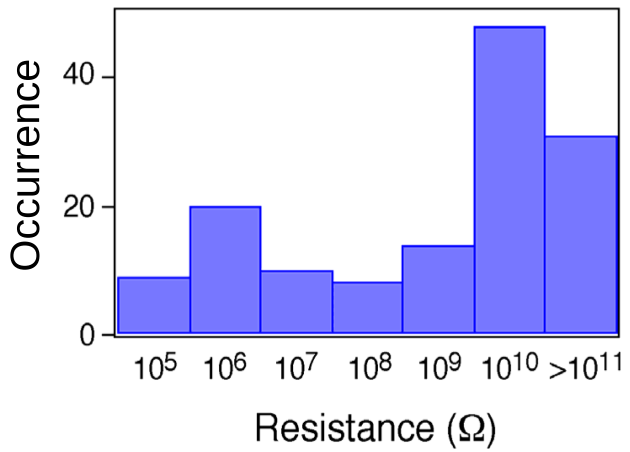

Figure 3.4: A histogram of tunnel resistances of wires broken by electromigration, from [2]

1. The lead resistance should be minimized to get smallest gaps. If the lead has a resistance R_L and the wire a low-bias resistance R_S, the voltage that the wire sees across its ends is $V_S = V\frac{R_S}{R_S+R_L}$ instead of the voltage V applied by the source. When the wire fails however, $R_S >> R_L$ and the entire voltage drop falls across the wire. This sudden change in voltage in general causes larger gaps to form. It is therefore necessary to have a low lead resistance (typically less than 10 Ω) to be able to do the electromigration procedure properly. This means, for example, that conventional manganin wiring in the dilution fridge is unsuitable for the experiment. We had a probe made with low-resistance copper wiring down to the 1 K region and pure superconducting wire down to the mixing chamber (to cut heat conduction) in order to be able to do the electromigration procedure in the dilution fridge.

2. The nanowires can be "re-broken" to increase their resistance. Quite often, after the first break is made in the wire, there could be multiple conduction paths between the electrodes. By taking the junction out to higher bias than what was applied previously, you can change cause atomic rearrangements to happen. Usually such rearrangements lead to an increase in resistance, but sometimes the resistance can also drop. The maximum voltage that you can subject these junctions to is determined by the strength of the gate dielectric (typically 2 V for native aluminum oxide). Of course, if you apply more than about 3 V to the junction, you will cause sufficiently large gaps so that no tunnel current can be measured. Once this happens, the junction is useless.

3. You can "slowly" break nanowires to get low resistances. Many times, when the nanowire is initially broken, single-atom contacts are formed (or tunnel

junctions with resistances in the tens of kΩ's). These kind of resistances are required in order to see Kondo-assisted tunneling for example. Unfortunately, these low resistance contacts are usually not very stable at the voltages at which the wire initially breaks (0.5 - 1 V). In this case, a trick can be employed to force them to break at slightly lower voltages. It depends on two properties of the electromigration process.

(a) There is a region of applied voltage (just before point C in fig. 3.1) where the resistance of the wire continues to increase even though the voltage bias is held constant (this is the analogue of the plastic flow region when a material is strained beyond its yield point). A neck develops in the wire, and the current density increases at the neck.

(b) It is known from studies of interconnects in integrated circuits that electromigration is an activated process. The mean time for failure of a wire can be phenomenologically related to the current density j through the wire by means of Black's law [4, 5]

$$MFT = A\frac{1}{j^n}e^{E_a/kT}. \tag{3.1}$$

Typical values for gold in earlier studies [6] are $n = 2$ and $E_a = 1$ eV.

These points together give us a way to "slowly" break nanowires. First ramp the voltage to a point where plastic flow just begins, but the mean time for failure is still fairly large (several seconds). As the resistance increases, slowly decrease the voltage, while keeping the current density high enough that plastic flow is still occurring. Eventually, the wire will fail, but at a lower voltage than it would without this procedure (as demonstrated in fig. 3.5). This procedure is not necessary always - some wafers break to point contacts that are fairly robust up to 0.7 V or so (for reasons unknown to me).

3.3 Control experiments

It is clear that the method we use to create closely-spaced electrodes is uncontrolled. It is unfortunate that we also do not have any method of imaging the "device" that we believe consists of a single molecule attached to two electrodes. In this situation, it is essential that we do some control experiments to make sure that the transport properties are really due to the molecule that we want to study.

The control experiments I do are fairly straightforward. They consist of doing transport measurements on samples that undergo all the treatments that the "good" devices receive, except that no molecules are deposited on the chip. Our molecules are usually placed in a solvent and deposited on the chip. So to do a control experiment, the chip is cleaned and then exposed to the same solvent. It is then cooled to low temperature, the electromigration procedure is performed, and then transport measurements are taken.

Ideally, we would expect only simple tunnel junctions from the samples that have gone through the electromigration procedure without any molecule deposition. The I-V curves should follow eqn. 1.1. Nature is not this kind to us however - we see a fair amount of junk in our measurements.

One simple kind of artifact that we often see is an asymmetric I-V curve, as shown in fig. 3.6. The tunnel model of Simmons, eqn. 1.1 predicts a symmetric

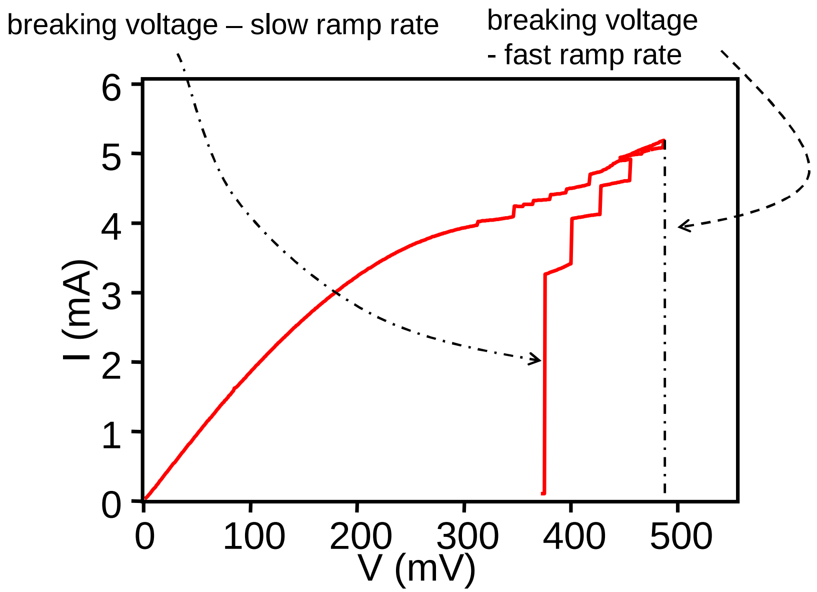

Figure 3.5: I vs. V for a nanowire during the electromigration procedure - the voltage is monitored and minimized during the breaking process.

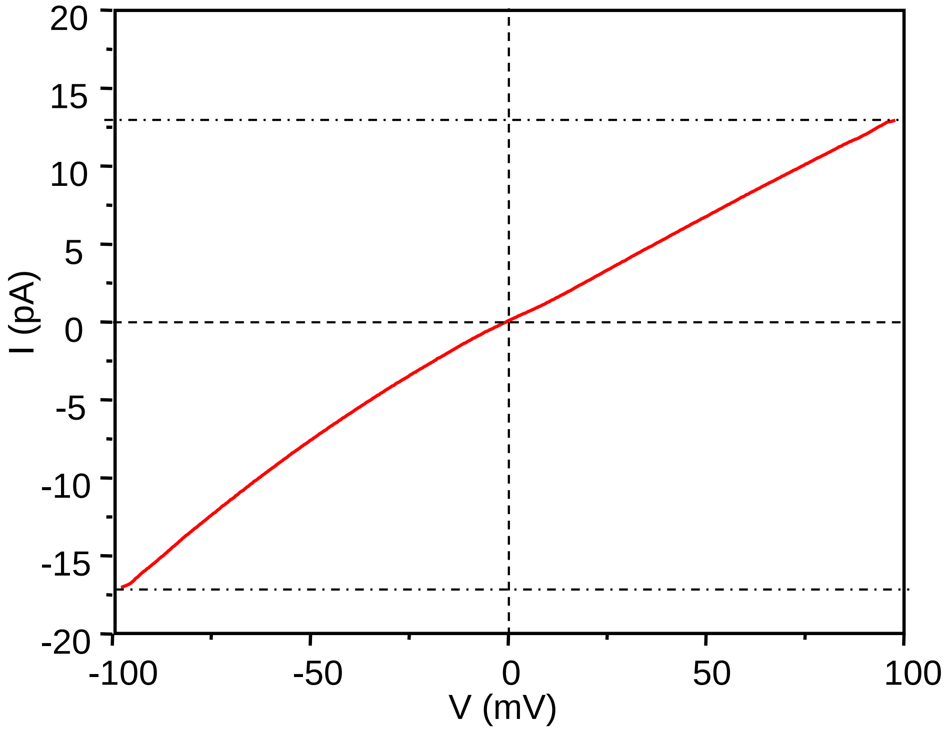

Figure 3.6: An asymmetric tunnel junction formed between gold electrodes.

I-*V* curve. Asymmetry in the *I*-*V* curve can come from anything that makes the two electrodes asymmetric, such as:

1. Differences in the workfunction of the two electrodes. It is well known that the workfunction of a metal at the surface is modified strongly by the geometry of atoms at the surface. Thus the two electrodes can have different workfunctions, resulting in asymmetric *I*-*V* curves [7].
2. Differences in image charge distribution. The image charge of a tunneling electron lowers the barrier faced by the tunneling electron [8]. If the geometry of the electrodes is asymmetric, the image charge distribution and hence the conductance will also be asymmetric in bias voltage.
3. Impurities in the barrier. The presence of impurities in the barrier will strongly affect the barrier height, resulting in asymmetric *I*-*V* curves. Such impurities can exist either in the metal nanowire, or if there is a sticking layer present (typically Cr or Ti), or by the inclusion of organic impurities into the tunnel barrier (such as resist). Since the wire is broken at low temperatures, there should not be any oxide formation at the junction.

The asymmetries that we see in *I*-*V* curves become more pronounced at higher bias. In fact, beyond about 300 mV of applied bias, the *I*-*V* curves usually are extremely asymmetric, as well as irreproducible. The irreproducibility comes from the fact that we can physically move gold ions at high applied voltages [9].

Another kind of artifact seen especially in bare gold wires is *I*-*V* curves that somewhat resemble Coulomb blockade. A typical *I*-*V* curve is shown in fig. 3.7

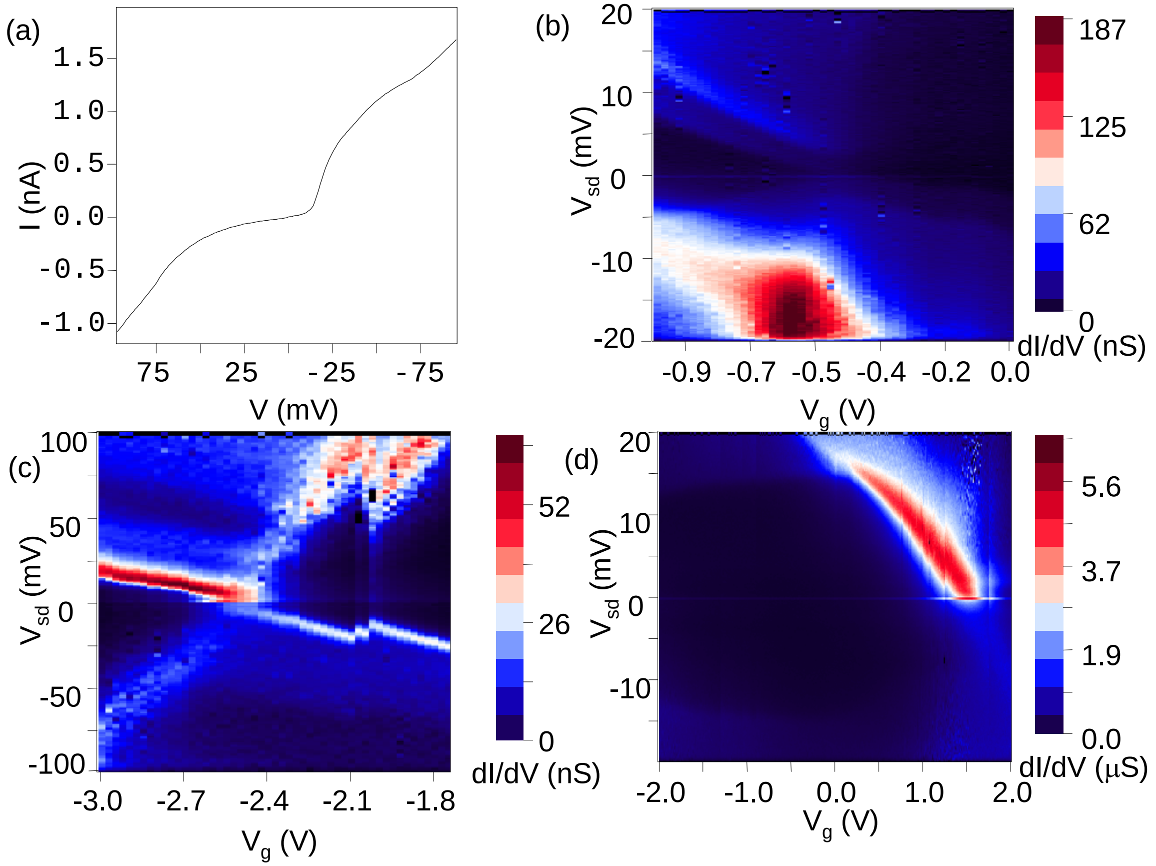

Figure 3.7: Artifacts from thin (10 nm) gold wires. (a) *I*-*V* (b),(c) and (d) dI/dV plots as a function of gate (x-axis) and bias (y-axis) voltage.

(a). These *I*-*V* features can even be gate-voltage dependent, as shown in fig. 3.7 (b)-(d). These features are rather troubling, since they are typically the kind of features we expect from the molecules we are studying. I believe that a major reason for such features is the graininess of gold. Shown in fig. 3.8 is the typical grain structure of one of our nanowires. The typical grain size is about 10 nm. This implies that oftentimes, a single grain can be left at the tip of an electrode created after electromigration, as shown in fig. 3.8. If the coupling between the grain at the tip and the rest of the electrode is sufficiently weak, this can result in Coulomb blockade characteristics. This conclusion is also supported by the fact that we usually see fairly weak gate-voltage dependence, as we would expect if the grain is fairly strongly coupled to one electrode. I have also not seen this problem for electrodes made from Ni, Co or Al, probably because they form smaller grains. I have seen the same problem for Pt electrodes.

How do we get past this problem? One way in which this problem can be minimized is to use reasonably thick gold electrodes (at least 16 nm, preferably over 20 nm). We once used 10 nm thick gold electrodes in an effort to have the molecules as close to the gate electrode as possible. The results were disastrous - nearly every wire showed Coulomb-blockade like characteristics. It is also prudent to discard wafers in which such features appear frequently. My rule of thumb is to discard any wafer that has more than 2 wires per chip showing such features below 50 mV bias voltage.

Another test is to look for “positive controls”. This implies making statistics of the number of times blockade-like features are seen from the molecule as against bare gold wires. Another good test is to see how the wires break in the presence

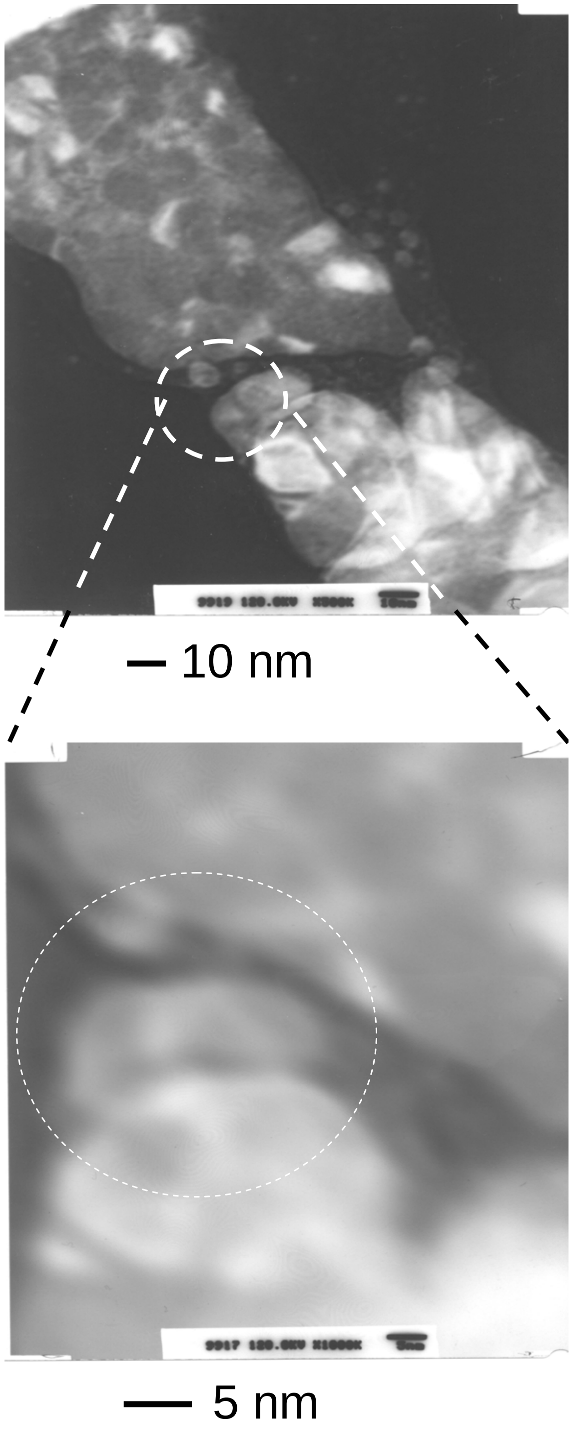

Figure 3.8: TEM picture of the grain structure of our gold wires. (Zoom-in) Sometimes a gold grain at the tip can be weakly coupled to the rest of the electrode.

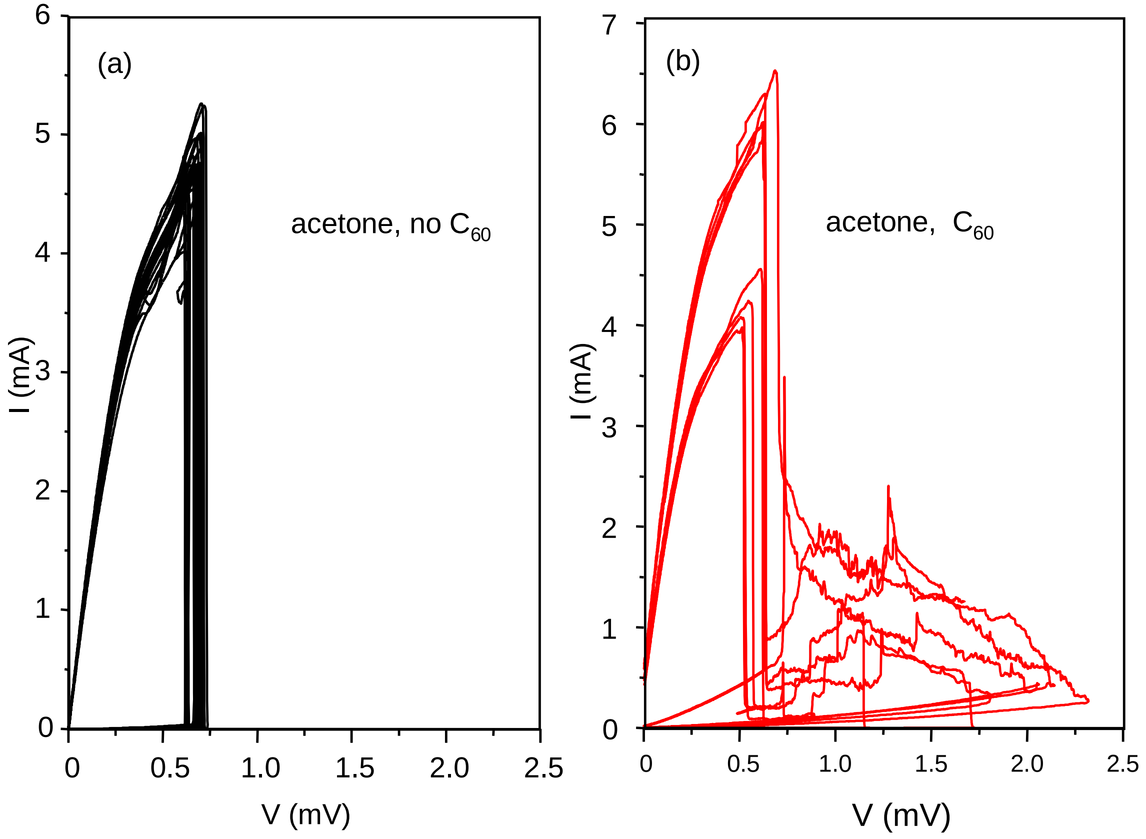

Figure 3.9: Breaking traces of chips without (a) and with (b) adsorbed C_{60} molecules.

and in the absence of molecules. Shown in fig. 3.9(a) is a series of 20 bare gold wires broken by electromigration. This is to be contrasted with fig. 3.9(b) which shows breaking traces of 20 wires that have adsorbed molecules (in this case C_{60}) on them. The wires with adsorbed C_{60} have much larger conductance after breaking signifying that the C_{60} is indeed included in the junction.

A phenomenon closely related to Coulomb blockade in quantum dots is the Kondo effect. The Kondo effect as it appears in quantum dots is described in chapter 5. It appears when at least one of the contacts between the quantum dot and the electrodes has a conductance comparable to $G_0 = 2e^2/h$. It shows up in $dI/dV - V$ curves as a peak at $V = 0$. We have seen such signals from our control samples in the case of gold wires (fig. 3.10). As in the case of Coulomb blockade, the culprit is quite likely to be a gold grain at the tip of an electrode, since it is very likely to be well coupled to the electrode. Glazman *et. al.* [10] have shown theoretically that a quantum dot that has a high density of available electronic energy levels will exhibit a Kondo effect similar to that shown by a single-level quantum dot with an enhanced Kondo temperature.

3.4 Measurements

Once we have a good sample, it is important to be able to take good measurements. In particular, this means minimizing the noise on the electrical lines going down into the cryostat, by filtering it out. Electrical noise is particularly a problem on the dilution fridge, since it reaches the lowest temperatures. Our electrical lines have three filters on the way down into the dilution fridge. Mounted in the mixing

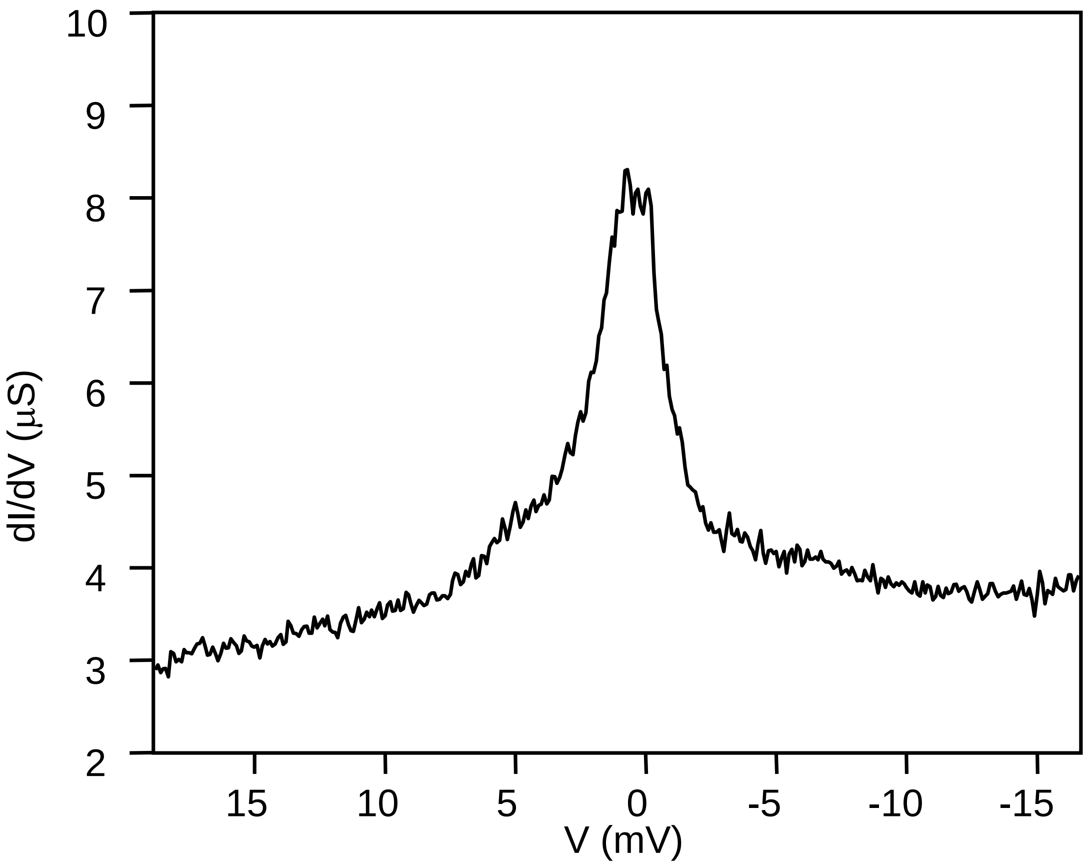

Figure 3.10: dI/dV peak at $V = 0$ from a bare gold (10 nm thick) junction.

chamber are copper powder filters that work by the skin effect. We have found that they are useful at cutting off noise above 100 MHz. The lines travel up through the cryostat and into a breakout box with BNC connectors. To this is attached a "Pi" filter for each line with a cutoff frequency of about 100 kHz. Above this is a low-pass RC filter with a cutoff of about 1 Hz.

The measurement schematic we use is shown in fig. 3.11(a). The voltages we use are supplied by HP3325A function generators, with a typical noise level of 10 μV rms. The voltage is recorded by feeding the voltage output into a PAR113 voltage preamplifier whose output goes into the computer DAC. The current is measured by an Ithaco 1211 current preamp, with a noise floor of about 10 fA when measured at 1 Hz. The output is fed directly into the computer DAC. For low resistance measurements (less than 1 MΩ), we alternatively use a lock-in arrangement to measure the differential conductance. We use a PAR124 lock-in with an excitation of 5 μV at 3 Hz. The current is converted to voltage by means of the Ithaco 1211, whose output is fed into the lock-in. DC bias can be applied across the sample most conveniently by using a voltage divider, as shown in fig. 3.11(b).

I can think of a number of improvements that can be made to the current setup to improve on the noise level:

1. Using twisted pair wiring. The current design does not allow us to use twisted-pair wiring. This is because all the samples have a common ground. Moving over to twisted-pairs would therefore mean a significant reduction in the number of samples that can be cooled in one run.

2. Improving the breakout box. The breakout box is currently very poorly

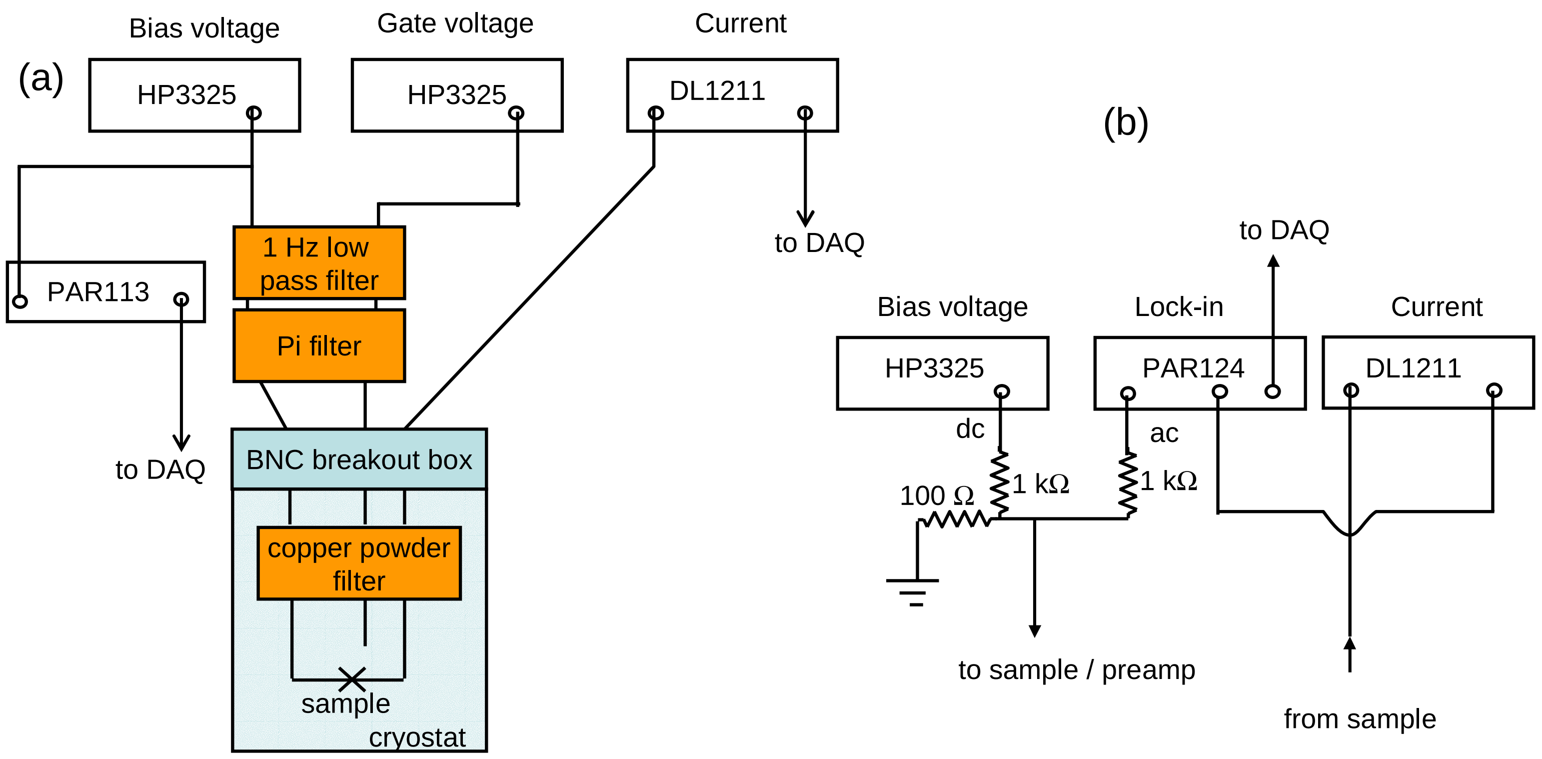

Figure 3.11: (a) Measurement setup for DC measurements. (b) Illustrating the use of a lock-in amplifier for dI/dV measurements.

designed. It consists of signal wires going through the various switches to the BNC connectors, without any shielding along the way. The best solution would be to have twisted pairs within the box which are also shielded. The current design is very susceptible to magnetic 60 Hz pickup.

3. Mu metal shielding. Magnetic 60 Hz pickup can be minimized by covering the upper 3 feet of the probe (that stick out of the cryostat) with mu metal. The little boxes that we make to go from BNC to triax connectors can also be similarly shielded.

4. Low temperature voltage divider. We can use a low temperature voltage divider to reduce noise on the bias voltage. This might be difficult to do if we also want to break wires at low temperature, since we need to minimize the series resistance.

5. A low temperature current preamplifier. We could significantly reduce the current noise by reducing the length of wire between the sample and the current preamp. I have heard that silicon-based FET preamps do not work at cryogenic temperatures [11]. GaAs FETs do work, but they are reputed to be fairly noisy below about 100 kHz. I have not however looked into this matter myself.

3.5 Measuring samples quickly

We typically go through a lot of samples before finding a good device. To speed up this process a little, I automated the procedure for electromigration and preliminary measurements on samples by electronically switching between samples.

Since our samples have resistances that go up to the GΩ range, it is essential that our electronic switch not have a leakage resistance smaller than a few hundred GΩ. The usual FET switches will not work for this purpose. I have used reed-relay switches instead [12], which have a leakage resistance greater than a TΩ. The reed relays are in turn switched using an FET demultiplexer [13]. The problem with the reed relays is that they tend to "ring" when they are switched quickly (using the bare demultiplexer signal). This results in a 100 MHz voltage signal that can be as large as 1 V. In order to get rid of this, I have sent the output of the demultiplexer through a low pass filter (1000 μF, 50 Ohms). The switching circuit for one board (8 lines) is shown in fig. 3.12. The low pass filter is conveniently made using surface-mount components [14].

I have made the boards by patterning double-sided copper-coated printed circuit boards using photolithography. I use S1813 as the resist. I print out the pattern on transparencies. It is fairly easy to do alignment between the front and back sides of the board just using a few dots outside the board area (the alignment is good to a few hundred microns). I expose for about 30 seconds on the HTG (the transparencies absorb a fair amount of UV necessitating the long exposure). Develop in MIF300 for 2 minutes. To etch the copper, use ferric chloride solution. The stuff called "copper etchant type A" is ferric chloride, but is very dilute for the present purpose. You can add some more ferric chloride solid to it (making the final solution at least 1:3 in water by weight). Heat up the mix to about 60 °C to speed up the etching. It takes about 10 minutes to etch a board.

I originally made these boards because I was worried that custom-made boards from commercial vendors would leak (they are typically guaranteed to 100 MΩ).

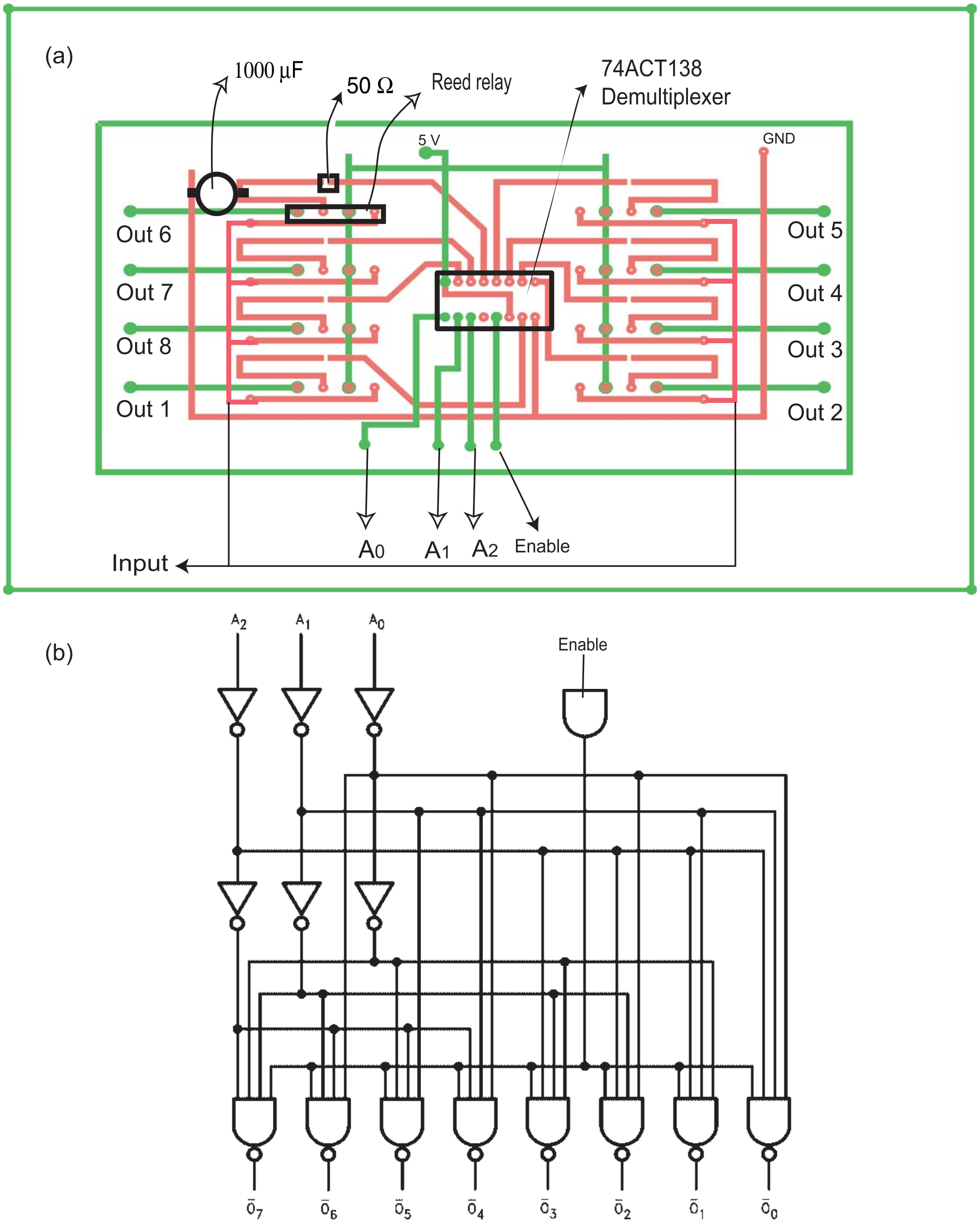

Figure 3.12: (a) A single board of the electronic switchbox that switches between eight outputs. The green and red patterns are on opposite sides. Alignment is done by eye using the two outer rectangles. (b) Demux switching logic.

However, I have since tested a couple of commercial boards and found the leakage low enough (greater than 100 GΩ).

I have made four boards that switch between 8 samples each. Three of the inputs are wired together and are used to switch the bias voltage between a maximum of 24 samples. The fourth board switches the gate voltage between one of 8 different gates. Each of the demultiplexers uses three control and two enable lines. One of the enable lines is always on (wired to 5 V). We therefore need 3 enable lines for the three boards plus 3 control lines that are common to the three boards to switch between the 24 outputs. I use the outputs of the printer parallel port to perform this function. The LPT1 port has only 8 outputs, so the 4 outputs required to control the gate demux come from the digital output lines (DIO) lines of the DAC card. The switching logic is shown in fig. 3.13.

In order to use the box, I have made several modifications to the software used to take advantage of the box [15]. Provision has been made to automatically break a wire. This is done by ramping up the voltage until the current falls below a preset value, and then ramping down the voltage to zero. I have also incorporated an "automatic" measurement, where the voltage is ramped quickly down to the starting (negative) voltage, then ramped up slowly to the ending (positive) voltage while recording the current, and finally ramping it quickly back down to zero.

Using the two basic functions described above, I have built up an automatic measurement sequence. This is done by calling up a file that has a sequence of commands in a primitive scripting language [16]. Thus, for example, wires 1,2 and 6 can be broken by the command lines "b 1 b 2 b 6". Commands to automatically break wires, do I-V measurements, open and close a given gate line and to set a

Source voltage switching
via LPT1 (printer port)

enable pins on demux: pin 4, pin 5, pin 6

control pins (A0,A1, A2)
on demux: pin 1, pin 2, pin 3

pin 1	pin 2	pin 3	pin 4	pin 5	pin 6	O/p
X	X	X	H	H	H	X
H	H	H	L	H	H	1
L	H	H	L	H	H	2
H	L	H	L	H	H	3
L	L	H	L	H	H	4
H	H	L	L	H	H	5
L	H	L	L	H	H	6
H	L	L	L	H	H	7
L	L	L	L	H	H	8
H	H	H	H	L	H	9
L	H	H	H	L	H	10
H	L	H	H	L	H	11
L	L	H	H	L	H	12
H	H	L	H	L	H	13
L	H	L	H	L	H	14
H	L	L	H	L	H	15
L	L	L	H	L	H	16
H	H	H	H	H	L	17
L	H	H	H	H	L	18
H	L	H	H	H	L	19
L	L	H	H	H	L	20
H	H	L	H	H	L	21
L	H	L	H	H	L	22
H	L	L	H	H	L	23
L	L	L	H	H	L	24

Gate voltage switching
via DAQ Digital I/O lines

DIO 1	DIO 2	DIO 3	DIO 4	O/p
X	X	X	H	X
H	H	H	L	1
L	H	H	L	2
H	L	H	L	3
L	L	H	L	4
H	H	L	L	5
L	H	L	L	6
H	L	L	L	7
L	L	L	L	8

Figure 3.13: Electronic switchbox logic table.

gate voltage have been implemented. Additional commands can be added easily to the software. The software is also integrated with the “sweep” functions of the “SETACQ” program, so that two dimensional sweeps (gate and bias, or field and bias) can be performed on multiple samples. This is especially useful if you want to study multiple samples in an overnight run.

The usefulness of the electronic switchbox is limited by the noise introduced into the signals by the switching circuitry. Currently, the noise introduced is of the order of 200 μV. This limits the switchbox to fairly coarse measurements on the dilution fridge. While the purpose of the switchbox is served by the current design, I can think of a few modifications that will lower the noise level significantly:

1. One major source of noise is the fact that we have exposed signal lines on the boards. If you order custom boards, you can sandwich all the signal lines between ground planes in order to isolate them from the digital lines (you probably have to have a four layer board).
2. The reed relays are not shielded. Using shielded reed relays [17] may cut down on the noise.
3. Keeping the grounds separate. Currently the signal ground is shared with the digital ground. Separating the grounds from each other will reduce current noise on the ground line.
4. Using better connectors. The current design has solder connections to the various signal lines that are rather haphazard. The wiring is also not shielded or twisted. With some thought, it should be possible to bring all the signal lines to the edge of the board, so a single card-edge connector [18] can be

used. The wiring can then be easily shielded or joined into pairs. This will also reduce the soldering to a minimum.

5. Using mumetal shielding to reduce magnetic pickup.

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[11] D. Goldhaber-Gordon, personal communication.

[12] I use Coto technology reed relays (number 9001-05-00).

[13] I use Fairchild Semiconductor's 74ACT138 1-of-8 decoder.

[14] from Newark electronics www.newark.com.

[15] I have modified both “Mezurit” and “SETACQ”. Wires are broken and preliminary measurements are taken with “Mezurit”. For sweeps of gate and field, “SETACQ” is used.

[16] The code can be found in “stuff.c” in the SETACQ project.

[17] For example, the 9002 series of relays from Coto technology.

[18] Samtec is a good resource for specialty connectors.

Chapter 4

Coulomb blockade in $[Co(tpy-(CH_2)_5-SH)_2]$

4.1 Introduction

In chapters 2 and 3, I described the fabrication and measurement of molecular devices created using electromigration. In this chapter, I will discuss my first application of the technique, the molecule $[Co(tpy-(CH_2)_5-SH)_2]$. This molecule is chosen on account of its electrochemical properties, as described in the next section.

4.2 Molecule synthesis and electrochemistry

The structure of $[Co(tpy-(CH_2)_5-SH)_2]^{2+}$ (where $tpy-(CH_2)_5-SH$ is 4'-(5-mercaptopentyl)-2,2':6',2"-terpyridinyl) is depicted in fig. 4.1a. The scale bar shows the length of the molecule as calculated by energy minimization. The molecule $[Co(tpy-(CH_2)_5-SH)_2]^{2+}$ was synthesized from an ethanolic solution of 4'-(5-mercaptopentyl)-2,2':6',2"-terpyridinyl ($tpy-(CH_2)_5-SH$) and aqueous $CoCl_2$ [1].

This molecule is a coordination complex in which one Co ion is bonded within an approximately octahedral environment to two terpyridinyl linker molecules with thiol end groups, which confer high adsorbability onto gold surfaces. This molecule was selected because it is known from electrochemical studies that the charge state of the Co ion can be changed from 2^+ to 3^+ at low energy. A cyclic voltammogram [2] for $[Co(tpy - (CH_2)_5 - SH)_2]^{2+}$ adsorbed on a gold electrode in 0.1M tetra-n-butylammonium hexafluorophosphate/Acetonitrile is shown in fig. 4.1(c), indicating that a positive voltage $V_s \sim +0.15$ V (measured against an Ag/AgCl reference) applied to the solution removes one electron from the ion (the Co $2^+/3^+$ redox peak). While the voltage required to change the charge state of the molecule in a transistor geometry might be very different from an electrochemical experiment, the fact that the molecule is electrochemically active gives us hope that the gate voltage in a transistor setup can also change the charge state of the molecule.

4.3 Device fabrication

For this molecule, I made transistors (schematically shown in the lower inset to fig. 4.2) using the silicon-gated electromigration junctions described in 2.2. Before electromigration, I cleaned the wires with acetone, methylene chloride and oxygen plasma, and placed them in a dilute solution of the molecules in acetonitrile for a day or more in order to form a self assembled monolayer on the Au electrodes. I then cooled the wires in our top-loading dilution refrigerator to an electron temperature < 100 mK, and broke them by electromigration. In the upper inset to figure 4.2, a topographic atomic force microscope image of the electrodes with a gap (scale bar, 100nm). After electromigration, I determined the electrical characteristics of the molecule by acquiring current versus bias voltage (I-V) curves while changing the gate voltage (V_g).

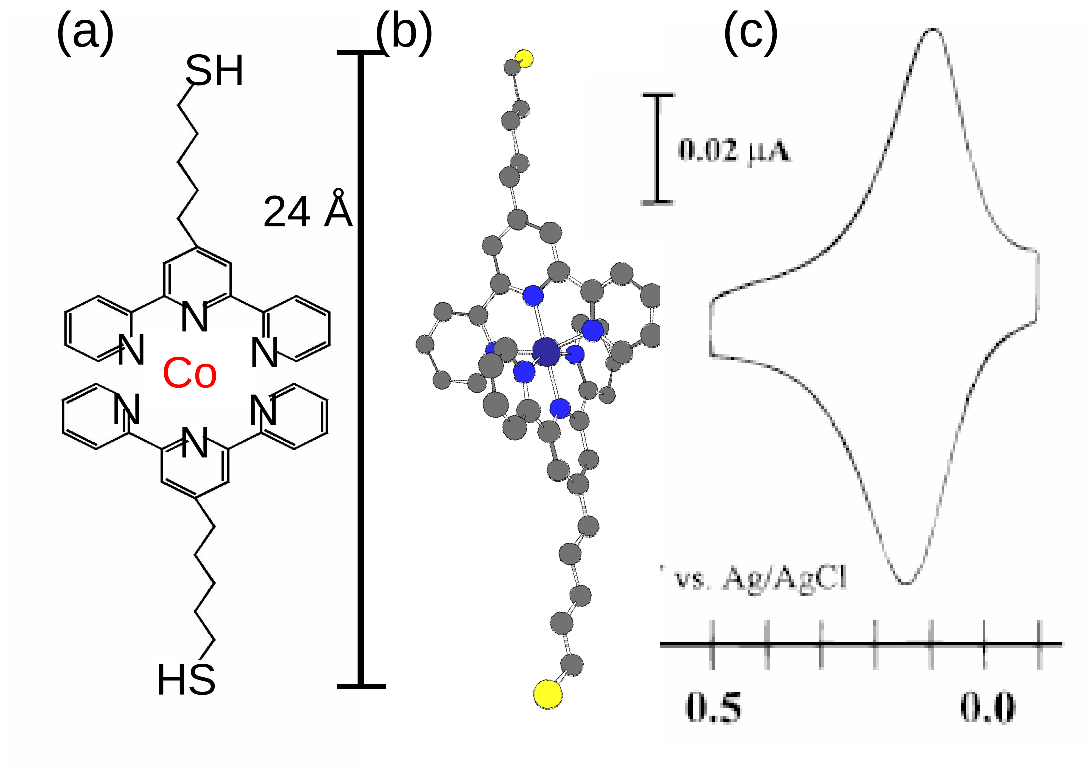

Figure 4.1: (a) Two-dimensional schematic of $[Co(tpy-(CH_2)_5-SH)_2]^{2+}$. (b) Three-dimensional energy-minimized structure. (c) Cyclic voltammogram in 0.1M tetra-n-butylammonium hexafluorophosphate/Acetonitrile.

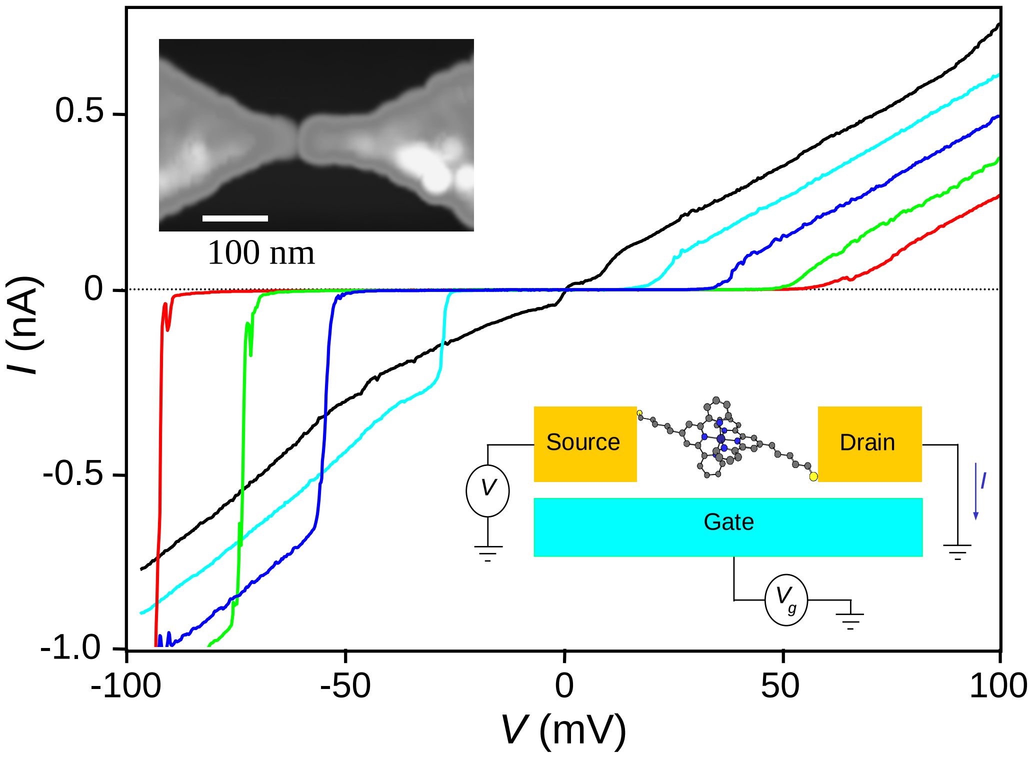

Figure 4.2: *I*-*V* curves from a $[Co(tpy-(CH_2)_5-SH)_2]^{2+}$ device at 100 mK, taken at equally-spaced gate voltages. (upper inset) AFM image of the device showing the electromigration gap. (lower inset) device schematic.

4.4 Coulomb blockade

In about 10% of 400 broken wires with adsorbed $[Co(tpy-(CH_2)_5-SH)_2]^{2+}$, we see *I*-*V* curves as shown in figure 4.2. The current is strongly suppressed up to some threshold voltage that depends on V_g and then it increases in steps. The different curves are at different gate voltages from -0.4 V (red) to -1.0 V (black) with $\Delta V_g \approx -0.15$ V. In figure 4.3 we show a higher-resolution color-scale plots of the differential conductance dI/dV at low bias, as a function of V and V_g. The darkest areas on the left and right of the plots indicate the regions of no current. The bright lines located outside of these regions correspond to a fine structure of current steps visible near the voltage thresholds.

This behavior is the signature of a single-electron transistor (SET) [3], a device containing a small island which is attached to electrodes by tunnel barriers and whose charge state can be tuned using a gate voltage. In this case the island is a single Co ion. For most values of V_g, the charge state of the ion is stable at low V (dark regions). An electron does not have sufficient energy to tunnel onto the island and therefore current is blocked (Coulomb blockade). The bright lines that define the boundaries of the Coulomb-blockade regions illustrate the tunneling thresholds for transitions between charge states. Conductance in the vicinity of $V=0$ is allowed at a value of gate voltage V_c where the charge states are degenerate. We label the charge states as Co^{2+} and Co^{3+}, in analogy with the electrochemical measurements, and this is supported by a spin analysis presented below.

In control experiments, this behavior has not been observed for any of 100

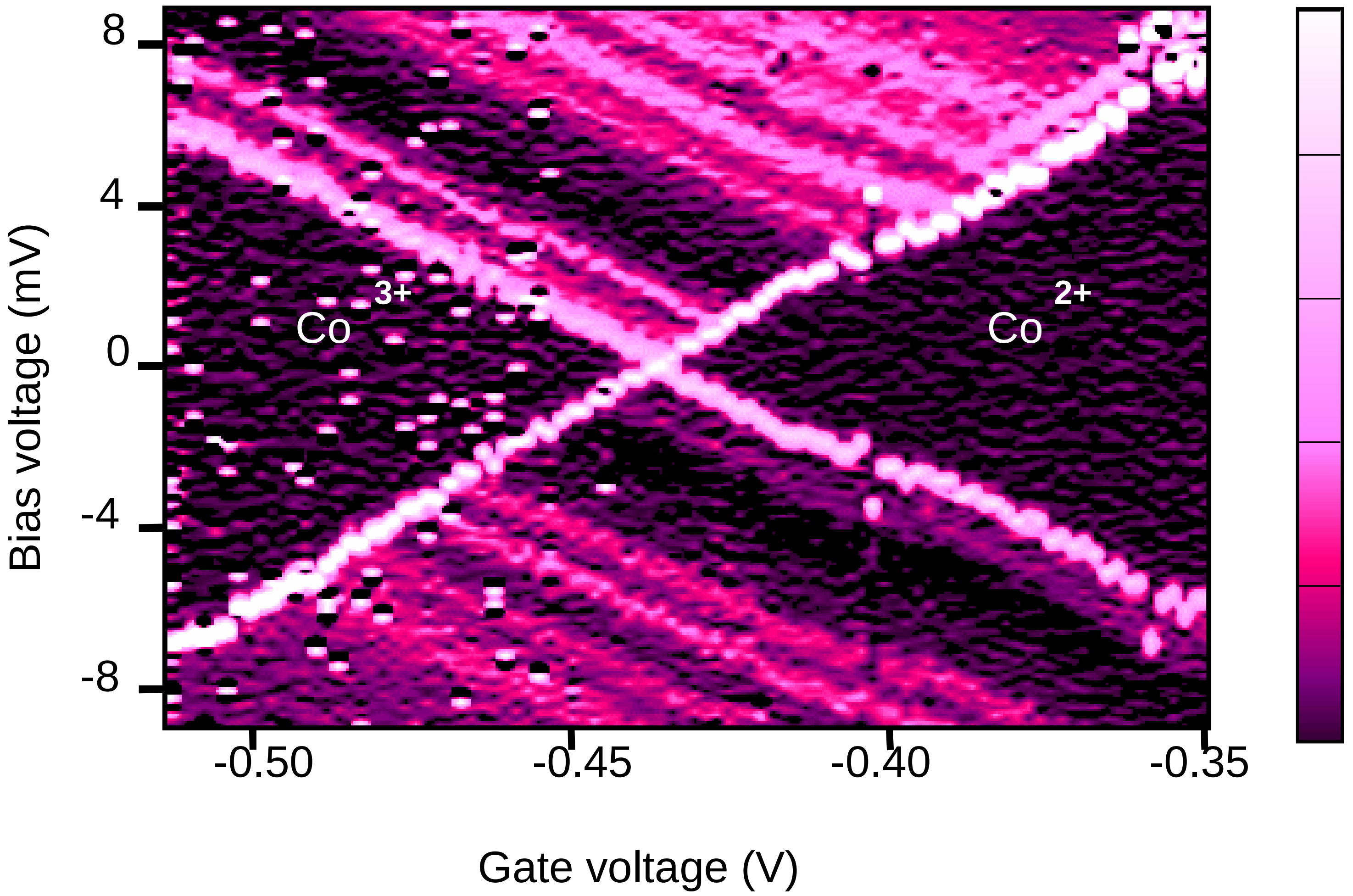

Figure 4.3: Colorscale dI/dV plots of a $[Co(tpy-(CH_2)_5-SH)_2]^{2+}$ single-electron transistor. The maxima of the scale is 5 nS.

bare gold wires or 50 gold wires coated with $tpy - (CH_2)_5 - SH$ linker molecules alone without Co ions. This provides strong evidence that the island of the SET is indeed the Co ion. We can be confident that the current near each degeneracy point is due to a single molecule because the degeneracy voltage V_c is different for each molecule due to local variations in the electrostatic environment. The non-blockaded resistance of devices range from 100 $M\Omega$ to $\approx$1 $G\Omega$. This is comparable to the resistance recently measured for alkanedithiol molecules whose length is comparable to the linker molecule used here [4]. These results clearly illustrate that the properties of the molecule are reflected in the electrical properties of the SET.

It is clear that dI/dV plots such as the one in fig. 4.3 carry a lot of spectroscopic information on the object being studied. There are several excellent discussions of the I-V characteristics of an SET [5, 6, 7]. They explain the experimental conditions under which such plots can be obtained as well as the interpretation of these plots. I will focus on two points that are relevant to this chapter as well as chapter 6:

1. To understand the various regions of these plots in terms of simple pictures.
2. To be able to extract energies of quantum levels from these plots.

4.5 Interpreting dI/dV plots: a single quantum level

Consider a molecule connected to source, drain and gate electrodes which has a some non-degenerate non-interacting levels available for transport. A circuit

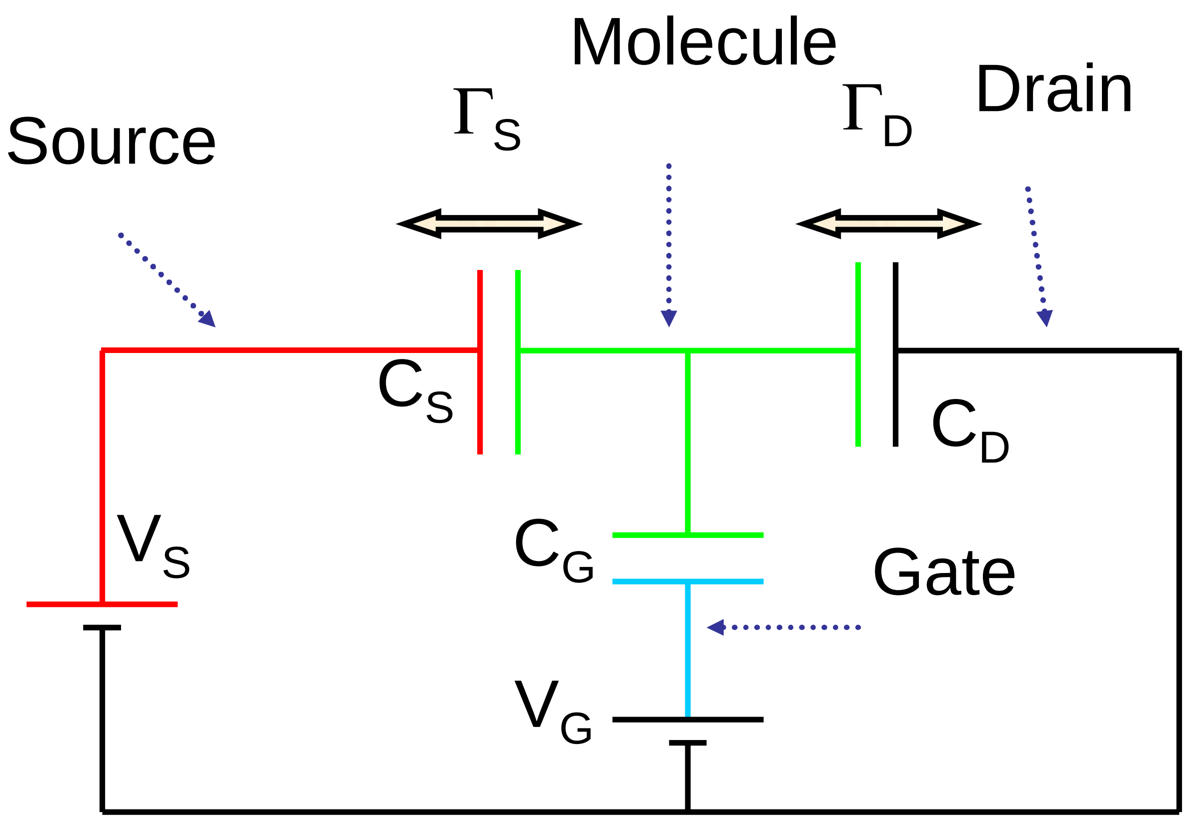

Figure 4.4: A circuit schematic of a single-electron transistor

schematic of this situation is shown in fig. 4.4. The following parameters determine transport through the dot at zero temperature:

1. The capacitances to the three electrodes C_S, C_D and C_G.
2. The coupling to the source Γ^i_S and drain Γ^i_D.

   $$\Gamma^i_A = \hbar \times W^i_A \quad (A = S, D) \tag{4.1}$$

   where W^i_A is the tunneling rate across barrier A. For a simple tunnel barrier (the sort discussed in 1.3.1) with a tunnel resistance R and capacitance C, at zero temperature $\Gamma = \hbar/RC$.
3. The voltage applied to the electrodes V_S, V_D and V_G.
4. The positions of the energy levels i on the dot relative to the Fermi level ϵ_i.

Let us start with the static equilibrium situation. In equilibrium, there are some number A electrons on the source electrode, B electrons on the molecule and C electrons on the drain (no current flows through the gate). Let us give this state a symbol - $(A|B|C)$. What is the total energy of the system?

1. Source potential energy

   $$-AeV_S.$$

2. Drain potential energy

   $$-CeV_D.$$

   We will assume henceforth that the drain is grounded ($V_D = 0$) so we can drop this term.

3. Molecule potential energy

$$-BeV_M^B + \sum_{i=0}^{B} \epsilon_i.$$

4. Energy stored in the capacitors

$$\sum_{i=S,D,G} \frac{Q_i^2}{2C_i}.$$

Here Q_i is the charge on each of the capacitors, given by

$$Q_i = C_i(V_i - V_M^B). \tag{4.2}$$

The potential of the molecule V_M^B with B electrons is set by the total charge on the molecule

$$\sum_i Q_i = -Be, \tag{4.3}$$

implying

$$V_M^B = \frac{\sum_i (C_i V_i) + Be}{C}, \tag{4.4}$$

with the total capacitance

$$C = \sum_i C_i. \tag{4.5}$$

To illustrate how to calculate when current will flow through the molecule, let us take the case where there is one level on the molecule, and only one electron available for transport. Then, using the previous equations, we get

$$E^{(0|1|0)} - E^{(1|0|0)} = \frac{e[(C_D + C_G)V_S - C_G V_G]}{C} + U + \epsilon_1, \tag{4.6}$$

$$E^{(0|1|0)} - E^{(0|0|1)} = -\frac{e[C_S V_S + C_G V_G]}{C} + U + \epsilon_1. \tag{4.7}$$

Here $E^{(A|B|C)}$ is the energy of $(A|B|C)$. The "charging energy" is given by the expression

$$U = \frac{e^2}{2C}. \tag{4.8}$$

Let us draw some pictures. A typical diagram describing the state of the system is shown in fig. 4.5(a). The figure has three parts. On the left and right are drawn the Fermi levels of the source and drain electrodes. Applying a positive bias to a lead is equivalent to pulling the Fermi energy down. In the center is shown the difference in energy between the occupied state and unoccupied state of the molecule (in general, this is the electrochemical potential)

$$\mu_1 = \frac{e[C_S V_S + C_G V_G]}{C} + U + \epsilon_1. \tag{4.9}$$

For fig. 4.5(a) $E^{(1|0|0)}, E^{(0|0|1)} > E^{(0|1|0)}$ In this case, the molecule prefers to stay occupied. The opposite is true in fig. 4.5(b), where the molecule is unoccupied. To simplify the math a little, let us redefine the zero of the gate potential so that $E^{(1|0|0)} = E^{(0|0|1)} = E^{(0|1|0)}$ at $V_G = 0$.

Let us now get some current to flow through the molecule by starting from fig. 4.5(a) and changing the bias voltage. As the source potential is varied, the electrochemical potential varies according to eqn. 4.9. In fig. 4.5(c) and (d) are shown diagrams for when current begins to flow. The conditions for current flow are $E^{(1|0|0)} = E^{(0|1|0)}$ for fig. 4.5(c) giving a critical value V_S^c at which current flows:

$$(C_D + C_G) V_S^c = C_G V_G. \tag{4.10}$$

Similarly, fig. 4.5(d) corresponds to $E^{(0|0|1)} = E^{(0|1|0)}$, or

$$C_S V_S^c = -C_G V_G. \tag{4.11}$$

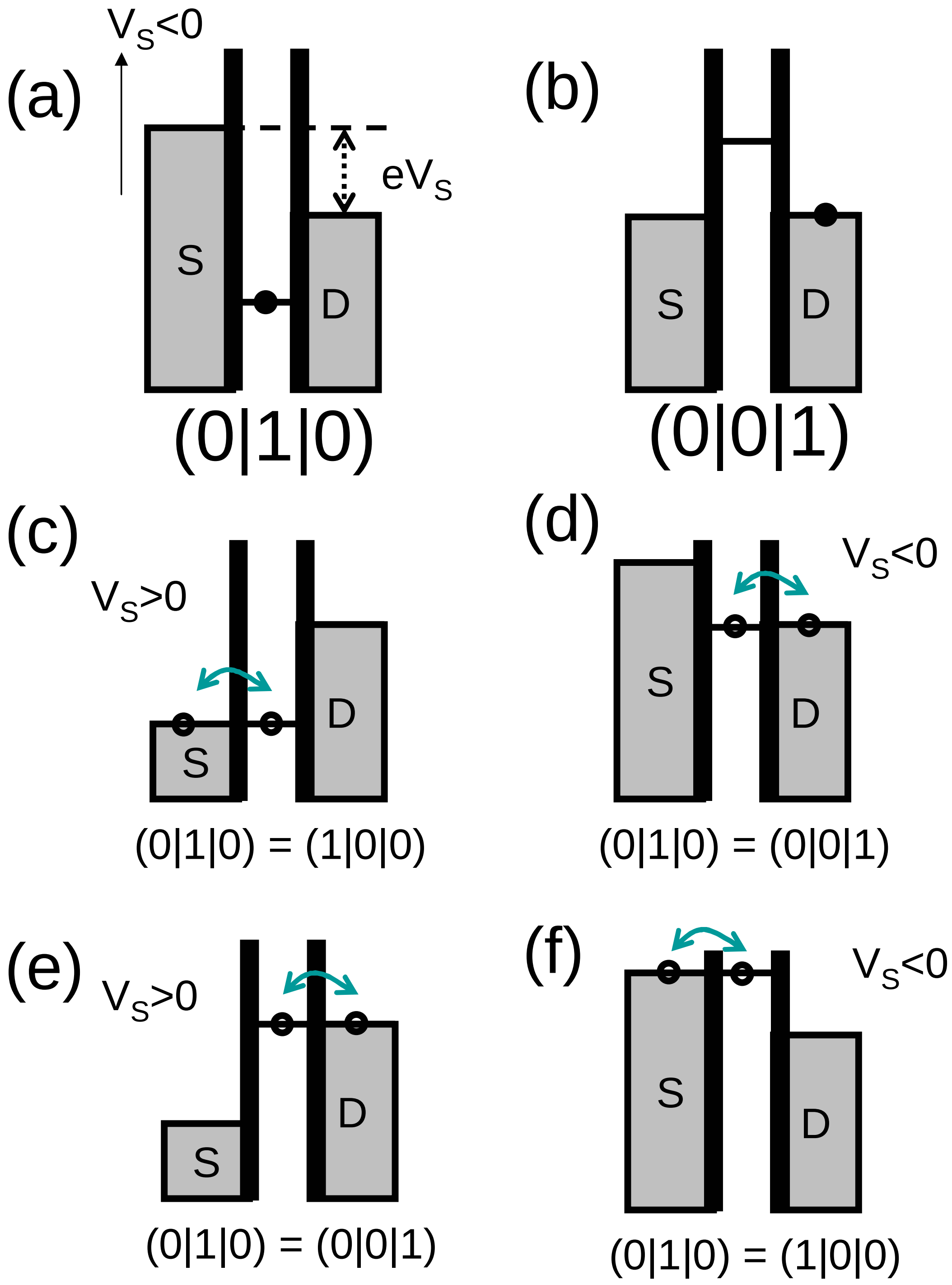

Figure 4.5: (a) occupied level. (b) unoccupied level. (c) and (d) - tunneling thresholds obtained by starting from (a) and changing V_S. (e) and (f) - thresholds when starting from (b).

Equations 4.10 and 4.11 together define the boundaries of the Coulomb blockade region. At non-zero temperature, the Fermi distribution of electrons on the electrodes also come into play in determining the current [6]. At zero temperature however, the current saturates as soon as the voltage thresholds are crossed.

We can put together all these diagrams and construct the two-dimensional plot of dI/dV for this single-level system. This is shown in fig. 4.6. The plot (and the plots in the following sections) has been generated with the help of Edgar Bonet's simulation program [8]. Cartoons for the various points on this plot are also shown.

4.6 Interpreting dI/dV plots: excited quantum levels

We have now understood what the conductance plot of a single level looks like. It is clear that additional lines in figure 4.3 running parallel to the tunneling thresholds indicate the contributions of excited states to the tunneling current. Let us extend the diagrams of the previous section to include these levels.

Both the occupied and unoccupied state of the molecule will have some excited level spectrum. Let us, as an example, consider a single excited level for the occupied state at energy $\epsilon_1 + \epsilon_1^e$. Let us also give the unoccupied molecule an excited state at $\epsilon_0 + \epsilon_0^e$. In general $\epsilon_0^e \neq \epsilon_1^e$. We can include them in our cartoon as shown in fig. 4.7(a). The three lines on the molecule now correspond to μ_1, $\mu_1 + \epsilon_1^e$ and $\mu_1 - \epsilon_0^e$.

Let us start at $V_S = V_G = 0$ (fig. 4.7(a)) and try to get some current to flow through these excited states by changing V_S. Shown in fig. 4.7(b) and (c) are the

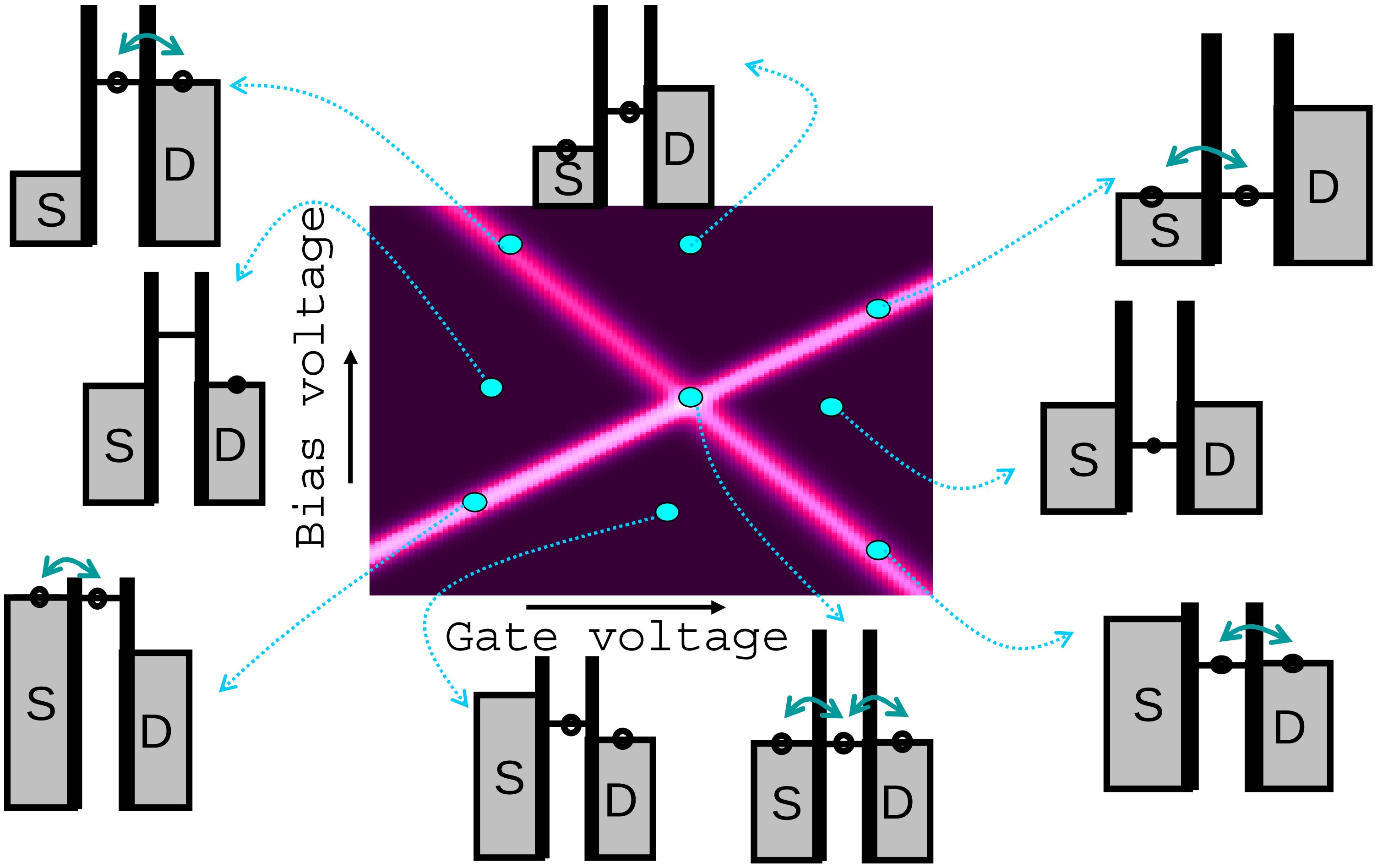

Figure 4.6: Two-dimensional colorscale plot of the theoretical dI/dV for a single-level quantum dot.

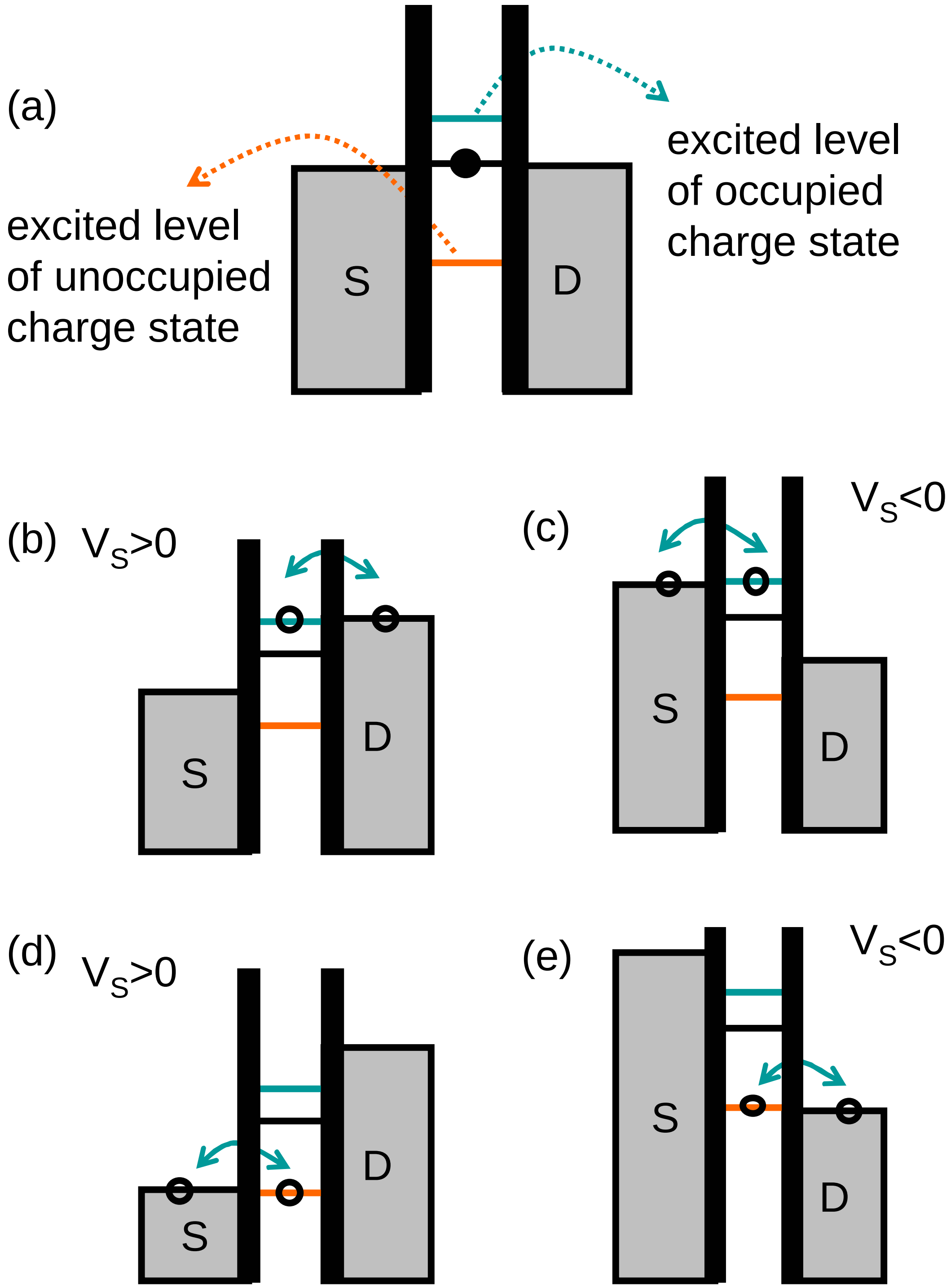

Figure 4.7: (a) Excited levels for the charged (blue) and uncharged (orange) states. (b) and (c) tunneling thresholds for the charged excited level. (d) and (e) thresholds for the uncharged excited level.

current flow thresholds for the excited state of the occupied charge state. Similar thresholds for the unoccupied excited state are shown in (d) and (e). It is clear from these figures that the equations governing the slopes of these thresholds are the same as that governing the transition between the ground states of the two charge states.

How about the blockade region in fig. 4.6? Is it modified in the presence of excited levels? This might seem possible, since there is (for example) a gate voltage where the excited *occupied* level has the same energy as the ground *unoccupied* level at zero source voltage. Can you then have current flowing due to transitions between these states? The answer is no - even if such transitions were occurring, eventually a transition will happen where the *ground* level of the occupied state is filled. As soon as this happens, all further transitions are blocked. Thus, in the absence of some external charge pumping mechanism [9], the blockade region does not depend on the presence of excited states.

Putting this story together, we can draw the conductance plot shown in fig. 4.8 and mark the points corresponding to (b) through (e) from fig. 4.7. This is beginning to look a lot more like fig. 4.3. Using the pictures we have developed, we can make the following statements

1. Lines ending in the blockade region of a given charge state, are excited levels of that state.
2. Lines with positive slope in fig. 4.8 are transitions where the source electrode lines up with an available level on the molecule.
3. All lines with negative slope in fig. 4.8 are transitions where the drain elec-

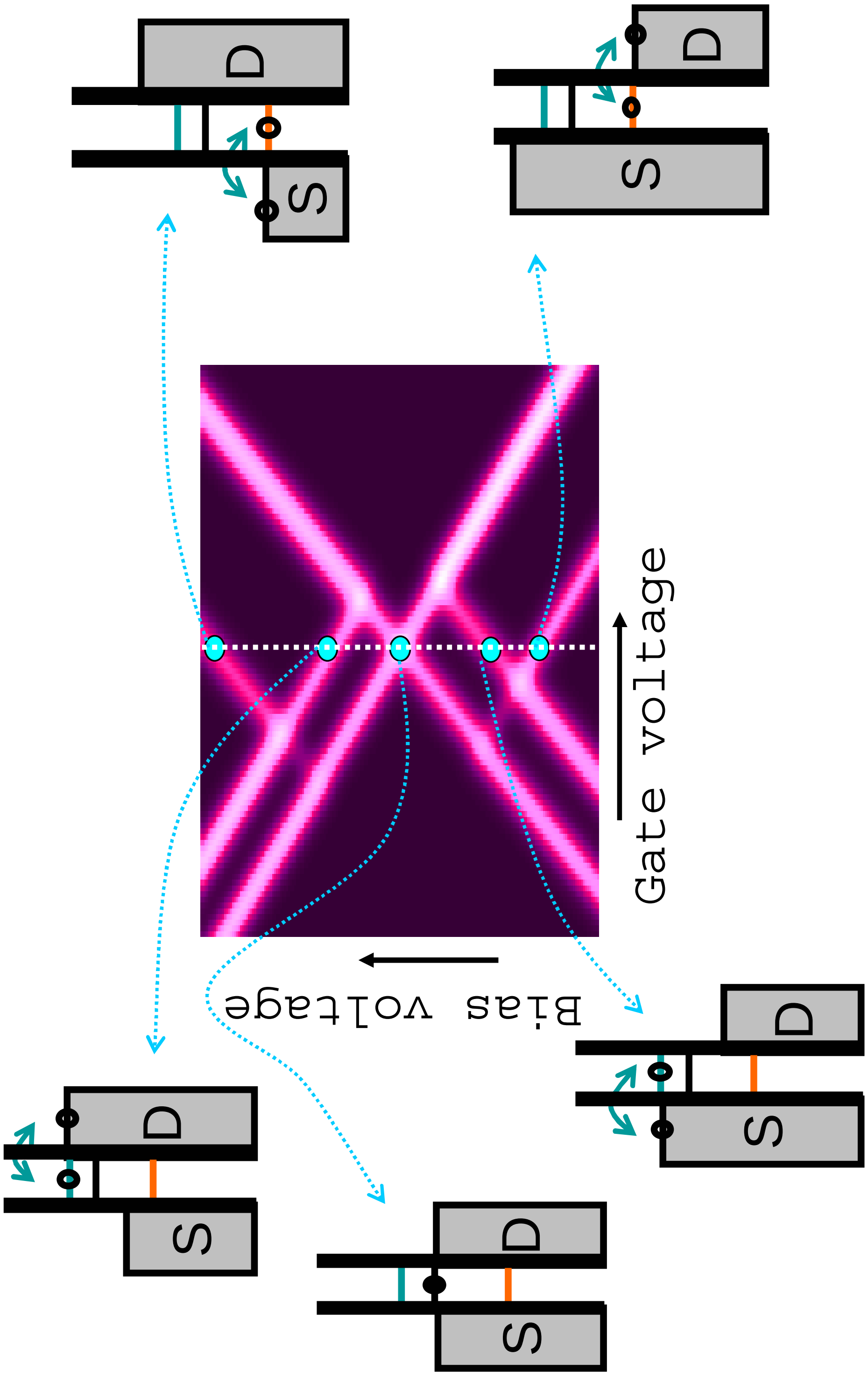

Figure 4.8: Two-dimensional colorscale plot of dI/dV for a quantum dot with a single excited level for each charge state.

trode lines up with an available level on the molecule.

4. The energy of a given excitation is the bias voltage at which the excitation meets the blockade region. This is shown in fig. 4.9. Here the molecule is shown to have a single excited level with energy ΔE. Points B and C are thresholds for the excited level at zero gate voltage. The source voltage at these points is larger than ΔE. At all points along line L1 the excited level is lined up with the source electrode. At all points along L2, the ground level is lined up with the drain electrode. At the point D, which is the intersection of these lines, both these conditions are true, and therefore the source voltage at this point is ΔE.

4.7 Current magnitudes

We are almost in a position to understand fig. 4.3. There is still one difference between fig. 4.3 and our theory plots such as fig. 4.8. You will notice in fig. 4.8 that every excited level shows up as two lines in the conductance plot - one at positive source voltage and one at negative source voltage. This however is not the case in fig. 4.3 - there is only one line visible for each excited level. Why is this the case?

When we ask how much current flows through a given level i, we have to clearly consider the tunnel rates Γ_S^i and Γ_D^i to the source and drain electrodes. In general, in our devices, one or the other of these rates is much larger. A small Γ corresponds to a large resistance, or a thicker barrier for tunneling. For a single level, the case $\Gamma_S >> \Gamma_D$ is schematically illustrated in fig. 4.10(a).

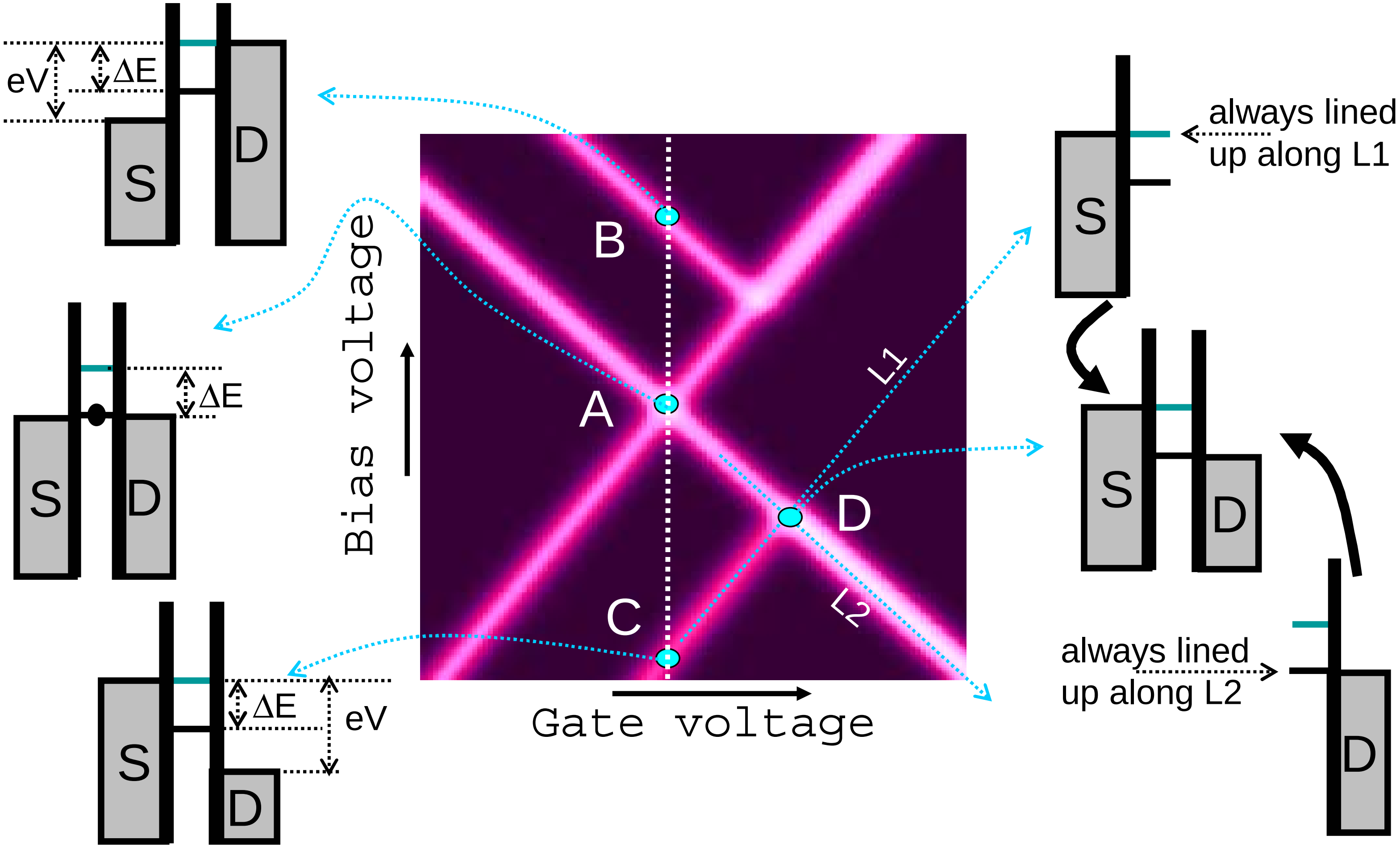

Figure 4.9: Deducing the energy of an excited level.

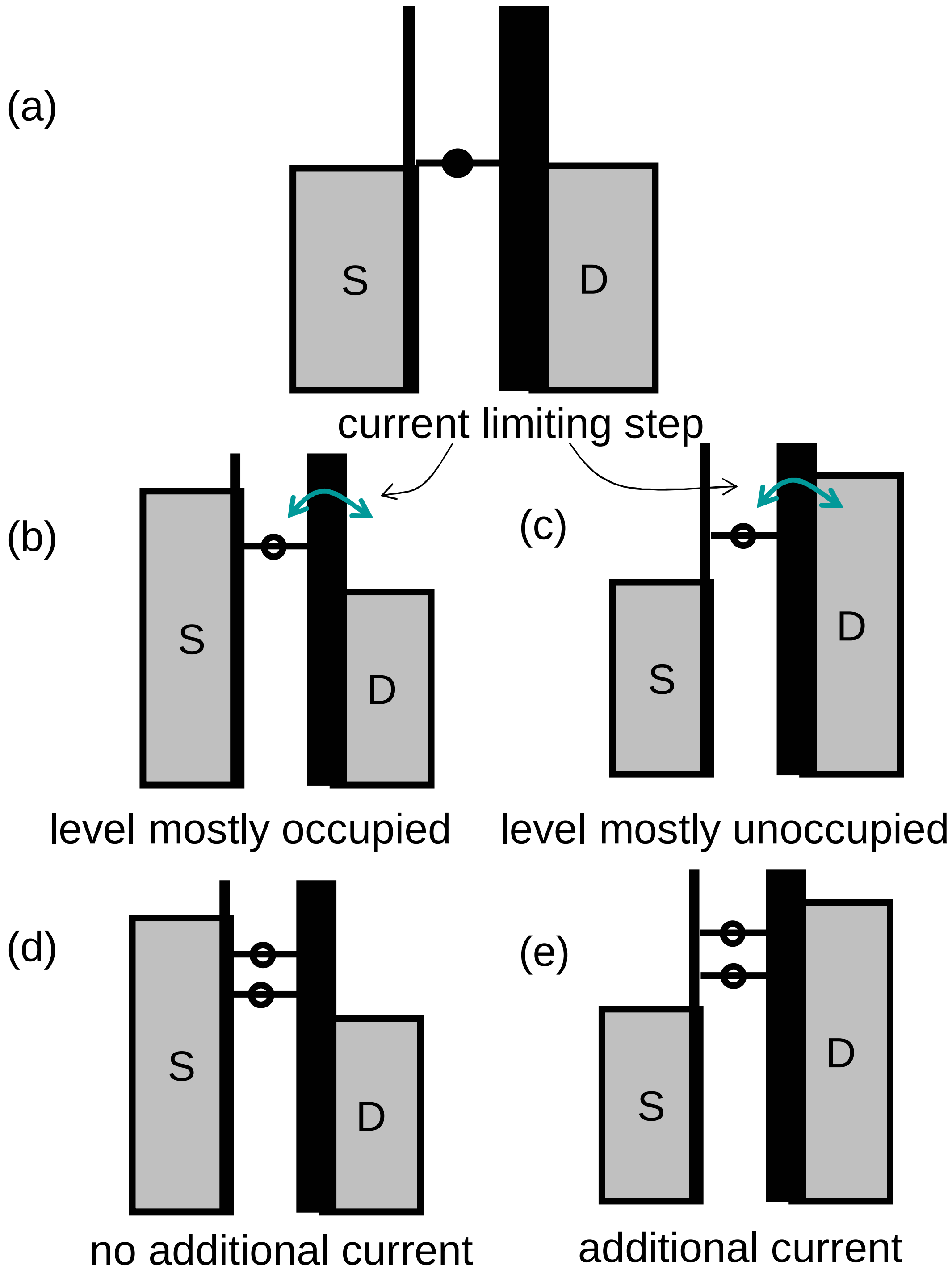

Figure 4.10: (a) Depicting the case $\Gamma_S > \Gamma_D$. (b) negative and (c) positive bias tunneling through a single level. (d) negative and (e) positive bias tunneling through two levels.

What is the consequence of asymmetric barriers? Consider the diagrams fig. 4.10(b) and (c). We can calculate the current flowing through the molecule in each case by using rate equations [5]. Let us start with fig. 4.10(b) - negative source bias. Let us also for the moment assume that there is no spin-degeneracy. If we assume that the time-averaged probability that the molecule level is occupied is p ($0 \leq p \leq 1$), the current flowing across the source is

$$(1-p)e\Gamma_S.$$

The current flowing across the drain is

$$pe\Gamma_D.$$

In equilibrium, these currents are equal, giving

$$p_- = \frac{\Gamma_S}{\Gamma_S + \Gamma_D}, \tag{4.12}$$

and

$$I_- = e\frac{\Gamma_D \Gamma_S}{\Gamma_S + \Gamma_D}. \tag{4.13}$$

For fig. 4.10(c), positive source bias, we have to switch source and drain in the last two equations, giving

$$p_+ = \frac{\Gamma_D}{\Gamma_D + \Gamma_S}, \tag{4.14}$$

and

$$I_+ = e\frac{\Gamma_S \Gamma_D}{\Gamma_D + \Gamma_S}. \tag{4.15}$$

We can make the following observations:

1. The total current flowing is the same for both positive and negative bias (remember again that we have assumed that there is no spin-degeneracy).

This is true since the electron has to get through both barriers to cause net current to flow. To lowest order, the current is given by the lower tunneling rate:

$$I_+ = I_- = e\Gamma_D. \tag{4.16}$$

2. The average occupation of the molecule is drastically different in the two cases when the barriers are asymmetric. In fact, if $\Gamma_S >> \Gamma_D$, we have (to first order)

$$p_- = 1 - \frac{\Gamma_D}{\Gamma_S}, \tag{4.17}$$

$$p_+ = \frac{\Gamma_D}{\Gamma_S}. \tag{4.18}$$

   This makes intuitive sense. In fig. 4.10(b), the electron easily makes it across the source barrier in time $\approx 1/\Gamma_S$, but has to wait a time $\approx 1/\Gamma_D$ to make it across the drain. Thus, the level is almost always occupied. The reverse is true for fig. 4.10(c). Here, the electron has to wait a long time to get onto the molecule from the drain, but it can jump off easily onto the source.

We saw that for a single level, asymmetry in the barriers does not influence the positive bias and negative bias currents through the level. This is no longer true when there are excited levels for transport.

Consider the cases shown in fig. 4.10(d) and (e), which correspond to the presence of a single excited level as in fig. 4.9. We assume that the tunneling rates are the same for both levels. We can calculate the currents in these cases once again using rate equations. If p_0 and p_1 are the time-averaged occupation of the ground level and excited level respectively ($0 \leq p_0 + p_1 \leq 1$), then for negative bias (fig.

4.10(d)), we have equations for the currents flowing through both levels:

$$(1 - p_{0-} - p_{1-})e\Gamma_S = p_0\Gamma_D, \tag{4.19}$$

$$(1 - p_{0-} - p_{1-})e\Gamma_S = p_1\Gamma_D. \tag{4.20}$$

$$\tag{4.21}$$

Solving these equations gives

$$p_{0-} = p_{1-} = \frac{\Gamma_S}{\Gamma_D + 2\Gamma_S}, \tag{4.22}$$

and the current

$$I_- = \frac{2\Gamma_S\Gamma_D}{\Gamma_D + 2\Gamma_S}. \tag{4.23}$$

To get the corresponding values for positive bias (fig. 4.10(e)), we switch source and drain in the previous equations giving

$$p_{0+} = p_{1+} = \frac{\Gamma_D}{\Gamma_S + 2\Gamma_D}, \tag{4.24}$$

and

$$I_+ = \frac{2\Gamma_D\Gamma_S}{\Gamma_S + 2\Gamma_D}. \tag{4.25}$$

Simplifying to lowest order gives

$$I_- = e\Gamma_D, \tag{4.26}$$

$$I_+ = 2e\Gamma_D. \tag{4.27}$$

To get the current flowing through the excited level, we subtract the current flowing through the ground level from eqn. 4.16, giving

$$I_-^1 = 0, \tag{4.28}$$

$$I_+^1 = e\Gamma_D. \tag{4.29}$$

So here we see that the barrier asymmetry has created a large asymmetry in the current for positive and negative bias. We can understand this by noting that in the case of positive bias, the occupation probabilities of the molecule are small. Thus every excited state carries significant current since it forms a bridge across the high-resistance barrier. In the case of negative bias however, the occupation probability is nearly unity even for a single level. Additional levels do not affect the current significantly.

In fig. 4.11 we have repeated the conductance plot shown in fig. 4.8, but we have fixed $\Gamma_S/\Gamma_D = 30$. The lines with negative slope (that have thresholds for tunneling across the drain) are visible clearly whereas the ones with positive slope do not show up on the plot.

4.8 Energy levels in $[Co(tpy-(CH_2)_5-SH)_2]^{2+}$ transistors

We can now understand completely the dI/dV plot in fig. 4.3. It is clear that there are a number of excited levels contributing to transport. Lines that end in the Co^{3+} (Co^{2+}) blockade region correspond to excited levels of the Co^{3+} (Co^{2+}) charge state.

How reproducible is the pattern of excited levels from device to device? In fig. 4.12 we show dI/dV plots for the device shown in fig. 4.3 and two other devices. The pattern of excited states is qualitatively, but not quantitatively, similar from molecule to molecule. Typically we observe several lines at energies below 6 meV. No additional lines are resolved between ≈6-30 meV, at which point additional strong peaks are seen.

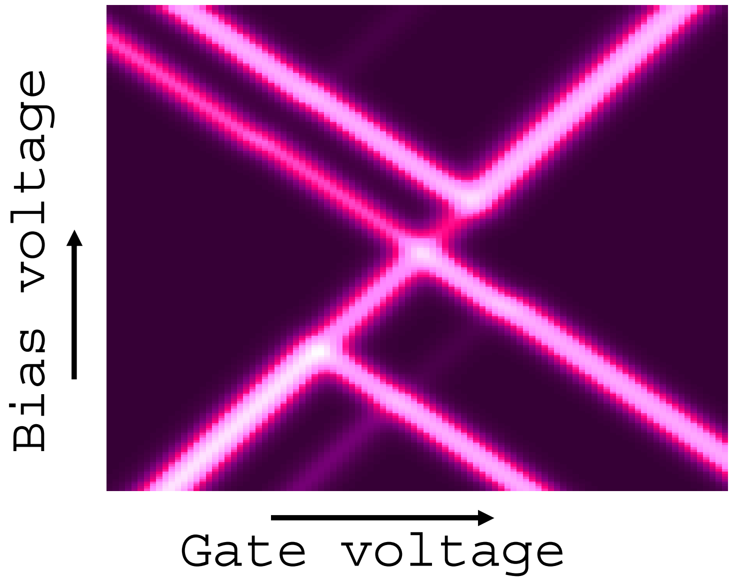

Figure 4.11: Conductance plot with the same parameters as fig. 4.8 except $\Gamma_S = 30\Gamma_D$.

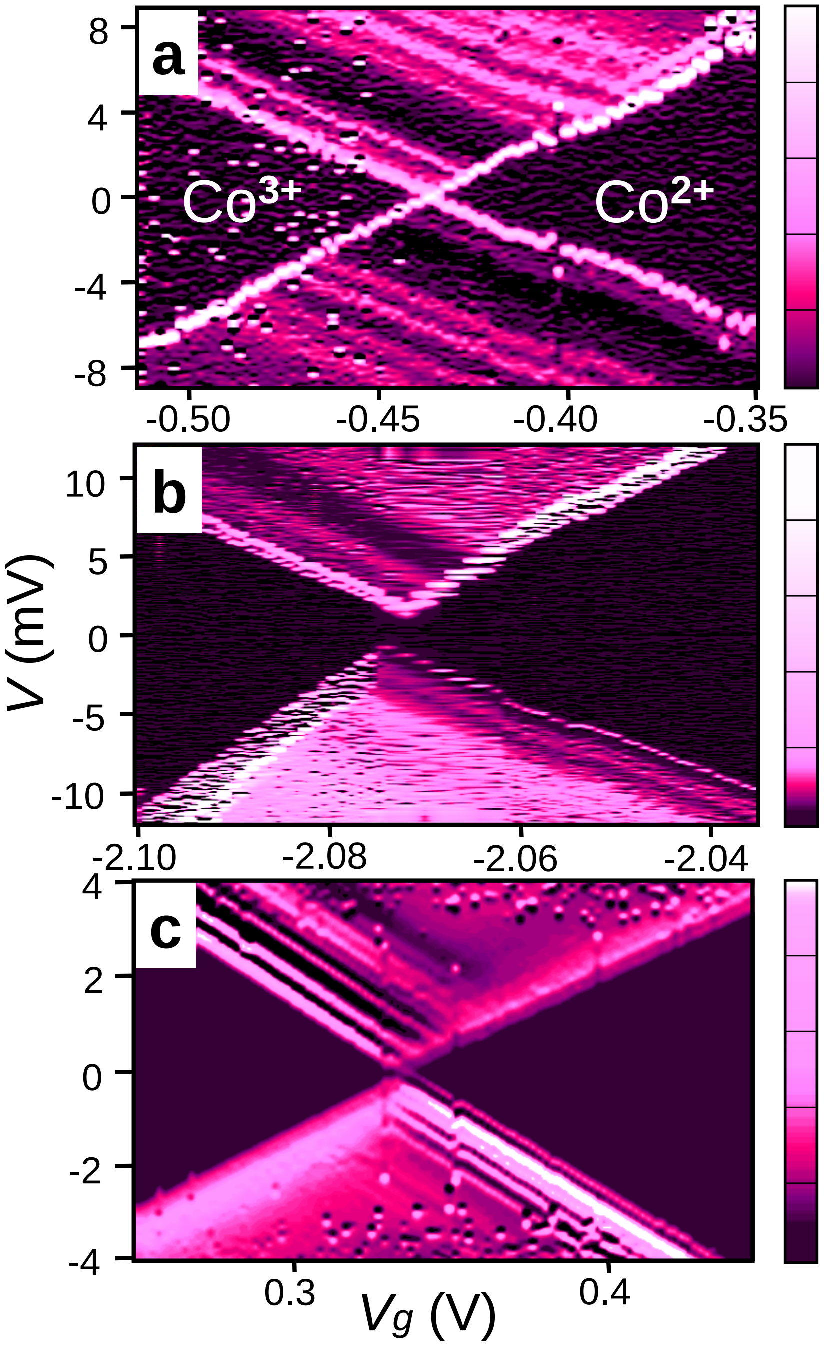

Figure 4.12: Colorscale dI/dV plots of three different devices. The maxima of the scales are 5 nS in (a), 10 nS in (b) and 500 nS in (c)

A notable feature of the excited-state spectra is that the pattern of low-lying excitations is the same for both charge states of a given molecule. This, together with the small energy scale, suggests that the low-energy excitations are not associated with different electronic configurations. In order to test whether the excitations may be associated with the emission of a phonon [10], we have calculated the normal modes of the molecule using a quantum chemistry package (HyperChem 7.0). The simulations show normal modes with energies beginning at approximately 1 meV, with a density of ≈2 modes/meV, in reasonable consistency with our observations. It will be interesting to study how the vibrational energies depend on the details of electrode attachment (using molecular modeling) in order to address the differences in the excited-state spectra.

We have applied a magnetic field H to determine the magnetic state of the Co ion. fig. 4.13(a) shows a color plot of dI/dV at a magnetic field of 6 T for the same device as in figure 4.3. A new excited Co^{2+} level, denoted by a triangle, has split from the Co^{3+} to Co^{2+} ground-state transition. The energy difference between these two states is linear in H, with a slope corresponding to a g-factor of 2.10.2. There is no corresponding Co^{3+} excited state splitting from the Co^{2+} to Co^{3+} ground-state transition.

These results indicate that the Co^{2+} state is spin-degenerate, while the Co^{3+} state is not. An unambiguous identification of the Co^{2+} ground state as $S = 1/2$ and the Co^{3+} ground state as $S = 0$ is indicated by an analysis of the tunneling current amplitudes. The lower-energy Zeeman-split state in figure 4.13(a) carries a current of 1.0 pA, and the second is nearly equal, 0.8 pA. Nearly equal currents are expected for $S = 0$ to $S = 1/2$ tunneling, for a tunneling threshold across the

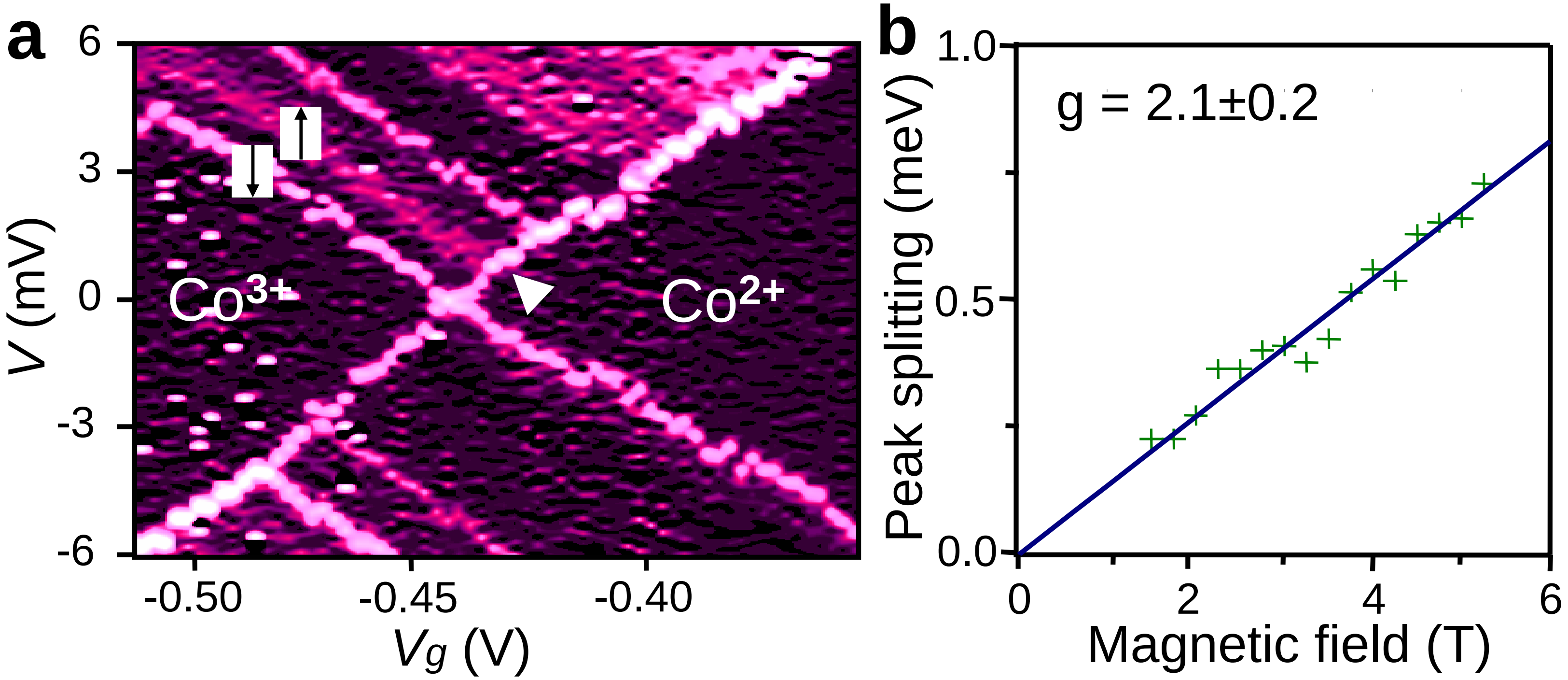

Figure 4.13: (a) dI/dV plot of the same device as figure 4.3 at a field of 6 T. There is an extra level (indicated with the triangle) seen due to the Zeeman splitting of the lowest energy level of Co^{2+}. The arrows denote the spin of the tunneling electron. (b) Magnitude of the Zeeman splitting as a function of magnetic field.

higher-resistance tunnel junction [11, 12]. For any higher spin, the current carried by the second state would be suppressed by a Clebsch-Gordan coefficient by at least a factor of 2 compared to the first state [13].

The electronic structure inferred above is consistent with the expected electronic structure of the Co ion if its angular momentum is quenched due to the binding to ligand molecules. A Co^{2+} ion ($3d^7$) has an odd number of electrons and possesses Kramers'-degenerate states that will split in a magnetic field, while Co^{3+} ($3d^6$) has an even number of electrons and may have a total spin $S = 0$ so that it will not undergo Zeeman splitting [14]. Previous magnetization studies in bulk material suggest that Co^{2+} in the molecule is $S = 1/2$ at cryogenic temperatures [15]. Our measurements provide a confirmation of this result.

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Chapter 5

Kondo-assisted tunneling in $[Co(tpy-SH)_2]$

5.1 Introduction

In the previous chapter, I described the fabrication and measurement of $[Co(tpy-(CH_2)_5-SH)_2]$ single-electron transistors. Using this molecule we were able to create high-resistance devices exhibiting Coulomb blockade. One obvious modification to the previous experiment is to modify the chemical structure of the molecule in some way and look for changes in the transport properties. In this chapter we will describe such an experiment, where we have removed the pentyl chains on $[Co(tpy-(CH_2)_5-SH)_2]$.

5.2 Molecule synthesis and electrochemistry

The structure of $[Co(tpy-SH)_2]^{2+}$ (where tpy-SH is 4'-(mercapto)- 2,2':6',2"-terpyridinyl) is depicted in fig. 5.1(a). The scale bars show the lengths of the molecules as calculated by energy minimization. $[Co(tpy-SH)_2]^{2+}$ is a complex of cobalt with 4'-(mercapto)- 2,2':6',2"-terpyridinyl (tpy-SH). The tpy-SH ligand was prepared from 4'-chloro-2,2':6',2" terpyridinyl and sodium ethanethiolate by a nucleophilic aromatic substitution followed by nucleophilic aliphatic substitution to give the thiolate anion and subsequent protonation to give the desired compound

[1, 2].

The electrochemical properties of $[Co(tpy - SH)_2]^{2+}$ are similar to $[Co(tpy - (CH_2)_5 - SH)_2]$. A cyclic voltammogram [3] for $[Co(tpy - SH)_2]^{2+}$ adsorbed on a gold electrode in 0.1M tetra-n-butylammonium hexafluorophosphate/Acetonitrile is shown in fig. 5.1(c), indicating that a positive voltage $V_s \sim +0.25$ V (measured against an Ag/AgCl reference) applied to the solution removes one electron from the ion (the Co $2^+/3^+$ redox peak).

5.3 Devices

Preparation of $[Co(tpy - SH)_2]^{2+}$ devices is performed exactly the same way as devices made from $[Co(tpy - (CH_2)_5SH)_2]^{2+}$ the gate voltage (V_g). One immediate difference seen in devices made from the two molecules is that we are usually able to see devices with fairly low resistance (100s of $k\Omega$), which we were not able to see in devices made from the longer molecule. This is reasonable, since we expect significantly larger conductances due to the shorter tether length. In fact, we observe conductances large enough that we can see directly when a molecule becomes inserted in the gap between the electrodes, as shown in fig. 5.2. During the course of electromigration, the conductance initially decreases below the conductance quantum ($2e^2/h$), indicating a tunneling gap between the electrodes. If the voltage is increased further, the current often suddenly increases by up to a factor of 10 (red dot, figure 5.2). This behavior is not observed for bare gold electrodes. We therefore interpret the jump as the inclusion of at least one molecule in the gap between electrodes [4]. We stop the electromigration process once this

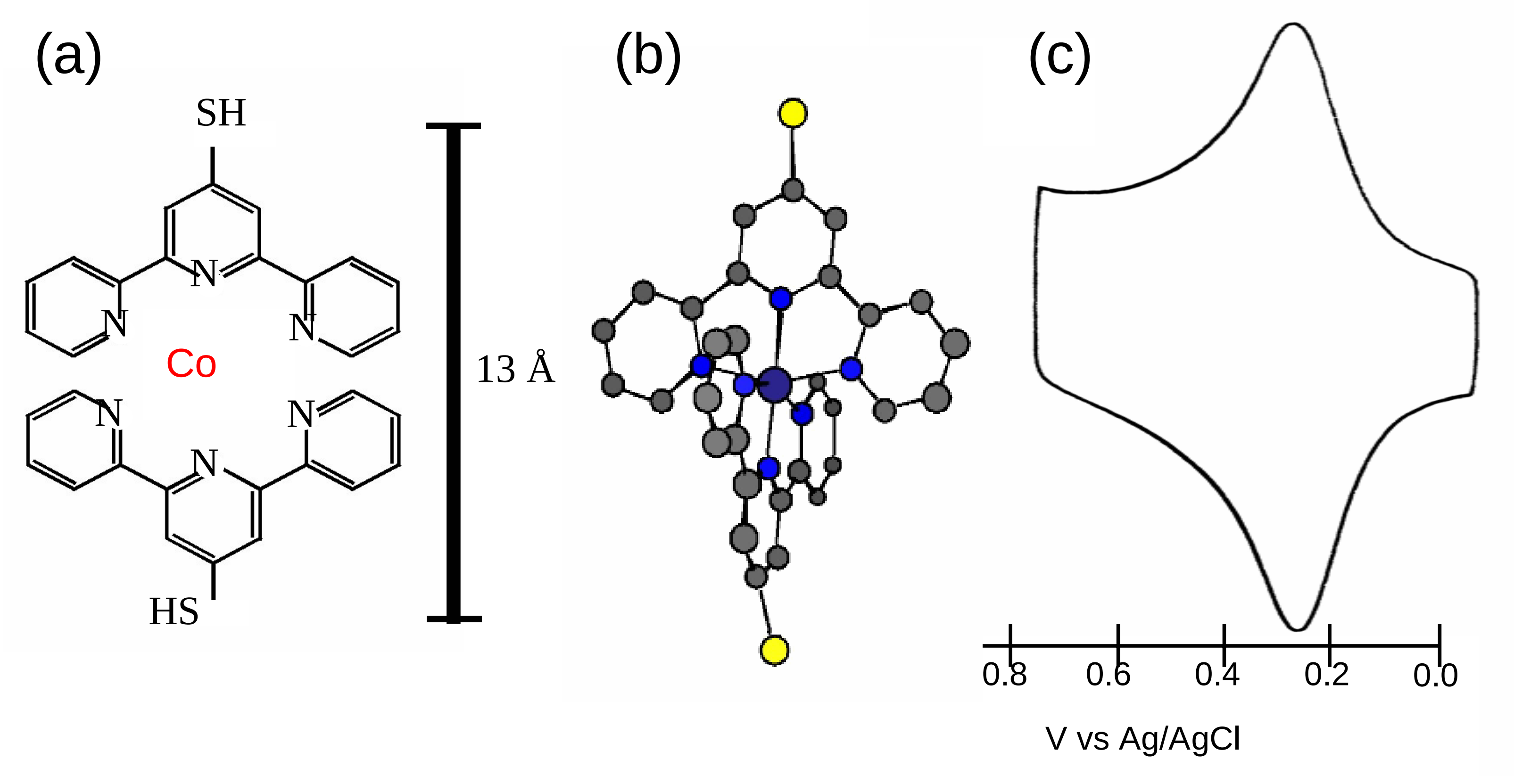

Figure 5.1: (a) Two-dimensional schematic of $[Co(tpy - SH)_2]^{2+}$ (b) Three-dimensional energy-minimized structure (c) Cyclic voltammogram in 0.1M tetra-n-butylammonium hexafluorophosphate/Acetonitrile

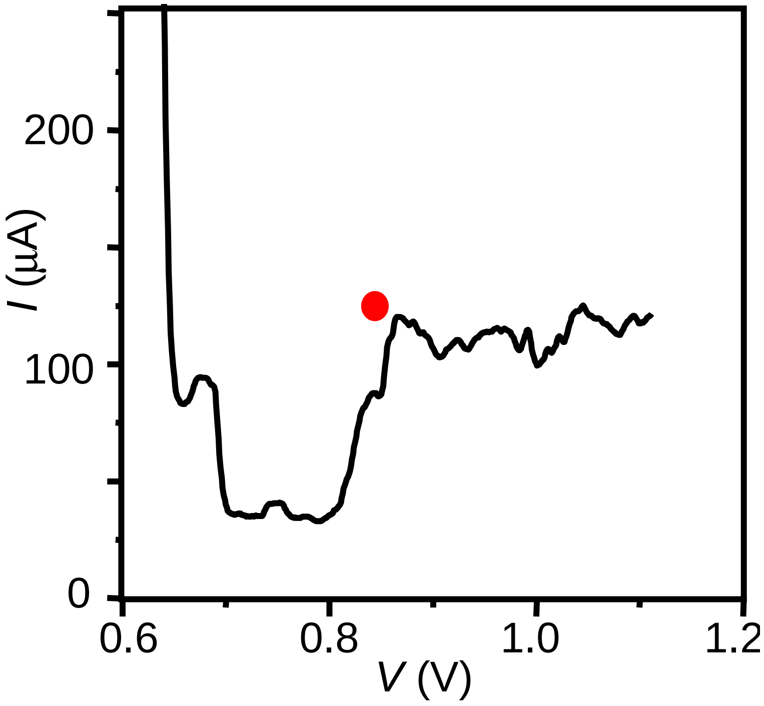

Figure 5.2: Breaking trace of a gold wire with adsorbed $[Co(tpy-SH)_2]^{2+}$ at 1.5K.

happens and study the devices at lower V. The differential conductance dI/dV for one such device is shown in fig. 5.3(a). The most striking property is a peak in dI/dV at $V = 0$. Fig. 5.3(b) shows dI/dV plots for bare gold point contacts for comparison.

The peak in dI/dV at $V = 0$, is very unlike devices made from $[Co(tpy - (CH_2)_5SH)_2]^{2+}$, where the conductance was suppressed on account of Coulomb blockade. We believe that the peak comes from Kondo-assisted tunneling through the molecule.

5.4 The Kondo effect: A brief non-history

The Kondo effect is now well known in transport through quantum dots. It has been seen in transport through defect states in metallic point contacts [5], semiconductor quantum dots [6, 7], carbon nanotubes [8] and single molecules [9, 10]. Perhaps the simplest manifestation of the Kondo effect is shown in fig. 5.4, taken from [7]. Here, the linear ($V = 0$) conductance of a quantum dot is plotted as a function of gate voltage. It is seen that every alternate Coulomb "valley" has high conductance, i.e. there seems to be no Coulomb blockade in every alternate valley. Further, the valleys can be made to reappear by increasing the temperature as shown in fig. 5.4.

The Kondo effect in bulk metals arises from the interaction of dilute magnetic impurities with the non-magnetic conduction electrons. The history of the Kondo effect is too long to recount in a reasonable way in this thesis. There is an extensive review of experiments on bulk Kondo systems in [11]. The usual textbook used for

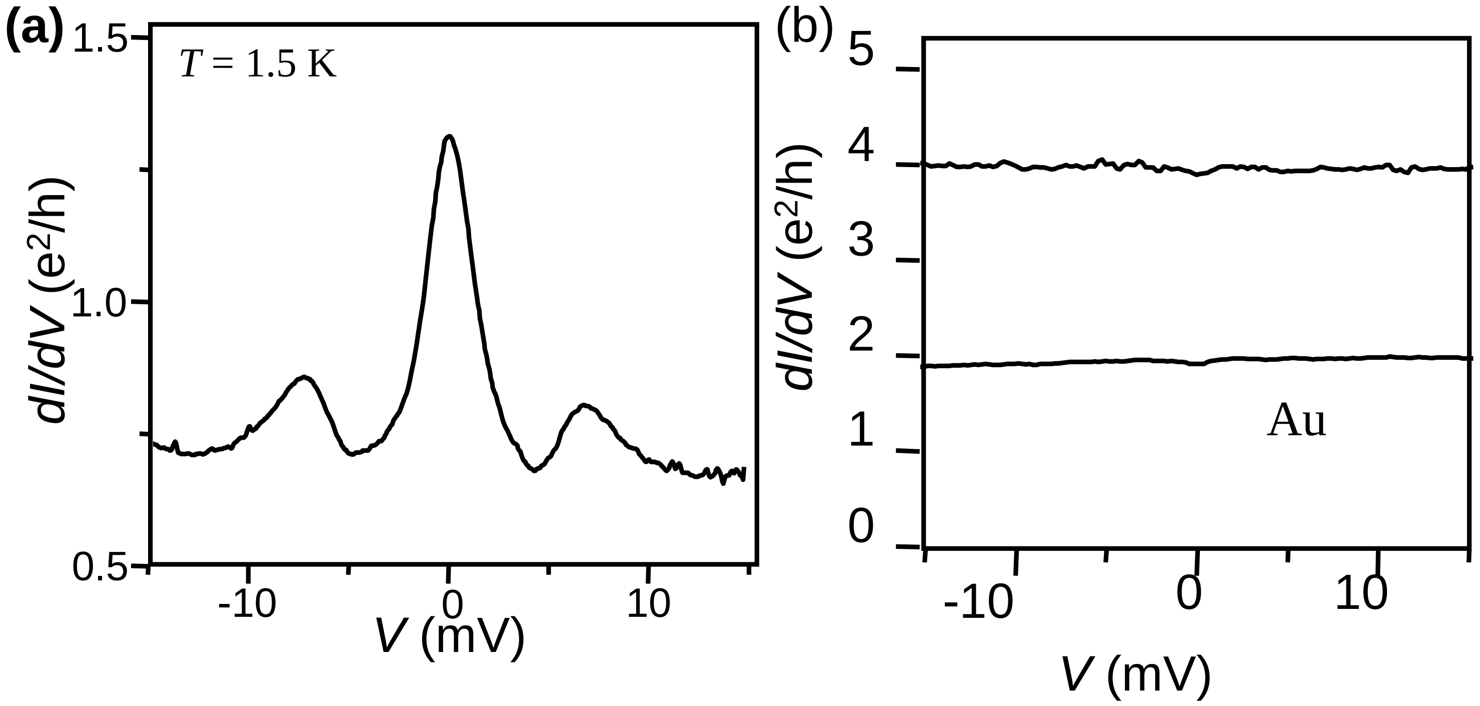

Figure 5.3: (a) dI/dV trace of a $Co-(tpy-SH)_2$ device at $T = 1.5$ K. (b) dI/dV traces of gold point contacts for comparison

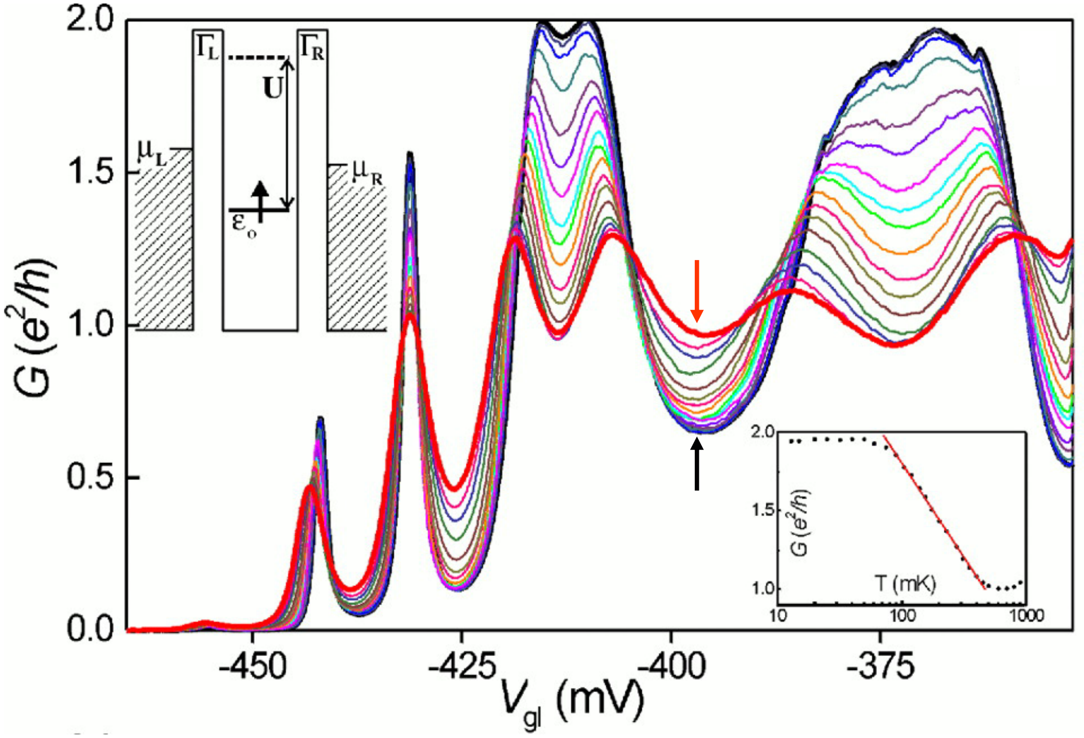

Figure 5.4: dI/dV - V_G traces (from [7]) at different temperatures. The red curve (red arrow, highest temperature) shows Coulomb blockade peaks. The black curve (black arrow, lowest temperature) shows enhanced conductance in alternate Coulomb valleys.

understanding the Kondo effect is [12].

What do quantum dots have to do with magnetic impurities? In a particular regime of parameter space (see below) a quantum dot *is* a magnetic impurity. Take a quantum dot with a single available energy level that is spin-degenerate. The dot can be occupied by 0, 1 or 2 electrons. A simple model for this system is the Anderson Hamiltonian [13]

$$H = H_L + H_R + H_{dot} + H_{int}, \tag{5.1}$$

where the different terms are (left and right lead conduction electrons)

$$H_{L(R)} = \sum_{k \in L(R),\sigma} \epsilon_{k\sigma} c^{\dagger}_{k\sigma} c_{k\sigma}, \tag{5.2}$$

(quantum dot, including the Coulomb interaction)

$$H_{dot} = \epsilon_0 \sum_{\sigma} d^{\dagger}_{\sigma} d_{\sigma} + U n_{\uparrow} n_{\downarrow}, \tag{5.3}$$

(interaction between the leads and the dot)

$$H_{int} = \sum_{k \in L,R;\sigma} (V_{k\sigma} c^{\dagger}_{k\sigma} d_{\sigma} + h.c.). \tag{5.4}$$

The definitions of the various quantities are:

1. $\epsilon_{k\sigma}$: dispersion relation for the conduction electrons with wavevector k and spin σ in the leads. I will assume in this chapter that $\epsilon_{k\uparrow} = \epsilon_{k\downarrow}$. The exact form of $\epsilon_{k\sigma}$ is relatively unimportant as long as it is a smooth function.

2. ϵ_0 : is the energy of the level on the dot.

3. U : is the Coulomb repulsion energy. In the absence of coupling to the leads, the energy of the dot is 0 (unoccupied state), ϵ_0 (singly occupied state) or

$2\epsilon_0 + U$ (doubly occupied state). This can be stated alternately by saying that the charging energy of the unoccupied dot is ϵ_0, and the charging energy of the singly-occupied dot is $\epsilon_0 + U$.

4. $V_{k\sigma}$: is the coupling between the leads and the dot.

5. $n_\sigma = d^\dagger_\sigma d_\sigma$: is the number operator for the dot.

The "Kondo regime" is when ϵ_0 is well below the Fermi energy ϵ_F, but $\epsilon_0 + U >> \epsilon_F$ so that the ground state of the system in the absence of tunneling is one electron on the dot. The system is drawn schematically in fig. 5.5(a). The temperature enters into the problem via the Fermi distribution of electrons on the lead.

A magnetic impurity in a bulk system is usually described by the Kondo Hamiltonian [14]. The Kondo Hamiltonian can be mapped on the spin-1/2 Anderson Hamiltonian in the limit where the charge fluctuations on the impurity are small [15]. In this sense, some thermodynamic properties of both systems such as the single-particle density of states [12] are identical.

The "Kondo problem" is finding the ground state of the spin-1/2 Anderson Hamiltonian at low temperatures. By now, there are several references [16, 17, 18, 19, 12, 20] giving various explanations for why the answer is what it is. I will content myself with describing the ground state with the following points:

1. At temperatures much larger than the Kondo temperature (defined below), the single-particle density of states of the dot is two resonances at energies ϵ_0 and $\epsilon_0 + U$ of width $\Gamma_L + \Gamma_R$ (as shown in fig. 5.5(b)) given by

$$\Gamma_{L,R} = \pi\nu V^2_{L,R}. \tag{5.5}$$

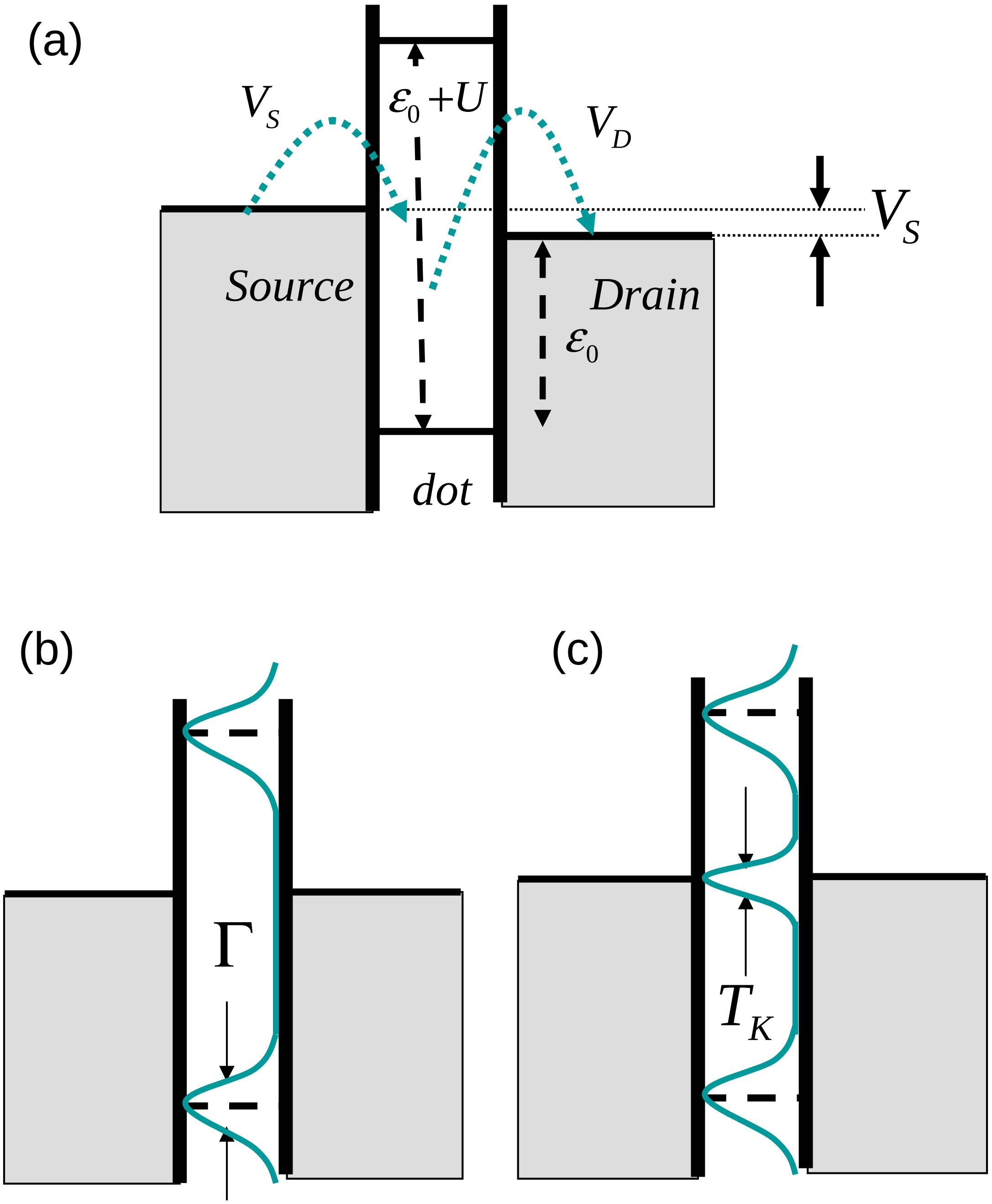

Figure 5.5: (a) The spin-1/2 Anderson model in the Kondo regime. (b) High temperature dot single-particle DOS ($\Gamma = \Gamma_L + \Gamma_R$). (c) Low temperature single-particle DOS showing the Kondo resonance at the Fermi energy.

Here ν is the conduction electron DOS (assumed constant).

2. Perturbation theory to order V^6 for various thermodynamic quantities gives corrections that go as $\log(T/T_K)$ where T_K is the Kondo temperature

$$T_K = \frac{\sqrt{\Gamma U}}{2} e^{\pi\epsilon_0(\epsilon_0+U)/\Gamma}. \tag{5.6}$$

   and $\Gamma = \Gamma_L + \Gamma_R$. This expression for the Kondo temperature is true in the limit where the conduction electron bandwidth W is larger than the charging energies. If this is not the case, the definition of the Kondo temperature will be different (see [21] for some other expressions).

3. At T=0, the single-particle density of states of the impurity has an additional resonance (the Kondo resonance) with width $\approx T_K$ (see fig. 5.5(c))

5.5 $T = 0$: The Friedel Sum Rule

At $T = 0$, the conductance of the dot is proportional to the single-particle density of states at the Fermi level $A_\sigma(\epsilon_F)$ [21]:

$$G = \sum_\sigma \frac{e^2}{h}\left(\frac{\Gamma_L\Gamma_R}{\Gamma_L + \Gamma_R}\right)A_\sigma(\epsilon_F). \tag{5.7}$$

The Kondo resonance in the density of states therefore implies a high conductance at $T = 0$ for a spin-1/2 quantum dot.

The Friedel sum rule [22, 23, 24] also gives an expression for the $T = 0$ conductance of the dot in terms of the average occupation of the dot levels:

$$G = \frac{e^2}{h}\sum_\sigma sin^2(\pi < n_\sigma >). \tag{5.8}$$

Here $< n_\sigma >$ is the average occupation of spin σ in the ground state. This equation tells us a fair bit about the Kondo effect:

1. Consider a single level with no spin degeneracy. In this case, $< n >$ is close to 1, and the conductance is close to zero. Consider also the spin-1/2 case where the Coulomb repulsion U goes to zero. In this case as well, the occupation of both spin channels is close to 1, and the conductance is small. So for the Kondo effect to work, both level degeneracy as well as a large Coulomb repulsion is essential. The degeneracy need not only arise from spin - other degeneracies will also give rise to the Kondo effect [12].

2. In the situation where there is nothing to break spin symmetry (no magnetic fields, for example),

   $$< n_\uparrow >=< n_\downarrow >= n_0, \tag{5.9}$$

   $$G = \frac{2e^2}{h} sin^2(n_0). \tag{5.10}$$

3. Further, for the symmetric Anderson model ($\epsilon_0 = -U/2$), particle-hole symmetry gives $n_0 = 1/2$ and so

   $$G = \frac{2e^2}{h}. \tag{5.11}$$

   In fact, this is true independent of the value of ϵ_0, implying that the Coulomb blockade is completely lifted for the spin-1/2 system.

4. In an externally applied magnetic field, the levels Zeeman split and the conductance is lowered. Once the magnitude of the field is larger than the width of the Kondo resonance, the occupation of the lower-energy spin channel tends to unity, and the conductance tends to zero.

5.6 Non-equilibrium

One reason why quantum dots are a better probe of the physics behind the Kondo effect than bulk systems is because you can apply an arbitrary voltage *across* a dot - something that cannot be done for a bulk system. We can see from fig. 5.3(a) that increasing the bias voltage leads to a drop in dI/dV. When a voltage bias is applied across the dot the following is true:

1. The single-particle density of states has two resonances at the Fermi energy of each electrode, as shown in fig. 5.6(a).
2. Electrons that are transferred from the higher bias lead to the lower bias lead dissipate to the Fermi energy of the lower bias lead in a time τ_{in}, and can no longer tunnel back to the higher bias lead. τ_{in} decreases with increasing bias voltage since the number of possible inelastic scattering processes increase.
3. Larger values of τ_{in} is equivalent to larger values of the temperature of the system [21], which lowers the height of the Kondo resonance.

The drop in dI/dV comes from both the fact that the Kondo resonances due to the two electrodes do not line up with each other, as well as the diminishing of the Kondo resonance [16].

In the presence of an externally applied magnetic field, more interesting things can happen. Firstly, at zero bias (or if you have only one electrode), the dot DOS is no longer spin-independent. Each spin direction produces a Kondo resonance in the DOS at an energy

$$\epsilon_\sigma = \epsilon_F + \sigma g \mu_B H. \tag{5.12}$$

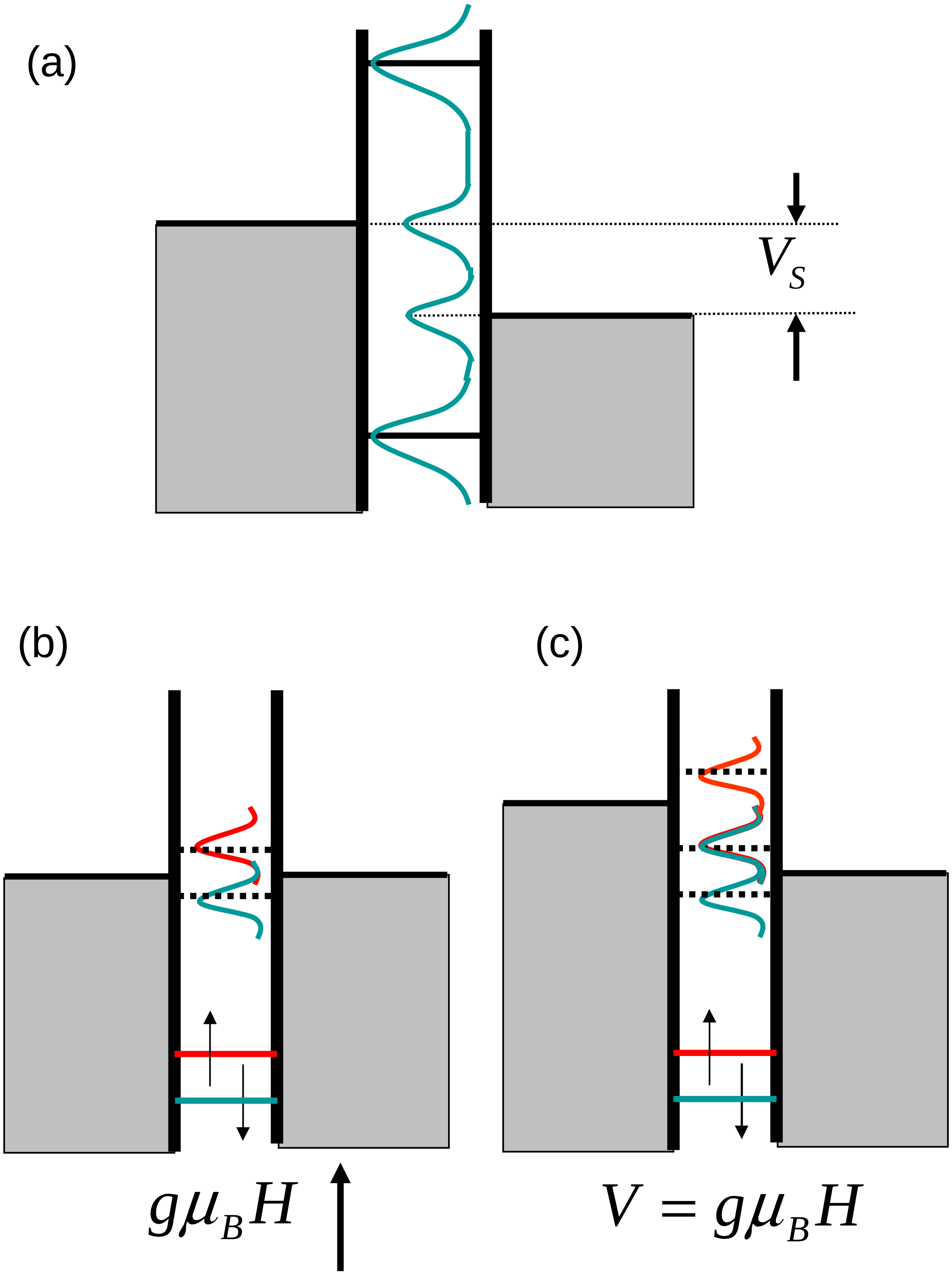

Figure 5.6: (a) Effect of non-zero V - two diminished resonances. (b) Effect of H - the DOS becomes spin-dependent, resonances shift away from ϵ_F. (c) a peak in dI/dV is seen when $V = g\mu_B H$.

Here g is the Lande g-factor, μ_B the Bohr magneton, H the applied field and $\sigma = \pm 1/2$. This is illustrated in fig. 5.6(b). This implies low linear conductance at $T = 0$. However, in the presence of a bias voltage, electrons from the higher bias lead can tunnel through the Kondo resonance due to the other lead, leading to a peak in dI/dV at a voltage (as illustrated in fig. 5.6(c))

$$eV_H = g\mu_B H. \tag{5.13}$$

5.7 Back to data

The observation of the Kondo effect in our devices is consistent with the identification of $S = 1/2$ for the Co^{2+} ion given in the previous chapter. Coming back to fig. 5.3, we can make an estimate of the Kondo temperature by setting the low-T full-width at half-maximum of the Kondo peak equal to $2k_BT_K/e$ [6, 7]. We estimate that T_K in different devices varies between 10 and 25 K. In order to make a better estimate, we would have to see the associated Coulomb peaks in order to get an estimate of Γ. We almost never see the Coulomb peaks in our measurements. The high values of the Kondo temperature we see suggest values of Γ that are several tens of meV (see eqn. 5.6). Seeing such a broad resonance would be very unlikely unless the background is perfectly flat, which is not usually the case in our devices.

We have seen the Kondo peak in 30% of ≈100 wires broken with the molecule, but is absent in clean gold electrodes, showing that it arises from the presence of the molecule. We have also seen the two signatures of the Kondo effect described above. The first is the splitting of the Kondo peak in an applied magnetic field. Shown in fig. 5.7 is a dI/dV plot of a device as a function of V_S and applied field

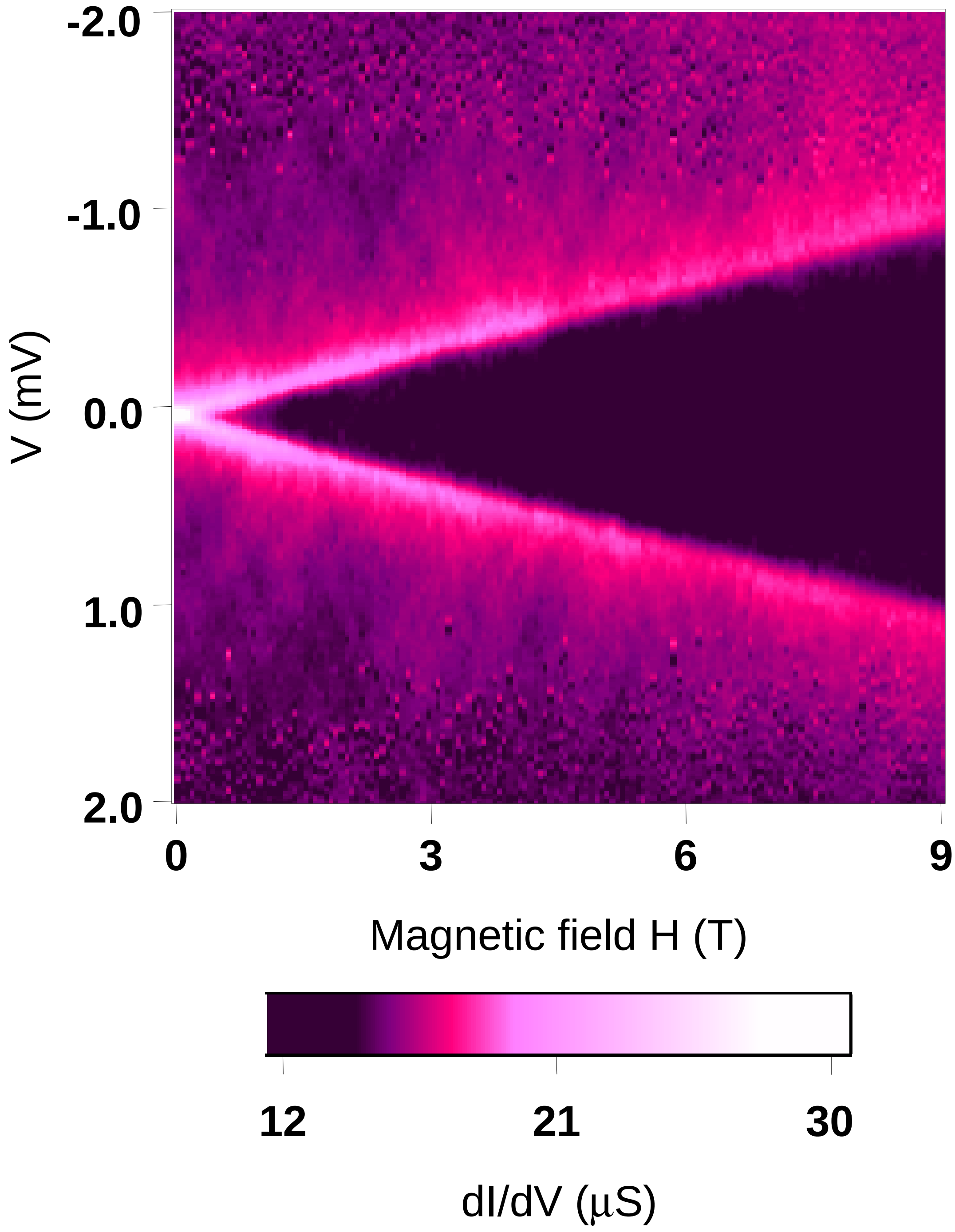

Figure 5.7: Effect of H - the peak in dI/dV splits into two peaks at $V = \pm g\mu_B H$ with $g = 2$.

H. The peak splits with a g-factor of 2 at high field. The value of the g-factor is consistent with measurements from the previous chapter. We see the same g-factor in all our devices to within measurement accuracy.

The conductance peak in our devices also displays the logarithmic dependence with temperature as is expected. Shown in fig. 5.8(a) is a device whose peak conductance (fig. 5.8(b)) has a logarithmic temperature dependence between 3 and 20K.

Another measurement that we would like to perform is to use a gate voltage to shift ϵ_0. We have been thus far unable to significantly gate our molecules. This is most likely due to the fact that they are very strongly coupled to the source and drain electrodes (as evidenced by the large Kondo temperatures we see).

In one device, we saw something rather unexpected. Instead of a single Kondo peak at $V = 0$, we saw two Kondo peaks even at zero applied field (see fig. 5.9). In an applied field, the splitting is first decreased, reduced to zero and then increases once again (fig. 5.10). Such behavior has been seen before in quantum dots [25, 26]. In general, for such behavior to happen, the dot has to have a spin state different from $S = 1/2$.

One possibility considered by Pustilnik and Glazman is the case where the dot has two unpaired electrons in states with different energies with total spin $S = 1$, and the couplings of the two states to the reservoirs is different [27]. This results in a two-stage Kondo effect where the total spin of the dot is screened first to $S = 1/2$ and then to $S = 0$ at two different temperatures. The completely screened dot has low linear conductance [27] similar to that seen in fig. 5.9.

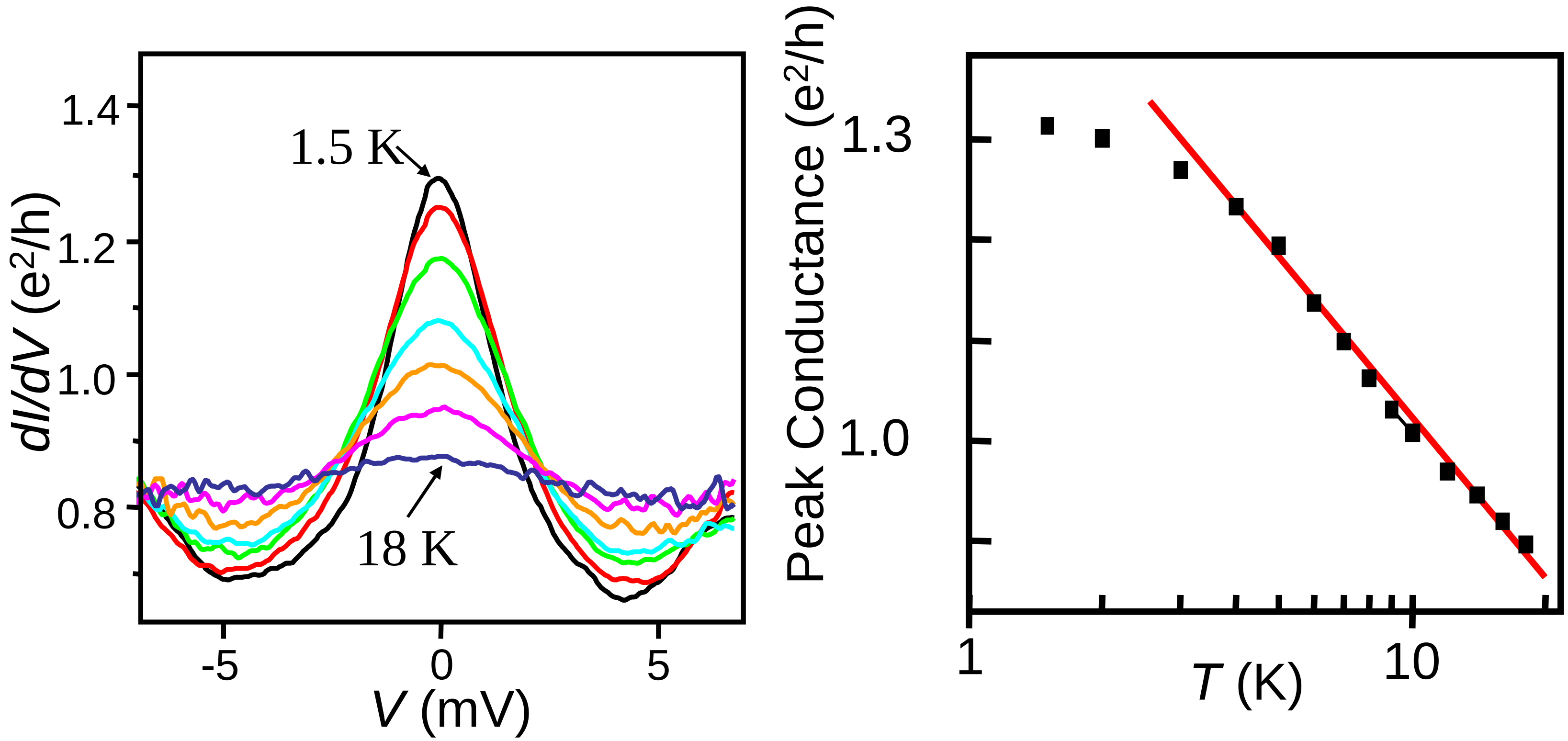

Figure 5.8: (a) dI/dV traces at different temperatures. (b) Peak conductance as a function of temperature showing logarithmic dependence.

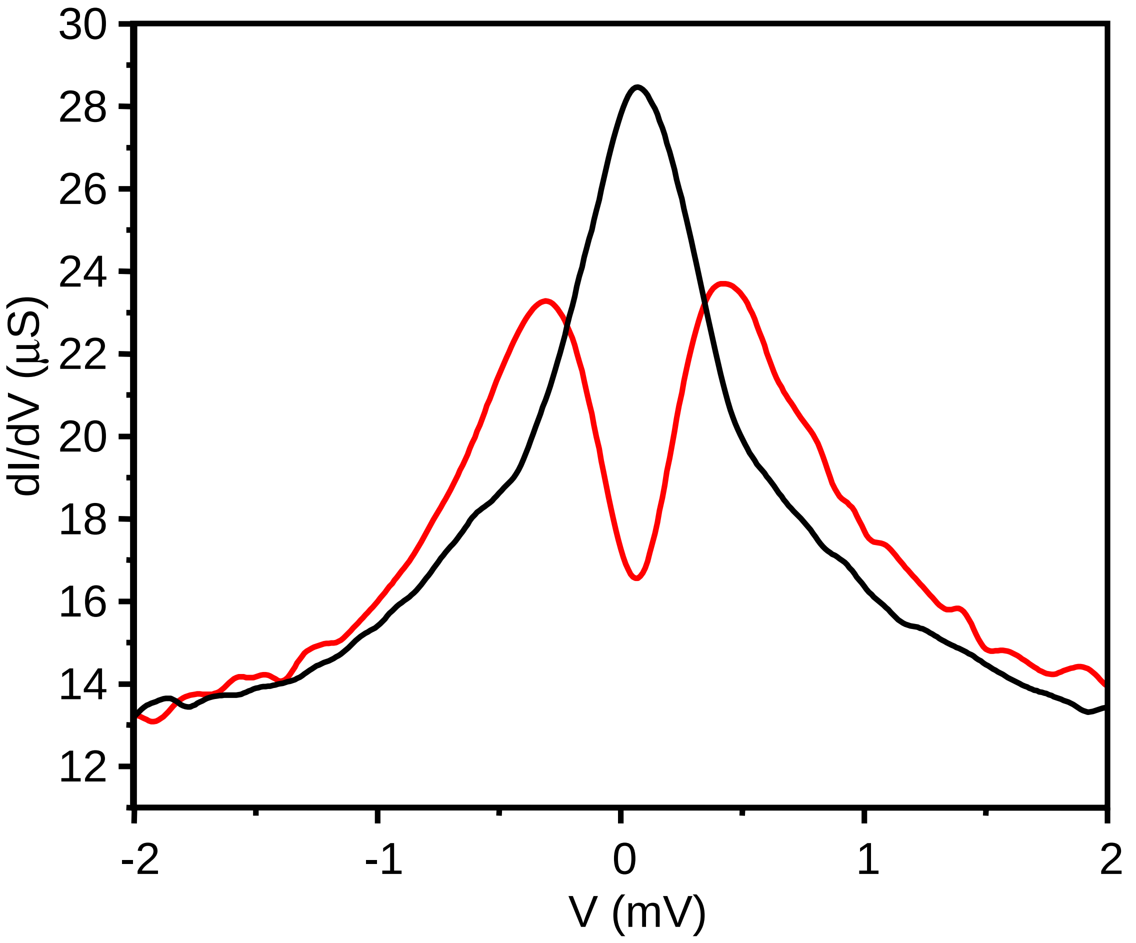

Figure 5.9: dI/dV trace at $H = 0$ (red curve) and $H = 2.5T$ (black curve) of an unusual device.

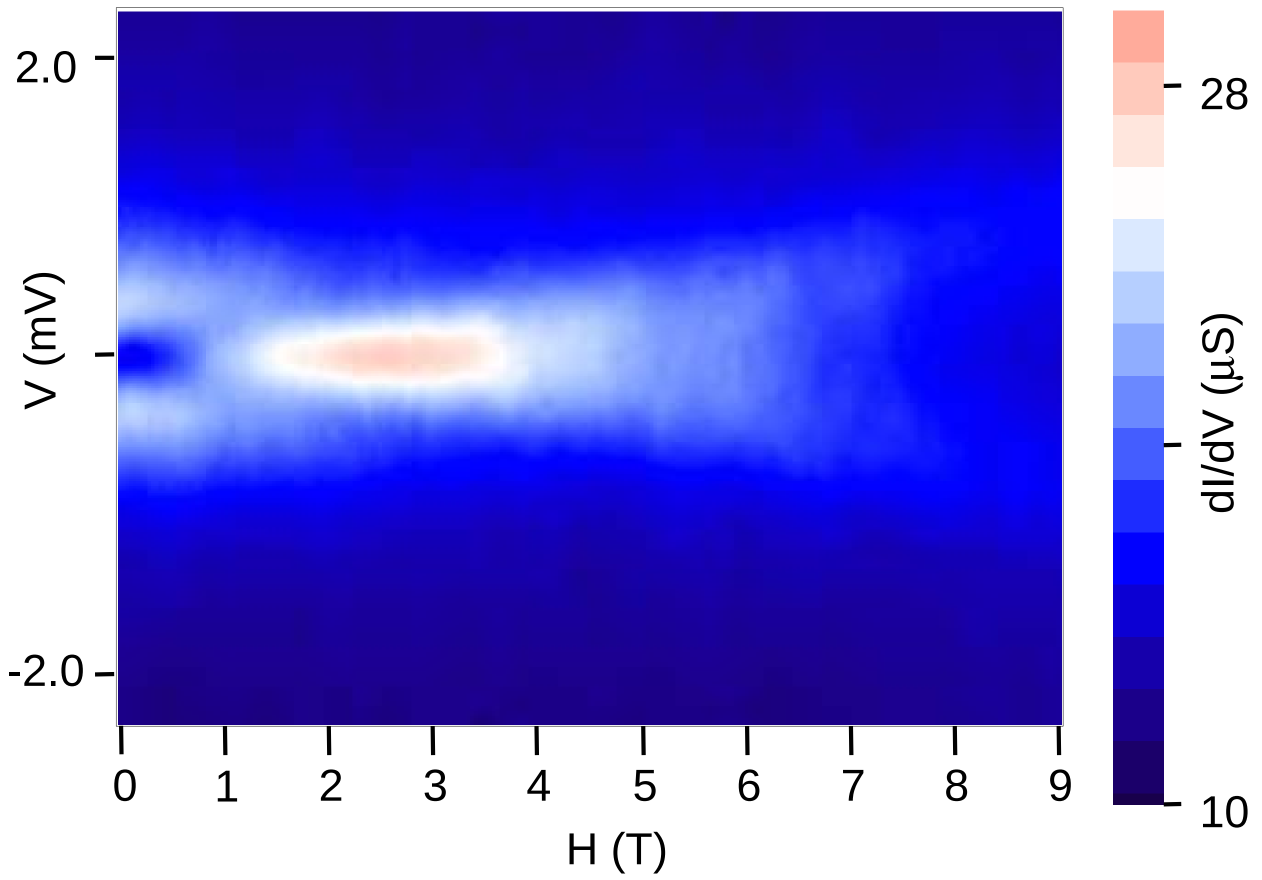

Figure 5.10: dI/dV plot for the same device as fig. 5.9.

Another possibility is the case considered by Hofstetter and Schoeller [28]. They consider a quantum dot with two spins that is close to the singlet-triplet degeneracy. The Hamiltonian used in [28] is $H = H_L + H_R + H_D + H_T$. This Hamiltonian contains two leads $H_r = \sum_{kr} \epsilon_{kr} a^\dagger_{k\sigma r} a_{k\sigma r}$ with $r = L/R$. The isolated dot is described by

$$H_D = \sum_{n\sigma} \epsilon_{dn} d^\dagger_{n\sigma} d_{n\sigma} + J\,\mathbf{S}_1\,\mathbf{S}_2 + U\,(N - \mathcal{N})^2 + g\mu_B H S_z \tag{5.14}$$

where $n = 1, 2$ denotes the two levels, $N = \sum_{n\sigma} d^\dagger_{n\sigma} d_{n\sigma}$ is the total number of electrons occupying the dot and $\mathbf{S}_n = (1/2)\sum_{\sigma\sigma'} d^\dagger_{n\sigma}\sigma_{\sigma\sigma'} d_{n\sigma'}$ are the spins of the two levels. The charging energy is U and an exchange coupling J has been introduced which arises due to Hund's rule. $\mathcal{N} = 2$ in order to achieve double occupancy of the dot. Through the energies ϵ_{dn} the level spacing $\Delta\epsilon = \epsilon_{d1} - \epsilon_{d2}$ as well as the precise position in the Coulomb blockade valley can be tuned. As a consequence of Hund's rule, the intra–dot exchange is ferromagnetic ($J < 0$).

Walter Hofstetter has used this model to fit to our data in fig. 5.10. Our data can be well explained by his model, assuming that the ground state is the singlet. The nonequilibrium Kondo peak occurs at the difference in energy between the singlet and triplet states. On applying a magnetic field, the singlet and the $S_z = 0$ triplet state are unaffected, but the $S_z = -1$ triplet state is lowered in energy. The $V = 0$ Kondo peak is restored when the $S_z = -1$ triplet state becomes degenerate with the singlet state. On further increasing the magnetic field, the Kondo peak is once again split, with the splitting governed by the energy difference between the $S_z = -1$ triplet state and the singlet state. The theory plots are shown in fig. 5.11, which can be used to match the experimental data in fig. 5.10 quite well.

The only problem with all of this is that according to our original story (chapter

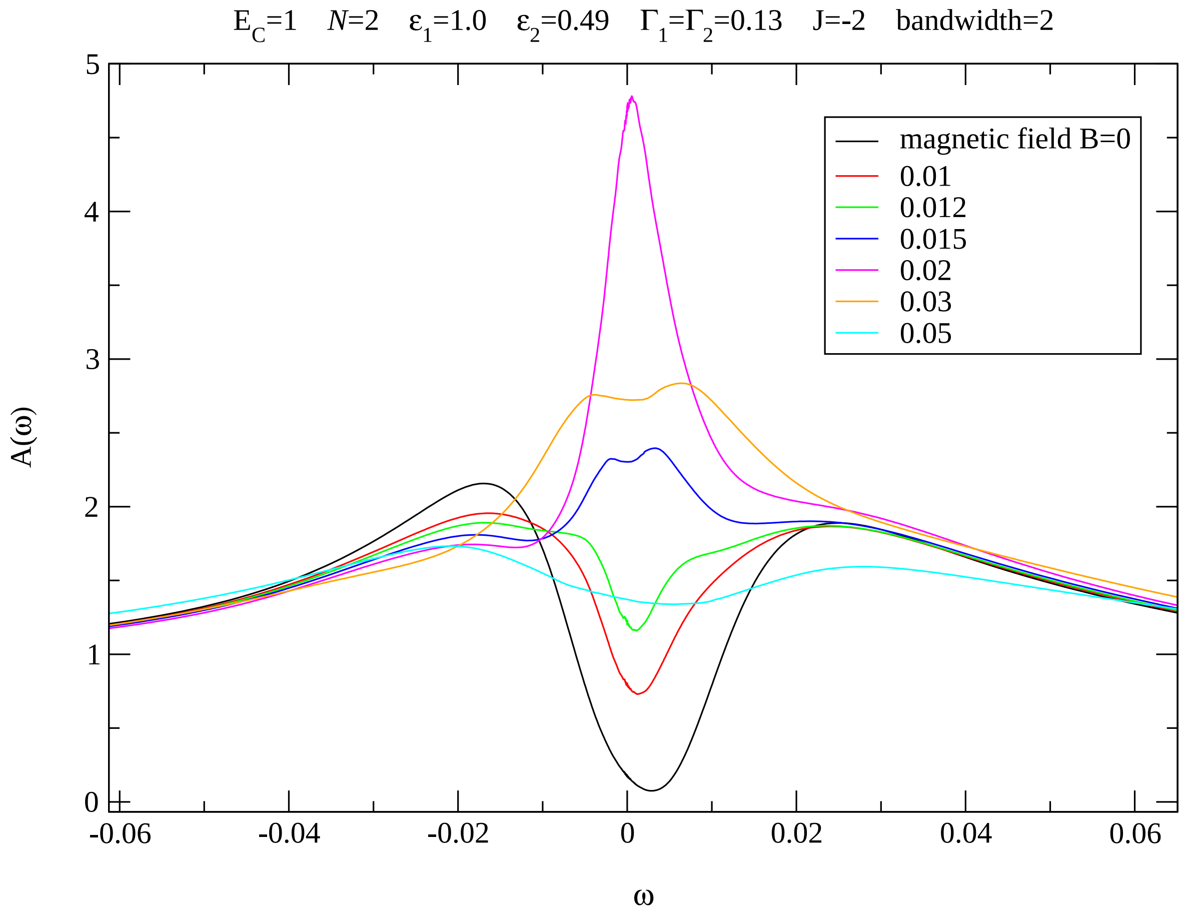

Figure 5.11: Spectral function for the two-spin Kondo model [28].

4, there is no $S = 1$ state of our molecule. The Co^{1+} state has been seen in electrochemistry [29]. However, even if we are seeing the Co^{1+} state in this device, it is tough to imagine it existing in the singlet state since the exchange energies in atoms are at least many 10's of meV. We have to conclude that the object measured in this device is something more complicated than the simple picture of one $Co - (tpy - SH)_2$ molecule between gold electrodes.

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Chapter 6

Vibration assisted tunneling in C_{140} single-molecule transistors

6.1 Introduction

In chapter 4, we saw excited levels in tunneling spectroscopy that we attributed to vibrational modes of the $Co-(tpy-(CH_2)_5-SH)_2$ molecule. In general, it is well known by now that when electrons travel through molecules, vibrational modes of the molecules can affect current flow. Molecular-vibration-assisted tunneling was first measured in the 1960's using devices whose tunnel barriers contained many molecules [1]. Effects of vibrations in single molecules have been measured using a scanning-tunneling microscope [2], mechanical break junctions [3] as well as single-molecule transistors made using the electromigration technique [4, 5]. Theoretical considerations suggest that different regimes may exist depending on whether tunneling electrons occupy resonant energy levels on the molecule, and also on the relative magnitudes of the rate of electron flow, the vibrational frequency, and the damping rate of vibrational energy [6, 7, 8, 9, 10, 11, 12, 13, 14, 15].

A quantitative analysis of electron-vibration interactions has been difficult to achieve in previous molecular-transistor experiments. In [5] (chapter 4), neither the precise nature of the vibrational modes nor their energies was determined independently of transport measurements. In [4], the "bouncing-ball" mode of a single C_{60} molecule against a gold surface was observed, a mode not intrinsic to the molecule itself. We therefore set out to make transistors from a molecule that has a small number of well-characterized vibrational modes at low energy. In this chapter we study single-molecule transistors made using a molecule, C_{140}, with low-energy internal vibrational modes that are well understood. We observe clear signatures of one of these modes and discuss theoretically why it has the strongest coupling to tunneling electrons.

6.2 Synthesis and characterization

The C_{140} molecule consists of two C_{70} balls joined by two covalent C-C bonds (schematic in fig. 6.1(a)). The C_{140} we use was synthesized by pressure treatment of polycrystalline C_{70} at 1 GPa and 200 °C, purified by chromatography and characterized by C^{13} NMR, Raman and infrared spectroscopy [16]. The vibrational modes of C_{140} have been measured by Raman spectroscopy and modeled numerically [16]. The six lowest-energy modes of C_{140} are not seen for C_{70}. They are intercage vibrations in which each C_{70} ball moves approximately as a rigid unit. Theoretical calculations (fig. 6.1(c)) show them to be at 2.5, 2.7, 4, 11, 15, and 17 meV. In fig. 6.1(b) we show Raman spectra for C_{70} before and after the dimerization procedure. The spectrum of the purified dimer shows the presence of the intercage modes at 11, 15 and 17 meV (the other modes have energies to small to be observed using Raman spectroscopy), with the stretching mode at 11 ± 0.5 meV being observed most prominently. The other intercage modes involve bending or twisting of the molecule. The lowest intracage excitation of C_{70} is 29 meV. [18].

We have also made transistors from C_{70} (schematic in fig. 6.1(a)). We bought

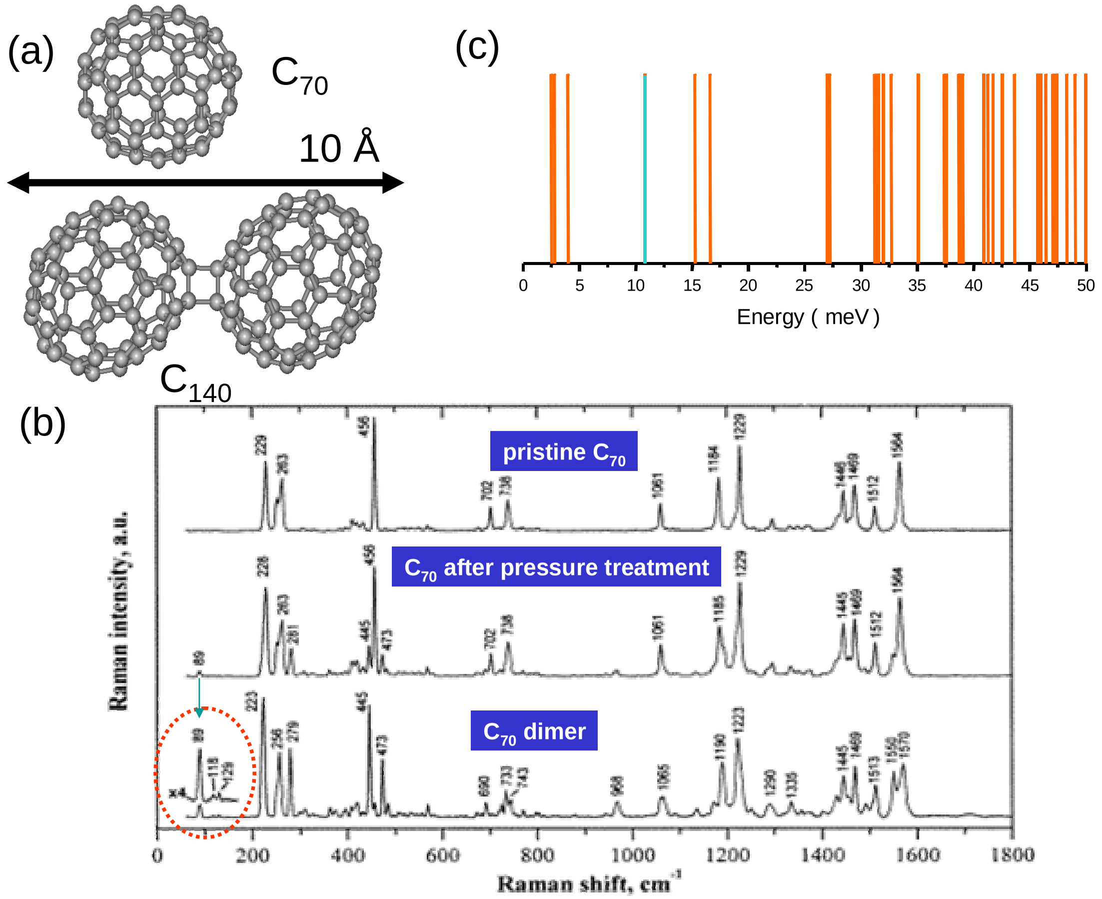

Figure 6.1: (a) Schematic of C_{140} and C_{70} (b) Raman spectra of C_{70} and C_{140} from [16]. The intercage modes are circled. Green arrow - stretch mode (c) Vibrational modes calculated by Gaussian03/PM3 [17]

this material (99.9% purity) from Alfa Aesar [19] and used it without further purification.

6.3 Devices

An atomic force microscope image of our transistor structure is shown in fig. 6.2(a). At least one C_{140} molecule bridges source and drain electrodes that are about 1 nm apart, with capacitive coupling to a gate electrode. We use an aluminum gate electrode as described in chapter 2 section 2.3. Our nanowire is made of 20 nm gold with 2-3 nm of Cr as an adhesion layer, or a platinum wire without the adhesion layer. We then deposit approximately 10 μl of a 100 μM solution of C_{140} molecules in o-dichlorobenzene onto the device, and we allow the solvent to evaporate or we blow dry after approximately 10 minutes. After the molecules are deposited, we cool to cryogenic temperatures and use electromigration to create a nm-scale gap in the wire within which a molecule is sometimes trapped [4, 5, 20, 21]. The success rate for incorporating a molecule is approximately 10% for both the gold and platinum wires. The orientation of the molecule in the device is not known. All the measurements were performed either at 1.5 K or below 100 mK.

In fig. 6.2(b), we show several current versus bias voltage (I-V) curves measured from a C_{140} device at different gate voltages (V_g). The device exhibits Coulomb-blockade behavior, like the case of $Co-(tpy-(CH_2)_5-SH)_2$ (section 4.3). Plots of dI/dV as a function of V and V_g are shown in fig. 6.3(a) for four of the fourteen C_{140} devices we have examined. The dark areas on the left and right of each plot are regions of Coulomb blockade. The blockade energy barrier can be tuned with

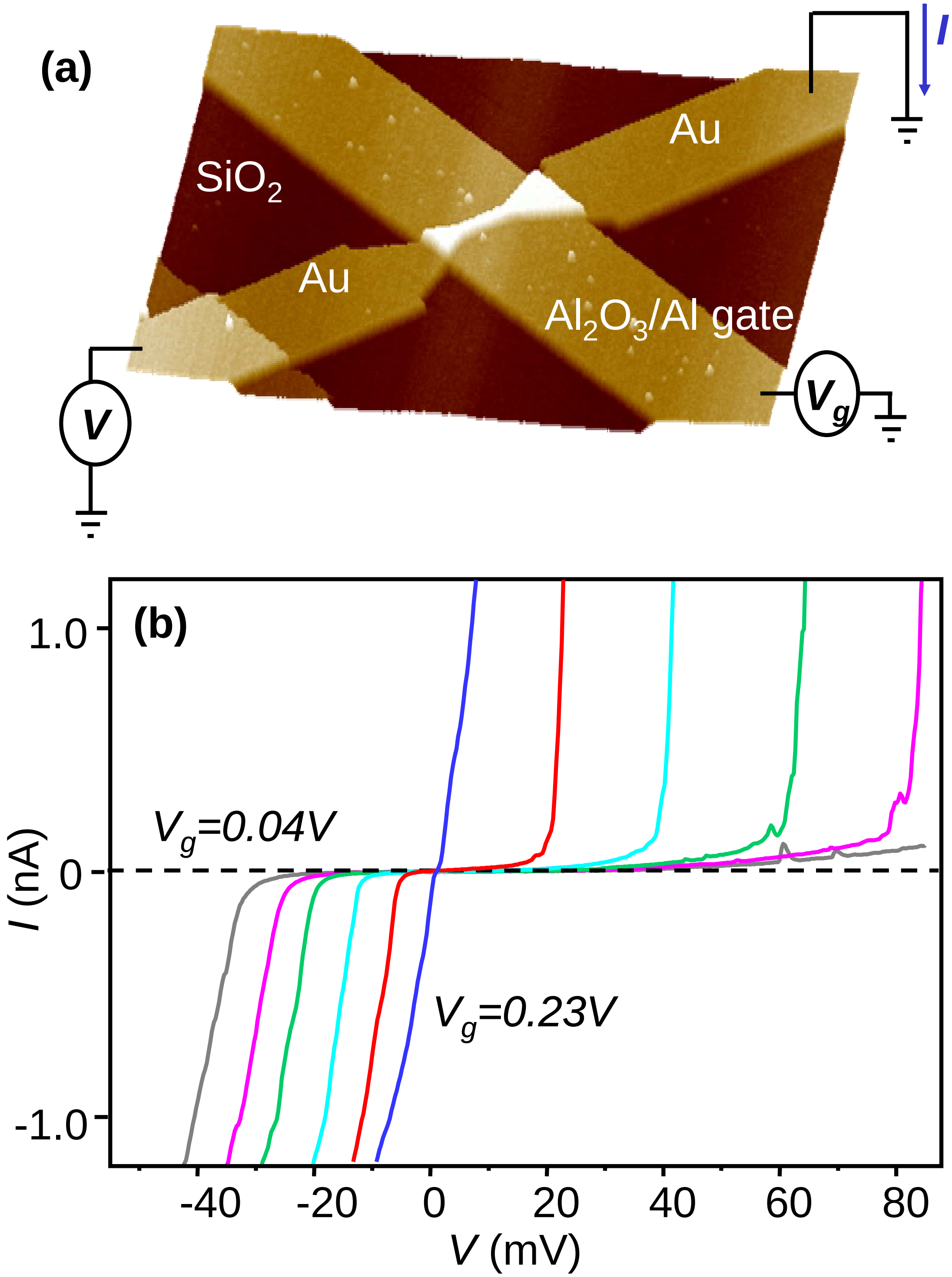

Figure 6.2: (a)AFM image of a gold nanowire on an oxidized Al gate (b) I-V curves at 1.5 K of a C_{140} device at equally-spaced gate voltages.

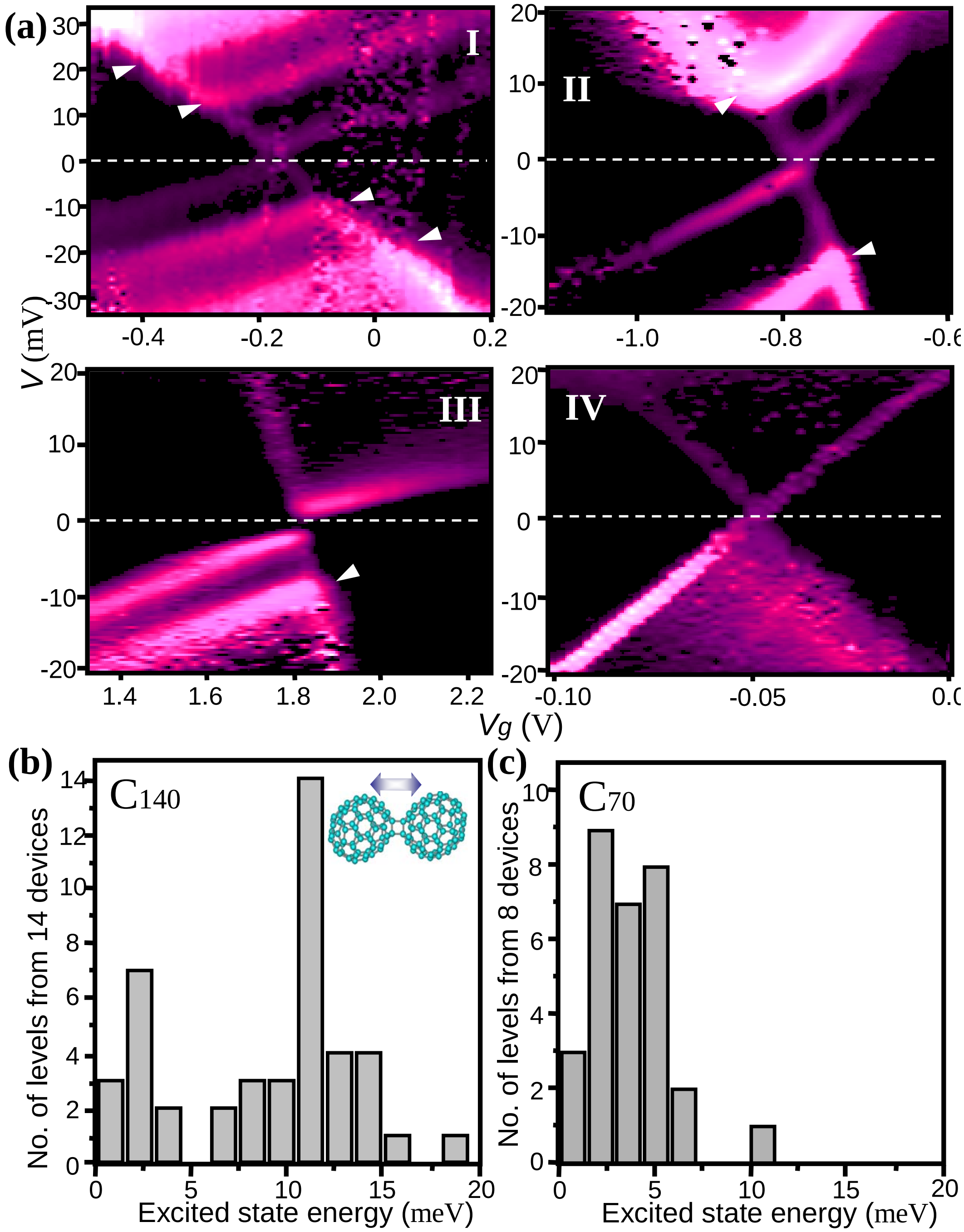

Figure 6.3: (a) dI/dV plots for four C_{140} devices. White arrows - 11 meV and 22 meV levels. Maximum conductance is 200 nS (device I), 600 nS (II), 15 nS (III), and 100 nS (IV). Measurements were done at 1.5 K for I-III and 100 mK for IV. (b) A histogram of observed excited energies from 28 charge states in 14 C_{140} devices. (c) A similar histogram for 8 C_{70} devices.

V_g to be > 200 meV, the measurement limit set by electrode stability and noise at high V. Tunneling can occur close to $V = 0$ only near one value of gate voltage, V_c, which varies from device to device because of variations in the local electrostatic environment. Each of the C_{140} devices reported has only one accessible degeneracy point V_c. As long as we perform measurements close to $V_g = V_c$ we can be confident that the current flows through only a single charge state within one nanoscale object. While we cannot in principle rule out transport via a quantum state delocalized over a small number of C_{140} molecules, we see no nm-scale clustering of molecules when imaged by AFM. If we make devices using C_{140} solutions 100 times more concentrated, we commonly observe independent parallel tunneling through two or more molecules, as indicated by multiple degeneracy points at different V_g, with conductance signals indicating different ratios of capacitance to the source and drain electrodes.

The subject of this chapter concerns the excited levels that contribute to electron transport in these devices. As in chapter 4, the lines which meet the dark blockade area at $V_g < V_c$ ($V_g > V_c$) correspond to excited quantum levels of the $V_g < V_c$ ($V_g > V_c$) charge state. The energy of each level can be read off from the bias voltage where the dI/dV line intercepts a boundary of the blockade region (white arrows).

In fig. 6.3(b), we plot a histogram of all of the excited-state energies that we resolve below 20 meV in fourteen C_{140} devices; excitations in each charge state are recorded separately. An excitation at 11 ± 1 meV is seen in eleven of the fourteen devices. In seven devices, the 11 meV line is present for both of the accessible charge states, while in four others it is seen for only one. In one sample (device I), well-resolved excited levels are also observed near 22 meV for both charge states, twice the 11 meV energy. As a control experiment, we measured eight devices made with C_{70} molecules. No prominent peak near 11 meV is present in the histogram of C_{70} levels (fig. 6.3(c)).

The presence of the 11 meV excitation in C_{140}, but not C_{70}, indicates that it is an excitation of the entire molecule, and not the C_{70} sub-units. The presence of the same excitation for different charge states of the same molecule, and the observation of an excitation at 2×11 meV in one device, strongly suggest that the 11 meV excitation is vibrational in nature. A purely electronic excitation should not be the same in both charge states nor should it appear as multiples of a fundamental excitation. Based on its energy, we identify this excitation with the intercage stretch mode of C_{140} [16].

As shown in figs. 6.3(b) and 6.3(c), additional excitations are present below 5 meV in both the C_{140} and C_{70} devices. For C_{70}, these are likely associated with the bouncing-ball mode of the molecule, as demonstrated previously for C_{60} [4]. The sub-5-meV excitations in C_{140} devices might arise either from similar bouncing modes or the intercage modes of C_{140} at 2.5, 2.7 and 4 meV. However, calculations (below) suggest that of the six intercage modes, the tunneling electrons couple strongly only to the stretch mode and not the other internal modes. We do not observe peaks in the C_{140} histogram near the bending/twisting intercage modes at 15 and 17 meV.

6.4 Franck-Condon model

We will analyze our data within the framework of the Franck-Condon model [22]. C_{140} has a large number of vibrational states we denote by α_j, where α labels the mode of frequency ω_α and j is the number of vibrational quanta excited in the mode. For each vibrational mode, the tunneling electron drives a transition from the ground vibrational state with A electrons to a vibrational state α_j with B electrons, where $B - A = +1(-1)$ for tunneling on (off) the molecule. The tunneling rate is determined by the overlap of the starting configurational wavefunction, Ψ_g^A, with the one after tunneling, $\Psi_{\alpha_j}^B$:

$$\Gamma_{\alpha_j}^{A \to B} = \Gamma_{electron} P_{\alpha_j}, \tag{6.1}$$

where

$$P_{\alpha_j} = \langle \Psi_{\alpha_j}^B | \Psi_g^A \rangle^2, \tag{6.2}$$

and

$$\sum_j P_{\alpha_j} = 1. \tag{6.3}$$

If the electronic contribution $\Gamma_{electron}$ is assumed constant for the different vibrational transitions and if the rate-limiting step for current flow is the $A \to B$ transition, the current step associated with a given vibrational excitation is:

$$\frac{\Delta I_{\alpha_j}}{\Delta I_g} = \frac{P_{\alpha_j}}{P_g}. \tag{6.4}$$

Here ΔI_g is the ground state current. In order to predict the size of the current steps, we must therefore calculate the atomic rearrangements that occur when a charge is added to or subtracted from the molecule. We will first perform this calculation for an isolated C_{140} molecule and then discuss effects of the local electrostatic environment, before making comparisons to our measurements.

For the isolated molecule, we calculated the overlaps P_{α_j} using the semi-empirical method PM3 under Gaussian 03 [17]. The charge state of C_{140} in our devices is not known, but since the fullerenes are easily reduced and not easily oxidized [23], we have analyzed the initial charge states $n^- = 0, 1^-, 2^-$ and 3^-. The PM3 calculations indicate that the probability of tunneling without exciting any of the vibrational degrees of freedom is small. This means that tunneling at low biases is suppressed. The coupling is distributed over all of the vibrational modes, but it is large for a relatively small number. Within our measurement range ($eV < 30meV$) the calculations indicate that the coupling is dominated by a single mode, the 11 meV stretching mode ($\alpha = s$). For the $0 \rightarrow 1^-$ transition,

$$\frac{P_{s1}}{P_g} = 0.25. \tag{6.5}$$

Couplings to all other vibrational modes in the measurement range are found to be smaller by at least a factor of 10. The results are qualitatively similar for other charge states.

The physics of the 11 meV stretching mode can be captured using a simple model of the molecule with two masses $M/2$ connected by a spring with a spring constant k, as illustrated in fig. 6.4. The vibrational frequency is

$$\omega_s = \sqrt{\frac{4k}{M}}. \tag{6.6}$$

The zero-point rms amplitude of fluctuations in the vibrational coordinate is [22]

$$x_0 = \sqrt{\frac{2\hbar}{M\omega}} = 2 \text{ pm}. \tag{6.7}$$

The length of the molecule changes by Δx when one charge is added. The Franck-Condon result for the transition probability associated with one quantum of the

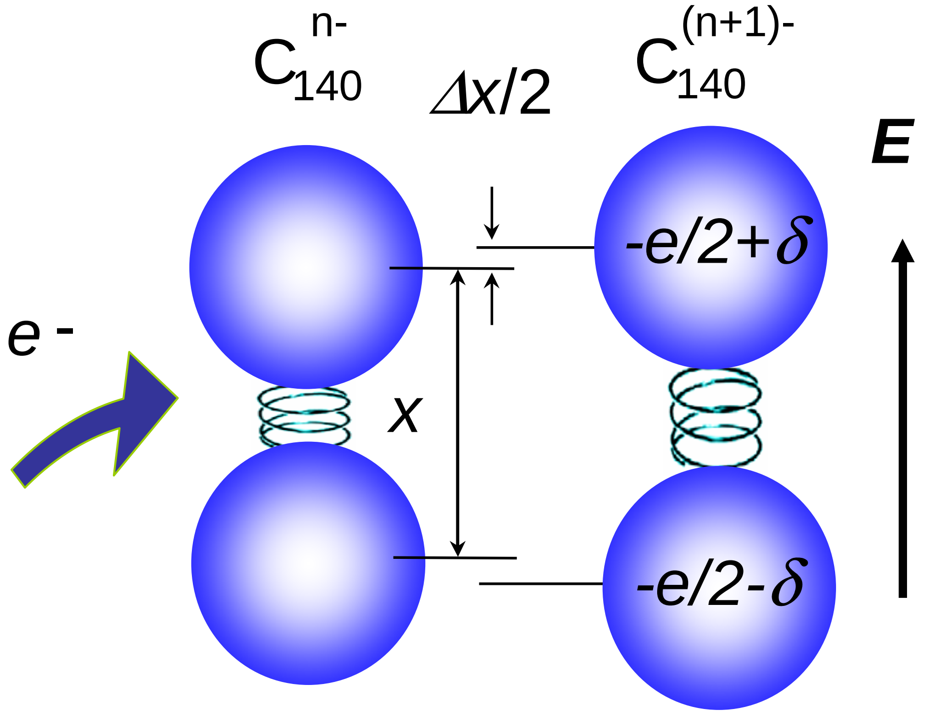

Figure 6.4: Cartoons illustrating the 11 meV mode. On the left is the 1-d cartoon of the 11 meV mode - two C_{70} units attached by a spring. On adding a charge, an extra electric field acts on the molecule due to the interaction with the environment (right). This in turn stretches the molecule.

stretching mode, normalized by the ground-state probability, is

$$\frac{P_{s1}}{P_g} = \left(\frac{\Delta x}{2x_0}\right)^2. \tag{6.8}$$

Higher-order transitions involving j quanta of a vibrational mode have rates related to the one-quantum transitions [22]:

$$\frac{P_{sj}}{P_g} = \frac{1}{j!}\left(\frac{P_{s1}}{P_g}\right)^j. \tag{6.9}$$

In going from the neutral to 1^- charge state for isolated C_{140}, PM3 predicts that $\Delta x = -1.9$ pm. Equation 6.8 then gives

$$\frac{I_{s1}}{I_g} = 0.23. \tag{6.10}$$

This is in good agreement with the full calculation above. Multiple-quanta transitions should be much smaller by eqn. 6.9. For other charge states, the calculated strength of the transition assisted by the stretching mode is weaker, because Δx is smaller: for the $1^- \rightarrow 2^-$ transition $\Delta x = -0.4$ pm, for $2^- \rightarrow 3^-$ $\Delta x = -0.1$ pm, and for $3^- \rightarrow 4^-$ $\Delta x = -0.3$ pm.

The electrostatic environment in the neighborhood of the C_{140} molecule may also play an important role in determining vibration-assisted tunneling rates. In general, we expect that the C_{140} molecule will be subject to a strong local electric field $\mathbf{E}$ due to image charges, work-function differences, and/or localized charged impurities. For example, an image charge at a distance 0.8 nm away generates $\mathbf{E} = 2$ V/nm. We have not succeeded in making quantitative estimates of these field-enhancement effects because the Gaussian 03 implementation of PM3 does not allow for solutions in an external field. However, a local field can be expected to preferentially enhance vibration-assisted tunneling associated with the stretching mode. When an extra electron tunnels onto C_{140}, the presence of $\mathbf{E}$ will produce unequal charges on the two C_{70} cages, as illustrated in fig. 6.4. The rearrangement of charge density within the molecule will produce changes in chemical bonding forces, leading to changes in Δx. In addition, the interaction of $\mathbf{E}$ with the charge polarization (δ in fig. 6.4) will stretch the C_{140} by a length

$$\Delta x = \frac{\mathbf{E}}{k}. \tag{6.11}$$

To estimate the magnitude of this stretching, assume that the charge is fully polarized: $\delta = e/2$, and $\mathbf{E} = 2$ V/nm. Then the electrostatic stretching is $\Delta x \approx 1pm$. Both this stretching and the chemical-bonding rearrangement might produce displacements of comparable magnitude to the values calculated above for isolated C_{140}. Such electric-field effects should depend strongly on the angle between the field and the molecular axis, because C_{140} is most easily polarized along its long axis.

6.5 Experimental current magnitudes and anomalies

Figure 6.5 shows the measured ratio I_{s1}/I_g for both charge states and of each device, determined by taking the ratio of the current-step height at the 11 meV peak to the current just before the step. An increasing overall background was also observed that gives uncertainties in the step heights. In five of the devices (I, II, V, VIII, and X), the ratios were the same to within experimental uncertainty in both charge states, as expected within the simple Franck-Condon picture if the vibrational energies are not altered significantly by the addition of an electron. In three of these devices, $\frac{I_{s1}}{I_g} < 0.6$, small enough to be consistent with the PM3

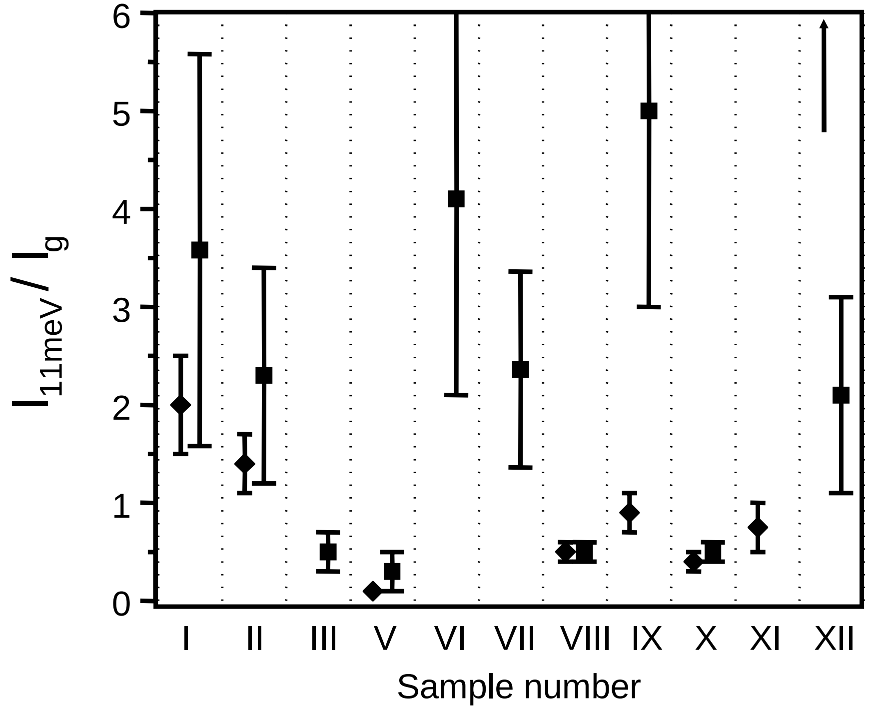

Figure 6.5: Values of I_{11meV}/I_g, the measured current step for the 11 meV signal relative to the ground-state. Values for n^- (squares) and $(n+1)^-$ (diamonds) are shown. One value is not displayed: for device XII, $I_{11meV}/I_g = 8 \pm 2.5$ for the $(n+1)^-$ charge state. Samples IV, XIII, and XIV have no visible 11 meV levels.

estimates above. Only the $j = 1$ vibrational state was observed for these three devices, in agreement with theory. For device I, $\frac{I_{s1}}{I_g} = 3.6 \pm 2.0$ and 2.0 ± 0.5 for the n^- and $(n+1)^-$ state respectively, indicating stronger coupling than expected from our estimate for isolated C_{140}. For this sample, additional lines were observed corresponding to the emission of two vibrational quanta ($j = 2$) with amplitudes $\frac{I_{s2}}{I_g} = 7.3 \pm 4$ for the n^- charge state and 2.3 ± 1.5 for the charge state. Equation 6.9 predicts 6.5 ± 4 and 2 ± 1 respectively, in good agreement with the measurements. For device II, strong coupling was also observed, but no $j = 2$ line was resolved, although the increasing background may have masked its presence. Overall, then, this subset of five devices is in reasonable agreement with the Franck-Condon predictions.

In the other devices showing an 11 meV feature, we observed behaviors that are unexpected in our simple Franck-Condon picture. Large differences were observed in $\frac{I_{s1}}{I_g}$ for the two charge states; sometimes a line was present for only one charge state (devices III, VI, VII, and XI). In addition, anomalously large values of $\frac{I_{s1}}{I_g}$ were observed. These could either reflect strong electron-phonon coupling or an anomalous suppression of tunneling into the ground state by vibrational or other phenomena.

One device (VI) showed a number of rather peculiar features. Firstly, it showed pronounced negative differential resistance at some bias and gate voltages [8, 9]. Negative differential resistance in single-electron transistors usually happens when there is a current-blocking mechanism that is accessed beyond the ground state - for example an excited state with very asymmetric couplings [24]. I cannot think of a simple explanation for why this should happen in a C_{140} single-molecule device.

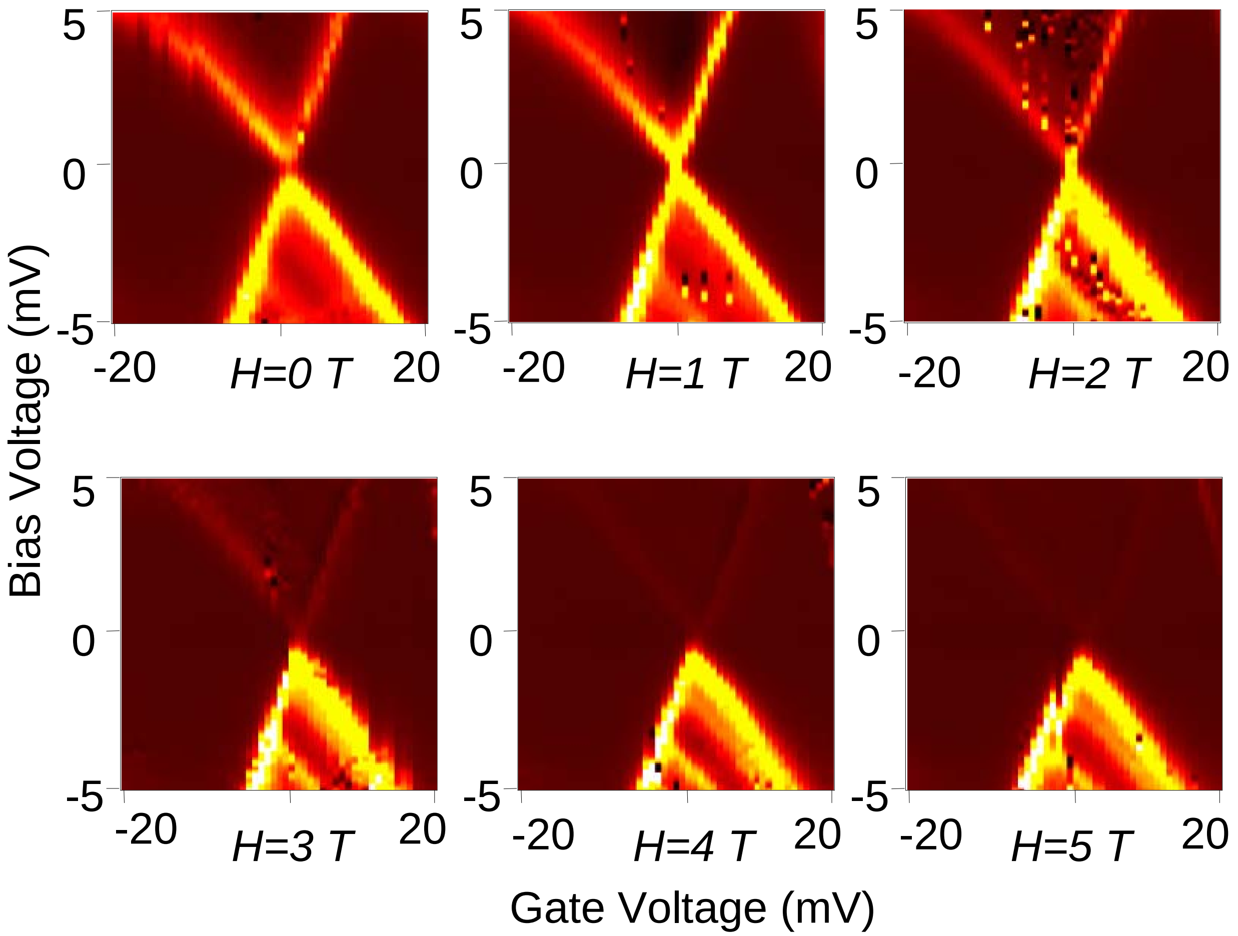

Figure 6.6: dI/dV plots of device VI at different magnetic fields. The maximum conductance is 1 μS.

Further, device VI showed strange behavior on applying a magnetic field. Shown in fig. 6.6 are a sequence of dI/dV plots at increasing magnetic fields (all the plots have the same colorscale). It is evident that the current is suppressed heavily for one sign of the bias voltage, but not for the other. I cannot think of *any* explanation (forget about a simple one) for this behavior in a C_{140} single-molecule transistor.

6.6 Summary

In summary, in transistors made from C_{140} we observe vibration-assisted tunneling associated with an internal stretching mode of the molecule. The strong coupling of this mode to tunneling electrons, relative to the other molecular modes, is consistent with molecular modeling. Variations in the measured strength of vibration-assisted tunneling between different devices may be associated with an enhancement of the coupling between tunneling electrons and stretching-mode excitations by local electric fields.

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Chapter 7

The Kondo effect in the presence of ferromagnetism

7.1 Introduction

Measurements on individual quantum dots have in recent years provided a detailed understanding of the Kondo effect [1, 2, 3, 4, 5, 6, 7], the coupling between a localized spin and conduction electrons that serves as a fundamental model for understanding correlated-electron physics [8]. Itinerant-electron ferromagnetism is an alternative correlated-electron state that can arise from Coulomb interactions between electrons. These two states ordinarily compete with each other – in heavy fermion systems a phase transition is thought to exist between the Kondo and magnetic ground states [9]. Calculations for the consequences of coupling between a Kondo-regime quantum dot and ferromagnetic electrodes have produced conflicting predictions [10, 11, 12, 13, 14]. Experimentally, Kondo physics has not previously been studied in quantum dots with magnetic electrodes, despite work with both normal-metal [1, 2, 3, 4, 5, 6] and superconducting [7] systems, because of difficulty in achieving sufficiently strong coupling between the dot and magnetic materials. In this chapter we demonstrate that C_{60} molecules can be strongly coupled to nickel electrodes so as to exhibit the Kondo effect. Ferromagnetism can suppress Kondo-assisted tunneling, but Kondo correlations are still present within the ferromagnetic electrodes and in particular situations the strong-coupling limit of the Kondo effect can still be achieved.

7.2 Fabrication

We will compare measurements made using (magnetic) nickel and (non-magnetic) gold electrodes. These experiments build upon studies of single-electron transistors made using C_{60} [15] and previous measurements of Kondo-assisted tunneling using C_{60} in contact with gold electrodes [6]. Our devices are made by using electron-beam lithography and liftoff (using the same procedure as chapter 2) to create electrodes that are 30 nm high and 50 nm wide at their narrowest point. After cleaning the electrodes in an oxygen plasma (0.25 W/cm^2 for 2 min), we deposit 50 μl of a dilute solution ($\approx$ 100 μM) of C_{60} in toluene over a 30 mm^2 area of the chip and allow the solvent to evaporate. We cool the chip to 1.5 K and then use an electromigration procedure [16] to create a nanometer-scale break in the wire. One or more molecules of C_{60} can bridge this gap.

7.3 Devices

We first describe results for C_{60} with non-magnetic gold electrodes. After electromigration, some samples show featureless tunnel conduction or conventional high-resistance Coulomb-blockade characteristics [15], but in approximately 20% of 100 junctions the differential conductance ($G(V) \equiv dI/dV \equiv 1/R(V)$) curves display a peak at $V = 0$, as shown in fig. 7.1(a) [6]. This peak can be split by applying a magnetic field B, with an average g factor ≈ 2. These features are

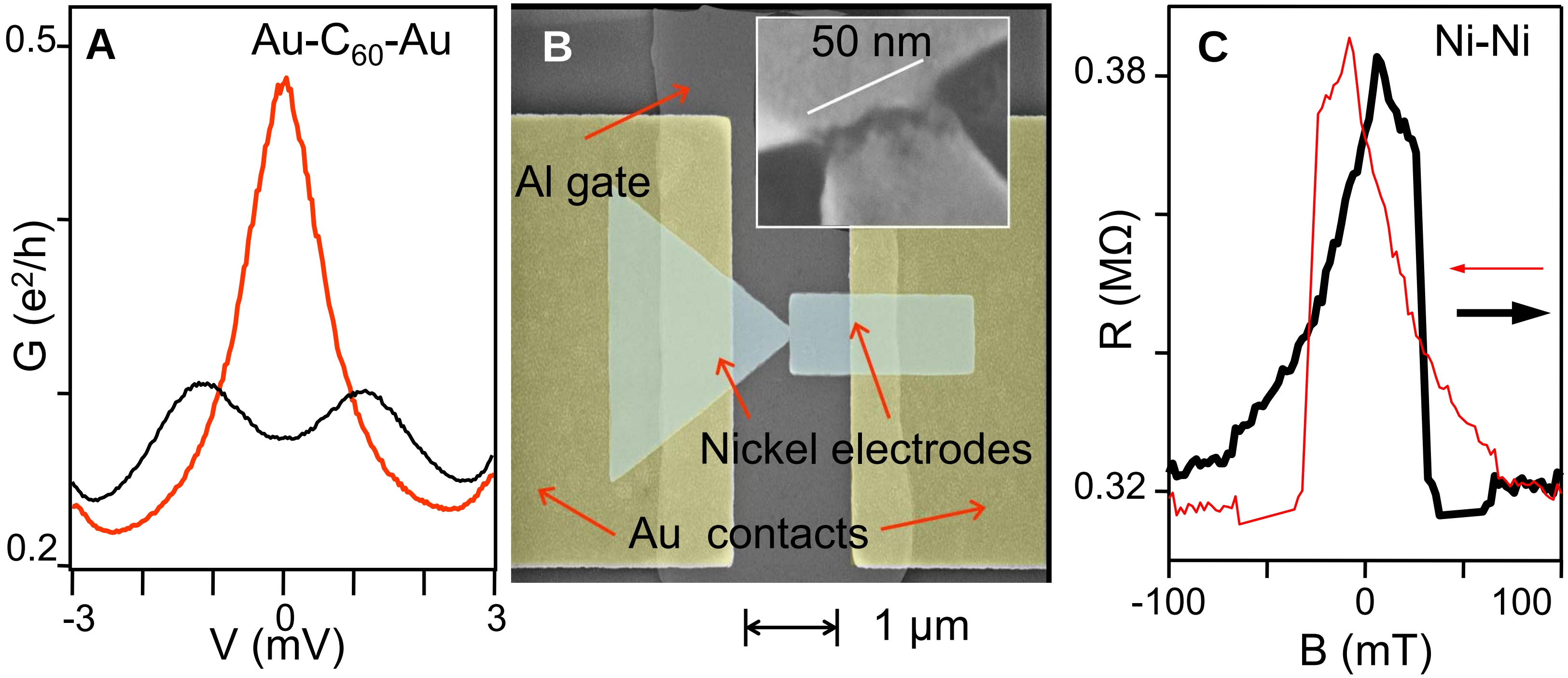

Figure 7.1: (a) Kondo signal for C_{60} with Au electrodes at $T = 1.5$ K. At $B = 0$ (red line), there is a zero-bias peak in $G(V)$ that becomes split for $B = 10$ T (black line). (b) SEM micrograph of a Ni break junction. (inset) close-up of the junction region after electromigration (c) Tunneling magnetoresistance near $V = 0$ at $T = 4.2$ K of a Ni contact after electromigration, with no C_{60} molecule present.

signatures of the Kondo effect in a spin-1/2 quantum dot [1, 2, 3, 4, 5, 6]. The Kondo signals were absent in a set of forty control samples that underwent the same fabrication procedure, but without the C_{60} deposition.

For magnetic Ni electrodes, we design the shapes of the two electrodes to give them different magnetic anisotropies, so that they undergo magnetic reversal at different values of B [17]. We have experimented with several combinations of shapes and have had good success with the pattern shown in fig. 7.1(b). We check the magnetic properties of test electrodes, in the absence of any molecules, by measuring the magnetoresistance of tunnel junctions created by electromigration (fig. 7.1(c)). The curves display hysteretic switching features familiar from previous studies of magnetic tunnel junctions [18], demonstrating that we can control the relative orientation of the magnetic moments in the two electrodes between parallel (P) and approximately antiparallel (AP) alignment. We can compare the magnitude of the junction magnetoresistance (JMR) to the Julliere estimate [19]:

$$\mathrm{JMR} \equiv \frac{R_{\mathrm{AP}} - R_{\mathrm{P}}}{R_{\mathrm{P}}} = \frac{2P^2}{(1 - P^2)}, \tag{7.1}$$

where R_{P} (R_{AP}) is the resistance when the magnetizations are parallel (antiparallel) and P is the tunneling spin polarization. Using $P = 0.31$ measured for thin films of nickel with aluminum-oxide tunnel barriers [20], the Julliere estimate is JMR = 21%. The sample shown in fig. 7.1(c) has JMR = 19%, and for other samples we find values in the range $10 - 19\%$.

After we perform electromigration on 1200 Ni samples with C_{60} adsorbed on them, about 5% of the devices exhibit simple high-resistance Coulomb-blockade characteristics [15]. In another 3% of the devices we observed $G(V)$ vs. V curves similar to figs. 7.2(a) and (c). Instead of having a single peak in $G(V)$ centered at $V = 0$ as observed for Kondo tunneling with Au electrodes, when the moments of the Ni electrodes were aligned parallel by a small applied field we observe two peaks in $G(V)$, approximately symmetric about $V = 0$ and with similar amplitudes and widths, situated atop a background that can be asymmetric in V. These characteristics are different from Coulomb-blockade conductance peaks [21].

7.4 Magnetization orientation dependence

Strikingly, the split peaks in fig. 7.2 display a strong dependence on the relative orientation of the magnetic moments in the two electrodes. Figure 7.2(b) shows a colorscale plot of $G(V, B)$ for sample #1 as a function of B (y-axis) and V (x-axis), recorded at 1.5 K. B is swept from negative to positive values. When $B < -10$ mT, there are two peaks in $G(V)$ with a splitting $\Delta V_{\mathrm{P}} = 16$ mV that displays only a weak dependence on B. At B = -10 mT there is an abrupt switch, at which point the splitting is reduced to $\Delta V_{\mathrm{AP}} = 7.6$ mV. In the range -10 mT $< B <$ 200 mT, the splitting between the peaks gradually increases. At $B = 200$ mT there is a second abrupt switching event, and the $G(V)$ curves for larger positive fields are the same as at large negative fields. When the sweep direction for B is reversed, the $G(V, B)$ plots exhibit magnetic hysteresis, with the switching fields reversed about $B = 0$. We can therefore associate these changes with the relative orientation of the moments in the two magnetic electrodes. For negative B in fig. 7.2(b) the moments are parallel and the peak splitting is large. At $B = -10$ mT one moment reverses to give an approximately antiparallel configuration with a smaller splitting. On further increasing B the other moment rotates gradually, and then at $B = 200$ mT the second moment reverses to restore the P configuration.

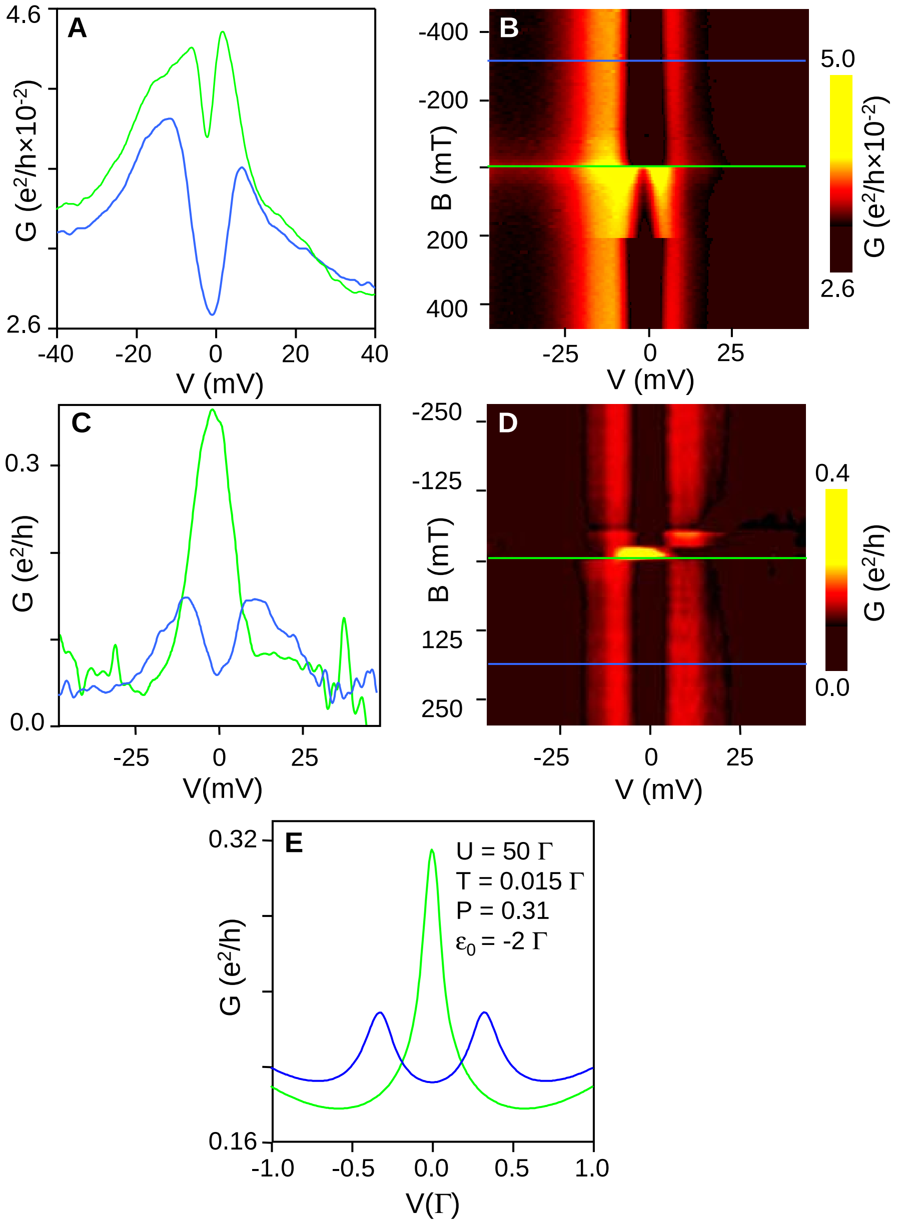

Figure 7.2: $G(V)$ curves at $T = 1.5$ K. (a) Sample #1: (blue) electrode magnetizations P, $B = -310$ mT; (green) magnetizations approximately AP, $B = -10$ mT. (b) Color-scale plot of $G(V)$ for sample #1 for B swept negative to positive. (c) Sample #2: (blue) magnetizations P, $B = -250$ mT; (green) magnetizations approximately AP, $B = 15$ mT. (d) Color-scale plot of $G(V)$ for sample #2 for B swept negative to positive. (e) Theoretical fit to (c) using the EOM method [10]. Here $\Gamma = (\Gamma_L + \Gamma_R)/2$

Fig. 7.2(c) and (d) show a similar progression as a function of B for sample #2. Again there is a large splitting, $\Delta V_{\mathrm{P}} = 18$ mV, for parallel moments in the electrodes, but in the AP configuration the splitting is reduced sufficiently that only one peak in $G(V)$ is resolvable. The lack of splitting for the AP case indicates that the strong coupling Kondo effect is possible even in the presence of ferromagnetic electrodes.

The splittings between the conductance peaks are too large to be associated with Zeeman splitting of the Kondo resonance in a local magnetic field. Assuming a g factor of 2, a splitting $\Delta V_{\mathrm{P}} = 16$ mV corresponds to a magnetic field of 70 Tesla. An upper limit on the local magnetic field that can be generated by the magnetic electrodes in the small gap is given by their magnetization, 0.6 T for Ni.

The magnetic-field dependence of our split peaks is in excellent agreement with some recent predictions that the interaction of a quantum dot with spin-polarized electrodes can produce a splitting of the Kondo resonance [10, 11, 12]. In this model, the conductance of a single-level quantum dot is determined by the tunneling spin polarizations $P_{\mathrm{L}}, P_{\mathrm{R}}$ and the couplings $\Gamma_{\mathrm{L}}, \Gamma_{\mathrm{R}}$ between the dot and the left and right electrodes. We will assume that polarizations are $P_{\mathrm{L}} = P_{\mathrm{R}} = P = 0.31$ (as for a Ni junction) for the P orientation and $P_{\mathrm{L}} = -P_{\mathrm{R}} = P$ for the AP orientation. Due to quantum charge fluctuations, the spin asymmetry in the coupling to the electrodes produces a spin-dependent renormalization of the dot's levels ϵ_σ, breaking the spin degeneracy: $\epsilon_\uparrow \neq \epsilon_\downarrow$. This results in a splitting of the $G(V)$ curve which (in the general case when an external field B is applied) has the value [11]

$$e\Delta V = 2 \left| g\mu_{\mathrm{B}} B + a \textstyle\sum_{r=\mathrm{L,R}} P_r \Gamma_r \right| \, . \tag{7.2}$$

Here μ_{B} is the Bohr magneton and a is a constant of order unity whose magnitude and sign depend on the charging energy U, ϵ_σ, and the detailed band structure [22]. If the magnetizations are AP and the dot has equal couplings to both electrodes $\Gamma_{\mathrm{L}} = \Gamma_{\mathrm{R}}$, the exchange interaction from the two electrodes are compensated. In this situation, the strong-coupling Kondo effect is restored despite the spin polarization in the leads, and the splitting is predicted to be reduced to zero near $B = 0$ (fig. 7.2(e)). However, when one takes into account that typically $\Gamma_{\mathrm{L}} \neq \Gamma_{\mathrm{R}}$, then the low-$B$ peak splittings in the P and AP orientations should be (assuming $\Gamma_{\mathrm{L}} > \Gamma_{\mathrm{R}}$)

$$\begin{aligned} e\Delta V_{\mathrm{P}} &= 2aP(\Gamma_{\mathrm{L}} + \Gamma_{\mathrm{R}}), && (7.3) \\ e\Delta V_{\mathrm{AP}} &= 2aP(\Gamma_{\mathrm{L}} - \Gamma_{\mathrm{R}}). && (7.4) \end{aligned}$$

These results are consistent with our measurements of larger splittings for parallel moments and smaller but generally non-zero splittings in the AP case [23].

For sample #1, fig. 7.2(b), equations (7.3) and (7.4) together provide an estimate for the tunnel coupling ratio $\Gamma_{\mathrm{L}}/\Gamma_{\mathrm{R}} = (\Delta V_{\mathrm{P}} + \Delta V_{\mathrm{AP}})/(\Delta V_{\mathrm{P}} - \Delta V_{\mathrm{AP}}) \approx 3$. If we pick a typical value of $aP \approx 0.15$ [10, 11, 12] we can estimate $\Gamma_{\mathrm{L}} \approx 45$ meV, $\Gamma_{\mathrm{R}} \approx 15$ meV. For sample #2, for which no splitting was resolved in the AP state, we can set the limit $\Gamma_{\mathrm{L}}/\Gamma_{\mathrm{R}} < 2$, with $\Gamma_{\mathrm{L}}, \Gamma_{\mathrm{R}} \approx 30$ meV. These numbers will change according to the value of aP assumed, according to eqn. (7.2). To obtain other estimates of device parameters, we have performed theoretical fits of $G(V)$ using the equations-of-motion (EOM) technique [10]. A plot for sample #2 in the parallel (solid) and antiparallel (dashed) magnetization orientations is shown in fig. 7.2(e). The parameters used are $\epsilon_0 = -60$ meV, $\Gamma = 30$ meV and $U = 1.5$ eV . The fits are relatively insensitive to changes in U by up to an order of magnitude.

Γ is determined to about a factor of two once $P_{\mathrm{L}}, P_{\mathrm{R}}$ are set. Values of the same order of magnitude are extracted for sample #1.

7.5 Temperature and high magnetic field

Further confirmation that the split peaks in $G(V)$ are associated with Kondo physics comes from their dependence on T and B. In order to measure changes at cryogenic temperatures and laboratory magnetic fields, one must focus on samples with narrow-in-V conductance peaks, associated with small Kondo temperatures (T_{K}) (fig. 7.3). Theory indicates that the T dependence of the peak conductance around T_{K} should be approximately logarithmic even when the Kondo resonance is split [24]. This is what we observe, for both parallel (fig. 7.3(a), sample #3) and antiparallel (fig. 7.3(b), sample #4) alignment of the electrode moments.

In fig. 7.3(c) we show how an applied magnetic field affects the $G(V)$ vs. V curves for sample #4, which has a particularly narrow peak width (0.3 meV). For all values of B displayed, the electrode moments are approximately parallel. The extracted peak positions are plotted in fig. 7.3(d). The peak spacing increases approximately linearly with $|B|$ with a g factor of 1.8±0.3. There is a residual zero-field splitting of $\Delta V_{\mathrm{P}} = 0.14 \pm 0.06$ mV. Assuming that the tunneling polarization of nickel is positive [20], this would imply that the sign of a in eqn. (7.2) is positive [22].

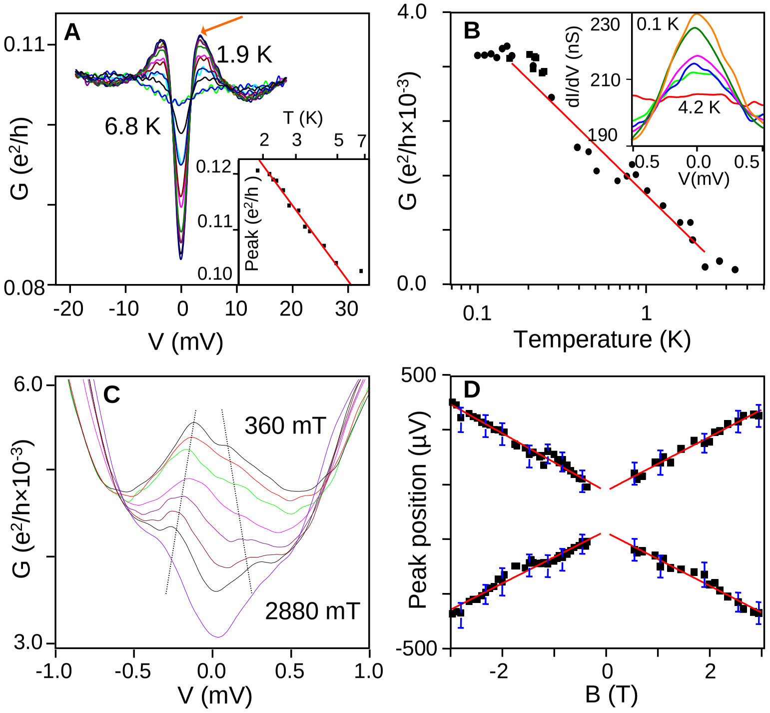

Figure 7.3: (a) T dependence of $G(V)$ for Ni-C$_{60}$-Ni sample #3 with electrode moments parallel, $B = 250$ mT. (inset) Peak conductance vs. T for these curves. (B) Fitted height above background for Kondo peak vs. T for Ni-C$_{60}$-Ni sample #4 with electrode moments approximately antiparallel, $B = 10$ mT. (c) $G(V)$ for sample #4 at 100 mK, at equally-spaced values of B for which the electrode moments are parallel. (d) Peak positions extracted from (c).

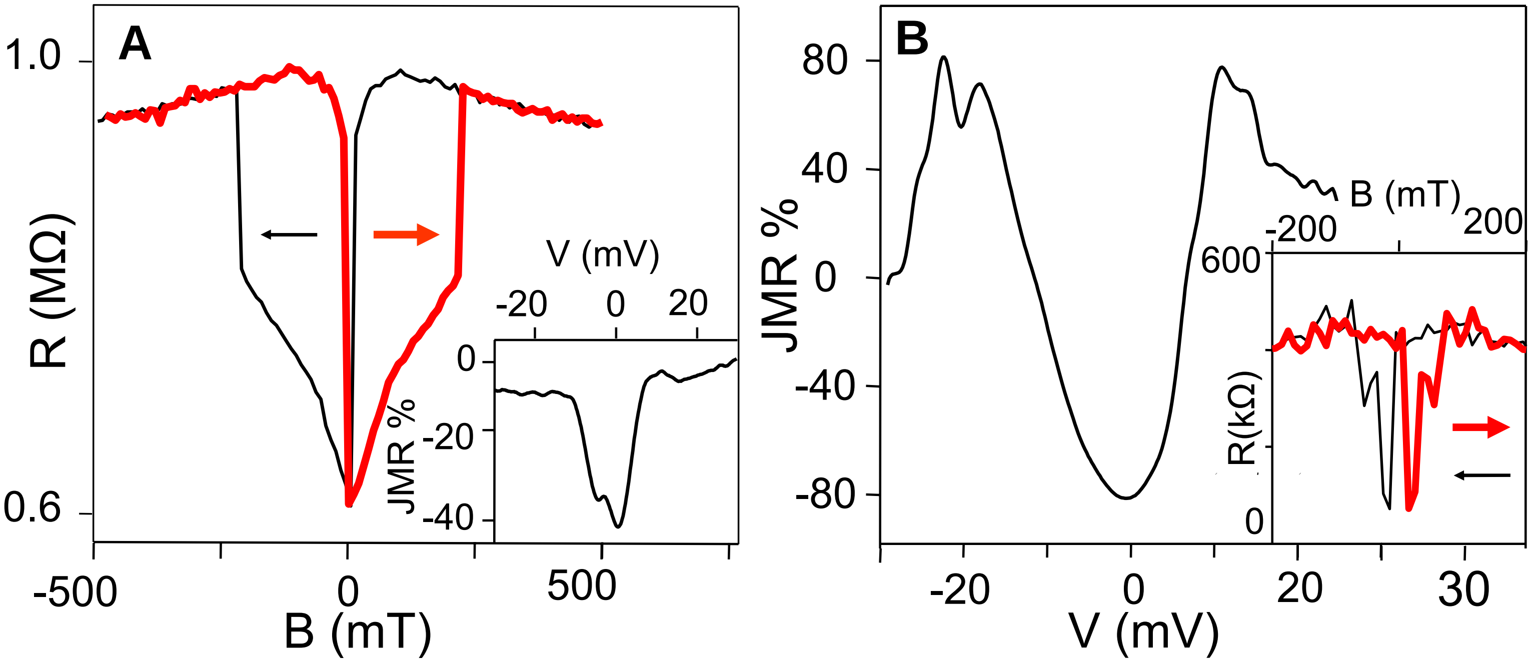

Figure 7.4: $V = 0$ magnetoresistance at $T = 1.5$ K and the junction magnetoresistance as a function of V for two Ni-C_{60}-Ni samples. (a) Sample #1. (b) Sample #2.

7.6 Kondo and JMR

We have shown that coupling to the magnetic electrodes produces a large local exchange field on the quantum dot (greater than 50 T), that can be modulated by using a small external magnetic field ($<$100 mT) to control the relative orientation of the moments in the electrodes. We find that this amplification can dramatically enhance the junction magnetoresistance (JMR), in agreement with theoretical predictions [10]. As a magnetic field is used to turn the electrode moments from parallel to antiparallel alignment, the zero-bias JMR is -38% for sample #1 (fig. 7.4(a)) and -80% for sample #2 (fig. 7.4(b)). The sign of the JMR is negative, opposite to the typical behavior in magnetic tunnel junctions, and the magnitude is much larger than the Julliere value of 21%. This happens because the Kondo resonance occurs closer to the Fermi energy for the antiparallel magnetization orientation, thus enhancing its conductance [10]. A different mechanism for negative values of JMR has been discussed previously in connection with sequential electron tunneling via localized charge states [25], but the magnitude of this effect is smaller than the Kondo mechanism we see.

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through these broad single-electron resonances contributes to the asymmetric conductance background underlying the Kondo signals.

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Chapter 8

Mechanical break junctions

In chapters 2 - 7, I described the fabrication of electrical break-junctions and several results obtained using the technique. It is fairly evident from these chapters that the *contact* between the metal electrode and molecule is central to the conductance properties observed. It would be very useful to be able to modify this contact in a controllable fashion. This is easily done in the case of semiconductor 2-DEG structures by applying a potential to electrodes placed above the 2-DEG. Unless we can figure out a good 4-dimensional fabrication scheme, this is not going to work in the case of 3-dimensional metals. In this chapter, I will describe the mechanical break junction (MBJ) - one way by which we can exert some control over the contact. This is done by physically moving the metal electrode like a scanned probe, yet keeping the whole structure on a chip so as to avoid the troubles faced by low-temperature scanned probes.

The mechanical break junction is a simple contraption first devised by Moreland and Ekin [1] and then developed by Muller [2] and van Ruitenbeek [3]. The concept is illustrated in fig. 8.1. The aim is to create a nm-sized controllable gap in a metal wire. The metal wire is notched to create a weak point, and is epoxied down onto an insulating substrate that is somewhat flexible. A typical substrate is a thin piece of glass. The glass is pushed from below (along the y direction) by a piezo stack. Flexing the substrate strains the wire and eventually breaks it. The gap δx created in the wire can be adjusted using motion along the y direction).

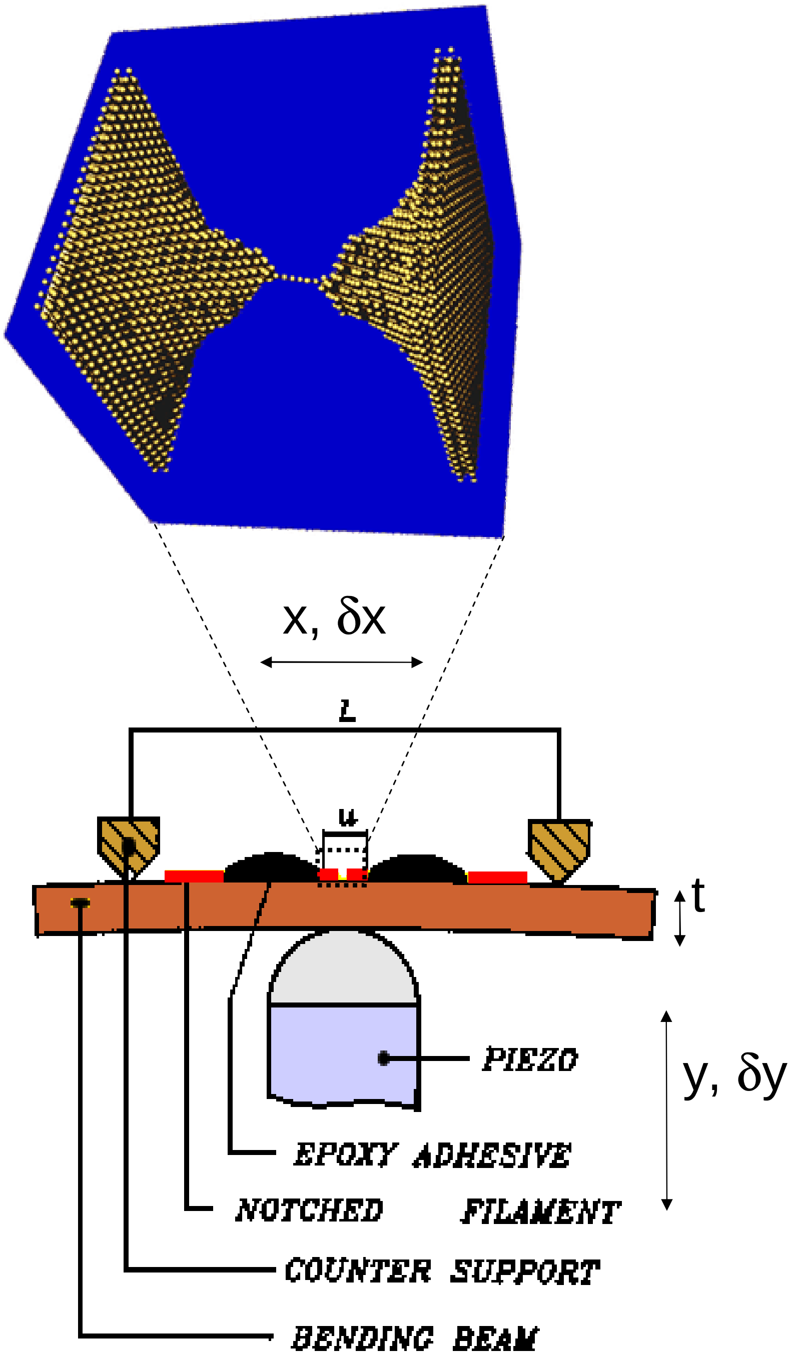

Figure 8.1: The mechanical break junction setup from [3]. A piezo stack pushes a thin bending beam, on which a notched wire is epoxied down.

Why is this geometry preferable to break the wire rather than just pulling the ends of the wire apart? Consider the schematic situation in fig. 8.1. Assume that there is a small gap x in the wire. Then, moving the piezo by an amount δy will create a change in x of

$$\delta x = R\delta y, \tag{8.1}$$

$$R = \frac{3tu}{L^2}. \tag{8.2}$$

Here u is the length of the unconstrained part of the wire (the distance between the drops of epoxy). t is the thickness of the substrate. We have assumed that the middle of the substrate is unstressed, and areas below (above) the middle plane are under compression (tension). L is the distance between the knife edges.

Let us stick some typical numbers into this equation - $L = 10$ mm, $t = 0.5$ mm, $u = 0.1$ mm. This gives us $R = 6 \times 10^{-3}$. What does this imply? For one, if you can control the piezo motion to 1 nm, you can control the gap to 3 pm! Equally importantly, vibrations along the y direction have little impact on the gap. A vibration level of 10 nm which can be achieved with very modest vibration isolation translates to a gap variability of 30 pm. Considering that typical tunnel currents fall off by an order of magnitude over an angstrom, this gives reasonable control over the tunnel gap.

Many experiments have been performed using this rather simple apparatus, and have given us a wealth of information about metallic point contacts [4]. Recently, this technique has been extended to studying conduction through adsorbed molecules [5]. A few years ago, van Ruitenbeek and co-workers devised a nanofabricated version of the MBJ. This is illustrated in fig. 8.2. A thin wire is lithographically patterned on an insulating substrate and is then suspended freely. The rest

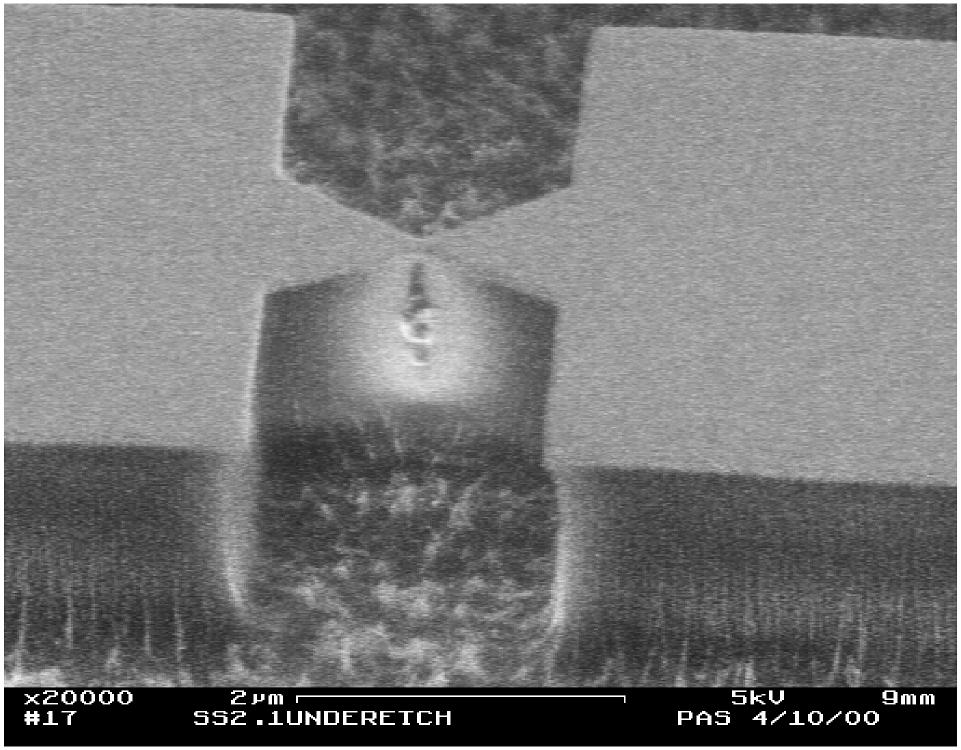

Figure 8.2: SEM of a nanofabricated gold mechanical break-junction. 50 nm of gold is patterned using e-beam lithography on a polyimide/spring steel substrate. The polyimide has been etched to suspend the gold.

of the experiment works in the same fashion as the previous experiments.

There are a couple of advantages of nanofabricated junctions. For one, the value of the displacement ratio R (eqn. 8.2) is significantly smaller. The reduction comes from the fact that the freely suspended part of the wire can be made arbitrarily small by nanofabrication. Typical values [6] are $u = 2$ μm, $t = 0.3$ mm, $L = 15$ mm. This gives $R = 3.2 \times 10^{-5}$, resulting in improved stability and resolution.

The second advantage to using nanofabricated junctions is that more elaborate metallic structures can now be built. For example, Scheer and co-workers [7] were able to make a gold point contact that was only few tens of nanometers away from a superconducting aluminum electrode, and thus able to flow supercurrent through the gold contact.

I have worked only on the nanofabricated version of the MBJ. In the next section I will describe the fabrication of devices that are identical to the original nanofabricated ones [6]. A short description of the experimental apparatus follows in section 8.2. In section 8.3 I will make a few suggestions for improvements to the fabrication process. In section 8.4, I will describe a modification of this technique where the substrate is made of silicon. This makes the nanofabrication significantly easier, and allows us to incorporate a gate electrode in the setup. A few results of this technique are also presented in this section. While the original setup and fabrication (section 8.1) were done by me, most of the work on the silicon substrate has been done by Alex Champagne. Read his thesis when it is done. I will conclude the chapter with a few suggestions for future experiments using this technique.

8.1 MBJ fabrication - metallic substrates

I will first discuss the fabrication of nanowire on metallic substrates. Not working with silicon as a substrate is a considerable nuisance, as this fabrication procedure indicates. The procedure I worked out was done in my early days as a grad student. In retrospect, several improvements can be made. Let me first describe how I did the fabrication, and then talk about improvements.

8.1.1 Substrate polishing

The first task is to make a substrate that is reasonably flat - below about 1 μm roughness over a mm-sized area. The metal substrates I used were phosphor bronze and spring steel. I bought them in two thicknesses - 0.005” and 0.01” from a commercial vendor [8]. They sell sheets, typically 6” wide and a foot long. The processing works as follows:

1. First dice the sheet into 7 mm × 15 mm pieces. This is best done in the machine shop using the sheet cutters. Try not to scratch the surface. You can use something to protect the surface, such as sticky plastic wrap. It is important to have a smooth edge without any protrusions at the edges, else you will never get the substrate flat on the e-beam holder.
2. Discard any pieces with deep scratches. I usually throw away 5 pieces for every piece I select. Metal is cheap, e-beam (and your time) is not.
3. Sand the pieces using increasingly finer grits of sandpaper - start with 180 grit, go to 320, then 600 and finally 1000 grit. Between each grit, wash the

pieces in water thoroughly (and your hands).

4. Polish the pieces using alumina polish. I start with 4.5 μm, then go to 3 μm, then 1 μm and finally 0.3 μm. I buy my polish supplies from Buehler [9]. Use gloves, and keep your own polishing cloths, polish etc. away from everybody else. When you are done with each grade of polishing, you have to wash the pieces thoroughly and then sonicate in acetone/IPA for 10 min. Keep the pieces always in a holder, away from each other. It is incredibly easy to
    (a) Contaminate your polish with larger particles.
    (b) Flip the pieces, or make them touch things they should not.

At the end of this you will have a fairly smooth substrate. Check the surface roughness on the profilometer. It should be smooth to about 0.1 μm over 100 μm, with about 1 μm undulations over a mm scale.

8.1.2 Polyimide coating

The next job is to coat the substrate with an insulating layer. I found that polyimide [10] does the job quite well. The process is:

- Spin on the adhesion promoter (QZ3289) at 4000 prm for 30 seconds. You have to use the smallest chuck to do this.
- Spin on polyimide PB284 at 3000 rpm for 1 minute. This gives a 3 μm thick film after baking.

- Softbake for 2 minutes at 90 °C. This will keep the polyimide from flowing around while you spin all your chips.
- Spread out your chips on aluminum foil, and bake them in the YES Polyimide oven. I used the process with three cures at 90 °C, 150 °C and 270 °C. This worked well for me - I saw no evidence for cracking of the film at low temperature (something you should check for, if you use a different recipe).
- Clean the chuck you used for spinning by soaking in polyimide strip for a few hours.

8.1.3 E-beam lithography

Doing photolithography to make contacts on these chips is a pointless task, since the time involved in doing photolithography on each individual piece is huge. This is one good reason to delay chopping up the substrate into pieces till much later in the process. I will talk about this in the next section. For now, I will describe the process in which the entire pattern is made by a single step of e-beam lithography.

The first step is to spin PMMA on your wafer. The process is:

1. Spin on PMMA coplymer (3:1 in Ethyl lactate) at 3000 rpm for 60 seconds.
2. Bake for 15 min on the hotplate at 170 °C.
3. Spin on 4% 496 K PMMA in Anisole at 3000 rpm for 60 seconds.
4. Bake for 15 min on the hotplate at 170 °C.

An alternate recipe is to use a single layer of resist, about 300 nm thick. The liftoff is not too special if you do this, but it saves some time.

The next step is to mount the chips on the holder for the VB6. This presents a problem - for the electron beam focussing to work properly, the substrate height has to be within $\pm 50\mu$m from the height at which the beam was calibrated (Leica says $\pm 20\mu$m, but I've had reasonable luck up to 50μm). The usual way this is accomplished is to stick the wafer on a three-point holder that is previously aligned with the height of the focus mark. There is no holder for small pieces with this mechanism (or at least none where we can hold several pieces at one time)

There are a couple of different ways of solving this problem. One way is to make a chip-holder using a 3-inch wafer. I have done this using the KOH wet-etching technique as described below:

1. Start with a double-sided wafer that is twice as thick as your metal pieces. If you choose a 0.005" metal substrate, the wafer thickness you use is 500μm, a standard size.
2. Grow 100 nm of silicon nitride on the wafer using LPCVD.
3. Spin resist on both sides of the wafer (S1813) and bake, as described in the fabrication steps for making nanopores [11].
4. Expose the two sides of the wafer using the masks shown in fig. 8.3(a) and (b) on the HTG contact aligner. The alignment of the two sides is coarse, so you can get away with a sheet of paper with the outline of the wafer as the alignment mark, as for the nanopore [11]. Develop for 90 seconds in MIF300.

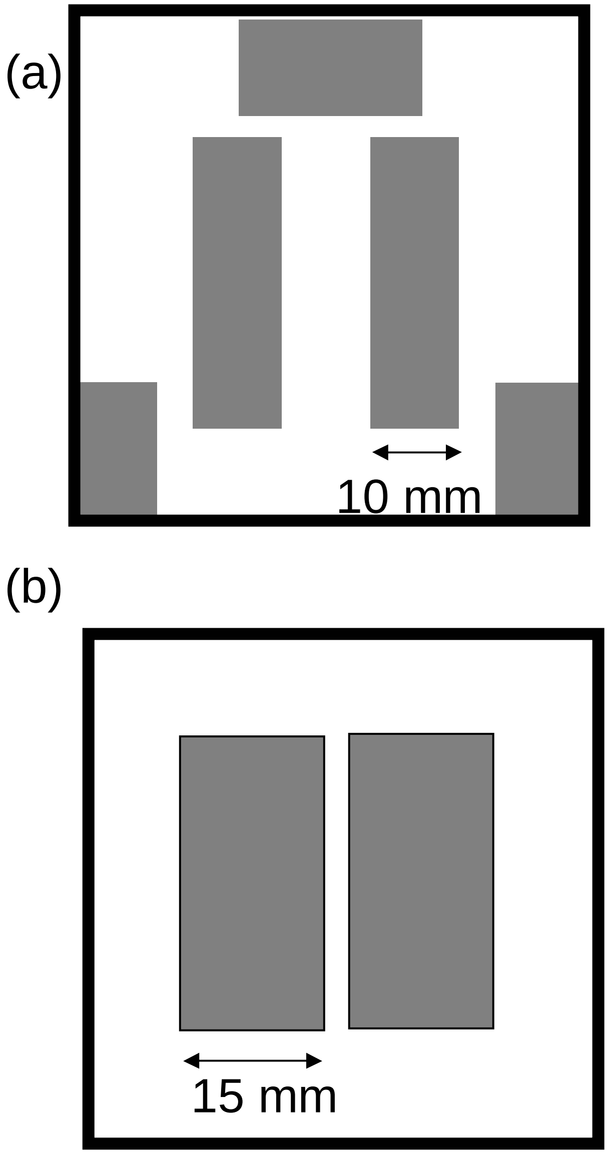

Figure 8.3: The two masks used to make a wafer clamp (a) Top side of the wafer. (b) Bottom side of the wafer.

5. Etch the nitride on both sides of the wafer using the Applied Materials or PT72 RIE, as described in [11]. Remove the resist using acetone or an oxygen plasma.

6. Etch the silicon using KOH (as described in [11]) till you see holes in the wafer. If the etch works right, you will have a wafer as shown in fig. 8.4. The steps below the three point mechanism should be half way through the wafer, as should be the steps where the phosphor bronze pieces sit, so that the pieces are at the right height for exposure. It can take a couple of tries to get the height of the steps line up well. It helps to keep turning the wafer around in KOH every few minutes, otherwise differences in concentration and temperature at different points in the solution can ruin your wafer. I've tried doing a dozen wafers with less care, hoping a couple would come out right. This did not work for me.

7. An alternative would be to use the deep silicon etcher (PT770 or Unaxis) to etch both sides of the wafer. This etch should be much more uniform than the KOH etch.

The "wafer holder" is a reasonable method, and I would advocate trying it first. The pieces do tend to jiggle around in the holder though, so you can sometime shoot the pattern over the wrong spot.

A different method I used was to use the X-ray holder of the VB6 which is designed to hold small pieces. This method is laborious, but it works every time. The big problem is the getting the height right. First, avoid blocking the height sensor. The height sensor is a laser that comes in at an angle of less than 30° onto

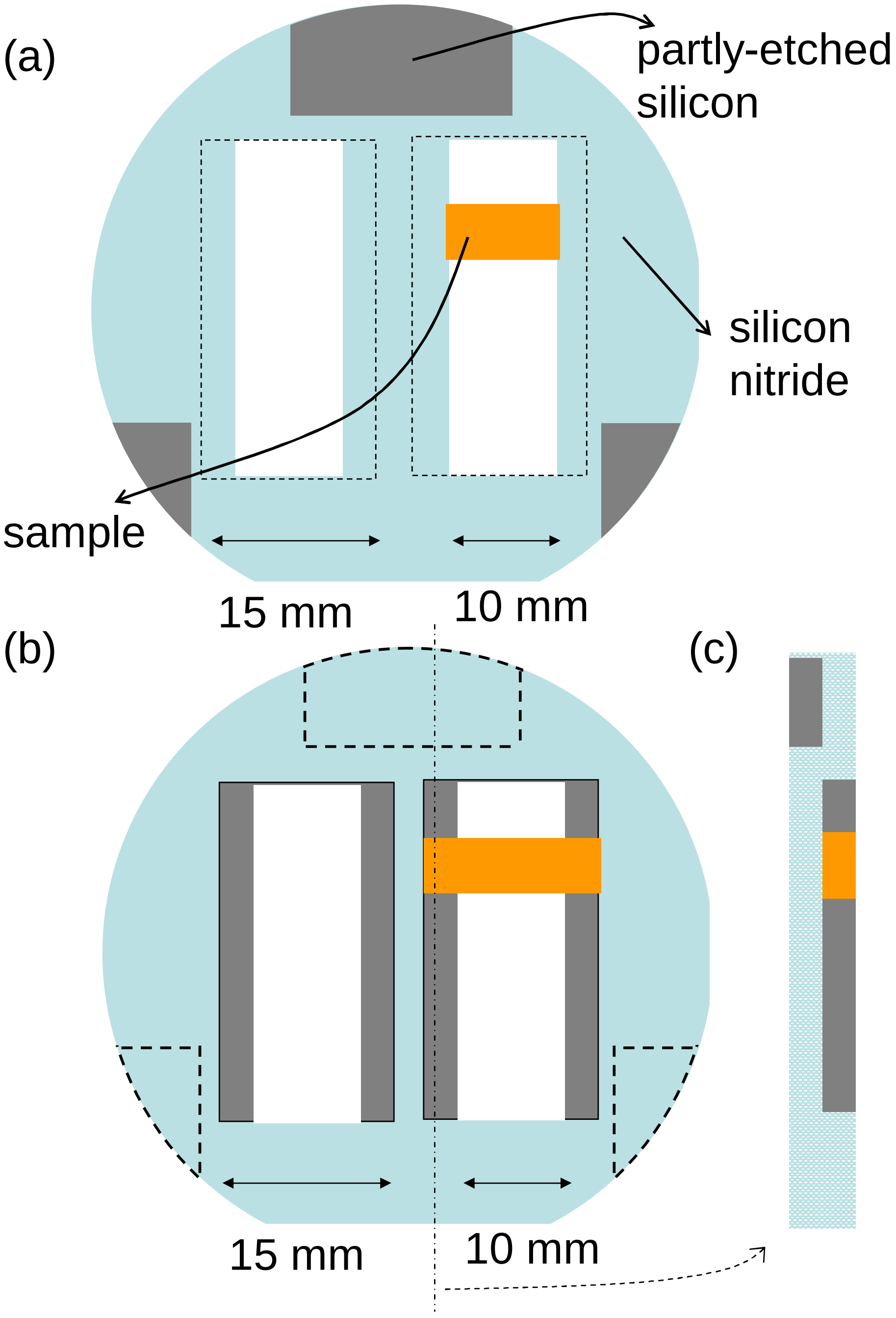

Figure 8.4: Result after using the masks in fig. 8.3. (a) Top view. (b) Bottom view. (c) Cross section.

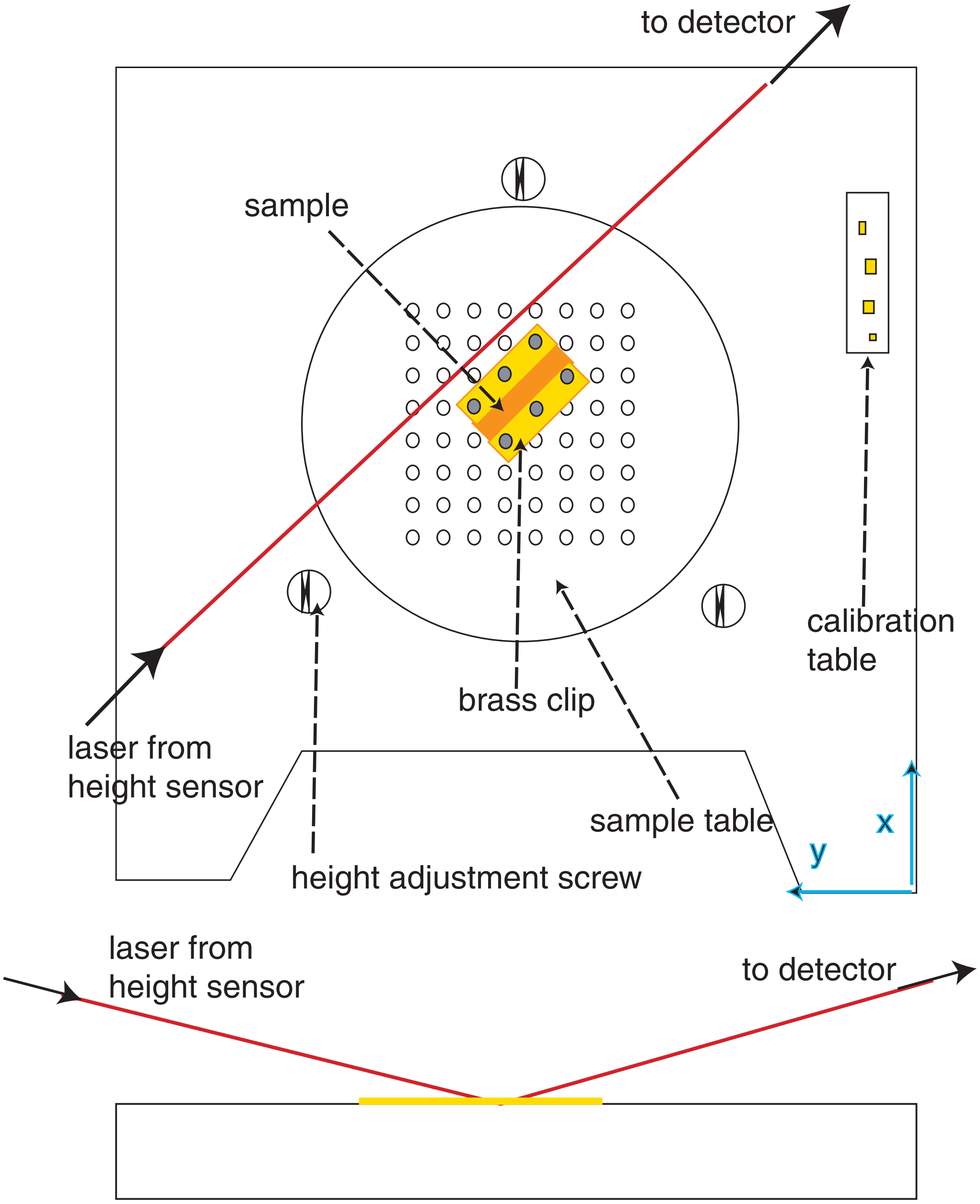

Figure 8.5: Illustrating the use of the X-ray holder on the VB6.

your substrate. If its path to or from your substrate is blocked, you are done for. The usual clips don't work with little pieces since they cast a long shadow. So I had to make some flat pieces of brass (about 0.02" thick) as shown in fig. 8.5 that I used to hold down my substrate. You have to have two of these things on either side of your substrate, or else the substrate will tip. If you keep the long axis of the piece parallel to the laser beam as shown in fig. 8.5, you will be safe. The height sensor axis is at an angle of 45° between the x and y axes of the stage. You therefore have to hold the pieces down as shown in fig. 8.5. The last I saw, these pieces were still lying in the VB6 room at CNF.

Once you have your pieces held down, the next job is to make sure that all the pieces are at the correct height. The X-ray holder height can be modified with three screws (shown in fig. 8.5). The only way of checking the height of the holder is to stick it in the machine, record the heights of all the chips (you can write a little script for this) and then pull the holder out of the machine and adjust the heights again. If you are lucky, you can do this in one try. This process is the most annoying part of the fabrication.

Once you have figured out a way of holding your chips in place, you are ready to do your exposure. You first have to know where the different chips are positioned on the holder. You can use the optical microscope for this. You will have about a 1 mm leeway in positioning the pattern, so the alignment with the optical microscope is pretty easy. Just note the center of where your pattern should lie. If you standardize your exposures (keeping the chips always in the same place on the holder), you could even use the same positions each time.

Well, all that is left is to expose the pattern. A typical pattern is shown in

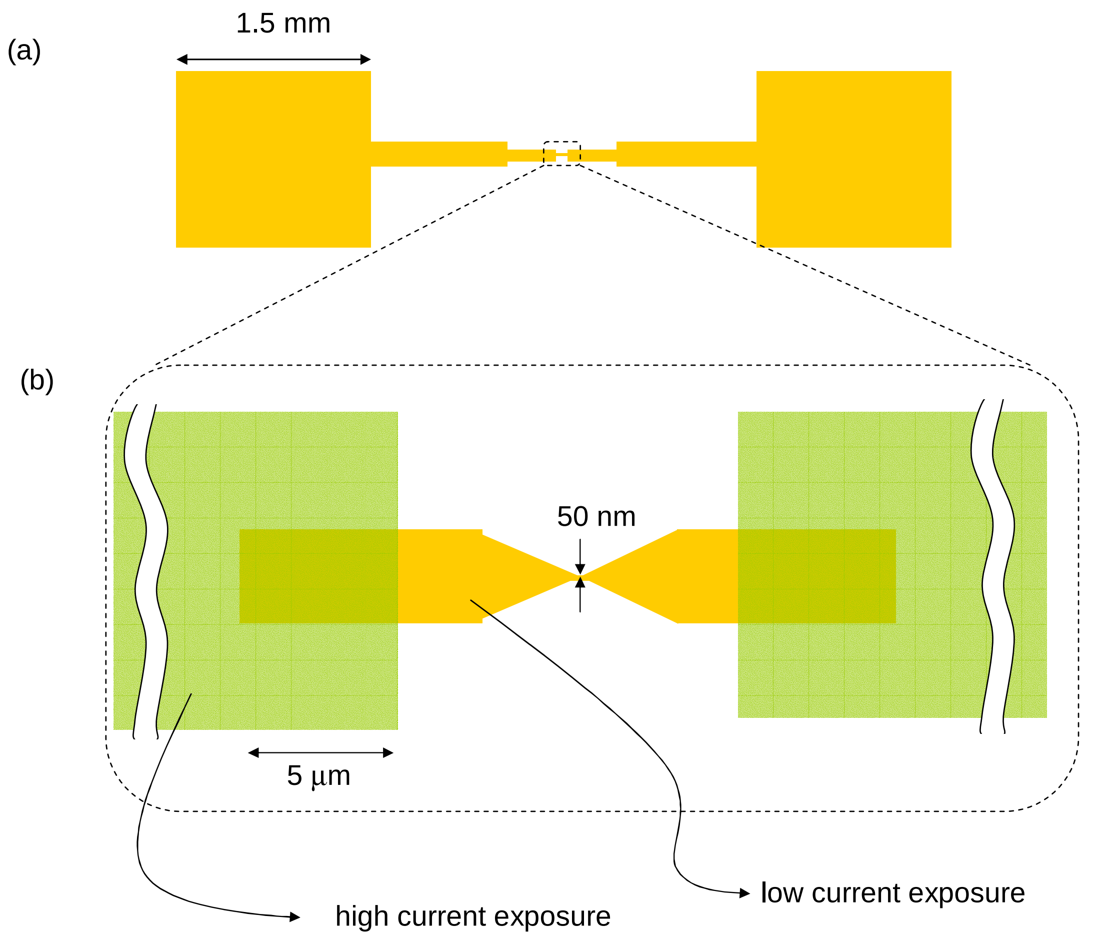

Figure 8.6: (a) E-beam pattern for metallic substrates (b) zoom-in showing the patterns written at high and low current.

fig. 8.6. Note the sizes - we want to make 1 mm contact pads using e-beam! You therefore have to split the pattern into a low-resolution and high-resolution part as indicated in the figure. The high resolution part can be written at 1 nA and a VRU of 1 as usual. For the low resolution part, increase the beam current to at least 50 nA and use the lowest dose possible (600-800 μC/cm^2). In the old days, I used to change the aperture to 400μm and crank the beam current up to nearly 200 nA. This might not be possible with the new rules in place for the machine. However, get the machine manager to set up the highest current possible. The way to estimate the writing time is to take the simple formula from the dose and current

$$t = \frac{A}{dI}, \tag{8.3}$$

and multiply it by about a factor of two. Here A is the area to be written, d the area dose and I the current. The factor of two takes care of dead time between pixels and stage moves. In order to minimize the dead time between pixels, use the largest possible VRU. Your VRU is limited by the maximum clock speed of the pattern generator (25 MHz). For a given VRU, the minimum dose writable is

$$d_{min} = \frac{I}{\nu_{\mathrm{max}}(\mathrm{VRU} \times 5\ \mathrm{nm})^2}. \tag{8.4}$$

Here ν_{max} is the maximum clock speed (25 MHz), I is the beam current and I am assuming that the base pixel size is 5 nm. Given your smallest dose, this sets an upper limit on the VRU.

The typical series of steps involved in the exposure are:

1. Do your job calibration at 1 nA.
2. Write your high resolution patterns.

3. Move to the focus mark, raise the current to 50 nA or whatever. You can do this manually as well, by adjusting lenses C2 and then C1 to keep the mark in focus.
4. If the mark is in reasonable focus, there is no need for recalibrating the machine. For the large features, both the exact focus as well as the conjugate blanking are not too important. Keep you small patterns at least 50 μm away from the big ones, and keep at least a 5 μm overlap between the two patterns.
5. Write the big pattern

If you are using the X-ray holder, there is an additional complication, caused by the fact that the long axis of the pattern is at 45° to the absolute coordinate system of the machine. You might think that you could get away by defining your wafer coordinate system at 45° to the absolute coordinate system, but this is not possible - any coordinate system can be at maximum 8° away from the absolute coordinate system. This means that you have to draw your original patterns at an angle of 45° to your coordinate axes.

After exposing the pattern, develop in MIBK/IPA, Methanol and IPA as for the devices described in chapter 2. I made a little holder out of aluminum with separate spaces for each chip, so that I could develop 8 chips at one time. This saves time. If you make two such holders, you can use one during the liftoff to keep the chips away from each other.

After developing, descum as described in chapter 2 (6-8 seconds on the PT72). Then evaporate 2 nm Ti + 50 nm Au. Liftoff overnight in acetone.

8.2 Metallic substrates - measurement

Unlike the samples made on thick silicon wafers (chapter 2), we cannot use the standard chip carriers for mounting our samples, since we need to be able to bend them. I have therefore designed an apparatus for this purpose, as shown in fig. 8.7. The sample is inserted in a slot cut into a copper piece, the edges of which hold the sample which is pushed by the 1/4"-80 TPI leadscrew [12]. Contact is made to the samples using spring-loaded probes [13].

The bending apparatus is mounted to the 1 K pot of a Desert Cryogenics dipstick. The line-of-sight feedthrough of the dipstick is off center, so I use a couple of gears to move the bending screw [14] as shown in fig. 8.7. A 1/8" stainless-steel rod comes down through the line-of-sight feedthrough to turn the screw. The rod goes through a quick-connect at the top of the dipstick. It is attached through a 50:1 gearbox which is in turn attached to a stepping motor.

The resolution of the stepper motor is 1.8°. This results in a minimum step of the bending screw of $\frac{1.8}{360\times50\times2\times80}$ in $= 0.016\ \mu$m. The true resolution of the screw is not necessarily as good as this number suggests - it is also determined by the machining precision of the screw and nut. The best way to calibrate the resolution of the screw is to study a tunnel junction.

Before measuring a sample, the narrow part of the stricture has to be suspended above the substrate. This is done using an oxygen plasma etch on the Applied Materials or PT72 RIE. Polyimide etches at roughly the same rate as resist. Etching down about 500 nm into the polyimide is sufficient to suspend the wire. An alternative is to use the polyimide wet etchant to suspend the wire.

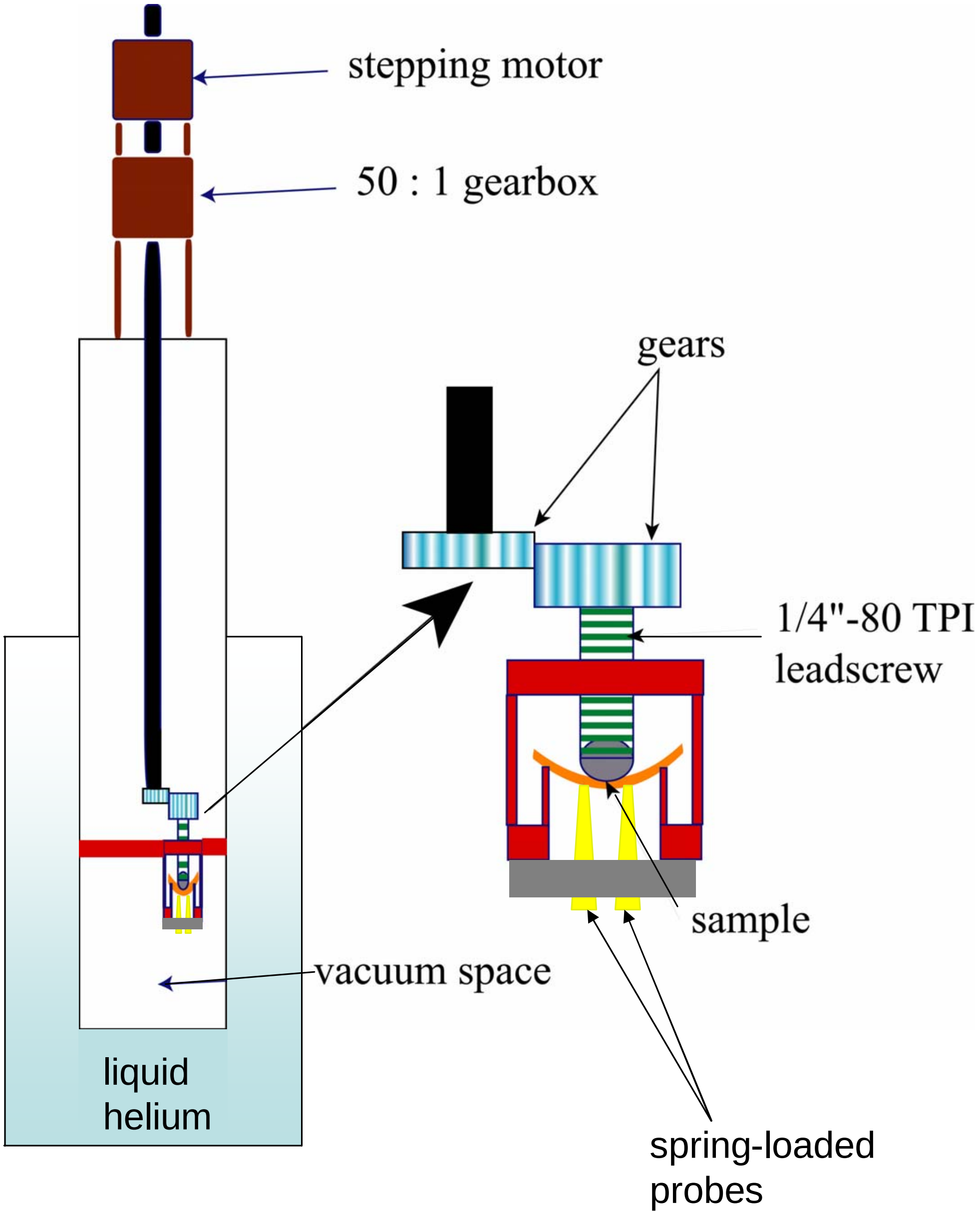

Figure 8.7: The apparatus used to bend the substrate for mechanical break junctions.

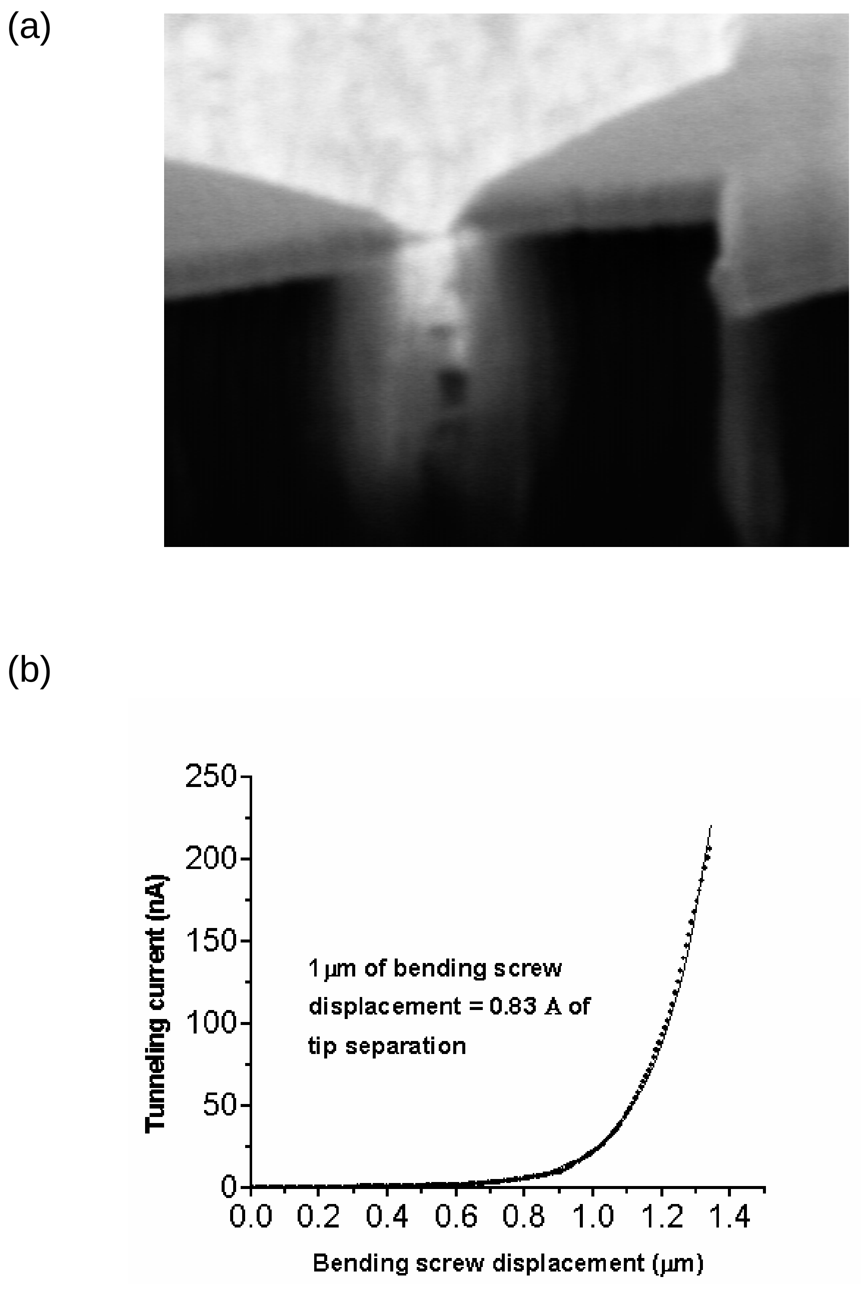

Figure 8.8: (a) SEM picture of a mechanically-broken gold nanowire. (b) Tunnel current at 1 V bias showing an exponential dependence with motor motion. The fit is to eqn. 1.3.

I have found the current apparatus to be fairly robust against vibration. It also has a reasonably good resolution. Shown in fig. 8.8 is the resistance of a tunnel junction at 4.2 K that was created by pulling a gold wire apart. As is evident, the tunnel current follows the simple tunneling formula (eqn. 1.3) fairly well. A fit to the tunnel current using eqn. 1.3 gives a displacement ratio of 8×10^{-4} which is about a factor of ten larger than suggested by eqn. 8.2. This is most likely due to non-uniform bending of the substrate. We can also see that the minimum resolution of the screw is comparable to the resolution dictated by the stepping motor, indicating that the machining is good enough not to be a concern.

8.3 Possible improvements - metallic substrates

I can think of a number of possible improvements to the current fabrication process to make the sample fabrication simpler:

1. Start with pre-polished (at least to a few microns) substrate. The substrate I used had several big scratches which really made polishing difficult. In retrospect, it would have been worth the money to start with pre-polished substrates.

2. One huge improvement would be getting pre-cut, flattened substrates that are roughly 2 inches in diameter. This would allow us to use the substrate like a silicon wafer and make multiple samples at one time. I have tried to do this myself by polishing larger pieces of phosphor bronze. The problem is getting the substrate flat enough on the polishing wheel to polish it uniformly. Releasing the metal after polishing is also bad, because it tends to curl up

around the edges.

3. In the event that you are able to buy (or make) polished substrates that are two or three inches in diameter, it would be ideal to mount this on a wafer somehow, so that it stays fixed on the wafer during the whole fabrication process. Something as simple as photoresist or spin-on glass might do the trick. If you can do this, you will have a really easy fabrication process - the substrate can be processed exactly like a silicon wafer. You can then do photolithography, make alignment marks, etc.

4. The problem with making multiple samples on a single piece of phosphor bronze is cutting the pieces apart after fabrication. I tried the laser cutter that once existed in Kimball hall, but it took way too long to cut through my piece (several hours). Since that time, they have acquired a new laser cutter, which is reputedly more powerful. This can be tried. There is also the possibility of using a diamond wafer saw. Conventional diamond-impregnated blades are easily dulled by cutting metal. I have heard that there are new blades designed for cutting metallic thin films on silicon substrates. These could be tried. Alternatively, it may be worth trying even the conventional blades. Even if the blade is ruined after one wafer, it is worth the expense (a blade costs a few dollars).

5. Multiple samples could be made on one chip. I have been unsuccessful in making wirebonds to the gold pads. Conventional wisdom has it that polyimide is a difficult substrate to make wirebonds on since it is springy. However, I feel that if the gold pads are thick enough (say 200 nm) wirebonding will work. This should be investigated. Even otherwise, it should be possi-

ble to make contact to more than one sample on a chip using spring-loaded probes, as long as the contact pads are made using photolithography (if you use e-beam, the time to do multiple pads on the e-beam makes this pointless).

8.4 Silicon substrates

Given all the trouble that using the metallic substrate involves, it will be nice to be able to use a flat substrate like silicon in this experiment. The problem however is that silicon is more brittle than any of the metals we use in our nanowires, so it will not be possible to mechanically stretch and break a gold wire on a silicon substrate without first fracturing the substrate. For example, a 200 μm-thick wafer of silicon that is 10 mm long can be bent by at most 0.5 mm (corresponding to a radius of curvature of 25 mm) before it breaks. Our gold nanowires typically need 1 to 1.5 mm of bending before breaking. This is where electromigration comes to the rescue. What if we break the wire using our favorite electromigration technique? We can then modulate the gap in the wire using the mechanical motion of the screw.

To fabricate such devices, a couple of things have to be done differently from the sample fabrication described in chapter 2. The first is that all the fabrication has to be done on the thinner wafer (200 μm). This means that you cannot use the standard 500 μm chuck on the stepper. Alex found that a couple of pieces of filter paper under the 200 μm wafer does just fine as far as the height is concerned. Secondly, the pieces have to be finally diced into 7×15 pieces instead of the 6×6 pieces that we are used to. Care has to be taken that the axis of the wires is parallel (and not perpendicular) to the long axis of the chip. This means in effect that all the patterns (photolithography and ebeam) are rotated at 90° to the ones used in chapter 2.

Since the fabrication works the same way as for the thick silicon substrates, it is possible to make wirebonds to the samples. This however requires a little more effort, since the usual chip carriers cannot be used. One convenient way to do this is to use a Samtec connector that has the tips cut off and is flattened, as shown in fig. 8.9(a). We can make contact to 16 samples by this technique, a great improvement over the spring-loaded probes.

After fabricating the wires and before breaking them by electromigration, they have to be suspended over the substrate. This is done by using a timed wet etch using buffered hydrofluoric acid. We have tried a number of thicknesses of oxide to see how thin we could make the oxide and still suspend the wires. A thickness of 40 nm works well. A typical suspended wire is shown in fig. 8.9(b).

After electromigration, the distance between the electrodes can be adjusted using the mechanical motion of the screw. Shown in fig. 8.10(a) is the resistance of a tunnel junction that is modulated by pushing on the bending screw. Using eqn. 1.3, we arrive at a calibration of 5.5 pm/turn of the motor. The tunnel junctions also have excellent mechanical stability, which we can check by monitoring the resistance of a tunnel junction over time (fig. 8.10(b)).

As a first experiment with the silicon substrates, Alex studied C_{60} molecules. The devices are made by dropping 100 μl of a 200 μM solution of C_{60} in toluene on the chip and blowing dry after a few seconds. After performing electromigration

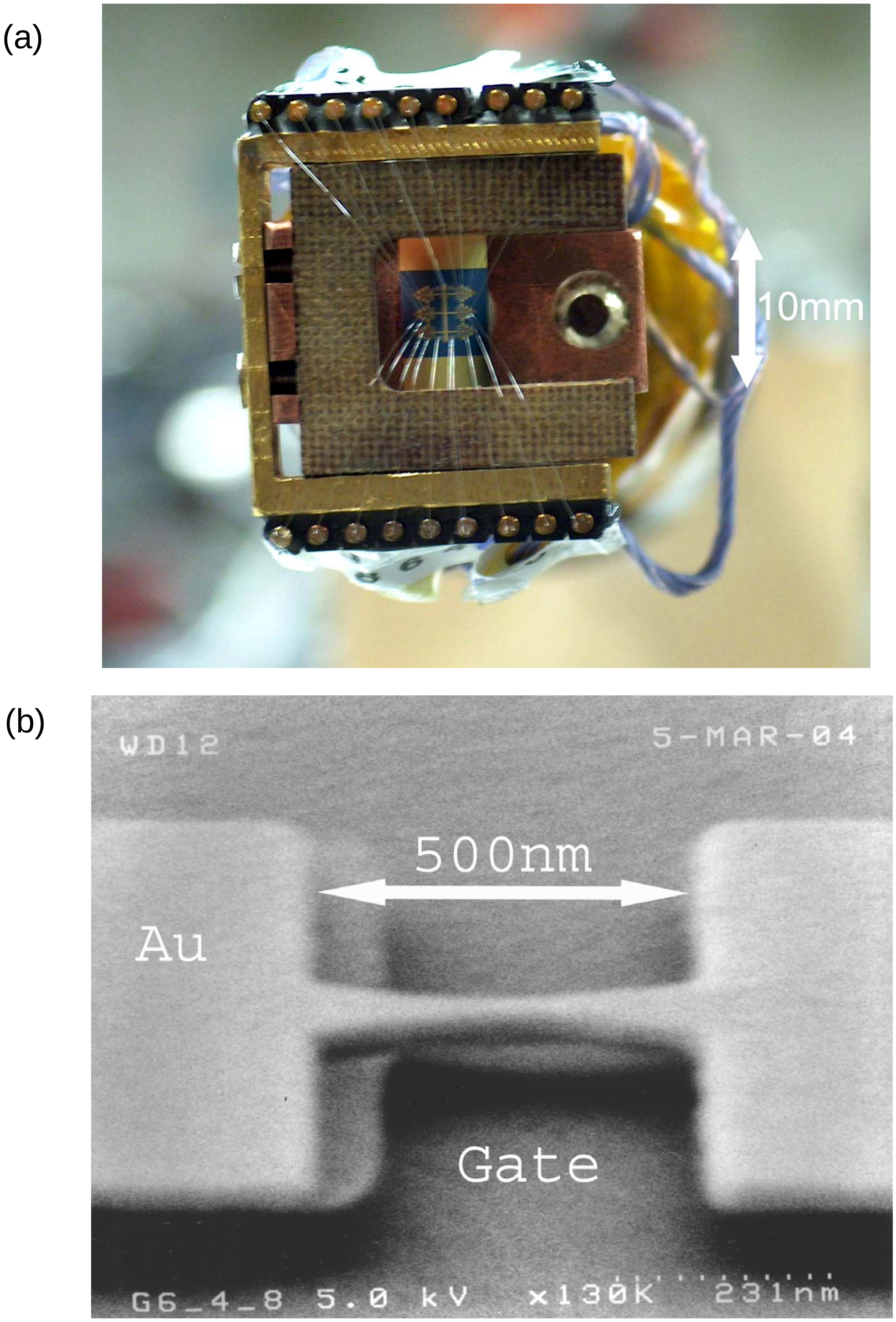

Figure 8.9: (a) Silicon substrate sample holder. (b) SEM image of a gold wire suspended 40 nm over a silicon substrate (courtesy A. Champagne).

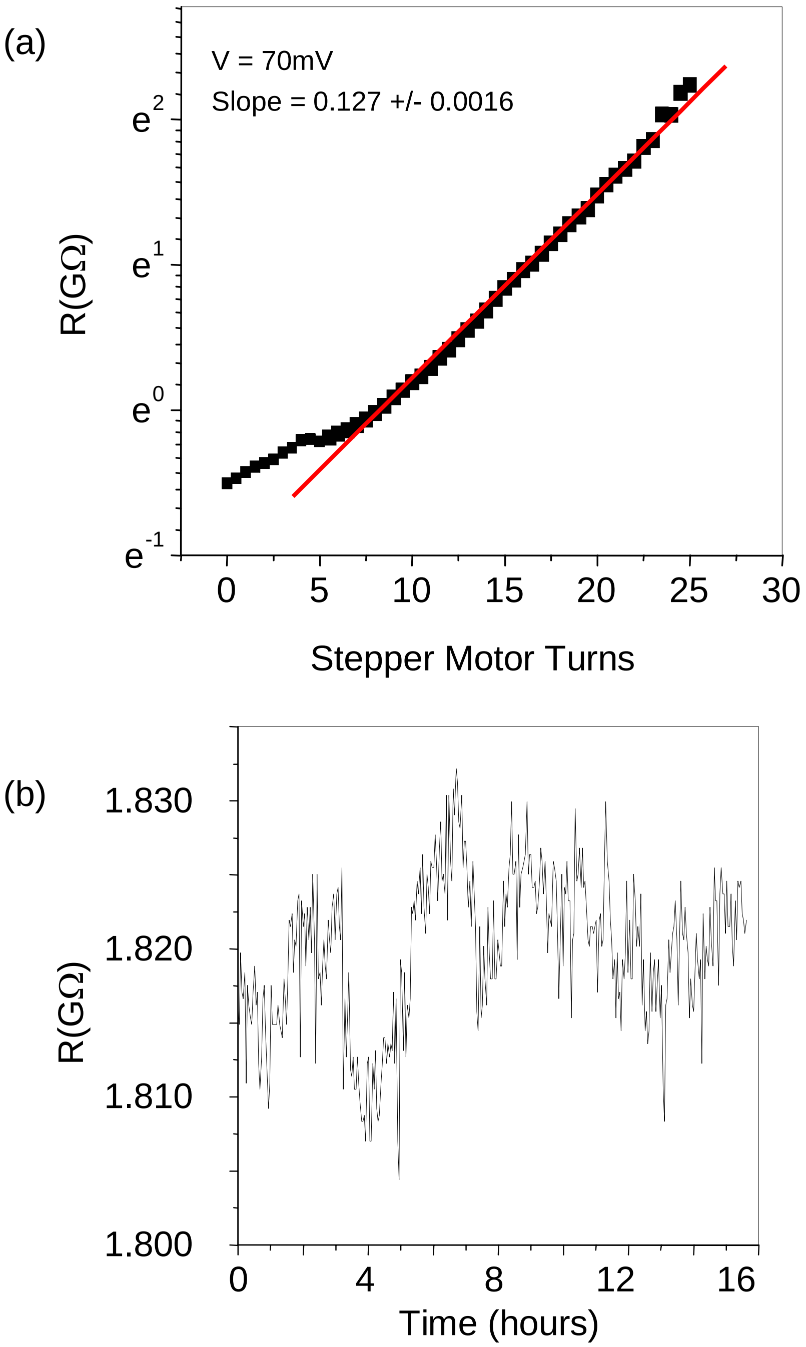

Figure 8.10: (a) Tunnel current on a gold junction showing an exponential dependence with motor motion. (b) Resistance of a gold junction over time showing good mechanical stability (courtesy A. Champagne).

at 4.2 K, the resulting device sometimes has one or more molecules C_{60} between the gold electrodes. We see typical Coulomb blockade characteristics from these devices. Further, by pushing on the bending screw, the conductance of the device can be changed because of changes in the tunnel distances. Shown in fig. 8.11(a) are I-V curves of one such device at different screw positions. Shown in fig. 8.12 are dI/dV plots of two samples at different source and gate voltages showing that the gate electrode is effective enough to change the charge state of the molecule. We can now therefore consider experiments analogous to 2DEG quantum dots where the tunnel resistances can be changed (albeit without as much control as in the 2DEG samples). As a first interesting finding, Alex has discovered that the charge offset on the molecule is modified by mechanical motion [15], resulting in "mechanical transistor" action.

8.5 Possible experiments with mechanical break junctions

There are a number of interesting experiments that can be performed with the mechanical break junction setup that we have. Among them are:

8.5.1 Carbon nanotubes

Recently, a lot of research has focussed on the properties of suspended nanotubes [16, 17, 18, 19, 20]. Suspended nanotubes show interesting nanoelectromechanical properties, and are also "ideal" nanotubes for doing transport measurements since they are free of interaction from a substrate. The typical method for straining a nanotube is to use an AFM tip, or to use the electrostatic force between the tube

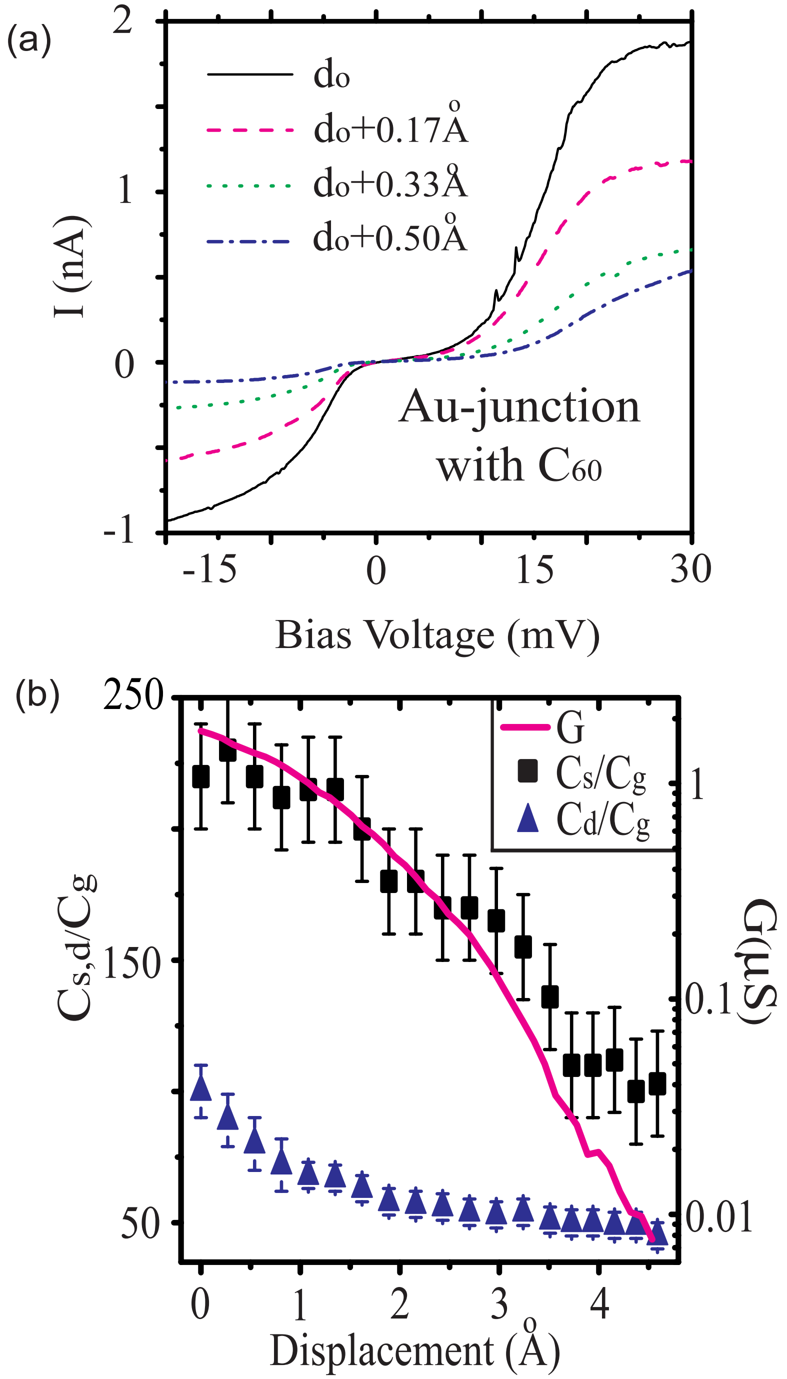

Figure 8.11: (a) An Au-C_{60}-Au device showing Coulomb blockade at different source-drain spacings. (b) Extracted capacitance ratios and conductance using fits to orthodox Coulomb blockade theory (courtesy A. Champagne).

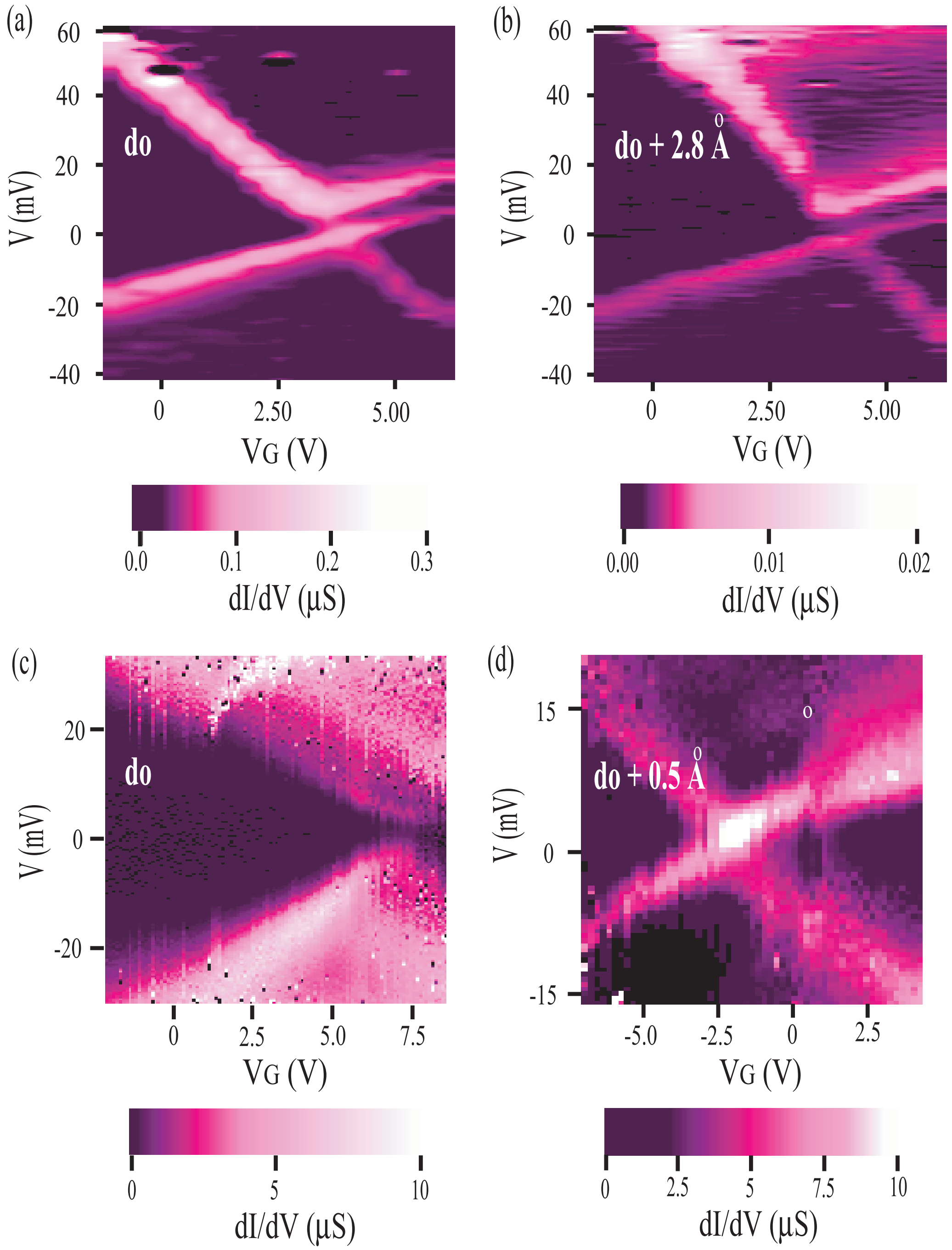

Figure 8.12: (a) and (b) dI/dV plots at two different electrode spacings showing that the charge state can be changed by the gate electrode. (c) and (d) A different sample (courtesy A. Champagne).

and a gate electrode. The break junction technique is another way of applying stress to a nanotube. The break junction will be a controlled way of applying stress at variable temperatures.

It may even be possible to strain a nanotube to its yield point using the break junction technique. One way of generating large strains in a nanotube is to have a very short tube between the electrodes. This can be achieved by having a nanotube in a nanometer-scale break junction created by electromigration. While we have been successful in making such devices, extensive measurements on them are yet to be carried out. It might also be necessary to use the more flexible metallic substrates to do this measurement. In this case, the nanotubes have to be spun on the substrate rather than grown by CVD.

8.5.2 Solution-gated molecular conduction

One way to make measurements of the conductance of molecules is to compile histograms of the conductance as a gold wire is stretched with adsorbed molecules on the surface [5]. N. J. Tao's group has extended these measurements by using an electrolyte solution to gate the molecules while the conductance traces are being obtained [21] (fig. 1.4). This technique is interesting and ought to be applied to the molecules that we have studied using the electromigration-junctions (C_{60}, C_{140} and especially the cobalt coordination complexes). This can give us good insight about what the average conductance of a molecule is.

8.5.3 Metallic dots, ferromagnetic electrodes

There have been several predictions for interesting spin-dependent behavior in normal and ferromagnetic quantum dots attached to ferromagnetic electrodes (for eg. see [22]). All of these predictions depend sensitively on the strength of the coupling between the electrode and the quantum dot. The mechanical break junction would give a way of changing this coupling.

8.5.4 From incoherent to coherent tunneling

As the conductance of a tunnel barrier approaches the conductance quantum, coherent tunneling begins to happen across the barrier. This coherent tunneling can show up in a variety of ways in a quantum dot device, as well as in interfaces between different materials (for example ferromagnet-superconductor junctions). Using the mechanical degree of freedom will allow us to turn coherent tunneling on and off in such devices.

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Chapter 9

Other experiments and outlook

In the previous chapters, I have described the use of electromigration to create two electrodes that are separated by a nm-scale gap. I have discussed the conductance of molecules incorporated into the gap. Can the same technique be used for other purposes? In this chapter I will discuss two experiments done using this technique. The first is the study of solution-gated polyaniline thin films. The second is the fabrication of gated metallic quantum dots using this technique. I have made some preliminary contributions to both experiments, but others (Jacob Grose, Burak Ülgüt, Kirill Bolotin and Ferdinand Kuemmeth) are responsible for them now. I will therefore be rather brief in describing them. I will finish by suggesting some other experiments that can be done.

9.1 Polyaniline field-effect transistors

Conducting polymers are an extremely interesting class of molecular materials for transport studies, the reason being that their conductance can be modulated by a factor of 10^6 by gating them in solution [1]. Further, their peak conductance can rival that of a metal. Conductance measurements have usually focussed on thin films of these polymers between two electrodes spaced on the order of a micron apart [1]. Recently, N. J. Tao's group has made some elegant STM measurements on single strands of polyaniline (PANI) [2], a typical conducting polymer. Such measurements can help distinguish between carrier transport within a single strand of polymer, as against measurements on bulk films, where the carriers have to move across several strands of polymer to move between electrodes. Inspired by this measurement, Jiwoong Park, Jacob Grose and I set out to do similar measurements in our setup, the idea being that we could make measurements that the STM setup is not capable of doing easily (such as temperature dependence or using a back-gate instead of a solution gate).

The first step in making our devices is making a film of polyaniline between the electrodes (that have been created by electromigration at room temperature). This is done by electroploymerization of aniline monomers, as described in [2]. The chip is immersed in a solution of 0.1 M purified aniline monomers in 0.5 M Na_2SO_4 with pH adjusted to ~ 1. The potential of the source electrode immersed in the solution is swept from 0.25 to 1.25 V relative to the drain and gate electrodes. This produces highly conductive polyaniline [3]. The polyaniline film is several tens of nanometers thick as measured by AFM.

After making the polyaniline film, the chip is rinsed in water and then solution gated. The macroscopic gate electrode was placed in a glass micropipette with a tip diameter of a few microns filled with an aqueous solution of 0.5 M $HClO_4$. The pipette was positioned over the polyaniline device. As the chip was brought up to the pipette tip, the hydrophilic surface drew the acid over the chip's surface forming a small drop of solution over the electrodes. The drop remained connected to the reservoir of solution in the pipette and thus was in contact with the macroscopic gate electrode which controlled its potential. The entire device is illustrated in fig. 9.1 (from [4]).

A typical measurement of a polyaniline film is shown in fig. 9.2. When one

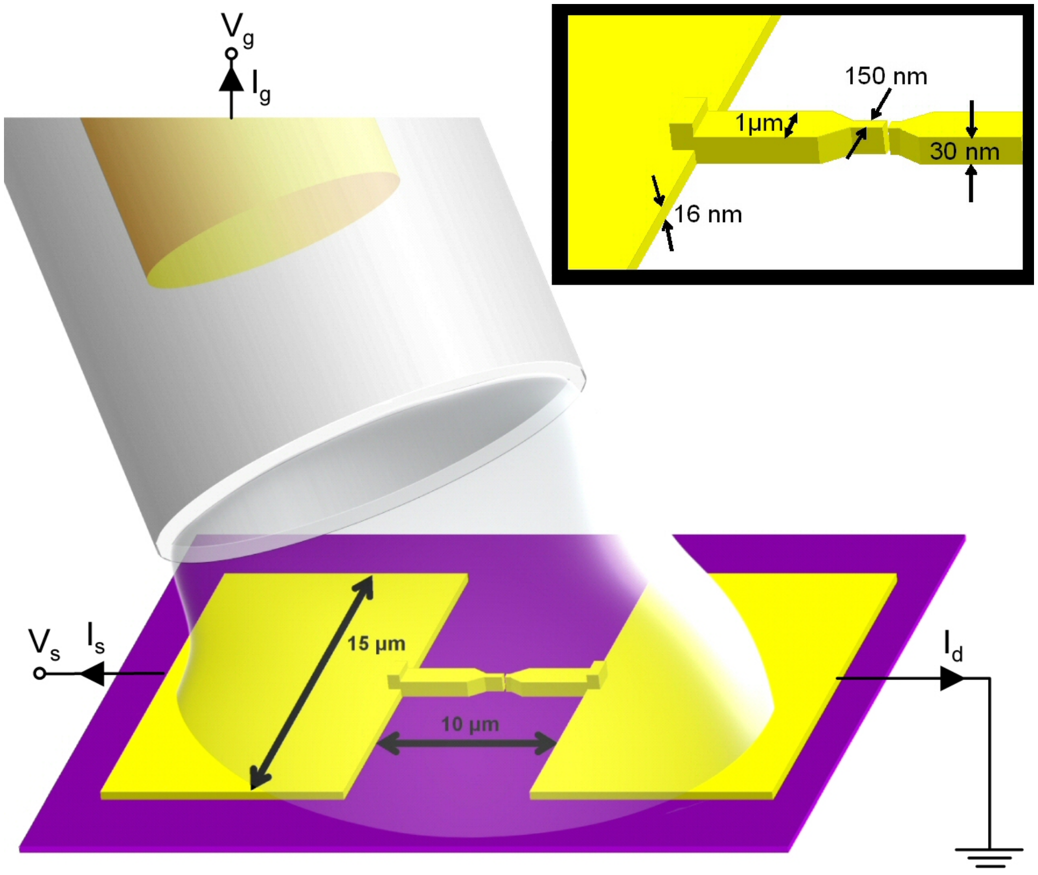


Figure 9.1: Setup used for solution-gating polyaniline transistors (figure courtesy of J. Grose and B. Ülgüt)

sweeps the gate voltage, the conductance of the film initially increases by a factor of 10^6 and then decreases back to a negligible value. The mechanism behind this modulation is that PANI has three distinct structural forms, only one of which is conducting in an acidic solution. As the gate potential is swept, the potential between the solution and the drain electrode (or the source electrode) forces the PANI to change from the insulating leucoemeraldine structure to the conducting emeraldine structure and then to the insulating pernigraniline structure. These changes in the structure are reversible. The conducting window in gate voltage keeps increasing with bias voltage.

It is our interest to make polymer films where only one strand of polymer makes it across from one electrode to the other. Jacob Grose is currently working on several ideas in order to do this. It may also be possible to use the mechanical junctions in order to pull and break polymer chains that have been formed across the electrodes.

9.2 Gated metal-nanoparticle SET's

Understanding how bulk properties such as superconductivity and ferromagnetism manifest themselves in the electronic states of small metal nanoparticles is an interesting subject [5]. Understanding the nature of electron interactions inside these small grains has been a focus of recent research [6, 7]. One experimental technique to do this is tunneling spectroscopy on a gated nanoparticle. Studying the evolution of electronic states as a function of the number of electrons on the dot gives us information on the nature of electron interactions in the particle [8].

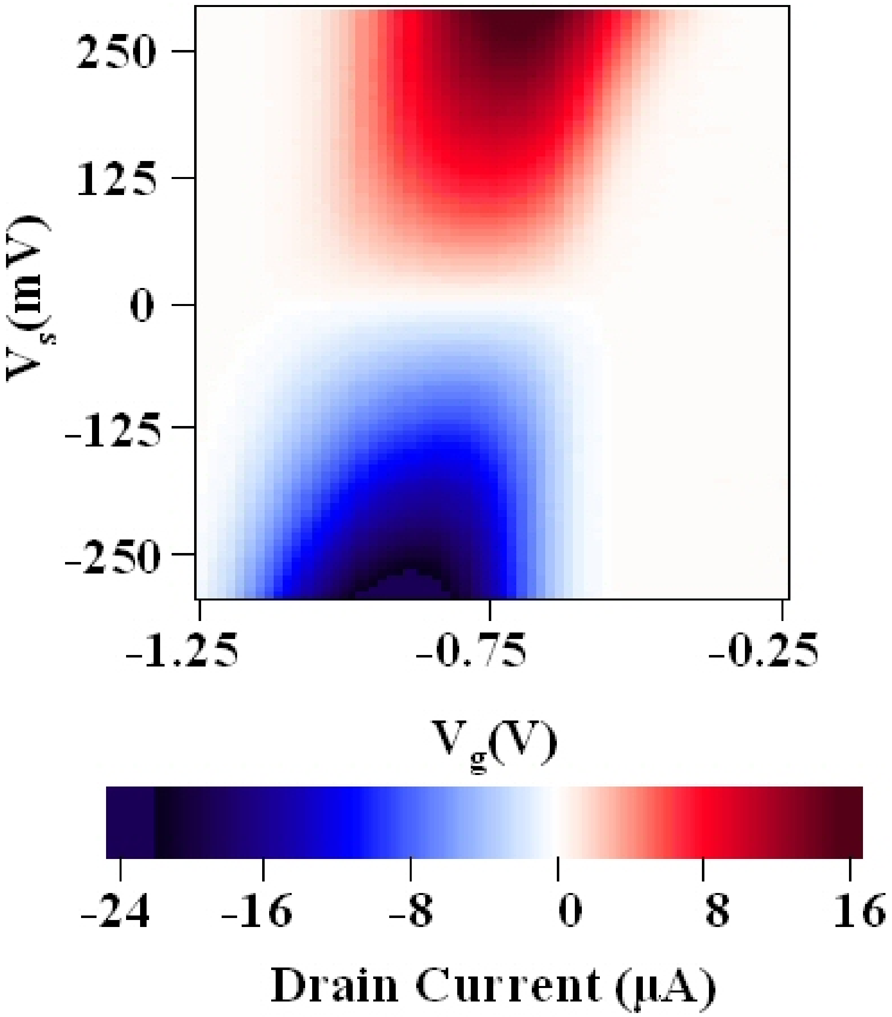


Figure 9.2: dI/dV plot of a polyaniline thin-film transistor.

The technique used till now to do this is the nanopore. The schematic of a typical gated nanopore device is shown in fig. 9.3 (a). We can see that this device has some undesirable features. For one, the parasitic capacitance between any two electrodes is very large (typically several nanofarads), limiting the speed of measurements. Secondly, given the large contact area between the gate and drain electrode, there is a good possibility of gate leakage. Thirdly, the gate has poor capacitive coupling to the nanoparticle. Making such devices turns out to be rather laborious as well [6].

In order to improve the device properties, Kirill Bolotin and Ferdianand Kuemmeth are making metal nanoparticle SET's using the planar break-junction geometry. An SEM image of a typical device is shown in fig. 9.3(b) (from [9]). We start with gold wires cleaned in oxygen plasma and submerge the chip in liquid helium. We break the wires using electromigration which results in a gap about 5-10 nm wide after the sample is warmed to room temperature fig. 9.3(c). The samples are then loaded into a high-vacuum evaporator. 20 Å of gold is evaporated at 0.6 Å/s, which self-assembles to produce particles with diameters of 5-15 nm as measured with SEM (fig. 9.3(c)). When measured immediately after the evaporation, approximately 25% of the junctions show a drop of resistance into the MΩ range, indicating that a nanoparticle may be bridging the gap.

We then cool the samples back down to liquid helium temperature and do I-V measurements as a function of V_G. In some cases, only a single particle contributed to transport between the electrodes resulting in the characteristics shown in fig. 9.4. From these plots, we see that the capacitance between the gate and the metal particle can be as large as 1 aF, which is an order of magnitude larger than that

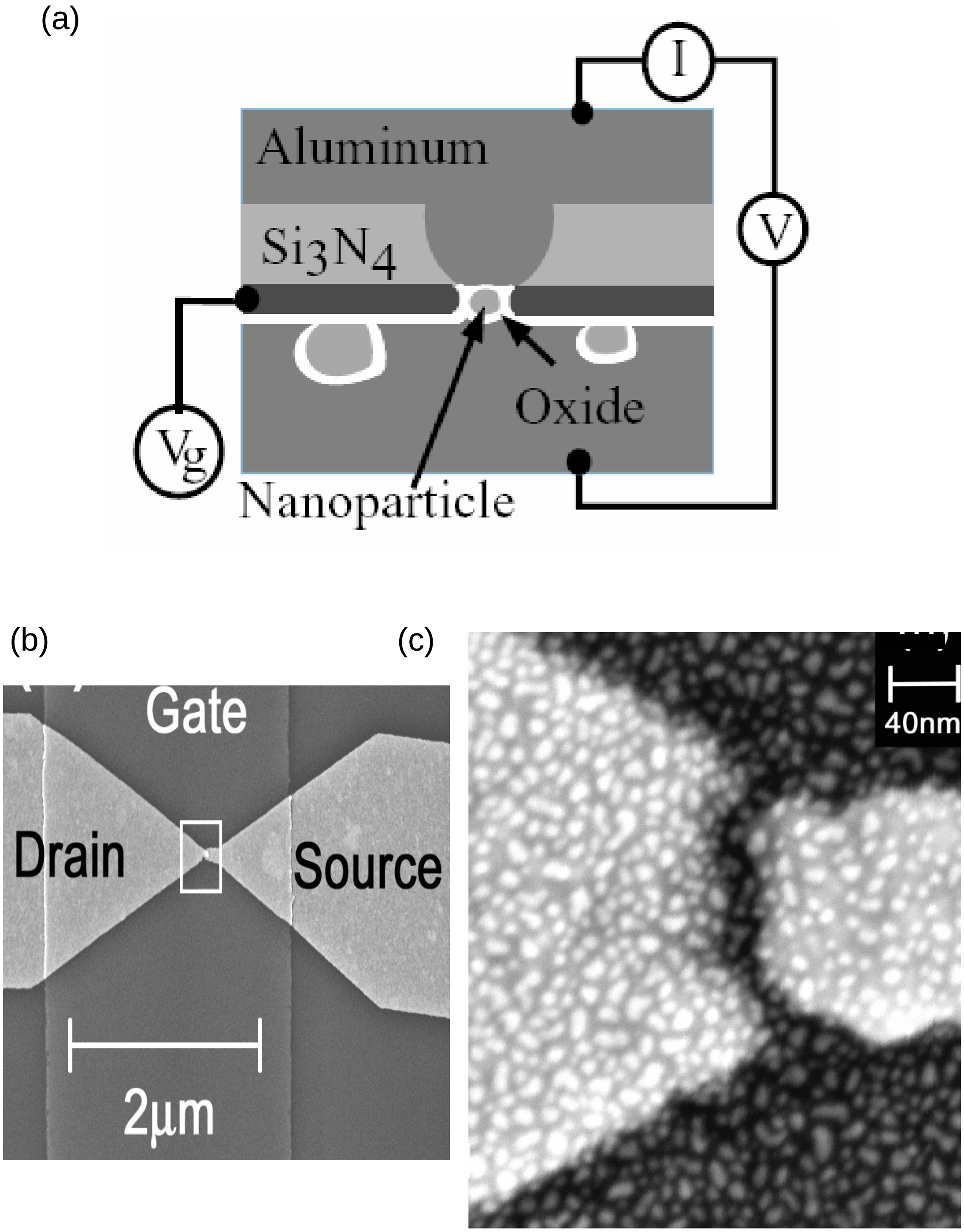


Figure 9.3: (a) Schematic of the gated nanopore device, from [6]. (b) and (c) (courtesy K. Bolotin and F. Kuemmeth) SEM pictures of the electromigration-based metal quantum dots.

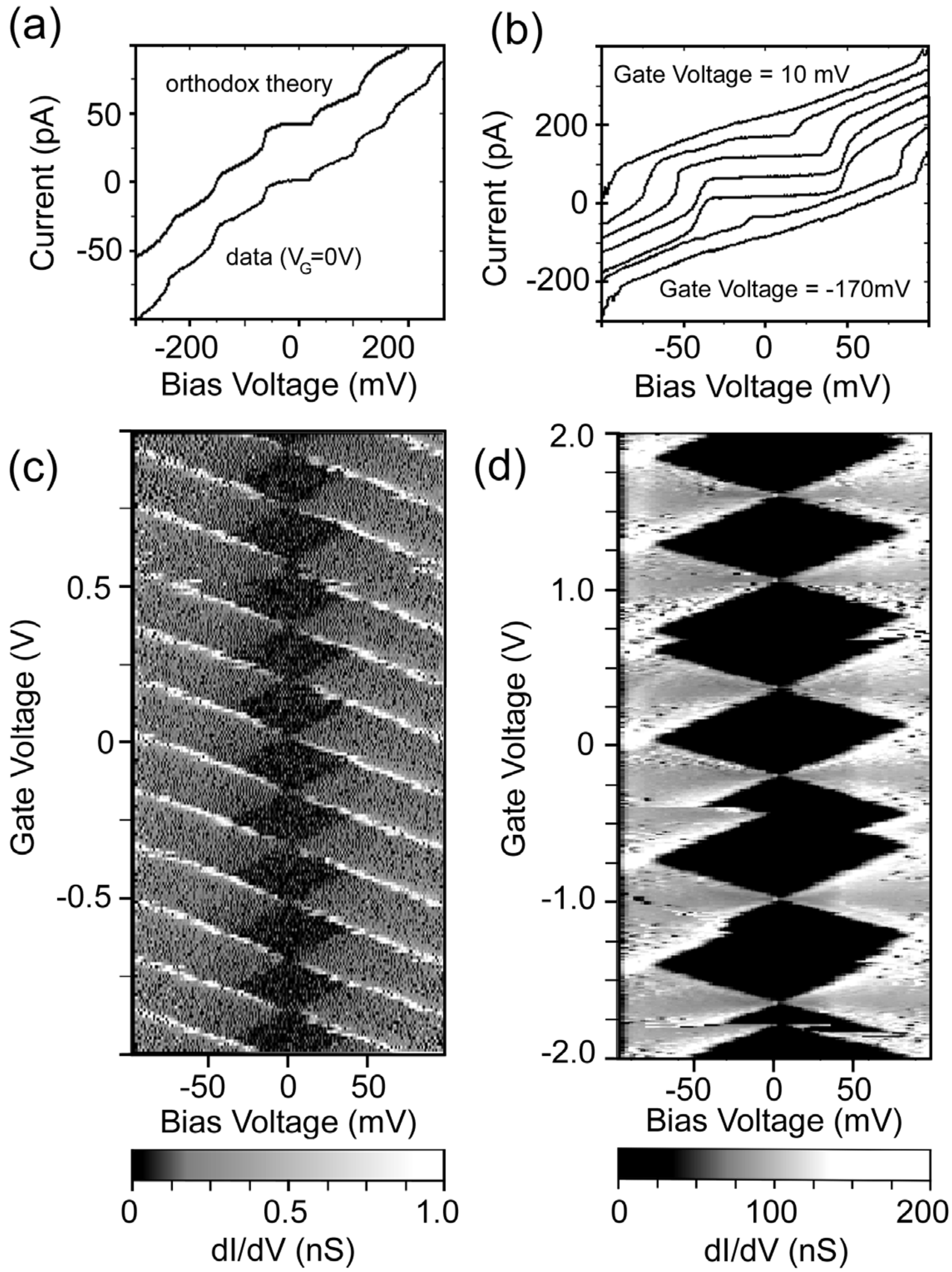


Figure 9.4: (Courtesy K. Bolotin and F. Kuemmeth) (a) and (b) *I*-*V* curves at different gate voltages in two gold quantum dots showing Coulomb blockade. (c) and (d) dI/dV plots showing that the charge state of the dot can be tuned by several electrons.

achieved with the nanopore technique. The charge state of the nanoparticle can also be changed by several electrons, as shown in fig. 9.4(c) and (d). The samples are stable enough to permit resolution of discrete electronic states [9].

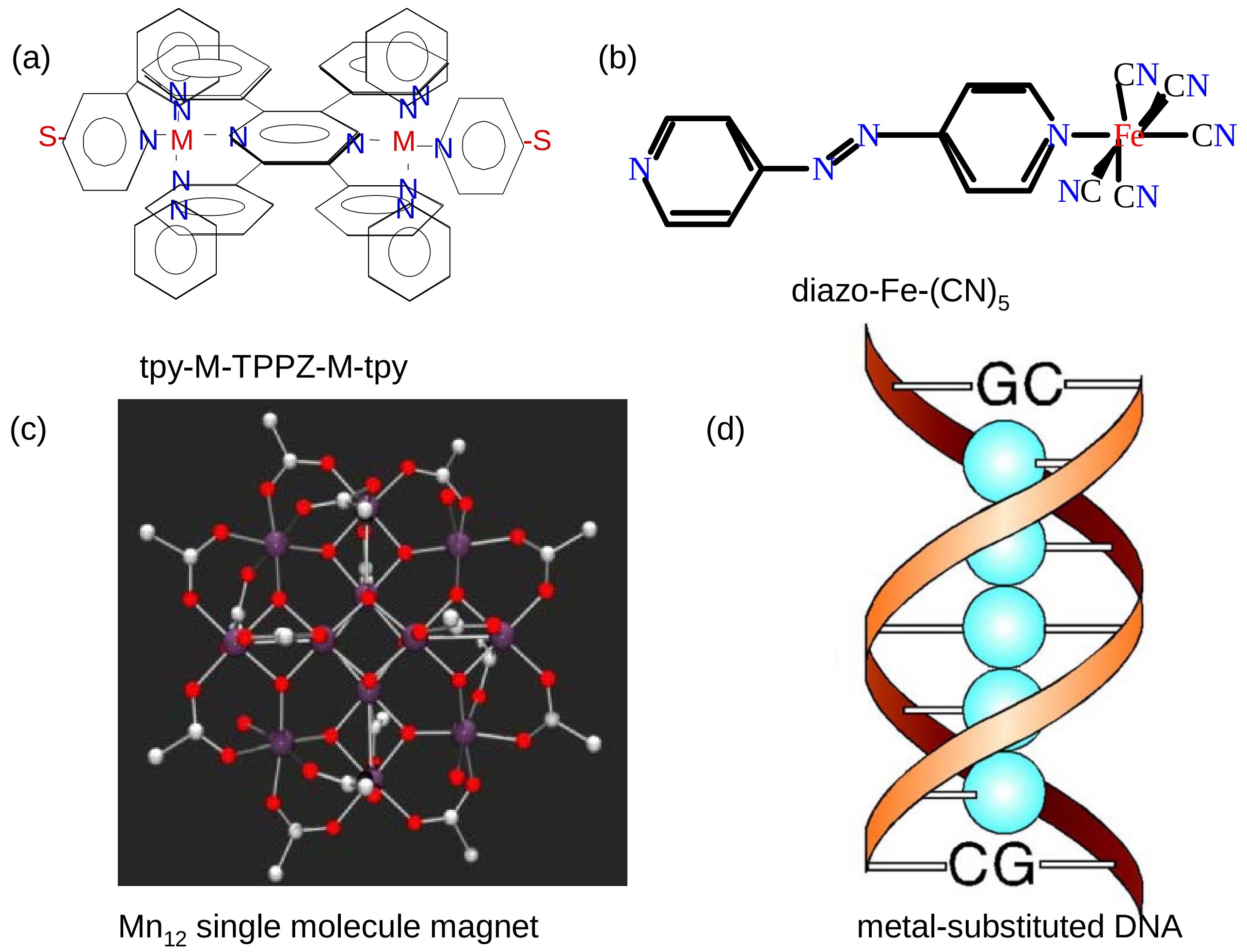
9.3 Future experiments

What does the future hold for the electromigration technique?

9.3.1 Single molecule experiments

One can think of a number of interesting experiments to do with single molecules. In general, the molecules that should be studied are the ones that show interesting electrochemical properties. An interesting candidate for example is the molecule shown in fig. 9.5(a). It is a close cousin to the molecules studied in chapter 4 and 5, but has two electrochemically active metal centers instead of one. It will be interesting to see if the charge state of this molecule can be changed by more than one by the electrostatic back-gate.

Other interesting molecules for transport studies are those having more elaborate geometries. Molecules that are sensitive to light or electromagnetic radiation (fig. 9.5(b)) will also be interesting candidates to study photon-assisted tunneling, for example. Single-molecule magnets (one is illustrated in fig. 9.5 (c)) have already been studied extensively by other techniques. It will be interesting to do transport measurements on these molecules - indeed, one such experiment is already being done [10]. One goal of the field might be to predict the form of designer molecules



tpy-M-TPPZ-M-tpy

diazo-Fe-$(CN)_5$

Mn_{12} single molecule magnet

metal-substituted DNA

Figure 9.5: Some interesting molecules for future transport measurements.

to produce a given transport property.

Another direction to take is to use different materials for the electrodes themselves. Chapter 7 is one such experiment, where we used ferromagnetic electrodes to study Kondo-assisted tunneling. Other interesting experiments can be done using ferromagnetic electrodes to create spin-polarized currents. I have also done some preliminary experiments with superconducting (aluminum) electrodes, looking for Kondo-assisted tunneling in the presence of superconductivity. These experiments promise to be relatively straightforward.

One drawback with the current technique for creating devices is the randomness of the final device geometry. As we have seen in the previous chapters, it takes a fair amount of statistics to make a claim with a fair degree of certainty. Now the questions we have asked thus far (say the vibrational mode of C_{140}) are reasonably independent of the exact device geometry. Asking more complicated questions will likely be a difficult task. The development of better experimental techniques or the use of multiple techniques will likely be necessary.

9.3.2 Polymer experiments

As noted earlier, conducting polymers are an interesting class of materials to study with the break-junctions, if single strands of polymer can be made to cross the electrodes. Even in the event that many such strands cross between the electrodes, transport measurements should still give insight into the nature of intra-strand electron transport.

It will be interesting to study polymers that are used for solar cells using the electromigration junctions. In solar cells, it is essential that electron-hole pairs make it to the electrodes before they have a chance to recombine in the material. The electromigration geometry (or related fabrication geometries) will help this happen. It may be possible therefore to study the polymers in a regime where there is little electron-hole recombination, something that has not been done to date.

9.3.3 Nanoparticle experiments

The metal nanoparticle experiments in the electromigration geometry have a bright future. Kirill and Ferdinand have already begun experiments on a number of different materials. Especially interesting are experiments where the electrodes are made from ferromagnets, in order to cause spin-polarized currents to flow through the nanoparticle [11]. Also interesting are possible studies of the lifetimes of electrons in excited quantum states in nanoparticles using high-frequency pulses.

9.4 Summary

In summary, I have described a technique to make two electrodes separated by a nanoscale gap which are also a few nanometers away from a gate electrode. I have described how molecules and nanoparticles can be incorporated into the gap and the transport properties of these devices.

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