THE KINETICS OF CHARGE TRAPPING IN POLYCRYSTALLINE PENTACENE AND ION MIGRATION IN LIGHT EMITTING ELECTROCHEMICAL CELLS STUDIED BY TIME- AND TEMPERATURE-RESOLVED ELECTRIC FORCE MICROSCOPY

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by

Michael J. Jaquith

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THE KINETICS OF CHARGE TRAPPING IN POLYCRYSTALLINE PENTACENE AND ION MIGRATION IN LIGHT EMITTING ELECTROCHEMICAL CELLS STUDIED BY TIME- AND TEMPERATURE-RESOLVED ELECTRIC FORCE MICROSCOPY

Michael J. Jaquith, Ph.D.
Cornell University 2009

The microscopic mechanisms by which charges trap in organic electronic materials are poorly understood. While trapping and bias stress in thin film transistors have been investigated through bulk techniques, these efforts cannot account for the known local variations of trap concentration and kinetics across the film. We show that electric force microscopy (EFM) can be used to follow local trap formation kinetics in working pentacene thin-film transistors. The trap formation rate we found was hole-concentration dependent, strongly suggesting a trapping mechanism involving one or more chemical reactions, or at least, we hypothesize, an activated process. Chemically modified pentacene also shows concentration dependent trapping despite the presence of functional groups that should inhibit the proposed chemical trap formation mechanisms. Furthermore, we found that electrons, injected by gate voltage in modified pentacene and by light in unmodified pentacene, clear trapped charges. When the trapped holes are cleared by electron injection, there is an uncharged intermediate species remaining which accelerates future charge trapping. Finally, we use variable temperature to show direct evidence that the trapping mechanism is an activated process.

In light-emitting electrochemical cells (LEECs) the redistribution of ions assists the injection of electronic carriers and leads to efficient light emission. The

mechanism of operation of LEECs has been controversial, and there is no consensus regarding the distribution of electric field in these devices. Here, we use EFM to directly observe ion motion within the channel of an operating LEEC. Initial results in a planar configuration show ion migration on top of the electrodes. To properly test the models, the organic material was patterned solely between the electrodes. The observed ion motion agrees with the electrodynamic surface potential model: ions move to the electrodes to assist injection.

BIOGRAPHICAL SKETCH

Michael Jaquith was born on January 18, 1981 to Don and Candy Jaquith in a small northern Michigan town named Petoskey. In 1982 Joshua Jaquith was born, and in 1985 Sarah Jaquith was born. The family lived in a small house for many years. When his parents divorced, his mother took up a job as an accountant, maintained the household, and raised the children. He spent a tremendous amount of time outdoors: hiking, swimming, skiing, and enjoying all that northern Michigan wilderness has to offer. His father's parents, who always remained close to the family, offered their grandchildren camping expeditions, leisurely summers at a small cottage on an inland lake, and more.

Michael's education began in a private Christian school, but left after 4th grade to attend public schools where more extracurricular activities were available. He participated heavily in the High School Band, Debate and Forensics Club, and advanced classes. In 1999, Michael graduated from Petoskey High School and enrolled at Michigan Technological University. Unable to decide between Chemistry and Chemical Engineering, he took up both majors. He graduated in 2003 with two Bachelor's degrees.

After applying and having been accepted to both Chemistry and Chemical Engineering programs at many universities, he chose to come to Ithaca, NY to attend to Cornell University. He enrolled at Cornell in July 2003, and began taking classes. By December 2003, he joined the group of Dr. John Marohn working on the material presented in this Thesis. He will next head to Portland, Oregon to work for the Process and Technology division of Intel.

No effect that requires more than 10 percent accuracy in measurement is worth investigating.

- Walther Nernst (1864-1941). Nobel prize, 1920

I often say that when you can measure what you are speaking about, and express it in numbers, you know something about it; but when you cannot measure it, when you cannot express it in numbers, your knowledge is of a meagre and unsatisfactory kind.

- Lord Kelvin (William Thomson, 1st Baron) (1824-1907)

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Professor John Marohn has been the largest contributor to the completion of this thesis. Any acknowledgement before thanking him for his guidance and inspiration would be inappropriate. He has created an environment that emphasized scientific accuracy over expediency, careful consideration of all the implications of a measurement over rapid publication. He's allowed me to explore the world of scientific research while in a stable and safe atmosphere. He's taught me the value of careful planning, patience, and thoroughness both before and while conducting an experiment. Most of the scientist that I am now, I owe to John.

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I'd like to thank collaborators in the lab of Professor George Malliaras. John Defranco is the master of organic liftoff technologies and has created many fantastic devices for me to study. Jason Slinker organized the first light emitting electrochemical cell project and worked tirelessly to provide working devices for me to study. Vladimir Pozdin has taught me a great deal about pentacene evaporation. Dr. Alex Zakhidov helped create novel device structures for the pentacene

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Thanks to my committee, Professors George Malliaras, Héctor Abruña, and Roald Hoffmann for their time and comments. I'd like to especially thank Professor Malliaras for both creating opportunities for and supporting many collaborative efforts.

Family

I'd like to thank all of my family for supporting me during my many years of schooling. My mother has been my stalwart proponent and public advocate at all times. My grandfather has been a role model and example for my entire life. All of my nuclear and extended family have given me support which I did not fully appreciate until I had observed the lack in others. Most of the human I am, I owe to my family. Their love and support has helped me far more than the most successful experiment or the most beautifully aligned instrument.

I'd also like to thank my extended adopted families: The Weavers gave me a supportive environment when things looked down, Dave has been a brother for many years. I've always been accepted and welcome, far beyond anything I deserved. The Tillotsons lead me to Catholicism. Paul, in addition to patient discussion, introduced me to new ways to have fun outdoors while remaining my partner in outdoor- and food-related altercations.

Friends

I chose Ithaca because of the beautiful surroundings and natural setting, but the true beauty here has been the friends I have made. I'd like to thank all of my friends through IAUA, especially Frank, Todd, Barry, Stephanie, Gavin, Sue, boB, Jeff T, Bill T, Jim, Mike, Jeff, Claire, Elaine, Penn, Rob, and many, many more. You've

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TABLE OF CONTENTS

Biographical Sketch . . . iii
Dedication . . . iv
Acknowledgements . . . v
Table of Contents . . . viii
List of Figures . . . x

1 Introduction **1**
1.1 Organics . . . 1
1.2 Pentacene . . . 2
1.3 Charge Trapping Candidates . . . 5
1.4 TIPS Pentacene . . . 15
1.5 Light Emitting electrochemical Cells . . . 17

2 Methods **20**
2.1 Brief History of Electric Force Microscopy . . . 20
2.2 EFM Basics . . . 22
2.3 Measurement Techniques . . . 26
2.4 Faster Frequency Determination . . . 31
2.5 Scan Types . . . 38

3 Kinetics of Charge Trapping in Polycrystalline Pentacene **43**
3.1 Introduction . . . 43
3.2 Methods . . . 46
3.2.1 Device Fabrication . . . 46
3.2.2 Atomic force microscopy . . . 47
3.2.3 Electric Force Microscopy . . . 48
3.2.4 Trap Kinetics . . . 48
3.3 Results . . . 50
3.4 Discussion . . . 52
3.5 Concluding Remarks . . . 53
3.6 Supporting Information . . . 54
3.6.1 Trap decay . . . 54
3.6.2 Analysis of charge trapping kinetics . . . 55
3.6.3 Force Distance Curve . . . 57
3.6.4 Author contributions . . . 58

4 Study of Charge Trapping in Modified Pentacene **59**
4.1 Introduction . . . 59
4.2 Methods . . . 60
4.2.1 EFM Details . . . 60
4.2.2 Device Fabrication . . . 64
4.2.3 TIPS Pentacene Deposition . . . 65
4.2.4 TES ADT . . . 65

4.3 Results 66
4.4 Discussion 74
4.5 Conclusions 78

5 Variable Temperature Study of Charge Trapping Kinetics 80
5.1 Introduction 80
5.2 Initial Observation of Trapping at Two Temperatures 81
5.3 Variable Temperature EFM Trapping Study 83
5.4 Using Light to Clear Charge Traps 90
5.5 Variable Temperature with Light 91
5.6 Atmospheric Exposure 94
5.7 Monolayer Pentacene 96
5.8 Pentacene Conclusions 102

6 Imaging Ion Motion and Internal Electric Fields in Transition Metal Light Emitting Electrochemical Cells 103
6.1 Introduction 103
6.2 Methods 104
6.2.1 Device Fabrication 104
6.2.2 Electric Force Microscopy 105
6.2.3 Optical Microscopy 106
6.2.4 Numerical Simulations 106
6.3 Results 107
6.4 Conclusions 116
6.5 Author Contributions 117
6.6 Correspondence 117

A Substrate Preparation Recipe 119

B XY Piezo Stage Construction Notes 121

References 127

LIST OF FIGURES

1.1 Three categories of organic semiconductors. 2
1.2 Chemical Structures 4
1.3 Pentacene Transistor Topography 5
1.4 Grain Boundary Barrier Model 6
1.5 Polarization Energy 8
1.6 Polarization Fields Adjacent Pentacene Domains 9
1.7 Density of States due to Dielectric Polarization 11
1.8 Trap Forming Reactions Proposed by Northrup 13

2.1 EFM Diagram 25
2.2 Parallel Plate Model 25
2.3 Tip Voltage Dependent Frequency 26
2.4 Trapped Charge as a Parallel Plate 27
2.5 Equipment Configuration for Different Measurement Types 29
2.6 Trap Release in Pentacene 32
2.7 Commercial Instruments 33
2.8 Time Variant Frequency Example 34
2.9 Filter Effects of Frequency Demodulator 35
2.10 Bandwidth Test Schemes 36
2.11 Bandwidth Test Results 38
2.12 Frequency Demodulator Noise 39
2.13 Examples of Images 40
2.14 Examples of Linescans 41
2.15 Example of a pointscan 42

3.1 Charge Trap Detection Scheme 45
3.2 Scheme to Measure Charge Trap Formation Rate 46
3.3 Topography and Charge Trapping in Pentacene 47
3.4 Equilibrium Results of Charge Trapping 50
3.5 Trapped Charge Release in Pentacene 54
3.6 Attempted Kinetic Fit of Formation Rates 55
3.7 Charge Trapping Kinetic Fit Results 57
3.8 Cantilever Force Distance Curve 57

4.1 Modified Pentacene Structures 61
4.2 Crystal Packing of TIPS-Pentacene 62
4.3 Crystal Packing of Pentacene 63
4.4 Crystal Packing of TES ADT 63
4.5 Topography of TIPS Pentacene 67
4.6 Charge Trap Patterns in TIPS-Pentacene 69
4.7 Kinetics of Trap Formation in TIPS Pentacene 71
4.8 Passive and Active Trap Clearing in TIPS Pentacene 72
4.9 Hole and Electron Mobility Determination in TIPS Pentacene . . . 73

4.10 Charge trap performance of TES ADT 75

5.1 Techniques for determining charge trap formation and release rates. 82
5.2 Effect of Temperature Change on Topography and Trapping in Pentacene 84
5.3 Temperature Dependent Rates 86
5.4 Variations in Pentacene Charge Trap Formation Rate 92
5.5 Temperature Dependent Rates with Light 95
5.6 Effects of Air-Exposure on Pentacene 97
5.7 Charge Trapping in a Monolayer Pentacene Transistor 101

6.1 Potential Profiles in Unpatterned LEEC 108
6.2 Schematic Diagram of LEEC Devices 109
6.3 LEEC Patterning Process 111
6.4 Potential Profiles in Patterned LEEC 112
6.5 LEEC Simulations 114
6.6 Voltage Dependence of LEEC Performance 115

CHAPTER 1

INTRODUCTION

Here we cover the previous work done on the topics of this thesis. We start with a general discussion of organic semiconductors, moving to pentacene, then focusing on previous studies of charge trapping in polycrystalline pentacene. We then discuss the work done with a functionalized pentacene molecule: TIPS pentacene. Finally, we discuss previous work done with light-emitting electrochemical cells.

1.1 Organics

Organic semiconductors differ from inorganic due to the delocalization of electrons in the π-conjugated bonds through a molecule instead of delocalized electrons within a crystal lattice[1, 2, 3]. There are three general categories of organics: polymers, molecularly doped polymers, and small molecules, shown in Fig. 1.1. In this work we use small molecules. Organic semiconductors offer many potential advantages over developed inorganic semiconductors, including reduced price, mechanical flexibility, low weight, low temperature processing, and brighter displays[4, 5, 6]. Although they have been known about for a long time[7, 8], chemical purification and synthesis technologies[9, 10] as well as an understanding of intermolecular interactions and molecular energy levels[11, 12, 4] have enabled significant improvements. Organics are good candidates for light emitting diodes[13, 14, 15, 16, 17], solar cells[13, 18, 19], large area displays[1, 13, 20] and thin film transistors [21, 1, 22, 23, 24, 25, 26, 13, 17, 27, 20]. Although some organic semiconductor products have made it into the market (e.g. E-Ink Displays and the Sony OLED 40” TV), significant performance problems remain with many

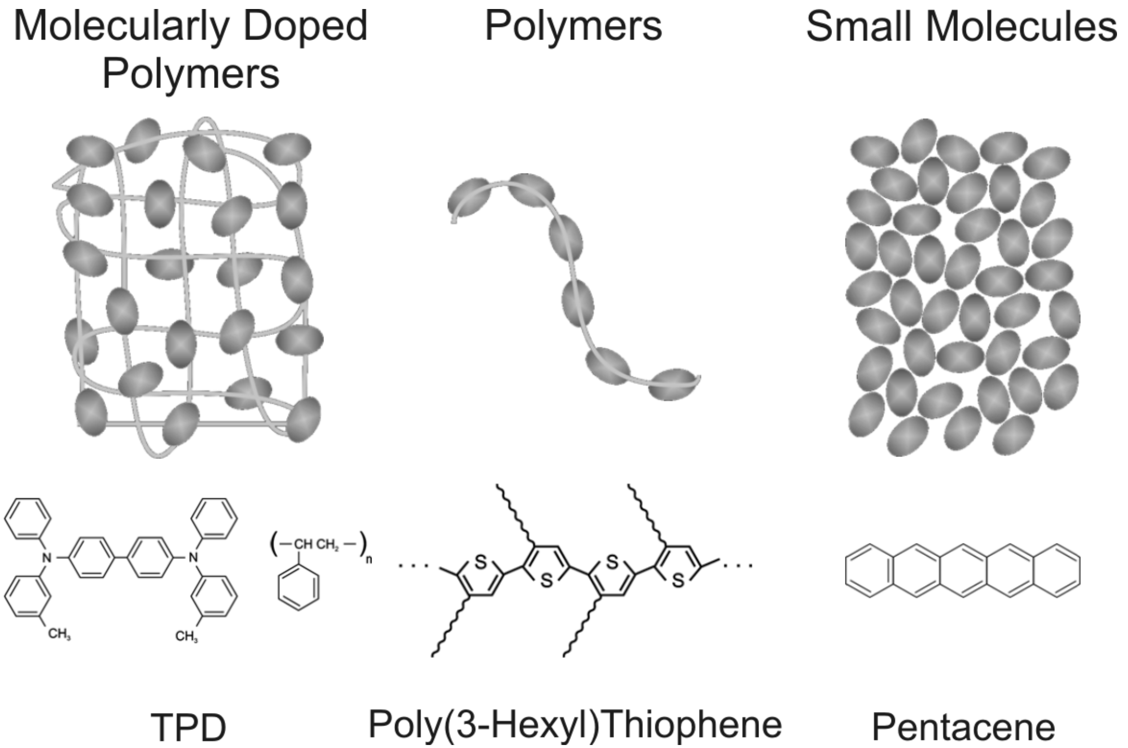

Figure 1.1: Three categories of organic semiconductors.

materials. This study focuses first upon Pentacene because, although it is one of the most widely studied materials, it still is not fully understood.

1.2 Pentacene

Pentacene, shown in Fig. 1.2a, is a leading organic semiconductor material because of its comparatively high mobility and it's ability to be deposited on flexible substrates at low temperatures. In 1991, Horowitz reported the first use of pentacene with a mobility (a benchmark of transistor performance[28]) of 0.002 cm^2/Vs[29]. Pentacene transistors with mobilities of 3.0[30], 3.3[31], and 5.5 cm^2/Vs[32] were reported in 2002, 2003 and 2006, respectively. This is approaching the theoretical

maximum of 10 cm^2/Vs suggested by quantum mechanical calculations[33, 34]. These calculations are not universally accepted due to a poor understanding of transport inside the pentacene film both due to trapping[34, 35, 36] and performance variation of the conductive states throughout the film[37]. Pentacene's performance is now similar to hydrogenated amorphous silicon[38], making it an attractive alternative for low-cost large area applications[39].

The goal of this study is to gain a better understanding of pentacene thin-film transistors (TFT) in ambient conditions. Pentacene is a good material to study because it forms thin ordered films easily and has a simple chemical structure. An example of a pentacene transistor film is shown in Fig. 1.3. This particular transistor has a 5 μm gap between 50 nm tall electrodes, with a 25 nm layer of pentacene evaporated on top. The entire substrate is fabricated locally at the Cornell NanoScale Science and Technology Facility. The fabrication process was developed by Eric Muller[40], and is discussed in Chapter 3 and Appendix A. A full description of the fabrication process can be found in Eric's thesis[40]. A good transistor has high mobility and low threshhold voltage[28], though achieving reproducible mobility and threshold voltage is often difficult with organic materials[41]. The mobility is a measure of how easily injected charge can move through the device. There are many factors that affect mobility in pentacene, including purity[42], substrate roughness[43, 44], and exposure to water[45, 46, 47] or oxygen[48]. The measured mobility is also decreased when a mobile charge encounters an energy barrier or a local energy minima; the charge might become immobilized or "trapped" at that location. The threshold voltage is a measure of the voltage required to "turn on" a transistor. Many of the same factors that decrease mobility also increase threshold voltage[49, 50, 51, 43, 52, 53], including charge trapping[54, 47, 48, 50, 55]. Sometimes these trap sites are not immediately available, and appear over time as

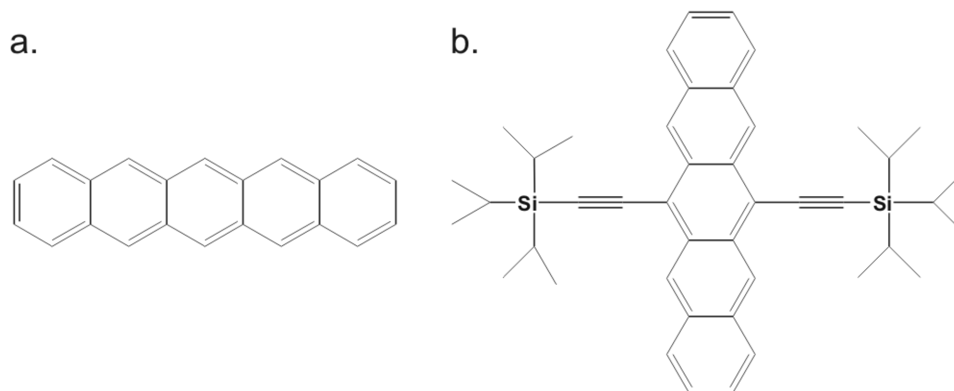

Figure 1.2: Chemical Structures

a. Pentacene, a five-ringed acene obtained from Aldrich. b. 6,13- bis(tri- isopropylsilylethynyl)pentacene or TIPS Pentacene, provided by Dr. John Anthony[59, 60].

bias stress[56, 57]. Bias stress arises from many factors, but may result in a drop in the current by a factor of 10 over time[58].

The first half of this thesis focuses primarily to understand charge trapping in polycrystalline pentacene. While the above macroscopic measurements are all affected by charge trapping, none of them provide a clear direct picture of what's really happening on a microscopic scale inside the material. Furthermore, differentiating the effects of charge trapping from other factors upon mobility, threshold voltage, and bias stress can be difficult. Direct study of this trapping process requires another technique. Here, we use electric force microscopy to directly image the traps inside of a polycrystalline pentacene film. This allows us to directly study charge trapping without the additional complications mobility or threshold voltage studies encounter. The experimental details are further discussed in Chapter 2.

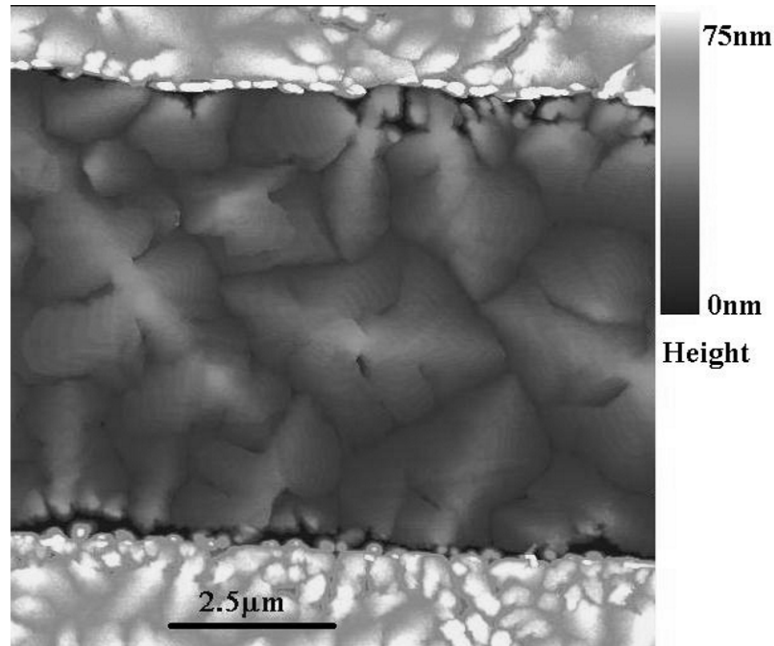

Figure 1.3: Pentacene Transistor Topography

Topography of a 25 nm pentacene thin film transistor by atomic force microscopy. The gold electrodes on top and bottom show smaller crystal size than the silicon dioxide channel in the middle. The grain size difference arises from a higher surface energy over gold than over oxide. It is energetically favorable for a pentacene molecule in the channel to migrate to a nearby formed crystal, while a pentacene molecule landing on gold is much more stationary.

1.3 Charge Trapping Candidates

Understanding the possible sources of charge traps is important to properly design a microscopy experiment. In this section I summarize the proposed trap candidates. The first trap candidate that gained wide spread support was the boundaries between pentacene crystals in polycrystalline samples. The boundaries between crystals (or grains) were connected with charge trapping because of the observed correlation of grain size and mobility[61, 38, 43, 44, 62, 63, 50] as well as the vacuum performance[64] and threshold mobility[52]. The mobility was found to drop quickly for grain sizes less than 2 μm, in agreement with modelling of a

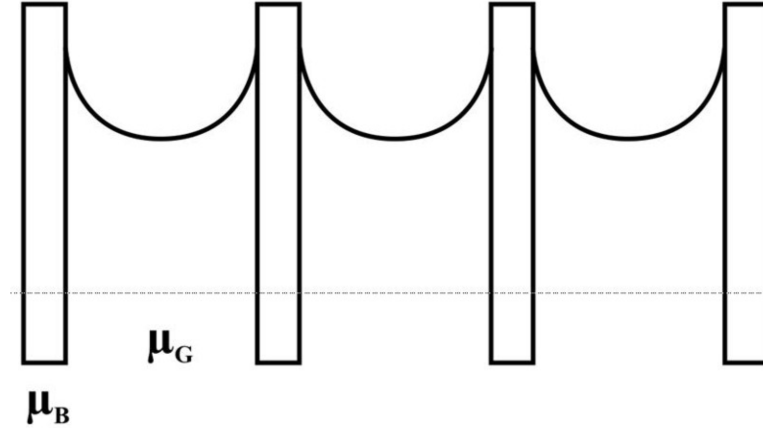

Figure 1.4: Grain Boundary Barrier Model

Model of high mobility grains with low mobility or barrier-like grain boundaries, adapted from Ref. [69].

single energy trap state at the grain boundary[65]. Single crystals of pentacene show bandlike transport[66, 67, 68] while polycrystalline pentacene is much more complex[6]. Different models have been proposed: Lin *et. all.* suggests that potential barriers exist at the grain boundaries similar to those seen in amorphous silicon[62]. Dimitrakopoulos *et. all.* advances the multiple trapping and release model, which is widely used to model the behavior of amorphous silicon transistors and suggests that grain boundaries give rise to energetic minima that form potential wells[69]. Horowitz *et. all.* proposes that grain boundaries give rise to back-to-back Schottky barriers[70, 71], shown in Fig. 1.4. Finally, Street *et. all.*[72] and Schön *et. all.*[63] propose that trapping at localized gap states[72, 63] is due to acceptors at the interface of grains. This would result in a net positive charge on the grain boundary. The Street data also suggests that Lin's barrier model does not apply.

It's important to note that although definite correlation between grain borders and device performance has been established, the reason why is not sufficiently understood. One study[70] found that the mobility varied from 0.11 to 0.28 cm^2/Vs

with a corresponding grain size change from 60 to 330 nm at room temperature. This device is modeled as high mobility regions within the grain in series with a low mobility grain boundary. However, dopants are assumed without quantifying their concentration, and the overall model doesn't explicitly state why the grain boundaries have such low mobility. A similar study[71] uses the multiple trapping and release model from amorphous silicon[73] with an assumed density of states to form a qualitative model of back-to-back Shottky barriers between grains. This study assumed tunneling and thermionic emission was the mechanism for moving charges across the grain boundary, though these would not be expected to result in mobility as high as that seen in pentacene. One possible mechanism of trap formation is atmospheric exposure[74], a process available only at the surface and intersections of grains. Grain boundaries are still considered a very likely source of charge trapping, though the mechanism is not agreed upon.

Another primary trap candidate arises due to the large polarization energies in polycrystalline pentacene[36]. Polarization can be viewed as the electronic reorganization of the pentacene molecules surrounding a charged pentacene molecule. While these neighbors carry no net charge, their electron density is shifted because of the free hole. This effect gives rise to an effective reduction of the band gap of pentacene by the Polarization Energy (P), shown in Fig. 1.5, for the pentacene cation or anions. The valence band is raised by a value of P_+, while the conduction band is lowered by P_-, such that $P = P_+ + P_-$. While polarization energies are normally relatively small, the polarization energy calculated by Tsiper and Soos is P= 1.0 eV. Assuming pentacene is a simple dielectric (the electric displacement vector is equal to the product of the electric field vector with an isotropic dielectric constant), the polarization energy can be calculated to be 1.37 eV[40]. This large polarization energy likely explains the large difference between the gas phase

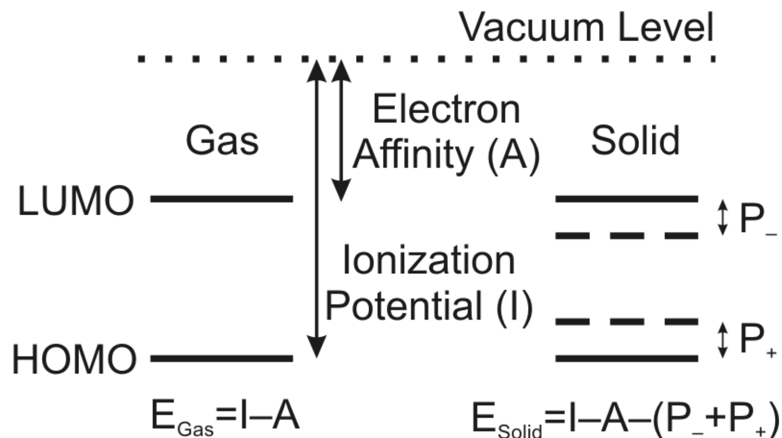

Figure 1.5: Polarization Energy

Polarization Energy is available only in the solid state; it decreases the solid-state transport band gap from that of the air.

energy band gap (5.22 eV)[36] and the solid phase energy band gap (2.85 eV)[36]. The polarization field produced by a free hole will extend many molecules away from the charged molecule. In the simplified case of an isotropic dielectric constant of 3, 99% of the polarization energy is contained within a radius of 124 molecules. This means that charge transport depends on not only the physical properties of the molecule carrying the charge, but those of all the molecules in the entire region.

A large polarization field would not pose any potential problems in a perfect dielectric, where the electric displacement vector is parallel to the electric field. In real materials, however, the dielectric is a tensor, and the displacement vector is the dot product of the dielectric tensor with the electric field. An anisotropic dielectric tensor has off-diagonal elements and will result in some amount of electric displacement vector in a different direction from the electric field produced by the charge. In fact, the dielectric tensor of pentacene is highly anisotropic, meaning that the energy landscape of the charge depends strongly on the local orientation of the pentacene molecules. When a physical defect is present, e.g. a grain boundary, the electric displacement vectors in one orientation domain will not point in

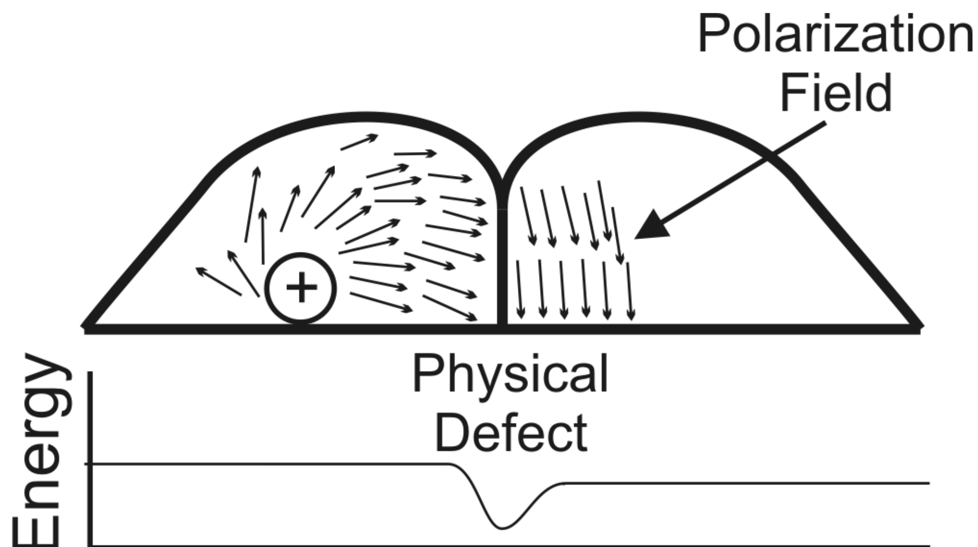

Figure 1.6: Polarization Fields Adjacent Pentacene Domains

Adjacent domains have differently orientated dielectric tensors. We hypothesize that the intersection of two domains creates a local energy minimum that may serve to trap charge.

the same direction as the electric displacement vectors in the adjacent orientation domain, shown in Fig. 1.6. We speculate that at the intersection of these two domains the energy may reach a local minimum, a possible charge trapping candidate. STM measurements of a pentacene film have confirmed that slight molecular shifting is responsible for shallow trapping[34].

Another possible trap candidate in organic thin film transistors is the underlying dielectric. There are two types of dielectric-related trapping: charge trapping in the dielectric itself and trapping in the organic semiconductor at the interface due to the dielectric. The first hypothesizes that charge flowing through the organic can fall into the dielectric and become trapped there. For example, both oxygen plasma and UV-ozone treatments of an organic polymer gate dielectric, parylene, introduce traps at the semiconductor-dielectric interface[75]. Optical measurements confirm the presence of a trap level at 420 nm in response to the treatment[75].

Modifying the dielectric layer with a self assembled monolayer has been shown to create both donor-like and acceptor-like trap states[54]. On silicon dioxide (SiO_2), pentacene growth starts as a wetting layer before the development of and between crystalline grains. Scanning capacitance microscopy measurements suggest the existence of trapped charges in the pentacene wetting layer[76]. The threshold voltage also reveals that the trapping phenomenon is strongly influenced by the structural ordering of pentacene adjacent to the pentacene/SiO_2 interface. Chemical modifications of SiO_2 surface reduce threshold voltage. A dielectric surface with alkyl chain functional groups leads to a highly ordered molecular structure in the channel thanks to a reduction of the surface energy, which could suppress the trapping site formation in the film as well as at the interface[77].

The second dielectric-related trapping candidate suggests that the dielectric layer itself may create charge traps in the organic semiconductor. This has been explored by Veres *et. all.*[78] studying small molecule transistors. In an organic thin film transistor, the region where charge transport takes place is buried under the bulk of the organic next to the dielectric interface. It is only a few nm thick. Furthermore, since organic materials show a very high variation in mobility with subtle orientation shifts, this accumulation layer orientation and packing are particularly critical. First, the dielectric surface must be smooth. Physical defects in the dielectric can cause deformations in the organic film, both significantly shifting the mobility and creating trap states[78]. Furthermore, it is observed that hydrophobic dielectrics seem to give better performance than hydrophillic dielectrics. Hydrophillic dielectrics used in field-effect transistors, e.g. SiO_2, tend to be more polar and thus have randomly orientated dipoles. These dipoles create electric fields that can shift the local potential inside the thin accumulation layer. While the net overall electric field produced by these dipoles is zero, there may be

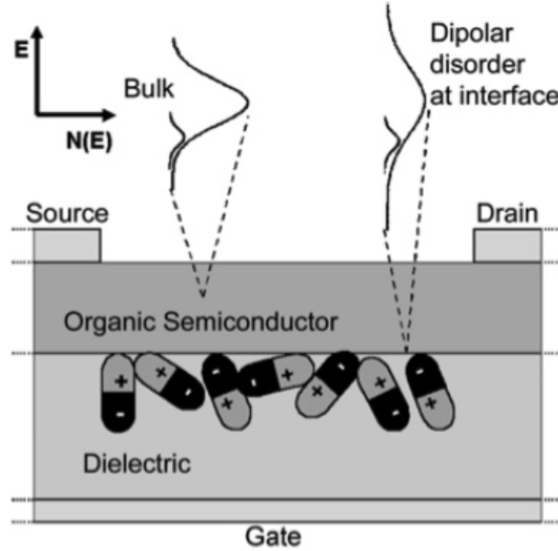

Figure 1.7: Density of States due to Dielectric Polarization

The density of states in the bulk of the semiconductor and at the interface with the dielectric. Local polarization may lead to an increase in the spread of site energies. Reproduced from Ref. [78].

local distributions which produce large fields into the first few layers of the film. These local variations give rise to a much wider density of states, shown in Fig. 1.7. Imagine a charge trap traveling through the accumulation layer. As it nears a region where all the local dipoles are orientated favorably, it may encounter a local minimum in the energy. It would fall into this lower energy states and become "trapped," unable to move further through the channel.

Another possible source of charge trapping is a chemical impurity. It has been known for some time that pentacene will react with atmospheric water[46, 45, 79, 53, 80, 81, 47] or oxygen[82, 83, 81, 53, 48], to decrease mobility and increase threshold voltage. Pentacene also reacts with hydrogen from a carrier gas[84]. Modeling moisture exposure as an increase of trap concentrations from 2 to $10.5 \times 10^{18}/\text{cm}^3$ at about 430 meV above the valence band edge agrees with current-voltage curves[47], but is not definitive. Photoconductivity measurements

of trapping rates suggest that atomic motion plays a role in both formation and quenching of charge traps[85]. A reaction mechanism for both the defect creation and trapping process was proposed by Northrup and Chabinyc[35], and is shown in Fig. 1.8. The impurities are formed by reactions between a middle carbon of pentacene and water, hydrogen, or oxygen either before or after film deposition. The impurity, e.g. dihydropentacene, requires another pentacene molecule and two holes (called a bipolaron) to form a trap. One of the central hydrogen atoms from the dihydropentacene molecule transfers to the normal pentacene molecule. When a hole removes one electron from each hydropentacene, some level of electron delocalization is restored and the molecules are stabilized. Although bipolarons are not intrinsically trapping, they have been suggested as a trapping mechanism in polymers as well[57]. These results could not explain why two holes were needed, possibly an intrinsic material property or associated with disorder, interfaces, or impurities.

One common source for Northrup's proposed impurities could be hydrogen carrier gas - commonly used to purify the pentacene prior to or during a deposition. At 1 atm of H_2, the formation of dihydropentacene is exothermic up to temperatures of about 400 °C[35]. This suggests that pentacene "purified" by hydrogen carrier gas is also heavily doped with dihydropentacene. At room temperature pentacene hydrogenation is a heavily exothermic process, by approximately 1.1 eV. The dihydropentacene defect has an energy level 0.34 eV above the valence band. Similarly. the hydrohydroxypentacene defect, formed by the reaction of pentacene and water, has an energy level 0.18 eV above the valence band. Both the H_2 and H_2O defects of pentacene can also give rise to n-type traps, at energy levels of 0.8 and 0.62 eV above the valence band, respectively. It is important to note that the reactions proposed by Northrup for trap formation will have both an ac-

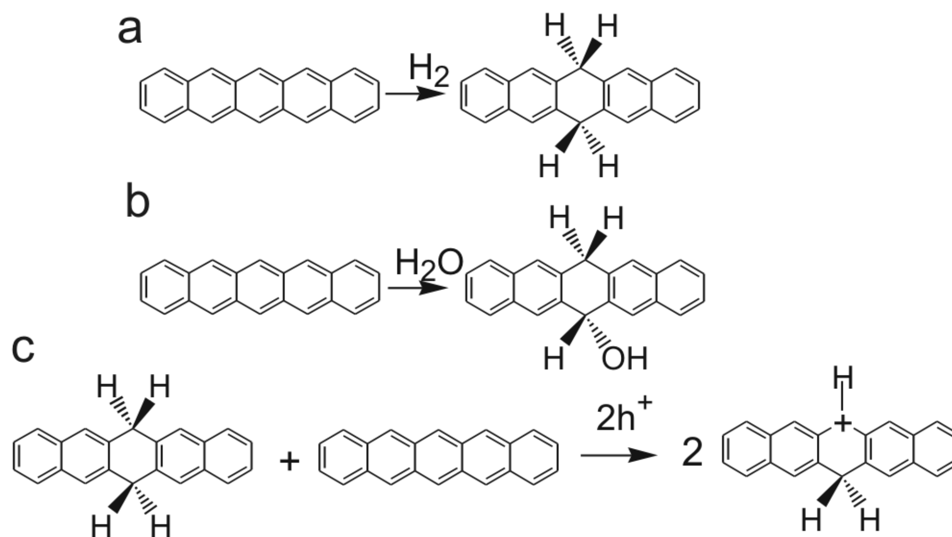

Figure 1.8: Trap Forming Reactions Proposed by Northrup

The pentacene molecule initially reacts with either a. hydrogen or b. water forming an impurity in the film. c. This impurity can react with free holes and another pentacene molecule to form the chemical traps. Adapted from Ref. [35].

tivation energy and reaction time arising from the atomic motion. Ramirez finds that chemical purity plays a significant role[86, 85], and trap formation activation energy of 0.67 eV, suggesting atomic motion[87]. This is fundamentally different from the previously considered energetic trapping scenarios, where the trap site is fully created before the arrival of the free charge and the charge must simply fall into an existing trap. Furthermore, many of the grain boundary studies could potentially be explained by the exposure of the pentacene molecules along the edge of the grain to atmosphere, creating the defects Northrup predicts.

Many of the above studies are supported with an array of bulk measurements: potential-current curves, mobility, threshold voltage, and bias stress. Although easy to measure even at various temperatures, all of these bulk properties share a common flaw: they are unable to measure local effects and produce only average values. Potential-current curves make assumptions about the contacts between organic semiconductors and metal when trying to extract performance parame-

ters. Good contact between an organic semiconductor and metal is difficult to achieve[41], and thus model assumptions about them are likely to be wrong. Mobility determinations suffer from similar contact assumptions. While threshold voltage does give an indication of charge trapping, it only gives an average value without any accompanying microscopic information about the distribution. Most models assume homogenous charge trapping, shown to be false in polycrystalline pentacene[88]. Bias stress measurements are complicated by the interpretation. It is difficult to differentiate charge trapping from molecular disorder or interfacial effects through bias stress[57].

Electric Force Microscopy (EFM) is able to avoid many of the above problems by imaging the local electrostatic potential, explained in Chapter 2. The effect of the metal-organic contact can be measured locally, avoiding assumptions about the quality. Charge trapping can both be imaged and measured on a local scale, creating a map of trapped charge in the device channel[88]. Both charge trapping and local structure can be measured locally across a sample, allowing a much clearer picture of the trapping process. Before the work in this thesis, EFM had been used to make static images of charge distribution through a polycrystalline pentacene film by Erik Muller[88]. This thesis describes several innovations: We improved the measurement speed by three orders of magnitude to allow real-time imaging of trap formation and measurement of formation kinetics discussed in Chapter 3. We modified the probe to allow and track variable temperature studies. This enabled us to extract an activation energy for the trapping process. Finally we introduced light into the experiment, allowing both quick trap clearing and exploration of the trap formation process. Although trap formation is a process with several steps, intermediate species show slow decay and only the final trap species reacts quickly with light. These discoveries are discussed in Chapter 5.

1.4 TIPS Pentacene

Polyacenes variants of pentacene are being explored by many groups for use in electronic devices [59]. Anthony *et al.* recently introduced a new family of functionalized polyacenes with improved solubility and controllable π-orbital overlap in the solid [89, 90]. In this class of molecules the central carbons of the acene are decorated with a bulky group tethered to the acene by a rigid alkyne. Analogous fluorinated acenes [91] and conjugated polymers [92] have also been developed.

Two soluble pentacene derivatives that have gained considerable attention in thin-film transistor applications are 6,13-bis(tri-isopropylsilylethynyl) pentacene [93, 94, 95, 96, 97] (TIPS pentacene) and triethylsilylethynyl anthradithiophene [98, 94, 99, 100, 101] (TES ADT). With optimized deposition, both molecules exhibit field-effect mobilities comparable to that of vacuum-deposited pentacene. TIPS pentacene has been used in solar cells [102] and ring oscillators [103] as well.

For these applications the molecules must be resistant to both photodegradation and charge trapping, in addition to having high mobility. The photodegradation of TIPS pentacene has been studied in both solution and in films by optical absorbtion and mass spectroscopy [104, 105]. Maliakal *et al.* propose that, in solution, photoexcited TIPS pentacene transfers an electron to oxygen, with subsequent reactions of the pentacene radical cation and the superoxide anion leading to endoperoxide and dimeric peroxide TIPS pentacene photoproducts [104]. They rationalized the higher rate of photodegradation of TIPS pentacene versus penacene films as due to the higher diffusivity of oxygen in TIPS pentacene films. Coppo *et al.* have studied the photochemistry of TIPS pentacene in the absence of oxygen. They find that photoexcited TIPS pentacene reacts by a 4+4 intermolecular cycloaddition [105].

Indirect evidence for charge trapping in photoexcited TIPS pentacene can be seen at long times (seconds) in 2- and 4-terminal electrical measurements of thermally stimulated current [106, 107]. These studies have led to the proposals that the silyl side groups on TIPS can trap electrons and that rearrangement of the lattice might trap a electron-hole pair [106]. Charge trapping in acenes, including TIPS pentacene, have also been examined at short times (picoseconds) in THz photoconductivity experiments [108]. While little evidence of charge trapping in TIPS pentacene was found in these studies, this is perhaps not surprising given that in pentacene films, charges were found to trap on the milliseconds to seconds timescale and at a rate that was supralinearly dependent on charge carrier concentration [88, 109]. Shallow traps have been invoked to rationalize the charge-concentration dependent (e.g., gate-voltage dependent) mobility observed in variable-temperature measurements of TIPS pentacene transistors [110, 111].

While TIPS Pentacene could undergo Northrup's proposed addition[35], the large functional groups should significantly decrease the rate of impurity formation. Furthermore, TIPS has a crystalline packing significantly different from that of unmodified pentacene. Unmodified pentacene crystallizes into a herringbone configuration with roughly 3.78 Å between the center carbons of two adjacent molecules, as determined by X-ray crystallography[112]. The TIPS structure, however, is composed of interleaved molecular plates, in just the same way that bricks are laid and produce a wall of molecules connected in 2-D[113]. There is 3.5 Å between sheets[93, 114], meaning that central carbon atoms of TIPS are roughly 16 Å apart. Northrup's mechanism requires a hydrogen to migrate from the center carbon of one impurity to that of an adjacent pentacene; it is unlikely to occur over such large distances.

Here we explore the spatial distribution of charge trapping *directly* in unilluminated TIPS pentacene and TES ADT films using vacuum electric force microscopy [115, 88, 109]. These results are discussed in Chapter 4.

1.5 Light Emitting electrochemical Cells

In addition to studies of charge trapping in pentacene and pentacene derivatives, this thesis includes work done on Light Emitting Electrochemical Cells (LEECs), a type of solid-state ionic device. This work was done in collaboration with Jason D. Slinker, John A. Defranco, and George Malliaras in the Cornell Department of Materials Sciences; Yu-Wu Zhong, Héctor D. Abruña, and John Marohn in the Cornell Department of Chemistry and Chemical Biology; Jose M. Moran-Mirabal and Harold G. Craighead in the Cornell Department of Applied and Engineered Physics. The original text of the paper was written by Jason D. Slinker, most of which is reproduced in Chapter 6 of this thesis.

The field of solid-state ionics encompasses a broad range of materials, such as ceramics, polymers and glasses[116, 117]. The identifying characteristic of this class of materials is their ability to transport ions in the solid state. Ionic space-charge effects can be exploited to facilitate changes in the optical, mechanical or electrical properties, giving rise to a host of applications in chemical sensors[118, 119], electrochromic windows[120], fuel cells[121], batteries[122, 123] and solar cells[124, 125]. Of particular interest within this class of materials are mixed conductors, in which, in addition to ionic conductivity, significant electronic conductivity is also present. The coupling between ionic and electronic carriers in mixed conductors offers rich physics and unique potential in devices[117]. An ex-

ample of such a device is the light-emitting electrochemical cell (LEEC), which recently received attention for its potential in flat-panel display and solid-state lighting applications[124, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159]. LEECs consist of a mixed-conductor layer sandwiched between two metal electrodes. A typical example of a mixed conductor used in LEECs is ionic transitionmetal complexes (iTMCs), such as ruthenium tris-bipyridine hexafluorophosphate[124, 141, 138, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159], $[Ru(bpy)_3]^{2+}(PF_6^-)_2$. The ruthenium complex is an (intrinsic) molecular semiconductor, in which the highest occupied molecular orbital (HOMO) is the t_{2g} orbital of the metal, and the lowest unoccupied molecular orbital (LUMO) is a π^* orbital of the ligands. Upon application of a bias in this LEEC, holes and electrons are injected from the anode and the cathode, respectively, into the ruthenium complex. These carriers are transported towards the opposite electrode via hopping, and may recombine to produce light emission with a characteristic color that corresponds to the energy gap of the complex. Critical to the operation of these LEECs are the counter ions (PF_6^- in this example), which are mobile in the film and at room temperature. Their redistribution on the application of a bias assists the injection of electronic carriers and enables novel device architectures[124, 146, 147, 156, 157], including fault-tolerant large-area illumination panels[147, 157] as well as illumination panels that can be plugged directly into an a.c. power outlet[157]. The presence of both ionic and electronic carriers in iTMCs, as well as other mixed conductors, poses a significant challenge in understanding their device physics. This is illustrated by the lack of consensus on the distribution of the electric field in LEECs[124, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148,

149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159]. The two extremes are represented by the electrochemical model[133], which predicts a high electric field in the bulk of the film, and the electrodynamic model[128], which predicts high electric fields near the electrodes. In addition to its significant fundamental interest, understanding the device physics of mixed conductors is essential to enable the engineering of better devices.

CHAPTER 2

METHODS

In this chapter, we discuss the electric force microscope. We first look at a brief history of the microscope and how it works. We discuss the types of measurements performed, and how the speed of these measurements was increased during this thesis. Finally we discuss how these measurement techniques are used to image (both spatially and temporally) properties of organic devices.

2.1 Brief History of Electric Force Microscopy

At the end of the 19th century, Sir William Thomson, Lord Kelvin, invented an instrument with multiple metal plates to record weak electrical signals transmitted by the Atlantic Cable. The instrument was also able to test voltaic theory and measure contact potential differences between metals[160]. In 1986, the atomic force miscroscope (AFM) was invented[161] and was on its way to becoming a powerful tool. These two tools provided the inspiration for Scanning Kelvin Probe Force Microscopy (SKPM), invented in 1991[162]. SKPM uses a metal coated cantilever to measure local electrostatic potential, as follows. First the cantilever is brought near a surface. The difference in contact potential between tip and sample create a force on the cantilever. The contact potential is a function of both the chemical potential and electrostatic potential, discussed later. The force is measured (and usually compensated for) to determine the local electrostatic potential. Electric (or sometimes Electrostatic) Force Microscopy (EFM) is another name for the technique; EFM and SKPM are commonly interchanged throughout the literature. The advantage EFM and SKPM have over conventional force microscope techniques is the ability to see through low conductivity, uncharged, top layers to

the active layers of interest in multilayer electronic devices[115, 88]. The spatial resolution, however, is limited by how close the cantilever can be brought to the surface. In most of our work, we generally achieve a resolution of about 100 nm. Furthermore, it is able to reach single charge sensitivity at room temperature in high vacuum[163, 164, 165, 166].

The first application of EFM to study pentacene was by Frisbee *et all.*[167]. They compared top and bottom contact pentacene devices, finding that bottom contact devices had a larger potential drop at the contacts than did top contact devices. They concluded that bottom contact was contact limited. The second application of EFM to conduction through pentacene was by Jackson *et all.*[168], who studied the voltage drop at the contacts for different metal electrodes. Jackson concluded that lining up the band between organic and metal was important for injection. Muller and Marohn studied the location of long-lived charge traps in polycrystalline pentacene transistors[88]. They found that the charge trapping does not occur predominantly at grain boundaries as previously believed. Muller and Marohn produced the first images of charge traps in an active transistor and it was surprising that their findings agreed with none of the existing charge trap theories.

EFM has since become a more widely practiced technique to study pentacene. One study found potential drops in a top contact transistor that was assigned to pentacene damage during gold evaporation[169]. Phase-contrast EFM was used to visualize the potential drop in an working transistor occurring across domain boundaries[170]. Another study used the tip to inject charge into gold nanoparticles on top of pentacene islands, then measured the potential distribution[171]. This study was intended to explore EFM techniques to study charge injection.

Aluminum/pentacene bilayers were found to show thickness-dependent surface potential while the surface potential of gold/pentacene bilayers were thickness independent[32]. This may have been due to a potential barrier at the aluminum/organic interface arising from space charge. A more recent study by the Frisbee group finds potential wells at the grain boundaries[172] in monolayer pentacene transistors. They conclude that the grain boundaries in these very thin films are the source of hole traps. It is also observed that thin oxides allow charge to tunnel from the gate electrode to the pentacene, through the dielectric oxide and fill trap states in monolayer pentacene islands[173].

2.2 EFM Basics

The EFM microscope has changed from the early SKPM experiment, but many of the fundamental principles remain. The metalized cantilever is the heart of the instrument. A potential is applied to the cantilever, and the tip is brought near a surface shown in Fig. 2.1. The tip and surface can be modeled as a parallel plate capacitor with applied tip potential (V_T), shown in Fig. 2.2 over a typical transistor with source, drain, and gate. The energy (E) of a parallel plate capacitor is one half the capacitance (C) times the potential difference squared.

$$E = \frac{1}{2} C (V_T - \phi_C)^2 \tag{2.1}$$

Here the potential difference is between the applied tip potential (V_T), and contact potential (ϕ_C). The contact potential has two sources, both the chemical potential shift between tip and sample (μ) and the local electrostatic potential($\phi(x)$). The derivation of this relationship is discussed in Eric Muller's Thesis[40] and by

Silveira *et all.*[174]. There are several assumptions: First the charge on the tip is assumed to re-equilibrate instantly at each height as it oscillates. Secondly, the measured potential is treated as being independent on distance from the surface. The contact potential of an oscillating cantilever tip over an organic planar device can be expressed as:

$$\phi_C = \phi(x) - \frac{\mu}{e} \tag{2.2}$$

Because μ is an energy, we divide by the charge of an electron (e) to obtain potential. In practice, the chemical potential difference is constant over a surface and spatial variation in observed potential arises from local variation in the electrostatic potential. The chemical potential term is often neglected when large electrostatic shifts are present. The potential difference creates a force (F) on the cantilever, and the spring constant (k) of a cantilever changes due to the force gradient it experiences in the direction of movement. Because our cantilevers oscillate perpendicular to the surface (defined as z), the force on the cantilever (derived from the grand canonical free energy)[40] is:

$$F_z = \frac{\partial E}{\partial z} \tag{2.3}$$

$$\Delta k = \frac{\partial F_z}{\partial z} = \frac{1}{2}\frac{\partial^2 C}{\partial z^2}(V_T + \frac{\mu}{e} - \phi(x))^2 \tag{2.4}$$

The frequency (f) of the cantilever is proportional to the square root of the spring constant divided by the mass (m). When the tip potential matches the contact potential, Δk $\rightarrow$ 0 and the frequency and spring constant become the resonant frequency (f_0) and resonant spring constant (k_0), respectively.

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_0}{m}} \tag{2.5}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{k_0 + \Delta k}{m}} \tag{2.6}$$

Thus the observed frequency of the cantilever can be expressed in terms of the capacitance (C), applied tip potential (V_T), chemical potential (μ) and the electrostatic potential in the sample ($\phi(x)$), shown in Eq. 2.7.

$$f(V_T) \simeq f_0 - \frac{f_0}{4k_0}\frac{\partial^2 C}{\partial z^2}(V_T + \frac{\mu}{e} - \phi(x))^2 \tag{2.7}$$

To determine the local potential in an operating microscope, the tip is brought near the surface and the frequency measured as a function of tip voltage. As predicted by Eq. 2.7, the frequency is parabolic in applied tip voltage, shown in Fig. 2.3. The curvature of the parabola depends on the capacitance. As the tip gets closer to the sample, the capacitance increases - resulting in larger shifts in frequency. The position of the parabola depends on potential. The center of the parabola occurs where the tip voltage matches the local electrostatic potential.

When trapped charge is present, the measured electrostatic potential can be used to estimate the planar charge concentration. Again, the parallel plate approximation is used. The bottom plate is the gate, on top of which sits a dielectric (dielectric constant ϵ, thickness t). Let us model trapped charge as a surface charge (σ) on top of the dielectric shown in Fig. 2.4. The surface charge density is determined via Eq. 2.8. The derivation of this equation is presented in Eric Muller's thesis[40], and assumes both that the channel is "off" and approximates the pentacene dielectric as air.

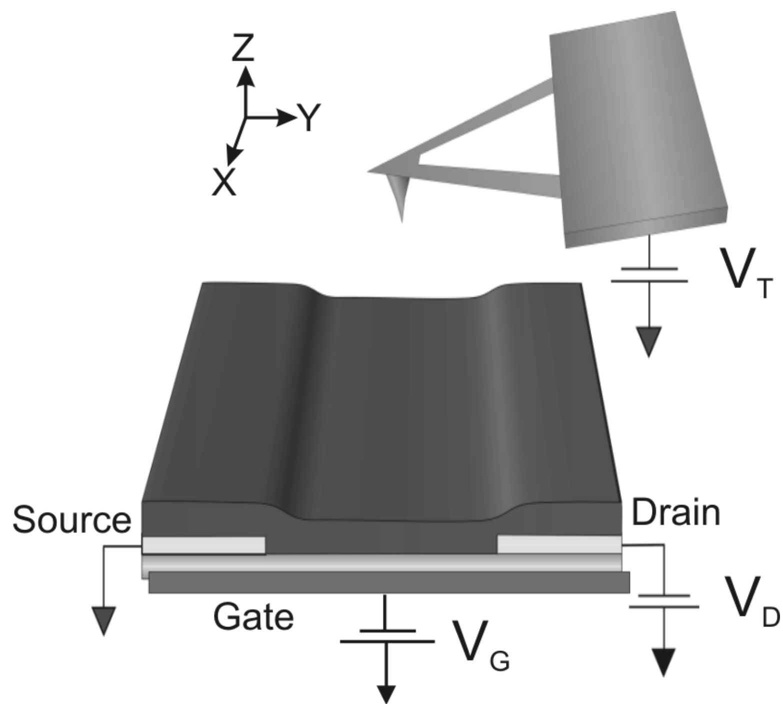

Figure 2.1: EFM Diagram

A charged cantilever over a transistor with drain, gate, and tip potentials, and source grounded.

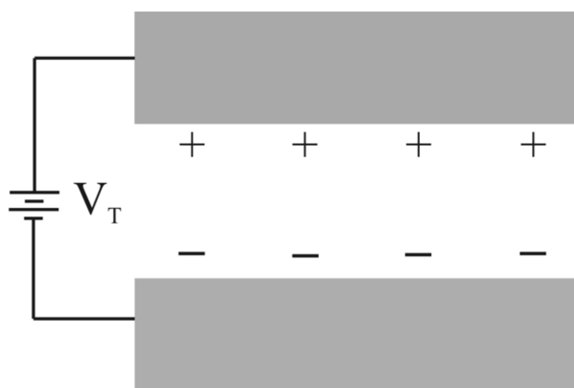

Figure 2.2: Parallel Plate Model

Charged EFM tip over surface modelled as a parallel plate.

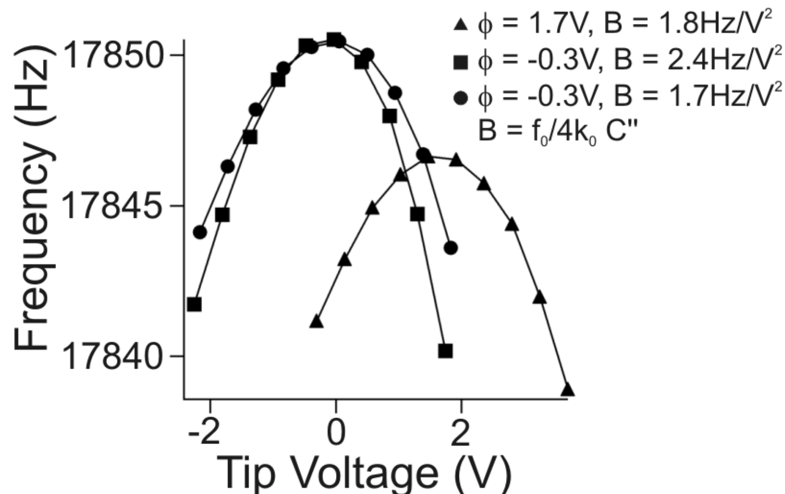

Figure 2.3: Tip Voltage Dependent Frequency

Collected frequency data demonstrates the effect of potential change (circles and triangles) and capacitance changes (circles and squares). This data is fit to Eq. 2.7. The cantilever tip (f_0 = 75 kHz, k_0 = 1 N/m) is about 100 nm over the top a sample of 25 nm pentacene film transistor. The squares frequency data was collected over the electrode (50 nm closer), while the circles frequency data was collected over a neutral region in the channel. The triangles frequency data was collected over trapped charges in the channel.

$$\Delta\phi = \frac{\Delta\sigma t}{\epsilon} \tag{2.8}$$

The interested reader is referred to Eric Muller's thesis[40] and the Silveira book chapter[174] for a detailed derivation of Eq. 2.7 and Eq. 2.8. These equations will be used throughout the remainder of this thesis.

2.3 Measurement Techniques

There are two measurement modes used with an EFM: topography is collected by tapping mode AFM, while local electrostatic potential and capacitance are collected by measuring frequency. In this section I describe how cantilever am-

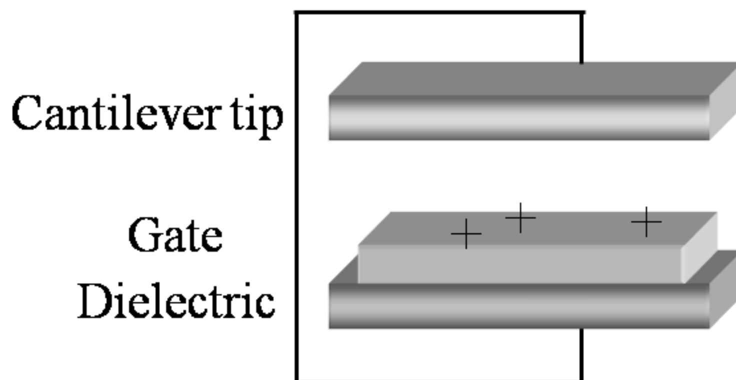

Figure 2.4: Trapped Charge as a Parallel Plate

A charged cantilever over trapped charge modelled as a parallel plate. The gate forms the bottom plate, with the dielectric (often silicon dioxide) between the trapped charge and the gate.

plitude and frequency are used to determine these local characteristics. Later I will discuss how the microscope uses both sample positioning and local topography, potential, and capacitance information to characterize samples. We used a commercial cantilever (MikroMasch NSC18/TiPt) with a spring constant, k_0, of $3.5 Nm^{-1}$, a resonance frequency, f_0, of 75 kHz, and a vacuum quality factor, Q, of 10^4 in high vacuum (10^{-5} torr). Cantilever displacement is monitored by a laser interferometer[175]. The light is generated by a laser diode (Laser Diode Incorporated, model # SCW 1301G-200FC with an FC-APC angle polished connector) operating at 1310 nm and sent down a single mode optical fiber (Corning 9/125 - the core is 9 μm in diameter and the cladding is 125 μm in diameter). An optical coupler is used which sends ten percent of the light down an optical fiber that is cleaved at ninety degrees and mounted approximately 50 μm above the cantilever.

Topography is recorded using the cantilever as used in AFM[161]. We found that tapping mode works better than contact mode with our cantilevers. The cantilever is excited by a resonance frequency sin wave of approximately 50 mV_{rms}, applied to piezoelectric element mounted beneath the cantilever. The general

scheme is shown in Fig. 2.5a. The cantilever is driven to a full interferometic fringe (328 $\mathrm{nm_{PP}}$). The cantilever amplitude is determined either by a Lockin Amplifier (Stanford Research SR-830) or a commercial frequency demodulator (Standford Research SR620 or RHK PLLPRO). The cantilever amplitude is input into a Stanford Research SIM960 proportional-integral-derivative (PID) feedback controller. The PID controls the height of the cantilever above the sample by applying a potential to a home-built slip-stick surface approach[40] referred to as the Z-piezo. The piezo element extends approximately 30 nm per volt, and applied potential is multiplied by 15 by a ThorLabs 3-Axis Piezo Controller Model MDT693. This results in approximately 450 nm/V as applied by the PID. The cantilever is extended until the amplitude drops to the setpoint of 82% (268 $\mathrm{nm_{PP}}$). The PID is programmed as follows: P=-0.1 OFF, I=500 $\mathrm{s^{-1}}$ ON, D=5×10^{-4} s ON, Internal Setpoint = 4.5 V. These settings were determined by trial and error. The output of the PID is also recorded by a conventional DAQ interface card (National Instruments DAQ board, model NI PCI-6259) controlled by Labview. 64 Hz measurement gives the general shape of the topography, but slower measurement is required to allow the cantilever to fully react to topographical steps. When a reliable topographical image is desired, the speed is reduced to 16 Hz.

In this thesis, there are 3 types of frequency measurement: Swept Voltage Frequency Measurement (Swept VFM), Fixed Voltage Frequency Measurement (Fixed VFM), and Modulated Voltage Frequency Measurement (Modulated VFM).

Swept VFM measures the cantilever frequency as a function of the applied tip potential. The cantilever is paused over the measurement location and sequential voltages over a typical range of 6 V are sent to the tip by a DAQ board, shown in Fig. 2.5b. The cantilever frequency is recorded for each voltage and fit to Eq. 2.7

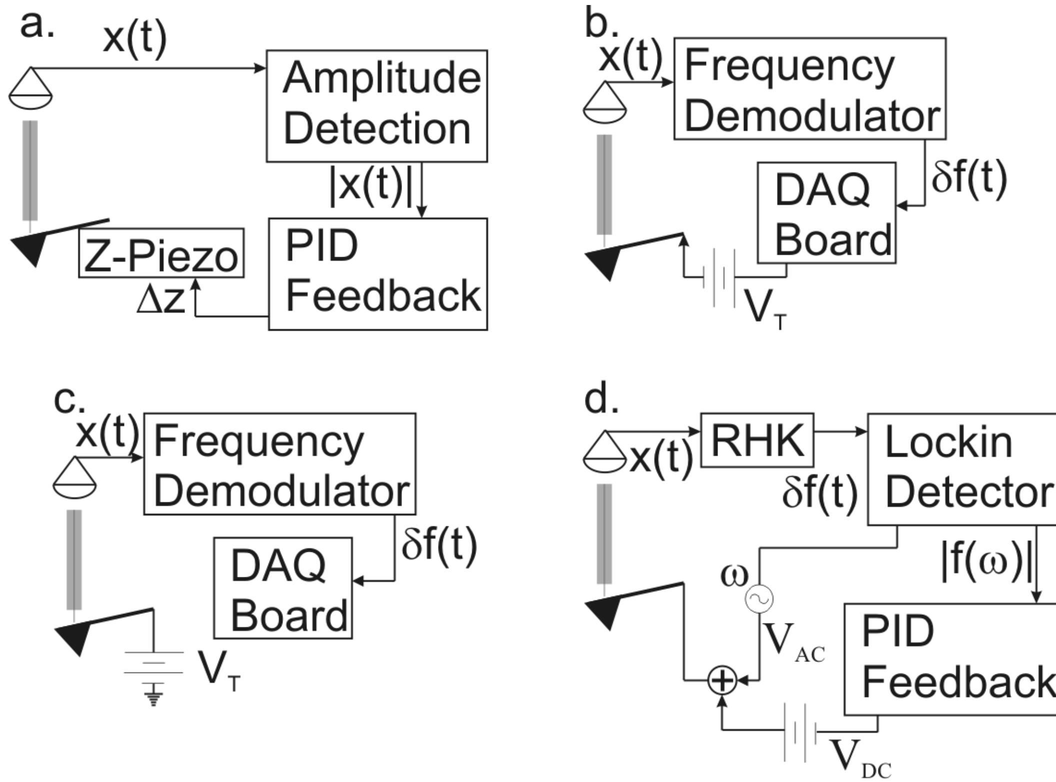

Figure 2.5: Equipment Configuration for Different Measurement Types

a. Equipment configuration for tapping mode AFM. The cantilever amplitude is maintained at a constant value by the PID controlled Z-piezo. b. Equipment configuration for Swept VFM. The DAQ board is programmed to both sweep the potential applied to the cantilever and record the hardware-demodulated frequency at each potential. c. Equipment configuration for Fixed VFM. A potential is applied to the cantilever (usually -2V) and the demodulated frequency is recorded by a DAQ board. d. Equipment configuration for Modulated VFM. A lockin amplifier creates an AC potential (of frequency ω) applied to the tip. The cantilever frequency component at ω is fed into a PID which modifies a DC tip potential to bring the ω frequency component to 0.

to obtain capacitance and potential at that point. Fig. 2.3 shows representative frequency data for a cantilever over a pentacene transistor. While this approach is easy to implement, it is slow; 5 seconds with the SR620 or 1 second with the RHK-PLLPRO are required to collect one parabola. Collecting a two-dimensional image of $\phi(x, y)$ takes far too long to be practical.

Instead of sweeping the applied tip potential, Fixed VFM measures the fre-

quency while applying a single tip potential. This measurement is outlined in Fig. 2.5c. A DC potential is applied to the tip (usually -2V), and the frequency is measured while the cantilever is rapidly moved across the sample. This can be viewed as fixing the tip potential in Fig. 2.3. Changes in both capacitive and electrostatic potential will shift the frequency, though electrostatic potential changes generally cause a much larger shift in frequency. Fixed VFM measurement provides an approximation of capacitive and potential change through a sample, but a topographical image of the same area is required to definitively distinguish between the two. Fixed VFM frequency measurement generally takes about 1 second per 7 $\mu(m)$ line of 128 measurement points.

Modulated VFM, shown in Fig. 2.5d, is a fast technique to measure both potential and capacitance. It shares properties with both Swept and Fixed VFM. The potential applied to the tip during Modulated VFM has two components: an AC wave at frequency ω generated by a Lockin Amplifier and a DC value generated by a PID controller, shown in Eq. 2.9.

$$V_T(t) = V_{T,DC} + V_{T,AC}\cos(\omega t) \tag{2.9}$$

The tip reacts to the applied potential parabolically in frequency according to Eq. 2.10.

$$f(V_T(t)) \simeq f_0 - \frac{f_0}{4k_0}\frac{\partial^2 C}{\partial z^2}(V_T(t) - \phi)^2 \tag{2.10}$$

Expanding the squared term in Eq. 2.10 gives Eq. 2.11.

$$\begin{aligned} (V_T(t) - \phi)^2 &= ((V_{T,DC} - \phi) + V_{T,AC}\cos(\omega t))^2 \\ &= (V_{T,DC} - \phi)^2 + 2(V_{T,DC} - \phi)V_{T,AC}\cos(\omega t) + V_{T,AC}^2\cos^2(\omega t) \end{aligned} \tag{2.11}$$

Eq. 2.11 can be simplified using $\cos^2(\omega t) = \frac{1}{2} + \frac{1}{2}\cos(2\omega \mathrm{t})$. We can see that application of AC tip voltage generates both frequency-ω and frequency-2ω cantilever frequency. We can separate out these components of the resulting cantilever

frequency:

$$\hat{f}(\omega) = \frac{f_0 V_{T,AC}}{2k_0} \frac{\partial^2 C}{\partial z^2}(V_{T,DC} - \phi) \tag{2.12}$$

$$\hat{f}(2\omega) = \frac{f_0 V_{T,AC}^2}{8k_0} \frac{\partial^2 C}{\partial z^2} \tag{2.13}$$

$\hat{f}(\omega)$ and $\hat{f}(2\omega)$ are essentially the frequency fourier components created by the tip potential. When the cantilever frequency is demodulated and fed into the Lockin Amplifier, the amplitude of $\hat{f}(\omega)$ can measured and sent to the PID. When the static tip potential output by the PID matches the local potential ($V_{T,DC} = \phi$), the amplitude of $\hat{f}(\omega)$ goes to zero. Thus the PID output is the local potential and recorded by the DAQ board. If a second Lockin Amplifier is used, the amplitude of $\hat{f}(2\omega)$ can be extracted and used to determine the capacitance second derivative ($\frac{\partial^2 C}{\partial z^2}$) since $V_{T,AC}$, f_0, and k_0 are known. The PID is programmed as follows: P = +1.5 ON, I = 100 s^{-1} ON, D = OFF, Internal Setpoint = 13 mV - to cancel out the DC Offset of our Lock-in Amplifier. Modulated VFM can be measured at up to 32 Hz speed, more than ten times faster than the fastest Swept VFM measurement. The data collected is slightly more noisy, but this can be adjusted by controlling the measurement speed. Because the sample might not be able to respond to rapid changes in voltage, the Modulated VFM measurement may not yield identical results to Swept VFM. Both methods do give potential and capacitance that agree in our samples so far - but this had to be tested experimentally.

2.4 Faster Frequency Determination

During the work of this thesis we realized that we would need faster measurement of capacitance and electrostatic potential. The microscope constructed by Eric Muller used a Stanford Research SR620 Frequency Counter to demodulate the frequency.

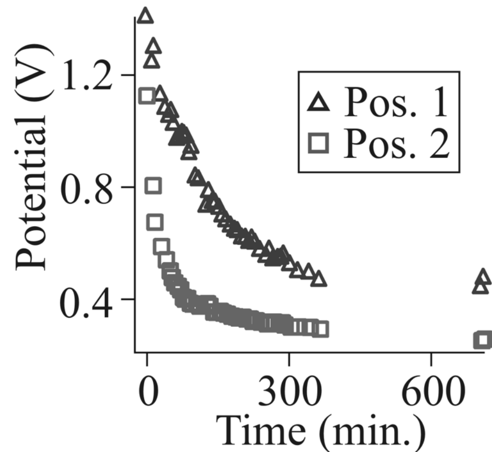

Figure 2.6: Trap Release in Pentacene

Trap release in 25 nm thick polycrystalline pentacene film on SiO_2. The transistor was charged for 60 seconds at $V_G = -50$ V. The cantilever is roughly 100 nm above the surface. While some charge remains trapped for hours, much of the charged is released in the first few minutes.

This machine offered both a 1 Hz GPIB interface and a 50 Hz, 8-bit analog output. The first trap measurement experiment performed with this equipment required 5 min. between each sequential measurement of potential. Our early work using EFM to quantify local charge trap release rates in polycrystalline pentacene shown in Fig. 2.6. Perhaps as much as 20% of the charge was being released before we had completed the first measurement of potential. To increase the measurement speed we considered two instruments: the RHK PLLPRO and the Nanosurf EasyPLL, whose key attributes are summarized in Fig. 2.7. Both the RHK and the Nanosurf offered significantly faster demodulation. While the Nanosurf was the industrial standard for reliability and ease of use, the RHK offered a very attractive new technology. It employed a Field Programmable Gate Array, a technology that could literally be “reprogrammed” to the user’s specific needs as they evolved. The possibility we may need a new feature in some future experiment compelled us to test the RHK PLLPRO first.

Figure 2.7: Commercial Instruments

The three commercial instruments used to demodulate frequency and their relative capabilities.

The RHK PLLPRO claimed a bandwidth (B) of 900 Hz, implying a response time of 1/B or 1.1 ms. There are three frequencies to consider when evaluating bandwidth. The cantilever frequency (f) will deviate from a center frequency by an excursion frequency at a modulation frequency. A simple example of these frequencies is shown in Fig. 2.8. Here the tip is oscillating at a center frequency of 10 Hz; the frequency changes by 5 Hz (going from 5 Hz to 15 Hz) at a rate of 0.4 Hz (twice in 10 s). To generate a general time dependent frequency $f(t) = a + b \times \sin(2\pi\omega t)$ centered at a with an excursion of b at modulated rate ω, the equation for position ($x(t)$) is not $\sin(f(t) \times t)$ but instead:

$$x(t) = \sin(2\pi a t + \frac{2\pi b}{\omega}\cos(2\pi\omega t) + \Phi) \tag{2.14}$$

Φ here is simply a phase shift. An ideal machine with bandwidth of B would perfectly demodulate any frequency component with a modulation frequency less than B. Commercially, however, frequency components with modulation frequency approaching B are often attenuated by a filter. As B is increased the attenuation decreases, demonstrated in Fig. 2.9. In this figure, the excursion frequency is 100 Hz and modulation frequency is 1000 Hz. Increasing the bandwidth enables

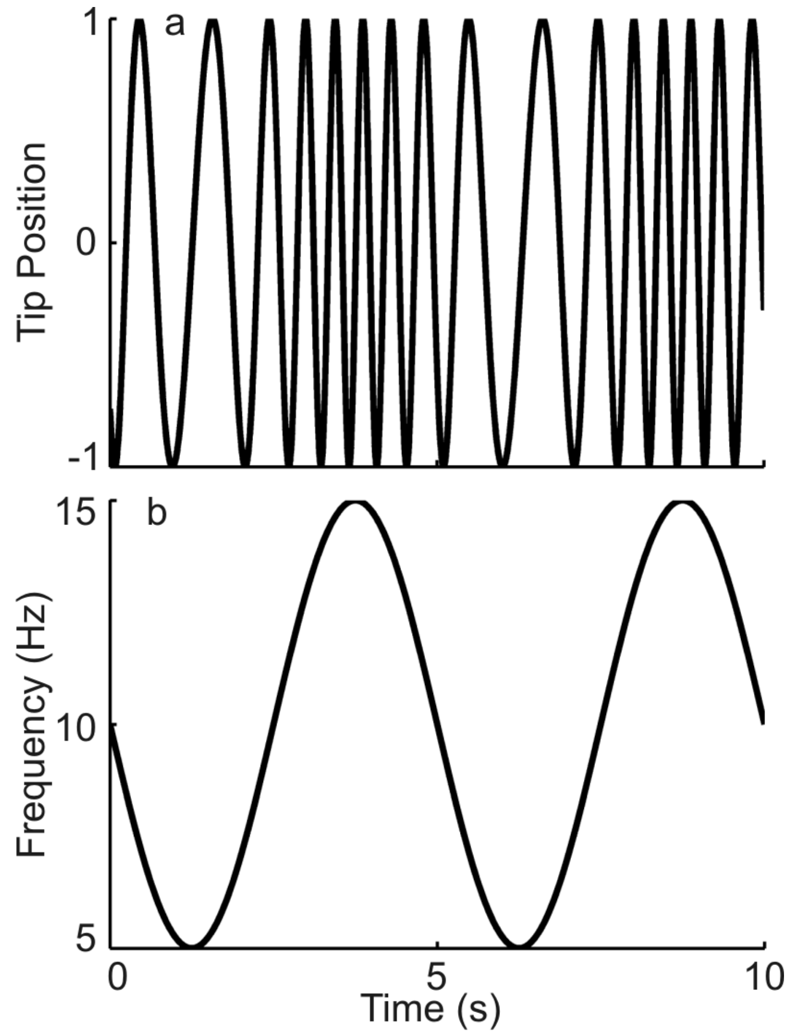

Figure 2.8: Time Variant Frequency Example

a. Example cantilever position and b. frequency as a function of time during modulation. The center frequency is 10 Hz, and it deviates from this by 5 Hz at a modulation frequency of 0.4 Hz.

accurate demodulation, at the expense of increased noise.

The RHK as received did not give the expected output, even when the bandwidth was much greater than modulation frequency. In order to understand what was happening, we developed two protocols to directly test the bandwidth of commercial frequency demodulators. These demodulation characterization protocols are drawn in Fig. 2.10. In the first scheme, we compare the commercial demodula-

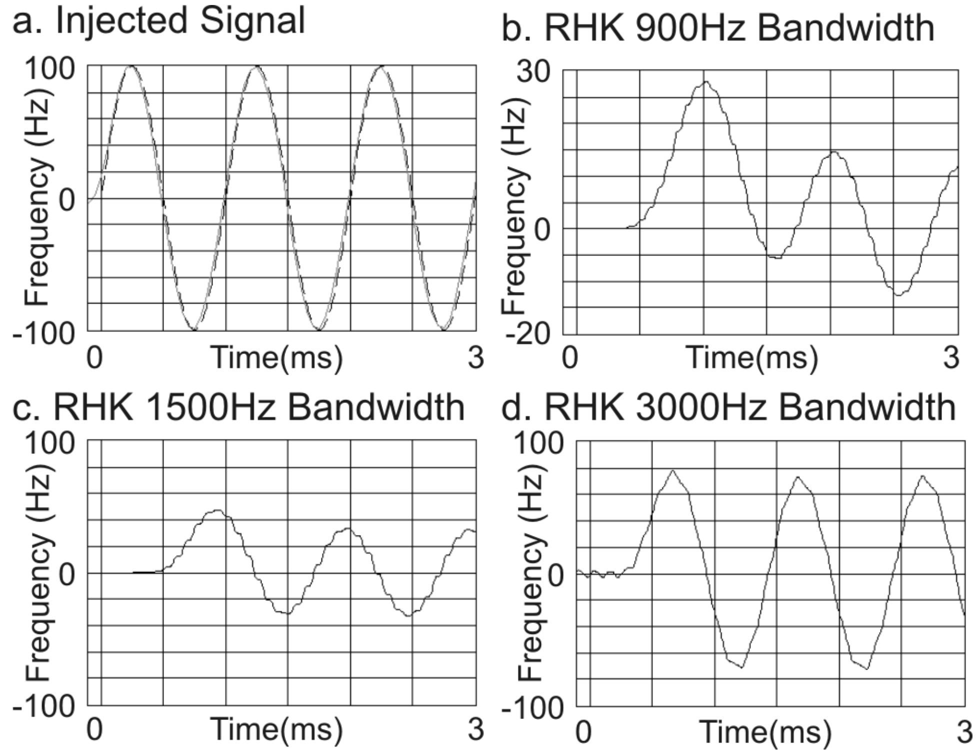

Figure 2.9: Filter Effects of Frequency Demodulator

a. The time-dependent frequency (solid) is injected into the RHK at different bandwidth settings The signal is artifially demodulated via software (dashed) to verify performance. As bandwidth is increased from b. 900Hz to c. 1500Hz to d.3000Hz, the amplitude of the excursion frequency is attenuated less, but the frequency noise increases.

tor to a software-based demodulator operation on a copy of $x(t)$ generated by the DAQ board according to Eq. 2.14. The frequency demodulator should reduce $x(t)$ to the previous $f(t)$, allowing the demodulated frequency to be directly compared with a that calculated by a software based demodulator. The second testing protocol uses a commercial arbitrary-waveform generator. The instantaneous frequency of the sine wave generated by this instrument can be modified via an input. A Lockin Amplifier generates $b \times \sin(\omega t)$, applied to the waveform generator's input. This creates an waveform with frequency $f(t)$, sent into the commercial demodulator. While measuring the output of this demodulator, the Lockin sweeps ω

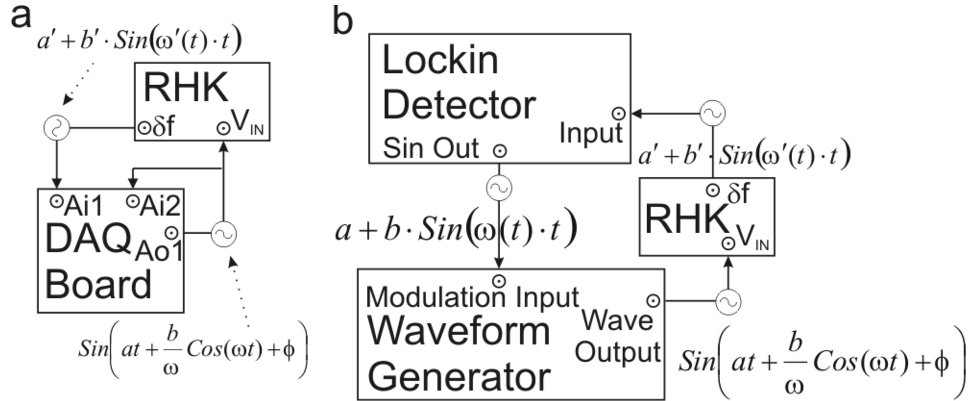

Figure 2.10: Bandwidth Test Schemes

Two techniques to test the attenuation at different bandwidth of commercial frequency demodulators. Direct data creation by a. DAQ board and b. Lockin-produced variation of a frequency generator should both demodulate to same wave components.

through the desired range and calculates the excursion frequency (b) at each modulation frequency (ω). The calculated amplitude can then be directly compared to the generating amplitude in the Lockin at each value of ω and the attenuation determined.

The results of these tests confirmed that the RHK had a bandwidth significantly less than the claimed 900 Hz, see Fig. 2.9. When these results were communicated to RHK, they worked with us to reprogram the demodulator - demonstrating the power of a field programmable gate array. The ratio of measured excursion frequency to applied excursion frequency (Δb) of each bandwidth setting on each device is tested both by DAQ protocol (dots) and Lockin protocol (lines), shown in Fig. 2.11 For example, the yellow data indicates the RHK PLLPRO at a bandwidth setting of 900 Hz. At low modulation frequencies the excursion frequency matches the applied, but starts to decrease about 200 Hz. By 450 Hz, the measured excursion frequency is one half the applied. Δb continues to decay exponentially as modulation frequency increases. By contrast, the green data indicates the Nanosurf

EasyPLL at a bandwidth setting of 400 Hz. While the Δb at low modulation frequency is 1, here some amplification is seen. The measured excursion frequency is actually larger than the applied excursion frequency at a modulation frequency of 200 Hz, though the attention reaches one half by 500 Hz. The filter design in the Nanosurf is different from that in the RHK, causing both amplification at lower modulation frequencies and a quicker attenuation at higher modulation frequencies compared to the RHK. In general the Nanosurf bandwidth settings are more accurate as labeled, but RHK will give similar performance if a higher bandwidth setting is used. It was our conclusion that the bandwidth was acceptable for both devices. The last factor to consider was the noise generated by the demodulation process. The noise generated by the two instruments is very similar, a sample is shown in Fig. 2.12. This noise was collected by taking the power spectrum of the frequency collected from each demodulator while exciting a cantilever to roughly 200 nm in vacuum far from any surface. The noise for both instruments should be thermally limited at low modulation frequencies and by instrument attenuation of detector noise at higher modulation frequencies. The noise in the RHK output was reduced when the input was converted from 50 Ohm impedance to high impedance by removing a resistor. Previously a noisy operational amplifier was used to boost the current of the photodiode signal as the photodiode could not provide enough current to drive a 50 Ohm impedance. Ultimately the RHK PLLPRO was chosen for the lab because of the demonstrated power of the gate array and is now used to make much faster measurements.

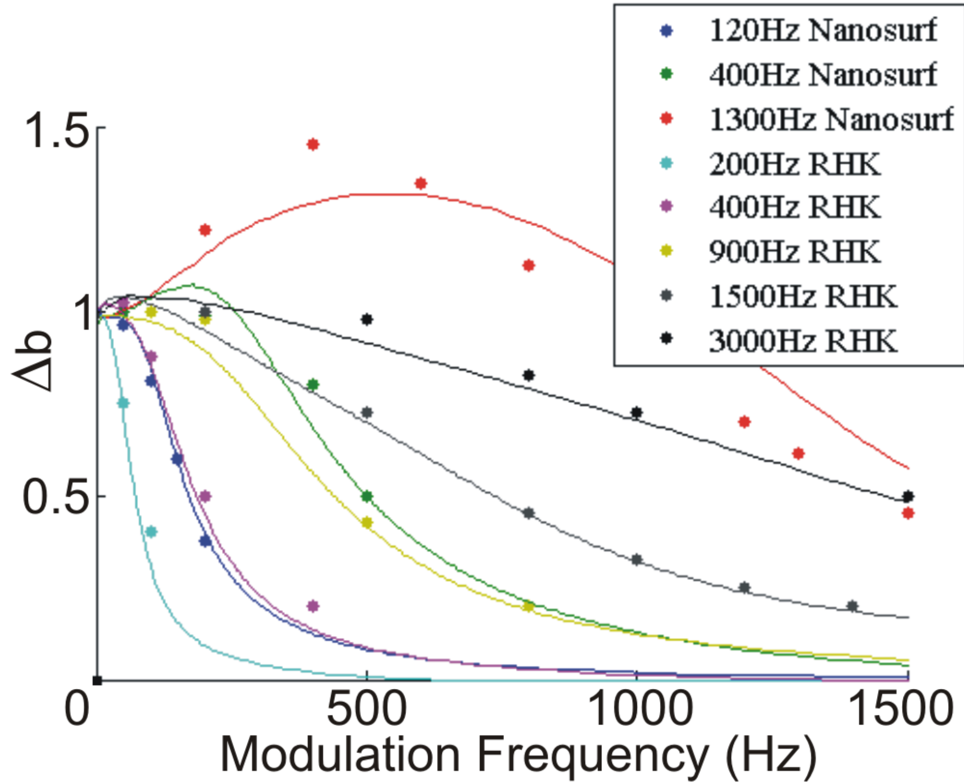

Figure 2.11: Bandwidth Test Results

DAQ (dots) and Lockin (lines) bandwidth test results for both the RHK PLLPRO and Nanosurf EasyPLL at multiple bandwidth settings. The Nanosurf bandwidth settings are more accurate than the RHK as labelled. The Nanosurf has both a sharper filter than RHK and regions of signal amplification. The DAQ data was collected by with a center frequency of 12 kHz, and excursion frequency of 400 Hz. The Lockin data was collected using a center frequency of 20145 Hz, an excursion frequency of 100 Hz and the modulation frequency was stepped by 5 Hz. The sensitivity was 146.5 Hz/V for both devices for all tests.

2.5 Scan Types

Scanning is accomplished by the use of a custom built piezoelectric stage. The construction of the stage is outlined in Eric Muller's thesis[40], with additional notes in Appendix B. The piezos are powered by bipolar amplifiers: Piezo Systems Inc. Piezo Amplifier Model EPA-104. There are three types of scanning motion performed in this thesis: images, linescans, and pointscans. When a new sample

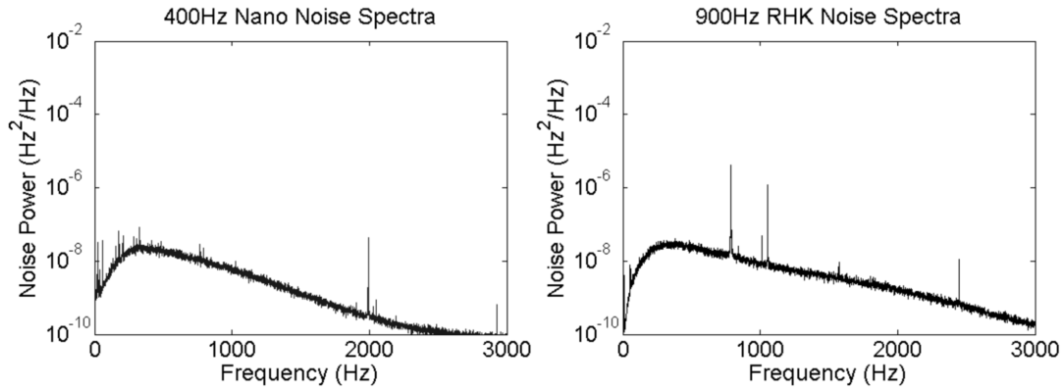

Figure 2.12: Frequency Demodulator Noise

Noise spectrum for RHK PLLPRO at 900Hz Bandwidth setting and Nanosurf EasyPLL at 400Hz Bandwidth setting. The noise of both instruments is very similar. The noise was collected using a lockin generated 80 kHz clean sine wave and a sensitivity of 1.831 Hz/V for both machines for all tests. The noise was averaged 60 times, collected at 100 kHz sampling.

is loaded it is very helpful create an image of a large area, varying both x and y. This is commonly done to obtain topographical information (at 64 Hz or 16 Hz depending on quality desired), Fixed VFM (at 128 Hz), or Modulated VFM (at a maximum of 32 Hz). Example images of these measurements from different samples are shown in Fig. 2.13. Swept VFM simply take too long to measure in a two dimensional grid. A typical image is 128 pixels by 128 pixels. During this thesis, we increased the effective speed of topographical image formation by a factor of 4 while allowing larger height variations to be mapped. This was the result of both increased amplitude measurement speed by the RHK and improved PID parameters. Using the RHK increased the range of the frequency shift detection beyond what actually occur with current equipment configuration, and the ability to image potential at reasonable times was introduced.

Linescans are the second scan type. Instead of creating a two dimensional grid as in an image, a single line is chosen either in x or y direction. Most commonly a

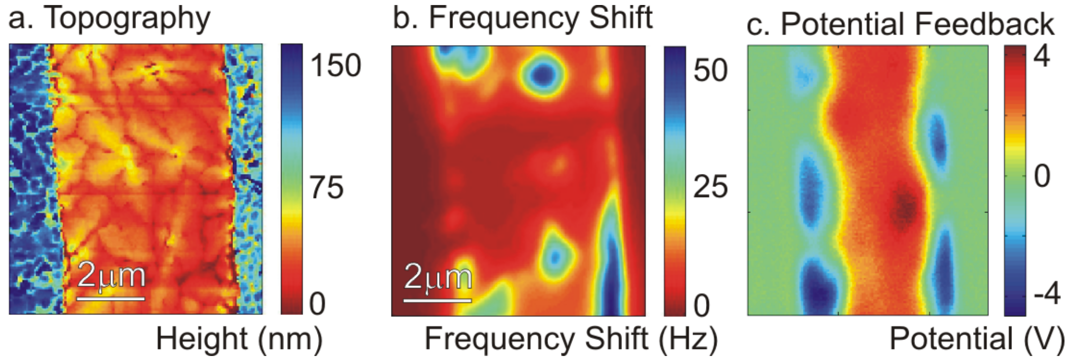

Figure 2.13: Examples of Images

a. Topographical images of a 25 nm thin film pentacene transistor are made by tapping mode AFM. Left and right are gold electrodes. b. Frequency shift images of a thin film pentacene transistor are made with a constant tip potential $V_T = -2$ V while the tip is about 100 nm above the surface. The large frequency shift here indicates trapped holes. The sample was charged at $V_G = -50$ V for 1 min. c. Potential feedback images of a pentacene monolayer transistor are made with PID feedback of tip potential to measure true local potential. Here both holes and electrons are trapped. The tip is about 100 nm above the surface. This pattern was created by charging at $V_G = +50$ V with light exposure for a long time to fill the entire channel with electrons, then charging at $V_G = -50$ V for about 30 seconds to introduce holes at the edges.

line is chosen to cross the active channel of the sample. Typically a line is broken into 64 samples. Generally either Swept or Modulated VFM data are collected in a linescan. A 64 point Swept VFM linescan takes about 1.5 min. A 64 point Modulated VFM linescan takes about two seconds to collect and one second for Labview to process, taking about three seconds total to complete. Examples of Swept and Modulated VFM linescans are shown in Fig. 2.14. It is important that the data collected by both agrees, suggesting that the charge has time to equilibrate in both sample and cantilever during each cycle of potential in Modulated VFM. The Swept VFM linescan has lower noise and is more easily adapted to handle large changes potential across the scan. During this thesis the available speed of linescans was increased by a factor of 100, from 300 s to 3 s. This enabled the measurement of fast ion motion in light-emitting electrochemical cells for the first

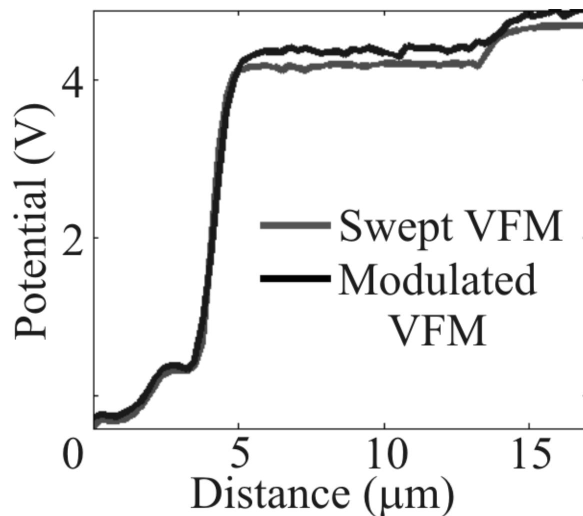

Figure 2.14: Examples of Linescans

Examples of the two linescans taken over a light-emitting electrochemical cell with $V_D = +5$ V. The tip is about 150 nm above the surface. Swept VFM results in lower noise and takes about 90 seconds; Modulated VFM requires only 3 seconds but has slightly more noise. The techniques give similar results.

time.

Pointscans are the last type of scan. A single point on the sample is chosen and the cantilever position is maintained over that point during the scan. This helps to minimize piezo drift. Again, either parabolic or feedback potential may be used once the cantilever is positioned. Generally this type of scan is used to to study the kinetics of charge trap formation or release, shown in Fig. 2.15. At the start of this thesis data points were collected five minutes apart, while they now can be collected every 0.5 s - an increase in time resolution by a factor of 600.

These three scan types are used in the next chapters to study both pentacene charge trapping and ion migration in light-emitting electrochemical cells. While events between scans will change, the fundamental properties of the scan do not. The power of the electric force microscope is the ability to measure topography, potential, and capacitance locally. The coming chapters show how this can be used

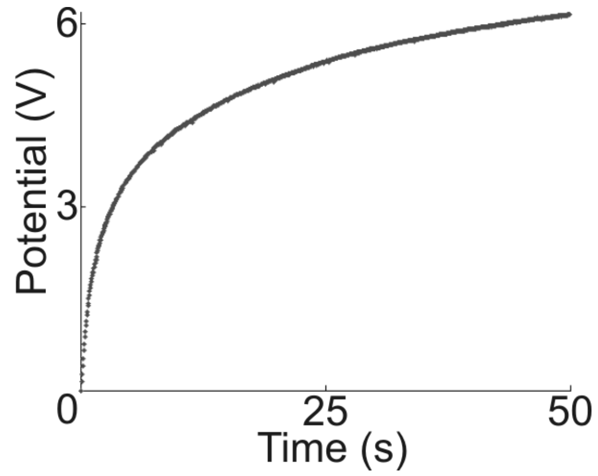

Figure 2.15: Example of a pointscan

Trap concentration in a polycrystalline film increasing as a function of time at one point. The tip is about 100 nm above the surface, $V_G = -50$ V for each 50 ms pulse to fill the traps.

to solve problems which other approaches cannot.

CHAPTER 3

KINETICS OF CHARGE TRAPPING IN POLYCRYSTALLINE PENTACENE

3.1 Introduction

In this chapter we discuss the early works done to temporally resolve the formation of charge traps in a polycrystalline pentacene film. This chapter is based on a paper published in Journal of Physical Chemistry B[109]. First we discuss the previous methods of studying charge trapping, then describe how we use EFM to study them directly.

Obtaining direct evidence in support of a charge trapping mechanism in pentacene has proven problematic. Transport measurements study traps only indirectly, through their effect on transistor subthreshold slope[50, 176, 81] and field-effect mobility[63, 64, 74, 87, 85], and interpreting these measurements requires assumptions about trap heterogeneity, charge conduction mechanisms, and contact resistance. The kinetics of trap formation and decay in pentacene have been studied by variable-temperature space-charged current measurements [87], but these measurements were bulk measurements carried out on a single crystal, so it is not clear whether the conclusions apply to polycrystalline pentacene employed in transistors. Although capacitance-voltage and deep-level-transient spectroscopy have identified a number of trap states near the pentacene/SiO_2 interface [177], the data analysis requires modeling traps as fixed energy levels, not as states whose creation requires the presence of mobile holes [35].

Electric force microscopy (EFM) is a powerful method for locally probing charge

trapping in semiconductor devices. In contrast with competing techniques, it does not require assumptions about either injection at the contact or transport through the bulk and gives quantitative measurements of local trap concentration as described in Chapters 1 and 2. Burgi *et al.*[115] were the first to introduce a technique to detect trapped charge in polymer-based transistors using EFM. They also show how light clears traps. Muller and Marohn[88] were the first to image the charge traps in polycrystalline pentacene using EFM.

The challenge of studying trapped charge via EFM is to differentiate between trapped charge and free charge. The reason for this and Muller and Marohn's approach to distinguishing trapped charge from free charge in a transistor is illustrated in Fig. 3.1. The energy levels of pentacene/SiO_2 interface with a trap state are drawn in Fig. 3.1a. When the gate turned on, free charge fills both the conductive channel and the trap sites in Fig. 3.1b. The total charge in the channel matches that in the gate. While some of this charge is trapped, trapped charge is difficult to detect in the presence of free charge (Fig. 3.1c). Since electron injection into pentacene from gold is very slow, our transistors readily conduct only holes. When a negative gate voltage is applied, the mobile holes fill the channel to create an effective parallel plate capacitor. The tip, outside of this capacitor, observes a ground plane (zero potential), shown in Fig. 3.1d. However, when the gate is turned off, the free charge leaves the channel. The trapped charge remains behind and is detectable as a change in the sample's surface potential, shown in Fig. 3.1e. This state is not in equilibrium, and the charge will eventually be released. Trapped charge can be detected in this way as long as the trap release time is at least a few cantilever cycles or, ideally, as long as a scan time. This is the case for polycrystalline pentacene at room temperature.

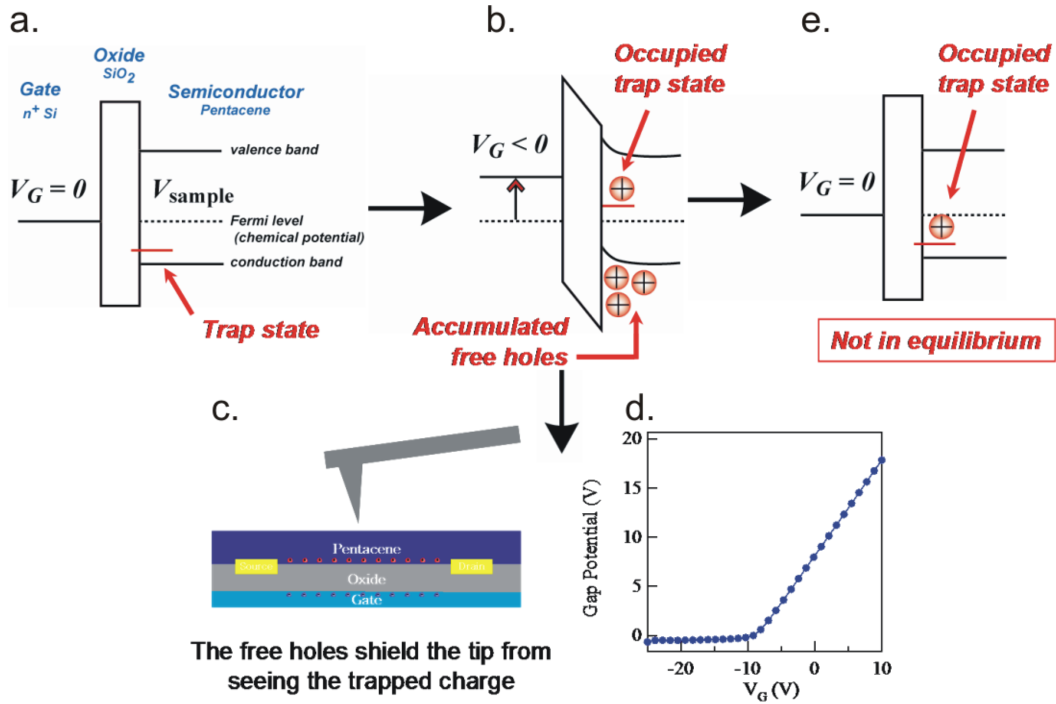

Figure 3.1: Charge Trap Detection Scheme

(a) Energy band diagram of the pentacene/SiO_2 interface. (b) When the gate is turned on, free holes fill the channel. (c) These free holes screen the tip. (d) Because only holes can be readily injected into pentacene from the gold electrodes used here, the tip observes a ground plane (zero potential) at negative gate voltages but sees the gate at positive gate voltages. (e) When the gate is turned off the trapped charge is left behind and can be imaged.

In order to gain information about the *kinetics* of charge trapping in pentacene, here we introduce *time-resolved* electric force microscopy to probe the evolution of charge traps as a function of initial hole concentration, position, and time. The dependence of *trap formation rate* on hole concentration and location provide important new clues about the mechanism of charge trapping in polycrystalline pentacene.

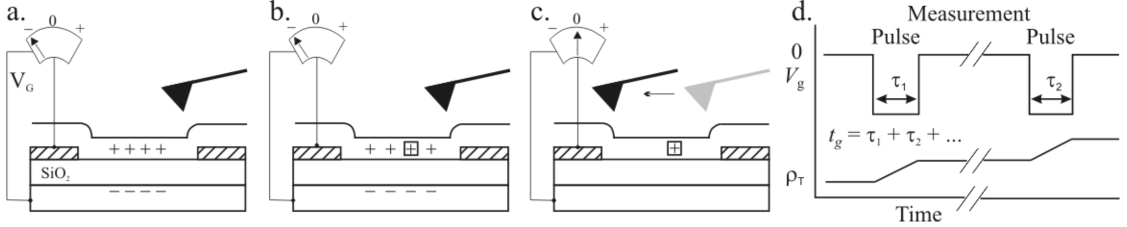

Figure 3.2: Scheme to Measure Charge Trap Formation Rate

(a) A voltage is applied to the transistor gate, causing mobile charge to accumulate at the pentacene/SiO_2 interface. (b) After a time τ_i, some of this mobile charge becomes trapped, as indicated by the box. (c) The gate voltage is returned to zero, inducing mobile charges to leave the pentacene/SiO_2 interface. Trapped charge remains behind, and is characterized by Swept VFM. (d) To measure the kinetics of charge trap growth, the voltage to the gate is pulsed; Swept VFM imaging of the trapped charge density ρ_T is carried out in between gate pulses. Local charge trap density is studied as a function of the time t_g that free holes were available at the pentacene/SiO_2 interface.

3.2 Methods

3.2.1 Device Fabrication

Bottom-contact pentacene transistors were fabricated as follows. The electrodes were interdigitated channels of width 5 μm and total length 30 mm. The source and drain electrodes were 50 nm of Au deposited over 5 nm of Cr. The dielectric, SiO_2, was thermally grown to a thickness, h_{SiO_2}, of 900 nm. Substrate preparation is further detailed in Appendix A. Prior to pentacene deposition, the transistor substrate was cleaned with Microposit Remover 1165, acetone, and isopropyl alcohol to remove a protective layer of Microposit S1813 photo resist. The substrate was then treated with a 10 min. UV-ozone clean to remove any residual organic material and quickly transported to the vacuum deposition chamber. The sample was exposed to air for a maximum of 20 minutes between cleaning and evaporation.

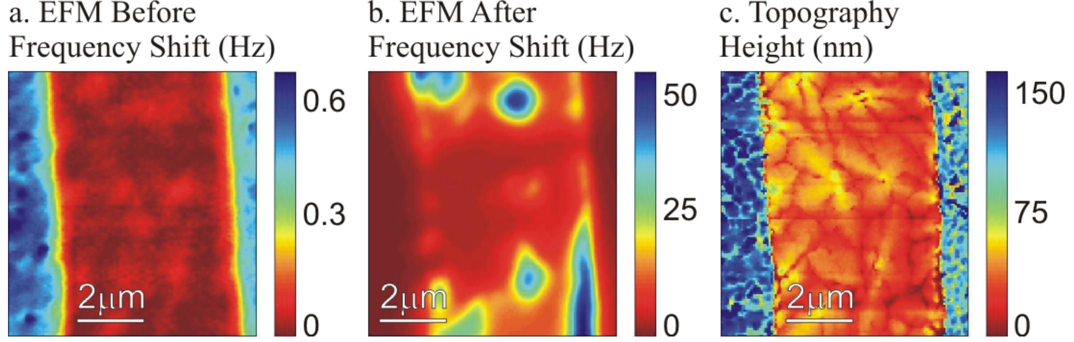

Figure 3.3: Topography and Charge Trapping in Pentacene

(a) Fixed VFM image of pristine sample. (b) Fixed VFM image acquired after the gate had been turned on for $t_g = 5$ min at $V_G = -50$ V. Trapped charge is highly localized. (c) Pentacene transistor topography, by AFM. The contacts appear as 50 nm-tall (blue) features on the left and right of the image.

A 25 nm thick layer of pentacene (Aldrich, used as received) was deposited onto the oxide via vacuum evaporation in the dark at a rate of approximately 0.1 Å/s while the substrate was held at a temperature of 60 °C. Following pentacene deposition, the sample was cooled for 2 to 3 hours in air and transferred into vacuum within 12 hours. The resulting polycrystalline pentacene film transistors exhibited a saturation mobility of 1.3×10^{-2}cm^2/Vs and a threshold voltage of $V_T = -6$ V.

3.2.2 Atomic force microscopy

All microscopy was carried out in high vacuum and in the dark using a custom-fabricated vacuum electric force microscope[88, 178]. We employed a commercial cantilever (MikroMasch NSC21/Ti-Pt) with a spring constant, k_0, of 1.0 N/m, a resonance frequency, f_0, of 25 kHz, and a vacuum quality factor, Q, of 1×10^4. Tapping mode atomic force microscopy was carried out using a drive amplitude of $x_{\text{drive}} = 180\,\text{nm}_{\text{pp}}$, a set point of $0.82\,x_{\text{drive}}$, and a linescan rate of 0.125 Hz.

3.2.3 Electric Force Microscopy

Fixed VFM was used to probe local electrostatic potential and capacitance. In these experiments, the cantilever was retracted to a height, z, of 200 nm above the pentacene surface. With no appreciable mobile charge in the transistor channel, the dependence of cantilever frequency f on tip-gate voltage V_{tg} may be approximated by [179]

$$f(V_{tg}) \approx f_0 - \frac{f_0}{2k_0} \frac{\partial^2 C_{tg}}{\partial z^2} \left(V_{tg} - \Delta\phi_{tg} - \Delta\phi_T(t_g)\right)^2 \tag{3.1}$$

where C_{tg} is the tip-gate capacitance and $\Delta\phi_{tg}$ is the contact potential difference between the tip and gate in the absence of trapped charge. Trapped charge at the pentacene dielectric interface shifts the local electrostatic potential by an amount [179]

$$\Delta\phi_T(t_g) \approx \sigma_T(t_g)\, h_{\mathrm{SiO_2}}/\epsilon \tag{3.2}$$

where σ_T is the planar trap density, $h_{\mathrm{SiO_2}}$ is the SiO_2 thickness, and $\epsilon = 4.64\,\epsilon_0$ is the dielectric constant of SiO_2. Equation 3.2 is derived by modeling the tip and gate as a parallel-plate capacitor and is valid when the dielectric is much thicker than the pentacene film, which is the case here. From a plot of $f(V_{tg})$ we extract both $\partial^2 C_{tg}/\partial z^2$ and $\Delta\phi_T$. From $\Delta\phi_T$ we extract an estimate of the local planar charge density, $\sigma_T(t_g)$, using Eq. 3.2.

3.2.4 Trap Kinetics

The procedure used to study the kinetics of trap formation in the pentacene transistor is sketched in Fig. 3.2. Holes are introduced into the transistor's pentacene film by applying a negative voltage V_g to the gate electrode (Fig. 3.2(a)). This results in a planar charge density of injected holes equal to $\sigma_h = C_g(V_g - V_T)$, where

C_g is the gate capacitance per unit area and V_T is the transistor's threshhold voltage. The gate was held at this voltage for a time step τ_i which ranged from 50 ms initially to 1000 ms subsequently, during which time some of the mobile charge is converted into trapped charge (Fig. 3.2(b)). The gate is then returned to zero in order to drive the mobile charge from the transistor channel. The gate voltage is applied by a Keithley 6430 sub-femptoamp remote sourcemeter. Initially τ was measured manually using a digital oscilliscope, but later program modifications allowed a hardware controlled pulse by the Keithley. This pulse has less than 1 ms variation, limited by the Keithley itself.

Trapped charge, which decays with a time constant of approximately $45-140$ min. (see Supplemental Information), may now be imaged. To detect the presence of trapped charge, Swept VFM, described in Chapter 2, is measured in a linescan between the source and drain electrodes (Fig. 3.2(c)). A single measurement of potential required about 4.5 seconds; the frequency was measured ten times as the tip potential was varied about 6 volts, centered on the predicted local potential. Each 64 point linescan typically takes 5 min and covers about 7 μm. The pulse-measure sequence of Fig. 3.4(a-c) is repeated up to $n_{\text{tot}} \sim 50$ times and the trap density is plotted as a function of the total time $t_g = \sum_i \tau_i$ that holes were allowed to react (Fig. 3.2(d)). After charge trap concentrations have reached steady-state, trapped charge is given 12 hours to decay to zero before trap kinetics are studied at the next gate voltage.

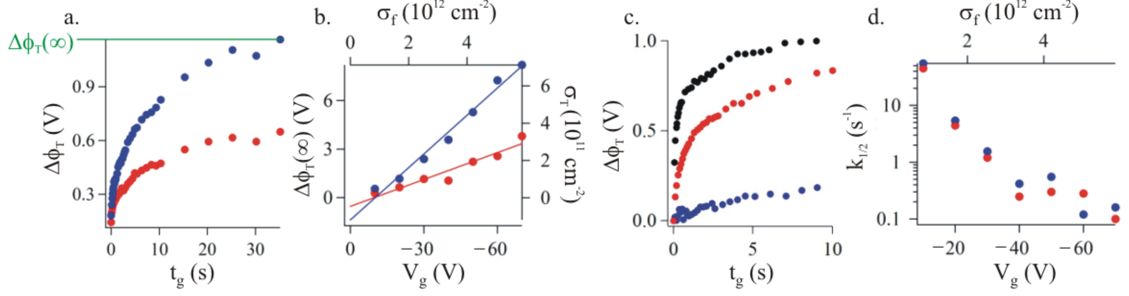

Figure 3.4: Equilibrium Results of Charge Trapping

(a) Potential versus gate time at two locations. The potential reaches reaches a steady-state value $\Delta\phi_T(\infty)$ which is different at each location. (b) Steady-state potential (trapped charge density σ_T) versus gate voltage (initial free charge density σ_f) at two locations. The density of trapped charge is linearly proportional to the density of initial free charge. (c) Normalized potential at one location for three different gate voltages: $-70\,\mathrm{V}$ (circle), $-30\,\mathrm{V}$ (square) and $-10\,\mathrm{V}$ (triangle). The rate of trap formation increases with gate voltage. (d) A log-log plot of trap formation rate versus initial free charge density.

3.3 Results

Before the transistor was operated, we verified that no trapped charge was present initially. An image was recorded by Fixed VFM at a tip voltage of $V_{tg} = -2$ V (Fig. 3.3(a)). Swept VFM linescans indicate that the observed frequency variations in Fig. 3.3(a) are due mainly to local variations in capacitance (e.g, height).

We then imaged the steady-state trapped charge distribution to locate trap sites. To generate trapped charge, a gate voltage $V_g = -50$ V was applied for a time $\tau = 5\,\mathrm{min}$ before being switched to zero. When trapped charge is present, the observed frequency variations are due predominantly to local variations in $\Delta\phi_T$. An image was collected again by Fixed VFM to give the of Fig. 3.3(b); this image is essentially a map of long-lived trapped charge. Approximately one third of sample points showed evidence of trapping. Comparing this image of trapped charge to the transistor topography shown in Fig. 3.3(c), we can see that trapped charge,

although it does not appear to be confined specifically to grain boundaries or small grains, is nevertheless highly localized.

We used time-resolved electric force microscopy to examine locally the rate of trap formation. In Fig. 3.4(a) we plot the potential $\Delta\phi_T$ versus time observed over two different points in the sample at $V_g = -40\,\mathrm{V}$. In Fig. 3.4(b) we plot the steady-state potential $\Delta\phi_T(\infty)$ as a function of gate voltage V_g. For pentacene stressed at $V_g = -60\,\mathrm{V}$, we can see that the steady-state density of trapped charge (calculated as $\sigma_T(\infty) = \Delta\phi_T(\infty)\epsilon/h_{\mathrm{SiO_2}}$) can be as large as $\sigma_T = 0.7 \times 10^{12}$ holes/cm^2. Comparing the trapped charge density to the initial free charge density at this gate voltage, $\sigma_f = 6 \times\ 10^{12}$ holes/cm^2, we can see that as many as ten percent of initially available free holes trap. (The free charge density was calculated as $\sigma_f = C_g(V_g - V_{Th})/q_e$, using a a threshold voltage of $V_{Th} = -6\,\mathrm{V}$.) Assuming that all of the trapped charge is confined to a single pentacene layer at the SiO_2 interface, at a $V_g = -60\,\mathrm{V}$ bias stress, the maximum observed concentration of trapped corresponds to approximately 1 trapped charge per 640 pentacene molecules.

In order to compare the rate of charge trap formation at different gate voltages, we plot the normalized potential versus time over one point in the sample at three different gate voltages (Fig. 3.4(c)). We can see immediately that the rate of trap formation depends strikingly on the initial concentration of free holes. To extract a model-free estimate of the trapping rate, we measure $t_{1/2}$, the time to reach half equilibrium, from plots like those in Fig. 3.4(c). The trapping rate $k_{1/2} = t_{1/2}^{-1}$ is plotted in Fig. 3.4(d) as a function of the initial free hole density for two points in the sample. The slope of the $\log(k_{1/2})$ vs $\log(\sigma_f)$ line in Fig. 3.4(d) is 3.0 ± 1.4; the reaction rate is *supra*linear in hole concentration.

3.4 Discussion

The main finding of this study is that traps in polycrystalline pentacene take at least seconds to reach steady-state. This observation suggests immediately that the trapping process in our pentacene sample should not be viewed as a gate-driven filling of midgap energy levels, as is widely assumed[87, 78, 177]. Instead, the dependence of trap formation rate on hole concentration seen here indicates that the rate-limiting step in trap formation involves an activated process, such as bipolaron formation or a defect-related chemical reaction. The data of Fig. 3.4(c-d) does not fit well to either first of second order kinetics, suggesting that trap formation involves a series of reactions not well approximated by a single reaction which is rate limiting. The linear dependence of trap concentration on gate voltage indicates that free holes are the limiting reagent, not the impurities.

The spatial distribution of trapped charge found here differs markedly from the charge trap distribution observed recently in electric force microscopy experiments by Muller and Marohn [88], who found that charge traps in their polycrystalline pentacene transistor were distributed in large patches within the transistor gap. Their sample had considerably smaller grains ($< 0.5\,\mu$m diameter) than does our sample ($0.5 - 2\,\mu$m diameter), but was otherwise identical. This observation raises the intriguing possibility that two distinct charge trapping mechanisms are at play in pentacene, depending on the grain size. At a minimum, it suggests that comparing bulk measurements of trap density from different samples should be done with great care, unless electric force microscopy images are also available to verify the trapping pattern. Our finding of highly localized charge trapping in polycrystalline pentacene suggests that analyzing the temperature dependence of bulk trapping kinetics[87] assuming a spatially homogeneous distribution of traps

will considerably *under*estimate the Arrhenius prefactor (attempt rate).

Although seemingly inconsistent with grain-boundary trapping, the localized trapping seen in the polycrystalline pentacene sample studied here can be rationalized using a competing trapping mechanisms. Given the finite time that our samples spend in air, chemical reactions of pentacene with ambient water [53, 80, 35] are one potential source of traps. The trap image of Fig. 3.4(a) indicates that these reactions, if occurring, are not occurring uniformly throughout the film or even at grain boundaries. Instead, the reactions would have to be occurring much faster at particular and relatively rare structural defect sites [180]. Another possibility is that holes are reacting with an impurity, such as hydrogenated pentacene[35], already present in the as-received pentacene; Fig. 3.4(a) suggests that reactions of holes with hydrogenated pentacene are ineffectually slow in the bulk. Again, we would need to invoke a structural-defect-assisted chemical reaction (or bipolaron formation) to explain our charge trap image.

3.5 Concluding Remarks

We have used time-resolved electric force microscopy to probe the local kinetics of charge trap formation in polycrystalline pentacene. The trapping rate depends strongly on the initial concentration of free holes. Trapped charge is highly localized. These findings suggest grain boundary trapping is not as important in polycrystalline pentacene as one would expect. Instead, our data support the notion that charges trap via an activated process, such as a chemical reaction, that is being assisted by a localized structural defect.

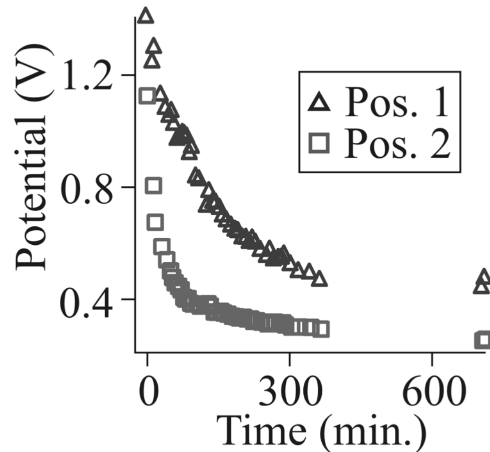

Figure 3.5: Trapped Charge Release in Pentacene

Swept VFM pointscan of the decay of trapped charge in polycrystalline pentacene, at two locations in the sample, following the return of the gate voltage to zero. The cantilever was roughly 200 nm over the sample. The trapped charge was created by applying -50 V gate bias for two minutes.

3.6 Supporting Information

3.6.1 Trap decay

In analyzing the time-resolved electric force microscope (EFM) trap-formation data presented in the manuscript, we assumed that the decay of trapped charge during the EFM measurements between gate pulses could be neglected. In order to justify this assumption, we measured the decay of trapped trapped charge, as follows. The initial potential was measured along a line, after which trapped charge was created by setting the gate to $-50\,\mathrm{V}$ for approximately $2\,\mathrm{min}$.. The gate was then returned to zero, and the potential along the line was measured sequentially until it returned to the initial value (Fig. 3.5). In between linescans, the tip was retracted a few hundred nanometers from the surface to minimize the possibility of the cantilever tip perturbing the trap decay. The observed decay of the potential, proportional to

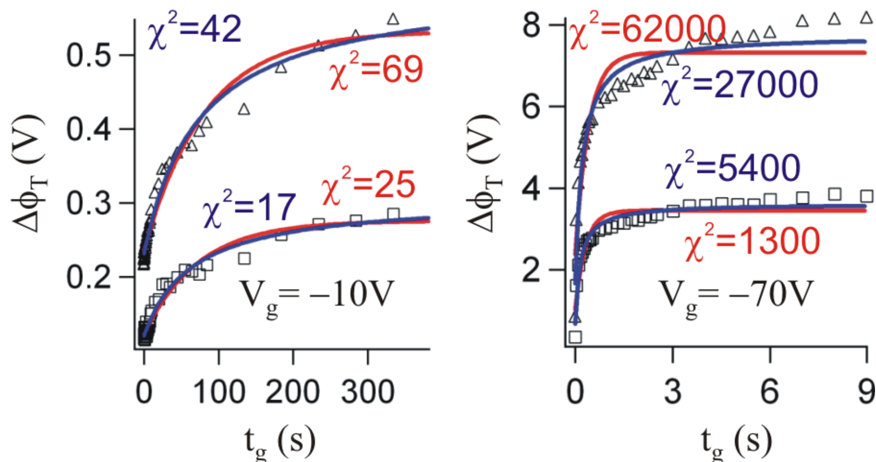

Figure 3.6: Attempted Kinetic Fit of Formation Rates

The local potential versus total gate time t_g at two locations (squares; triangles) in polycrystalline pentacene; here $V_g = -10, -70$ V. Neither first order (red) nor second order (blue) rate laws describe the growth of trapped charge very well. χ^2 values are provided for all fits and provide a measure of the fit accuracy. High χ^2 values indicate a poor fit, as discussed in the text. Pulse lengths were 50 ms, and the cantilever was roughly 200 nm over the surface.

the trapped charge density, had a $t_{1/2}$ ranging from 45 min to 140 min. This decay time is indeed significantly longer than the EFM measurement time of 5 minutes, suggesting that our assumption is valid.

3.6.2 Analysis of charge trapping kinetics

We know that injected holes are the limiting reagent in the trap formation reaction because final trap concentrations scale linearly with injected charge (Fig. 3.4(b) above). If another reagent limited trap formation, we would expect the final trap concentration to saturate as more charge was injected; this is not seen. Given this, it is reasonable to analyze the data of Fig. 3.4(d) so see whether the trap formation rate is first or second order in the initial free hole concentration.

If the trapping reaction is first order in the initial concentration of free holes (e.g., one free hole reacts to form one unit of trapped charge), we would expect:

$$\sigma_T(t) \;=\; \sigma_{TO} + \sigma_{TF}(1 - e^{-k_1 \cdot t}) \tag{3.3}$$

where σ_{TO} is the initial concentration of trapped charge (it may be non-zero if we have not waited long enough after stepping the gate voltage), σ_{TF} is the concentration of newly formed traps, and k_1 is the first order rate constant. If the trapping reaction is second order in the initial concentration of free holes (e.g., two free holes react to form one unit of trapped charge), we would expect:

$$\sigma_{2T}(t) \;=\; \sigma_{2TF} - \frac{1}{2k_2 t + \dfrac{1}{\sigma_{2TF} + \sigma_{2TO}}} \tag{3.4}$$

where $\sigma_{2T}(t)$ is the bipolaron trap concentration, σ_{2TO} is the initial concentration of trapped charge, σ_{2TF} is the concentration of newly formed traps, and k_2 is the second order rate constant. Fits of potential versus gate time data recorded at two locations is shown in Fig. 3.6. The χ^2 values are listed for all the fits in Fig. 3.6. The details of χ^2 are discussed in Chapter 5. For $V_G = -10$V data, a χ^2 value of less than 56 suggests a good fit (using a 95% threshold explained in Chapter 5). For the $V_G = -70$V data, a χ^2 value of less than 41 suggests a good fit. While most of the low voltage fits are valid, high voltage fits are definitely not.

Despite poor agreement, we fit all of the trap buildup data to both first and second order models. The resulting rate constants are shown in Fig. 3.7. If the kinetic model is correct, the rate constant should be independent of gate voltage (e.g., the initial concentration of free holes). This is not observed. The variation of first and second order rate constants with gate voltage suggests that either we are not using the correct kinetic model, or, alternatively, that the rates depend on electric field.

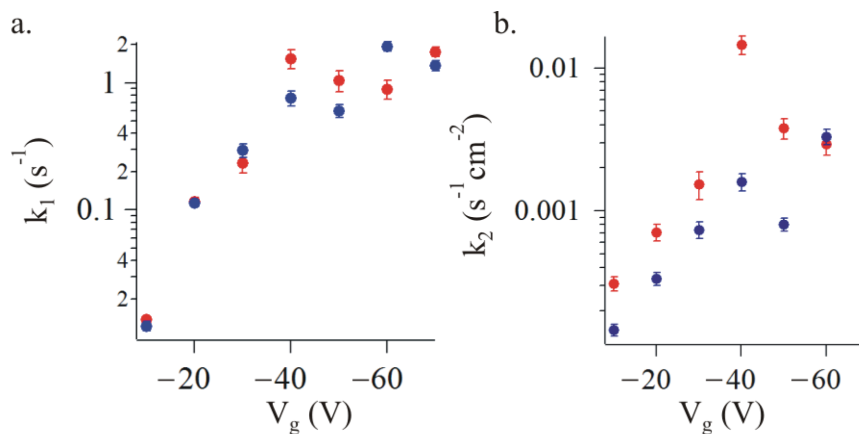

Figure 3.7: Charge Trapping Kinetic Fit Results

Trap formation rate constant fit values for two separate sample locations vs gate voltage. (a) First order. (b) Second order. Sample is a polycrystalline pentacene film. Gate pulses were 50 ms long. The cantilever was about 200 nm over the surface.

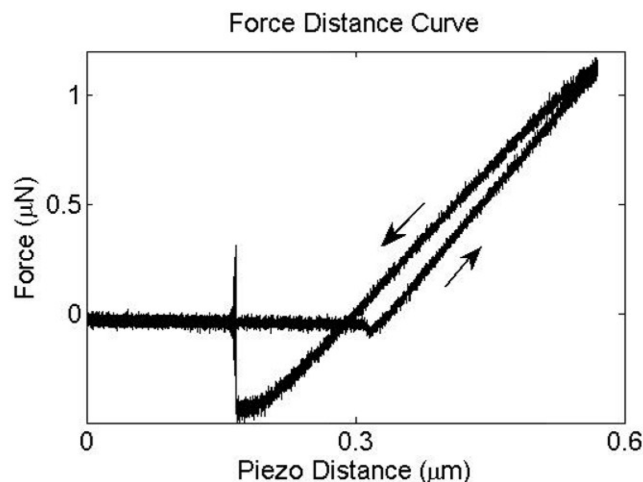

Figure 3.8: Cantilever Force Distance Curve

A cantilever force distance curve for the cantilever over a pentacene sample. The cantilever has a resonance frequency of 75 kHz and a spring constant of 1 N/m.

3.6.3 Force Distance Curve

Here we report the force distance curve for our sample, shown in Fig. 3.8. This curve was obtained by extending the cantilever towards the sample, then retract-

ing it in one continuous motion. The cantilever position was measured using a 1310 nm wavelength laser; thus one interferometric fringe corresponds to 655 nm displacement. A spring constant of 3.5 N/m was used to calculate the applied force from the observed displacement.

3.6.4 Author contributions

M.J. prepared all samples, carried out all measurements, and analyzed all data reported in this manuscript. E.M.M designed and built the electric force microscope and much of the associated software used for this study. J.A.M. initiated and supervised the project.

CHAPTER 4

STUDY OF CHARGE TRAPPING IN MODIFIED PENTACENE

4.1 Introduction

In this chapter we discuss our investigation of charge trapping in two functionalized polyacene molecules: 6,13-bis(tri-isopropylsilylethynyl)pentacene (TIPS pentacene, **1**) and triethylsilylethynyl anthradithiophene (TES ADT, **2**), shown in Fig. 4.1a and b, respectively. Three charge trapping mechanisms have been proposed to date for **1**. First, the crystal packing in **1** (shown in Fig. 4.2) is very different from that of pentacene (shown in Fig. 4.3). Measurements of thermally stimulated current[106, 107] have led to the proposals that the silyl side groups on **1** can trap electrons and that rearrangement of the lattice might trap a electron-hole pair[106]. Here we investigate **2**, which packs similarly to that of **1** (see Fig. 4.4), in order to test this hypothesis. If lattice rearrangement is the primary source of charge traps in **1**, the spatial distribution and kinetics of charge trapping of **2** should be similar to that in **1**.

The second trap candidate is the shallow traps invoked to rationalize the charge-concentration dependent (e.g., gate-voltage dependent) mobility observed in variable-temperature conductivity measurements of TIPS pentacene trasistors by Park *et. all.*[110, 111]. Park *et. all.* report a mobility activation energy of 60-80 meV (only a few times thermal energy of $k_B T = 25$ mV at room temperature) suggesting that the traps affecting the mobility have a small energy and therefore should release very quickly. Our trap measurement technique cannot detect short-lived traps, suggesting that we are unlikely to see the traps proposed by Park *et. all.*.

Finally, chemical degradation of **1** has been observed both with exposure to oxygen[104] and light[105]. While the Chabinyc-Northrup mechanism of trapping proposed for pentacene[35] is not likely to be active in **1** because of the bulky side groups and different crystal packing, hydrogenated TIPS pentacene impurities might also trap charge. Although Maliakal *et. all.*[104] observe improved solution stability of **1** vs. pentacene, they rationalized the higher rate of photodegradation of films of **1** comparatively as due to the higher diffusivity of oxygen in films of **1**. This suggests that, if the charge trapping results from a chemical impurity, the film morphology and structure will have a significant effect on the charge trapping observed.

Here we explore the spatial distribution of charge trapping in TIPS pentacene and TES ADT films using vacuum electric force microscopy (EFM). We imaged long-lived charge traps in transistors following a period of bias stress. Organic thin-film transistors were fabricated using a variety of methods to deposit TIPS pentacene from solution onto the transistor substrate. The structure of the films of these materials depends strongly on how the film is deposited. In a variety of transistors, the spatial distribution of long-lived traps as well as the kinetics of trap formation and decay were studied.

4.2 Methods

4.2.1 EFM Details

Imaging the Trap Distribution All image data was collected as described in Chapter 2. Topography was collected at 16 Hz with a grounded tip. Fixed VFM

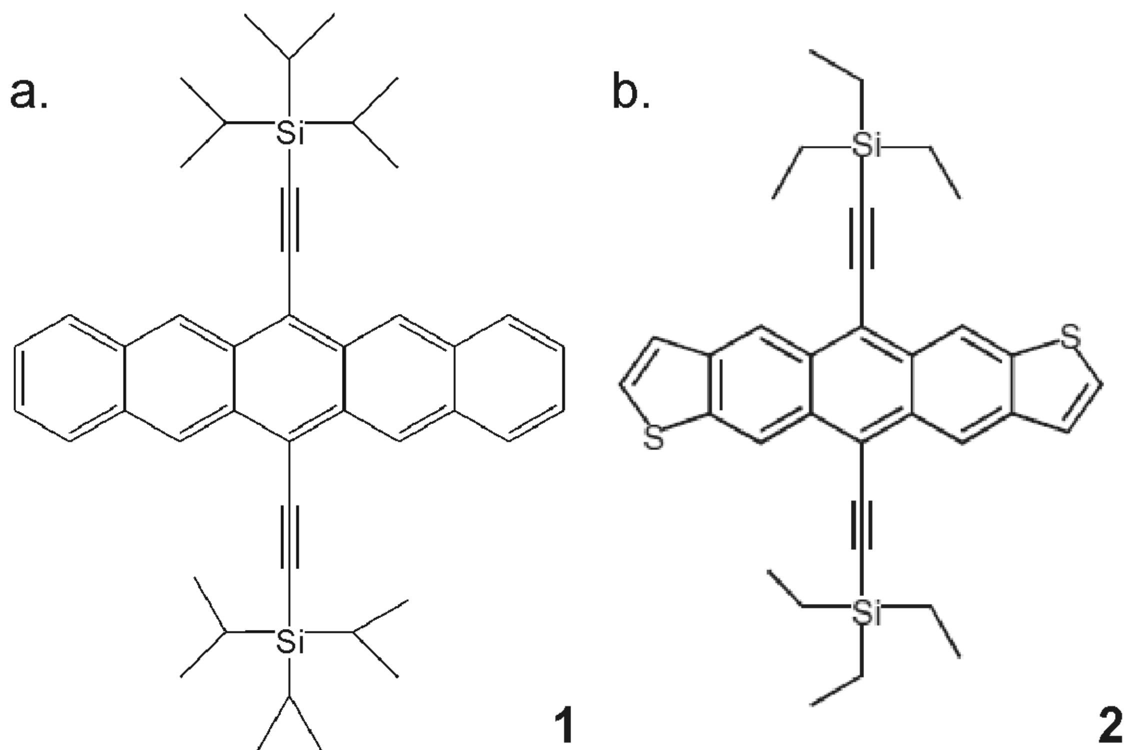

Figure 4.1: Modified Pentacene Structures

Structure of (a) TIPS-pentacene (b) and TES ADT (figure from Ref. [99]). Both materials were provided by Dr. John Anthony of University of Kentucky.

images were collected at 128 Hz with $V_T = -2$ V, after the indicated gate bias was applied for $t_g = 60$ seconds. The cantilever had a frequency of 75 kHz, a quality factor of 5×10^3, and a spring constant of 1 N/m. During Fixed VFM imaging and charge trap formation measurements the tip was held about 100 nm over the surface, unless otherwise indicated.

Charge trap formation rate was measured as indicated in Chapter 3, only more quickly. While Chapter 3 used the Stanford Research SR620 to demodulate frequency, here we use the RHK PLLPRO. This enabled much quicker measurement of trap formation: each successive potential measurement in Chapter 3 required five minutes to collect, but required only about two seconds in the measurements

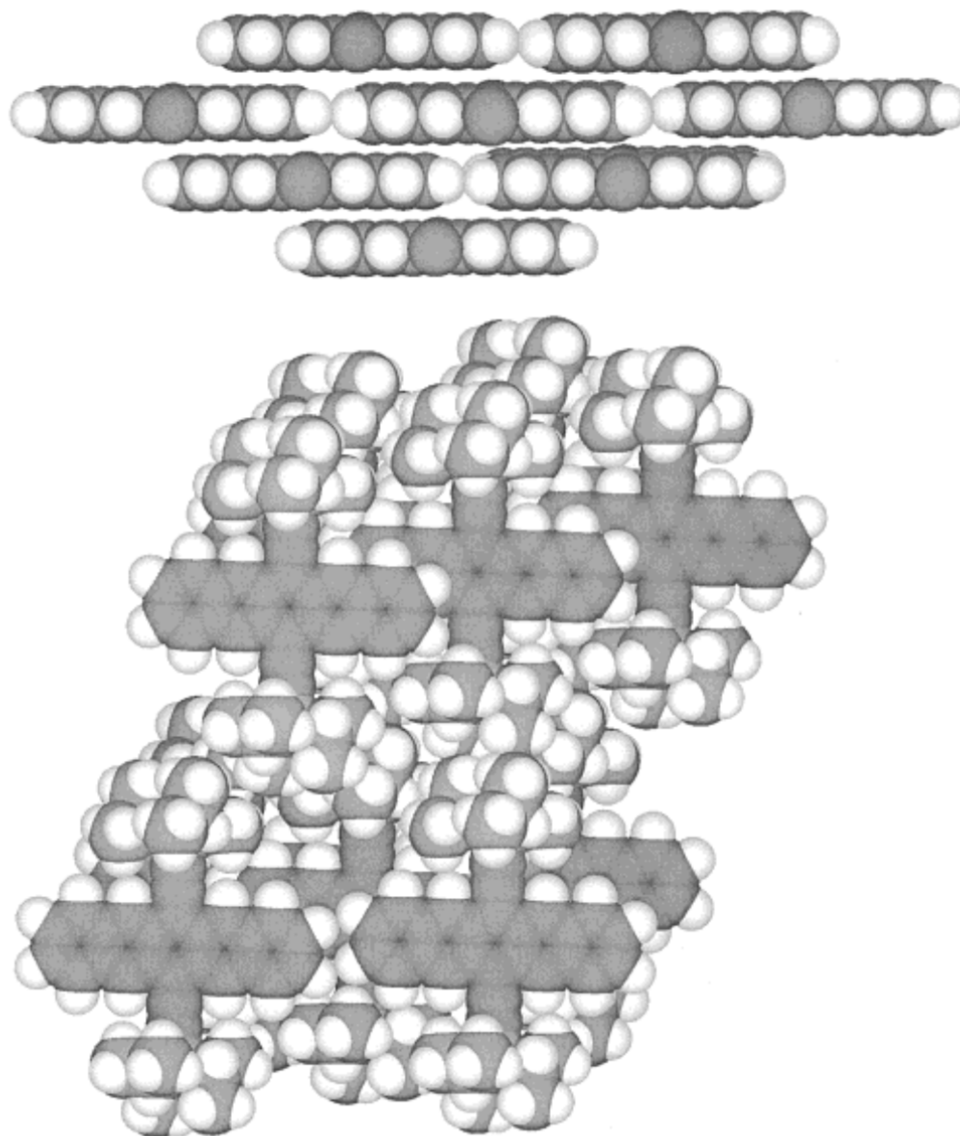

Figure 4.2: Crystal Packing of TIPS-Pentacene

Crystal packing of TIPS-Pentacene, figure taken from Ref. [113].

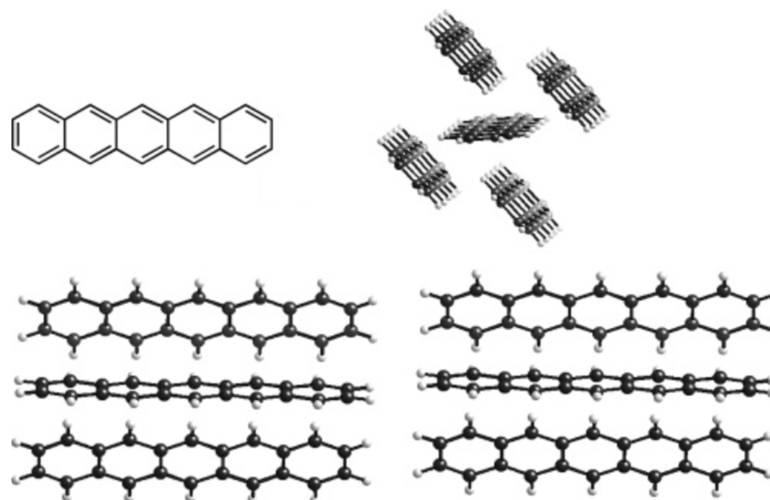

Figure 4.3: Crystal Packing of Pentacene

Crystal packing of Pentacene, figure taken from Ref. [59].

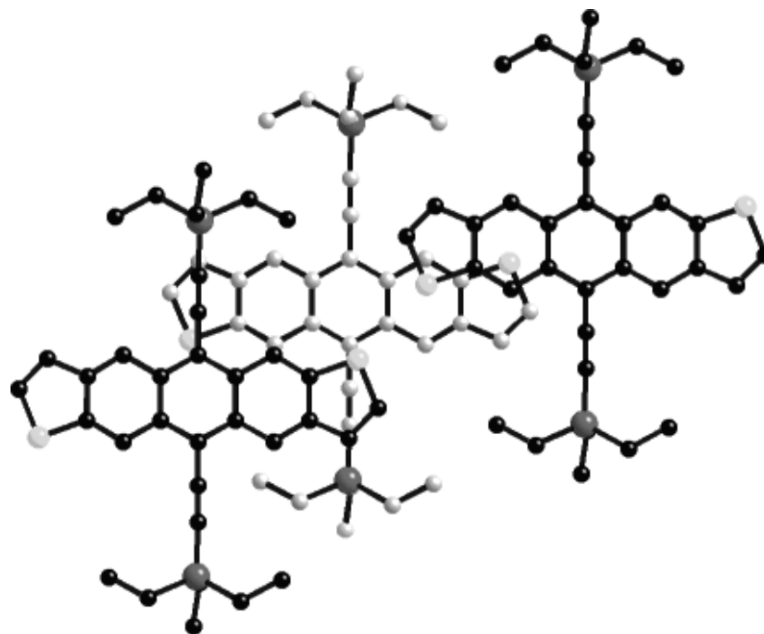

Figure 4.4: Crystal Packing of TES ADT

Crystal packing of TES ADT, figure taken from Ref. [100].

reported in this chapter. The rate of charge trap formation (k_f) and final trap concentration (ϕ_F) were determined by fitting the measured potential vs time to a first order exponential fit.

$$\Delta\phi_T = \phi_O + \phi_F(1 - e^{-kt_g}) \tag{4.1}$$

where $\Delta\phi_T$ is the potential generated by trapped charge, ϕ_O is the potential of the initial charge present (a necessary but small fit parameter that accounts for non-zero initial charge), and t_g is the total gate-on time. The best fit parameters and their relative error were determined using the Matlab Fit function. As was done in Chapter 3, the gate was pulsed, here in 50 ms steps.

4.2.2 Device Fabrication

Silicon substrates to create bottom contact transistors, fabricated exactly as described in Chapter 3. Pentacene devices were created as described in Chapter 3. Before **1** was deposited, the surface was treated with either a liquid or gaseous hexamethyldisilazane (HMDS) treatment to create a self-assembled monolayer over the oxide. HMDS was obtained from Aldrich (CAS 999-97-3, Catalog No. 37921-2, Lot No. PO 1344PO) and used as received. **1** is appealing commercially because it is soluble in many organic solvents. **1** is very soluble in toluene, used here at a concentration of 1 wt%. We used toluene that had been present in the lab for many months, without attempting to remove water. We deposit **1** via three different techniques: drop casting, spin casting, and dip casting.

4.2.3 TIPS Pentacene Deposition

Drop casting was performed in a closed atmosphere and required about 10 minutes for the solution to dry. Drop casting allowed the molecules time to properly align and form crystalline domains. Slow spin casting (about 250 rpm) required about 2-3 minutes for the solvent to dry over the interdigitated regions. When a higher spin speed (2000 rpm) was used, a much more uniform film of about 80 nm thickness was formed, but it showed very poor electronic performance. The film was annealed in a toluene rich environment by placing the substrate upside down over a partially filled beaker of toluene in a closed environment for 10 min. Dip casting is the final deposition technique. The substrate was slowly lifted out of a solution of **1** in toluene over a range of 2-20 min. The substrate is approximately 1.5 cm long, resulting in a movement speed of 0.01-0.001 cm/s rate. The substrate was sealed in a solvent-rich environment during withdrawal and for about 20 minutes after.

4.2.4 TES ADT

Transistors of **2** were created using the same substrates as for **1**, again using tolune as a solvent. **2** was deposited by spin casting at 2000 rpm for 30 seconds, then solvent annealed for 10 minutes. These treatments have previously been shown to improve performance[99]. Two solution concentrations were used: 1 wt% and 2 wt%. **2** deposited this way produced large (about 2-20 μm) crystals easily visible under an optical microscope. 1 wt% solution resulted in incomplete surface coverage, while 2 wt% solution resulted in an increase in the size and number of crystals.

4.3 Results

The four deposition techniques using **1** produced films of very different morphologies shown in Fig. 4.5. Drop casting (Fig. 4.5a) produced very rough surfaces. Root-mean-square surface roughness (R_{RMS}) was determined by Eq. 4.2.

$$R_{\mathrm{RMS}} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(y_i - \overline{y})^2} \tag{4.2}$$

where y_i are the n topographical measurements through the image and $\overline{y}$ is the average height of the image. We found $R_{\mathrm{RMS}} = 127$ nm for the drop cast film. The saturation mobility in drop cast films was measured to be 10^{-3} cm^2/Vs. Slow spin casting (Fig. 4.5b) produced smoother films ($R_{\mathrm{RMS}} = 20$ nm) that are easier to study with EFM, but have a mobility about $10^{-5} - 10^{-4}$ cm^2/Vs. The thickness of the slow spin cast films was very difficult to determine because the thickness increases significantly with increasing distance from the center of spinning. Annealed films had a mobility of about 10^{-4} cm^2/Vs. The surface of the annealed film (Fig. 4.5c) were smooth ($R_{\mathrm{RMS}} = 23$ nm) but showed distinct small crystals. Dip casting (Fig. 4.5d) produced partial film coverage of highly variable thickness with a maximum mobility of 7×10^{-4} cm^2/Vs and roughness of $R_{\mathrm{RMS}} = 63$ nm.

In all transistors made from **1** we observed significant charge trapping. In general, trapped charge persisted for much longer than in transistors made from **1** than in transistors made from polycrystalline pentacene: while trapped charge in a pentacene films released within eight hours, trapped charge in **1** generally remained for more than 24 hours. Additionally, the concentration of trapped charge in **1** was found to be independent of the time spent in solution prior to

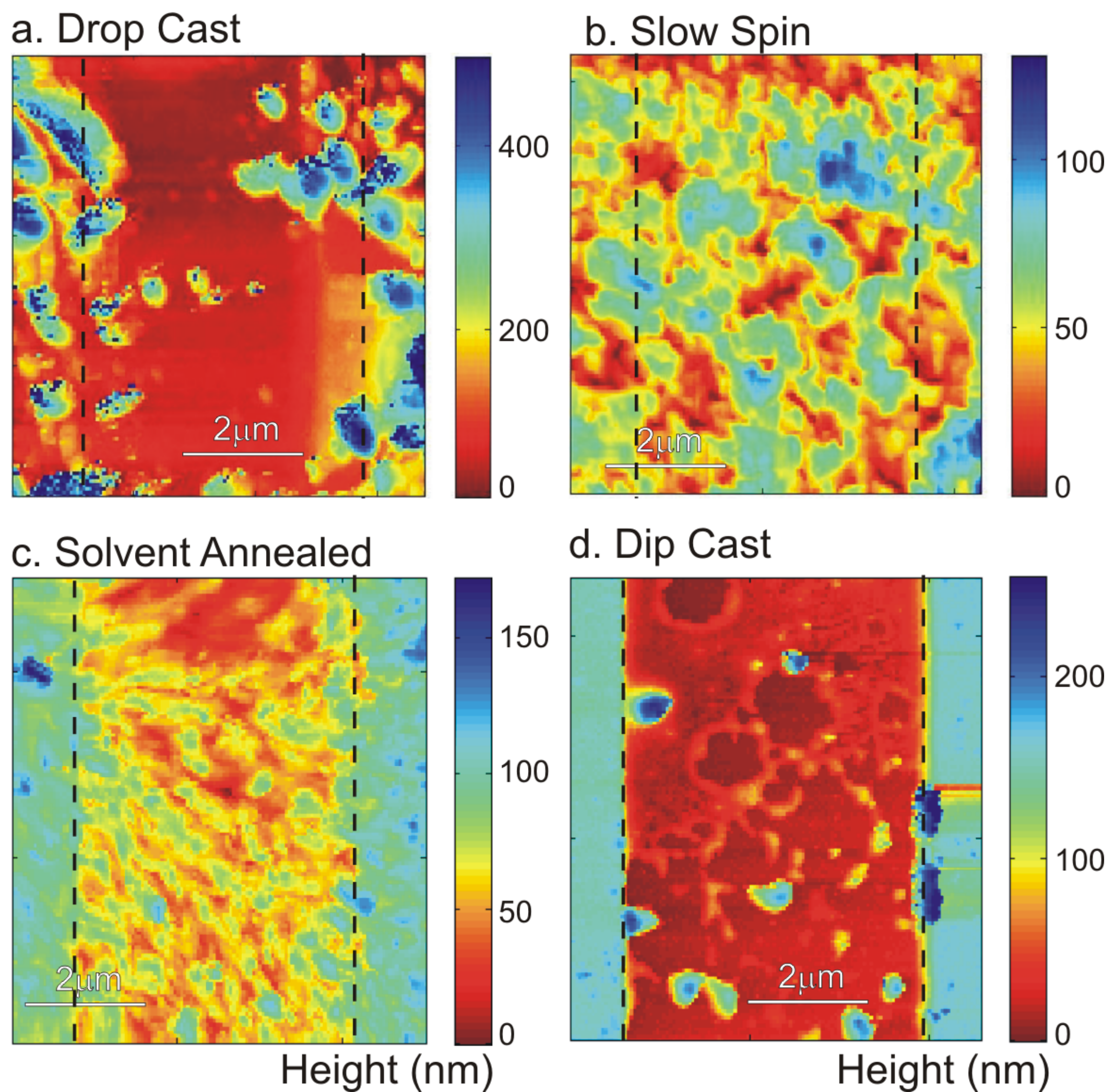

Figure 4.5: Topography of TIPS Pentacene

TIPS pentacene deposited by different techniques: a. drop casting, b. slow spin casting, c. spin casting + solvent anneal, and d. dip casting. Dashed lines indicate electrode positions.

deposition. Transistors made from solutions of **1** left sealed for five days in a lighted area showed similar trap concentrations to those made from fresh solution.

The trap formation pattern was found to depend strongly on the deposition technique, see Fig. 4.6. In general, slower solution evaporation leads to larger continuous trapping domains and fast evaporation produces smaller localized islands of charge trapping. In drop cast films, for example, we observed both regions with no charge trapping (Fig. 4.6a) and with heavy charge trapping (Fig. 4.6b). Surprisingly, trapped charges in some regions in drop cast films (Fig. 4.6c) were found to release very quickly, clearing entirely within 10 minutes in some regions. Trapped charge in slow-spin cast films (Fig. 4.6d) also formed large domains of continuous trapped charge. Trapped charge in solvent-annealed films, however, formed a very different pattern (Fig. 4.6e). Here the trapping is much more homogenous throughout the channel. Finally, trapped charge in dip cast films shows yet another pattern(Fig. 4.6f). This pattern likely arises from the poor TIPS pentacene surface coverage (Fig. 4.5d).

The kinetics of trap formation in **1** were measured in an identical manner to that employed for pentacene in Chapter 3. Because the traps lasted for so much longer, we expected to find a different rate of formation. The trap formation kinetics experiment described in the Methods section of Chapter 3 was performed for both drop cast and slow spin cast films. The gate was pulsed for 50 ms between each measurement. There are two parameters to compare: rate of formation and final charge trap concentration. These parameters for drop cast and slow spin cast films of **1** are shown in Fig. 4.7a and b. These parameters for an unmodified pentacene transistor measured at the same time are shown in Fig. 4.7c for comparison.

The rate of trap formation observed in drop cast films of **1** was much higher

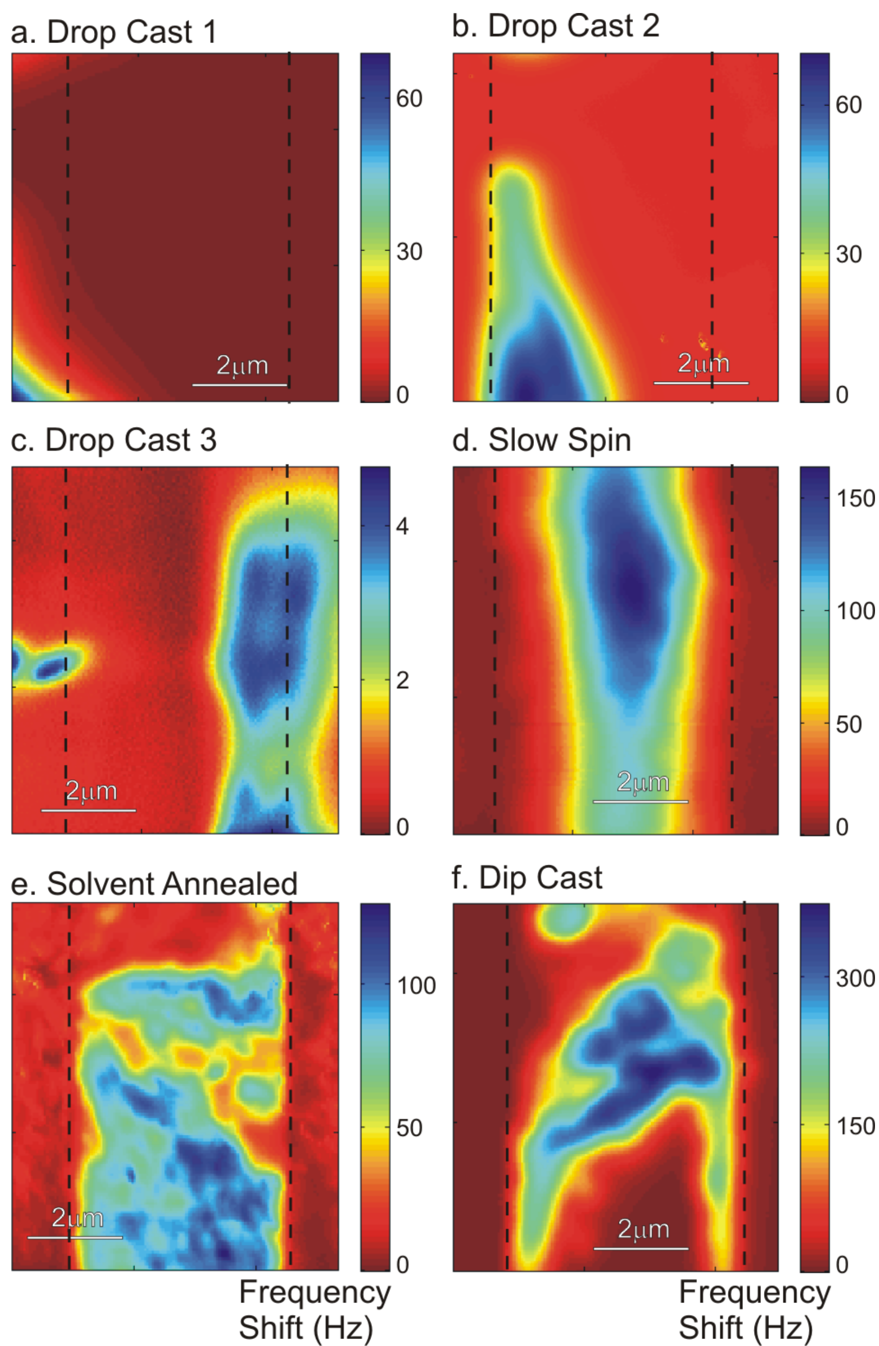

Figure 4.6: Charge Trap Patterns in TIPS-Pentacene

TIPS pentacene deposited by different techniques: In these images blue indicates a higher concentration of (positive) trapped charge. Drop casting shows a. regions with no trapping, b. regions with heavy trapping, c. regions with traps that release in less than ten minutes, d. Slow spin casting, e. Spin casting + solvent anneal, and f. dip casting. The cantilever tip is about 100 nm over the surface, and a gate voltage of -50 V was used to fill the traps. Dashed lines indicate electrode positions.

than that observed in slow spin cast films of **1**, but this might arise from the lower hole mobility in the slow spin cast film. Surprisingly, the unmodified pentacene trap formation rate lies between these two cases. The final trap concentration in drop cast **1** shows a unique behavior: it appears to saturate. This suggests that at this one location in the drop cast film, free holes were no longer the limiting reagent. By contrast, the final hole concentration in the slow spin cast film did not saturate. This further differentiates the trap formation mechanism in **1** from that of unmodified pentacene, where the final hole concentration has never been observed to saturate in an EFM experiment[109, 88].

One further difference between **1** and unmodified pentacene that quickly became clear was the trapped charge release rate. Unmodified pentacene typically requires about 8 hours for trapped charge to completely clear, while most locations in **1** required more than 24 hours. Images of trap charge clearing in **1** are shown in Fig. 4.8. In some regions of a drop cast film (Fig. 4.8a), trapped charge was completely released within 10 minutes (Fig. 4.8b). Slow spin cast films also showed trap retention for greater than 24 hours (Fig. 4.8c). Interestingly, application of a positive gate voltage was found to clear all of the trapped charge within 60 seconds (Fig. 4.8d). The same response was observed in annealed films (Fig. 4.8e-f), where again all of the trapped charge was quickly and completely released. Finally, we observed that the charge trapping in dip cast films (Fig. 4.8g) did not completely clear upon application of a gate voltage (Fig. 4.8h).

We also measured the saturation mobility of **1**. The trap clearing effects of positive gate bias encouraged us to measure both hole and electron mobilities. Saturation mobility was determined by fitting the square root of the saturation current vs. the applied gate potential [28], shown in Fig. 4.9. The hole mobility

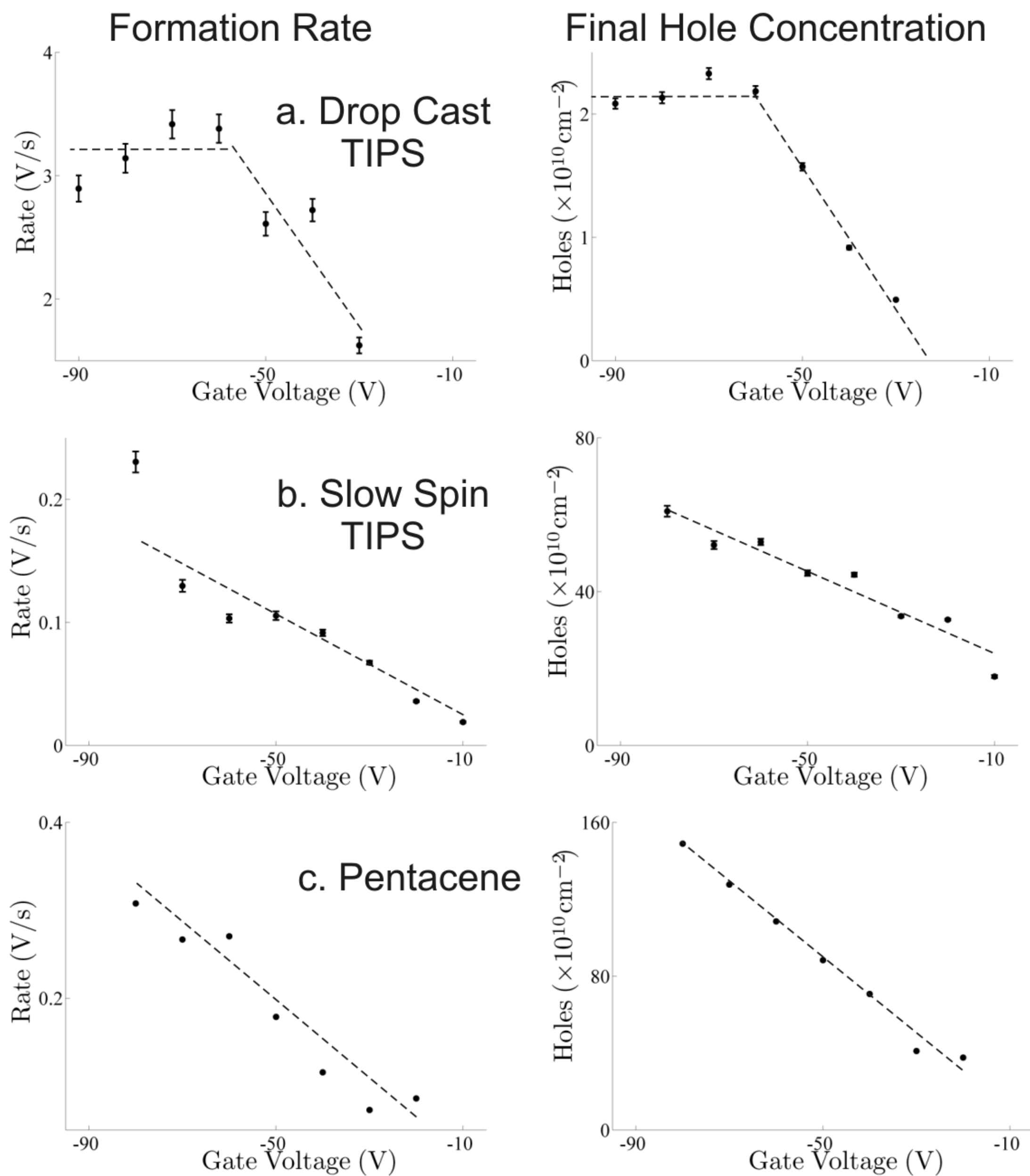

Figure 4.7: Kinetics of Trap Formation in TIPS Pentacene

Trap formation rate and final trapped hole concentrations for: a. drop-cast TIPS pentacene (dashed lines indicate saturation in this sample), b. slow spin cast TIPS pentacene, and for comparison, c. unmodified pentacene. The data was collected and fit as described in the text.

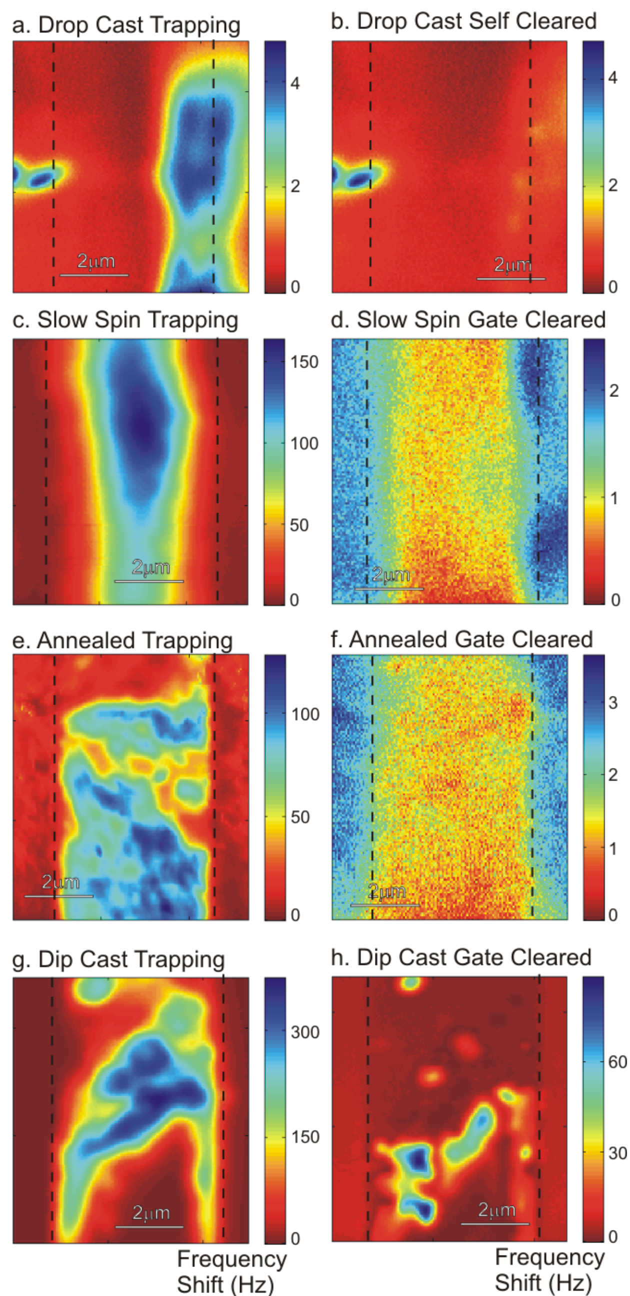

Figure 4.8: Passive and Active Trap Clearing in TIPS Pentacene

TIPS pentacene deposited by different techniques: a. Trapped charge in drop cast films will b. clear within 10 minutes without external bias (the frequency shift on the left is due to a large topographical pillar). c. Traps in both slow-spin and e. solvent-annealed films will d,f. clear by the application of +50 V of gate voltage. g. Traps in dip-cast films only h. clear in some regions, possibly those with a continuous film. The cantilever tip is about 100 nm over the surface, and a gate voltage of -50 V was used to fill the traps initially. Dashed lines indicate electrode positions.

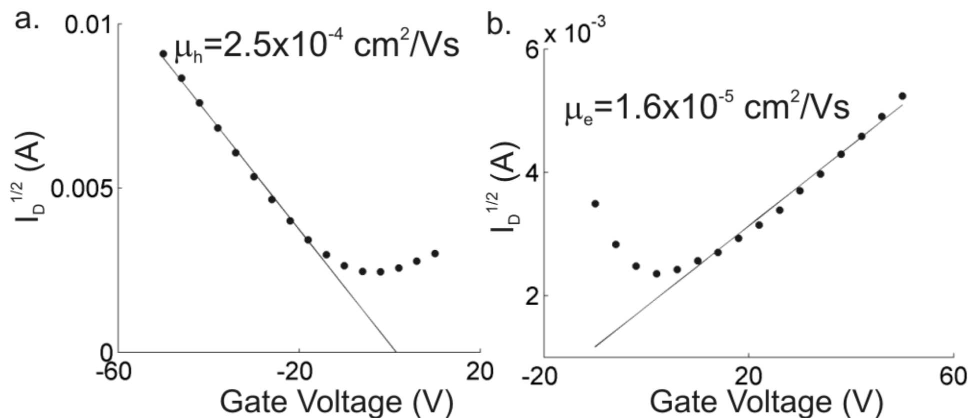

Figure 4.9: Hole and Electron Mobility Determination in TIPS Pentacene

Plot of the square root of saturation current vs applied gate voltage for a. negative and b. positive gate voltage. The data from ±20V to ±60V is fit to determine the indicated hole mobility (μ_h) and electron mobility (μ_e). A source-drain bias of -50 V was used for all measurements. The sample is a TIPS pentacene transistor prepared by fast spin cast followed by a 10 minute anneal.

(Fig. 4.9a) in this sample was only 2.5×10^{-4} cm^2/Vs, a relatively low value. The electron mobility (Fig. 4.9b) is measured at 1.6×10^{-5} cm^2/Vs, the first time to our knowledge that a finite electron mobility has been observed in **1**. While the hole mobility is relatively low for **1**, the measured electron mobility demonstrates that electrons do inject into **1** from gold electrodes.

2 produced large crystals easily visible under an optical microscope. The highest mobility found was 10^{-4} cm^2/Vs. The topography and charge trapping properties of **2** are shown in Fig. 4.10 for two different solution concentrations. The 1 wt% solution shows isolated crystals that bend over the electrode into the channel (Fig. 4.10a) and $R_{\mathrm{RMS}} = 63$ nm. Surprisingly, and in contrast with **1**, charge trapping in **2** was found only at the outer edge of the crystal (Fig. 4.10b). The 2 wt% solution shows a structure of overlapping crystal leaves (Fig. 4.10d) and $R_{\mathrm{RMS}} = 34$ nm. Here too, charge trapping is only seen at the outer edges of crystals (Fig. 4.10e).

Unlike **1**, however, positive gate voltage does not have such a dramatic effect on the clearing of charge traps in **2**. Application of 30 seconds of −50 V gate voltage clears only few of the trapped charges (Fig. 4.10c). This may be due to either a very low electron mobility in **2** or to the inability of gold electrodes to inject electrons into **2**. Further application of gate voltage was found to clear more of the trapped charges, but slowly. Even several minutes of positive gate voltage are insufficient to clear the trapped charges, though those closest to the electrode are cleared preferentially (Fig. 4.10f), indicating the ability of the gold to inject electrons, though at a lower rate than with **1**.

4.4 Discussion

Trapped charge is clearly present at high concentration in transistors made from both **1** and **2**. The spatial distributions of long-lived traps seen in films of **1** and **2** are qualitatively different from both the homogeneous regions of trapped charge seen before in polyflourenethiophene [181] as well as the large-area [88] or localized regions [109] of trapped charge seen before in polycrystalline pentacene. The spatial distribution of trapped charge is qualitatively different in films of **1** and **2**.

Transistors made from **2** exhibit micron-sized single crystals whose interiors are essentially trap free. Conversion of free holes to trapped holes in **2** takes place nearly exclusively at the crystal surface. These observations indicate that silyl groups alone, at least in well-formed crystals, are not a potent source of long-lived *hole* traps. The absence of any traps after applying positive gate voltage also shows that silyl groups in crystalline films of functionalized pentacene are also not a source of long-lived *electron* traps, as suggested in Ref. [106].

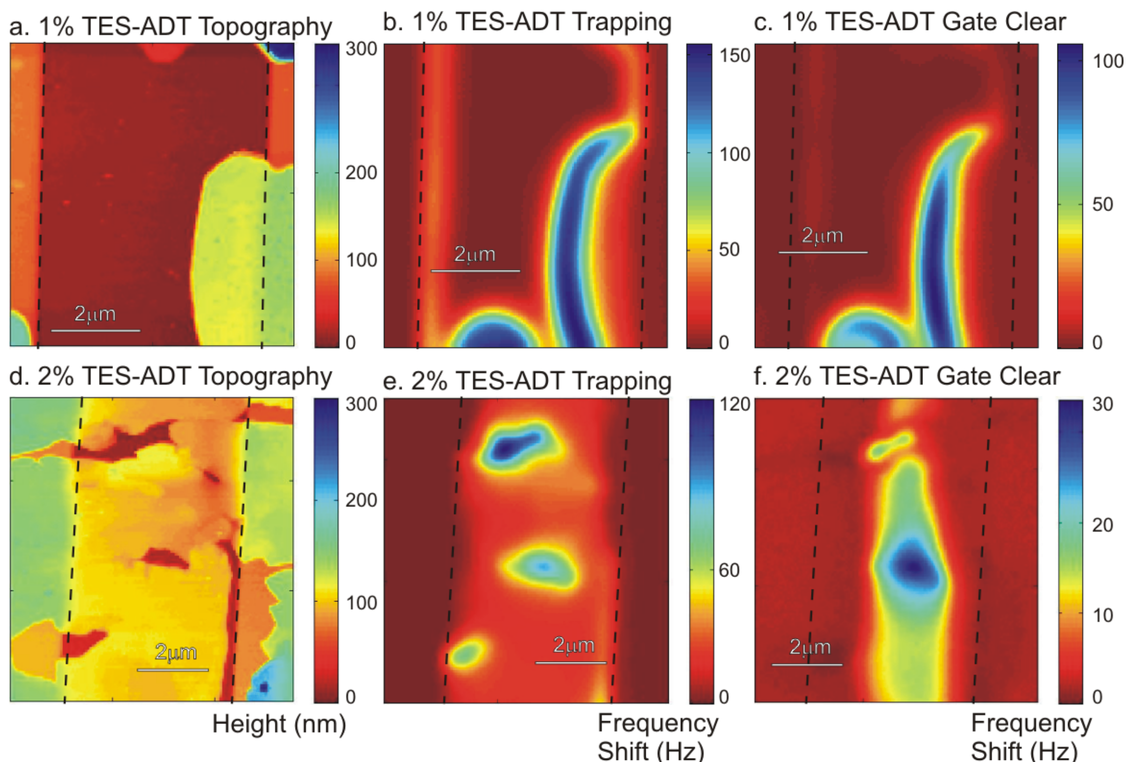

Figure 4.10: Charge trap performance of TES ADT

TES ADT deposited at 1 wt% deposition (a-c) and 2 wt% deposition (d-f). TES ADT forms large crystals (a, d) that show charge trapping only at the edge of the crystals (b, e). Application of positive gate voltage only clears some traps (c, f). The cantilever tip is about 100 nm over the surface, and a gate voltage of -50 V was used to fill the traps. A gate voltage of +50 V was used to attempt to clear the traps. Dashed lines indicate electrode positions.

Films of **1** were prepared with a range of mobilities and topographies and a large variation in the spatial distribution and lifetime of long-lived hole traps was found.

The lowest mobility films of **1**, and presumably the most poorly ordered, were those prepared by slow spinning. In these films the initial trap formation rate depended strongly on hole concentration, consistent with the conversion of free holes to trapped holes being an activated process, such as a chemical reaction. The concentration of trapped holes increases linearly with free hole concentration

in transistors of **1** prepared by slow spinning. This continuous increase indicates that free holes are a limiting reagent in the conversion of free holes to trapped holes, as seen previously in transistors made from as-received pentacene [109, 88].

The highest mobility films of **1**, and presumably the most highly ordered, were those prepared by drop casting. In these films, in contrast, the concentration of trapped holes becomes *independent* of free hole concentration for V_G below -60 V (corresponding to an initial free hole concentration of 4.3×10^{12} charges/cm^2 and a final trap concentration of 2.1×10^{10} charges/cm^2). This finding is consistent with hole trapping being due to a chemical reaction in which an impurity (or potentially a low concentration physical defect) becomes depleted and is therefore the limiting reagent.

If we assume that the transistor's accumulation layer is only one monolayer thick, we can estimate the concentration of the putative impurity. From the X-ray structure of **1**[89], we calculate the planar density of molecules in a monolayer to be 7.7×10^{13} cm^{-2}. The observed concentration of trapped charge corresponds to a planar impurity concentration of 0.027% at this location, equivalent to a volume concentration of impurity of approximately 4 parts per million. This concentration is very low. It therefore makes sense that trap saturation could be observed in **1** but not in pentacene: compound **1** is of far higher purity than the used-as-received Aldrich pentacene employed in our previous EFM studies of charge trapping in pentacene [88, 109]. Interestingly, in transistors of **1** prepared by drop casting the *rate* of conversion of free holes to trapped holes is also essentially independent of the free hole concentration. While the holes must be participating in the chemical reaction, once the impurity becomes depleted the free holes seem to be no longer involved in the rate-determining step.

Our finding that the charge trap concentration is independent of the time that **1** was stored in solvent further suggests that the impurity involved in the charge trapping reaction is not one produced by photochemical degradation [104, 105] or reaction of **1** with the solvent. The impurity could thus be either (1) present initially, due to side-reactions during synthesis, (2) formed by a reaction with light and/or air during the 20 minutes required to transfer the sample into vacuum [104], or (3) formed by reaction of holes with the dielectric of with residual water or oxygen at the dielectric surface in vacuum [182]. In polyflourenethiophene transistors in which the substrate was known to be involved in charge trap formation, EFM images always showed long-lived traps to be distributed homogeneously throughout the transistor channel [181]. This is not what is seen here with **1**. The wide variation in the spatial distribution seen among transistors made from **1** prepared on nominally identical substrates (4.6) would therefore seem to rule out (3).

The finding that trapped charge can cleared in films of **1** on the seconds timescale by application of a positive (e.g., electron injecting) gate bias indicates that (1) electrons can be facilely injected into **1** from gold, (2) **1** conducts electrons, and (3) that the injection of electrons is an effective way to release trapped charge. The injection of electrons into **1** from gold is in agreement with calculations which indicate that the LUMO of **1** is 0.31 eV below the LUMO in pentacene [104]. We thus expect that electrons should inject into **1** from gold more easily than into pentacene from gold, in agreement with what is observed. When investigated by transport measurements, slow spin cast films were indeed found to have an electron mobility of $\mu_{e,\mathrm{sat}} \sim 10^{-8}$ cm^2/Vs, while annealed films showed a mobility in the range of $\mu_{e,\mathrm{sat}} \sim 10^{-5} - 10^{-11}$ cm^2/Vs.

Finally we should note that our measurements provide a lower estimate of the

total amount of trapped charge. Our experiments are sensitive only to trapped charge with lifetimes longer than a few hundred milliseconds. Shallow traps, such as those invoked to rationalize the charge-concentration dependent mobility seen in transistors made of **1**[110, 111], may also be present, but we do not detect them in our experiments.

4.5 Conclusions

In this chapter, we explored charge trapping in two molecules: TIPS pentacene (**1**) and TES ADT (**2**). Figures 4.6 and 4.10 are the first direct evidence of long-lived charge traps in both materials. In contrast with previous work using photoexcited carriers, the charge trapping observed here formed from free holes the findings are therefore directly applicable to transistors.

Trapped holes in TIPS pentacene transistors with gold electrodes were quickly and completely cleared by application of positive gate bias. Transistor curves provided independent evidence of electron injection into TIPS pentacene from gold, leading us to conclude that charge trap formation can be reversed by the introduction of electrons.

We observed significant variation in the spatial distribution, rate of formation, and final concentration of long-lived trapped charge in TIPS pentacene films prepared by four deposition techniques. Trap release times varied from greater than 24 hours to less than 5 minutes within one drop cast sample. These observations establish that charge trapping in TIPS pentacene is at least as sensitive to morphology, and therefore device preparation, as mobility is [183, 94, 97, 96]. The broader implication is that comparing transistor performance between compounds

(such as **1**, **2**, and pentacene) should be done only if morphology is controlled for.

In TES ADT we found that traps were far more prevalent at grain boundaries. This makes TES ADT only the second polyacene to exhibit direct evidence of grain boundary trapping [172], to our knowledge.

In a drop cast TIPS pentacene film, local saturation of a charge trap was seen for the first time in any pentacene derivative. This suggests the possibility that traps may arise from a low concentration chemical impurity (or perhaps a rate reactive defect site) which becomes the limiting reagent at higher gate biases. If this indirect physical evidence of a chemical impurity is born out by further measurements, it would indicate that transistor applications would benefit from developing a route to further purifying TIPS pentacene. Comparing TIPS pentacene and TES ADT we see that crystalline packing is not a necessary condition for trap-free films, since large trap free regions could be found even in drop-cast TIPS pentacene films with amorphous-looking topography. Cations of TIPS pentacene are not inherently prone to trapping and degradation in an unilluminated film.

CHAPTER 5

VARIABLE TEMPERATURE STUDY OF CHARGE TRAPPING KINETICS

5.1 Introduction

This chapter continues the investigation of charge trapping in polycrystalline pentacene films begun in Chapter 3. The trap build experiment used here is identical to that discussed in the Methods section of Chapter 3 except that the scan speed has been increased. While Chapter 3 used the Stanford Research SR620 to demodulate frequency, here we use the RHK PLLPRO. This enabled much quicker measurement of trap formation: each successive potential measurement in Chapter 3 required five minutes to collect, but required only about two seconds in this chapter. The results of Chapter 3 strongly suggested that charge trap formation in polycrystalline pentacene is an activated process.

In this chapter we first investigate charge trapping at two temperatures and observe a large change in both trap formation rate and concentration with change in temperature. We then measure formation rate at multiple temperatures, but these measurements were corrupted by irreproducible initial conditions. Variable Temperature EFM measurements were harder than expected due to two factors: First, we observed slow recovery of initial rates during successive measurements of charge trap formation. We correct for this slow recovery by introducing light and again measure the trap formation rate at multiple temperatures, finding a trap formation activation energy of 0.16 ± 0.06 eV. During this experiment, we noticed slow piezo drifting between successive measurements resulting in a change of the cantilever-sample position. Further efforts are underway to measure and control

this drift, but will not be completed until after the submission of this thesis.

Pentacene samples were created in the manner described in the Methods section of Chapter 3 exactly. The cantilever had a frequency of 75 kHz, a quality factor of 5×10^3, and a spring constant of 1 N/m. During VFM measurements it was held about 100 nm over the surface. Fixed VFM was conducted with a tip voltage of -2 V. Swept and Modulated VFM were conducted using the common parameters listed in Chapter 2. The determination of trap formation rate in this chapter was slightly different. Instead of looking at half-time of formation, which requires that the final concentration be reached, we instead measure the initial rate of formation, as shown in Fig. 5.1. There are two techniques used to calculate the initial rate: we first fit the second to sixth measurements of potential to a line and extract the slope (see Fig. 5.1a and b), then fit the second to eleventh measurements of the derivative of the potential with time (see Fig. 5.1c and d). The derivative fit is then extrapolated to t= 0. The first measurement of potential is discarded because it fits poorly - possibly because any residual intermediate species present would contribute to the potential found by this measurement. We find that the derivative method gives more consistent results and is used in this chapter.

5.2 Initial Observation of Trapping at Two Temperatures

To explore the effects of temperature on polycrystalline pentacene films, we initially measured the formation rate of charge traps both at room temperature and at 80°C. The results of these two experiments are shown in Fig. 5.2. At room temperature we observed a large grain pentacene film with spatially varying trapping similar to that observed previously. When the sample was heated, however, we observed new

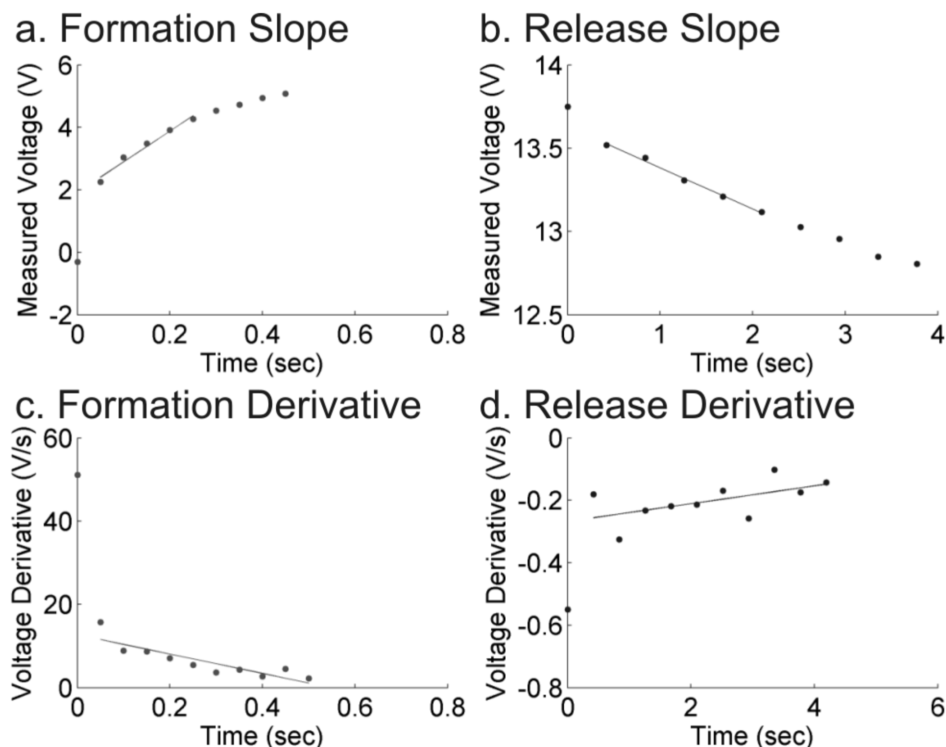

Figure 5.1: Techniques for determining charge trap formation and release rates.

Determination of initial rate of a. formation and b. release by calculating the slope of potential measurements 2-6. Determination of initial rate of c. formation and d. release by fitting the derivative of measurements 2-11, and extrapolating back to zero. The polycrystalline pentacene transistor was at room temperature, -50 V gate bias pulses of 50 ms were applied between each measurement. Cantilever was roughly 100 nm over the polycrystalline pentacene film.

behavior. At 80°C we first observed a change in the topography of the device. This suggests that the pentacene molecules may be slightly mobile at this temperature. This is consistent with the observation that heating the substrate to 60°C during pentacene evaporation increases the size of the grains[184]. These larger grains are likely the result of pentacene molecules moving across the surface during deposition to join pre-existing crystal formations.

We also see a change in the charge trapping distribution: at 80°C we observed

channel-wide charge trapping. Furthermore, we observed very quick trap release. The charges were released during the 5 minutes required to image them. When creating an image, the cantilever tip starts at the bottom left of the image, then scans to the right. The next scan begins after the tip is moved up one line, as indicated in Fig. 5.2b inset. We believe that the trapped charge concentration throughout the channel was nearly homogenous initially and that the heterogenous pattern observed arose because the trap release time was comparable to scan speed. The trap formation rate and final concentration are compared in Fig. 5.2c and d, respectively. The increase in trap formation rate observed at higher temperatures qualitatively supports the claim that trap formation is an activated process. The increase in charge trap concentration - both locally at the measured location and in the film overall - suggest that more trap sites were created when the sample was heated, perhaps as the result of the pentacene molecules becoming more mobile. If, as Northrup suggests, the traps are caused by chemical impurities formed by atmospheric exposure, then the top layers of the film should contain many defects. When heated, perhaps these interchange with pentacene molecules in the active layer of the channel.

5.3 Variable Temperature EFM Trapping Study

The temperature-dependent rates observed in this preliminary experiment prompted us to further study the temperature dependence of charge trapping. Here we introduce *variable temperature* time resolved electric force microscopy of charge trap formation in polycrystalline pentacene. Instead of measuring the kinetics of trap formation at two temperatures, we now measure the formation rate at 26°C, 37°C, 49°C, and 55°C at seven gate voltages from -20 V to -80 V. All measurements

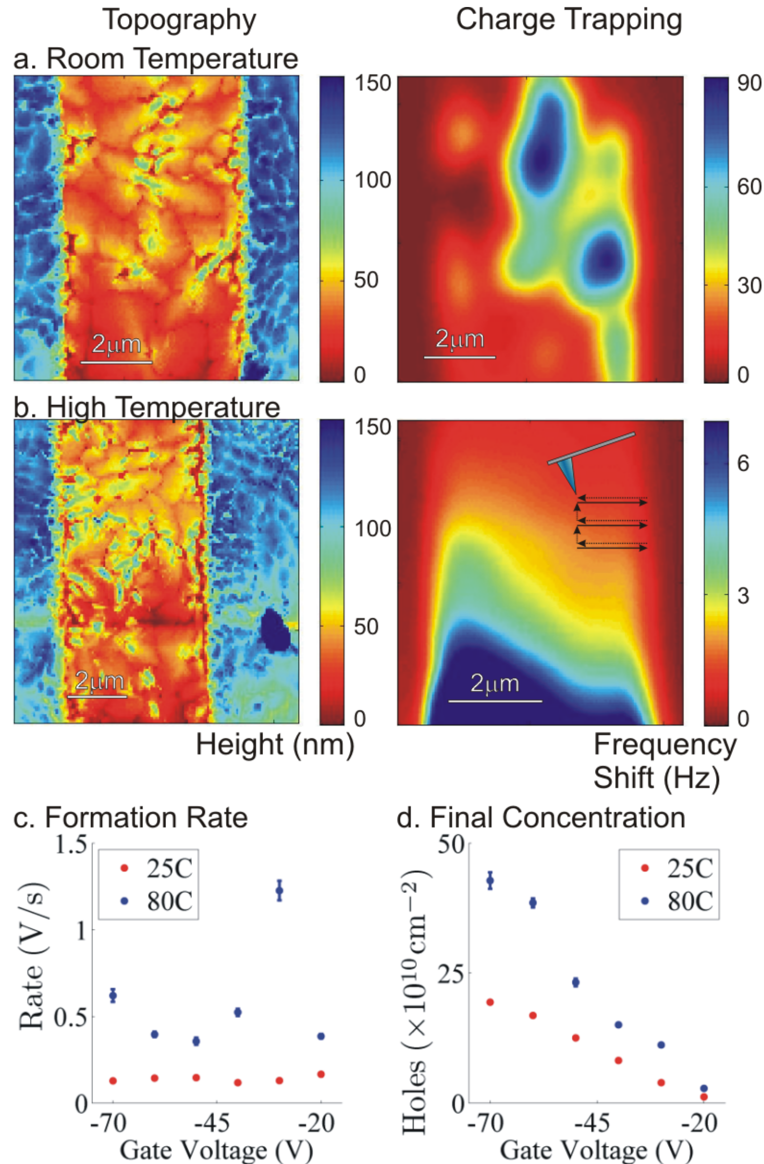

Figure 5.2: Effect of Temperature Change on Topography and Trapping in Pentacene

a. Room temperature topography and charge trap patterns. The charge traps were created by applying -50 V to the gate. b. The topography and charge trap pattern at 80°C. Here the trapped charges are released during the time of the scan. The cantilever starts in the bottom left of the image, records moving right, then moves to the line above as indicated by the figure inset. c. The trap formation rate and d. final hole concentration of various gate biases at both temperatures. At higher temperatures, both rates and concentrations are increased. Topography takes about 10 s per line, while Fixed VFM takes about 2 seconds per line. The cantilever was generally about 100 nm above the surface during Fixed VFM images and trap formation pointscans. Sample was a 25 nm polycrystalline pentacene thin film transistor.

were performed at a single location in a pentacene sample, chosen because it had a high concentration of trapped charge. The rate at each condition was measured once, the error of the rate was calculated from the fit of the derivative by Matlab. Example fits can be seen in Fig. 5.1.

The results of these measurements are shown in Fig. 5.3. If trap formation is an activated chemical process, it should obey the Arrhenius Law: $R = Ae^{\frac{-E_A}{k_B T}}$, where R is the observed rate, A is the exponential prefactor, E_A is the activation energy, k_B is the Boltzmann constant, and T is the temperature. To fit this equation, we take the natural logarithm of both sides. Log(R) plotted against 1/T should form a line with negative slope when gate voltage is constant. The activation energy can be calculated from this slope.

Fig. 5.3a shows the log of the formation rate plotted against one over temperature. Higher temperatures are to the left, while lower are to the right. Each gate voltage is plotted in a unique color. For example the magenta markers, $V_G = -70$ V, show a slight decrease in rate as temperature drops but does not fit well to a line. The activation energy was calculated by linear fit in Matlab for each gate voltage. The best fit line is also plotted in Fig. 5.3a for each gate voltage. The qualities of the fits, χ^2, are shown in Fig. 5.3c and the energies, E_A, are shown in Fig. 5.3e. The errors of the energies are calculated by the Matlab Fit function. The energies are all near zero with large errors. The trap release rates were also measured at each temperature and gate voltage and are shown in Fig. 5.3b. The fit qualities and activation energies were again calculated for each gate voltage and shown in Fig. 5.3d and Fig. 5.3f. The errors of these energies are again generally larger than the values. We next use Linear Least Squares to both calculate a weighted average of the activation energies and to determine the uncertainty in

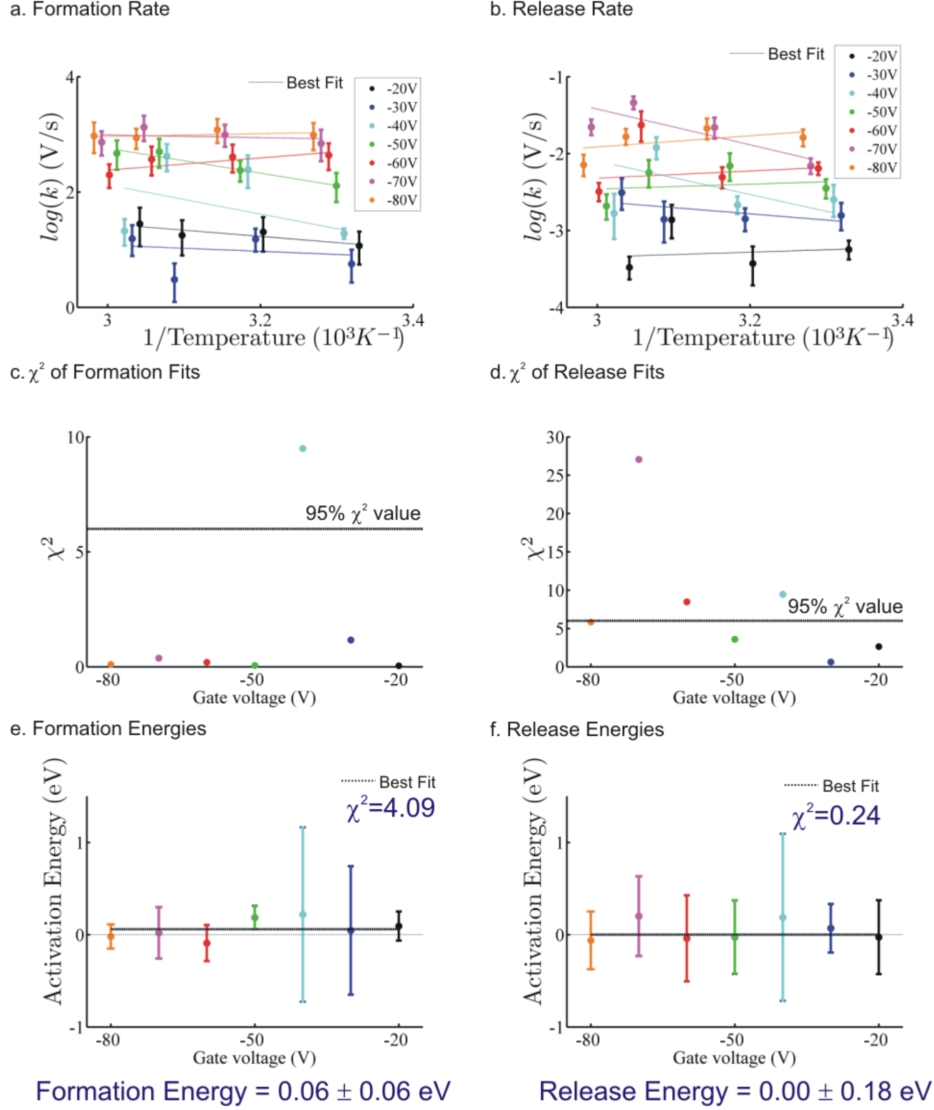

Figure 5.3: Temperature Dependent Rates

Variable temperature trap formation and release rates in a polycrystalline pentacene thin film transistor. a. The natural log of trap formation rate and b. natural log of trap release rate are plotted as a function of inverse temperature (x-axis) and for different gate voltages (color). These rates are fit to the Arrhenius equation, and activation energy extracted. The χ^2 values for these fits are shown for c. trap formation and d. trap release. The 95% χ^2 value is also plotted. Activation energies from fits with a χ^2 value greater than the 95% limit are not used. The energies determined at each gate voltage for both e. trap formation and f. trap release are statistically averaged together (dashed line) to give the final energy values at the bottom of the figure, as discussed in the text.

this averaged value.

Linear Least Squares (both with and without weights) is discussed thoroughly in Numerical Methods[185]. The approach used here mirrors that of Numerical Methods. We first present the general Linear Least Squares, then show how it is adapted to our needs. We define a linear least squares problem statement of $\vec{y} = f_1(\vec{x}) \times a_1 + f_2(\vec{x}) \times a_2 + f_3(\vec{x}) \times a_3 + ...f_n(\vec{x}) \times a_n$. Here $\vec{y}$ is the vector of m observed values y_i, $\vec{x}$ is a vector of m coordinate values x_i, corresponding to each y_i observed, $f_j(x)$ is a desired fit function, and a_j is a fit parameter for each $f_j(x)$. There are n fit functions and parameters. The problem statement can be rewritten as $\vec{y} = \mathbf{X}\vec{a}$. $\vec{a}$ is a vector of the a_j fit parameters and $\mathbf{X}$ is the $n \times m$ matrix formed by mapping the desired fit functions over the x_i values: $\mathbf{X}_{ij} = f_j(x_i)$. We define weights ($W_i$) for the y_i observation as $W_i = \frac{1}{\sigma_i^2}$, where σ_i is the standard deviation of y_i observation. The $\mathbf{X}$ matrix becomes the weighted matrix $\mathbf{A}$ as $\mathbf{A}_{ij} = \frac{f_j(x_i)}{\sigma_i}$. We also define a weighted observable (b_i) as $b_i = \frac{y_i}{\sigma_i}$. The standard solutions for nonweighted and weighted Linear Least Squares are given in Eqs. 5.1 and 5.2[185].

$$\vec{a}_{\text{nonweighted}} = (\mathbf{X}^T\mathbf{X})^{-1}\mathbf{X}^T\vec{y} \tag{5.1}$$

$$\vec{a}_{\text{weighted}} = (\mathbf{A}^T\mathbf{A})^{-1}\mathbf{A}^T\vec{b} \tag{5.2}$$

To fit to the Arrhenius Law, we use $\log(R)$ as y and $1/T$ and x data. The weights here are calculated by error propagation of the standard deviation in the rates, shown in Eq. 5.3.

$$\sigma_{\log(R)} = \frac{\sigma_R}{R} \tag{5.3}$$

The activation energies determined by fit to Arrhenius law are averaged over gate voltages to give an average ($\overline{E_A}$). A weighted average is a simplified version of the general Least Squares solution (Eq. 5.2), shown in Eq. 5.4.

$$\overline{E_A} = \frac{\sum_{i=1}^{m} \frac{E_{A,i}}{\sigma_{E,i}^2}}{\sum_{i=1}^{m} \frac{1}{\sigma_{E,i}^2}} \tag{5.4}$$

Where $m = 7$ is the number of gate voltages and $\sigma_{E,i}$ are the standard deviations of the activation energies calculated for each gate voltage. Using Eq. 5.4, we calculate an activation energy of trap formation of 0.06 eV and an activation energy of trap release of 0.00 eV.

The quality of the fit is determined by χ^2 analysis, discussed in Numerical Methods[185]. We calculate χ^2 from the weighted residuals ($\vec{r}$).

$$\vec{r} = \vec{b} - \mathbf{A}\vec{a} \tag{5.5}$$

$$\chi^2 = r.r \tag{5.6}$$

A fit is considered "good" when the value of χ^2 is small. More precisely, the χ^2 value for $m - n$ degrees of freedom indicates the probability that the fit is valid. Successive fits of data with randomly distributed noise will create a distribution of χ^2 values with various probabilities. For example, for $m - n = 2$ degrees of freedom, 95% of the χ^2 values of good fits should be less than 5.99 - larger χ^2 values have only a 5% chance of occurring when the fit is valid[185]. In this experiment, all fits with a χ^2 values greater than the 95% value are rejected. χ^2 values for fits are shown in Fig. 5.3c and d. For those fits with χ^2 less than the 95% threshold, we calculate the variance (σ_j^2) of the fit parameters (a_j) by Eq. 5.7[185].

$$S = (\mathbf{A}^T \mathbf{A})^{-1} \tag{5.7}$$

S is the covariance matrix of the best-fit parameters. S_{jj} is the variance ($\sigma_{a,j}^2$) of the parameter a_j, while S_{jk} gives the covariance[185] between parameters a_j and a_k. The confidence interval (CI) of the parameters is calculated from the variance (σ^2) using the Student T distribution[185].

$$CI = \frac{\sigma t}{\sqrt{n}} \tag{5.8}$$

σ is the standard deviation of the measurements, t is the Student's T value, extracted from a table for a specific confidence level[185], and n is the number of measurements.

Using Eq. 5.8, we calculate errors at 95% confidence for the trap formation activation energies shown in Fig. 5.3e and f. We calculate an error of the averaged activation energy of trap formation of 0.06 eV and an error of the averaged activation energy of trap release of 0.18 eV using Eq. 5.7. The χ^2 values for these fits listed in Fig. 5.3e and f, both values are below the 95% cutoff value of 14.07 for 6 degrees of freedom, indicating the fit is valid.

This variable temperature EFM study of trap formation and release did not yield activation energies for either trap formation or release that were statistically different from zero. This indicates that the observed rates do not fit the Arrhenius Law. We believe that this was due to systematic error: we did not allow enough time between measurements for the chemical environment to reset to initial conditions. This will be shown in the in the next section.

5.4 Using Light to Clear Charge Traps

In Chapter 3, we presented data that demonstrated that a long time was required for trapped charge to fully release from a pentacene transistor. When the film was allowed to relax for 24 hours, the measured formation rate was reproducible. Successive measurements of charge trap formation over one location with 24 hours between measurements are shown in Fig. 5.4a. Successive scans are numbered. The potential is normalized to allow comparison of initial rates between scans of slightly different final trap concentrations. When the film was given less than 24 hours to relax, the formation rate was not reproducible, see Fig. 5.4b. Successive measurements in this experiment were repeated as soon as no trapped charge from the previous measurement could be detected. Nevertheless, each successive measurement yielded a faster rate. We speculate that an intermediate uncharged species remained which affects the initial rate. This intermediate species might react with free holes during the next measurement to trap charge more quickly than in a pristine film.

To facilitate initialization of the uncharged intermediate, we introduced light. This was suggested in Chapter 4 as a way to clear trapped charges. We use a white LED, Lite-On Technology Corporation Part No. LTW-1KHC5, at a 30° angle approximately 1 cm from the surface with a estimated power intensity of 3 mW/cm^2. A voltage of 3.2 V is used to power the LED; the power intensity was estimated from included documentation. The spectrum of light emitted by the LED has a sharp peak about 460 nm, and a very broad peak centered on 575 nm. Application of an LED very quickly clears trapped charge in pentacene, shown in Fig. 5.4c. We find that even 2 seconds of light exposure quickly clears all the trapped charge, but additional exposure is required to remove the intermediate

species. The proposed intermediate species requires up to 300 seconds of light exposure to fully decay, as shown in Fig. 5.4d. The rate of trap formation seems to be fully recovered for 300 and 400 seconds of light exposure, suggesting all intermediate species had been cleared. Furthermore, introducing a dark time of 600 seconds after 300 seconds of light exposure completely reset the trap formation, as shown in Fig. 5.4e.

Although successive measurements of trap formation in this sample overlapped using both 300 seconds of light and 600 seconds of dark, this approach was not universally successful. Successive measurements in another sample using this approach did not yield fully reproducible results, shown in Fig. 5.4f. We speculate that perhaps we are not completely clearing the intermediate species, but instead the sample is reaching a steady, non-equilibrium state between measurements. Perhaps the intermediate is being reduced to a consistent non-zero level between each scan in Fig. 5.4e, while in Fig. 5.4f the intermediate concentration after light exposure is slightly different each time. Alternatively, subsequent work on this apparatus showed that drift in the coarse approach piezo was a problem. This may account for the shifting final potential during the measurements of Fig. 5.4f. To solve this problem, we have recently modified the software to check the tip-sample distance before each trap formation pointscan.

5.5 Variable Temperature with Light

Using the LED to clear trapped charge as described above, we repeated the variable temperature trap formation measurement at temperatures of 24°C, 35°C, 44°C, 53°C, and 62°C and at 6 gate voltages from -20 V to -70 V. The results of these

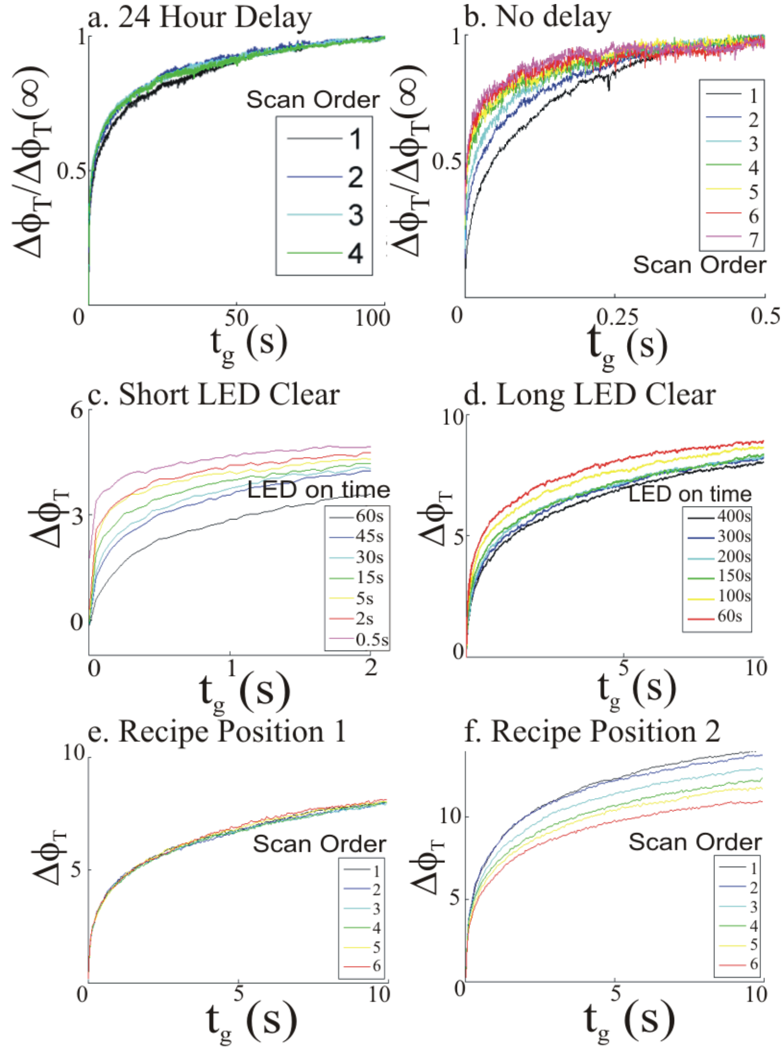

Figure 5.4: Variations in Pentacene Charge Trap Formation Rate

Successive trap formation pointscans on a 25 nm thin film polycrystalline pentacene thin film. a. When measurements were separated by 24 hours, similar rates were observed. b. When experiment was repeated quickly, the rate of formation increased with each scan. c. Short exposure to light generated by an LED quickly cleared trapped charge. d. Longer exposure assisted the decomposition of any intermediate species. We found that about 300 s of light exposure were required to recover trap formation rates. e. We observed reproducible trap formation using a recipe of 300 s of LED time followed by 600 s of dark waiting. f. This same recipe in another sample was not as successful, though here piezo drift may be responsible for the shifted final potential. All experiments used 50 ms pulses of $V_G = -50$ V. The legend indicates the order of successive scans. The measured potential has been normalized in a. and b. to allow comparison of formation rate between measurements with different final concentrations.

experiments are shown in Fig. 5.5. The trap formation rates are shown in Fig. 5.5a and follow the Arrhenius Law more closely than before, though there are still some data points that don't fit well. During the measurement of trap formation at $V_G = -50$ V and 53°C, the cantilever drifted into the sample. This changed the calculated rate, but the error was not immediately detected. This data point was omitted from fitting. The rates were again fit to the Arrhenius Law. The χ^2 values and the extracted activation energies are plotted in Fig. 5.5c and e, respectively. The charge trap release rates, χ^2 values, and activation energies were also calculated and shown in Fig. 5.5b, d, and f respectively. We use Eq. 5.4, Eq. 5.7, and Eq. 5.8 to calculate an average value, the variance, and 95% confidence interval, respectively, of the activation energies. As before, fits with χ^2 values greater than the 95% limit were omitted from averaging. We report a trap formation activation energy of 0.16 ± 0.06 eV and a trap release activation energy of 0.35 ± 1.12 eV.

The χ^2 values of 0.36 and 0.00 for formation and release, respectively indicate much better fits than the first variable temperature measurement. The trap release activation energy, however, is not statistically above from zero because most fits were omitted due to the large χ^2 values of individual gate voltages. Furthermore, even those trap release fits with acceptable χ^2 values had large errors in the extracted parameters. The poor fits suggest that the charge trap release might be an activationless process. This might be the case, for example, if charge trap release required electrons to inject from the gold into the pentacene, then slowly hop to the trap sites. If the slowest step of the trap release process were electron transport, then we might not observe a temperature dependence. Alternatively, the activation energy may be very small and our poor fits are due to further systematic error.

Although we successfully measured a positive activation energy for charge trap formation, there were several known experimental problems. We believe that the tip height changed over time, causing changes in the measured potential. Potential is only weakly dependent on height for a planar charge distribution but more strongly dependent if the tip and trapped charge are modeled as point charges[40]. Future experiments are planned to repeat this measurement while verifying sample distance between each scan. These experiments will not be completed until after the submission of this thesis.

5.6 Atmospheric Exposure

Previous work has suggested that charge trapping in polycrystalline pentacene is due to reactions with atmospheric water[46, 45, 79, 53, 80, 81, 47] or oxygen[82, 83, 81, 53, 48]. Both of these possibilities were discussed in Chapter 1. To further explore the hypothesis that charge traps are created by atmosphere exposure, we studied the concentration of charge traps as a function of atmospheric exposure time. Maps of trapped charge are shown in Fig. 5.6. A 25 nm thin film of pentacene was deposited onto a bottom contact transistor substrate and allowed to cool in vacuum. The device was loaded into the EFM as quickly as possible. We estimate that the film was exposed to air for a maximum of 20 minutes during loading. A Fixed VFM measurement after one minute of applying the indicated gate bias revealed that there were a few charge traps in the film already (Fig. 5.6a). Two gate biases were used: -50 V and -80 V. To expose the sample to air, the vacuum pump was turned off and the chamber was vented. After the 16 hours of air exposure, the vacuum pump was turned back on. Topography was measured to verify that the xy piezos had not drifted. After exposing the sample to the

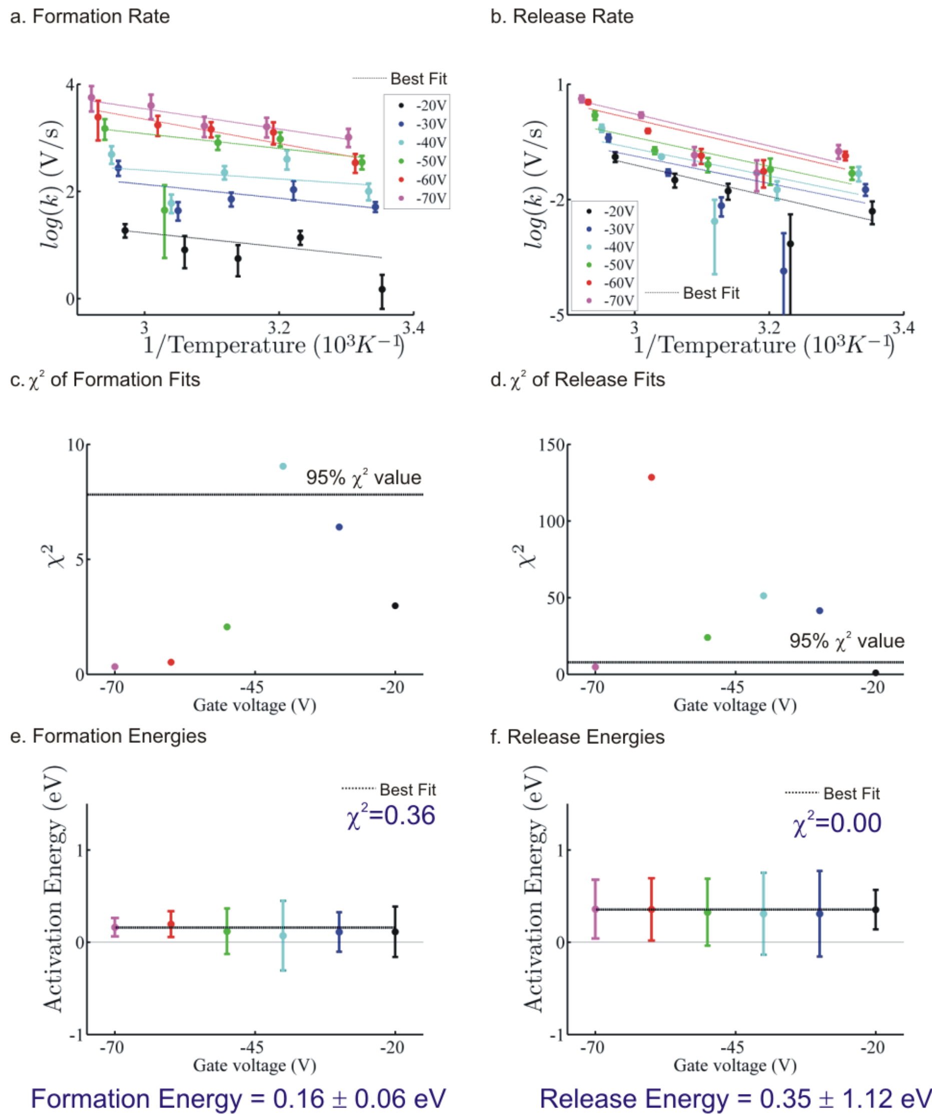

Figure 5.5: Temperature Dependent Rates with Light

Variable temperature trap formation and release rates in a polycrystalline pentacene thin film transistor. The natural log of the rates of a. trap formation and b. trap release are plotted as a function of both inverse temperature (x-axis) and gate voltage (color). These rates are fit to the Arrhenius equation, and activation energy extracted. The χ^2 values for these fits are shown for c. trap formation and d. trap release. The 95% χ^2 value is also plotted. Activation energies from fits with a χ^2 value greater than the 95% limit are not used. The energies determined at each gate voltage for both e. trap formation and f. trap release are statistically averaged together (dotted line) as described in the text to give the final energy values at the bottom of the figure. Using light to reset the sample improves the accuracy of the measurement considerably. The trap formation appears to be activated, though trap release may be an unactivated process.

same gate biases at increased exposure time, Fixed VFM measurements showed significantly increased frequency shift at the previously identified locations. This indicates that the charge trap concentrations increased.

The charge trap concentration further increased after exposure to an additional 24 hours of air (40 hours total) (Fig. 5.6c). The sample was next exposed to air for an additional 65 hours. When a Fixed VFM measurement was attempted, the trapped charge concentration was large enough to disrupt cantilever oscillation. The cantilever was moved about 100 nm farther away from the sample and Fixed VFM measurement was successfully completed, as shown in Fig. 5.6d. Because frequency shift is strongly dependent on the height above the sample, the frequency shift shown in Fig. 5.6d was smaller than that seen in Fig. 5.6c, though we believe the trap concentration was higher. Modulated or Swept VFM measurements would have produced the potential directly and avoided this height dependence, but there was not sufficient time available to perform such measurements. Even without direct potential measurement, this data clearly shows that the charge trap concentrations in polycrystalline pentacene films increase with exposure to air. This suggest that an impurity, which is not present in as-received pentacene, is created by atmospheric exposure. This was measured by others[46, 45, 79, 53, 80, 81, 47, 82, 83, 48], but our measurement is more direct.

5.7 Monolayer Pentacene

One possible systematic error in the variable temperature EFM measurements was due to the presence of a thick (25 nm) pentacene film. We know that when a negative gate bias is applied, the applied potential lowers the electron chemical

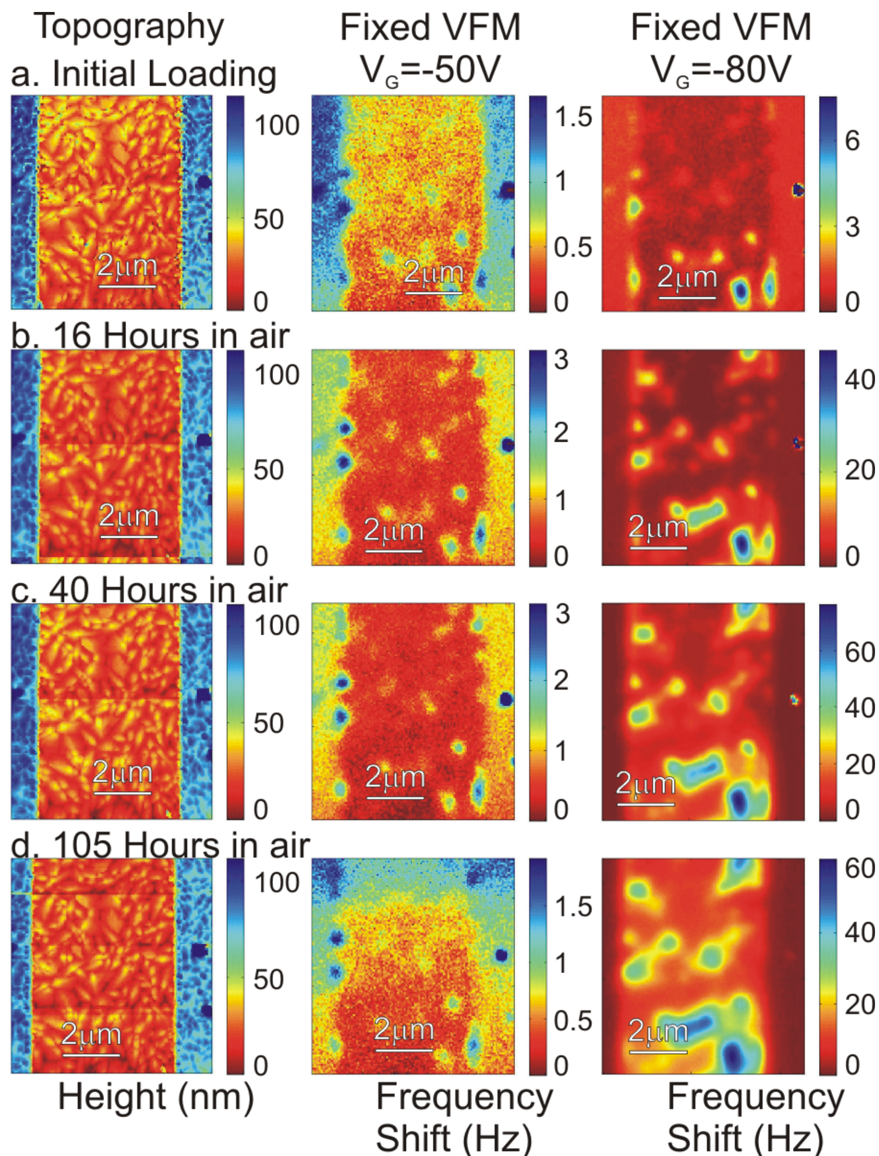

Figure 5.6: Effects of Air-Exposure on Pentacene

Topography and Fixed VFM of a polycrystalline pentacene thin film transistor. Fixed VFM is measured after the indicated gate voltage had been applied for 60 seconds. The tip is roughly 100 nm from the surface during Fixed VFM. a. This sample was loaded into vacuum very quickly after pentacene deposition and little trapping was initially observed. b. 16 hours of air exposure increased the frequency shift observed considerably, especially when $V_G = -80$ V. c. 40 hours of air exposure further increased the trapping seen. d. The potential of the trapped charge after 105 hours of air exposure created too strong of a force on the cantilever to measure by Fixed VFM. The tip was moved to about 200 nm away from the surface. This reduced the total frequency shift seen in these images, though trapped charge concentration further increased.

potential of the interfacial pentacene layer, filling it with free holes. It is not clear how deep into the pentacene layer the chemical potential is affected. We thought that the system could be simplified by creating a transistor with a single monolayer of pentacene. In this proposed device, both free and trapped charge are forced to live in a single monolayer of pentacene. The change in chemical potential would then be confined to a single layer.

Creating a single monolayer pentacene transistor is typically accomplished using a shadow mask, but this approach has limited resolution. Instead, we entered into a collaboration with several scientists from the group of Professor George Malliaras in the Materials Science and Engineering Department at Cornell. They had developed a hydroflouroether solvent compatible with organic materials[186]. In collaboration with the group of Professor Chris Ober, also of the Materials Science and Engineering Department at Cornell, they had developed a novel organic-compatible photoresist[187]. A single monolayer of pentacene was grown on a clean silicon oxide surface by Vladimir Pozdin of the Malliaras group. The oxide surface was cleaned by scrubbing with soap, then sonicating in several steps of DI water for 5 min. each. It was then dried with nitrogen and placed in a UV-ozone cleaner for 10 min. Pentacene was deposited at about 0.1 Å/s. The interdigitated transistor structure with 5 μm channel widths was defined using this organic-compatible photoresist by John Defranco of the Malliaras group in the methods described by Zakhidov[186]. 25 nm of gold was evaporated without a chrome adhesion layer, and liftoff was performed by Dr. Alex Zakhidov of the Malliaras Group. This effort resulted in the creation of single monolayer, 5 μm channel width, top-contact pentacene transistors.

As produced, these devices did not show measurable current upon application of

source, drain, and gate bias. When the device was loaded into the EFM, we found the topography shown in Fig. 5.7a. The actual deposition thickness determined by crystal monitor was about 1.4 layers of pentacene, suggesting that the island seen in the topography are the beginnings of a second layer. When a -50 V gate bias was applied for 60 seconds, Fixed VFM measurements produced a startling image, shown in Fig. 5.7b. It appears that when holes entered the sides of the channel (in response to the gate bias), they quickly became trapped. Swept VFM measurements indicated that the Fixed VFM frequency shift of about 200 Hz in Fig. 5.7b corresponds to a measured potential of +50 V. This means that the concentration of trapped charge was nearly that of the expected gate-induced charge concentration - essentially every charge injected is trapped. Furthermore, when -50 V gate bias was applied for 300 seconds, the trapped charge moved further into the channel, as shown in Fig. 5.7c. We know that holes are injected into the pentacene upon application of negative gate bias in an attempt to fill the channel. We speculate that they slowly hop from trap site to trap site towards the center as the gate bias persists.

We also observed that light exposure allowed the charges to move much more quickly through the channel. Since the application of light released trapped charge from experiments in thicker pentacene films, shown above, we speculate that light releases the trapped holes to travel slightly further, falling into the next available trap. This process continues, but the delay time between hops is significantly decreased. Surprisingly the application of positive gate bias yielded trapped electrons in the channel while the sample was illuminated. We speculate that the excitons created by the light are split and the positive gate bias drives holes away, leaving electrons behind. The holes move slowly through the channel and are extracted into the gold upon reaching the pentacene-gold boundary. Thus electrons appear

to “fill” from the channel edges.

This effect is shown by a Modulated VFM image in Fig. 5.7d. Here a -50 V gate bias was applied while illuminating the sample until the entire channel was filled with trapped holes. Then the gate bias was switched to +50 V for about 60 seconds while maintaining illumination. We observed that near the electrodes the measured potential was negative, indicating trapped electrons. In the center of the channel, the potential was positive, indicating trapped holes. Intriguingly, this image suggests a mechanism to compare effective “hole release rates” locally. In regions where electron trapping extends further into the channel, holes must have a higher release rate to escape more quickly into the gold.

Unfortunately, this sample proved unsuitable for measuring charge trap formation by variable temperature EFM. The experiment described in Chapter 3 assumes that gate-induced free charge fills the channel in significantly less time than the gate pulse duration. This assumption is clearly not valid for this sample. This sample, however, furthers support the idea that trap formation is primarily the result of atmospheric exposure of pentacene after deposition. In a thicker film, the top layers of pentacene shield the interfacial region from the the air across most of the film. Because the monolayer has no protective layers of pentacene, the entire surface was exposed to air and essentially every injected hole becomes trapped. The EFM studies of this section and the last section establish a correlation between atmospheric exposure and charge trapping in pentacene transistors.

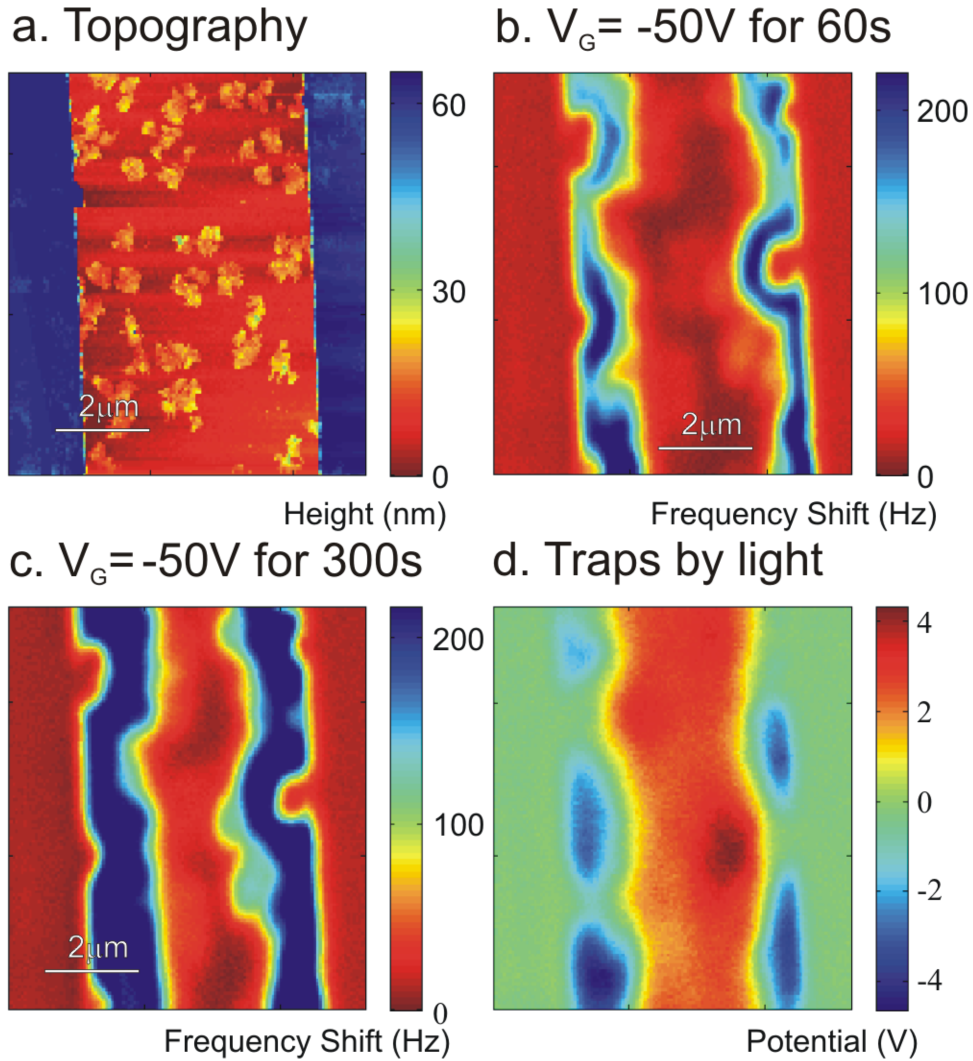

Figure 5.7: Charge Trapping in a Monolayer Pentacene Transistor

a. Topography of a 1.4 layer top contact pentacene thin film transistor created in collaboration with the Malliaras Lab. This transistor showed no electrical activity when created. b. Fixed VFM after 60 seconds of applied -50 V bias to the gate. The trapped charge concentration was extremely high. A frequency shift of 200 Hz measured by Fixed VFM corresponded to +50 V surface potential measured by Swept VFM. This means that nearly every injected charge became trapped. c. Applying 300 s of -50 V gate bias further filled the channel with trapped charges. The charges moved into the channel very slowly. d. Both electrons and holes were trapped in this image: red (positive potential) indicates trapped holes while blue (negative potential) indicates trapped electrons. A -50 V gate bias was applied for several minutes while the sample was exposed to light. This filled the channel with trapped holes. The gate potential was switched to +50 V bias while the light was still on. Although excitons were likely created throughout the sample, only near the electrodes could the holes escape and leave trapped electrons behind.

5.8 Pentacene Conclusions

We have shown in this chapter that charge trap formation in polycrystalline pentacene is an activated process with a measured activation energy of 0.16 ± 0.06 eV. The release of these charge traps may be activationless, perhaps limited by the time required for electrons to reach the charge traps and reverse the trapping reaction. We find that release of trapped charge is dramatically accelerated by exposure of pentacene to white light. Because additional wait time is required to recover reproducible initial trap formation rates, even after all trapped charge has cleared, we believe that charge trap formation has at least one uncharged intermediate step. This intermediate does not decay upon light exposure as quickly as trapped charges release. Finally, two studies provide direct evidence that the primary source of the charge traps is chemical reaction with atmospheric species: trap density increases as a function of air exposure time and we observe essentially complete conversion of free to trapped charge in a single monolayer pentacene device.

There is one final experiment planned with pentacene: trap formation and release rates will be measured by variable temperature EFM while carefully controlling tip-sample distance. It is expected that the results of this experiment will not be available before the completion of this thesis.

CHAPTER 6

IMAGING ION MOTION AND INTERNAL ELECTRIC FIELDS IN TRANSITION METAL LIGHT EMITTING ELECTROCHEMICAL CELLS

6.1 Introduction

In this final chapter, we discuss collaborative work done on study light emitting electrochemical cells. We monitor the ion migration through the channel of an active device to understand the physics which drives migration. We find that the observed results agree with the electrodynamic model of ion migration, where ions migrate to the electrodes to assist charge injection. The ion migration creates a large electric field which, in this sample, occurs at a different location from emission. This work was published in Nature Materials[188]. The bulk of this paper is reproduced here. The Methods section has been expanded.

LEECs differ from other organic light-emitting diodes because they have ions which are mobile in the film and at room temperature. Their redistribution on the application of a bias assists the injection of electronic carriers and enables novel device architectures[124, 146, 147, 156, 157], including fault-tolerant large-area illumination panels[147, 157] as well as illumination panels that can be plugged directly into an a.c. power outlet[157]. Unfortunately, the sandwich-type configuration that is used in LEECs to minimize the thickness of the ionic-Transition Metal Complex (iTMC) layer is not amenable to facile probing by electric force microscopy (EFM). To enable a direct measurement of the electric-field distribution in LEECs with EFM, planar devices were fabricated in which a $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ film was spin-coated onto an insulating substrate with pre-patterned Au electrodes.

6.2 Methods

6.2.1 Device Fabrication

To fabricate the devices, 500 Å of gold (with a 2050 Å Cr adhesion layer) was deposited on an oxide-passivated silicon wafer. The gold surface was treated with a surfactant (Micro 90 cleaning solution) to discourage irreversible adhesion of the parylene layer. Approximately 2 μm of parylene C was deposited on the wafer in a PDS 2010 Labcoater. Parylene dimer was vaporized above 80°C (the furnace was kept at 130°C) and then in a separate chamber, the parylene was pyrolysed into the monomer form at 690°C. The sample was held at room temperature so that the parylene polymerized on contact with the surface forming a conformal film. A Shipley SPR 220 3.0 photoresist was spun on at 4000 r.p.m. and pre-baked at 115°C for 90 seconds. The device patterns were exposed on a contact aligner and developed after a post-exposure bake at the same time and temperature as the pre-bake. The parylene layer was etched in an oxygen plasma etcher at 150 W for 1215 minutes, removing it completely from the gold in the patterned areas. The wafer was then etched in a Veeco ion mill to remove the gold layer underneath. Interdigitated electrode stacks of gold and parylene were left on the wafer. For patterned devices, a dilute solution of $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ (2 mg in 1 ml of acetonitrile) was then spin-cast in a nitrogen glove box onto individual devices at 8000 r.p.m., to make a layer of around 200 Å in the channels. The parylene was peeled from the gold, leaving $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ in the channel, but not on top of the electrodes, as shown in Fig. 6.2, right panel. Unpatterned devices were prepared by peeling off the parylene before spin-coating; hence, these were subject to the same processing steps as the patterned devices. Both types of film were

imaged using atomic force microscopy and scanning electron microscopy to ensure uniform coverage of $[Ru(bpy)_3]^{2+}(PF_6^-)^2$. A complete discussion of parylene use can be found in DeFranco[189].

6.2.2 Electric Force Microscopy

Devices for EFM measurement were transported directly from the glove box to a custom-built EFM[40] in a vacuum desiccator to minimize exposure to air and water. Electrical contact for EFM operation was made by connecting wire leads to the devices with SC Electronics Silver Paste, Part No 22-023, during which time devices were exposed to air for approximately 20 minutes. The devices were loaded into the EFM and the pressure was pumped down to less than 5×10^{-6} mbar. Swept VFM (see Chapter 2) was measured by linescan both initially and during application of source-drain bias. Because ion migration took over an hour to equilibrate, we were able to measure many linescans during the migration process. Labview software was written to repeatedly measure linescans both during the initial bias-induced ion migration and the ion return after the bias was removed. Since $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ does not form smooth films upon deposition, the tip was maintained at a greater elevation over the sample than in previous work. When 5 V or 10 V was applied to source drain, the tip was about 200 nm from the surface. When the applied potential was 120 V, the tip was pulled slightly further back yet - 250 to 300 nm. This was done to prevent contact between tip and sample due to electrostatic forces in case the applied tip potential was significantly different from the local electrostatic potential. Contact results in a (relatively) large current flow that will damage both tip and sample. The cantilever and hardware used are identical to those described Chapter 5 Introduction. The linescan here typically

took about 1.5 minutes to complete.

6.2.3 Optical Microscopy

Patterned devices were mounted in a nitrogen-filled enclosure on an IX-71 inverted microscope (Olympus) and imaged through a $\times 50/0.5$ numerical aperture LMPlanFl objective (Olympus) and a D620/60 emission filter (Chroma). Images were acquired using a Cascade512 CCD camera (Roper Scientific), and analysed with a custom Matlab (The Mathworks) routine. Ten to fifteen rows of pixels (1 pixel = 130 nm) spanning the inter-electrode gap were averaged to decrease noise.

6.2.4 Numerical Simulations

For the numerical simulations, we used the method of forward-time iteration[190] and included ions as described by deMello *et al.*[126, 128]. The mixed-conductor layer had fixed positive ionic charge and mobile negative ionic charge, with densities that were equal to 10^{19}cm^{-3}. These values are underestimates, which enable the simulations to reach steady-state quickly while still capturing the essential physics. It was assumed that the mobilities of the electrons and holes were the same, and their diffusion coefficients obeyed the Einstein equation. The layers were depleted of electronic carriers, and electronic carrier injection was described according to the Scott-Malliaras injection theory[191]. Ion transport across the metal interfaces and charge exchange between the PF_6^- ions and the electrodes were not allowed. The two metals used had the same work function of 5.0 eV, whereas the HOMO and LUMO of the mixed conductor were at 5.3 and 3.0 eV respectively. The simulation was run at 1 V (which, as there was no built-in potential, allowed

injection of electronic carriers) until steady state was achieved.

6.3 Results

Figure 6.1 shows the distribution of the potential (Fig. 6.1a) and the electric field (Fig. 6.1b) in these devices. The thick green trace, which indicates the first measurement after the application of a 5 V bias, shows that the potential drops linearly as a function of distance between the two electrodes. The corresponding electric field is approximately constant, indicating that the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ film acts as a resistor. After 1 hour of continuous application of bias, during which steady-state is reached, the electric field (thick red trace) shows a small enhancement near the cathode, accompanied by a slight decrease throughout the rest of the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ film. On the basis of this electric-field distribution, it is not possible to unambiguously discriminate between the two models of LEEC operation, and hence it is not possible to determine the underlying device physics.

A closer observation of the data, however, reveals considerable changes of the potential over the metal electrodes. This can be seen in Fig. 6.1c, where the potential over the anode decreases substantially with time. This phenomenon can be understood by the diffusion of the PF_6^- counter ions over the metal electrode. A schematic illustration is shown in Fig. 6.2. Under the influence of the applied bias, the counter ions drift towards the anode. However, in the case of a film that extends over the metal electrodes, counter ions that pile up against the anode can diffuse over the electrode. This will result in artificially lower ion concentrations near the electrodes compared with that in sandwich-type devices, where the ions cannot diffuse around the electrode. This difference in boundary conditions causes

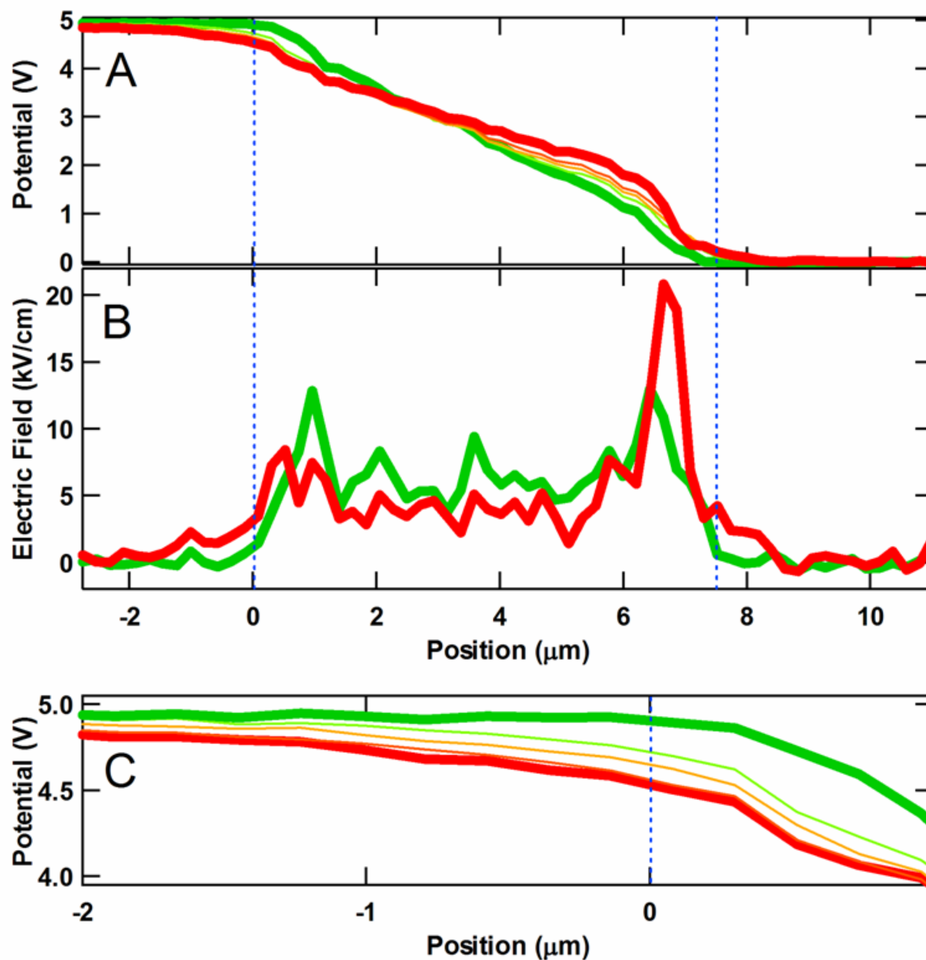

Figure 6.1: Potential Profiles in Unpatterned LEEC

Time dependence of the *in situ* potential and electric-field profiles for Au/$[Ru(bpy)_3]^{2+}(PF_6^-)^2$/Au devices under 5 V operation, in which the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ is unpatterned. In each part, the initial scan on application of a bias is the thick green trace and the final scan is the thick red trace. The inter-electrode region is the region between the blue dashed lines, as determined from the capacitance. a. *In situ* potential across one device. The curves are spaced by equal increments of 15 min in time. b. *In situ* electric field across the same device. c. A close-up near the anode of the *in situ* potential from a, revealing an evolution in the potential at the anode with time. The anode is located to the left of the blue dashed line.

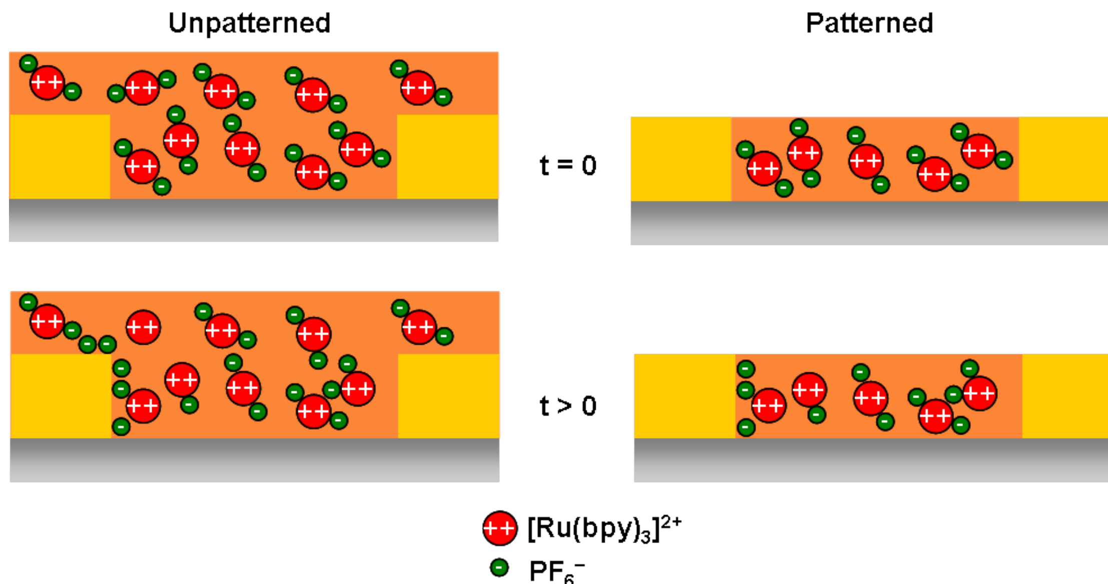

Figure 6.2: Schematic Diagram of LEEC Devices

Schematic diagram of the ionic space-charge effects in unpatterned and patterned Au/$[Ru(bpy)_3]^{2+}(PF_6^-)^2$/Au devices (not to scale). In the unpatterned device, PF_6^- ions can leave the active area and change the potential that is obtained by a surface scan. In the patterned device, the ions are blocked from further lateral motion by the contact.

measurements on unpatterned planar devices to fail to capture the relevant device physics of LEECs. It should be noted that the top-contact devices (in which metal electrodes are deposited on top of the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ film) also suffer from this effect, as ions can diffuse underneath the metal electrodes.

To establish the same boundary conditions as in sandwichtype devices, the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ layer needs to be patterned to avoid overlap with the metal electrodes, as shown in Fig. 6.2. This was achieved by using a variation of the parylene lift-off technique developed by DeFranco *et al.*[189]. Parylene is a chemical-vapour deposited polymer that offers conformal, pinhole-free coatings that adhere weakly to a variety of substrates, including freshly cleaned gold[189, 192]. Planar devices were prepared using the process shown in Fig. 6.3a, as described in detail in

the Methods section. In short, gold was deposited on an oxidized silicon wafer. A layer of parylene was then deposited on top and patterned by photolithography and reactive ion etching. An ion mill was used to etch the gold, with the parylene layer acting as an etch mask. A layer of $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ was then deposited from solution and patterned by peeling off the parylene with the help of adhesive tape. The advantage of this patterning technique is that the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ film is patterned in a self-aligned manner between the electrodes, having sufficient contact to inject electrons and holes, while never coming into contact with solvents or developers. A wide range of materials can be patterned in this manner, including vapour-deposited thin films, provided that the processing temperature is kept below 200°C.

Figure 6.4 shows the distribution of the potential (Fig. 6.4a) and the electric field (Fig. 6.4b) in devices with a $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ layer patterned with the technique outlined above. As with the unpatterned devices, the first measurement (thick green trace), shows that the electric field is approximately constant between the two electrodes. After 1 hour of continuous application of the 5 V bias, however, a large electric-field enhancement is visible near the cathode, and a smaller field is located near the anode (thick red trace). At the same time, the electric field in the bulk of the device is suppressed from 5.4 ± 1.0 kVcm^{-1} to 0.9 ± 0.8 kVcm^{-1}, a reduction by nearly a factor of 6. A small electric field is also apparent near the anode. A closer inspection (Fig. 6.4c) shows that the potential over the electrodes is constant, indicating that the patterned samples effectively confine ions between the two electrodes.

The results of Fig. 6.4 can be qualitatively understood within the context of the electrodynamic model[126, 128]. Under the influence of the applied bias, the PF_6^-

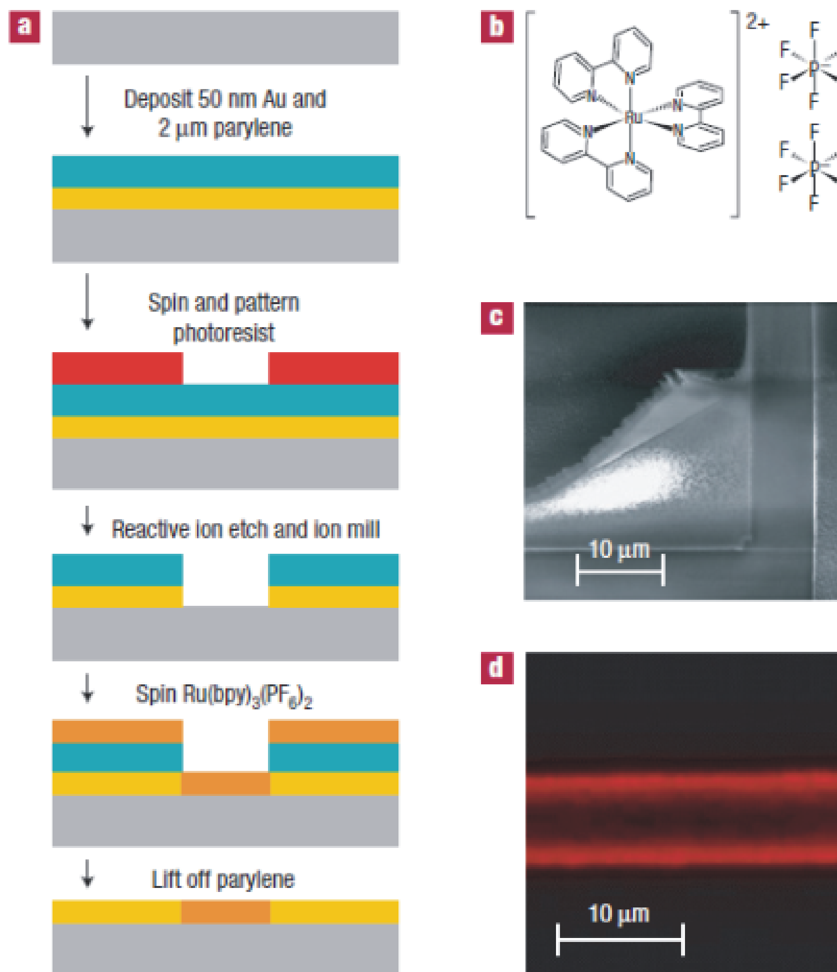

Figure 6.3: LEEC Patterning Process

Patterning $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ with parylene. a. Photolithographic steps for patterning with parylene. b. The structure of $[Ru(bpy)_3]^{2+}(PF_6^-)^2$. c. Scanning electron microscopy image of parylene delaminating from a gold electrode. d. Fluorescence microscopy image of a Au/$[Ru(bpy)_3]^{2+}(PF_6^-)^2$/Au device, showing that the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ film is restricted to the area between the electrodes. (The higher brightness near the electrodes is an optical effect due to scattering by the gold electrodes.).

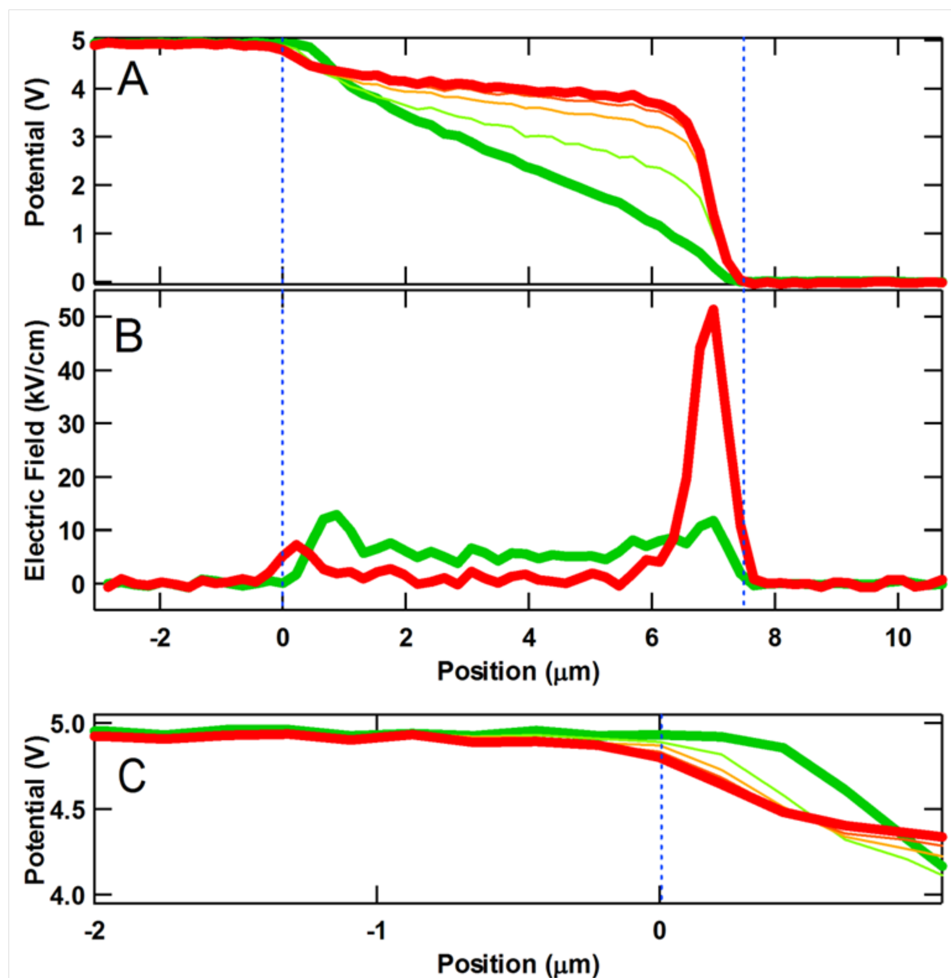

Figure 6.4: Potential Profiles in Patterned LEEC

Time dependence of the *in situ* potential and electric-field profiles for Au/$[Ru(bpy)_3]^{2+}(PF_6^-)^2$/Au devices under 5 V operation, in which the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ layer has been patterned to be restricted between the electrodes. In each part, the initial scan on application of a bias is the thick green trace and the final scan is the thick red trace. The inter-electrode region is the region between the blue dashed lines, as determined from the capacitance. a. *In situ* potential across one device. The curves are spaced by equal increments of 15 min in time. b. *In situ* electric field across the same device. c. A close-up near the anode of the *in situ* potential from a, revealing that the potential over the electrode remains constant with time. The anode is located to the left of the blue dashed line.

counter ions pile up against the anode and are depleted near the cathode. The redistribution creates high electric fields at the electrodes, whereas in the rest of the film the field is screened. The injection of holes and electrons is assisted by the interfacial fields, and these carriers move towards opposite contacts primarily by diffusion. A key prediction of the model is that the redistribution of the ionic charge will self-consistently create the highest electric field near the electrode with the highest barrier for charge injection. This is shown in Fig. 6.5, where a simulation based on the electrodynamic model (see the Methods section) for a planar LEEC with negative mobile ions is shown. The simulation was set up with a smaller barrier for hole injection than for electron injection, and the resulting electric field is the highest near the cathode, where it is needed the most. This observation is in agreement with the results of the EFM measurements. As the Fermi level of gold (work function of 5.1 eV) is closer to the HOMO ($\sim$ 5.8 eV:) than to the LUMO ($\sim$ 3.2 eV)[124] of $[Ru(bpy)_3]^{2+}(PF_6^-)^2$, a higher barrier is expected for electron injection. As a result, the highest electric field occurs near the cathode.

It should be noted that the problem of bipolar current injection in a semiconductor that contains mobile ions is complicated by the large number of parameters that are needed to account for steric effects associated with ion packing and with injection of electronic carriers across metal organic interfaces. Rather than aiming at quantitative agreement with the data, the simulations were meant to provide some insight into the physics of LEEC devices with one mobile ion. As a result, the high electric fields predicted by the simulation are chiefly a consequence of the lack of restriction in the density of ions near the electrodes. In real devices, the density of ions near the electrodes will be limited by steric effects, resulting in smaller interfacial fields.

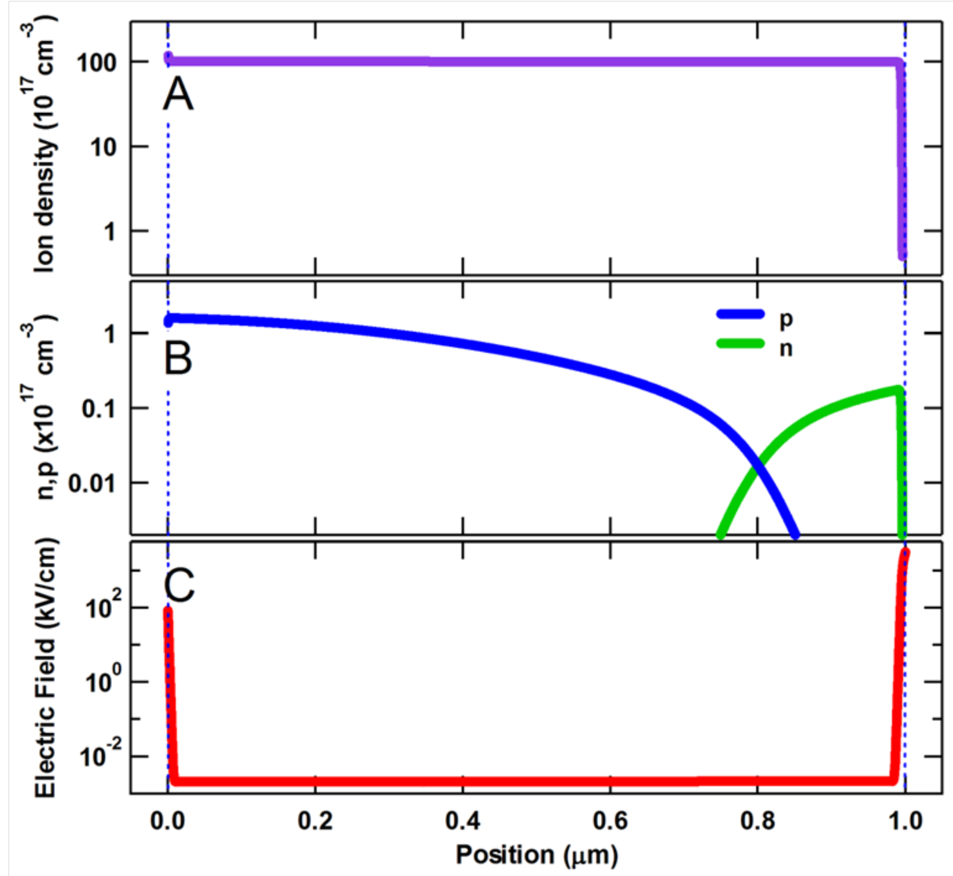

Figure 6.5: LEEC Simulations

Simulation results for carrier and electric-field distributions in an LEEC. Steady-state distributions for a. negative ions, b. electronic carriers, and c. the resulting electric-field profile. The blue dashed lines indicate the positions of the electrodes.

The normalized distributions of potential and electric field in patterned LEECs operating at higher voltages are shown in Fig. 6.6a,b. Qualitatively, the general features of 5 V operation are seen in the data for 15 and 120 V operation (light emission is clearly visible to the eye at the latter voltage). In all three cases, there is a trend towards cancellation of the electric field in the bulk and a drop of the potential near the electrodes. At 120 V, however, some fraction of the potential is distributed over the bulk of the device, leading to an appreciable electric field. This effect is also accounted for by the electrodynamic model: at a high applied bias, the ionic space charge is no longer sufficient to screen the field in the bulk[126].

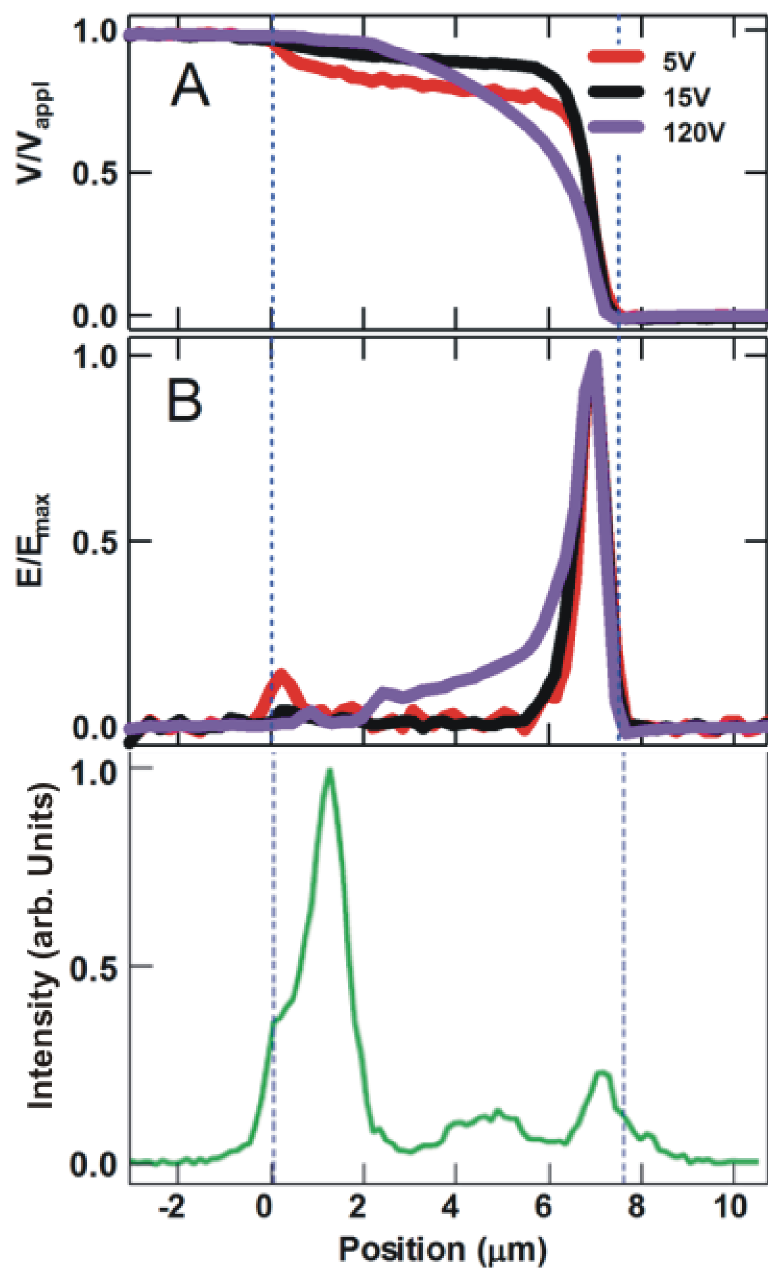

Figure 6.6: Voltage Dependence of LEEC Performance

Voltage dependence of potential and electric-field distributions and spatial profile of light emission. a. Normalized in situ potential and b. electric-field profiles after 1 hour of operation for Au/$[Ru(bpy)_3]^{2+}(PF_6^-)^2$/Au devices under 5, 15 and 120 V. The inter-electrode region is the region between the blue dashed lines, as determined from the capacitance. c. Emission profile from a patterned device acquired at a bias of 120 V. The inter-electrode region is the region between the blue dashed lines, as determined by optical microscopy.

It should be mentioned that the recombination zone in these devices seems to be located near the anode. This was found by mounting a patterned device on an optical microscope and directly imaging its emission with a CCD (charge-coupled device) camera. The data, obtained at a bias of 120 V, are shown in Fig. 6c. The maximum of the emission occurs within less than 2 μm from the anode, whereas a small peak near the cathode is probably due to scattering from the electrode. The location of the maximum was found to remain unchanged as a function of bias down to 30 V, the lowest voltage at which emission was still measurable. The location of the recombination zone implies that the hole mobility in $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ is smaller than the one for electrons[126]. Comparison with Fig. 6.6a,b shows that there is no significant potential drop near the recombination zone. An alternative interpretation is that the recombination zone corresponds to the small peak at 5 μm, but the light is strongly waveguided in the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ film and the peaks near the electrodes arise owing to scattering. Again, the majority of the potential drop is away from the recombination zone.

6.4 Conclusions

The observation of high interfacial fields, as predicted by the electrodynamic model, has important consequences for the design of LEECs. It explains the ability of these devices to function efficiently even when high-work-function (hence air-stable) cathodes are used. The high-energy barrier at the cathode, which would normally prohibit efficient electron injection, is reduced in width by the interfacial electric field. Smaller counter ions can pack near the electrodes with greater density and produce higher electric fields at the electrodes that help inject electrons and holes more efficiently. On the other hand, if too many ions pile up near an

electrode, the resulting electric field will be very high, leading to local electrochemical breakdown of the device. Such phenomena are not only important for LEECs, but for all solid-state ionic devices. Here we have established that EFM measurements on planar and appropriately patterned devices can help to quantify these effects, understand the underlying physics and improve the performance of mixed-conductor devices.

6.5 Author Contributions

The following work on light emitting electrochemical cells (LEECs) was done in collaboration with the groups of Dr. Malliaras, Dr. Craighead, and Dr. Abruña. In the group of Dr. George Malliaras, Jason D. Slinker was the principle coordinator, designed experiments, connected other collaborators, and wrote the paper. John A. Defranco developed the parylene liftoff technique and fabricated all substrates. In the group of Dr. Harold G. Craighead, Jose M. Moran-Mirabal measured the light emission by optical microscopy. In the group of Dr. Hector D. Abruña, Yu-Wu Zhong helped with the theoretical calculations. The EFM measurements were performed by members of the Marohn group. This work was published in Nature Materials[188].

6.6 Correspondence

After this paper was published, Pei and Heeger published an critique[193] of the above conclusions. Their first principle objection is that this material is poorly suited for this study. Specifically, in $[Ru(bpy)_3]^{2+}(PF_6^-)^2$, the $[Ru(bpy)^3]^{2+}$ can be

oxidized to $[Ru(bpy)^3]^{3+}$ or reduced to $[Ru(bpy)^3]^{1+}$ with associated redistribution of the PF^{6-} counterions. The conductivity of holes and electrons changes when $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ is doped. Furthermore, they claim that the resolution of the EFM is not sufficient and that large electric fields we measured might occur up to 1 μm away from the electrode, in disagreement with the electrodynamic model.

Malliaras *et al.*[194] published a response to these two objections. First, while the exact mobilities of electrons and holes in $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ are not known, the mobilities must be substantial to support electroluminescence. This has been extensively studied in LEECs made from $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ and its derivatives over the past decade[158]. We would thus expect that the observed interfacial fields are not a peculiarity of the $[Ru(bpy)_3]^{2+}(PF_6^-)^2$ material. Indeed, in a recent publication[195], the Ginger group at the University of Washington reported scanning Kelvin probe measurements of electrostatic potential in LEECs made using a poly(p-phenylene vinylene) with mobile ions. The potential in their study was also found to drop primarily near the cathode. Second, the spatial resolution of our EFM measurement is 200 nm. As we determine the lateral electric field by numerically differentiating the measured electrostatic potential[179], this finite resolution necessarily results in an electric field that peaks at least 200 nm away from the metal electrode. Given an additional ±250 nm uncertainty in the location of the electrode determined from measured capacitance we can locate the peak of the electric field to within only approximately ±450 nm. Fig. 6.4 in the paper shows the field maxima to be 450 nm and 220 nm away from the cathode and the anode, respectively. The measured locations of the electric field maxima are thus entirely consistent with the hypothesis that the electric field peaks right at the contacts.

APPENDIX A

SUBSTRATE PREPARATION RECIPE

The following recipe for creation of substrates in the Cornell Nanoscale Technology and Fabrication Facility was originally adapted by Erik Muller from a recipe from the Malliaras lab to suit the needs of the Marohn group. It has been further modified by Michael Jaquith.

Layer 1 1) Liquid prime with P-20 (20% HMDS) primer. Apply over entire wafer, allow to remain 10 seconds, then spin dry at 4000 rpm for 30 seconds.

2) Spin S1813 resist at 4000 rpm for 30 seconds (producess $\sim 1.3\ \mu$m of resist)

3) Bake on hot plate at 90°C for 90 seconds.

4) EV620 - Choose 5 inch mask chuck and 4 inch wafer chuck. Select first layer mask (gates electrodes only - clean mask with acetone and IPA). Follow directions for soft contact. Expose for 11 seconds.

5) Develop in 300 MIF for 60 seconds. Rinse thoroughly in DI water and dry with N_2

6) (Optional) Hard bake for 60 seconds at 115°C, or 20-30 minutes in oven.

7) Etch oxide on Oxford 80 RIE (CHF_3/O_2, 2:1 to resist, $\sim$ 25 nm/min)

8) Etch silicon on Oxford 80 RIE (Nitride CF_4, $\sim$ 40 nm/min)

9) Strip resist with 1165 bath for 10 minutes, rinse thoroughly in DI water, dry with N_2

Layer 2 10) Liquid prime with P-20 (20% HMDS) primer. Apply over entire

wafer, allow to remain 10 seconds, then spin dry at 4000 rpm for 30 seconds.

11) Spin S1813 resist at 4000 rpm for 30 seconds.

12) Bake on hot plate at 90°C for 90 seconds.

13) EV620 - Choose 5 inch mask chuck and 4 inch wafer chuck. Select first layer mask (source-drain-gate electrodes only - clean mask with acetone, then isopropanol). Follow directions for soft contact. Expose for 11 seconds.

14) YES Oven-Ammonia (NH_3) bake. Run process #2 for 80 minutes.

15) HTG flood expose for 60 seconds (no mask).

16) Develop in MF 321 for 60 seconds. Rinse thoroughly in DI water and dry with N_2. (Optional descum with O_2 for 2 minutes in plasma etcher.)

17) Descum - Branson or Oxford 80 RIE

18) (optional - for recessed electrodes) Oxide-etch in Oxford 80 RIE. (must descum first!, step 17)

19) CHA thermal evaporator - Load wafers, chrome and Au (ebeam). Evaporate 50 ÅCr followed by 500 ÅAu.

20) Strip resist in acetone for at least 4 hours. May require overnight. Rinse thoroughly in DI water and dry with N_2

APPENDIX B

XY PIEZO STAGE CONSTRUCTION NOTES

The following is an addition to Erik and Bill's thesis. It will help avoid many possible problems while constructing and XY Piezo stage using S-bender piezos.

Building an xy piezo scanning stage is much more complicated than is suggested in the available theses of Bill and Eric. While their rough procedure is accurate, there are several additional tips that will save one a great deal of time and frustration when trying to build a scanner stage. Read the entire instructions before beginning the process, many steps have a time requirement. If you are rebuilding the scanner, make sure to remove the sapphire plate from the inner top base piece before proceeding. This can be done by sonication in acetone.

First, construct a fiber interferometer motion detection system using the optical stage. What you need is 1. A way to test the direction a piezo is going all by itself, 2. a way to test the direction a piezo is going when it is glued to the top half of the scanner stage, and 3. a way to test the motion of the final scanner stage. This can all be done with a fiber optic cable run through a long thin tube, with the tube attached to the moving optical stage. You then need to find a way to attach the other components. A single piezo can be attached by using two optical-stage "L" pieces together, pinching the piezo in between. If the piezo is attached to a heavy piece of metal, it does not need to be secured directly to the stage, but that is recommended. Make sure that the entire assembly is placed upon a piece of foam before testing to reduce noise to useable levels. With careful positioning and consistent attachment, a very good signal to noise can be achieved. All that is necessary, however, is the ability to recognize a single fringe in the laser intensity signal.

Before performing any other steps, test the piezos individually. I used a pair of magnets crossing the top of the piezo to reflect the laser signal. Do not assume that they are marked correctly from the factory, or that the orientation of the wires determines the direction of bending - this second factor is most assuredly not true. My method was to use a marker to mark on the red-wire side - marking the edge of the piezo that moves towards the fiber under the application of positive voltage to the red wire. (The white wire is grounded.) This determination is much more difficult than one might initially assume. Because of the subtleties of angles (the metal tube holding the fiber is never perfectly straight, the magnets are never perfectly parallel, and the piezo does not move precisely towards and away from the tube), it is very possible (and quite likely) to get a false result. The things I found were necessary to counter this were:

1. Test both positive and negative voltage application, ensuring that the opposite response is gathered. 2. Test at multiple fiber-magnet distances, ensuring that you have multiple signal strengths. All tests will not necessarily agree. 3. You will know when you have the correct test when you see a significant change (¿20%) of signal intensity in both directions. (20% smaller moving away, 20% larger when moving towards) and multiple fringes 4. Readjust the magnets and tube positions at least once to make sure you are getting the right signal. I can not underemphasize the importance of this test - the entire scanner success depends upon it.

Once you have successfully orientated the piezo pieces, you can begin the gluing process. Make sure that you have ample light (I recommend a fiber light). Using too much glue will cause later problems - especially on the top outer scan base. Too much glue on this piece will cause it to crack when screwed into the stage holder.

If you apply the glue incorrectly, immerse the makor piece entirely in acetone, remove the glue (you can wait $\sim$ 15-20 min and remove the glue manually, or wait several hours and it will be fully dissolved), and start over. It is best to do this before the piezo ever touches the base, or the acetone will remove the marker from the piezo. When you are gluing the pieces, it does not matter if you do the outer or inner top scan base piece first, both must be done. I found success in trying to line the first piezo perpendicular, then using tweezers to install the second piezo. Then, use the secondary base makor piece to fix the distance between the free ends of the two piezos. This must be done quickly, while the superglue is still drying at the top scan base pieces. Glue only one scan base piece at a time, because you need to leave the secondary base sitting on the free ends of the piezos for at least 10 minutes. I have seen the piezos move if the secondary base is not kept in place. Important: The secondary base is not square. The orientation does matter. I recommend that the smaller dimension of the secondary base be used when positioning the free piezo ends of the inner top base piece.

Do not attempt to join the two top base pieces until the superglue has had at least 30 minutes to dry. I recommend more than an hour. Joining the two pieces will stress the piezos, and the piezos can be broken in this process. If you have orientated the secondary base so that the inner top base piece used the smaller dimension of the secondary base, then the two pieces will fit together much more easily. This process is best accomplished by straightening the wires of the inner base piece piezos so that the wires are parallel with the long edge of the piezo. I recommend putting a small amount of superglue on the inner wire-piezo attachments of both pieces before sliding the two pieces together - the inner piezo sides are inaccessible after joining. The superglue will help avoid a wire being broken off later. Slide the two pieces together slowly and carefully, do not stress

the piezos or they can break. Often, if they feel they cannot get in, wiggle them back and forth to help them slide through. Once the pieces are together (inner top base piece is inside the outer top base piece) you are ready for the attachment of the secondary base.

The secondary base can be extremely difficult to attach. The process is made amazingly easier with the use of an alignment device. Erik constructed a device that will correctly position the inner and outer top base pieces relative to each other, it is in one of the drawers of the desk, aluminum, with four raised slots and 3 screw holes. Make sure that the sapphire plate is removed from the inner top base before attempting to use this device. If desired, this is a good time to test that you correctly determined the orientation of the piezos. If you got one wrong, you are still in time to fix it without major time requirements. The test process is similar to above, but the piezos are attached to the makor stage, which can simply rest on the optical stage.

The secondary base is attached by first carefully selecting the wires that must pass through the hole of the secondary base. Slide the secondary base down to the piezos, and ensure that it fits easily into the prepared orientation. Then, I used tweezers on the inside hole of the secondary base, applying pressure apart to hold the secondary base still. You need to apply superglue to all four edges of the secondary base, then quickly maneuver it into position inside the four piezo edges. You have very little time to do this - I strongly recommend you practice the maneuver several times using only tweezers before you apply the glue. Once the secondary base is glued into place, press it firmly into position then leave it to dry for an hour. This is also a good time to apply a small amount of superglue to the outside edge of the piezos at the piezo-wire junction, to strengthen the wires

and prevent them from being broken off.

At this point, you can test the performance of the stage. This is can be done before or after you have soldered up the connections to a pin connecter. I believe it is faster to solder first, then test. The time required to connect alligator clips successfully to two piezo wires is considerable. Soldering the piezo wires to the pin connector wires (made beforehand) is greatly assisted with a bit of tape to hold them all together in close proximity, and a bit of flux applied to the wires before applying solder. Do not forget to place the plastic heat-shrinks on the wires before soldering. Do not shrink them until the stage is finished though. If you test the stage and find that it works in both directions, you are nearly done. If you get a false test, don't panic. The first step is to ensure all electrical connections. Next, mount a multimeter in parallel with the applied voltage, to verify that the actual delivered voltage is accurate. I had an issue with grounding between the x red wire and y white wire that nearly caused me to start over incorrectly. Also, the amps sometimes don't work right - just make sure the voltage delivered is correct. If you have the correct electrical connections and the voltage is delivered, but the stage isn't working then you likely have orientated a piezo incorrectly. Place the entire stage into acetone, and let all the joints dissolve overnight. Do not attempt to separate the piezo-makor connections prematurely, they should fall apart when dissolved.

If you have a successfully working stage, then you are at the final step - gluing the sapphire plate into place. While this seems a trivial step, screwing up now means you must start over. This glue step is significantly different from all previous gluing experiences. Because of the high surface area of the sapphire plate, you are unable to move it whatsoever the moment it touches the superglue. There is

no time of adjustment, the sapphire plate must be placed exactly in the correct position. I recommend using a tool in the center hole of the plate (a tweezers end or doubled-wire will work), and using that to lower the plate precisely into position. It is imperative that you practice this maneuver several times before using the glue. Once this is done successfully, you can heat-shrink the plastic covers for your solder joints, and you are done.

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