INTEGRATION OF PHOTODETECTORS AND OPTICAL RECEIVER FRONT-END CIRCUITS

A Thesis

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ABSTRACT

As computing systems and communication networks grow more complex, so is the need for higher bandwidth data links. Optical interconnect promises to offer lower-cost, high-bandwidth data communication at a lower cost than electrical equivalents.

This thesis investigates two different implementations of optical receiver front-end circuits with photodetectors to take advantage of the unique properties of inexpensive mature CMOS technologies.

The first optical receiver integrates a SiGe phototransistor monolithically with the front-end circuits in a 0.18µm BiCMOS technology. This technique enables monolithically integrated detector design and lowers manufacturing cost. It also enables detectors with smaller parasitic effects to help boost the receiver performance. With the phototransistor, we measured an receiver operation speed of 1 Gb/s.

The second design implements a 10 Gb/s receiver in a 0.25µm silicon-on-sapphire technology with a flip-chip bonded commercial photodetector. We take advantage of the lower parasitic in devices and various circuit techniques to achieve the 10 Gb/s operation. This is the first reported 10 Gb/s optical receiver front-end with photodetector and limiting amplifiers implemented in a 0.25µm technology.

These receiver implementations demonstrate ways to take advantage of mature commercial technologies in designing optical receiver front-end circuits to achieve high-performance, low-cost optical links.

BIOGRAPHICAL SKETCH

Paul Cheng Po Chen was born in Yunlin, Taiwan, Republic of China, in May 1983. Paul attended elementary school in Tainan, Taiwan. After completing elementary school, he immigrated to the United States with his family in the summer of 1995. From 7th to 12th grades, he attended Mid-Pacific Institute. After graduating from high school in 2001, he attended Cornell University in the College of Engineering and majored in Electrical and Computer Engineering. During his undergraduate studies, Paul took a 1-year leave after freshman year to help kick-start a family business endeavor in helping Chinese people learn the English language.

During his senior year, Paul started working with a graduate student, Anand Pappu, in Professor Alyssa Apsel's research group on research projects. After graduating in May of 2006 with the B.S. degree, Paul entered the Cornell Graduate School in pursuit of the Master of Engineering degree in ECE.

After one semester in the M.Eng. program, Paul decided to switch to the MS/PhD program and worked with professor Apsel to continue research on optical receiver related projects.

To Jennifer Yu Zhao

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CHAPTER 1

INTRODUCTION

Demand for communication and data processing bandwidth has increased along with
higher computing power and network complexity. In many applications, performance
is limited by the bandwidth-length product and the channel packing density of the
electrical interconnects. Using optical interconnects allows for higher bandwidth and
longer lengths due to lower loss, EM interference, and signal distortion. Optical fiber
also provides space and weight savings for highly parallel applications such as
computer networking. A survey of recent developments in communication standards
shows a continuing interest in moving to higher bandwidth links.   The Ethernet
standards from IEEE 802.3 define a 10 Gb/s connection for a range of 80 km over
single mode fiber or 300 m over multi-mode fiber [1.1]. The cheapest electrical 10
Gb/s Ethernet link uses 4 twisted-pairs but is limited to a range of 15 m [1.1].
Additional range can be achieved with more expensive cables and more signal
processing within both the transmitter and the receiver, thus require much higher
power consumption per bandwidth [1.2]. Future standards call for 40 Gb/s and 100
Gb/s on a single link, reflecting the need for higher bandwidth in networking
applications [1.3].

  For applications in distances less than 1 m, electrical transmission lines can be
used with careful impedance matching to provide a high bandwidth link, but the cost
and bulk of the cables can be prohibitive in some consumer applications. Micro
coaxial cables that exhibit 50 Ω transmission line characteristics for low profile
interconnects are available for data rates up to 655 Mb/s, useful in applications such as
flat panel display, handheld mobile devices, and laptop computers [1.4]. Future
demands in multimedia capabilities will require the electrical interconnect to scale up

in parallel channels, where as optical interconnect can offer higher bandwidth per channel as well as superior mechanical stability.

The main challenges for optical interconnect in short range applications in portable devices are low cost integration and low power consumption per unit bandwidth. In this thesis, we explore ways to implement low-power, low-cost Gb/s optical receivers in CMOS technologies to bring optical interconnect closer to the mainstream consumer applications.

In the 1 Gb/s to 2.5 Gb/s data rate range, optical receivers with photodetectors have been implemented in standard 0.25µm CMOS technology [1.5-1.6] and some in silicon-on-insulator technology [1.7]. Other related work demonstrates 2.5 Gb/s operation of either a transimpedance amplifier or a limiting amplifier, but without a detector and no optical measurements [1.8-1.9]. Once 0.18µm CMOS becomes available, various 10 Gb/s receivers were demonstrated [1.10-1.12]. A 10 Gb/s transimpedance amplifier in 0.25µm CMOS has been demonstrated [1.13], however, a full receiver front-end integration with photodetector and limiting amplifier remains elusive.

Attempts to integrate photodetectors with the receiver circuit include many silicon based photodiodes, include lateral p-i-n diodes in SOI technology [1.14-1.15] and bulk silicon CMOS compatible processes [1.16]. These approaches require a high reverse bias voltage of up to 10 V for high speed operation and are not readily available in commercial CMOS processes.

This thesis is based on two conference papers that I authored and published [1.17-1.18]. Chapter 2 is about the monolithically integrated phototransistors with receivers. The integration of the photodetector with the receiver circuit on the same die promises to reduce the overall cost of the optical interconnect system. Chapter 3 investigates the Silicon-on-sapphire CMOS 10 Gb/s receiver with commercial

photodetectors. Combining various circuit techniques, we demonstrate that high performance optical receivers can be designed and fabricated with relatively mature and inexpensive technologies. In addition to these papers, I include an appendix to detail some of the experimental methods and procedures used in these studies.

REFERENCES

[1.1] IEEE Standard 802.3 (http://standards.ieee.org/), 2005.

[1.2] Louis Frenzel, "10 Gbits/s Over UTP? Gimme a Break!", Electronic Design, v. 52, n. 10, pp. 29, May 10, 2004.

[1.3] A. Umbach, "Photoreceivers from 40 Gb/s to 100 Gigabit Ethernet", Conference on Optical Fiber Communication/National Fiber Optic Engineers Conference, San Diego, CA, 2008.

[1.4] Hiromasa Futamata, Yoshinori Satoh, Tatsuya Watanabe, Hiroshi Aoki, Yoshio Nakazawa, Shigeru Kojima, and Yoshio Noda, "Micro Coaxial Cable Assembly", Fujikura Technical Review, n. 31, Jan. 2002.

[1.5] Zhaofeng Xue, Zhigun Li, Zhigong Wang, Mingzhen Xiong, and Wei Li, "Low Noise 1.25 Gb/s Front-end Amplifier for Optical Receivers", Chinese Journal of Semiconductors, v. 27, n. 8, Aug. 2006.

[1.6] P. Mitran, F. Beaudoin, and M. N. El-Gamal, "A 2.5-Gbit/s CMOS Optical Receiver Frontend," IEEE International Symposium on Circuits and Systems, vol. 5, pp. 441-444, 2002.

[1.7] R. Li, J. D. Schaub, S. M. Csutak, and J. C. Campbell, "A High-Speed Monolithic Silicon Photoreceiver Fabricated on SOI", IEEE Photonics Technology Letters, v. 12, n. 8, Aug. 2000.

[1.8] Eduard Säckinger, Wilhelm C. Fischer, "A 3Ghz, 32 dB CMOS Limiting Amplifier for SONET OC-48 Receivers", IEEE International Solid-State Circuits Conference, Dec. 2000.

[1.9] Patrick Mitran, Francis Beaudoin, and Mourad N. El-Gamal, "A 2.5-Gbits/s CMOS Optical Receiver Frontend", IEEE International Symposium on Circuits and Systems, v. 5, May 2002.

[1.10] W. Chen and D. Lin, "A 90-dBΩ 10-Gb/s Optical Receiver Analog Front-end in a 0.18-μm CMOS Technology," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 3, pp. 358-365, March 2007.

[1.11] Jie Jin, Jun Feng, Zhi-Wei Sheng, Zhi-Gong Wang, "0.18μm CMOS Limiting Amplifier for 10 Gb/s Optical Receiver", Acta Electronica Sinica, v. 32, n. 8, Aug. 2004.

[1.12] Rui Tao, Manfred Berroth, "10 Gb/s CMOS Limiting Amplifier for Optical Links", IEEE Solid-State Circuits Conference, Sept. 2003.

[1.13] D. Guckenberger, J. D. Schaub, and K. T. Kornegay, "A DC-coupled Low-power Transimpedance Architecture for Gb/s Communication System Applications," IEEE Radio Frequency Integrated Circuits Systems, pp. 515-518, 2004.

[1.14] B. Yang, J. D. Schaub, S. M. Csutak, D. L. Rogers, and J. C. Campbell, "10-Gb/s All-Silicon Optical Receiver", IEEE Photonics Technology Letters, v. 15, n. 5, May 2003.

[1.15] Min Yang, Jeremy Schaub, Dennis Rogers, Mark Ritter, Ken Rim, Jeffery Welser, Byeongju Park, "High Speed Silicon Lateral Trench Detector on SOI Substrate," IEDM Tech. Dig., 2001, pp. 547-550.

[1.16] S. M. Csutak, J. D. Schaub, W. E. Wu, J. C. Campbell, "8 Gb/s CMOS Compatible Monolithically Integrated Silicon Optical Receiver", Fiber Communications Conference, March 2002.

[1.17] Paul C. P. Chen, Anand M. Pappu, Alyssa B. Apsel, "Monolithic Integrated SiGe Optical Receiver and Detector," Conference on Lasers and Electro-Optics (CLEO) 2007, talk CTuZ4, Baltimore, Maryland, May 8, 2007.

[1.18] Paul C. P. Chen, Anand M. Pappu, Zhongtao Fu, Woradorn Wattanapanitch, Alyssa B. Apsel, "A 10 Gbps Optical Receiver in 0.25 μm Silicon-on-Sapphire CMOS," International Symposium of Circuits and Systems, talk A1L-K.4, Seattle WA, May 2008.

CHAPTER 2

MONOLITHICALLY INTEGRATED SIGE OPTICAL RECEIVER AND

DETECTOR[1]

2.1 Introduction

High performance electronics with electrical interconnects are becoming more expensive to manufacture due to the physical limitations of metal wires and the subsequent complexities. Issues such as crosstalk, signal propagation delay, and power consumption are becoming the bottlenecks of many systems. Low cost optical interconnect, already used in long distance telecommunication networks and automotive systems, is becoming an attractive alternative to electrical interconnect for shorter distances [2.1].

Optoelectronic devices fabricated in material systems such as gallium arsenide or germanium have high cost due to the material and the extra processing steps necessary to integrate with other silicon parts [2.2,2.3]. Figure 2.1 illustrates the difference between conventional and monolithically integrated photodetector schemes in receiver designs. We present a monolithically integrated photodetector to be included in the receiver substrate. Furthermore, silicon p-n and p-i-n diode detectors have been used in recent designs to lower production cost. In order to operate at high speeds with high responsivity, silicon photodiodes require a high reverse voltage supply, adding complexity to the receiver design. The SiGe photodetector in this study requires only 1.8V to operate, which we designed and integrated with an optical receiver circuit to run at 1 Gb/s.

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[1] The contents of this chapter was published in [2.8]

(a)   (b)

Figure 2.1 (a) Conventional detector integration, i.e. flex, wirebond, or flip-chip bond.

(b) Monolithically integrated detector.

2.2 Phototransistor

The detector in our optical receiver is a modified heterojunction bipolar transistor (HBT) with an exposed emitter for vertical coupling of light [2.4]. It is based on the stock HBT in IBM's BiCMOS process, thus making it easily integratable with the rest of the receiver circuit. The SiGe HBT used in this study has approximately a 90 nm base graded with germanium from 12% to 0%. The transistor is modified to have an exposed area of 8 x 8 μm^2 to allow free space vertical coupling of light. Figure 2.2 illustrates how the transistor layout needs to be modified to turn this device into a photodetector.

(a)   (b)
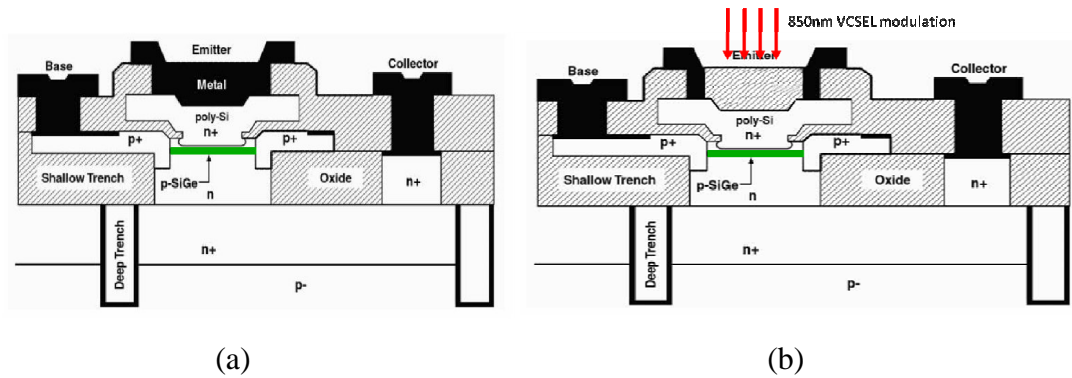
Figure 2.2 (a) Cross section of SiGe heterojunction bipolar transistor before modification. (b) Cross section of SiGe heterojunction bipolar transistor after layout modification to allow vertical optical coupling.

The operation of the phototransistor is similar to a photodiode, but its transistor action and thin base amplifies the photocurrent with small parasitic capacitances, resulting in higher responsivity and bandwidth. Based on previous measurements using impulse optical response and inverse Fourier transform, we calculated the

8

intrinsic bandwidth of this device to be 0.9 GHz [2.4]. The responsivity at 850nm is 2.7 A/W. The responsivity can be further boosted by operating the phototransistor in a high gain region with base biasing. The intrinsic device bandwidth can be as high as 5 GHz for a small device with an optical window of 2 x 2 μm^2 [2.4].

2.3 Performance

We fabricated the integrated optical receiver using IBM's BiCMOS 7wl process with 0.18 μm feature size. The receiver consists of a transimpedance amplifier, 3 post-amplifier stages, and an output driver. The die photo in figure 2.3 shows the detector and the receiver circuit integrated on the same die. The detector device including extrinsic contacts and vias takes up an area of about 18 x 25 μm^2 and the receiver has an area of about 200 x 50 μm^2. The entire receiver can be compactly integrated with other system components for high speed data communication.
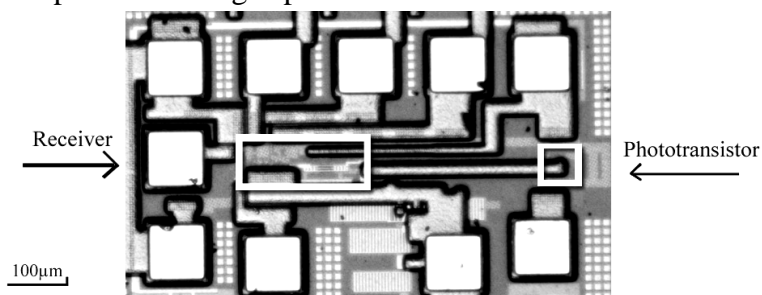

Receiver

Phototransistor

100μm

Figure 2.3 Die photo of fabricated integrated optical receiver

A 850nm high speed laser is modulated and coupled to the detector vertically using a multimode fiber probe. The optical receiver produces signals with peak to peak voltage of 50mV when driving a 50ohm oscilloscope. The eye diagram of the full receiver with optical input is shown in Figure 2.4.
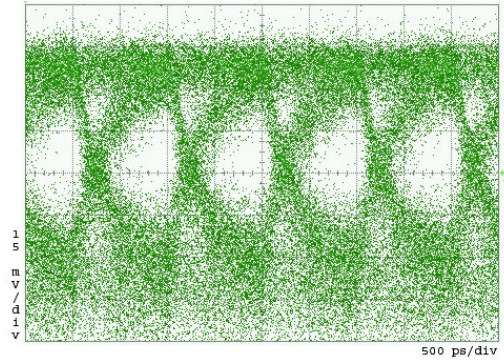
Figure 2.4 Eye diagram from output of optical receiver ($2^7 - 1$ PRBS at 1 Gb/s)

Similar to photodiodes with a low reverse bias voltage, the phototransistor response has a small fast component and a larger slower component in its output current. We believe this is due to the current being absorbed in the collector-substrate junction below the device. This reverse biased junction has a higher capacitance and thus slows down the output current, especially in our collector coupled scheme. The slow part of the response can be observed clearly in Figure 2.5, where we provide a 500 MHz square wave input and see the waveform contains a fast transient followed by a slow tail.

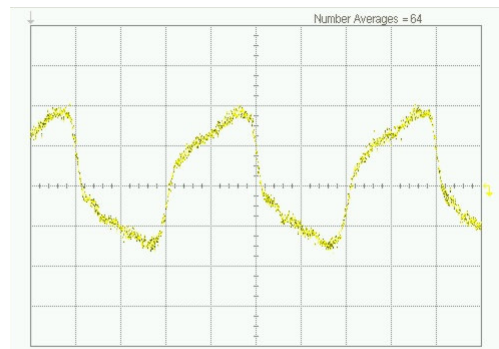Figure 2.5 Optical receiver response with 500 MHz square wave input.

We reduce the impact of the slow response by AC coupling between the detector and the front end of the receiver to filter the low frequency response of the photodetector. When we test the receiver circuit without the photodetector and only with electrical inputs, we see that the receiver is capable of 3.5 Gb/s operation (Figure

2.6), further confirms that the phototransistor's intrinsic bandwidth is the limiting factor.

2⁷-1 PRBS eye diagram
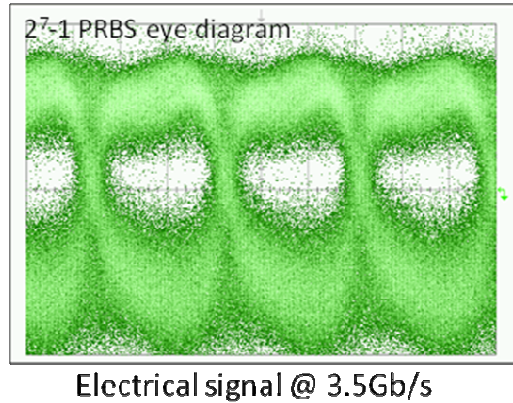
Electrical signal @ 3.5Gb/s

Figure 2.6 Optical receiver eye diagram at 3.5 Gb/s with electrical input.

In the test circuit, the phototransistor base is left open, and a single supply of 1.8 V is used to bias the phototransistor collector and to power the rest of the receiver. It is shown running on a 1.8 V supply, although the detector only requires 1.3V for high speed operation. To the best of our knowledge this is the first monolithic Gb/s optical receiver in a commercial process that requires a voltage supply below 5 V and no post-processing [2.5-2.7].

2.4 Conclusion

The monolithically integrated optical receiver in this study presents the first Gb/s receiver using a commercially available SiGe process with a low supply voltage of 1.8V. Previous works required higher supply voltages which add cost and complexity. With no extra post-processing steps and a simpler power supply, this integration scheme lowers the cost of the optical receiver and makes it more suitable for high speed low power optoelectronic systems in short distance applications.

REFERENCES

[2.1] Anand M. Pappu, "Analysis of Intrachip Electrical and Optical Fanout," Applied Optics, v 44, n 30, 6361-6372, (2005).

[2.2] Kai Ma, Ray Chen, David Miller, and James S. Harris, Jr. "Novel On-Chip Fully Monolithic Integration of GaAs Devices With Completely Fabricated Si CMOS Circuits," IEEE Journal of Selected Topics in Quantum Electronics, v 11, n 6, 1278-1283, (2005).

[2.3] Gitty N. Nasserbakht, James W. Adkisson, Bruce A. Wooley, James S. Harris, and Theodore I. Kamins, "A Monolithic GaAs-on-Si Receiver Front End for Optical Interconnect Systems," IEEE Journal of Solid-State Circuits, v 28, n 6, 622-630, (1993).

[2.4] Yao Yin, Anand M. Pappu, and Alyssa B. Apsel, "Low-cost, high-efficiency, and high-speed sige phototransistors in commercial bicmos," Photonics Technology Letters, v 18, 55-57, (2006).

[2.5] T. K. Woodward and Ashok V. Krishnamoorthy, "1-Gb/s Integrated Optical Detectors and Receivers in Commercial CMOS Technologies," IEEE Journal of Selected Topics in Quantum Electronics, v 5, n 2, 146-156, (1999).

[2.6] Kamel Ayadi, Maarten Kuijk, Paul Heremans, Gerhard Bickel, Gustaaf Borghs, and Roger Vounckx, "A Monolithic Optoelectronic Receiver in Standard 0.7-µm CMOS Operating at 180 MHz and 176-fJ Light Input Energy," IEEE Photonics Technology Letters, v 9, n 1, 88-90, (1997).

[2.7] R. Li, J. D. Schaub, S. M. Csutak, and J. C. Campbell, "A High-Speed Monolithic Silicon Photoreceiver Fabricated on SOI," IEEE Photonics Technology Letters, v 12, n 8, 1046-1048, (2000).

[2.8] Paul C. P. Chen, Anand M. Pappu, Alyssa B. Apsel, "Monolithic Integrated SiGe Optical Receiver and Detector," Conference on Lasers and Electro-Optics (CLEO) 2007, talk CTuZ4, Baltimore, Maryland, May 8, 2007.

CHAPTER 3

A 10 GB/S OPTICAL RECEIVER IN 0.25 MICROMETER

SILICON-ON-SAPPHIRE CMOS[2]

3.1 Introduction

Increasing demand for data communication bandwidth in short-distance applications has fueled a growing interest in finding low cost solutions for optical interconnects. High speed receivers have been demonstrated using GaAs, InP, and silicon BiCMOS technologies [3.1-3.3]. Cost and CMOS compatibility issues justify a continued search for an inexpensive CMOS solution. Although integration of the optical receiver in CMOS compatible technologies allows easy integration with other CMOS system components, its slower devices pose challenging design trade-offs not encountered in other bipolar technologies or material systems.

This paper presents an integrated optical receiver in a 0.25μm silicon-on-insulator (SOI) CMOS process operating at 10 Gb/s under optical testing. To the best of our knowledge, this is the first complete optical receiver front-end design with photodetector, TIA, and limiting amplifiers, in a CMOS 0.25μm technology capable of operation at 10 Gb/s.

3.2 Receiver Architecture

We designed and fabricated an optical receiver in the 0.25μm ultra-thin silicon-on-sapphire (SOS) technology developed by Peregrine Semiconductor [3.4]. Similar to other SOI processes, SOS CMOS transistors are fabricated on a 100 nm layer of silicon supported by an insulating sapphire substrate, reducing parasitic capacitance, body effect, and substrate crosstalk between devices. Figure 3.1 shows a cross-sectional diagram of the SOS CMOS technology.

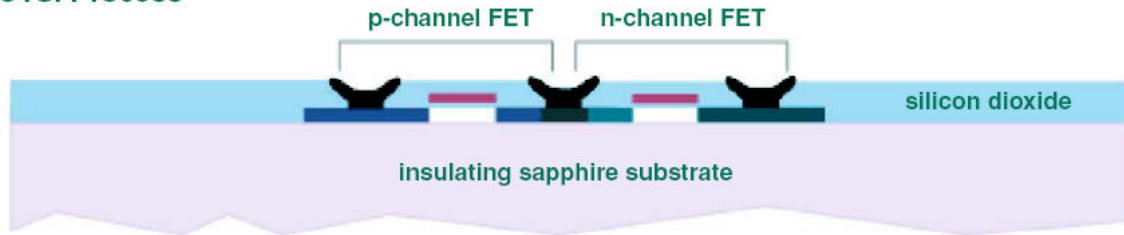[2] The contents of this chapter was published in [3.13]

Figure 3.1 Silicon-on-sapphire CMOS technology.

This technology allows dense integration of high speed transceivers suitable for optical interconnect arrays. The transparency of the sapphire substrate enables simple flip-chip integration of optoelectronic devices such as photodetectors and vertical cavity surface emitting lasers (VCSEL). Optical signals can couple and transmit through the die with little loss [3.4, 3.5]. The primary benefits of the SOS technology for our receiver design are the reduced parasitic capacitance of the input devices and the inductors. This characteristic enables faster charging and discharging of high speed nodes.

The implemented receiver front-end shown in Fig. 3.2 consists of two photodiodes forming a differential input, AC coupled to a common-gate differential transimpedance amplifier (TIA). The photodiodes are GaAs p-i-n diodes from Emcore with 250 fF of parasitic capacitance. The output of the TIA is amplified by two stages of limiting amplifiers (LA) and the output buffer drives external 50 Ω loads.
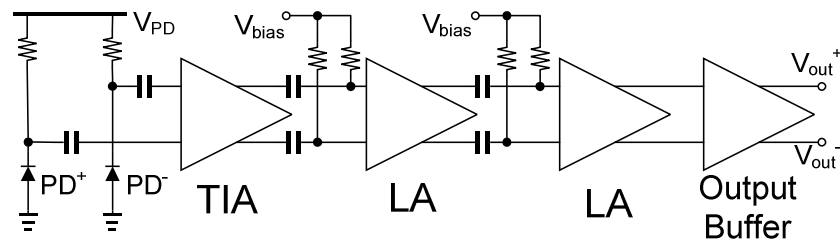

Figure 3.2 Optical receiver block diagram.

3.3 Transimpedance Amplifier

The TIA circuit is shown in Fig. 3.3(a). It uses a common-gate topology with AC coupled inputs, making the TIA truly differential. This open-loop topology was chosen to isolate the low impedance input node from the output node and maximize the amplifier bandwidth, which is limited by the f_T of M_3 and M_4. The differential architecture has additional benefits of power supply rejection, increased gain, and dark current rejection. Due to AC coupling, the TIA output is also insensitive to variations in ambient light conditions.

(a)   (b)
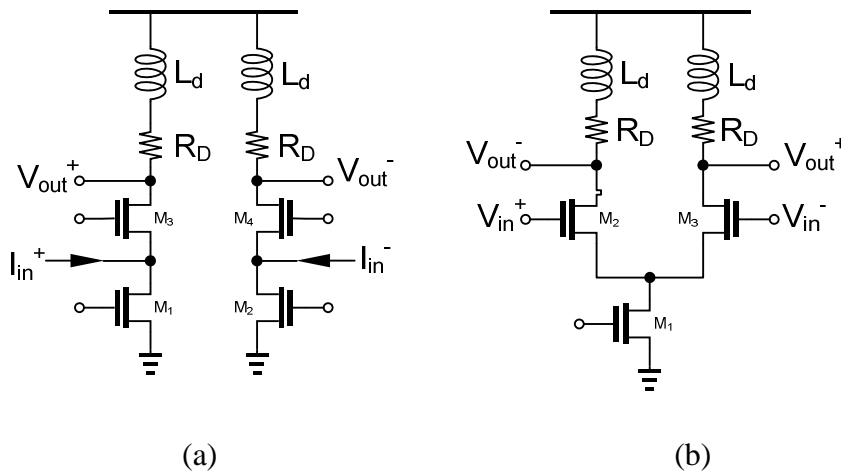
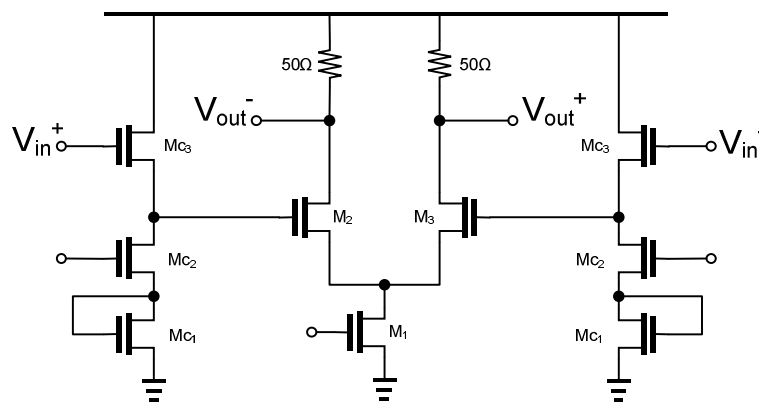Figure 3.3 (a) Differential common-gate TIA. (b) Limiting amplifier.

Figure 3.4 Output buffer.

The TIA bandwidth is limited by its input pole due to the large photodiode parasitic capacitance. The pole can be calculated from the input resistance and the input capacitance:

$$\omega_{in} = \frac{1}{R_{in}C_{in}} \tag{3.1}$$

where C_{in}, the input capacitance, is the sum of the photodiode parasitic capacitance, the gate-to-drain capacitance of M_1, and the gate-to-source capacitance of M_3. The input resistance R_{in} can be calculated by equation (3.2).

$$R_{in} = \frac{r_{o3} + R_D}{1 + g_{m3}r_{o3}} \| r_{o1} \approx \frac{r_{o3} + R_D}{1 + g_{m3}r_{o3}} \tag{3.2}$$

The TIA bandwidth is extended with inductive peaking using on-chip inductors in series with the load resistors. The inductors are picked from a set of available inductors in this process to have an inductance value of

$$L_D = 0.5R_{out}^2 C_{out} \tag{3.3}$$

to achieve a maximally flat frequency response [3.6]. The expression for the output resistance R_{out} is

$$R_{out} = \left(r_{o3} + r_{o1}\left(g_{m3}r_{o3} + 1\right)\right) \| R_D \approx R_D \tag{3.4}$$

and C_{out} includes the limiting amplifier gate-to-source capacitance, the limiting amplifier gate-to-drain Miller capacitance, and the gate-to-drain capacitance of M_3 of TIA. This capacitance is reduced for the SOS process since the drain-to-bulk and the source-to-bulk capacitances are negligible. The inductor was chosen to be 1 nH based on equations (3.3) and (3.4).

The transimpedance gain is given by the following:

$$Z_{T0} = R_D \frac{\left(g_m r_{o3} + 1\right)r_{o1}}{\left(g_m r_{o3} + 1\right)r_{o1} + r_{o3} + R_D} \approx R_D \tag{3.5}$$

We choose a low R_D value of 120 Ω to ensure that the output pole does not affect the TIA bandwidth and that a reasonable L_D can be used.

3.4 Limiting Amplifier

The limiting amplifier topology is shown in Fig. 3.3(b). It is designed for high bandwidth using the same inductive peaking technique as for the TIA. Each limiting amplifier input is AC coupled, which relaxes the DC biasing condition and reduces input capacitance. The limiting amplifiers run on a supply voltage of 5 V instead of the nominal 2.5 V for this process. This feature is unique to SOI technologies because of the lack of the bulk terminal. As long as the potential difference between the source and the drain does not exceed 2.5 V, the higher supply voltage allows us to satisfy the overdrive voltage requirements for the input nFET pair at high current levels. We do not risk transistor failure because the gate-to-source and the drain-to-source voltages are still within the reliability limits, there are no bulk terminal diode breakdown issues, and the supply voltage is split across several devices.

3.5 Output Buffer

The output buffer as shown in Fig. 3.4 consists of a pair of source followers with cascoded current sources followed by a differential amplifier driving external 50 Ω loads. The output buffer runs on a supply voltage of 3.5 V and a source follower is used to lower the higher voltage level from the limiting amplifier output.

3.6 Simulation

From simulation, the TIA has a transimpedance gain of 115 Ω and a bandwidth of 13.8 GHz. The gain of the two cascaded limiting amplifiers is 6.4, giving a total transimpedance gain of 736 Ω. The output buffer has a gain of 0.5 and reduces the circuit bandwidth by about 12%. The AC coupling limits the lower cut-off of the receiver to 5 MHz, which is appropriate for a variety of encoding schemes such as 8b/10b or 64b/66b encoding. The simulated transimpedance gains of the TIA and the receiver without output buffer are shown in Fig. 3.5.
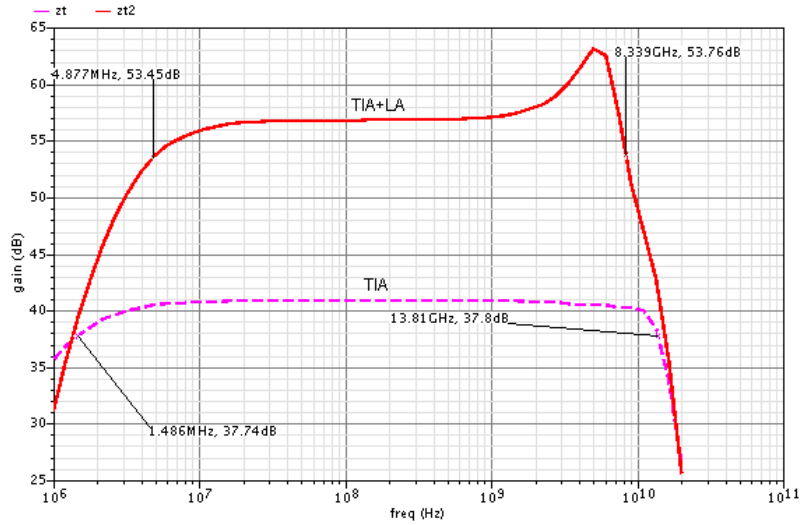
Figure 3.5 Simulated transimpedance gain of the TIA and limiting amplifiers.

The bandwidth of the TIA is 13.8 GHz, and it drops to 8.3 GHz after the limiting amplifiers. There is an emphasis at 6 GHz from inductive peaking. This is used to equalize the attenuation from the output buffer and also the laser source transfer function.

3.7 Experimental Results

Fig. 3.6 shows the fabricated optical receiver with photodiodes flip-chip bonded to the top. The photodiodes are GaAs p-i-n diodes for 850 nm detection. The die size for each detector is 450 μm x 450 μm, and they have a detection aperture of 100 μm. Optical signal is coupled from behind the chip using lensed multimode fiber with a 50 μm diameter spot size. The laser source is an electrically modulated VCSEL coupled to multimode fiber.
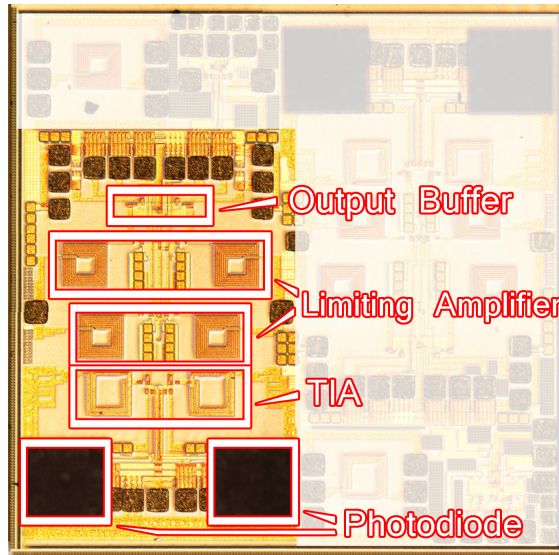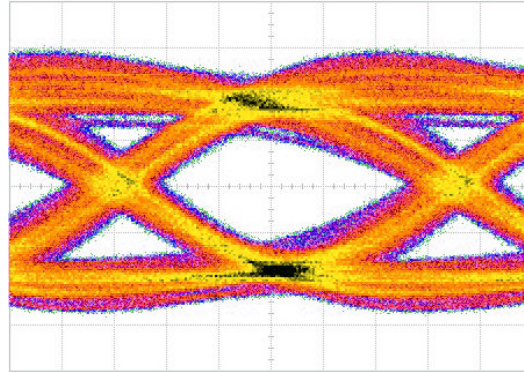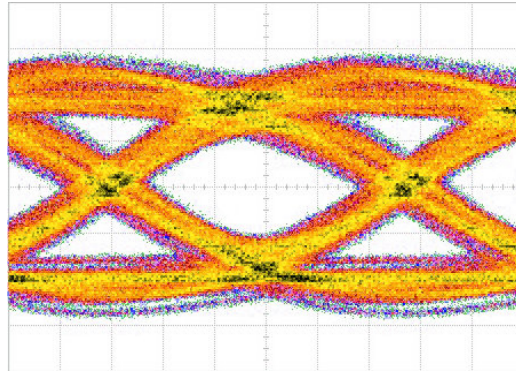
Figure 3.6 Photograph of the integrated optical receiver test chip. The photodiodes are bonded face down. The area shown is 1.5 mm x 2 mm.

A differential non-return-to-zero (NRZ) 2^7-1 pseudo-random bit sequence is applied to the inputs at 8 Gb/s, 9 Gb/s, and 10 Gb/s data rates. Fig. 3.7 shows the resulting eye diagrams.

(a)

(b)
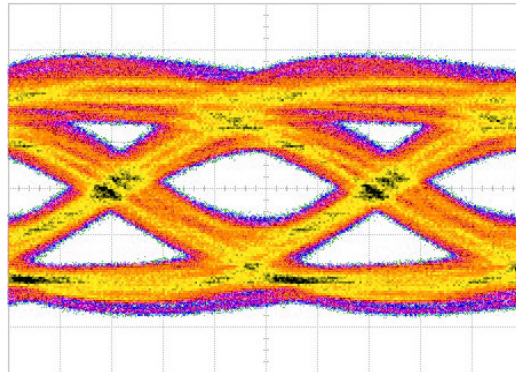
(c)

Figure 3.7 Output eye diagram with 2^7-1 PRBS input, -1.5 dBm optical power. x: 19.3 ps/div, y: 50 mV/div (a) 8 Gb/s. (b) 9 Gb/s. (c) 10 Gb/s.

A bit-error rate (BER) test was also performed to measure the sensitivity of the receiver. As shown in Fig. 3.8, at 10 Gb/s, a BER of 10^{-9} was observed with an average input power of -1.7 dBm for the differential inputs. Sensitivity for BER of

10^{-12} is extrapolated from the measured data and is calculated to be -0.85 dBm. BER for 9 Gb/s and 8 Gb/s are also shown and a BER of 10^{-12} or better was measured.

The differential output swing is about 300 mV for an input current swing of about 840 μA. Assuming an output buffer gain of 0.5, the transimpedance gain before the output buffer is 714 Ω. Power consumption is 20.4 mW for the TIA and 46.9 mW for the two limiting amplifiers.
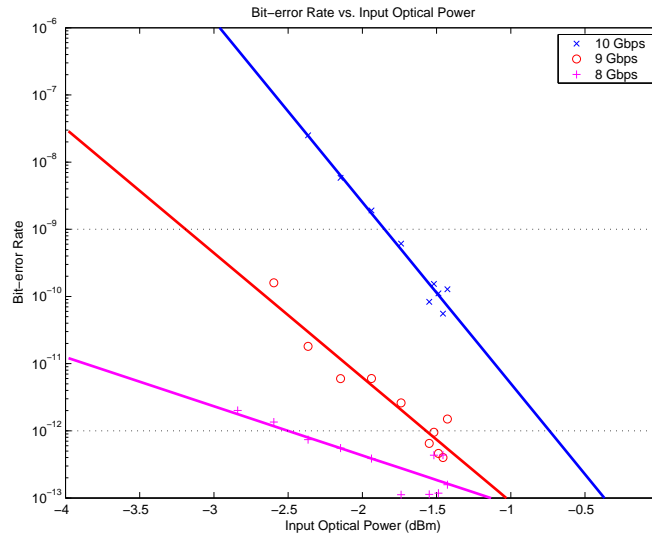
Figure 3.8 Bit-error rate vs. input optical power for 8 Gb/s, 9 Gb/s, and 10 Gb/s.

Table 3.1 compares results from several published optical receivers in similar CMOS technologies. Our TIA has similar transimpedance gain as other TIAs with higher bandwidth, due to inductive peaking and advantages in SOI. Our design demonstrates 10 Gb/s operation of the TIA and limiting amplifier codesign in a relatively low cost 0.25μm CMOS process. Sensitivity of our receiver suffers from significant inter-symbol interference because the system transfer function has peaks near the operating frequency. The design was not optimized for low power consumption, but this TIA topology can be optimized for low power as demonstrated by [3.7].

TABLE 3.1   Comparison of Published Optical Receivers

Design	This Work	[3.7]	[3.9]	[3.10]	[3.11]	[3.12]
Technology	0.25μm SOS CMOS	0.25μm CMOS[a]	0.25μm CMOS	0.25μm CMOS	0.18μm CMOS	0.18μm CMOS
Data Rate (Gb/s)	10	10	2.5	2.5	10	10
TIA gain (Ω)	110	129	-	250	316	1.12k
LA gain (dB)	16	-	32	-	40	-
Total Gain (dBΩ)	57	42.2	-	48	90	61
TIA Bandwidth (GHz)	13.4	8.4[b]	-	1.5	8	7.2
Power Supply (V)	2.5/5[c]	1.5	2.5	2	1.8	1.8
Power (mW) — TIA	20.4	1.6	-	76	164	70.2
Power (mW) — LA	46.9	-	53	76	164	-
Function	PD+TIA+LA	PD+TIA	LA	TIA+LA	PD+TIA+AGC+LA	TIA

a. Fabricated in a BiCMOS process

b. From [3.8]

c. TIA runs on 2.5V & LAs run on 5V

3.8 Conclusions

An optical receiver with a hybrid integration of photodetectors, TIA, and limiting amplifiers has been shown to operate at 10 Gb/s. This is the first optical receiver front-end design including TIA and limiting amplifiers to operate at 10 Gb/s in a 0.25μm CMOS technology.

Integrating the optical receiver in a SOS CMOS technology allows dense integration of optical transceiver arrays using economical hybridization techniques. This receiver is suitable as a low cost building block for high performance short-range optical interconnects and data communication systems.

REFERENCES

[3.1] Y. Amamiya, Y. Suzuki, M. Kawanaka, K. Hosoya, Z. Yamazaki, M. Mamada, H. Takahashi, S. Wada, T. Kato, Y. Ikenaga, S. Tanaka, T. Takeuchi, and H. Hida, "40-Gb/s optical receiver IC chipset – including a transimpedance amplifier, a differential amplifier, and a decision circuit – using GaAs-based HBT technology," IEEE MTT-S International Microwave Symposium Digest, vol. 1, pp. 87-90, 2002.

[3.2] C. Q. Wu, E. A. Sovero, and B. Massey, "40-GHz transimpedance amplifier with differential outputs using InP-InGaAs heterojunction bipolar transistors," IEEE Journal of Solid-State Circuits, vol. 38, no. 9, pp. 1518-1523, September 2003.

[3.3] H. H. Kim, S. Chandrasekhar, C. A. Jr. Burrus, and J. Bauman, "A Si BiCMOS transimpedance amplifier for 10-Gb/s SONET receiver," IEEE Journal of Solid-State Circuits, vol. 36, no. 5, pp. 769-776, May 2001.

[3.4] A. G. Andreou, Z. K. Kalayjian, A. B. Apsel, P. O. Pouliquen, R. A. Athale, G. Simonis, and R. Reedy, "Silicon on sapphire CMOS for optoelectronic microsystems," IEEE Circuits and Systems Magazine, vol. 1, no. 3, pp. 22-30, 2001.

[3.5] A. Apsel, Z. Fu, and A. G. Andreou, "A 2.5-mW SOS CMOS optical receiver for chip-to-chip interconnect," Journal of Lightwave Technology, vol. 22, no. 9, pp. 2149-2157, September 2004.

[3.6] B. Razavi, Design of Integrated Circuits for Optical Communications, McGraw-Hill, 2003.

[3.7] D. Guckenberger, J. D. Schaub, and K. T. Kornegay, "A DC-coupled low-power transimpedance architecture for Gb/s communication system applications," IEEE Radio Frequency Integrated Circuits Systems, pp. 515-518, 2004.

[3.8] D. Guckenberger and K. Kornegay, "Novel low-voltage, low-power Gb/s transimpedance amplifier architecture," Proceedings of SPIE, vol. 5117, pp. 274-285, 2003.

[3.9] E. Säckinger and W. C. Fisher, "A 3 GHz, 32 dB CMOS limiting amplifier for SONET OC-48 receivers," IEEE International Solid-State Circuits Conference, pp. 158-159, 2000.

[3.10] P. Mitran, F. Beaudoin, and M. N. El-Gamal, "A 2.5-Gbit/s CMOS optical receiver frontend," IEEE International Symposium on Circuits and Systems, vol. 5, pp. 441-444, 2002.

[3.11] W. Chen and D. Lin, "A 90-dBΩ 10-Gb/s optical receiver analog front-end in a 0.18-μm CMOS technology," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 3, pp. 358-365, March 2007.

[3.12] C. Wu, C. Lee, W. Chen, and S. Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," IEEE Journal of Solid-State Circuits, vol. 40, no. 2, pp. 548-552, Feburary 2005.

[3.13] Paul C. P. Chen, Anand M. Pappu, Zhongtao Fu, Woradorn Wattanapanitch, Alyssa B. Apsel, "A 10 Gbps Optical Receiver in 0.25 μm Silicon-on-Sapphire CMOS," International Symposium of Circuits and Systems, talk A1L-K.4, Seattle WA, May 2008.

CHAPTER 4

CONCLUSION

Two distinct optical receiver implementations were demonstrated. SiGe BiCMOS technology provides a convenient way to monolithically integrate detector with the front-end receiver circuit without modifying the fabrication processes. This technique eliminates separate detector chip design and fabrication and achieves performance boost through lower detector parasitics. Because the nature of these small SiGe detectors, optical coupling and signal processing are key challenges to achieve data rates in excess of 1 Gb/s.

The silicon-on-sapphire technology provides unique opportunities for optical receiver design using a mature 0.25µm CMOS technology. Using inductive equalization, raised supply voltages, and differential transimpedance amplifier, we were able to demonstrate the first fully integrated 10 Gb/s receiver front-end in a 0.25µm CMOS technology.

I believe these creative uses of mature CMOS technologies will inspire further exploration in making high speed optical interconnect a mainstream technology in future short range communication subsystems. Further advances in packaging, optical fiber alignment and coupling will greatly enhance the viability of new inexpensive optical interconnect systems.

APPENDIX A

MEASURING PERFORMANCE OF OPTICAL RECEIVERS

A.1 Testing Setup

The silicon-on-sapphire (SoS) chip discussed in chapter 3 was designed for free-space back illumination of a differential optical channel. This design poses some challenges when we set it up for measurements in the lab.

Figure A.1 illustrates the bench-top solution I used to obtain results from this receiver chip. The SoS chip is mounted on a printed circuit board with a through-hole that is roughly 4mm in diameter. Because the SoS chip has a transparent substrate and the photodiodes are bonded to the chip faced down, free-space optical fiber probes are mounted and positioned underneath the chip. The fiber probes are aligned with the aid of a video camera looking into a microscope focused from the top onto the SoS chip. A fluorescent lamp is lit from underneath to illuminate the fiber tips, which will come into focus as they move closer to the back-surface of the SoS chip.

Wideband GSG probes are used on the top-surface of the chip to provide electrical connection to the output of the SoS chip. Wirebonds from the chip to the PCB provide power and bias voltages. The fiber probes carry differential optical signals from the pulse generator to drive the inputs of the receiver.
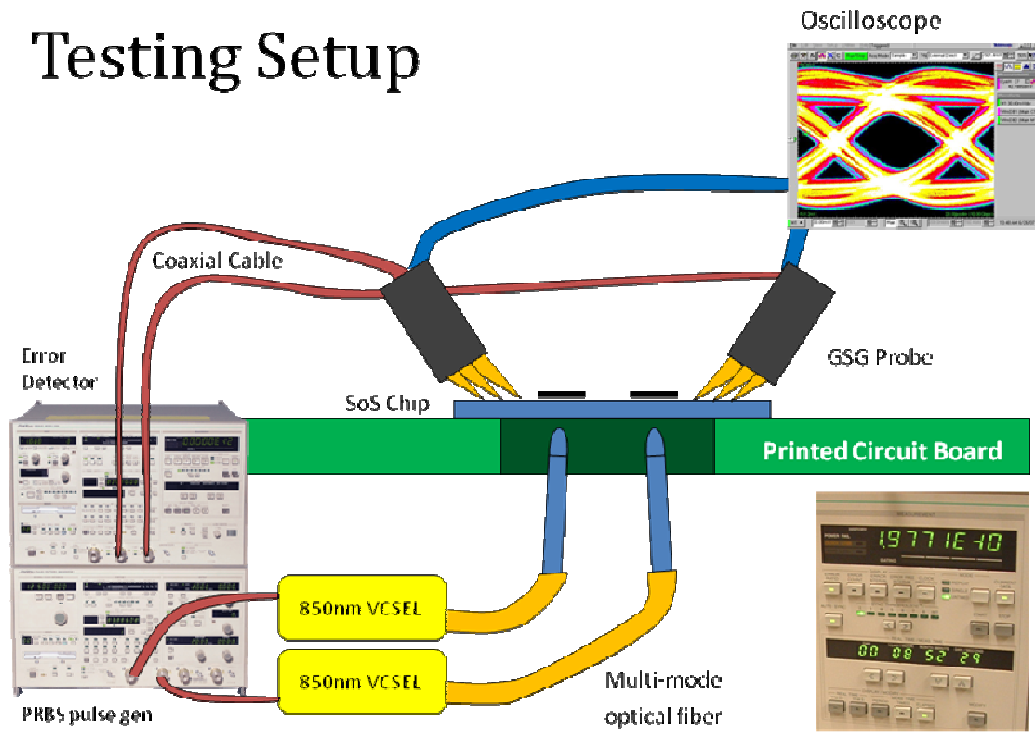
Figure A.1 Testing setup for SoS chip.

A.2 Photodiode

The photodiode used on this chip was a p-i-n GaAs device from Emcore rated for 10 Gb/s operation using 850nm wavelength (Figure A.2). The middle pad is the anode and the outside two pads are the cathode, which should be at a higher bias potential for proper reversed biased operation. This diode measures 450µm on each side, with a detector aperture of 150µm. This aperture is suitable for a multimode fiber tip which generates a spot size of about 50µm.

Testing of the diode confirms its 10 Gb/s operation, as evidenced from eye diagrams in Figures A.3, A.4, and A5 for operations at 1 Gb/s, 5 Gb/s, and 12 Gb/s, respectively. These results were obtained with a reverse bias of 2 V through a bias-T.
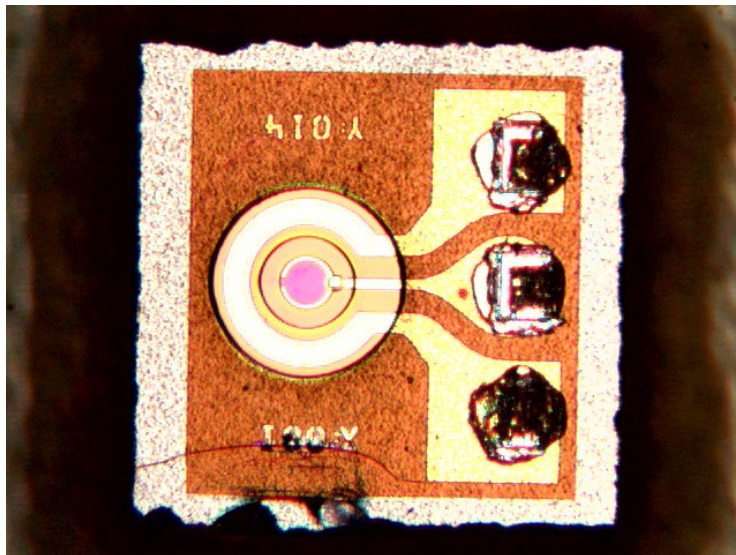
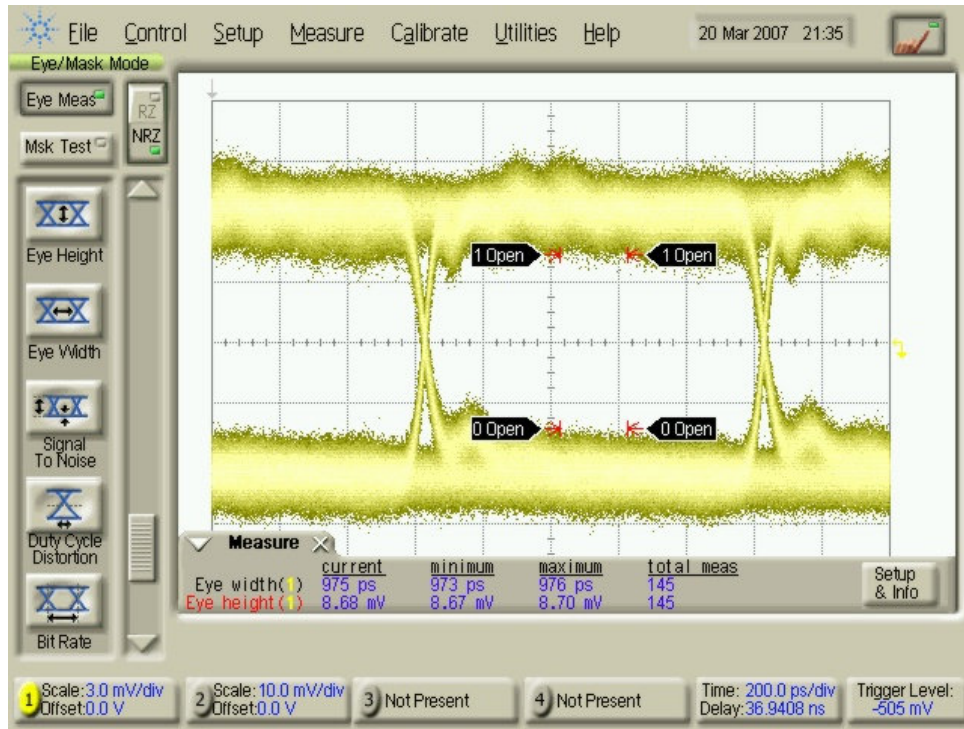Figure A.2 Commercial p-i-n photodiode from Emcore.

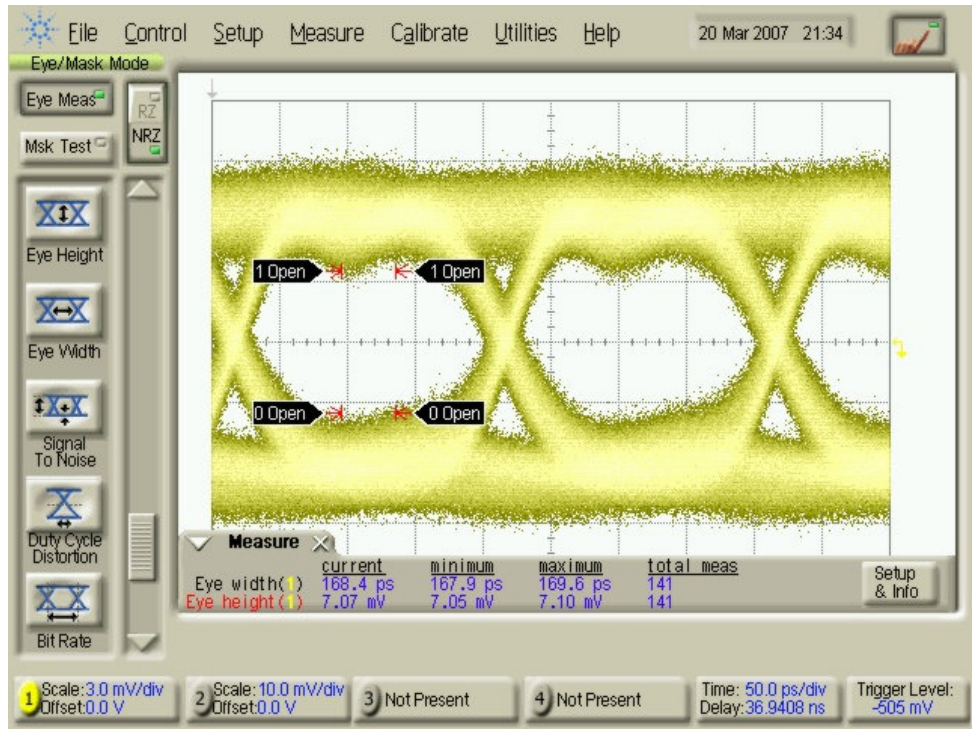Figure A.3 photodiode eye diagram at 1 Gb/s.
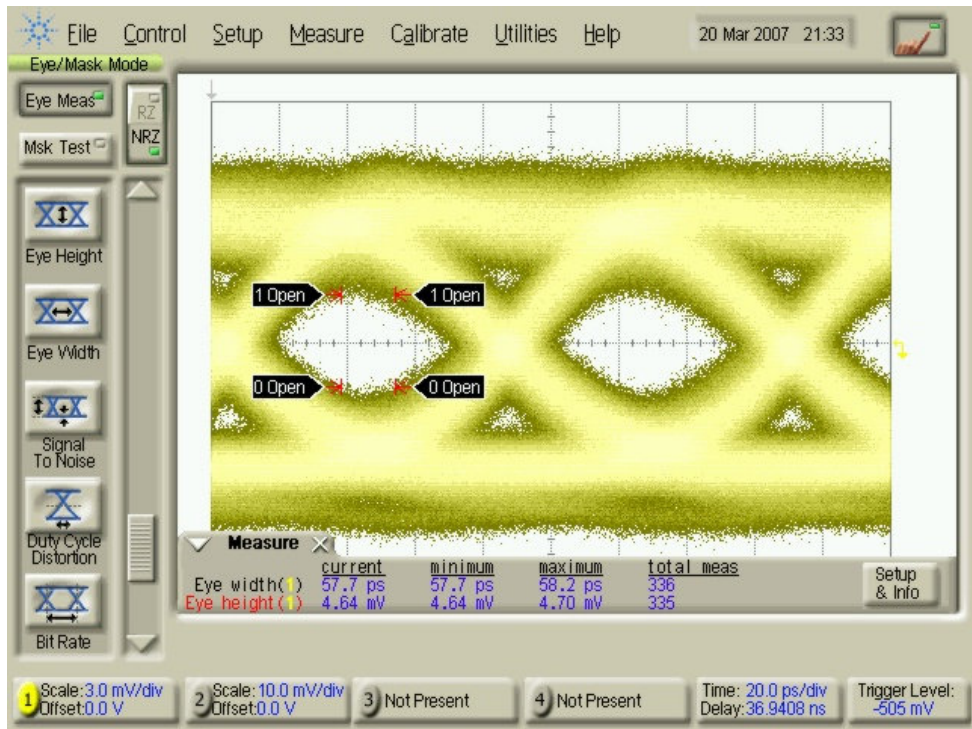
Figure A.4 photodiode eye diagram at 5 Gb/s.

Figure A.5 photodiode eye diagram at 12 Gb/s.

Advances in commercial photodiodes have made photodiodes with backside contacts available. These devices can be bonded to the receiver chip in the same way done with our SoS chip but allow the optical fiber to come in from the top-surface, which would have made testing and packaging easier.

A.3 Bit Error Rate Determination

Even at 10 Gb/s, getting an error ratio for the receiver characterization requires careful tuning and leaving the data collector running for about 8 hours. Figure A.6 shows a typical error count progression over time. We can see that there is a trend of steady rise in error events but also some sudden jumps in error. The error ratio is extracted from these data sets by fitting a line through a portion of the error count history that looks the quietest, thus free from disturbances from factors outside the circuit.
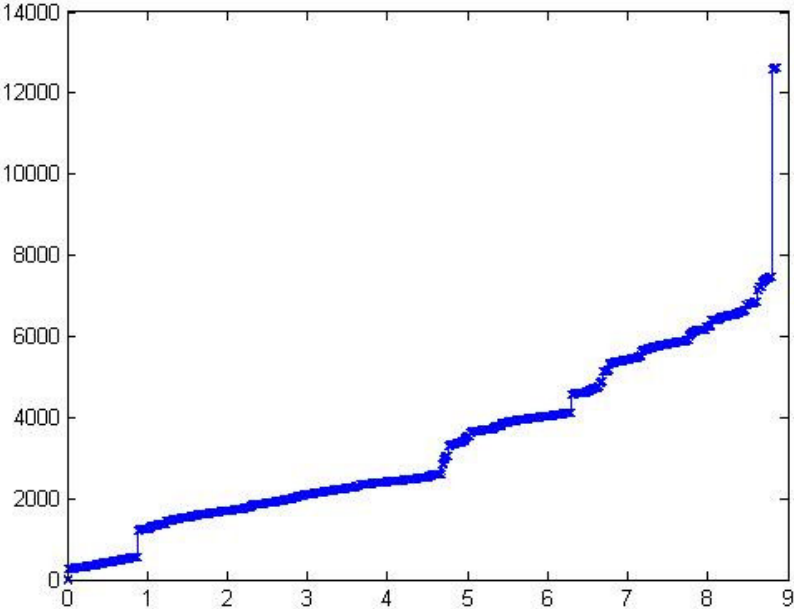

Figure A.6 A typical error count vs. time (in hours) data.

A.4 GPIB communication between MATLAB and Anritsu Error Detector

In order to log the progression of error count over time, I use a Matlab script to poll the error count at fixed intervals and stop after a preset time before storing the result to a file. The set of scripts are documented below. To start logging, run bertstart.m

```
bertstart.m
% this function starts the GPIB communication with the Anritsu BERT machine
clear;                  % remove all workspace variables
instrreset;             % remove all instrument connections and objects
delete(timerfind);      % remove all timer objects
bertHandle = gpib('ni',0,1);
if bertHandle.Status == 'closed'
    fopen(bertHandle);
end
% check to see if we are connected to the right device
fprintf(bertHandle, '*IDN?');
id = fscanf(bertHandle);
if strncmp(id,'ANRITSU,MP1762C',15)
    clear global data;
    clear global data2;
    global data;
    global data2;
    t = timer('TimerFcn',…
        '[data data2] = plotBER(bertHandle,data,data2,starttime);',…
        'StopFcn',…
        'bertloopstop(bertHandle,t)',…
        'Period',…
         5.0,…
        'TasksToExecute',5000);
    t.ExecutionMode = 'FixedDelay';
    t.StartFcn = {@bertloopstart, bertHandle};
%   t.StopFcn = {@bertloopstop, bertHandle,t};
    starttime = now;
    start(t);
else
    display('GPIB Address 1 is not Anritsu MP1762C, exiting')
    fclose(bertHanlde);
end

bertloopstart.m
function bertloopstart(obj, event, bertHandle)
  fprintf(bertHandle, 'MOD 2');
  fprintf(bertHandle, 'STA');

bertloopstop.m
function bertloopstop(bertHandle, t)
fprintf(bertHandle, 'STO');
stop(t);
```

plotBER.m
```
function [data data2] = plotBER(bertHandle,data,data2,starttime)
curData = getBERM(bertHandle);
datapoint = [(curData.t1-starttime)*24 curData.ER];
data = [data; datapoint];
datapoint2 = [(curData.t2-starttime)*24 curData.EC];
data2 = [data2; datapoint2];
if size(get(0,'CurrentFigure')) == 0
else
   figure(1);
   plot(data(:,1),data(:,2),'-');
   figure(2);
   plot(data2(:,1),data2(:,2),'-x');
end
```

getBERM.m
```
% this program reads the error measurements from Anritsu Error Detector
% MP1764C
% function [t1, errorRatio, t2, errorCount, t3, errorInterval, t4, errorFreeInterval, t5,
freq] = getBERM(bertHandle)
function BERdata = getBERM(bertHandle)

[t1, errorRatio] = getEr(bertHandle);
[t2, errorCount] = getEc(bertHandle);
[t3, errorInterval] = getEi(bertHandle);
[t4, errorFreeInterval] = getEfi(bertHandle);
[t5, freq] = getFrq(bertHandle);
BERdata = struct('t1',t1,'ER',errorRatio,...
            't2',t2,'EC',errorCount,...
            't3',t3,'EI',errorInterval,...
            't4',t4,'EFI',errorFreeInterval,...
            't5',t5,'freq',freq);
```

getEr.m
```
% this program reads the error ratio measurement from Anritsu Error Detector
% MP1764C
function [timestamp, errorRatio] = getEr(bertHandle)
fprintf(bertHandle, 'ER?');
timestamp = now;
errorRatio = fscanf(bertHandle,'%s');
errorRatio = cell2mat(textscan(errorRatio,'ER%n'));
```

getEc.m
```
% this program reads the error count measurement from Anritsu Error Detector
% MP1764C
function [timestamp, errorCount] = getEc(bertHandle)
fprintf(bertHandle, 'EC?');
timestamp = now;
errorCount = fscanf(bertHandle,'%s');
errorCount = cell2mat(textscan(errorCount,'EC%n'));
```

getEi.m

```
% this program reads the error interval measurement from Anritsu Error Detector
% MP1764C
function [timestamp, errorInterval] = getEi(bertHandle)
fprintf(bertHandle, 'EI?');
timestamp = now;
errorInterval = fscanf(bertHandle,'%s');
errorInterval = cell2mat(textscan(errorInterval,'EI%n'));
```

getEfi.m
```
% this program reads the error free interval ratio measurement from Anritsu Error
Detector
% MP1764C
function [timestamp, errorFreeInterval] = getEfi(bertHandle)
fprintf(bertHandle, 'EFI?');
timestamp = now;
errorFreeInterval = fscanf(bertHandle,'%s');
errorFreeInterval = cell2mat(textscan(errorFreeInterval,'EFI%n'));
```

getFrq.m
```
% this program reads the datarate measurement from Anritsu Error Detector
% MP1764C
function [timestamp, freq] = getFrq(bertHandle)
fprintf(bertHandle, 'FRQ?');
timestamp = now;
freq = fscanf(bertHandle,'%s');
freq = cell2mat(textscan(freq,'FRQ%n'));
```

A.5 Input Optical Power

When estimating the power incident upon the SiGe photodetector used in Chapter 2, I start by measuring the power coming out from the fiber probe tip using an optical power meter. If we assume the photodetection area is larger than the beam spot size, we still have to discount the optical power due to reflection. Table A.1 shows the calculation of reflected optical power at each interface. Roughly 78% of incident power gets to the detector. Here I assumed the absorption in the air and silicon oxide is negligible.

Table A.1 Reflection and Transmission of Optical Power Through Detector Materials

	Reflective Index	Reflected $\sqrt{\dfrac{n_2 - n_1}{n_1 + n_2}}$	Transmitted
Air	1		100%
SiO2	1.455	3.43%	96.57%
Si	3.65	18.49%	78.71%